Ph.D. DISSERTATION

Highly Efficient Reconfigurable Devices with Programmable Bottom Gate Array

프로그램 가능한 하부 전극 어레이 구조를 갖는 고효율 재구성 가능 소자

BY

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이 논문을 공학박사 학위논문으로 제출함

2016 년 8 월

서울대학교 대학원

전기컴퓨터공학부

박 준 모

박준모의 공학박사 학위논문을 인준함

2016 년 8 월

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ABSTRACT

A novel poly-Si reconfigurable device with programmable bottom gate array having non-volatile memory (NVM) functionality was demonstrated for the first time. The device is very efficient in terms of device size, reliability, uniformity, and reproducibility. By changing bias or program/erase state (PGM/ERS) of the bottom gates (BGs), a device can be transformed to behave one of the following devices: *n*-/*p*-MOSFET, *n*-*p*, and *p*-*n* diode. Threshold voltage (V_{th}) and contact resistance (R_c) of MOSFETs can be controlled independently by the BGs. The subthreshold swing (SS) and I_{on}/I_{off} of the *n*-/*p*-MOSFETs are ~120 mV/dec and $>10^6$, respectively, which are comparable to those of conventional poly-Si devices. Full-swing CMOS inverter logic gates implemented by using two identical reconfigurable devices were successfully demonstrated. Relationship between bottom gate biases and resistance of channel and Schottky junction was investigated by DC *I*-*V*, temperature dependency of I_D, and low frequency noise measurement. Aluminum source/drain (S/D) layer forms Schottky junction with poly-Si body being electrically doped with *n*- or *p*-type, and the current mechanism is dominated by Schottky reverse junction tunneling.

Optimization of fabrication process was performed and stable BG structure

with enhanced uniformity and flatness was achieved. The optimized device demonstrated enhanced PGM/ERS performance and improved on-current characteristics. Gate controllability was also enhanced in the double gate operation with SS of ~90 mV/dec, and I_{on}/I_{off} increased to more than 10^7. A full-swing CMOS inverter and NAND/NOR logic gates implemented by using four identical reconfigurable devices were also successfully demonstrated with complete device isolation by process optimization. The effect of S/D metal and electrical oxide thickness (EOT) of the gate stack on the device characteristics were investigated by both experiments and simulations.

Keywords: Reconfigurable, bottom gate array, NVM functionality, threshold voltage, transformable, PGM/ERS

Student number: 2012-30208

CONTENTS

Chapter 1

Introduction

1. 1 Motivation

The semiconductor technology has been developed in respond to market demand in terms of cost-effective and high-performance, keeping up with Moore's law. To reduce cost, device scaling and fabrication yield have been improved for decades [1]. On the other hand, for better performance, semiconductor industry adopted the FinFETs from the 22 nm technology node (Fig. 1.1 and Fig. 1.2) [2]-[5]. However, semiconductor industry is facing the limit of device scaling with some technological issues, such as photolithography (Fig. 1.3) [6], [7], gate oxide tunneling (Fig. 1.4) [8]-[10], short channel effect [9]-[11] and abrupt junction doping profile [9], [10]. Moreover, even if the technology overcomes such issues, there still exist physical limits such as variability due to random dopant fluctuation (Fig. 1.5) and quantum effects with atomically-scaled material [12]-[15].

In order to overcome the fundamental limits, researchers are searching in the other direction to replace silicon (Si) technology, so called emerging technologies based on novel materials and different mechanisms. A 2-

dimensional materials such as transition metal dichalcogenides (TMDCs) (Fig. 1.6) [16] and graphene [17], and 1-dimensional materials such as carbon nanotube (CNT) (Fig. 1.7) [18], [19] and silicon nanowire (SiNW) (Fig. 1.8) [20] are used as an active layer. Phase change RAM, resistive RAM, magnetoresistive RAM, ferroelectric FET, tunnel FET, and single electron transistor have been demonstrated with new working mechanisms [21-26]. Recently, Intel and Micron have reported a 3D X-Point architecture that can replace FLASH and DRAM technology (Fig. 1.9) [27].

In this thesis, as an alternative to overcome those fundamental limits, we proposed the highly efficient reconfigurable devices with programmable bottom gate array.

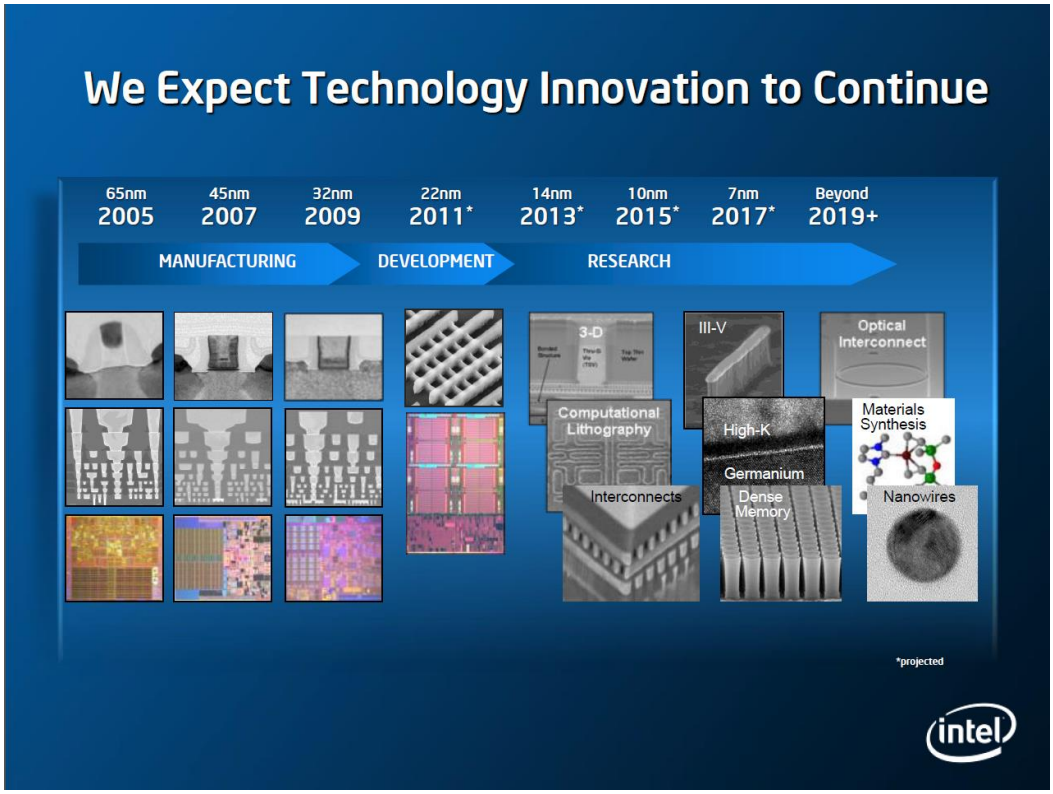


Fig. 1.1. Technology scaling roadmap for 7 nm CMOS and beyond [5].

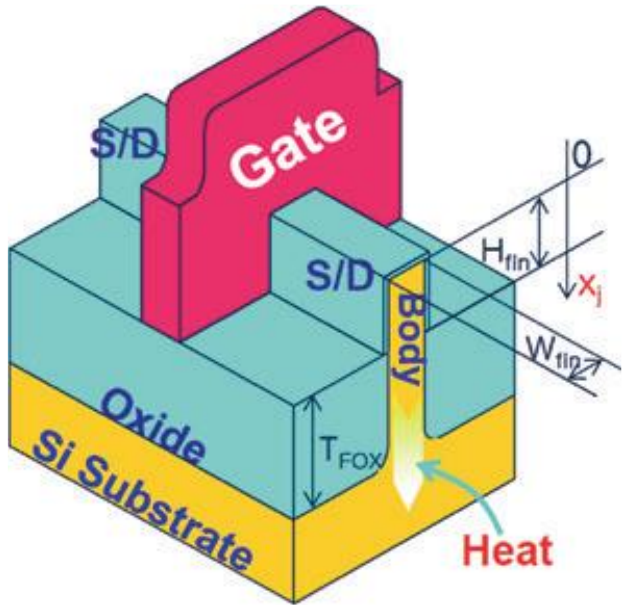


Fig. 1.2. Three-dimensional schematic of bulk FinFET [2].

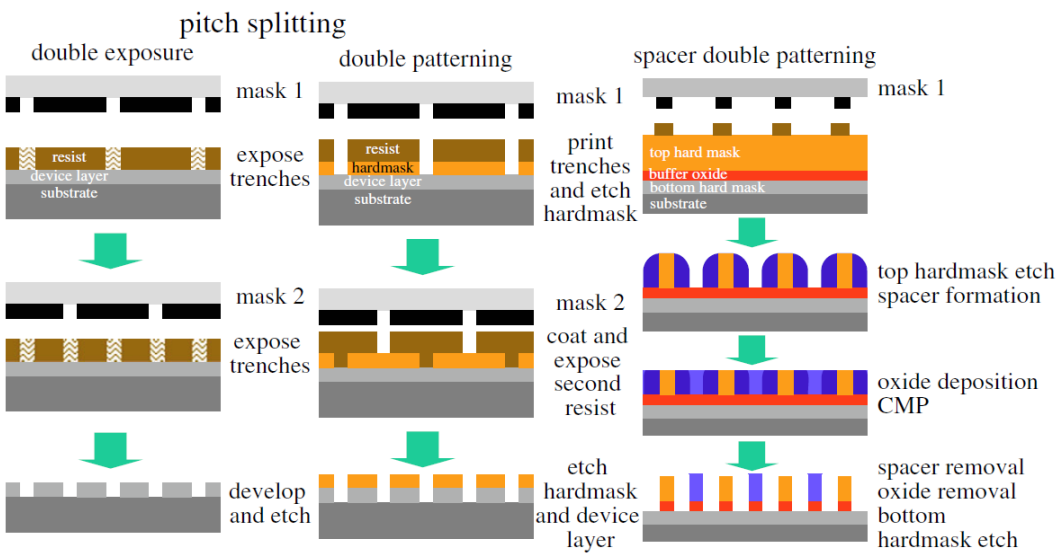


Fig. 1.3. ITRS lithography examples of pitch division or splitting [6].

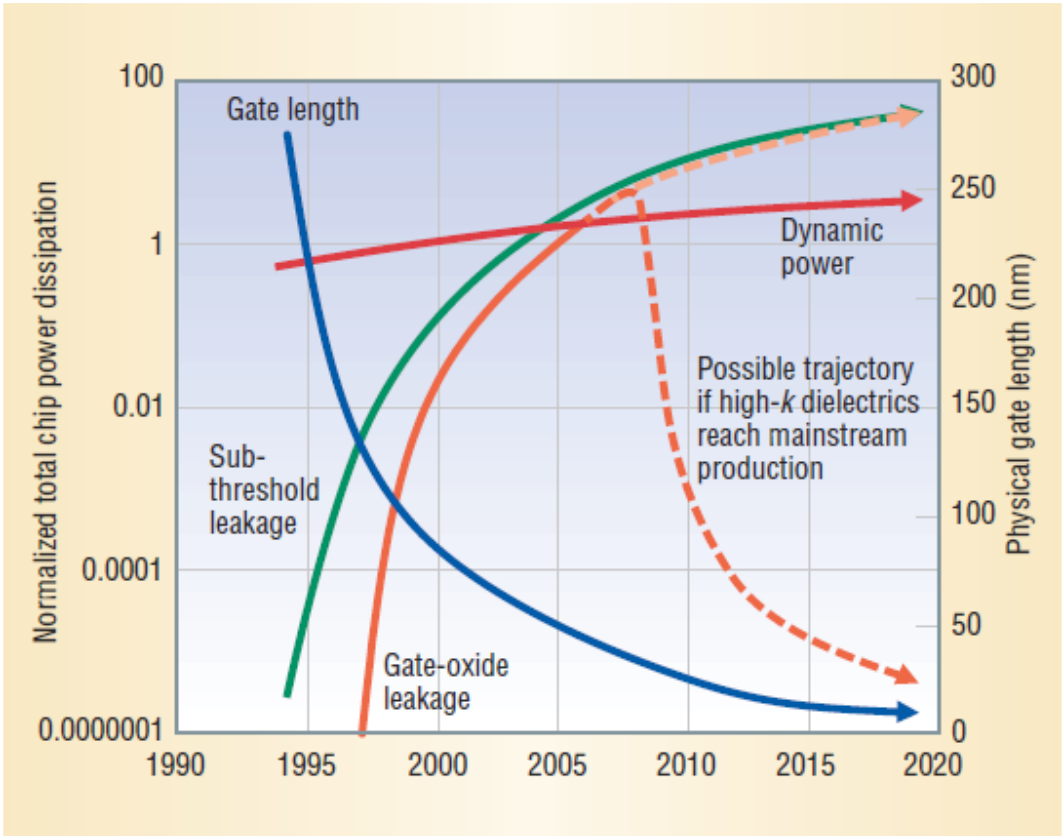


Fig. 1.4. Total chip dynamic and static power dissipation trends based on the International Technology Roadmap for Semiconductors. The two power plots for static power represent the 2002 ITRS projections normalized to those for 2001. The dynamic power increase assumes a doubling of on-chip devices every two years [8].

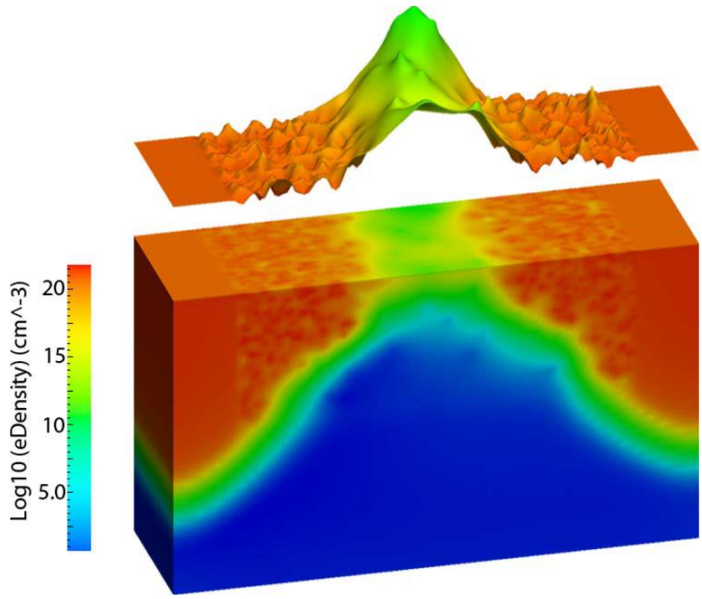


Fig. 1.5. Electron density distribution in the 35-nm device simulated with random discrete doping (RDD), line edge roughness (LER), and Metal gate granularity (MGG) as sources of variability. The surface indicates the potential landscape [15].

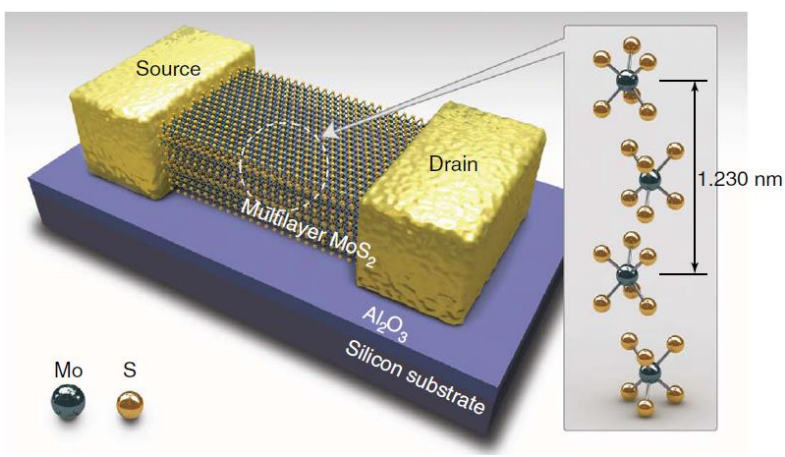


Fig. 1.6. Schematic perspective view of a MoS_2 TFT with a multilayer MoS_2 [16].

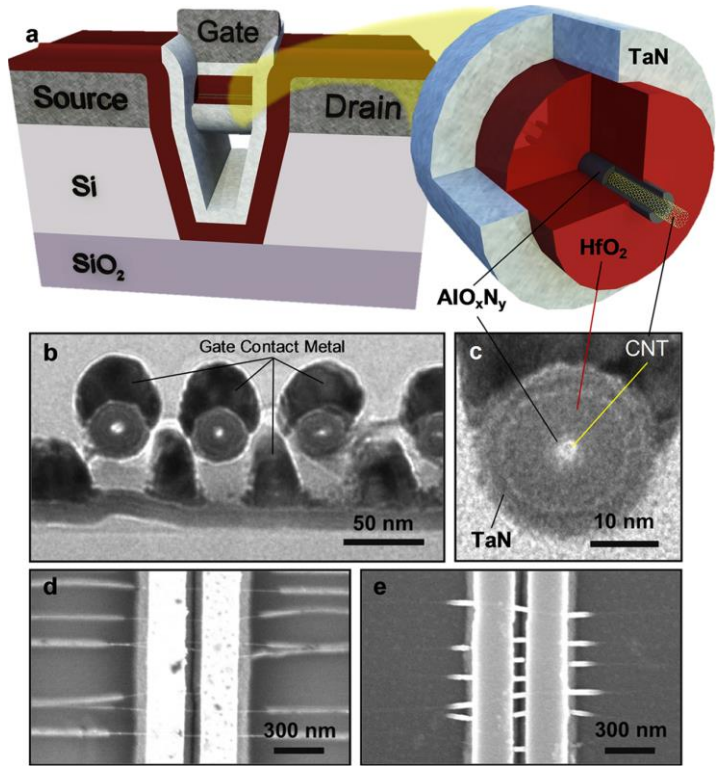


Fig. 1.7. Cross-sectional diagram and TEM image of a GAA CNTFET [18].

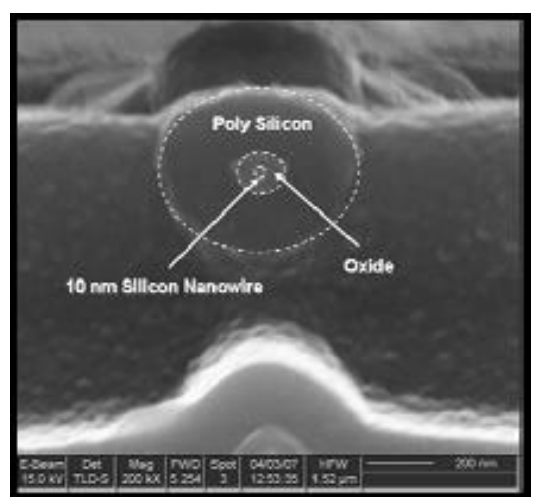


Fig. 1.8. SEM image of the fabricated SNWT with 10nm diameter [20].

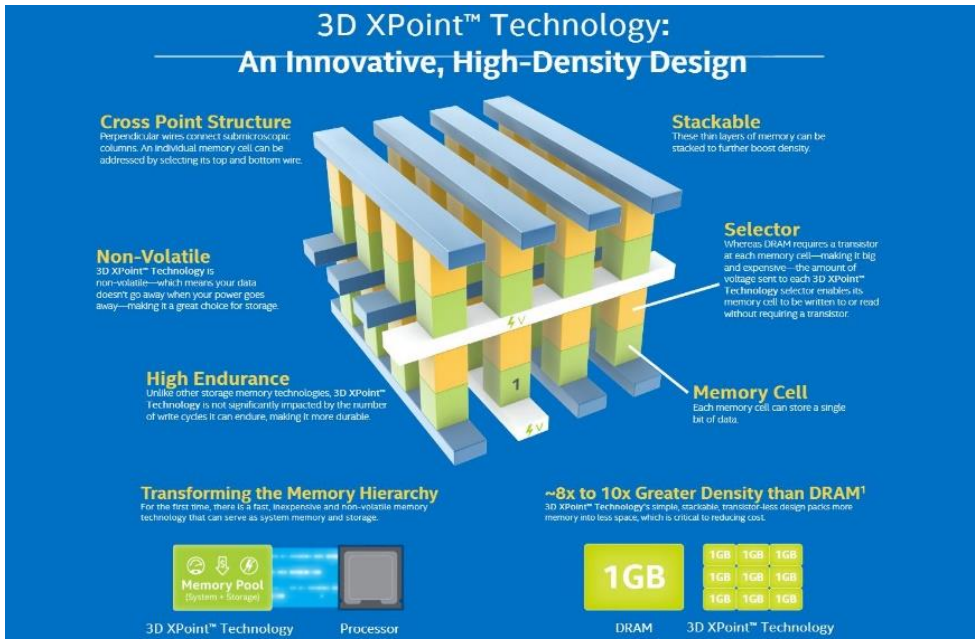


Fig. 1.9. Intel&Micron Xpoint memory [27].

1. 2 Background of Reconfigurable Devices

In parallel to the interest on changing material and mechanism for devices, some researchers have been focusing on increasing functionalities of individual device. There have been some reports on Reconfigurable Field-Effect Transistors (RFETs) (Fig. 1.10 and Fig. 1.11) [28-32]. The RFET is an emerging structure based on Schottky barrier MOSFET (SBMOSFET), and has switchable source and drain Schottky contacts for *p*- and *n*- MOSFETs. Most of the reported RFETs consist of lightly p-type doped SiNW (~10^{15}/cm^3) active layer and at least two gates over the channel and nickel silicide source and drain Schottky contact [28-32]. By changing gate bias, Si nearby Schottky junction is electrically doped to *n*- or *p*-type. When the carrier concentration is large enough, tunneling through Schottky junction occurs, and the junction can be worked as Ohmic-like contact to either *n*- or *p*-type silicon. Since the devices have tri-gate or gate-all-around (GAA) structure, they have a good subthreshold swing characteristics. The RFETs have a clear advantage over conventional Si devices because they can change their device types by biasing each gate on purpose (for example, *n*- to *p*-MOSFET). Moreover, the RFETs require no doping process during fabrication, thus reducing constraints at layout design and excluding device variation due to random dopants such as random dopant fluctuation and abrupt junction profile. By using the RFETs, there have been efforts to build an

effective computational block with functional diversity [30]-[32]. For example, the RFETs reported by Giovanni De Micheli group (Fig. 1.10) [29], [30], [32], which consist of SiNW channel, nickel silicide source/drain, a control gate and two program gates, have common advantage of reconfigurable device that they do not need doping process during fabrication and polarity configuration including dual threshold voltage operation can be achieved (Fig. 1.13 and Fig. 1.14). Furthermore, new logic architectures using RFETs are being developed. Due to the increased functionalities of individual device compared to conventional CMOS technology, it requires fewer resources and can be used to build an effective computational block (Fig. 1.15, Fig. 1.16, and Fig 1.17). The RFETs reported by Walter M. Weber group (Fig. 1.11) [28], [31], which consist of SiNW channel, nickel silicide source/drain, a control gate and a program gates, also have common advantage of reconfigurable device. Similar studies for developing a simple and compact hardware platform using RFETs based on unprecedented circuit design flexibility are in progress (Fig. 1.12).

However, the reported RFETs are using SiNW as a channel material, which gives the issues in process variation, yield and reliability. They also require constant biases to switch a device to *n*- or *p*-MOSFET, resulting in coupling, leakage, and reliability problems. There have been no trials to control the threshold voltage (V_{th}) of the channel region in reported RFETs

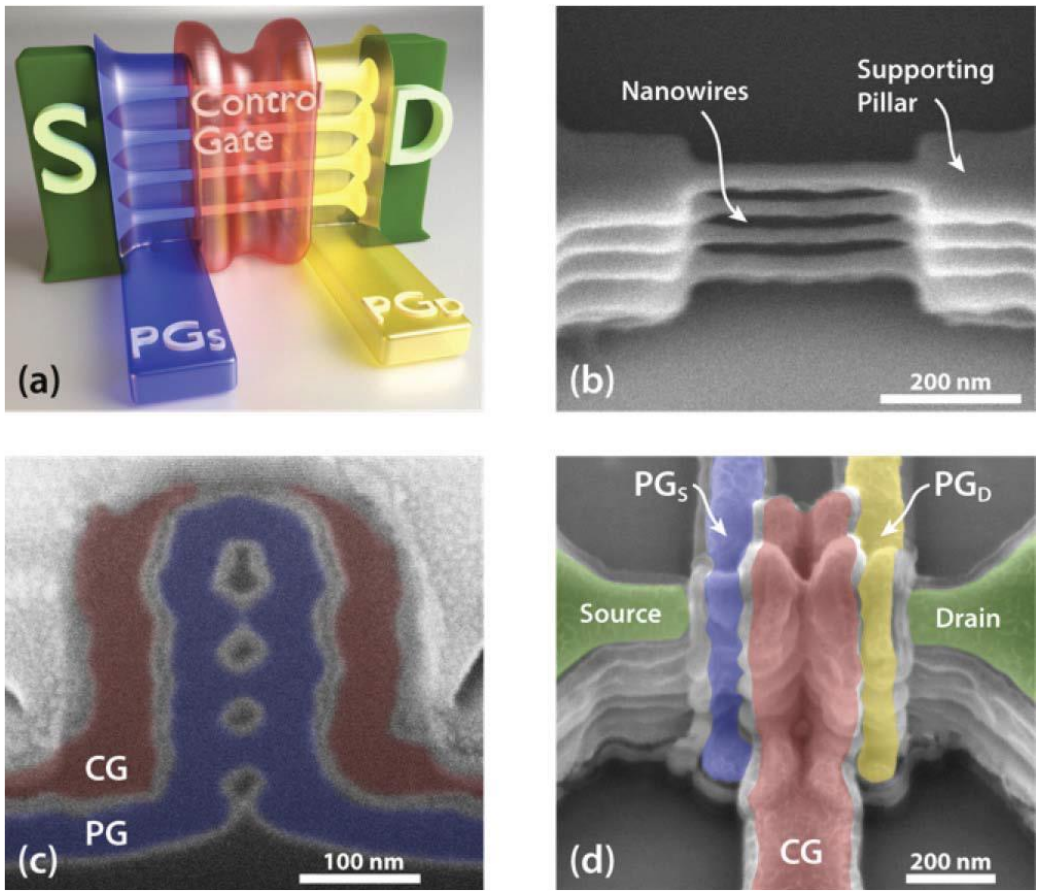


Fig. 1.10. Conceptual sketch and SEM image of a SNWT RFET with three independent gates [32].

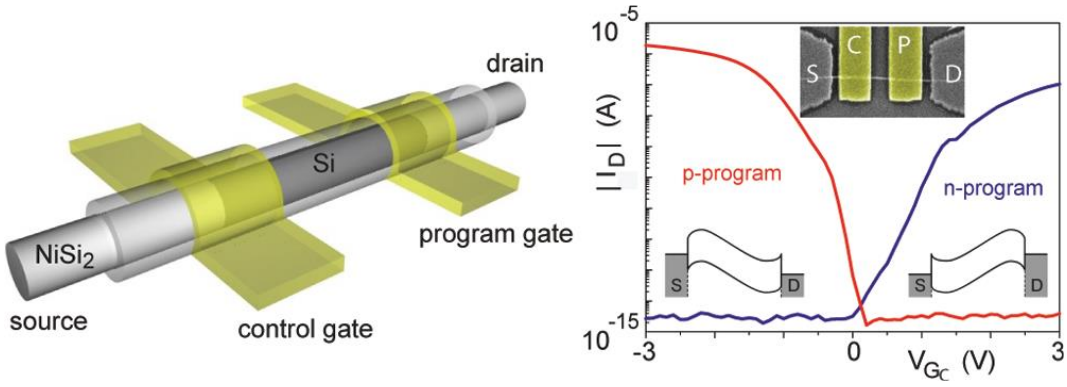


Fig. 1.11. Schematic of a reconfigurable silicon NW FET and its measured transfer characteristics [28].

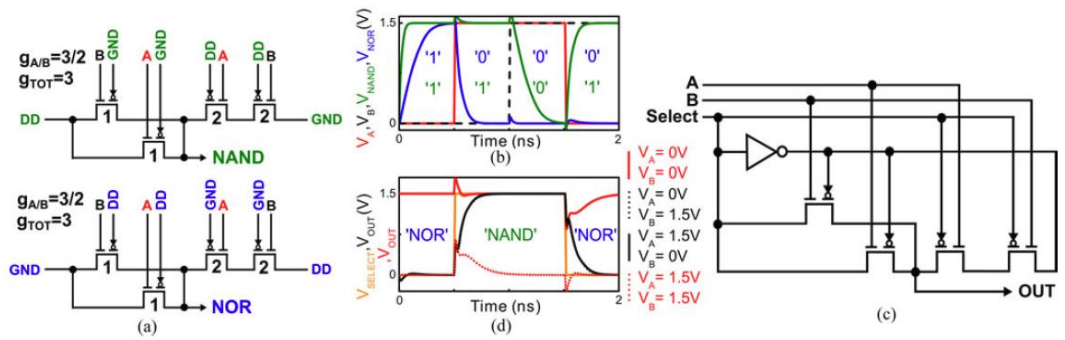


Fig. 1.12. Switching NAND to NOR. (a) A four transistor template circuit, which can be programmed to NAND (top) and NOR (bottom) function. The numbers give capacitances for calculation of the logical effort *g*. (b) Transient simulation of the output signal of both configurations and look-up table. (c) Circuit diagram for a 6-T cell capable of switching between both functions. (d) Transient simulation results of switching the select signal S for all combinations of inputs A and B [31].

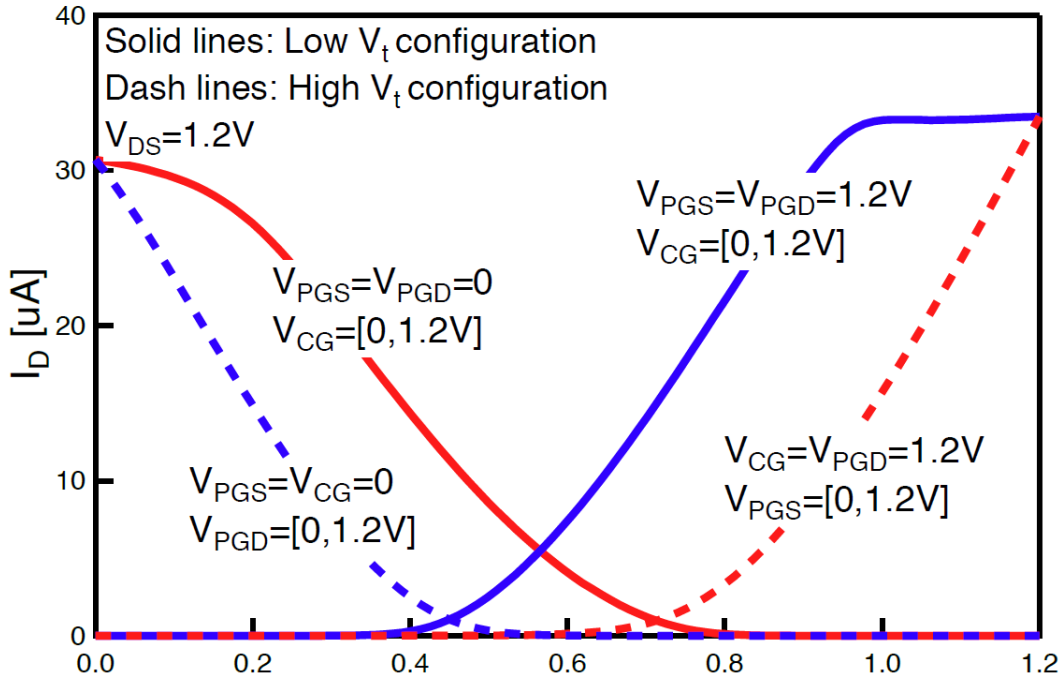


Fig. 1.13. Dual-V_{th} ambipolar characteristic of a single TIG SiNWFET [29].

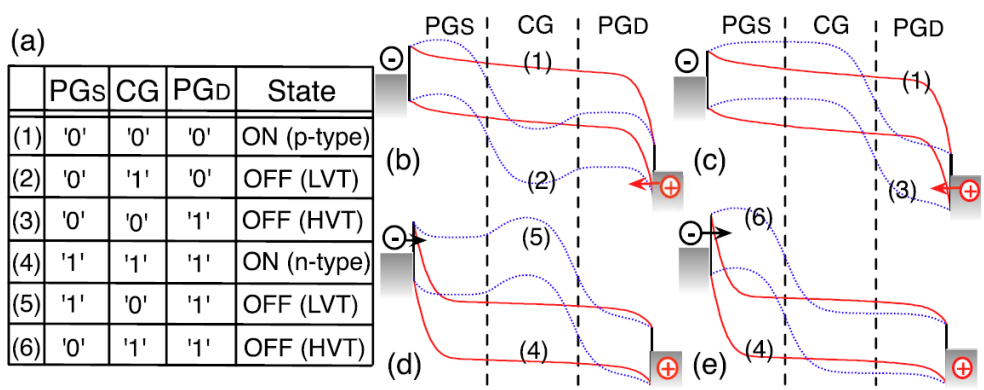


Fig. 1.14. (a) Operation states of fabricated device under different bias conditions. Note that, two other possible configurations do not yield useful operation states. Band diagrams of corresponding configurations. (b) Low-V_{th} *p*-FET. (c) High-V_{th} *p*-FET. (d) Low-V_{th} *n*-FET. (e) High-V_{th} *n*-FET. Numbers: corresponding states in (a) [32].

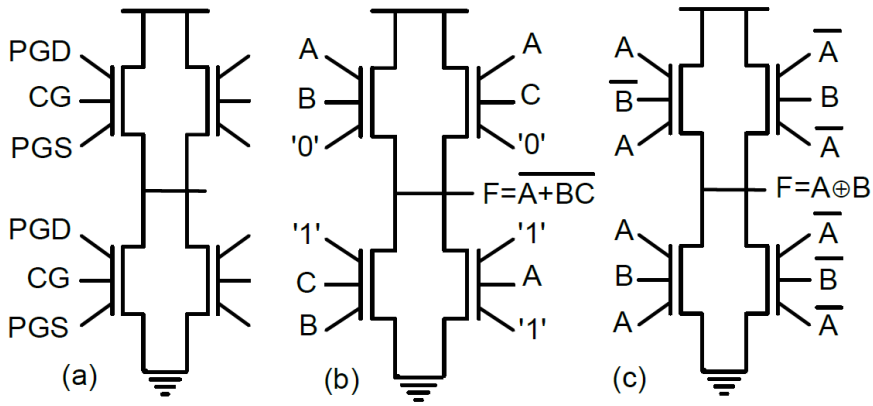


Fig. 1.15. Uncommitted logic gate pattern, (b) AOI gate and (c) XOR gate mapped onto this logic gate pattern [29].

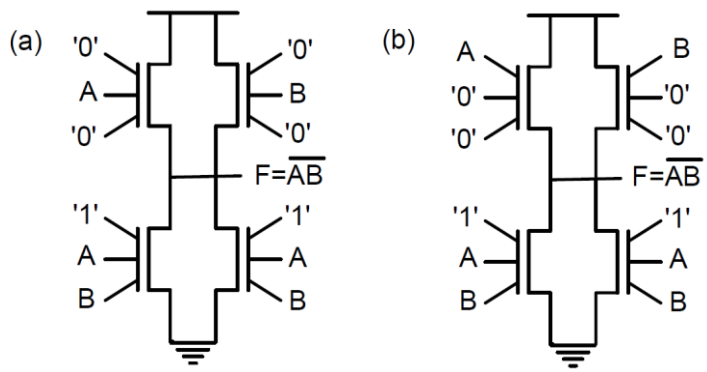


Fig. 1.16. Mapping of NAND gate towards (a) HP (high performance) and (b) LL (low leakage) application [29].

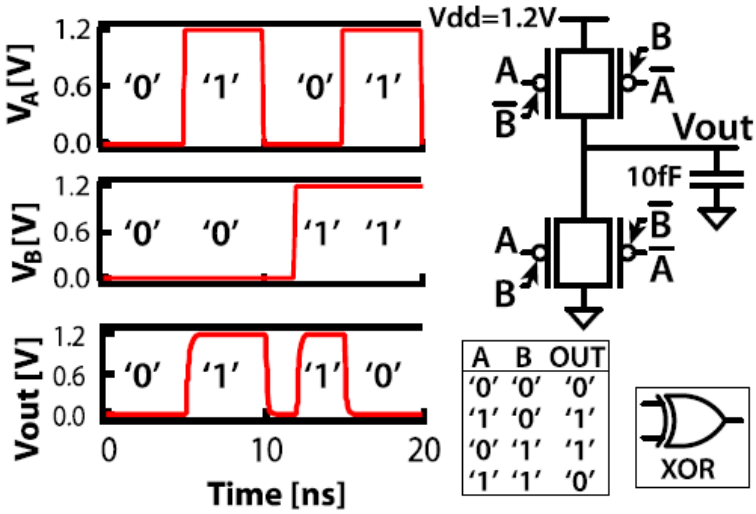


Fig. 1.17. The four-transistor XOR gate is built and simulated by using a table model for the optimized device based on the data extracted from TCAD simulations [30].

1. 3 Thesis Organization

In this thesis, a novel poly-Si reconfigurable device with programmable bottom gate array is demonstrated for the first time and the device physics behind the reconfigurability is characterized. In the chapter 1, the motivation of this thesis including an overview of reported RFETs is provided. In the chapter 2, the structure, advantage, and fundamentals of proposed reconfigurable device are introduced. Chapter 3 provides the fabrication process of the proposed reconfigurable device. Fabrication method for bottom gate formation using nitride spacer and poly-Si CMP are shown with fabrication issues. In the chapter 4, the characteristics of the proposed reconfigurable device are demonstrated. Polarity configuration is shown with *I-V* characteristics of *n*-/*p*-MOSFETs and *p-n*/*n-p* diode operation in a single reconfigurable device. The reconfigurability of the device using programmable bottom gate array is also investigated. In addition, logic gate operations with the proposed reconfigurable devices are demonstrated. In the chapter 5, the Schottky contact resistance of the device is analyzed in detail. The Schottky barrier modulation by bottom gate bias, the temperature dependence of reconfigurable device, and the noise characteristics of MOSFET with bottom gate biases are investigated. In the chapter 6, with the characterization and analysis of the proposed reconfigurable device, we optimized the fabrication process and obtained enhanced performance with

improved Schottky contact resistance. Also, we have researched on the on-current improvement. Finally, we conclude this thesis in chapter 7.

Chapter 2

Proposed Reconfigurable Device

2. 1 Structure and Features of Proposed Reconfigurable Device

A proposed reconfigurable device consists of bottom gate array, O/N/O gate stack, undoped poly-Si body, top gate oxide, a top gate, and source/drain (S/D). Fig. 2.1(a) shows the 3-D schematic of the proposed reconfigurable device. Cross-sectional views of A-A' and B-B' planes are shown in Fig. 2.1(b) and (c), respectively. The proposed device, in common with existing RFETs, can be fabricated without doping process and works as MOSFET and diode in any type by applying biases to the bottom gates and/or by programming/erasing the charge storage node on the bottom gate array. In addition, it is possible to develop new logic architectures using the proposed reconfigurable devices. However, unlike previously reported devices, the proposed device is fabricated by conventional Si complementary metal-oxide-semiconductor (CMOS) technology with only 6 (or 5 when the top gate is omitted) masks, thus the device is CMOS compatible and can be fabricated in a wafer scale without using SOI (Silicon-On-Insulator) wafer and/or e-beam process. These features make

our device very efficient compared to existing RFETs in terms of process variation, yield, cost, reliability, uniformity, and reproducibility. In addition, the device has the smaller area (or better scalability) compared to existing RFETs since the bottom gates are fabricated under the active layer and S/D regions. Note that the existing RFETs have at least two gates over the channel and nickel silicide source and drain Schottky contact [28-32]. The comparison of the feature size among the proposed reconfigurable device in this work and the RFETs proposed by G.D. Micheli and W.M. Weber group is shown in Fig. 2.2 [28-32]. The reported GFETs have a size of 6F (G.D. Micheli [31]) or 8F (W.M. Weber [28]), however, our device has a size of 6F (with top gate) and can be reduced to 4F (without top gate). The n^+ poly-Si bottom gates (BGs) can be used for metal wiring, resulting in simplified integrated circuit design. With a simple change in the process design, the number of bottom gate array can be increased to have increased functional diversity, therefore, the proposed device has the potential to be applied to various field (e.g. neuromorphic system). Furthermore, the noticeable advantage of the proposed device is the O/N/O gate stack between the bottom gate arrays and the active layer, resulting in the non-volatile memory (NVM) functionality. By introducing the non-volatile memory functionality, we can program (PGM) and erase (ERS) the storage layer on the bottom gates. Thus the device can be transformed to one of device types among *n*-/*p*-MOSFETs, *n*-*p* and *p*-*n* diodes without applying additional biases to the bottom gates, therefore,

the coupling, leakage, and reliability problems can be reduced. By using NVM functionality, the symmetric *I*-*V* characteristics for *n*-/*p*-MOSFETs which is important factor for circuit configuration. In addition, the proposed devices are suitable for the design of unrecognizable circuit (*i.e.* security circuit) thanks to the reconfigurable characteristics by PGM /ERS of the BGs. Another advantage of the proposed device is that it has a top gate electrode as well as the bottom gate array. The device can be operated by using the gate in the center of the bottom gate array as a switching gate. We can also use the top gate as a switching gate and the bottom gate as a V_{th} control gate. In addition, the double-gate operation is also possible by using both top and bottom gates simultaneously. Finally, the reconfigurable device with various channel material (e.g. CNT, graphene, TMDCs, crystalline Si by SOI transfer, and IGZO, etc.) can be investigated by using the bottom gate array architecture of our device as a platform of the reconfigurable device (Fig. 2.3). In addition, taking advantage of our separated bottom gate structure, the contact property of TFT can be analyzed and characterized. Moreover, since the device is isolated from the silicon substrate by the silicon oxide, the proposed device can be easily applied to the flexible device by using transfer printing techniques.

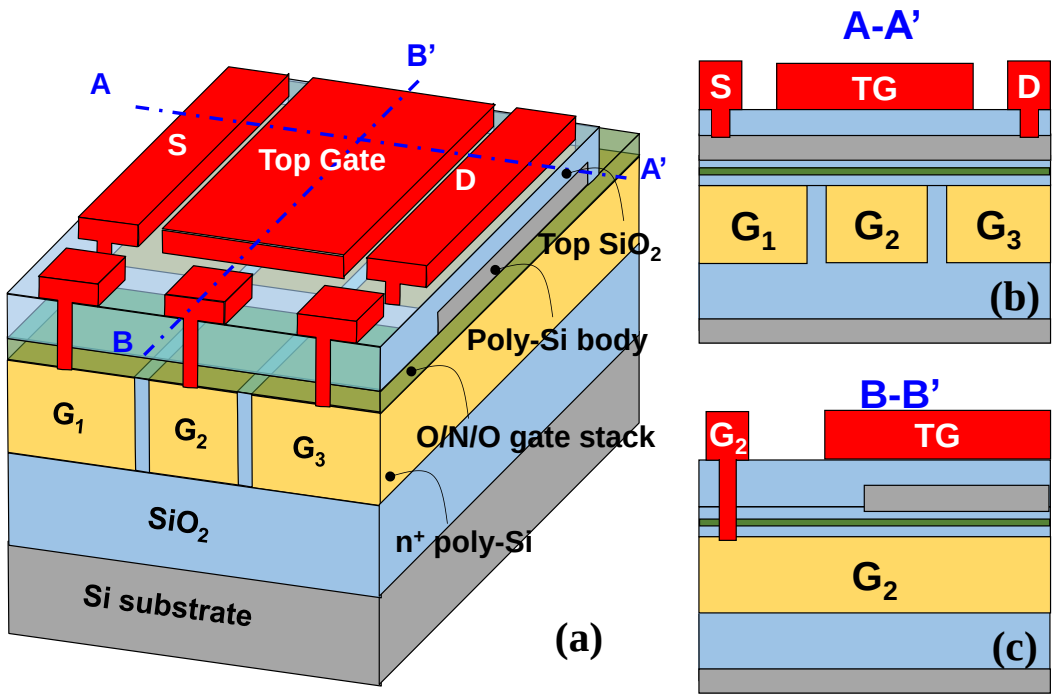


Fig. 2.1. 3-D schematic of the proposed reconfigurable device. Cross-sectional views of (b) A-A' and (c) B-B' planes. The n^+ poly-Si BGs can be used for metal wiring, resulting in simplified integrated circuit design.

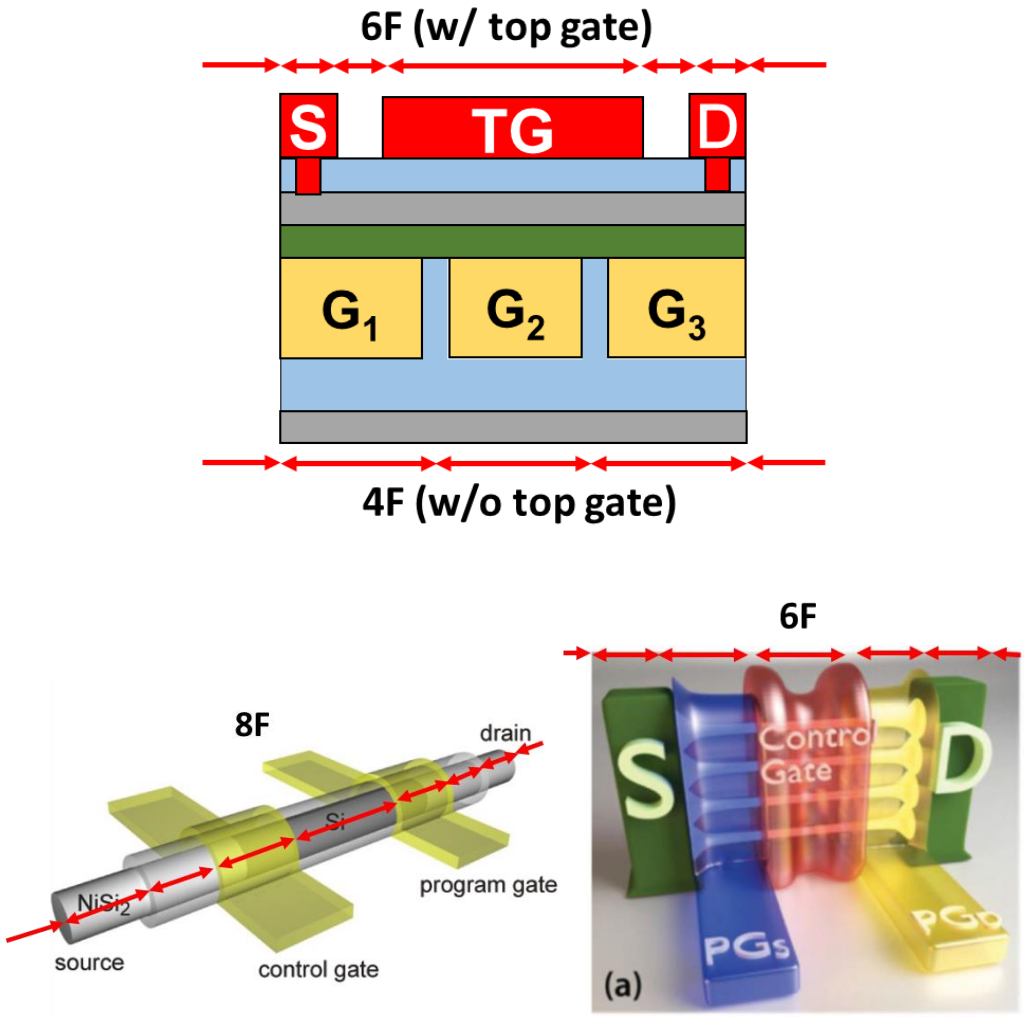


Fig. 2.2. Comparison of feature size among the proposed reconfigurable device and the previously reported RFETs [28-32].

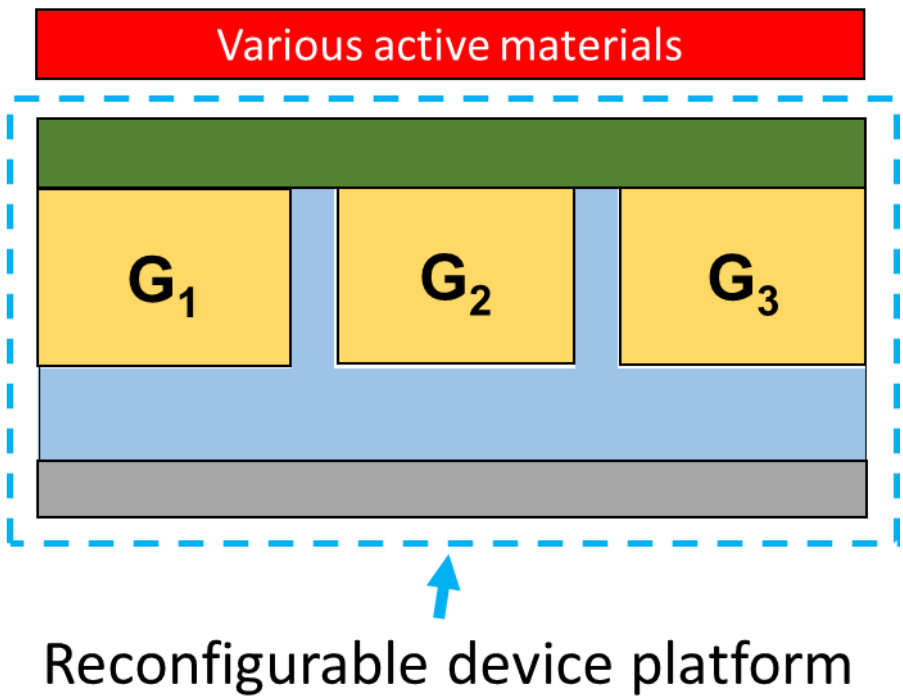


Fig. 2.3. Bottom gate array structure as a reconfigurable device platform.

2. 2 Fundamentals of Proposed Reconfigurable Device

As shown in Fig. 2.4, by changing bottom gate biases (V_{G1}, V_{G2}, and V_{G3}) independently, the active layer (poly-Si) above each bottom gate is electrically doped with either electrons (*n*-type) or holes (*p*-type), thus a user-defined electrical S/D regions can be formed. In addition, the electrical S/D regions can be achieved by programming or erasing the Si_3N_4 layer in the bottom gate stack. The device operation under program or erase state is equivalent to that when a negative or a positive bias is applied to the bottom gates (Fig. 2.5). Once the storage layer on the bottom gates are programmed or erased, the device can be operated without applying the bottom gate biases. Reasonable Schottky junction should be formed between the metal and the undoped poly-Si body so that we can achieve quite low off-current (I_{off}) or reverse current from any type of reconfigurable devices. The Schottky junction formed on the bottom gate can be an Ohmic-like contact when the electrons (e^-s) or holes (h^+s) are induced in the poly-Si body by the bottom gate bias and/or program/erase of the storage layer.

Since the Schottky junction can be converted to Ohmic-like contact between the metal and electrically induced *p*-type or *n*-type poly-Si body, we call it ambipolar contact which is imperative in reconfigurable devices. In this work, thermally evaporated Al is chosen to make Schottky junction with the undoped poly-Si. There have been a lot of reports on Al-Si Schottky junction, and Al is considered as a metal for ohmic contact when it is contacted with lightly doped *p*-type silicon [33]. The Schottky barrier formed between the Al and the poly-Si body can be modulated by the G_1 (or G_3) bias since the V_{G1} (or V_{G3}) affects the tunneling length and effective barrier height by changing electric field intensity across the Schottky junction [13]. The bottom gate bias and programming/erasing of the storage layer can induce e^-s or h^+s in the body butted to the Al. When the carrier concentration is high enough in the body, the tunneling barrier is narrow (effectively low Schottky barrier) and carriers easily tunnel from the metal to the body, and vice versa. A positive bottom gate bias and/or the hole storage (erasing) can convert the Al and poly-Si contact to the Al contact to n^+ body region. Then the Al contact to p^+ body region can be implemented by a negative bottom gate

bias and/or the electron storage (programming). The schematic band diagram and carrier behavior as a parameter of $V_{G1/G3}$ are shown in Fig. 2.6. Note the bottom gate bias and/or the charge storage can control the carrier concentration in the poly-Si body so that we can control conductivity in resistor and V_{th} in MOSFETs.

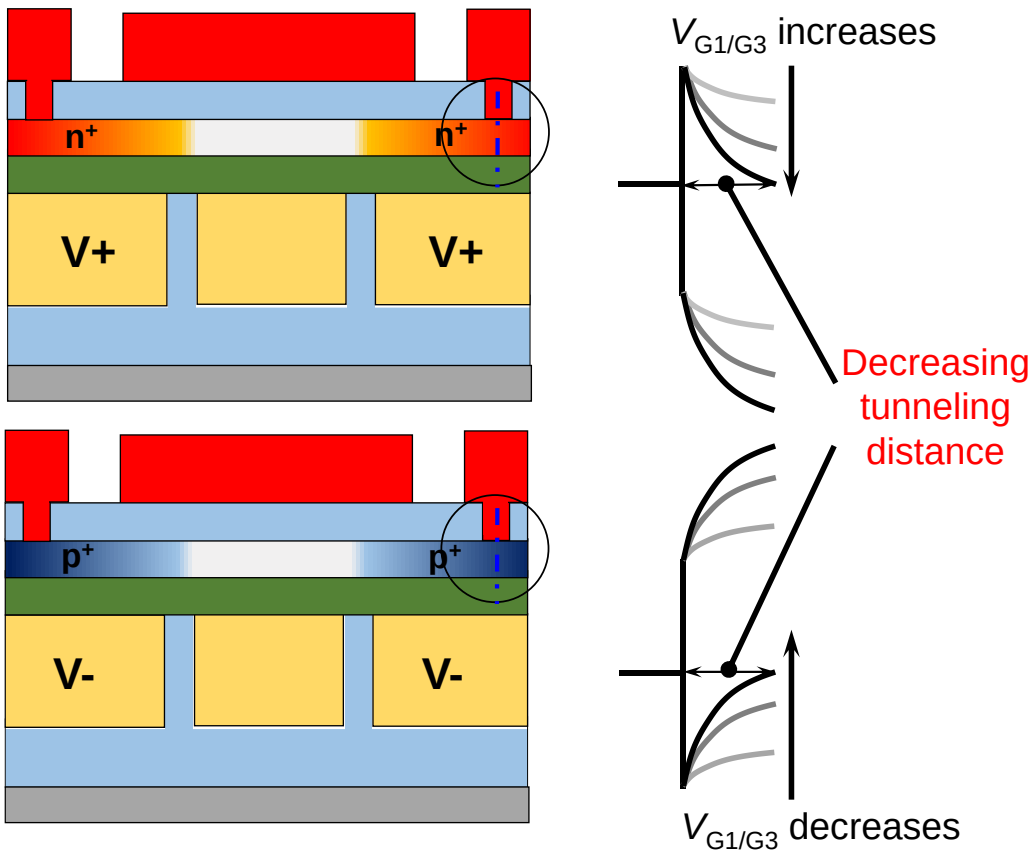


Fig. 2.4. The active layer (poly-Si) above each bottom gate is electrically doped with either electrons (*n*-type) or holes (*p*-type) by changing bottom gate biases (V_{G1}, V_{G2}, and V_{G3}) independently. Equivalently, the electrical S/D regions can be achieved by programming or erasing the Si_3N_4 layer in the bottom gate stack.

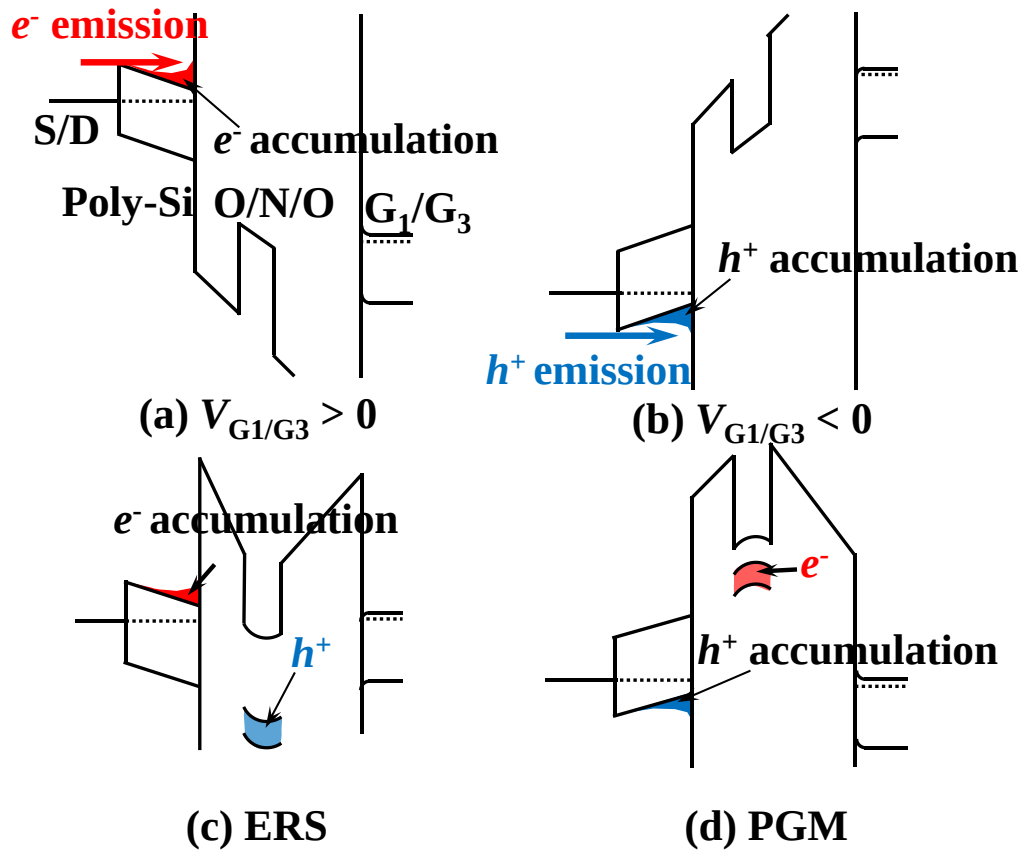


Fig. 2.5. Schematic energy band diagrams and e^-/h^+ behavior when (a) $V_{G1/G3} > 0$ V, (b) $V_{G1/G3} < 0$ V, (c) both G_1 and G_3 are erased and (d) programmed.

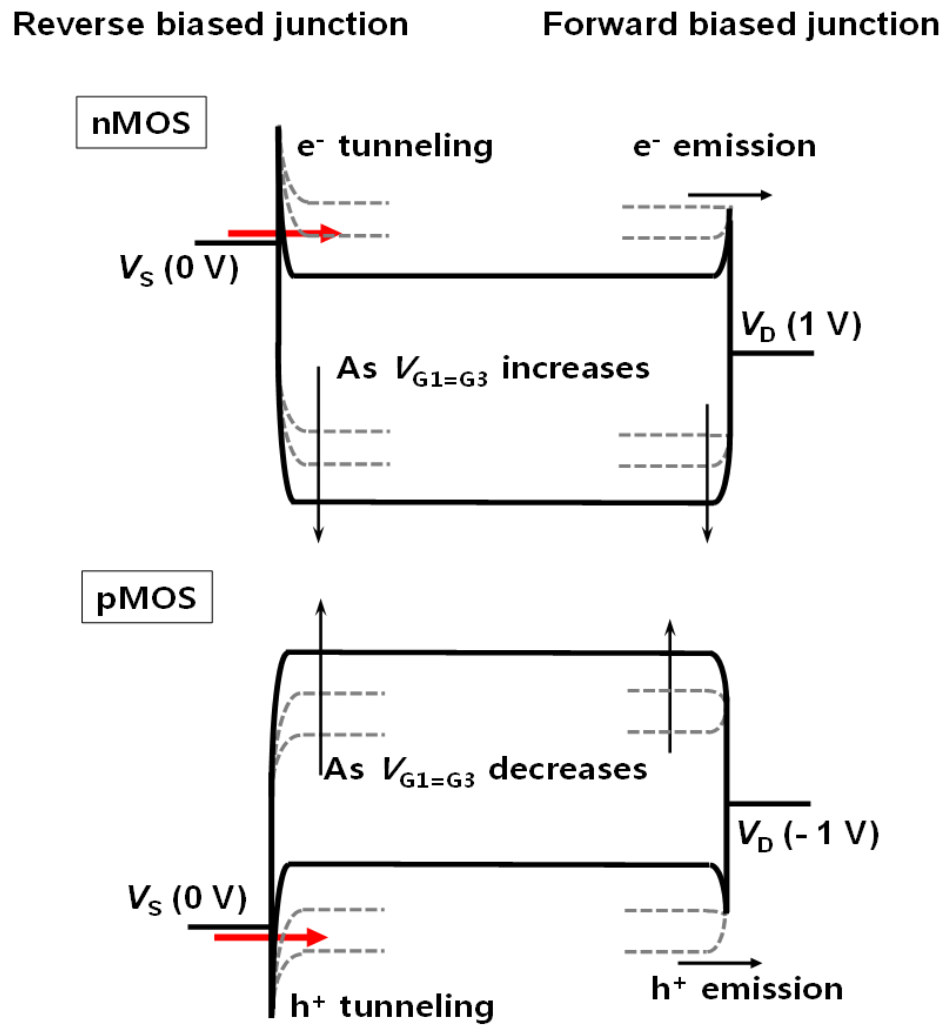


Fig. 2.6. Schematic energy band diagrams corresponding to the operation modes of the *n*-/*p*-MOSFET operations as a parameter of $V_{G1/G3}$. Both source and drain Schottky junctions are modulated by $V_{G1/G3}$.

Chapter 3

Fabrication of Proposed Reconfigurable Device

3. 1 Mask Layout and Fabrication Issues

Fig. 3.1 shows the mask layout for the proposed reconfigurable device. The total number of masks is 6. The masks are bottom gate patterning, device isolation, active patterning, bottom gate contact open, source/drain contact open, and metal lift-off, respectively. When we fabricate the device without the top gate structure, the top gate oxide is unnecessary, thus the source/drain contact open mask can be omitted. Therefore, the total number of masks can be reduced to 5. As shown in Fig. 3.2, with a simple change in the mask layout design, the reconfigurable device that can be transformed to BJTs as well as MOSFETs and diode. Also, as mentioned in the introduction part, the reconfigurable device platform can be fabricated with the mask layout that is shown in Fig. 3.3.

There are four main fabrication issues and are briefly shown in Fig. 3.4. The

device symbol is also shown in Fig. 3.4. First, the fabrication issues in the bottom gate formation are as follows. The width of the isolation oxide between each bottom gate should be controlled less than 30 nm. A complete isolation of each bottom gate and each device is important. The flatness of bottom gate of the device is also an important issue. Secondly, the quality and profile of SiO_2 and Si_3N_4 layers are critical to have a reliable O/N/O gate stack. Next, the active material selection is a key factor. In the reconfigurable devices, the switchable Schottky contact should be formed between the active material and source/drain metals, thus undoped poly-Si is used in this work. As shown in Fig. 3.5, in the case of doped poly-Si, it is difficult to obtain reasonable Schottky contact for both *n*- and *p*-type. Lastly, the source/drain metal should be chosen thoroughly. The source/drain metal should be a mid-gap metal having comparable Schottky barriers for both electron and hole. Due to the Fermi level pinning [34], the work function of metal in the Si-metal contact is different from the actual metal work function. Therefore, we used thermally evaporated aluminum (Al) as source/drain metal. As shown in Fig. 3.6 [33], the Al Schottky barriers for electron and hole

depend on the thickness of native oxide on the Si. In the reconfigurable devices used in this work, the hole Schottky barrier is slightly low than that of electron as shown in Fig. 3.7. To form the S/D and the top gate simultaneously, Al is also chosen for the top gate metal. The methods to resolve fabrication issues mentioned above are discussed in detail with each step of the process.

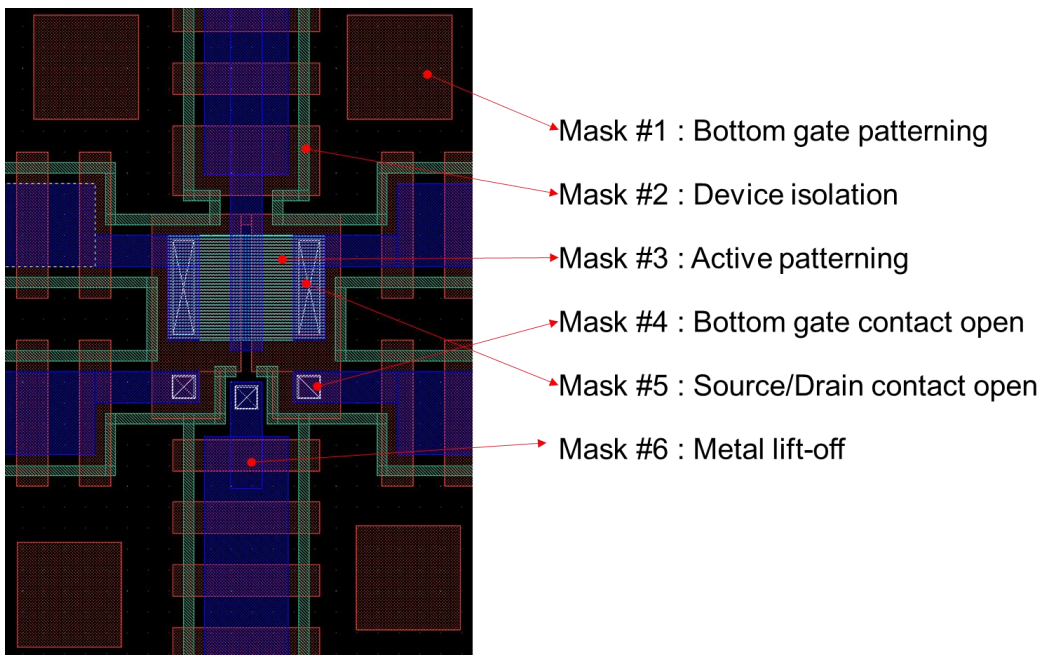


Fig. 3.1. The mask layout for device fabrication.

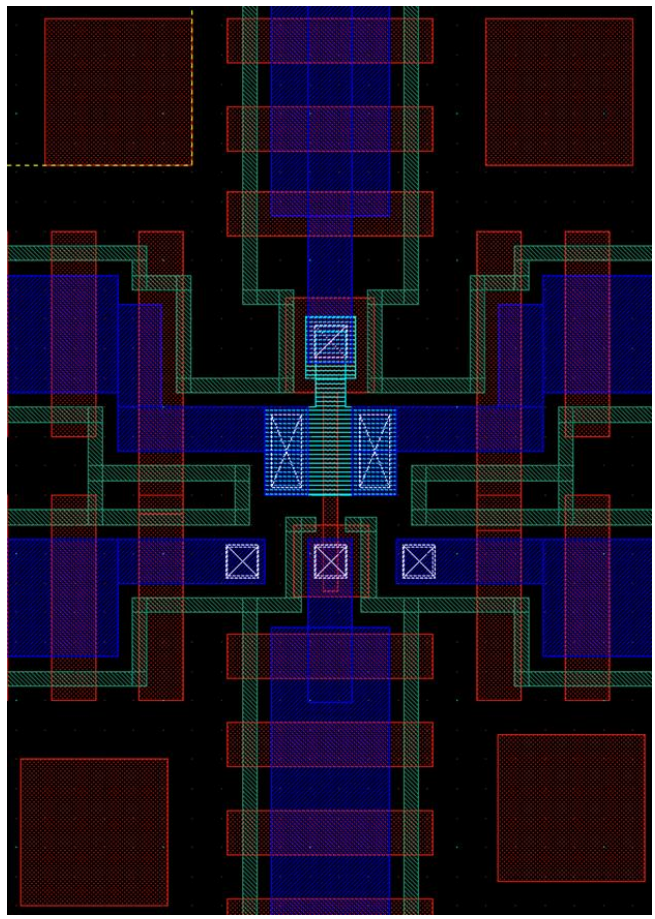


Fig. 3.2. The mask layout for device including BJT operation.

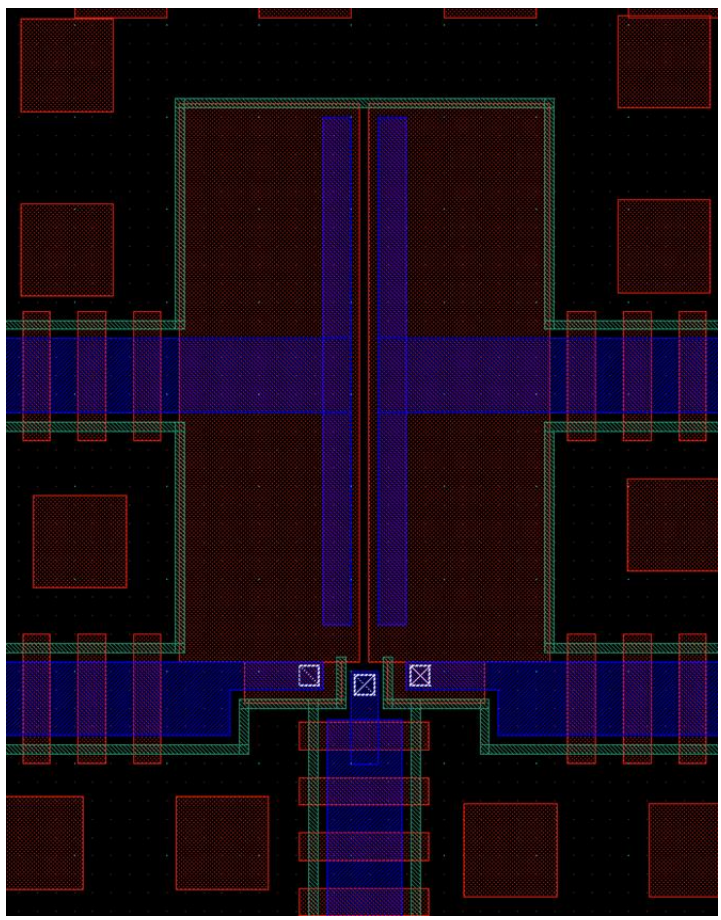


Fig. 3.3. The mask layout for device having various channel material (e.g. CNT, graphene, TMDCs, IGZO, and etc.).

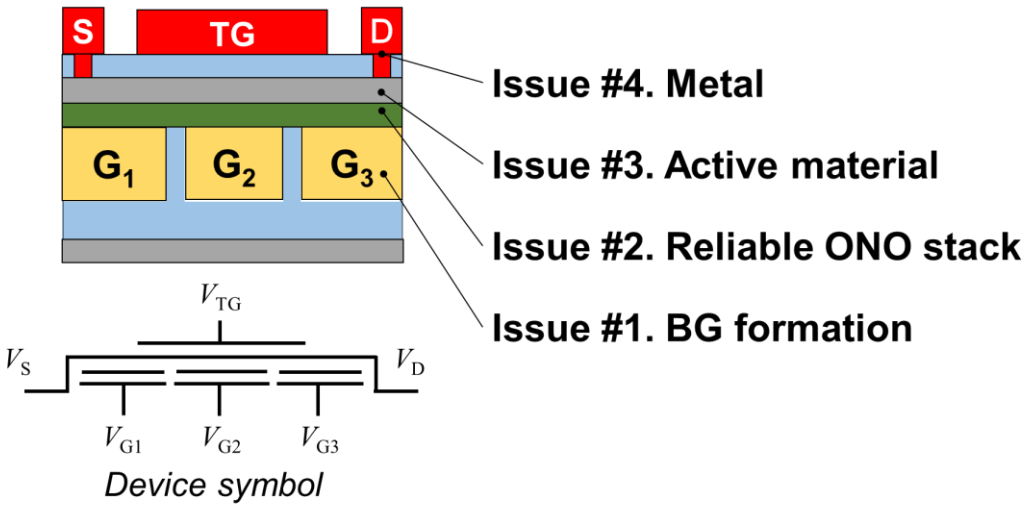


Fig. 3.4. Schematic diagram for brief explanation of fabrication issues.

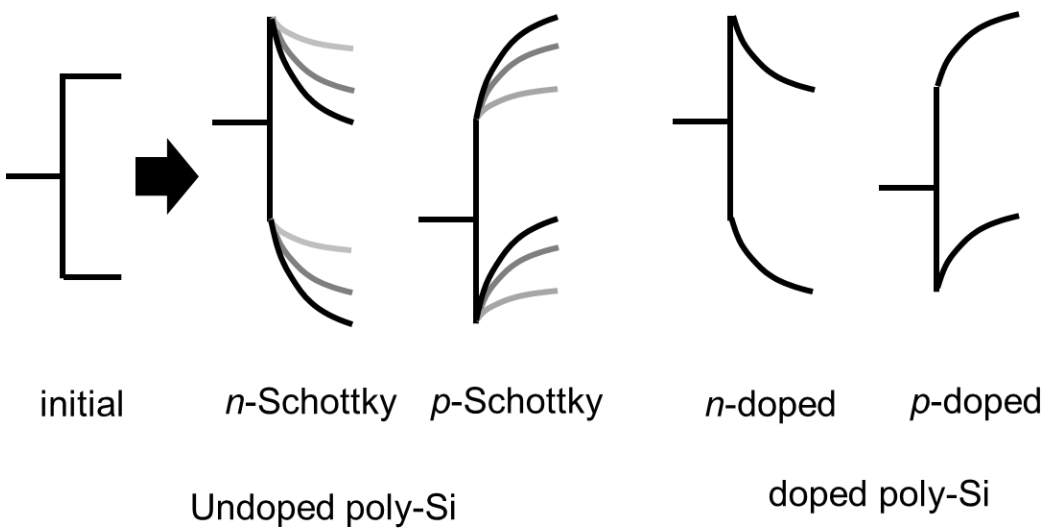


Fig. 3.5. Schematic diagram of Schottky contact between the active material and S/D contact metals.

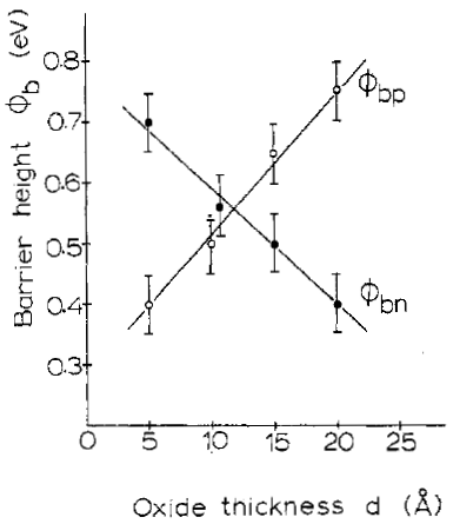


Fig. 3.6. Schottky barrier height, ϕ_{bn} (*n*-type) and ϕ_{bp} (*p*-type), versus oxide thickness *d* [33].

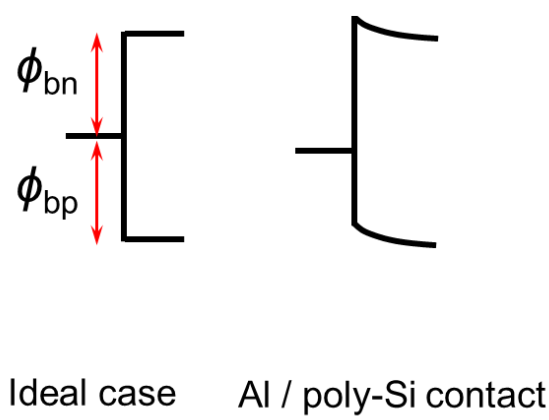


Fig. 3.7. Schematic diagrams of Schottky barrier height for ideal case and actual case in the device used in this work, respectively.

3. 2 Bottom Gate Formation

3. 2. 1 Nitride Spacer Method

We will first describe the fabrication process using the nitride spacer. The key process flows are shown in Fig. 3.8. To form an isolation layer, a 300 nm-thick thermal oxide is grown on a 6-inch *p*-type Si wafer by wet oxidation process. An n^+ poly-Si to be used as bottom gates is formed on a silicon dioxide (SiO_2) grown on the wafer. A layer of SiO_2 is thermally grown on the poly-Si layer by thermal oxidation (Fig. 3.8(a)). The SiO_2 layer is patterned by photo lithography (1^{st} mask) and dry etch process (Fig. 3.8(b)). The Si_3N_4 layer is deposited and etched to form a nitride spacer along the oxide sidewall (Fig. 3.8(c)). The SiO_2 layer is removed by wet etch process, therefore, only nitride spacer is remained (Fig. 3.8(d)). Then the thermal oxide is grown using a nitride spacer as a hard mask (Fig. 3.8(e)), followed by removing the nitride spacer by wet etched process (Fig. 3.8(f)). After that, using the thermally grown SiO_2 as a hard mask, the poly-Si layer is patterned

by dry etch process (Fig. 3.8(g)). The gap-fill process is conducted by depositing SiO_2 layer (Fig. 3.8(h)), then the SiO_2 layer is etched back by wet etch process and the bottom gate structure is formed (Fig. 3.8(i)).

In the nitride spacer method, it is difficult to define the width of the isolation oxide 30 nm or less. Especially the oxidation length under the nitride spacer is not uniform when growing SiO_2 using the nitride spacer as a hard mask as depicted in Fig. 3.9(a). The SEM images of the fabricated bottom gate structure are shown in Figs 3.9(b) and (c), and they show that the device isolation is not complete. To solve these problems, we proposed poly-Si CMP method to fabricate the bottom gate structure, and will be introduced in the following chapter.

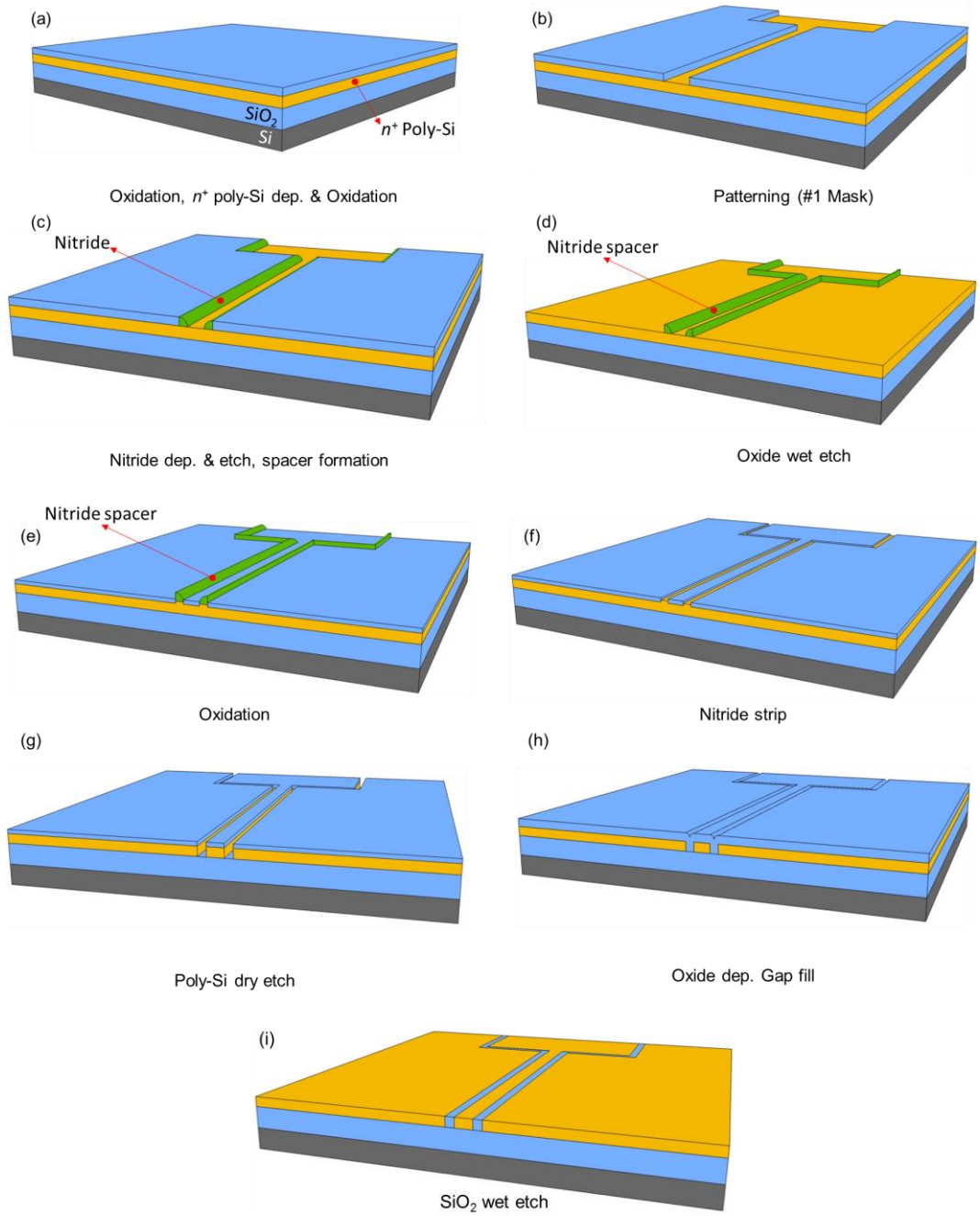


Fig. 3.8. The key process flow to fabricate the bottom gate structure by nitride spacer method.

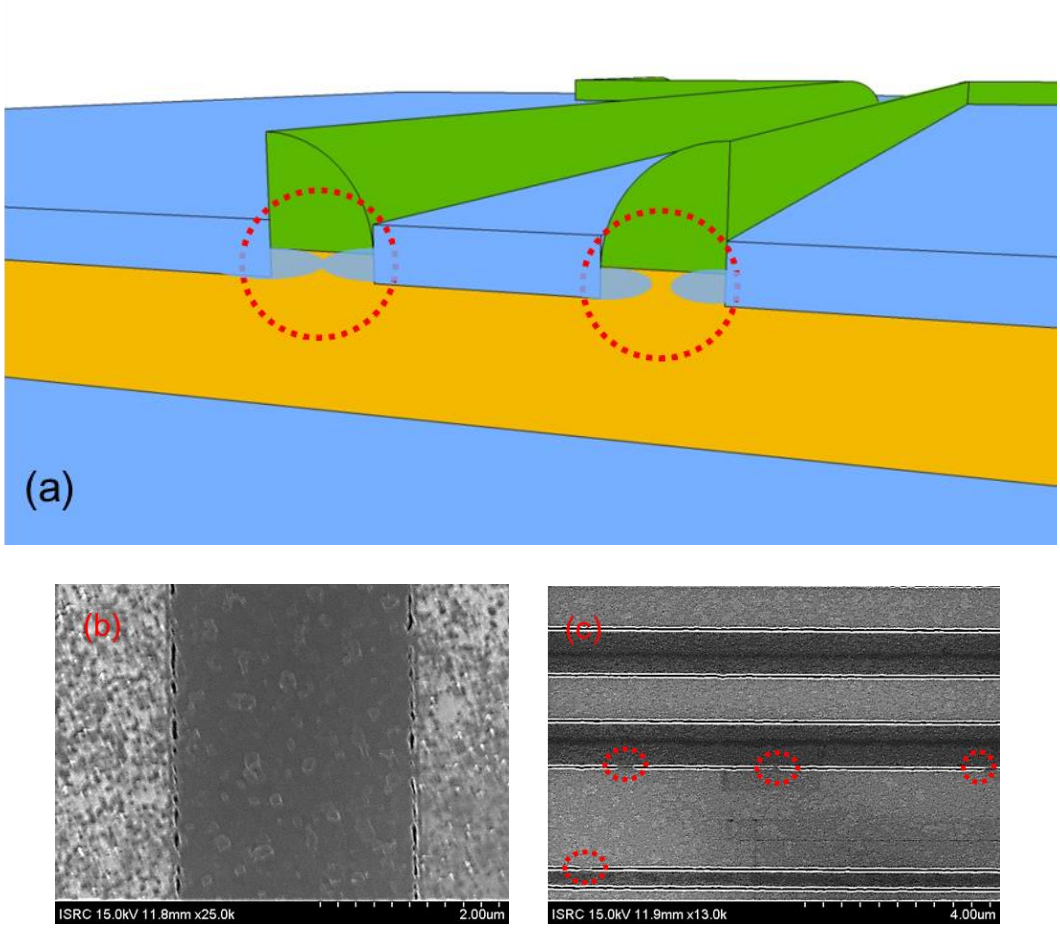


Fig. 3.9. (a) 3-D schematic for showing the randomness of oxidation length under the nitride spacer when growing SiO_2 using the nitride spacer as a hard mask. (b), (c) The SEM images of the fabricated bottom gate structure by nitride spacer method. The device isolation is incomplete.

3. 2. 2 Poly-Si CMP Method

The reconfigurable devices and circuits consisted of the devices are fabricated on a 6-inch Si wafer with conventional Si CMOS technology. The schematic cross-sectional views of key fabrication process steps of the reconfigurable devices are shown in Fig. 3.10. Key fabrication steps in detail are explained as follows. To form an isolation layer, a 300 nm-thick thermal oxide is grown on a 6-inch p-type Si wafer by wet oxidation process. A 140 nm-thick n^+ poly-Si (1^{st} poly-Si) to be used as bottom gates is formed on a silicon dioxide (SiO_2) grown on the wafer. A thin layer of SiO_2 is thermally grown on the poly-Si layer by rapid thermal oxidation (RTO) process, followed by the deposition of 100 nm thick silicon nitride (Si_3N_4) layer (Fig. 3.10(a)). The thin oxide shown in Fig. 3.10(a) is needed to prevent a damage on the poly-Si during Si_3N_4 strip in a following step. The Si_3N_4, thin SiO_2 and poly-Si layers are patterned by photo lithography (1^{st} mask) and dry etch process (Fig. 3.10(b)). A 24.6 nm-thick thermal SiO_2 is grown along the sidewall of the patterned poly-Si to separate

bottom gates (Fig. 3.10(c)), and a 140 nm-thick n^+ poly-Si (2nd poly-Si) is deposited again as shown Fig. 3.10(d). As shown in Fig. 3.11, if poly-Si chemical mechanical planarization (CMP) is done directly to the poly-Si using a nitride as a stopping layer, the uniformity cannot be controlled over the wafer due to the loading effect of the pattern density. We introduced thicker nitride to solve this problem, however, the uniformity problem still occurs and the bottom gate flatness issue arises due to the height difference between the 1st and 2nd poly-Si. Therefore, a thin buffer SiO_2 layer and Si_3N_4 layer are grown (Fig. 3.10(e)) and followed by poly-Si CMP process (Fig. 3.10(f)). Here the patterned Si_3N_4 layer acts as a CMP stopping layer. The thin Si_3N_4 layer left on the 2nd poly-Si is used as a mask for selective etch of some of the exposed poly-Si layer during isotropic poly-Si etch process to adjust the height of the 1st and 2nd poly-Si layers as shown in Fig. 3.10(g). Again, a buffer SiO_2 layer is grown on the exposed 2nd poly-Si remained after timed etch of the 2nd poly-Si and used for protecting poly-Si from the damage during the strip process of the Si_3N_4. After stripping the Si_3N_4 (Fig. 3.10(h)), thin SiO_2 layers on the 1st and 2nd poly-Si layers are stripped in diluted

HF (dHF). Then touch polishing is done by using CMP process for the planarization of the surface of the poly-Si layers and the oxide layer between 1st and 2nd poly-Si as shown in Fig. 3.10(i).

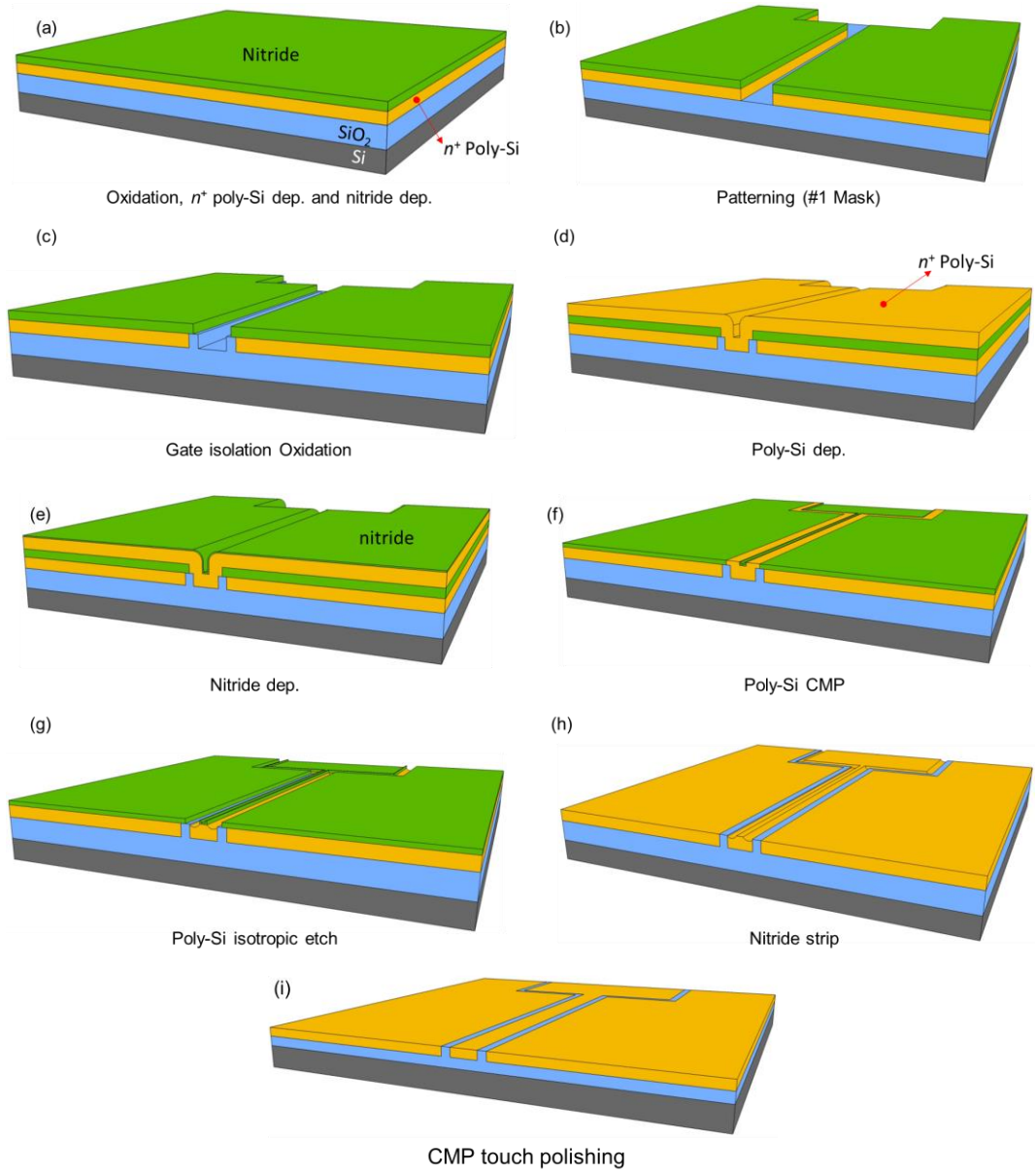


Fig. 3.10. The key process flow to fabricate the bottom gate structure by poly-Si CMP method.

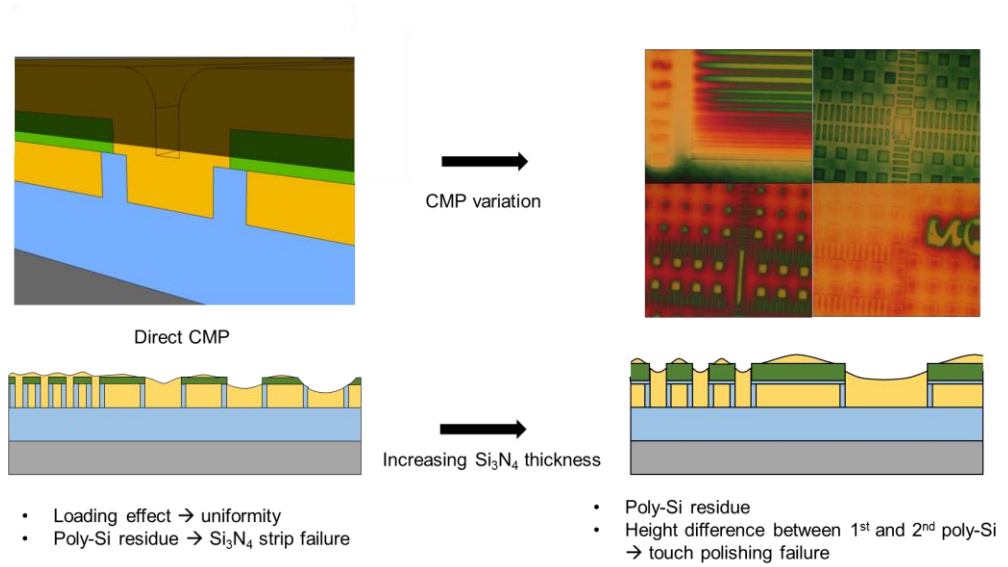


Fig. 3.11. Schematics and optical images to depict the loading effect due to the pattern density difference when the CMP process is directly done to the poly-Si. When the thicker nitride is introduced as a stopping layer, the uniformity problem still occurs and the bottom gate flatness issue arises due to the height difference between the 1st and 2nd poly-Si.

3. 3 Overall Fabrication Process

The schematic cross-sectional views of overall fabrication process steps of reconfigurable device in detail are shown in Fig. 3.12. Note that every process is CMOS compatible. After the bottom gate structure is fabricated, the 2^{nd} mask is used to isolate the bottom gate array for a device from adjacent devices. Using the 2^{nd} mask, the poly-Si layers are etched as shown in Fig. 3.13. Note that the isolation oxide has a negative slope since it is thermally grown along the poly-Si sidewall. Therefore, the poly-Si spacer remains after isolation process is done as shown in Fig. 3.13. The poly-Si spacer can act as a leakage path between adjacent devices, and it leads to degradation of the device performance in the circuit application and PGM/ERS operation. Fig. 3.14 shows TEM image of the device showing remained poly-Si spacer. Then, a $SiO_2/Si_3N_4/SiO_2$ (O/N/O) stack having 12/6/6 nm thickness is formed for the bottom gate insulator stack where the Si_3N_4 layer can store charges as shown in Fig. 3.15. A 20 nm-thick undoped amorphous Si (a-Si) active layer is deposited by LPCVD and annealed at 600 °C for 24 hours

to be poly-Si as shown in Fig. 3.16. The poly-Si active layer is defined by using the 3rd mask and dry etch process. A layer of 8 nm-thick SiO_2 is grown thermally for the top gate insulator, which reduces the thickness of active poly-Si to 16 nm as shown in Fig. 3.17. Using the 4th mask and dry etch process, the contact holes for the bottom gates are formed as shown in Fig. 3.18. Similarly, the contact holes for source and drain (S/D) contact are formed by using 5th mask and wet etch process (Fig. 3.18). Fig. 3.19 shows the aluminum (Al) electrodes for bottom gates, S/D, and top gate (TG) are formed at once by lift-off process using the 6th mask. The Al layer is formed by thermal evaporation. Note that there is no implantation process and only 6 masks are used. The number of masks can be reduced to 5 when we omit the TG formation process. The scanning electron microscope and transmission electron microscope (SEM/TEM) images of a fabricated device with a specific dimensions are shown in Fig. 3.20. In Fig. 3.20(a), which is SEM image of the device, the bottom gates and the TG are shown. Three bottom gates are denoted by G_1, G_2 and G_3 in sequence. The G_1 and G_3 are formed under the source and drain, respectively, and the G_2 is formed

under the channel as shown in Fig. 3.20(a) and Fig. 3.20(b). This device is a sort of poly-Si TFT. The device becomes inverted-staggered and coplanar structures, respectively, when the G_2 and TG are used for the switching gate of the TFT. Note that the device becomes a Silicon On Insulator (SOI) MOSFET when the channel material is single crystalline Si. Fig. 3.20(b) is TEM image of a fabricated device where adjacent bottom gates are separated by 24.6 nm thick SiO_2 and the length of G_2 (the bottom gate) is about 315 nm. The magnified TEM image is shown in Fig. 3.20(c), and shows that the thicknesses of O/N/O gate stack, poly-Si active layer, and top gate dielectric are about 12/6/6, 16, and 8 nm, respectively.

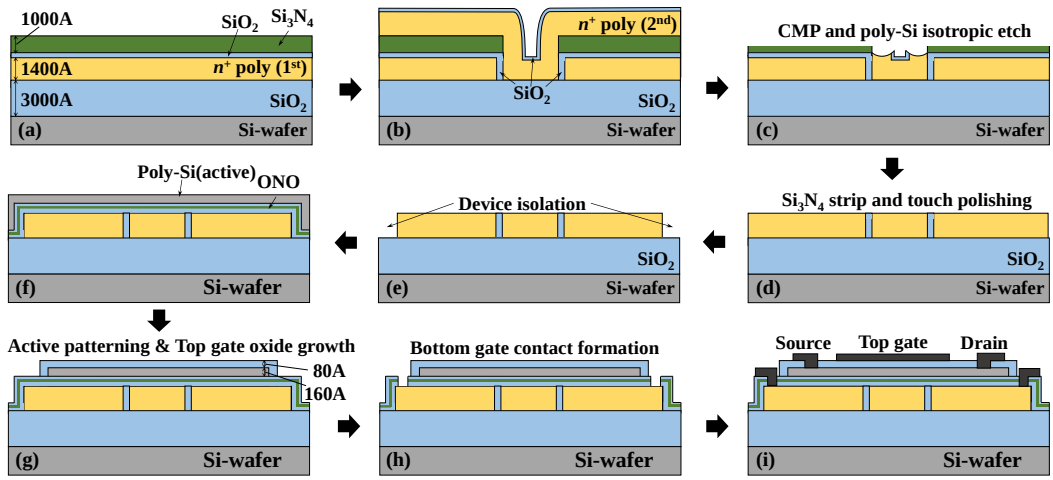


Fig. 3.12. Schematic cross-sectional views of overall fabrication process steps of reconfigurable device in detail. Every process is CMOS compatible.

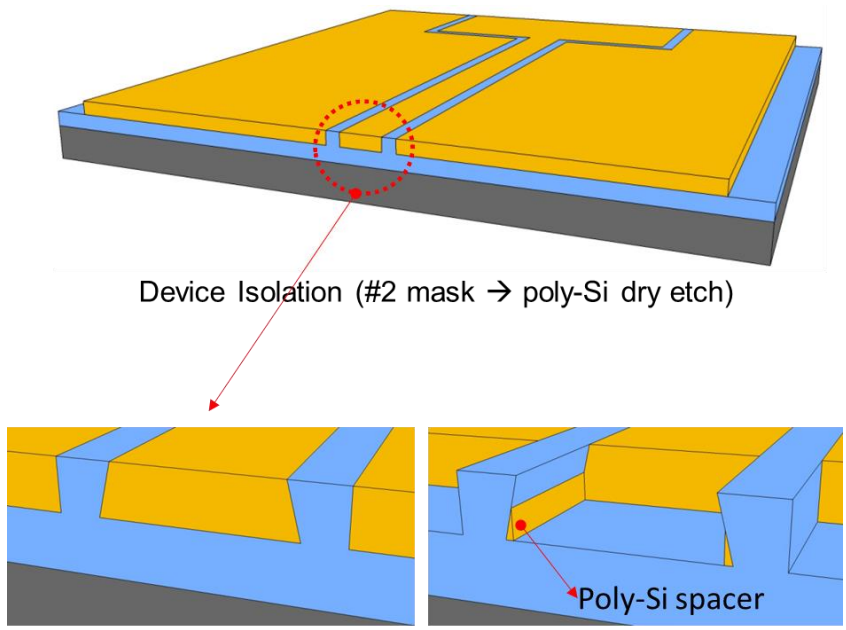


Fig. 3.13. 3-D schematic views of device isolation step. The isolation oxide has a reverse slope, and the poly-Si spacer remains after isolation process is done.

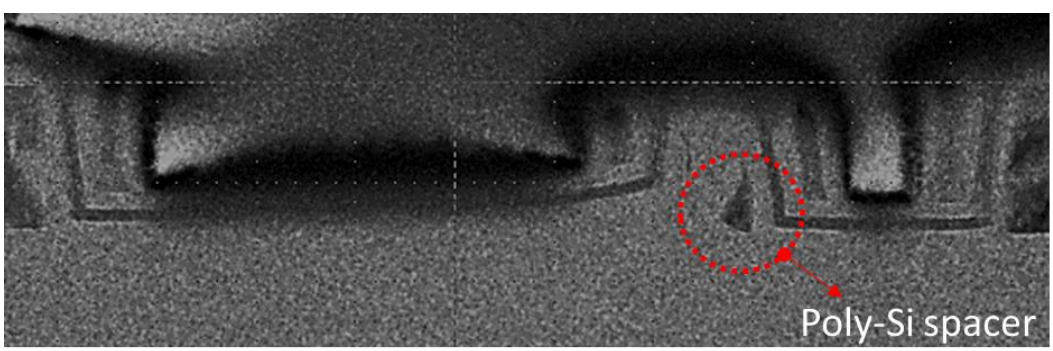


Fig. 3.14. TEM image of the device showing remained poly-Si spacer.

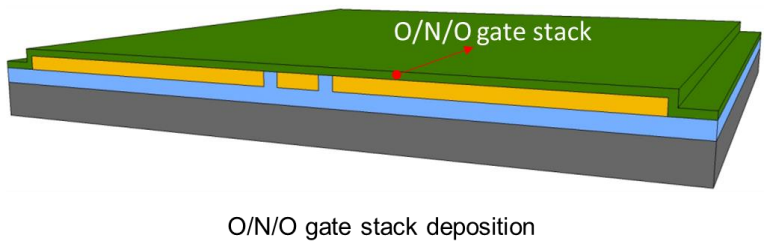


Fig. 3.15. 3-D schematic view after O/N/O gate stack is deposited.

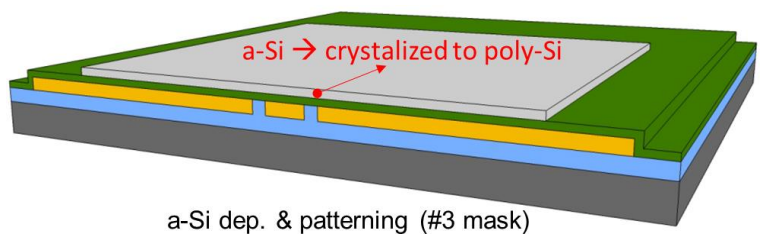


Fig. 3.16. 3-D schematic view after the active is deposited and patterned.

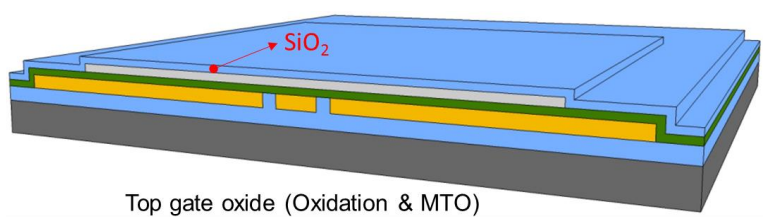


Fig. 3.17. 3-D schematic view after the top gate oxide is grown.

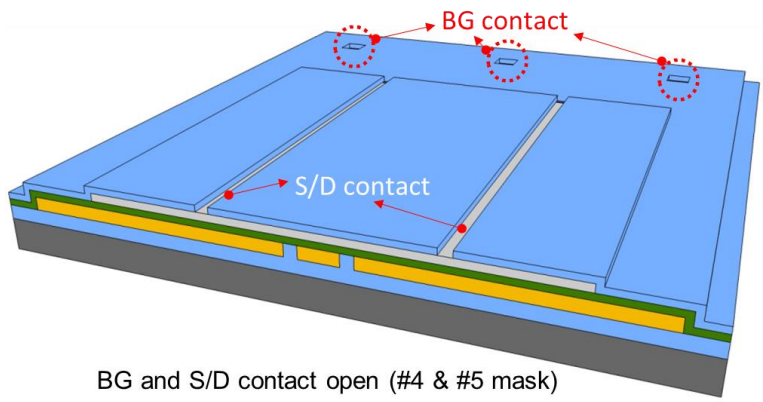


Fig. 3.18. 3-D schematic view after the BGs and S/D contacts are open.

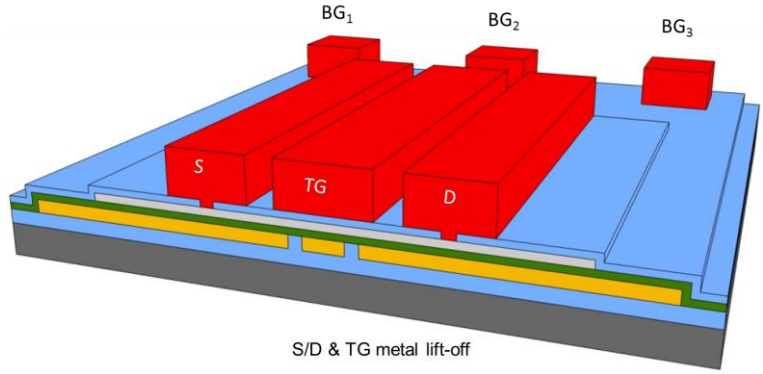


Fig. 3.19. 3-D schematic view after metal lift-off process is done.

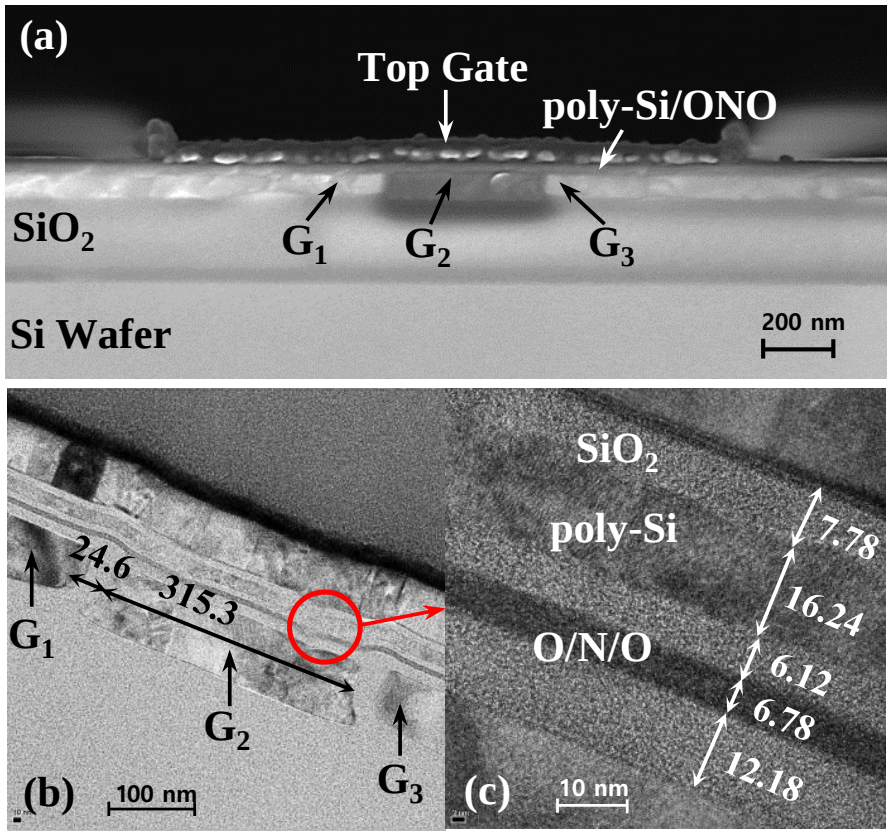


Fig. 3.20. Cross-sectional (a) SEM and (b), (c) TEM images of a fabricated reconfigurable device. The thickness and width of each layer are given in nanometers.

Chapter 4

Characterization of Proposed Reconfigurable Device

4. 1 *I-V* characteristics of *n*- and *p*-MOSFETs

In MOSFET operation, either G_2 or TG can be used for a switching-gate. Figs. 4.1 and 4.2 show measured drain current (I_D) versus V_{G2} and I_D versus TG bias (V_{TG}), respectively, as a parameter of the G_1 and G_3 bias ($V_{G1/G3}$) in a single reconfigurable device having a channel length of 1 μm and a width of 50 μm, demonstrating successful working of *n*-/*p*-MOSFETs. The drain biases (V_D) are fixed at 1 V and -1 V, respectively, for *n*- and *p*-MOSFETs. Depending on the polarity of $V_{G1/G3}$, a device is transformed to *n*- or *p*-MOSFET. Note that the magnitude of on-current (I_{on}) in *n*-/*p*-MOSFETs becomes large as the $V_{G1/G3}$ increases/decreases from 2/-2 V to 4/-4V. The I_{on}/I_{off} is ~10^6, and the I_{on} saturates with increasing V_{G2} since the contact resistance between the Al and the poly-Si body becomes dominant over the channel resistance. The SSs are less than 120 mV/dec and 170 mV/dec in I_D-V_{G2} and I_D-V_{TG} curves, respectively. Fig. 4.3(a) and (b) show energy band diagrams when a device is working as *n*-MOSFET and *p*-MOSFET, respectively as a parameter of V_{G2}. When the $V_{G1/G3}$ is positive, e^-s are induced in the poly-Si body on the bottom gates G_1 and G_3. As the $V_{G1/G3}$

increases, carriers move easily between the Al and the poly-Si body thanks to the reduced contact resistance. As a result, a kind of *n*-*p*-*n* junction is formed along the channel length direction, and the device is working as an *n*-MOSFET as shown in Fig. 4.3(a). Note that the Schottky junctions at the grounded source and positively biased drain are reverse and forward biased, respectively, since the poly-Si which has induced electrons acts as equivalently n^+ region. Similarly, the device can be operated as *p*-MOSFET by applying a negative $V_{G1/G3}$ to the G_1 and G_3. And the same story can be applied to the *p*-MOSFET. Simulated conduction band contour of *n*-MOSFET operation as a parameter of V_{G2} is also shown in Fig. 4.4. Note that the drain bias in *n*- and *p*-MOSFETs is dropped across the Schottky junction at the source when both devices are fully turned-on (V_{G2}= 4 V for *n*-MOSFET and V_{G2}= -4 V for *p*-MOSFET).

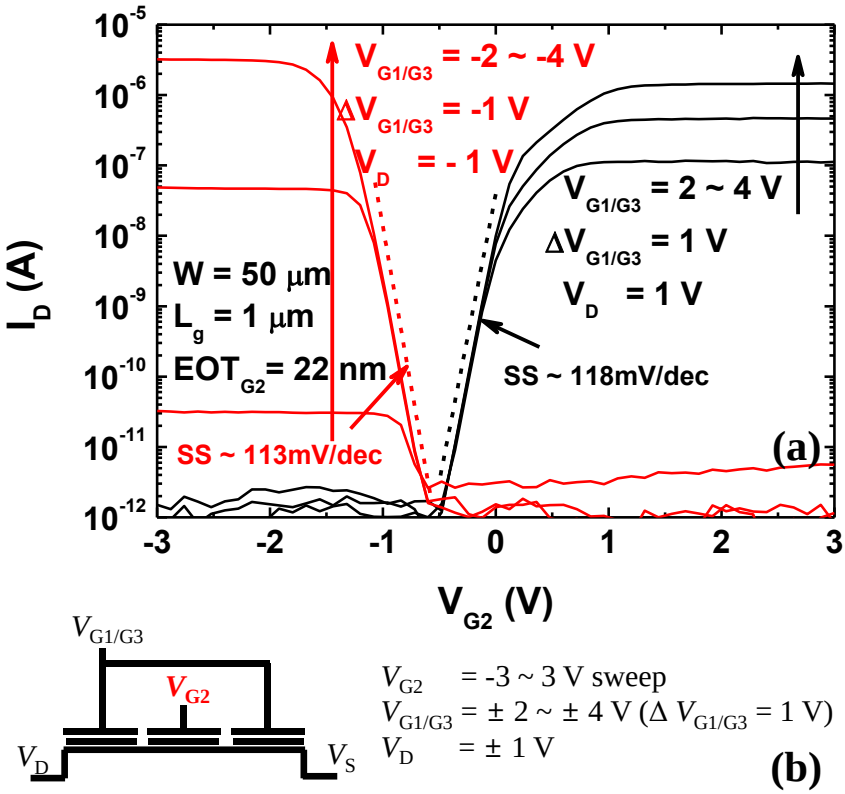


Fig. 4.1. (a) I_D-V_{G2} (bottom gate bias) curves of *n*-/*p*-MOSFETs measured from single reconfigurable device (W=50 μm, L_g= 1 μm). (b) Device symbol and a bias scheme for the I_D-V_{G2} curves. $V_{G1/G3}$s for *n*-/*p*-MOSFETs are positive (2, 3 and 4 V) at a V_D of 1 V and negative (-2, -3 and -4 V) at a V_D -1 V, respectively.

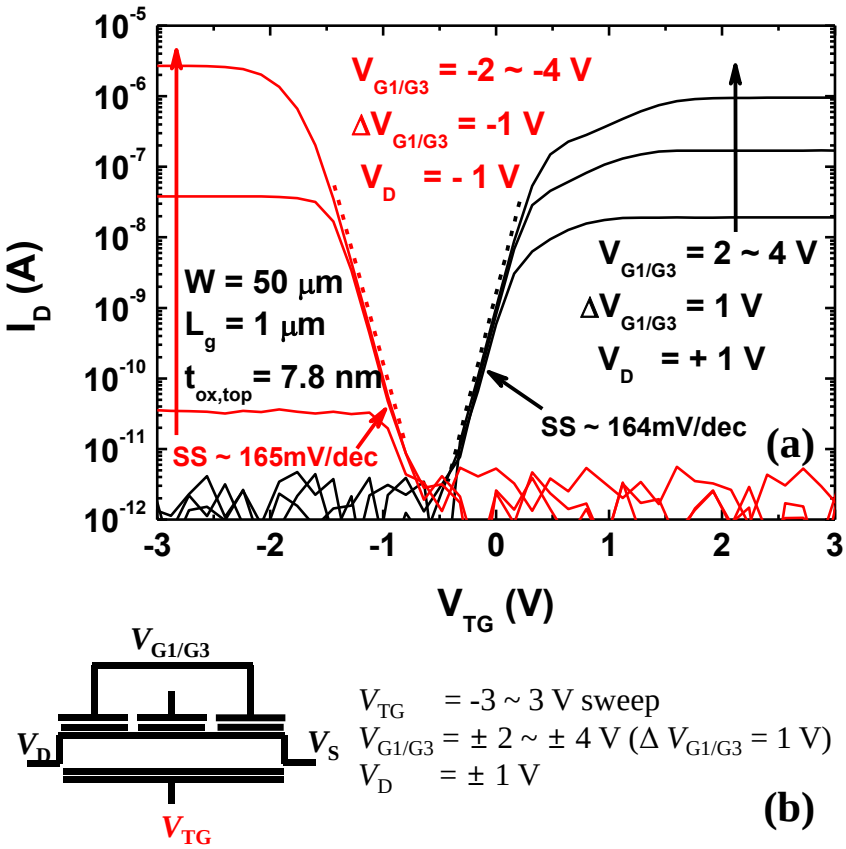


Fig. 4.2. (a) I_D-V_{TG} (top gate bias) curves of *n*-/*p*-MOSFETs measured from single reconfigurable device (W=50 μm, L_g= 1 μm). (b) Device symbol and a bias scheme for the I_D-V_{TG} curves. $V_{G1/G3}$s for *n*-/*p*-MOSFETs are positive (2, 3 and 4 V) at a V_D of 1 V and negative (-2, -3 and -4 V) at a V_D -1 V, respectively.

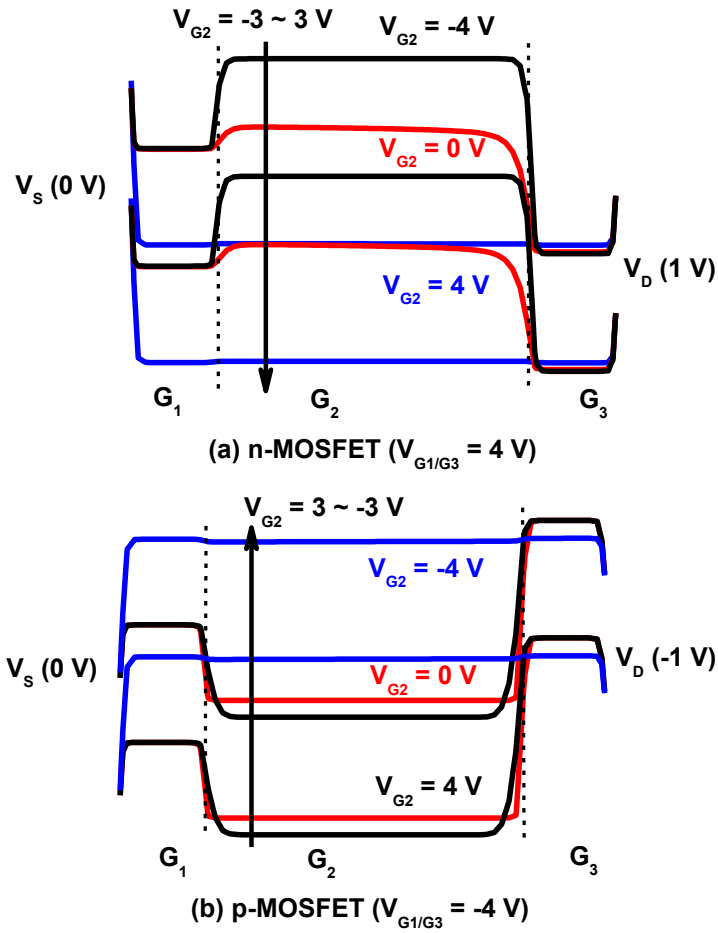


Fig. 4.3. Simulated energy band diagrams corresponding to the (a) *n*- and (b) *p*-MOSFET operations as a parameter of V_{G2} (-4, 0, 4 V). The channel barrier is modulated by controlling V_{G2}. The V_D mainly drops across the Schottky at the source.

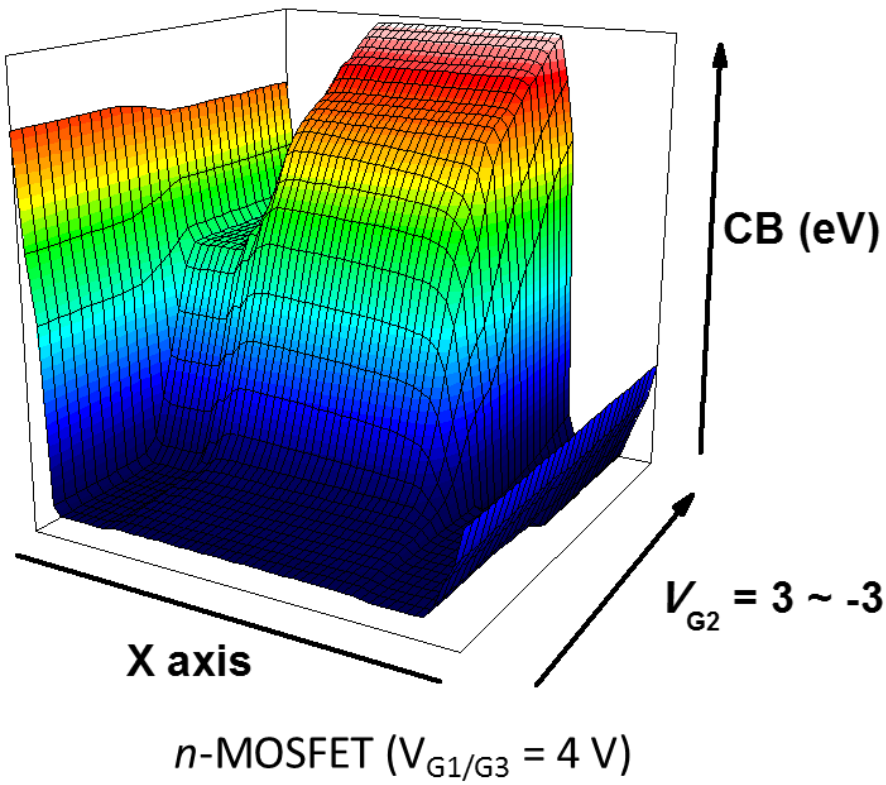


Fig. 4.4. Simulated conduction band contour of *n*-MOSFET operation as a parameter of V_{G2}.

4. 2 MOSFET *I-V* with PGM/ERS state of bottom gates

The gate insulator stack on the bottom gates includes a layer of nitride which can store electrons or holes. Thus the nonvolatile characteristic in our structure is very useful because it is not needed to keep a constant bias to sustain a specific device operation. We can achieve no cross-talk, no leakage, and better reliability thanks to the nonvolatile functionality. By applying a bias to the bottom gate for programming or erasing, electrons or holes can be injected to the charge storage layer. As a result, electrons or holes are induced in the poly-Si body on the bottom gates. The nitride layer in the gate insulator stack under the poly-Si body where the channel is formed stores electrons or holes so that we can control the V_{th} of the device. The programming or erasing is performed by applying a positive or negative bias to the G_1 and G_3 at the drain (V_D) and source biases (V_S) of 0 V. Fig. 4.5(a) shows I_D-V_{G2} curves of *n*-/*p*-MOSFETs where both G_1 and G_3 are erased for *n*-MOSFET and programmed for *p*-MOSFET. In the measurement of the *I-V*, the G_1 and G_3 are grounded. As in Figs. 4.1 and 4.2, the V_Ds are fixed at 1 V and -1 V

for *n*- and *p*-MOSFETs, respectively. The programmed and erased bottom gates are depicted by red dashed line in the symbol of the reconfigurable device in Fig. 4.5(b). The I_Ds of both *n*-/*p*-MOSFETs are comparable to those of Fig. 4.1 at the $V_{G1/G3} = \pm 4$ V. In addition, by programming or erasing the storage layer on the G_2 which is depicted as dashed line in the symbol of the Fig. 4.6(b), the V_{th} of MOSFETs can be controlled. Fig. 4.6(a) demonstrates that the V_{th} is controlled by the amount of programmed e^-s in the charge storage layer on the G_2. The programming bias (V_{PGM}) is 12 V or 13 V at a fixed pulse width (t_{PGM}) of 10 μs. The amount of V_{th} shift is increased with increasing V_{PGM}, which means more e^- are programmed. Note that both V_{th}s of *p*- and *n*-MOSFET change equally. In the same manner, the V_{th} can be shifted to the negative direction by erasing the G_2. The retention characteristics of program (PGM) and erase (ERS) states are observed in Fig. 4.7. Fig. 4.7(a) shows I_D drift biased at $V_{G2} = \pm 3$ V when the storage layer on the G_1 and G_3 is in PGM and ERS states. By using I_D-$V_{G1/G3}$ curves at $V_{G2} = \pm 3$ V as plotted in Fig. 4.7(c), the effective $V_{G1/G3}$ change corresponding to the I_D drift can be extrapolated. As a result, the effective $V_{G1/G3}$

change as a function of time after programming and erasing the storage layer on the G_1 and G_3 is plotted in Fig. 4.7(b). The programmed e^- and h^+ are hardly removed from charge storage layer until 2000 seconds. The characteristic can be improved by optimizing the process.

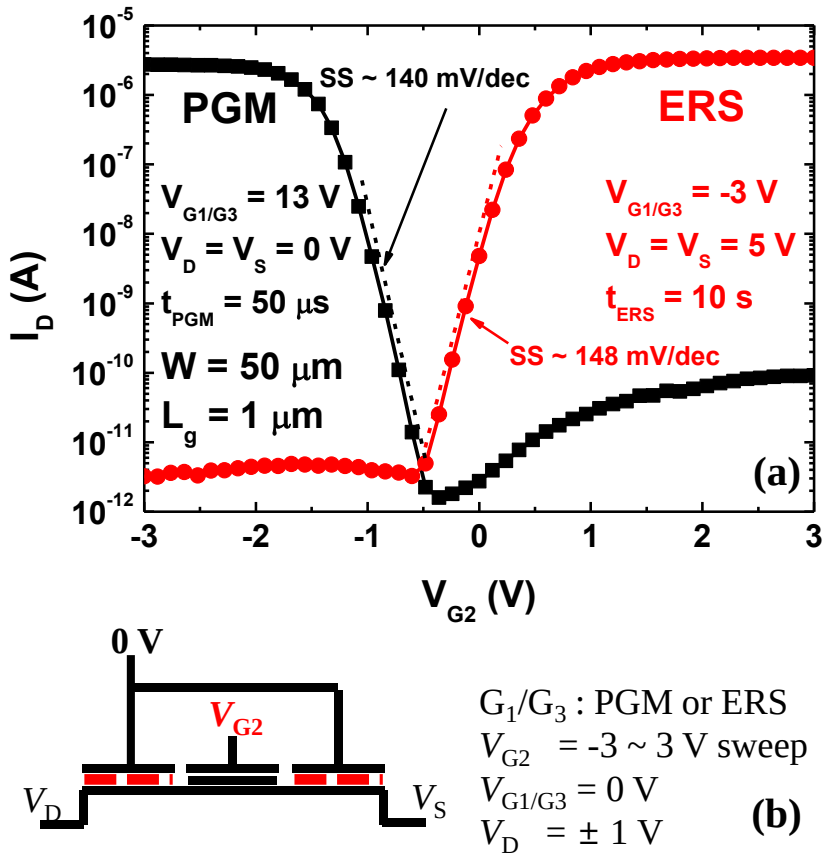


Fig. 4.5. (a) I_D-V_{G2} curves of *n*-/*p*-MOSFETs measured from a single reconfigurable device. Both bottom gates G_1 and G_3 are erased and programmed, respectively, to obtain *n*- and *p*-MOSFETs from the reconfigurable device. (b) Device symbol and a bias scheme for the I_D-V_{G2} curves. The dashed lines in the device symbol stand for program (PGM) or erase (ERS) state of the charge storage layer on the bottom gates.

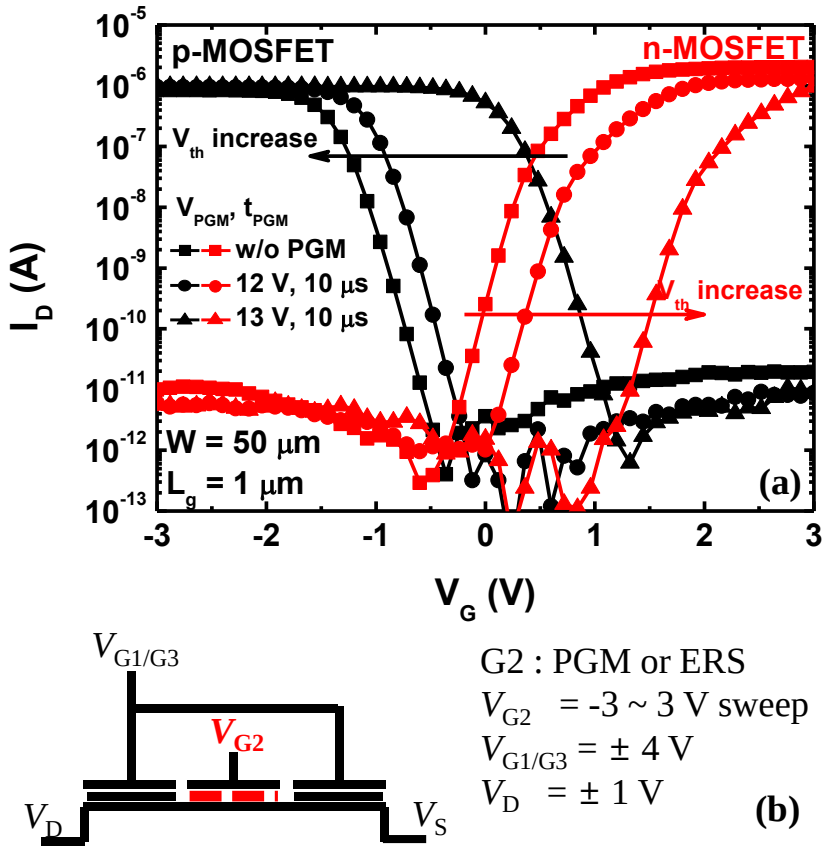


Fig. 4.6. (a) I_D-V_{G2} curves of *n*-/*p*-MOSFETs measured from a single reconfigurable device. Solid square symbols represent the curves without programming. The programming bias is applied to the G_2 for 10 μs. Solid circle and triangle symbols stand for the curves, respectively, with the programming biases of 12 and 13 V. (b) Device symbol and a bias scheme for the I_D-V_{G2} curves. The dashed line in the device symbol stands for PGM or ERS state of the charge storage layer on the G_2.

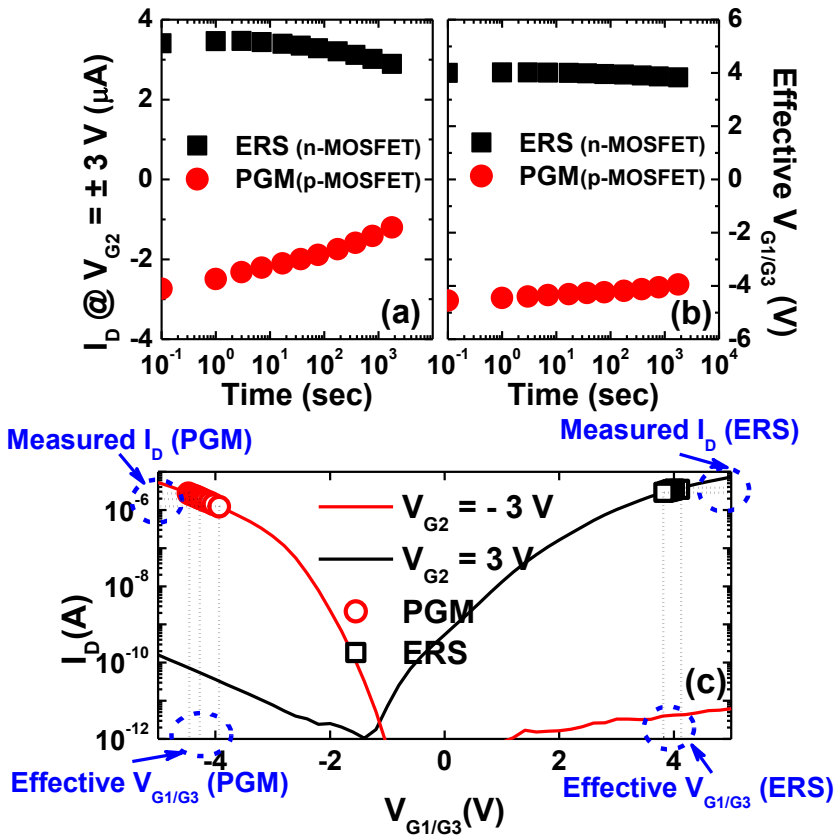


Fig. 4.7. Retention characteristics of the Si_3N_4 storage layer of the gate insulator stack on the G_1 and G_3 at $V_{G1/G2/G3} = V_D = V_S = 0$. (a) I_D (at $V_{G2} = \pm 3$ V) drift of *p*- and *n*-MOSFETs at programmed and erased states. (b) Drift of effective $V_{G1/G3}$ corresponding to the I_D drift. (c) Measured I_D-$V_{G1/G3}$ at the V_{G2} of ± 3 V where effective $V_{G1/G3}$s are obtained from I_D drift. Square and circle symbols in (c) are measured I_D-$V_{G1/G3}$s in (a) as time goes by.

4. 3 *p-n* / *n-p* diode operations

A reconfigurable device can be transformed to a diode as well as the MOSFET. In diode operation, the poly-Si body above each bottom gate can be electrically doped independently. By applying a positive (or negative) bias to the tied G_1/G_2 and a negative (or positive) bias to the G_3, *n-p* (or *p-n*) junction can be obtained. Fig. 4.8 shows measured *I-V* curves of *n-p* and *p-n* diodes from the same device used in MOSFET operation. $V_{G1/G2} = -V_{G3}$ is +4 V for *n-p* and -4 V for *p-n* diode. The ideality factor obtained from the slope of the forward bias sweep is between 1 and 2, which indicates conventional poly-Si diode characteristics with both diffusion and space charge region recombination current [35]. The related energy band diagrams are shown in Fig. 4.9. To make an *n-p* diode, the G_1 and G_2 are positively biased, and the G_3 is negatively biased. Therefore, e^- and h^+s are induced in the poly-Si body above the G_1/G_2, and G_3, respectively. As a result, the *n-p* junction is formed in the poly-Si body between the G_2 and G_3. By changing $V_{G1/G2}$ and V_{G3}, the doping concentration of corresponding poly-Si body is

modulated and the built-in potential of the *n-p* junction can be adjusted. Similarly, *p-n* junction can be realized by applying a positive $V_{G1/G2}$ and a negative V_{G3}. This result implies that the cathode and the anode of a diode can be changed. The simulated conduction band contour of diode operations as a parameter of V_D is also shown in Fig. 4.10. In this work, the *n-p* or *p-n* junction is formed at $V_{G1/G2}$ = $-V_{G3}$ = ± 4 V to reduce parasitic effect from the Schottky junction at the source/drain regions. Note that the diode operation can be realized by programing/erasing the charge storage layer on the bottom gates similar to MOSFET operation. In this case, a diode can be operated with only 2 electrodes after programming/erasing the charge storage layer.

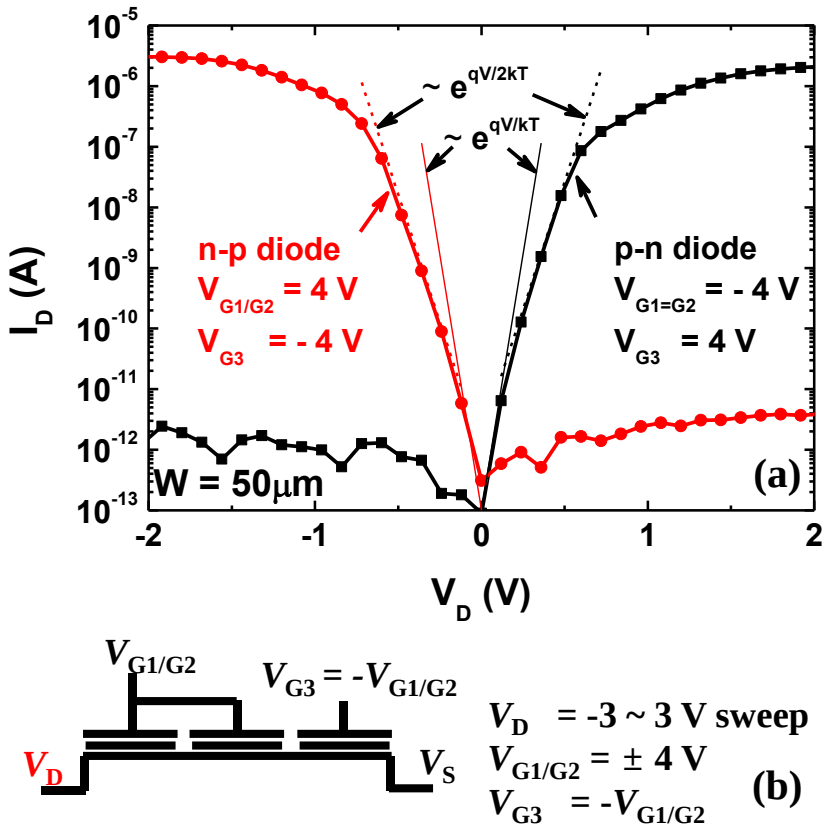


Fig. 4.8. (a) *I-V* curves of *n-p* and *p-n* diodes measured from a single reconfigurable device. (b) A bias scheme for *n-p and p-n* diode operations. $V_{G1/G2} = -V_{G3}$ is 4 V for *n-p* diode and -4 V for *p-n* diode. The slopes of q/kT and q/2kT are attributed to diffusion and recombination, respectively.

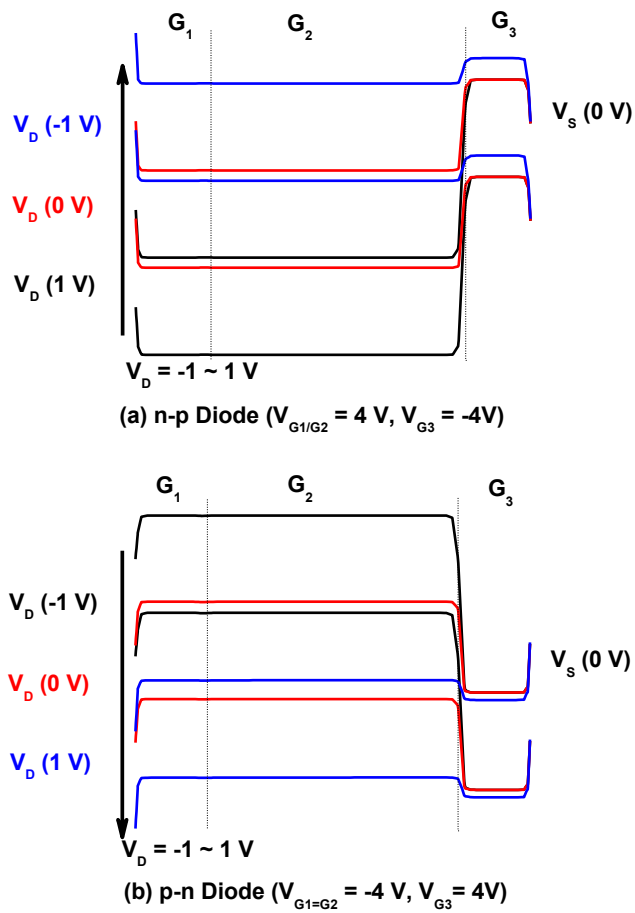


Fig. 4.9. Simulated energy band diagrams corresponding to the operation modes of the *n-p* and *p-n* diodes. (V_D = -1, 0, 1 V) Schottky junction exists at S/D but most of the V_D drops across *n-p*/*p-n* junction.

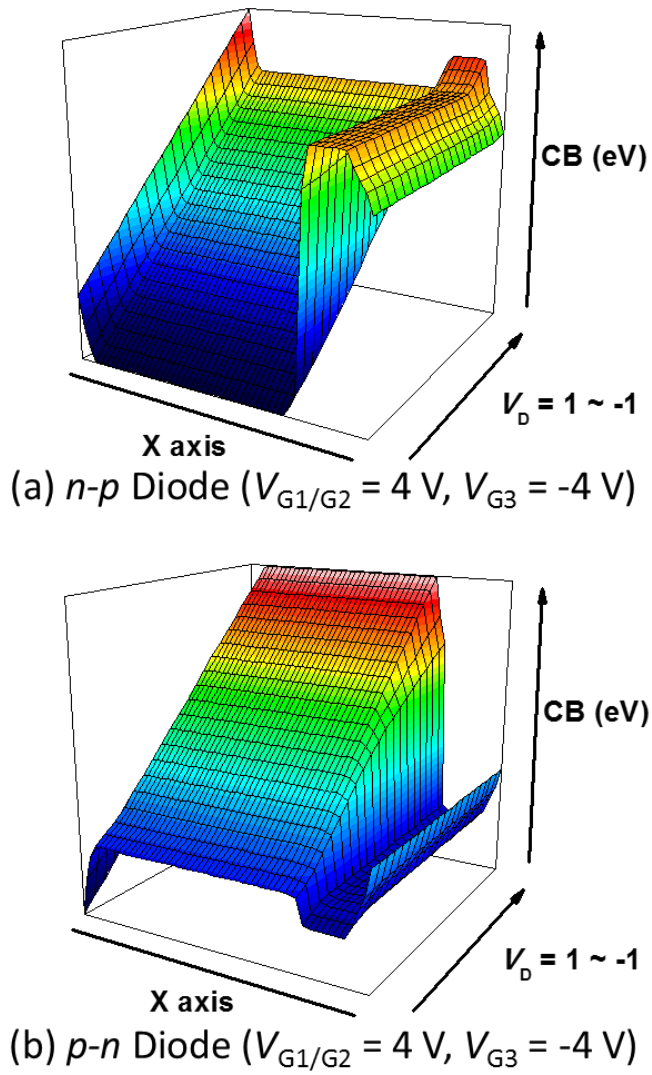


Fig. 4.10. Simulated conduction band contour of (a) *n-p* and (b) *p-n* diodes as a parameter of V_D.

4. 4 Logic Gate Operations

In order to evaluate the performance of a logic gate composed of the RFETs, we demonstrate inverting performance of a CMOS inverter with two RFETs having equal *W*/*L*. Reasonable transfer curves of a full-swing CMOS inverter are shown as a parameter of V_{DD} in Fig. 4.11. Logic transition is occurred at ~0.5V_{DD} for given V_{DD}s of 4, 5 and 6 V because the V_{th}s of both RFETs are controlled to have similar I_{on}. Fig. 4.12 shows reasonable transient response from the same CMOS inverter when the load capacitance is large (~2pF). As discussed in the chapter 3.3, the logic gate with four identical RFETs such as NAND and NOR gate characteristics cannot be properly obtained due to the incomplete isolation between adjacent devices. Optimized device structure and NAND/NOR gate operation will be discussed in the chapter 6.

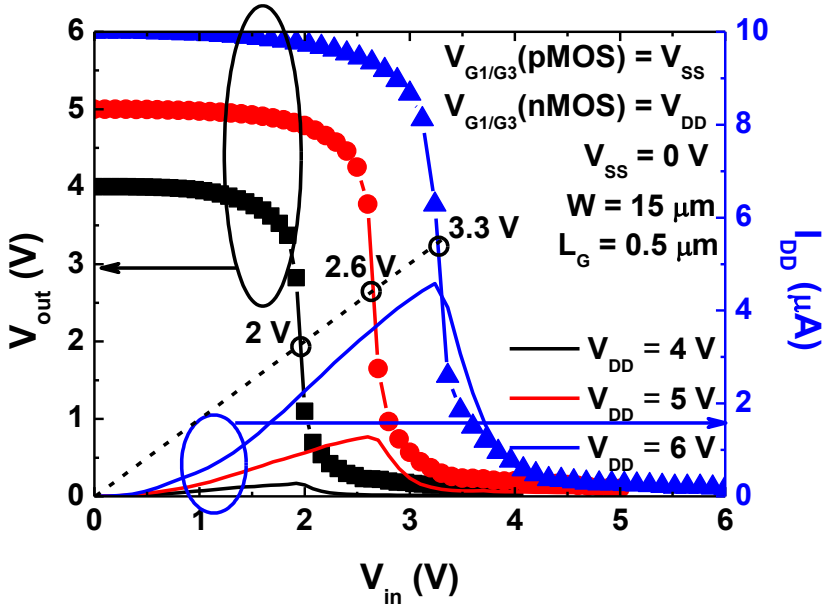


Fig. 4.11. Measured transfer characteristics of CMOS inverter composed of two reconfigurable devices as a parameter of V_{DD}. The V_{th}s of both devices are controlled by G_2 to give similar I_{on}. G_1/G_3s of n- and p-MOSFET are connected to V_{DD} and V_{SS}, respectively.

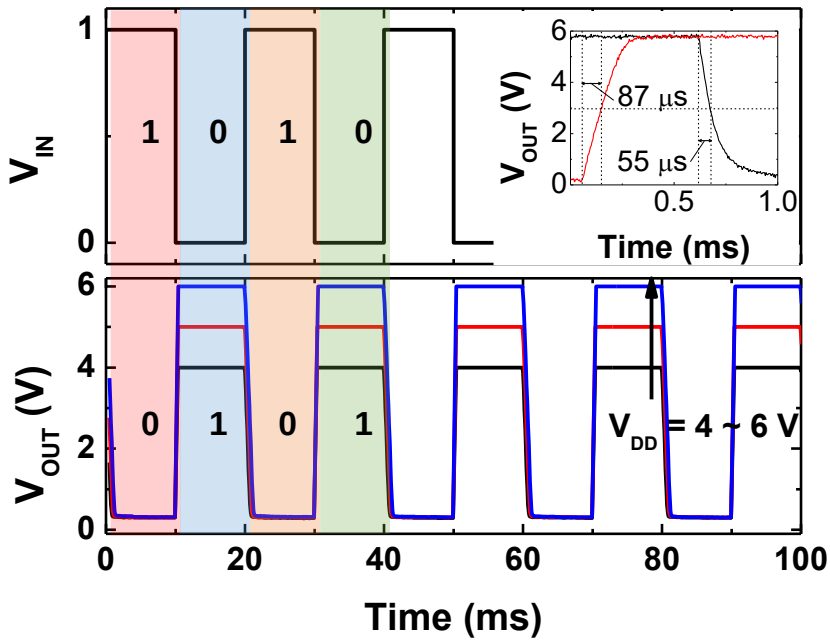


Fig. 4.12. Measured transient response of CMOS inverter as a parameter of V_{DD} (4, 5 and 6 V) at a load capacitance (C_L) of ~2 pF. The biasing scheme of G_1/G_3 is the same as that in Fig. 4.9. Inset shows magnified transient response. Propagation delay is less than 100 μs.

Chapter 5

Analysis of Schottky Contact Resistance

5. 1 Schottky barrier modulation by bottom gate bias

In both MOSFET and diode characteristics discussed above, the contact resistance is ~50 kΩ when V_{G1} (or V_{G3}) is ± 4 V. The resistance is relatively large and should be reduced. If we reduce the thickness of the poly-Si body butted to the metal, the resistance is significantly reduced. If the gate insulator stack on the bottom gates is improved in terms of quality, thickness, and material, the resistance be effectively reduced. To observe the relation between V_{G1} (or V_{G3}) and the resistance of Schottky junction, the S/D Schottky junction current is analyzed by changing $V_{G1/G3}$. I_D-$V_{G1/G3}$ at V_{G2} = ± 4 V and I_D-$V_{G1/G2/G3}$ curves are shown in Fig. 5.1. Generally, V_D is 1 V for *n*-MOSFET, and -1 V for *p*-MOSFET at a fixed V_S of 0 V. However, V_D and V_S are fixed to 1 V and 0 V in the measurement of both *n*- and *p*-MOSFETs for convenience. Therefore, the actual V_{GS} is less by 1 V

than V_G in the measurement of *p*-MOSFET. Consequently, the I_D of *p*-MOSFET is overestimated in comparison with that of *n*-MOSFET. In the I_D-$V_{G1/G3}$ curves, the channel is fully turned-on with e^- (or h^+) at V_{G2} = 4 V (or -4 V). Interestingly, I_D-$V_{G1/G2/G3}$ curve is identical to I_D-$V_{G1/G3}$ curves in two regions: one is $V_{G1/G3} > 0$ at V_{G2} = 4 and the other is $V_{G1/G3} < 0$ at V_{G2} = -4 V, which means the channel resistance at $|V_{G2}| \geq |V_{G1/G3}|$ is negligible compared to that of contact resistance. Therefore, the current flowing through Schottky junction determines total current, and is modulated by controlling $V_{G1/G3}$. Since the resistance of reverse biased Schottky junction is obviously larger than that of forward biased Schottky junction, the I_D measured in I_D-$V_{G1/G3}$ curves at V_{G2} = 4/-4 V is e^-/h^+ tunneling current of reverse biased Schottky junction [35], and most of V_D drops across the source as depicted in Fig. 4.3. The simulated contour plots of tunneling rate and e^-/h^+ current density at each bias condition ($V_{G1/G2/G3}$ = 4 or -4 V) are shown in Fig. 5.2. Fig. 5.2(a) shows that the I_D current flows by tunneling mechanism through Schottky reverse junction which is consistent with above explanation. Since the body is undoped poly-Si, both e^- and h^+ can tunnel from the source and flow

through the channel. Fig. 5.3 shows schematic band diagrams describing the carrier behavior in *n-/p*-MOSFET operation as a parameter of $V_{G1/G3}$. As discussed above, increasing $V_{G1/G3}$ enhances the band bending in the poly-Si layer for the source and drain, thus e^-/h^+ tunneling barrier becomes narrow and effective tunneling barrier height becomes low. As a result, the tunneling current through Schottky reverse junction increases as $V_{G1/G3}$ increases as shown in Fig. 5.1.

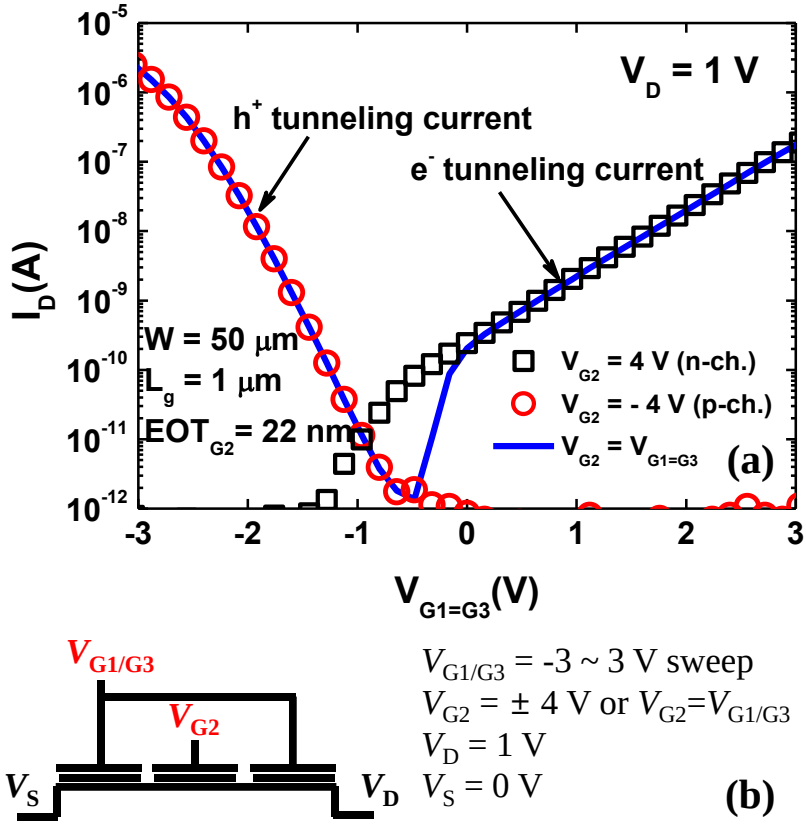


Fig. 5.1. (a) I_D-$V_{G1/G3}$ curves of *n*-/*p*-MOSFETs, measured from single reconfigurable device. (b) A bias scheme for this measurement. I_D-$V_{G1/G3}$ is measured at V_{G2} = 4 V (black square), V_{G2} = - 4 V (red circle), and V_{G2}=$V_{G1/G3}$ (blue line). V_D = 1 V and V_S = 0 V.

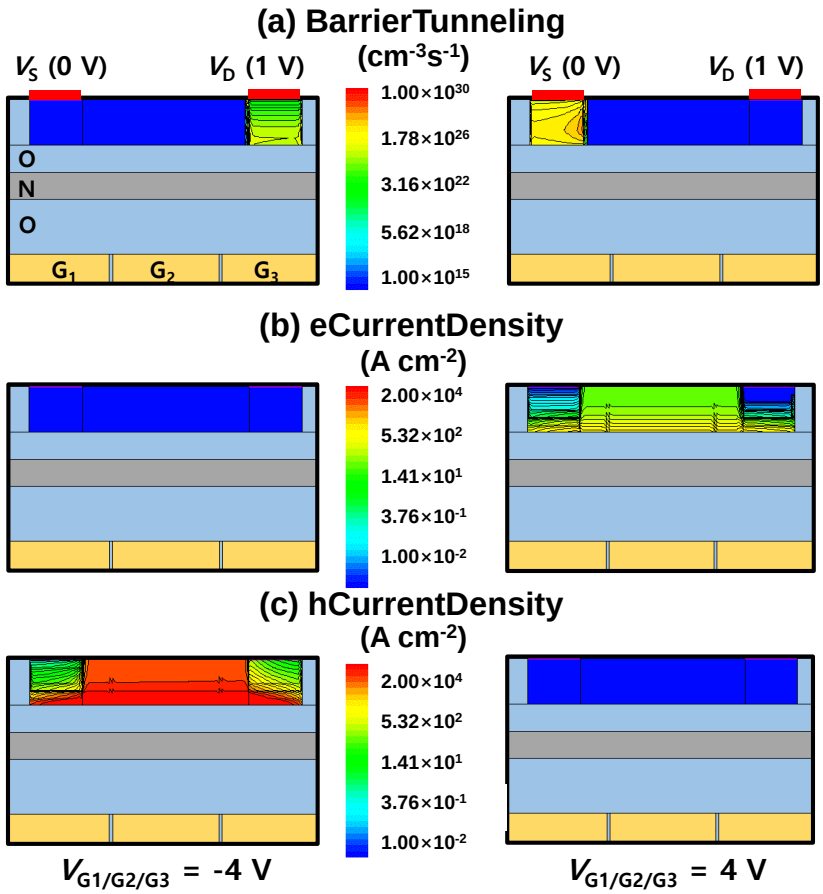


Fig. 5.2. Simulated contour plot of (a) e^-/h^+ barrier tunneling, (b) e^- and (c) h^+ current density sequentially from the top, at $V_{G1/G2/G3}$ = 4 V (e^- current mainly flows) and $V_{G1/G2/G3}$ = - 4 V (h^+ current mainly flows).

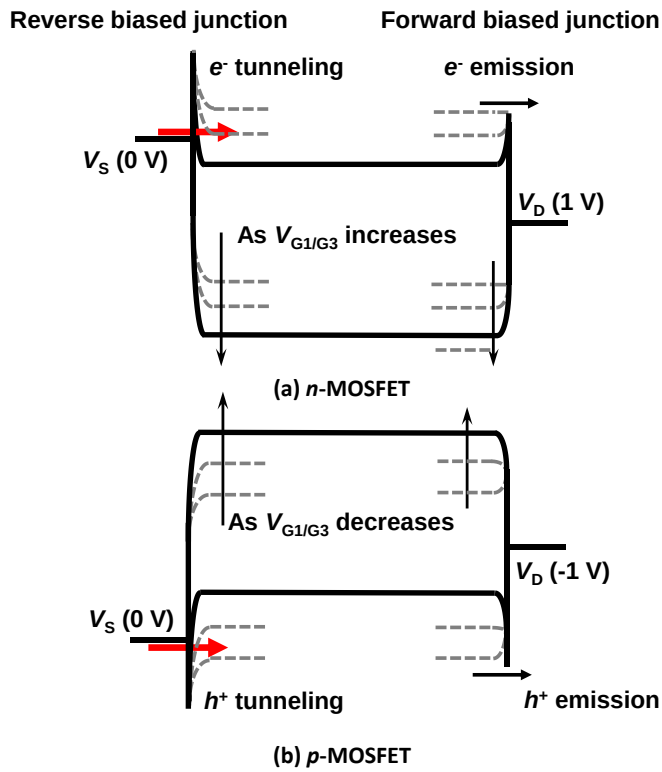


Fig. 5.3. Schematic energy band diagrams corresponding to the operation modes of the (a) *n*- and (b) *p*-MOSFET operations as a parameter of $V_{G1/G3}$. Both source and drain Schottky junctions are modulated by $V_{G1/G3}$. The red arrow indicates the direction of carrier tunneling.

5. 2 Temperature Dependence of Reconfigurable Device

To analyze further current behavior of reconfigurable MOSFET and diode, temperature effect in these devices is investigated. Fig. 5.4 shows I_D-$V_{G1/G2/G3}$ curves as a parameter of temperature (T). When the $|V_{G1/G2/G3}|$ is larger than 1 V, T dependency of I_D becomes weak. The tunneling mechanism has very weak dependence on T, and the I_D hardly changes as T increases at a high $V_{G1/G2/G3}$, indicating the I_D is determined by Schottky junction reverse current and dominated by tunneling mechanism as we described in the chapter 5.1. Fig. 5.5 shows T dependence of I-V curves in reconfigurable MOSFET and diode. The SS increases, and the on-current for MOSFET and diode increases as T rises because the mobility of intrinsic poly-Si body increases [37]. The MOSFET and diode leakage current also increases at a high T since more electron-hole pair are generated in depletion region. In the same manner, the I_D increases when the $|V_{G1/G2/G3}| < 1$ V in Fig. 5.4.

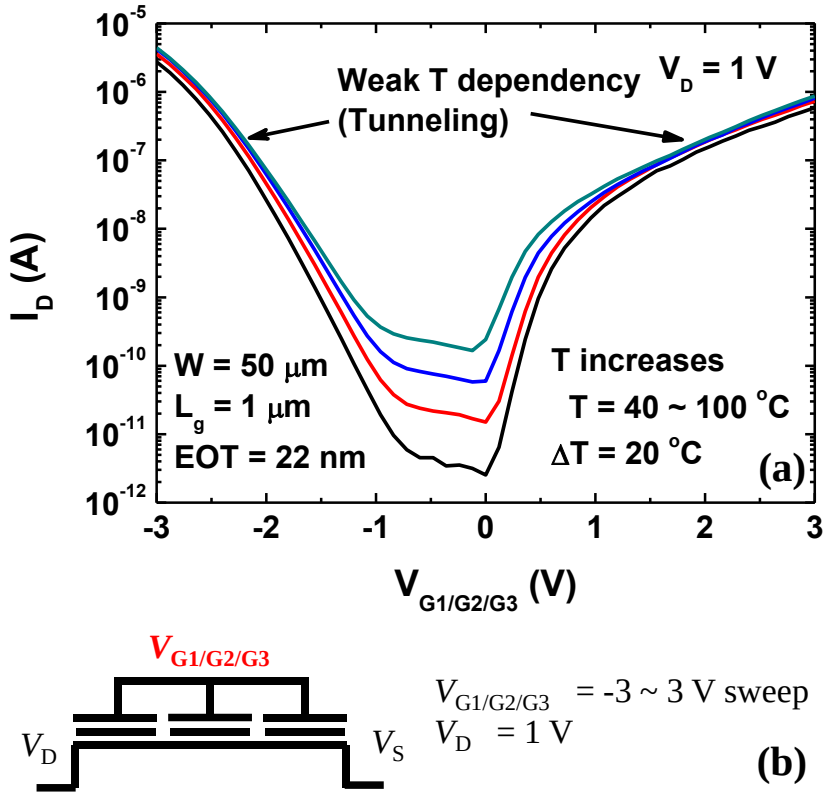


Fig. 5.4. (a) I_D-$V_{G1/G2/G3}$ curves measured from a reconfigurable device as a parameter of T (40 – 100 ºC, 20 ºC step). (b) A bias scheme for this measurement, $V_{G1/G2/G3}$ is swept at V_D = 1 V. T dependency becomes weak as I_D increases. The red arrow indicates the direction of carrier tunneling.

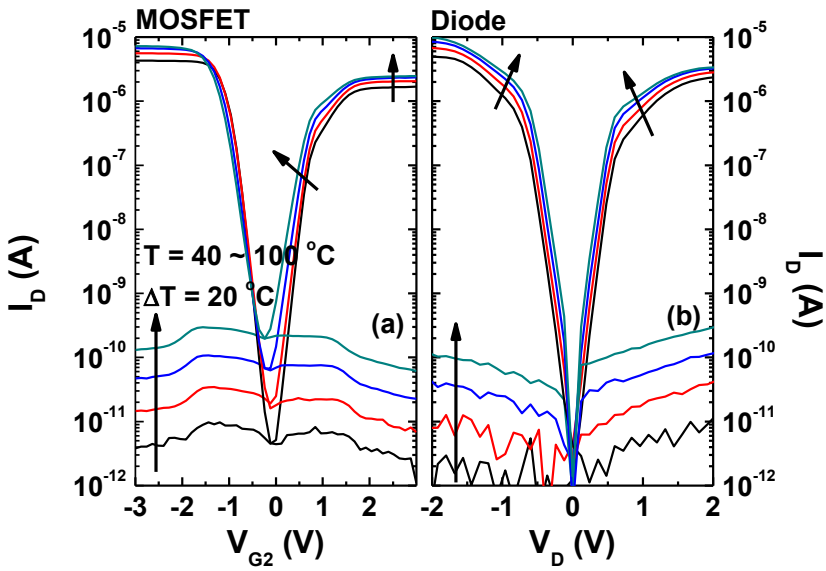


Fig. 5.5. (a) I_D-V_G curves of MOSFETs and (b) *I*-*V* curves of diodes as a parameter of *T*, measured from a single reconfigurable device. *T* increased from 40 to 100 °C with 20 °C step. The SS of MOSFET and the current of both MOSFET and diode rises as *T* increases.

5. 3 Noise characteristics of MOSFET with bottom gate biases

We investigate low frequency noise characteristics of a reconfigurable device. Fig. 5.6 shows noise power spectral density (S_{ID}) versus I_D curves measured from reconfigurable *n*- and *p*-MOSFETs. Fig. 5.6(a) shows S_{ID}-I_D curves when a device is working as MOSFET at $V_{G1/G3}$ = ± 4 V. When the I_D (i.e. V_{G2}) is small, the slope is proportional to I_D^2. It is considered that the noise behavior is dominated by the channel carrier number fluctuation. When the I_D increases further, the slope of S_{ID}-I_D is changed from I_D^2 to I_D^4. It indicates that the noise behavior is dominated by contact noise [38]. The S_{ID}-I_D slope in *p*-MOSFET is changed at relatively higher current level than that of *n*-MOSFET, which indicates *p*-MOSFET has smaller contact resistance than *n*-MOSFET. Fig. 5.6(b) shows S_{ID}-I_D curves when $V_{G1/G3}$ is changed to modulate the barrier at the Schottky junction at V_{G2} = ± 4 V. The S_{ID}-I_D curves shows the slope of ~I_D^2, which indicates Schottky reverse current noise behavior [39]. Typically, Schottky diode noise behavior is analyzed by changing the bias between the cathode and anode. However, in our experiment, the $V_{G1/G3}$ is

changed to modulate the barrier at the Schottky junction. Since the poly-Si layer is thin (16 nm) enough to fully depleted, we can assume that the $V_{G1/G3}$ drop across the poly-Si active layer is linear and proportional to the $V_{G1/G3}$ until induced carriers are accumulated on surface. Therefore, when I_D is higher than 10 nA, the carriers are accumulated in the poly-Si body above the G_1/G_3, and then the relation between I_D and S_{ID} becomes different.

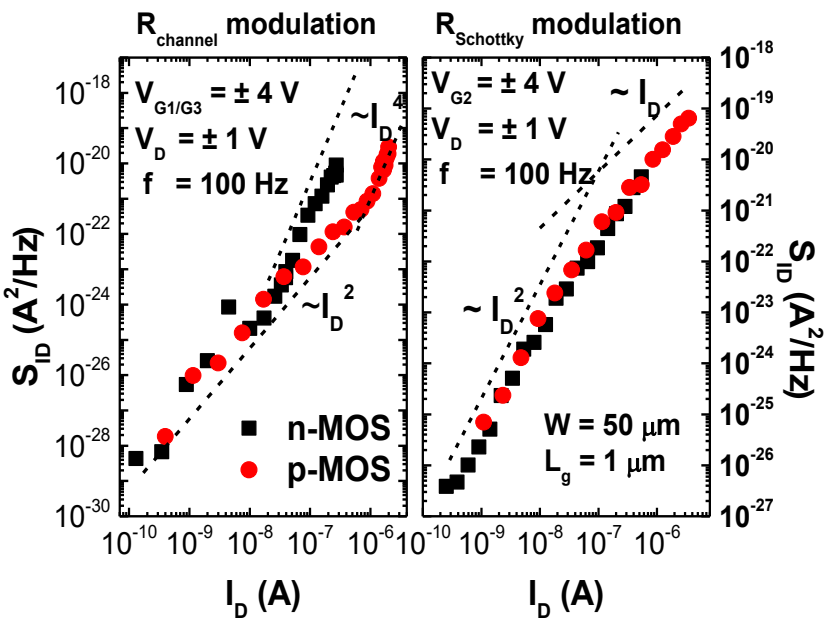


Fig. 5.6. S_{ID}-I_D curves of *n*-/*p*-MOSFET (black square and red circle, respectively) at frequency of 100 Hz with (a) channel resistance modulation by changing V_{G2} ($V_{G1/G3}$ = ± 4 V) and (b) Schottky junction modulation by changing $V_{G1/G3}$ (V_{G2} = ± 4 V), measured from a single reconfigurable device. The V_D is 1 V and -1 V for *n*- and *p*-MOSFET.

Chapter 6

Process Optimization and On-Current Improvement

6. 1 Performance of Proposed Device

As discussed in the chapter 3 and 4, the reconfigurable device fabricated by poly-Si shows reasonable characteristics such as subthreshold swing of ~120 mV/dec and on/off current ratio (I_{on}/I_{off}) of ~10^6 that are comparable to those of conventional poly-Si devices. However, it has some problems such as CMP uniformity, inappropriate circuit application (NAND/NOR), and narrow PGM/ERS condition. To solve the problems discussed in previous chapters and improve device performance, the researches for the process optimization and on-current improvement have been conducted. In this chapter, with process optimization, the uniformity of the device and device isolation are improved. Therefore, enhanced PGM/ERS performance and circuit application (NAND/NOR) have been achieved. In addition, we also conducted experiments to

obtain increased on-current by reducing Schottky contact resistance that is discussed in the chapter 5. The S/D metal split and reducing EOT of the gate stack have been studied.

6. 2 Process Optimization

6. 2. 1 SiO_2 Fin Method

To improve the uniformity of the bottom gate structure, the SiO_2 fin method is introduced to fabricate the bottom gate array. The 3-D schematic views of key fabrication process steps of the SiO_2 fin method are shown in Fig. 6.1. The key fabrication steps in detail are explained as follows. To form an isolation layer, a 300 nm-thick thermal oxide is grown on a 6-inch p-type Si wafer by wet oxidation process. An a-Si layer is formed on a silicon dioxide (SiO_2) grown on the wafer. A layer of SiO_2 is thermally grown on the a-Si layer (Fig. 6.1(a)). The SiO_2 layer is patterned by photo lithography (1^{st} mask) and dry etch process (Fig. 6.1(b)). The Si_3N_4 layer is deposited and etched to form a nitride spacer along the oxide sidewall (Fig. 6.1(c)). The SiO_2 layer is removed by wet etch process, therefore, only nitride spacer is remained (Fig. 6.1(d)). After that, using the nitride spacer as a hard mask, the a-Si and SiO_2 layers are patterned by dry etch process (Fig.

6.1(e)). The nitride spacer is stripped by wet etch process, and the a-Si layer is removed by isotropic etch process. Oxide fin thickness can be reduced by SiO_2 wet etch process in diluted HF (dHF) (Fig. 6.1(f)). An n^+ poly-Si is deposited as shown Fig. 6.1(g), and then touch polishing is done by using CMP process for the planarization of the surface of the poly-Si layers and the oxide layer between 1^{st} and 2^{nd} poly-Si as shown in Fig. 6.1(h). The SEM images corresponding to Figs. 6.1(d), (e), and (g) are shown in Figs. 6.2(a), (b), and (c), respectively.

The CMP pattern density of the bottom gate formation process using SiO_2 fin method is significantly reduced compared to poly-Si CMP method discussed in the chapter 3, therefore, the better flatness and uniformity of the bottom gate structure can be obtained by a touch polishing of CMP process. In addition, there is no remaining poly-Si spacer since the isolation oxide has a positive slope as shown in Fig. 6.3. The devices isolation can be significantly enhanced, therefore, circuit operation including NAND/NOR can be achieved, and enhanced PGM/ERS characteristics can be obtained. We experimentally verified that all bottom gates and individual devices are completely isolated from each other

with a leakage current level around 1 pA. Furthermore, the higher bias can be applied to the devices due to the stable bottom gate structure, which will lead to an increase in on-current. Subsequent fabrication processes after bottom gate formation is the same as in the chapter 3.3. A TEM images of the fabricated device are shown in Fig. 6.4. The isolation oxide has a positive slope, and the fin width is controlled less than 30 nm. The flatness of bottom gate array is improved, moreover, the uniformity of the entire wafer is increased significantly.

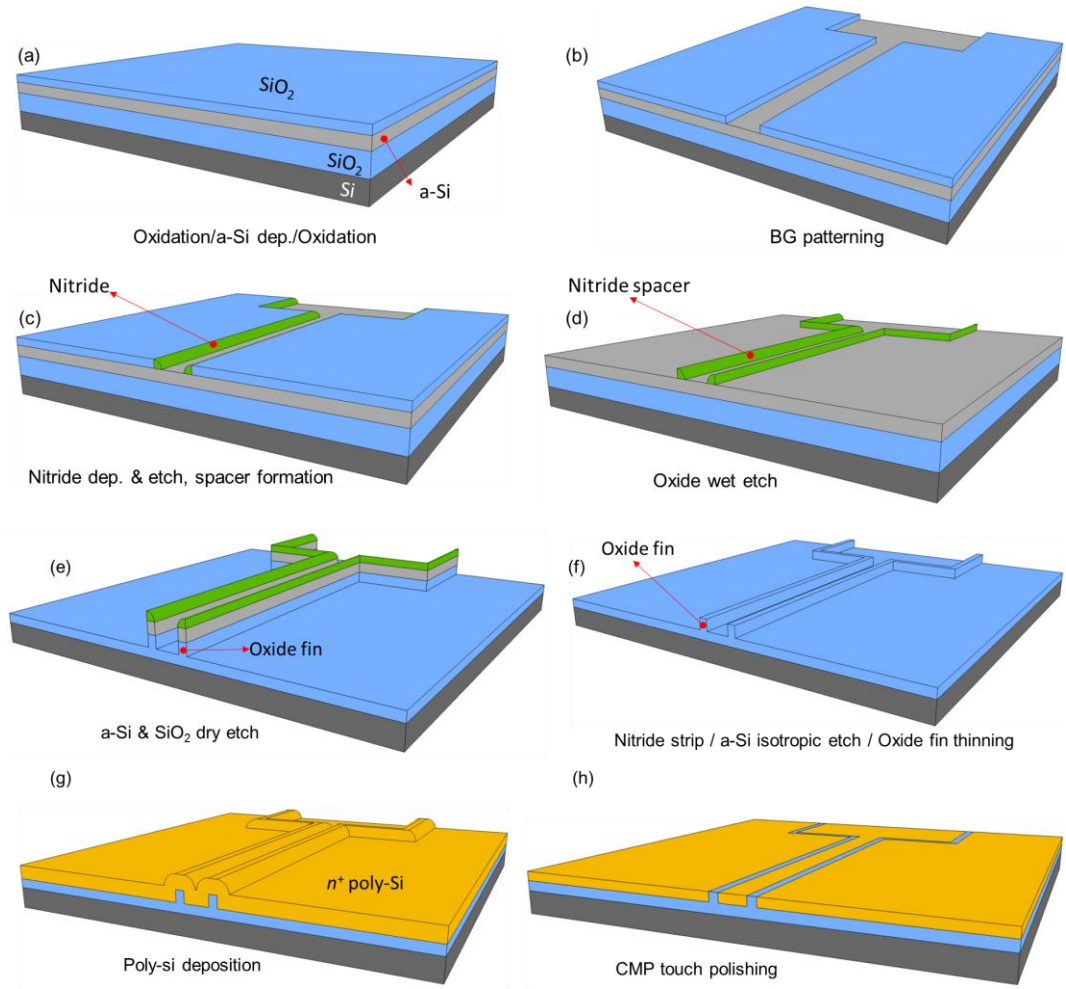


Fig. 6.1. The key process flow to fabricate the bottom gate structure by SiO_2 fin method.

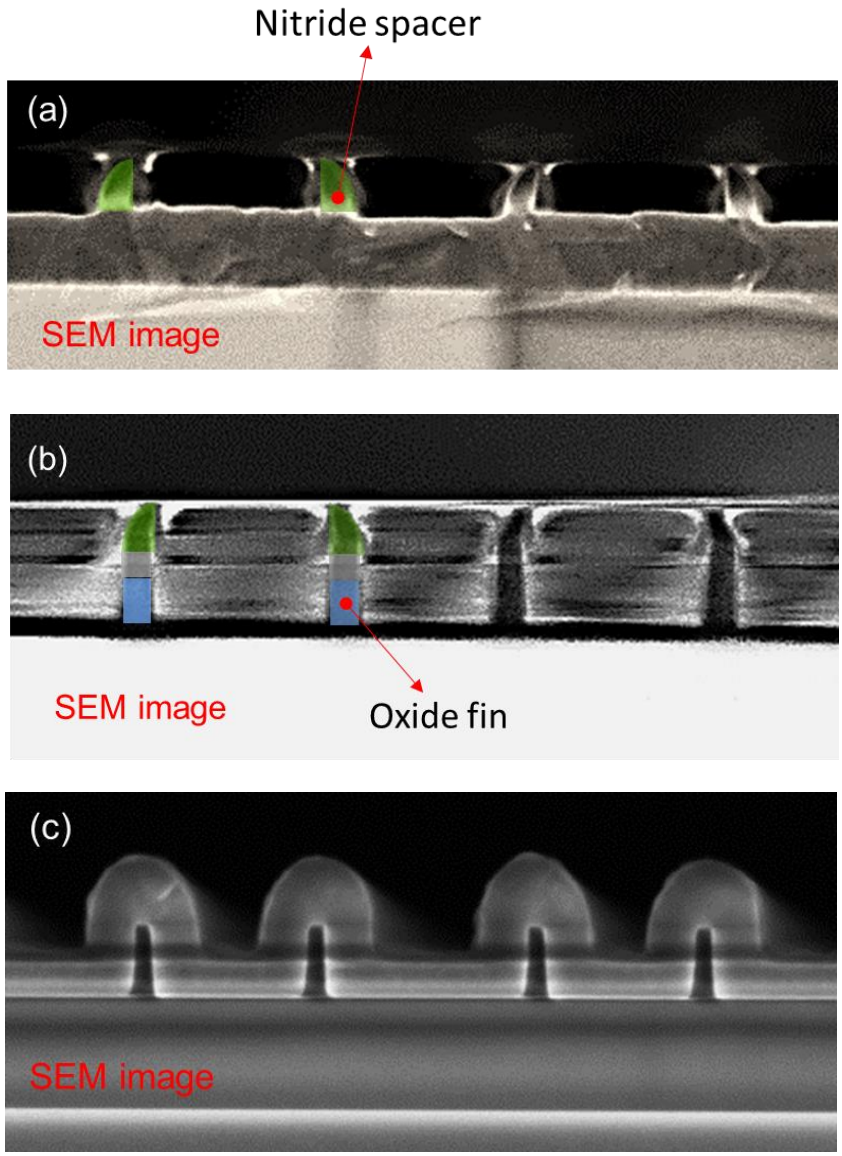


Fig. 6.2. The SEM images corresponding to Figs. 6.1(d), (e), and (g) are shown in (a), (b), and (c), respectively.

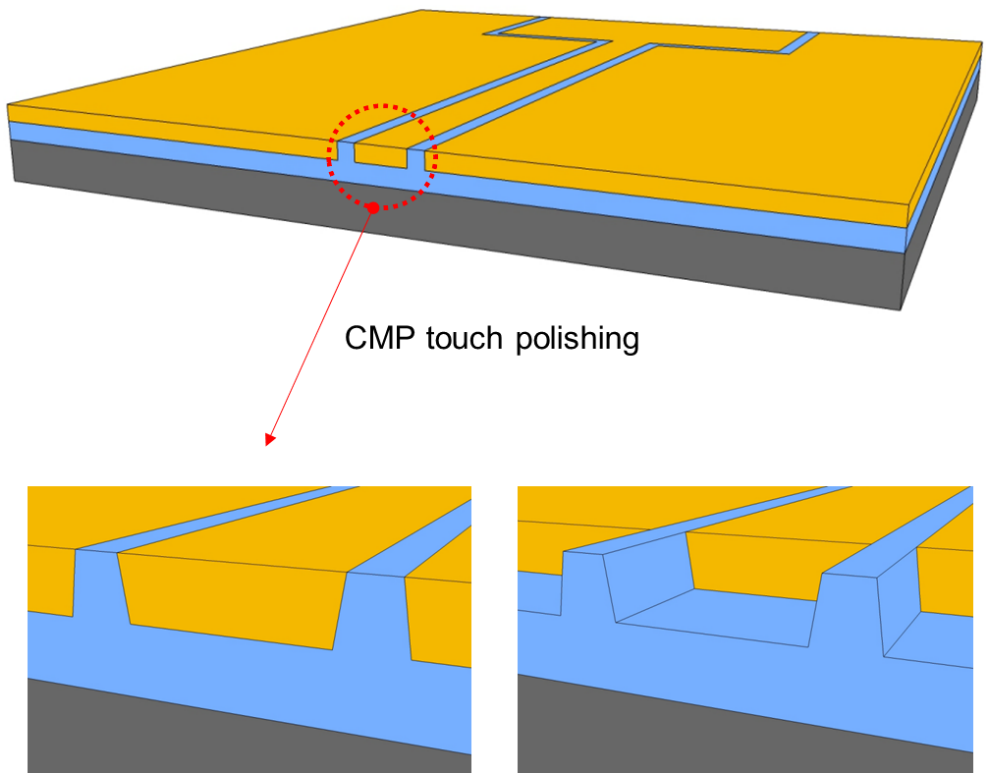


Fig. 6.3. 3-D schematic views of bottom gate structure fabricated by SiO_2 fin method. The isolation oxide has positive slope and there is no remaining poly-Si spacer.

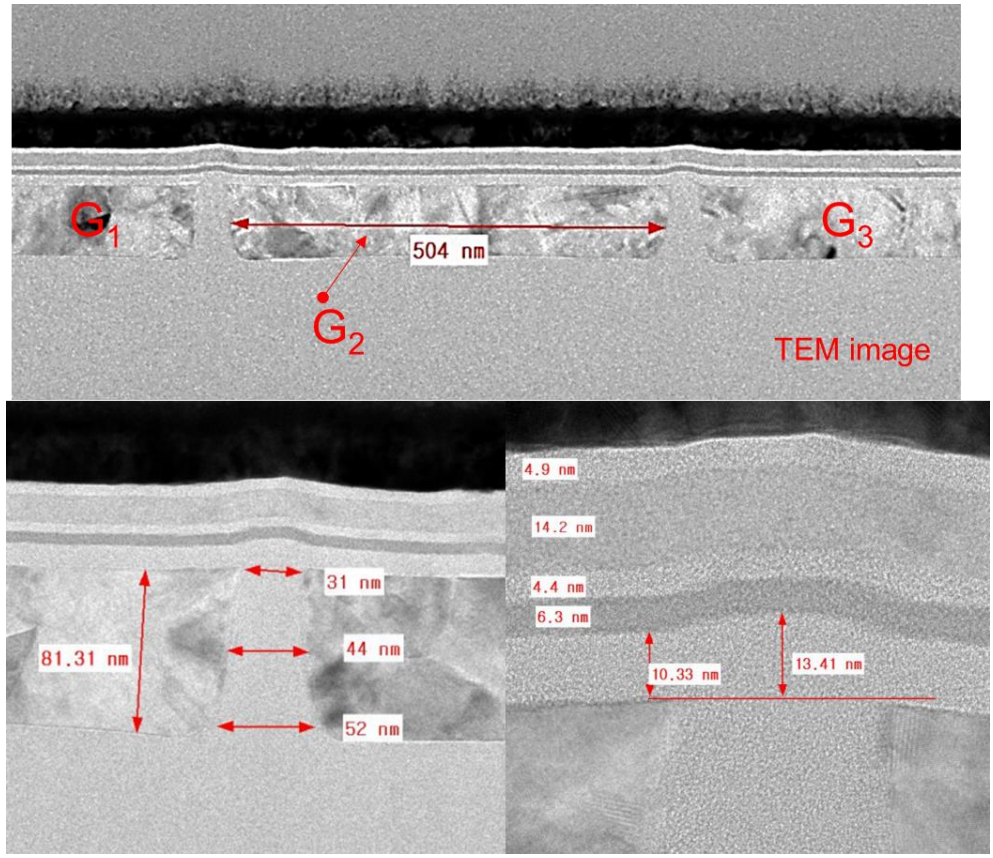


Fig. 6.4. TEM images of fabricated device using SiO_2 fin method.

6. 2. 2 Enhanced *I*-*V* characteristics

Figs. 6.5 and 6.6 show measured drain current (I_D) versus V_{G2} as a parameter of the G_1 and G_3 bias ($V_{G1/G3}$), and I_D versus V_D as a parameter of the V_{G2}, respectively, in a single reconfigurable device fabricated by SiO_2 fin method having a channel length of 1 μm and a width of 10 μm, demonstrating successful working of *n*-/*p*-MOSFETs. The drain biases (V_D) are fixed at 1 V and -1 V, respectively, for *n*- and *p*-MOSFETs. Note that the magnitude of on-current (I_{on}) in *n*-/*p*-MOSFETs is increased compared to those in Fig. 3.1 because the higher bias can be applied to the bottom gate array, resulting in reduced Schottky contact resistance at S/D. The I_{on}/I_{off} is increased from ~10^6 to ~10^7. Fig. 6.7 shows the transfer curves measured from the bottom gate, top gate, and double gate operation, respectively. The SSs are 90 mV/dec and 98 mV/dec for *n*- and *p*-MOSFETs, respectively, in double gate operation. The significant improvement on gate controllability is obtained in the double gate operation. The enhanced PGM/ERS characteristics are shown in Figs. 6.8 and 6.9. As shown in Fig. 6.8, precise V_{th} control is demonstrated by PGM at different bias conditions. Fig. 6.9(a) shows that the desired current level can be obtained by PGM/ERS. Furthermore, the symmetric characteristics of *n*-/*p*-MOSFETs can be obtained by PGM/ERS as shown in Fig. 6.9(b), which is imperative for circuit application. The enhanced logic gate operation is also demonstrated with optimized devices.

Fig. 6.10(a) shows undefined logic gate with four identical RFETs. This gate can be transformed to (b) NAND or (c) NOR gate by controlling V_1 and V_2. Measured transient responses shown in Fig. 6.10(d) verify successful transformation between logic gates. Note that the NAND/NOR gates can be realized by programing or erasing the BG of each RFET.

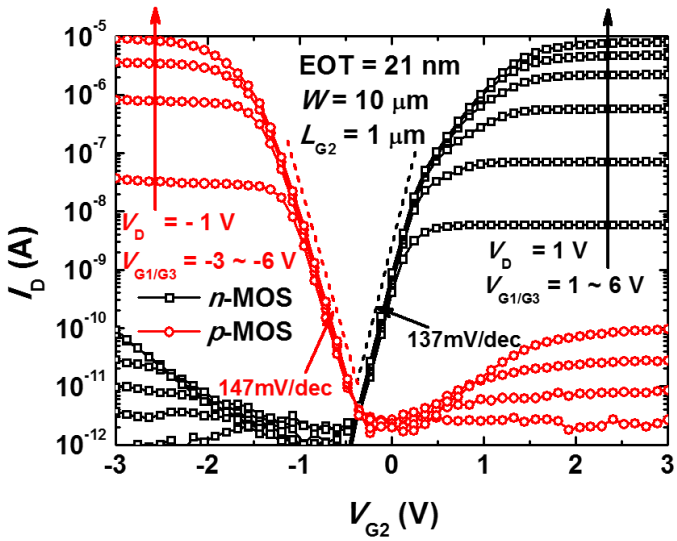


Fig. 6.5. Measured transfer curves as a parameter of $V_{G1/G3}$ from the optimized device.

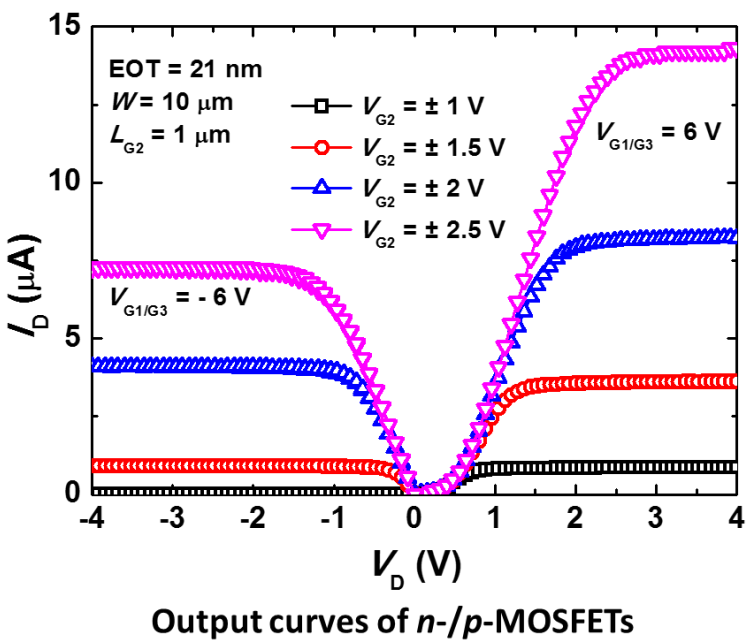


Fig. 6.6. Measured output curves as a parameter of V_{G2} from the optimized device.

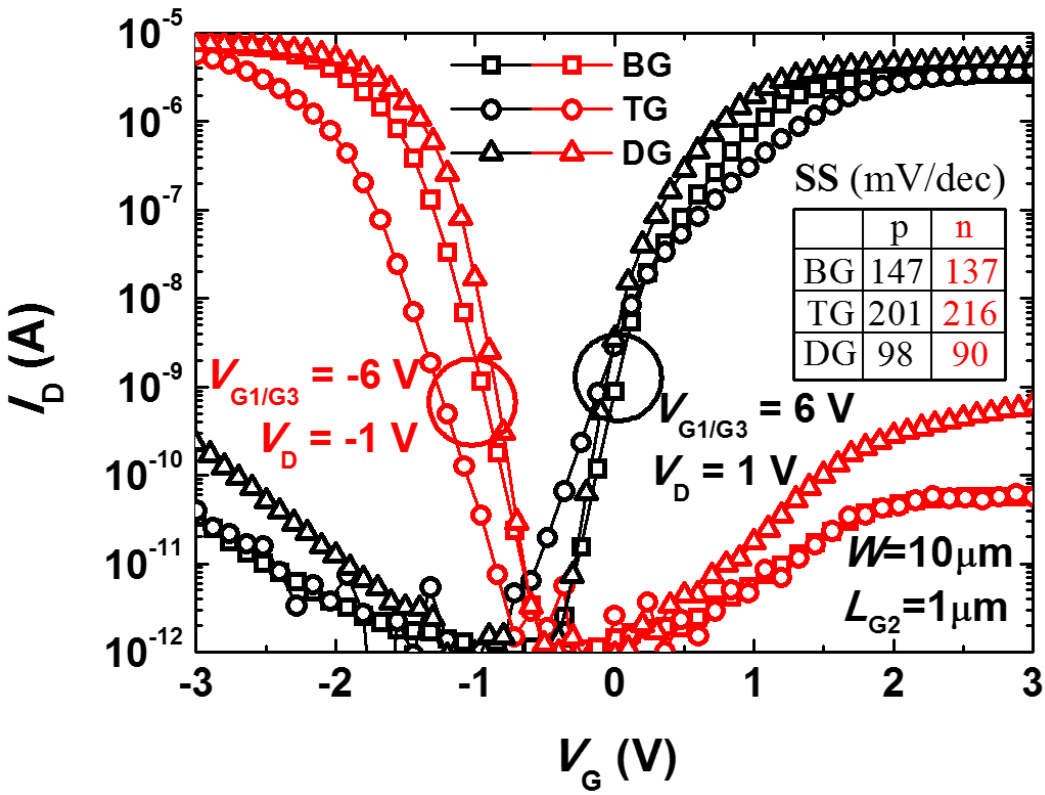


Fig. 6.7. Transfer curves measured from the bottom gate, top gate, and double gate operation, respectively.

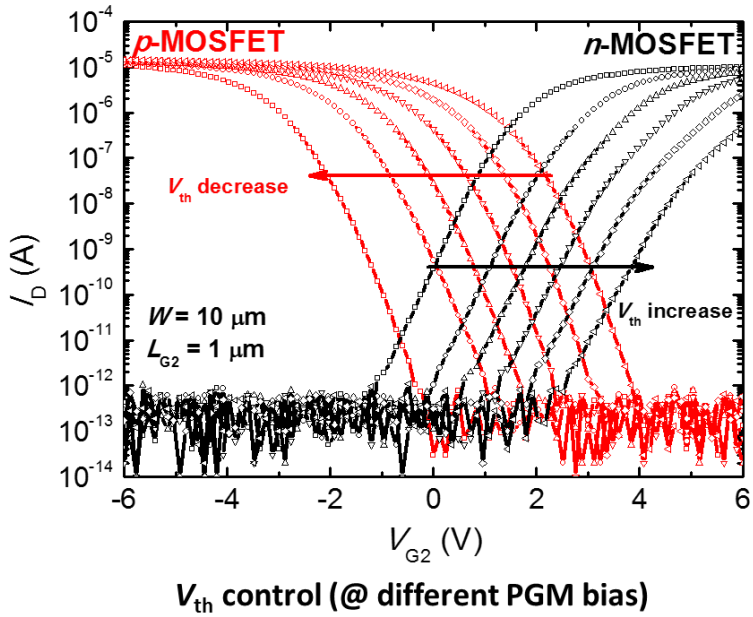


Fig. 6.8. Transfer curves of *n*-/*p*-MOSFETs showing precise V_{th} control by PGM G_2.

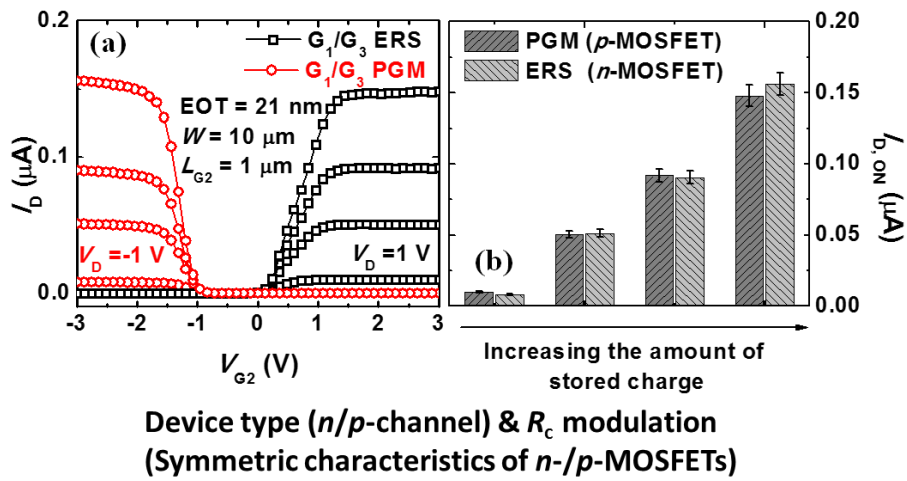
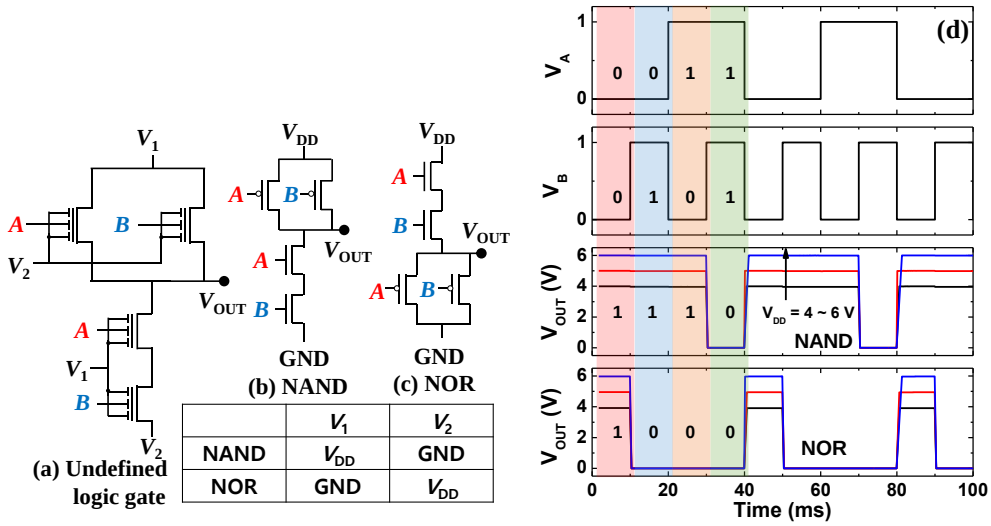


Fig. 6.9. (a) Measured I_D-V_{G2} curves of *n*-/*p*-MOSFETs with R_c modulation by controlling PGM/ERS state of both G_1 and G_3. (b) Both *n*-/*p*-MOSFETs have symmetric I_{on} with the amount of the stored charge. Well-matched I_D levels of *n*-/*p*- MOSFETs are demonstrated.



	V_1	V_2
NAND	V_{DD}	GND
NOR	GND	V_{DD}

Fig. 6.10. (a) The undefined gate works as (b) NAND or (c) NOR gate when V_1/V_2 are connected with V_{DD}/GND or GND/V_{DD}, respectively. (d) Measured transient response of CMOS NAND and NOR gates as a parameter of V_{DD} (4, 5 and 6 V).

6. 3 On-current Improvement

To study on the on-current improvement, we fabricated a poly-Si TFT using an n^+ wafer as shown in Fig. 6.11. By using this test device, S/D metal and gate stack EOT split test have been performed. For a metal split test, we compared transfer characteristics of devices with nickel silicide and aluminum S/D contact. In the devices using nickel silicide, the contact resistance changes in accordance with the different annealing conditions are observed as shown in Fig. 6.12. However, a metal which has low hole Schottky barrier must have relatively high electron Schottky barrier, and vice versa. In other words, the Schottky barriers for electron and hole are in the trade-off relationship. Therefore, S/D metal split is thought to be unsuitable way for the on-current improvement. On the contrary, noticeable on-current improvement is achieved as the gate stack EOT is reduced as shown in Fig. 6.13, which indicates that the enhanced on-current can be obtained in the devices with the high-k materials as a gate stack. Fig. 6.14 shows the simulation results based on the S/D metal and gate stack EOT split test, and it shows the same tendency with the experimental results.

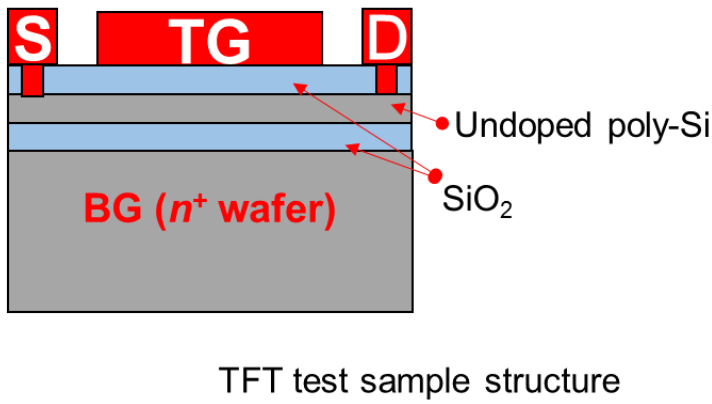


Fig. 6.11. Schematic cross-sectional view of TFT test sample structure for S/D metal and gate stack EOT split test.

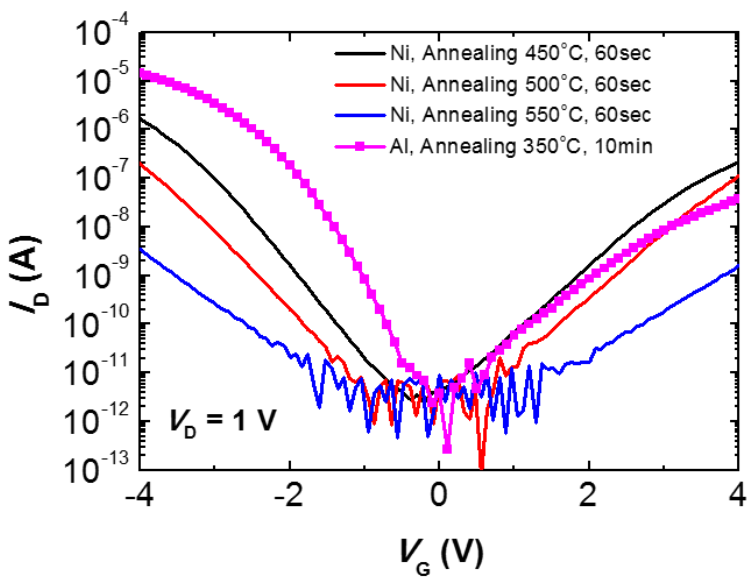


Fig. 6.12. Measured I_D-V_G curves from the TFT test sample with different S/D metal contact.

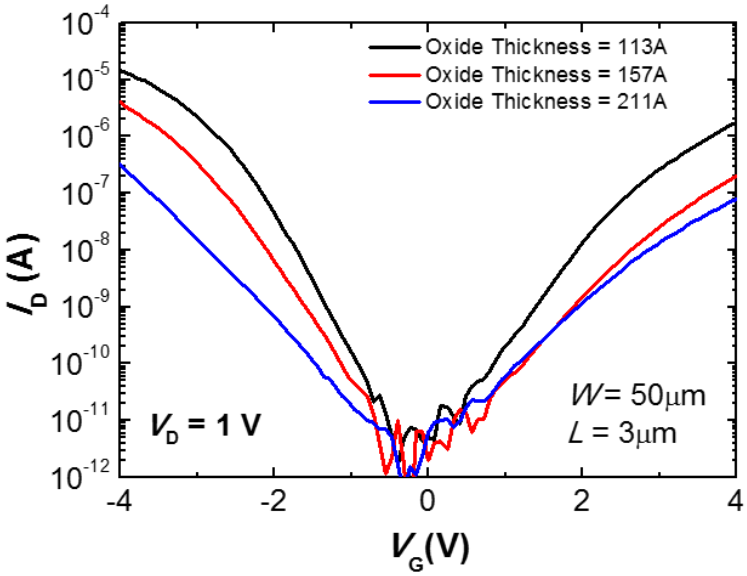


Fig. 6.13. Measured I_D-V_G curves from the TFT test sample with different gate oxide thickness.

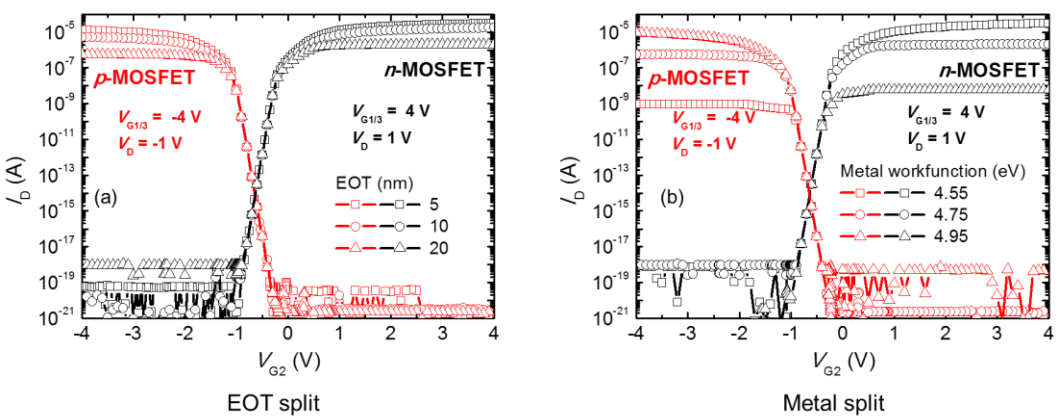


Fig. 6.14. Simulated transfer curves from the reconfigurable devices with different (a) gate stack EOT and (b) S/D metal contact.

Chapter 7

Conclusion

A novel reconfigurable device has been proposed, fabricated, and characterized. The proposed device was fabricated by conventional Si CMOS technology using only 6 (or 5) masks without implantation process. The device is very efficient in terms of device size, reliability, uniformity and reproducibility. We have demonstrated experimentally that a device can be operated in *n*-/*p*-MOSFETs and *n*-*p*/*p*-*n* diodes by changing biases to the bottom gates. In addition, by introducing programmable bottom gate array having non-volatile memory functionality, a device can be transformed to one of device types among *n*-/*p*-MOSFETs, *n*-*p* and *p*-*n* diodes depending on PGM/ERS states of the storage layer above the bottom gates. The device characteristics such as subthreshold swing (SS, ~120 mV/dec) and on/off current ratio (I_{on}/I_{off}, ~10^6) are comparable to those of conventional poly-Si devices. The retention characteristics of PGM and ERS states was investigated and reasonable until 2000 seconds. A full-swing CMOS

inverter implemented by using two identical reconfigurable devices has been successfully demonstrated. In addition, Device physics behind the reconfigurability was characterized. The relationship between bottom gate biases and the resistance of the channel and Schottky junction was investigated by DC *I-V*, temperature dependency of I_D, and low frequency noise measurement. The aluminum source/drain (S/D) layer forms Schottky junction with poly-Si body being electrically doped with *n*- or *p*-type, and the current mechanism is dominated by Schottky reverse junction tunneling. Based on the analysis of the fabricated devices, optimization of fabrication process was performed. Therefore, stable bottom gate structure with enhanced uniformity and flatness was achieved. Improved on-current characteristics and enhanced PGM/ERS performance have been demonstrated by the optimized device. The gate controllability was also enhanced in the double gate operation with SS of ~90 mV/dec, and I_{on}/I_{off} increased to more than 10^7 in the optimized device. With complete device isolation by process optimization, a full-swing CMOS inverter and NAND/NOR logic gates implemented by using four identical reconfigurable devices have been

successfully demonstrated. The effect of S/D metal and electrical oxide thickness (EOT) of the gate stack on the device characteristics were investigated by both experiments and simulations.

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초 록

본 논문에서는 비 휘발성 메모리 (NVM) 기능을 갖는 프로그램 가능한 하부 전극 어레이 (Bottom gate array) 로 구성된 새로운 폴리 실리콘 재구성 가능 소자를 최초로 고안하고 제작 및 분석하였다. 제안된 소자는 소자의 크기, 신뢰성, 균일성 및 재현성 측면에서 매우 효율적이다. 하부 전극 어레이에 직접 바이어스를 인가하거나, 또는 하부 전극의 프로그램/이레이즈 상태를 변화 시킴으로써, 제안된 재구성가능 소자는 *n*-/*p*-MOSFET, *n*-*p*/*p*-*n* 다이오드 중 하나의 형태로 동작할 수 있다. 또한, 소자의 MOSFET 동작에서, 문턱 전압 (V_{th})과 접합 저항 (R_C)은 하부 전극에 의해 독립적으로 제어 가능하며 이는 제안된 재구성 가능 소자의 고유한 장점이다. 제작된 소자는 *n*-/*p*-MOSFET 동작에서 기존의 폴리 실리콘 채널 기반 소자들과 유사한 약 120mV/dec 의 역치하 기울기 (subthreshold swing, SS) 및 10^6 이상의 on/off 전류 비 특성을 갖는다. 두 개의 동일한 재구성 가능 소자를 이용하여 제작된 풀 스윙 CMOS 인버터 로직 게이트의 동작도 성공적으로 구현되었다. 제작된 소자의 DC *I*-*V* 특성, 드레인 전류의 온도 의존성 및 저주파 잡음 특성 측정을 통하여, 하부 전극 전압과

채널 저항 및 쇼트키 접합 저항의 관계를 연구하였다. 이를 통하여 알루미늄 소스/드레인은 n 혹은 p 형으로 전기적으로 도핑된 폴리 실리콘 채널과 쇼트키 접합을 형성하게 되고, 소자의 전류는 쇼트키 역방향 접합 터널링에 의하여 결정됨을 확인하였다.

제작된 소자에 대한 분석을 바탕으로 소자의 제작 공정 최적화를 진행하였으며, 제작 공정 최적화를 통하여 개선된 균일성과 평탄도를 갖는 안정된 하부 전극 구조를 구현하였고 이를 통해 개선된 프로그램/이레이즈 성능과 온 커런트의 증가를 확인하였다. 최적화된 소자의 역치하 기울기는 이중 게이트 동작에서 약 90 mV/dec 로 게이트 제어력이 향상되었고, on/off 전류비는 10^7 이상으로 증가하였다. 공정 최적화를 통해 각각의 소자를 완전히 격리 시킴으로써, 네 개의 동일한 재구성 가능 소자를 이용하여 제작된 NAND/NOR 로직 게이트의 동작 또한 성공적으로 구현하였다. 또한, 실험과 시뮬레이션을 통하여 소스/드레인 메탈의 종류와 게이트 스택의 전기적 두께가 소자의 특성에 미치는 영향에 대해서도 분석 하였다.

주요어 : 재구성 가능 소자, 하부 전극 어레이, 비 휘발성 메모리 기능, 문턱 전압, 변형 가능 소자, 프로그램/이레이즈

학 번 : 2012-30208