Ph.D. DISSERTATION

A STUDY ON HIGHLY-EFFICIENT LINEAR TRANSMITTER USING PULSED DYNAMIC LOAD MODULATION (PDLM) TECHNIQUE

펄스에 의한 동적 부하 변조 기술을 이용한
고효율 선형 송신기에 관한 연구

BY

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Abstract

STRONG push for longer battery life time and growing thermal concerns for the modern 3G/4G mobile terminals lead to an ever-growing need for higher efficiencies from the handset power amplifiers (PAs). Furthermore, as the modulation signal bandwidth is increased and more complex modulation schemes are introduced for higher data rate, the peak-to-average power ratio (PAPR) of signals increases and the PA requires more power back-off to meet the stringent linearity requirement. Therefore, the PA design has to address the challenging task of enhancing the efficiencies in the back-off power levels.

In this dissertation, dynamic load modulation (DLM) technique is investigated to boost the efficiency of a PA in the back-off output power level. This technique increases the efficiency by adjusting the PA load impedance according to the magnitude of the envelope signal. It can be categorized into two types, continuous and discrete types. Continuous-type DLM PA changes load impedance continuously by changing the capacitance of varactors used in the load matching circuit. Although the continuous modulation of the load impedance may result in significant efficiency enhancement, difficulties on integration of varactors and complexities on linearization of the PA make it difficult to be applied to the handset PA applications. Discrete-type DLM PA switches the load impedance from one value to another using RF switches. This type has the advantage in the aspect of ease of integration and simplicity in linearization compared to the continuous-type DLM PA, which make it more suited to the handset PA applications. However, the overall efficiency enhancement is quite limited since the PA does not always operate under the optimal load conditions.

To overcome the limitation of the existing DLM techniques, a new method of DLM, called pulsed dynamic load modulation (PDLM), is proposed to operate the

PA near the optimum impedance across a continuous back-off power range while still benefiting from the advantages offered by the discrete-type DLM PA. PDLM PA combines the concept of Class-S PA with 1-bit discrete load switching. Analytical calculation using simplified equivalent model is well matched with simulation results. To prove the proposed concept, it is implemented by designing and fabricating a prototype PDLM PA at 837 MHz using a 0.32-μm silicon-on-insulator (SOI) CMOS process. The experimental results show the overall PAE improvement for high-PAPR signals such as LTE signals.

Several issues caused by the PDLM technique are also discussed such as imperfect pulse tone termination effect and output noise spectrum due to pulse tones. Improving methods are proposed through the further analysis and evaluation.

The proposed PA is compared to the envelope tracking (ET) PA which is commonly used to boost efficiency at the back-off output power. Since the proposed concept is realized with low-power control circuits unlike envelope tracking, which requires high-power circuits such as dc-dc converters and linear amplifiers, the PDLM PA concept of this work can provide a potential solution for high-efficiency PAs for the future mobile terminals using wideband modulation signals.

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Chapter 1

Introduction

Demand for low power consuming mobile components is growing exponentially. In case of power amplifier, one of the most power consuming components in handset, efficiency is especially emphasized. As the amount of data communication is explosively expanded in modern communication environment, signal bandwidth of a modulation scheme is broadened and peak to average power ratio (PAPR) becomes higher to increase the data bit rate [1]. This means that the power amplifier should operate in a more backoff-ed power region where efficiency is low in order to meet the stringent linearity requirement. Thus, numerous types of efficiency enhancement techniques have been investigated to increase the efficiency at the backoff-ed output power region.

Recently, envelope tracking (ET) technique is heavily investigated due to its high efficiency across a wide output power range [2-6]. However, few factors such as its inevitable complex structure, necessity of time delay alignment between RF path and supply modulator path in the baseband processor [7], switching noise of the modulator [4], [8], and the modulator efficiency degradation as a modulation

signal bandwidth increases obstruct ET PA to be applied in the commercial handset.
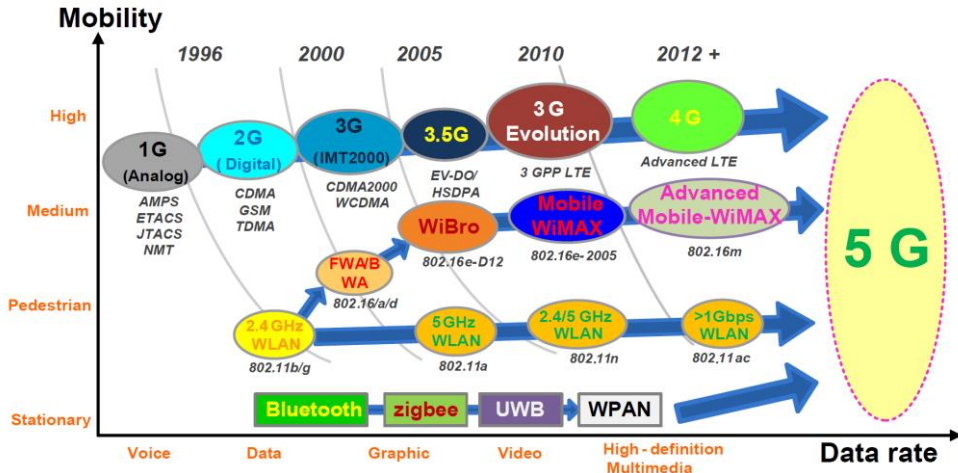
Figure 1.1 Evolution of the mobile technology
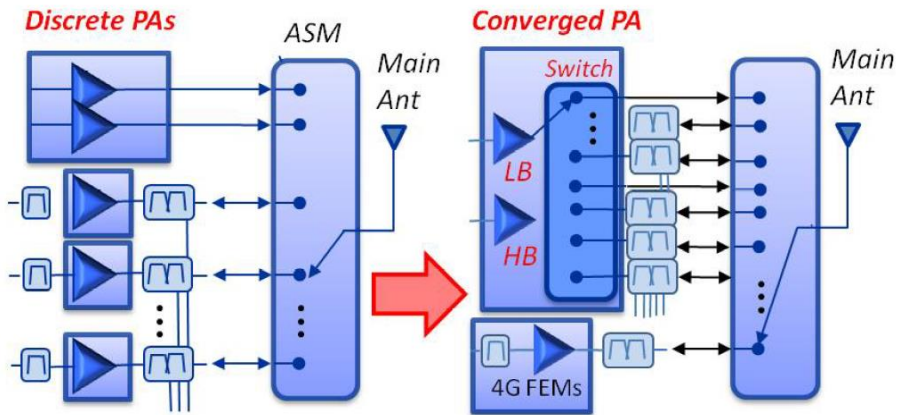
Figure 1.2 Transceiver architecture

A dynamic load modulation technique is another way for boosting efficiency [9-14]. Since the limitation of the supply modulator efficiency does not exist, it can achieve high efficiency regardless of a modulation signal bandwidth. In previous works, a varactor is prevalently used as a load modulation device to achieve high efficiency across wide output power range, but this method generates continuous gain and phase distortions. Hence, it requires assistance of complex linearization schemes, such as digital predistortion (DPD) technique, for linear amplification

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[10], [14]. As a result, the varactor-based DLM PA is not suitable to be applied to portable devices.
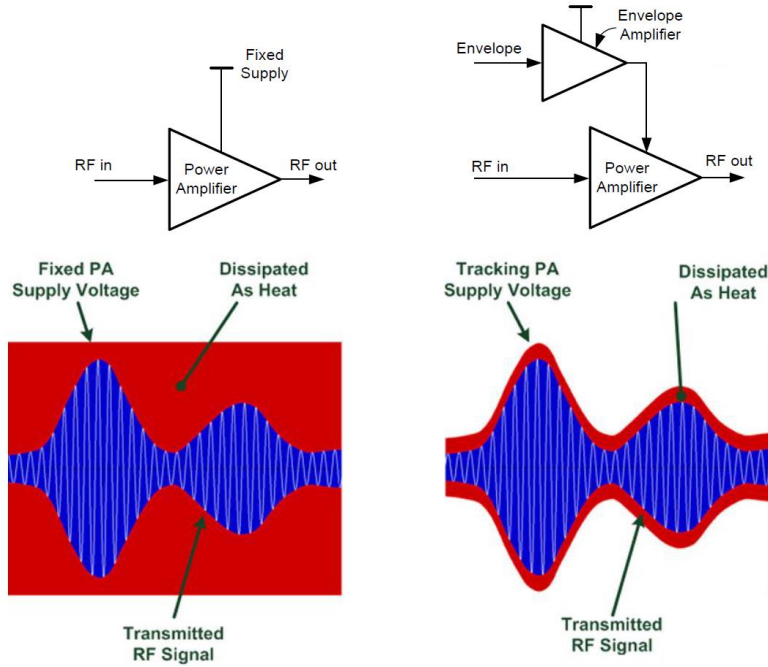
$$\eta_{Overall} = \eta_{Envelope\_Amp} . \eta_{RF\_PA}$$

Figure 1.3 Concept of the envelope tracking PA

Discrete-type DLM PA switches the load impedance from one value to another using an RF switch. The RF switch with low loss and high breakdown voltage can be integrated into the PA IC using high electron mobility transistor (HEMT) or silicon-on-insulator (SOI) CMOS process. Moreover, the linearity issues raised by the continuous-type DLM PA can be mitigated or avoided since the gain and phase distortion occurs only at the switching point. By compensating for the gain and phase discontinuity at this switching power level, the linearity can be preserved regardless of the load variations at the antenna. The discrete-type DLM PA is thus more suited to the handset PA applications. However, the overall efficiency

enhancement is quite limited since the PA does not always operate under the optimal load conditions. Further efficiency improvement is possible by using multi-bit load impedance switching [15-17], which again comes at the cost of the linearity and system complexity due to the increased number of gain and phase discontinuity points to compensate for.

In this dissertation, a new method of DLM, called pulsed dynamic load modulation (PDLM), is proposed to operate the PA near the optimum impedance across a continuous back-off power range while still benefiting from the advantages offered by the discrete-type DLM PA. PDLM PA combines the concept of Class-S PA with 1-bit discrete load switching. The proposed concept is verified by designing and fabricating a prototype PDLM PA at 837 MHz using SOI CMOS process. The fabricated PDLM PA shows the overall system efficiency enhancement comparable to the widely used envelope tracking PA.

In Chapter 2, the operation principle of the DLM PA is explained. A DLM PA using HBT PA with integrated HBT switch is demonstrated as an implementation example.

In Chapter 3, newly proposed PDLM PA concept is explained together with an analytical analysis using a simplified model. The overall PA structure and the detailed circuit block designs are elaborated together with the simulation results. The experimental results from RF SOI CMOS PA are compared with the simulation. Also the effect of non-ideal termination conditions on the PA efficiency and linearity is discussed.

In Chapter 4, some important factors are discussed for the PDLM PA to be applied to transceiver systems. First, effect on efficiency in case of wideband operation is simulated and compared with ET PA. Also, random PWM and sigma-delta modulation technique are discussed to reduce output noise spectral power

generated during PDLM operation.

Finally, Chapter 5 concludes this study.

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Chapter 2

Dynamic Load Modulation Technique

2.1   Introduction

Dynamic load modulation (DLM) technique is a method to boost the efficiency of a PA in the back-off output power levels. This technique increases the efficiency by adjusting the PA load impedance according to the magnitude of the envelope signal [1]-[6]. Fig 2.1 shows a conceptual block diagram of DLM PA. By modulating load impedance using tunable matching circuit, PAE improvement can be achieved at the back-off output power region as shown in Fig. 2.1(b).

It can be categorized into two types, continuous and discrete types. Advantages and issues of each type are investigated in Section 2.2 and 2.3. An actual implementation of discrete-type DLM PA is demonstrated for portable transmitter application in Section 2.4. Lastly, limitation of the conventional DLM PA is discussed in Section 2.5.
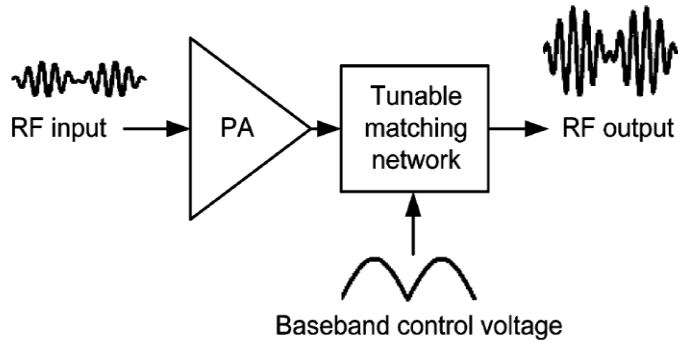
(a)
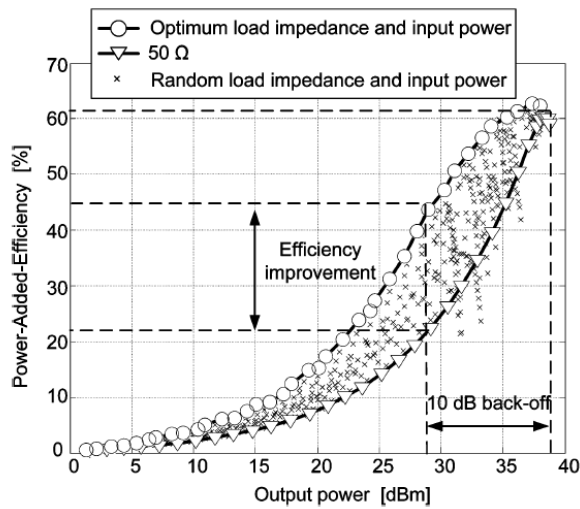
(b)

Figure 2.1 (a) Conceptual block diagram of dynamic load modulation technique.
(b) Loadpull measurements of a 1-GHz LDMOS PA

2.2   Continuous-type dynamic load modulation PA

Continuous-type DLM PA changes load impedance continuously by changing the capacitance of a varactor used in the load matching circuit. In case of modulation signal is applied to the PA, varactor control signal is also modulated according to the magnitude of the signal to modulate load impedance for best efficiency. Thus, the continuous modulation of the load impedance results in the significant efficiency enhancement. However, this method generates several

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problems for the handset PA applications. First, it is not easy to integrate a varactor with low loss and high breakdown voltage on a PA IC [7]. Second, the continuous load variation generates the distortion in the gain and phase of the PA, which degrades the overall system linearity. Moreover, in the practical handset PA application, the impedance presented to the antenna varies considerably according to the phone usage patterns, which changes the voltage swing across the varactor and thus its capacitance value [7]. To achieve the required system linearity, complicated circuit techniques such as the complex load matching structure with multiple varactors [8] and memory digital predistortion (DPD) technique [9] should be employed.

Fig. 2.2 shows an implementation example of the continuous-type DLM PA [3, 9]. Large varactors are applied at the output of the module as a tunable matching circuit. DSP is applied at the input of the PA to linearize PA using static and memory DPD. As shown at Fig. 2.3, static DPD cannot fully compensate the distortion of the DLM PA. Although the memory DPD provides full linearization, portable devices cannot afford to accommodate high-priced DSP processor consuming such a large power.

Fig. 2.4 is another example of the continuous-type DLM PA. 3 varactors are used to compensate the phase distortion generated during load impedance modulation [8]. This work provides good ACLR performance without using DPD linearization. However, efficiency improvement is greatly compromised due to the use of multiple varactors. Also, it prevents compact implementation of the DLM PA.

(a)

7 W, 1 GHz class-E PA [8]   Varactor-based tunable matching network
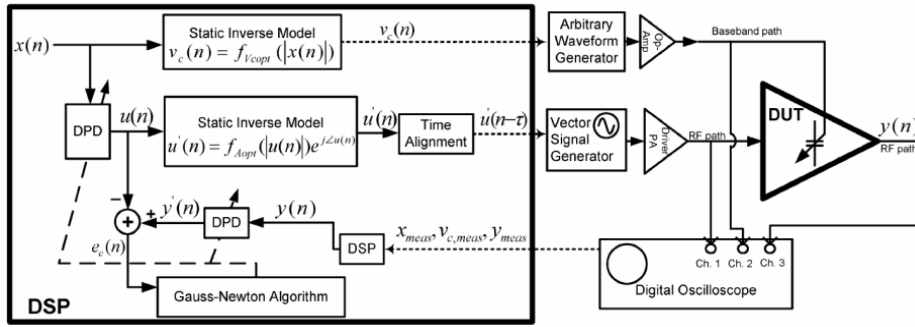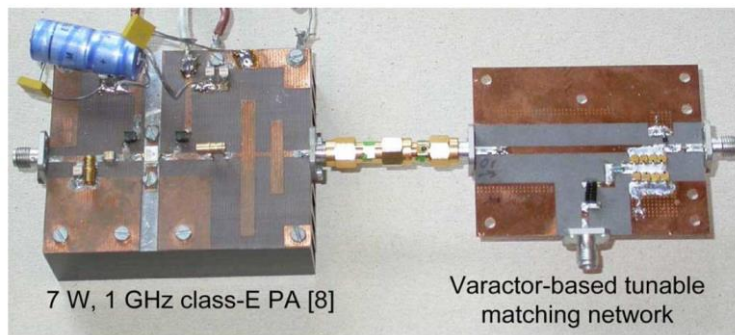
(b)

Figure 2.2 (a) Block diagram of digital predistorter and measurement setup for dynamic modulation PA. (b) Module picture of the varactor-based dynamic load modulation PA.
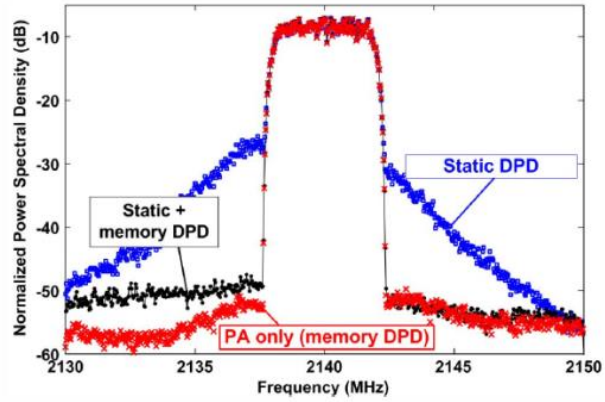
(a)
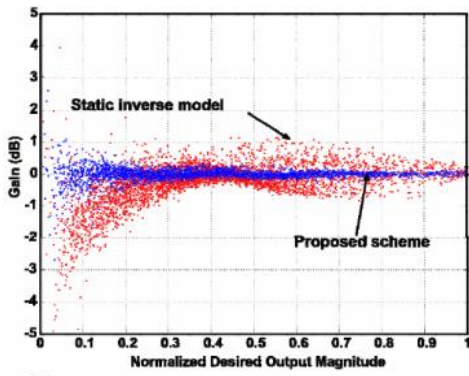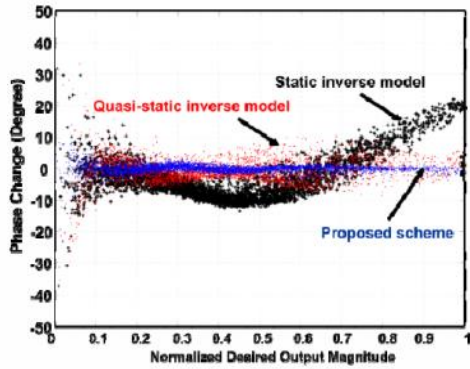
(b)   (c)

Figure 2.3 Measured (a) power spectral density and (b) dynamic AM-to-AM and
(c) AM-to-PM of the varactor-based dynamic load modulation PA.

(a)

(b)

(c)
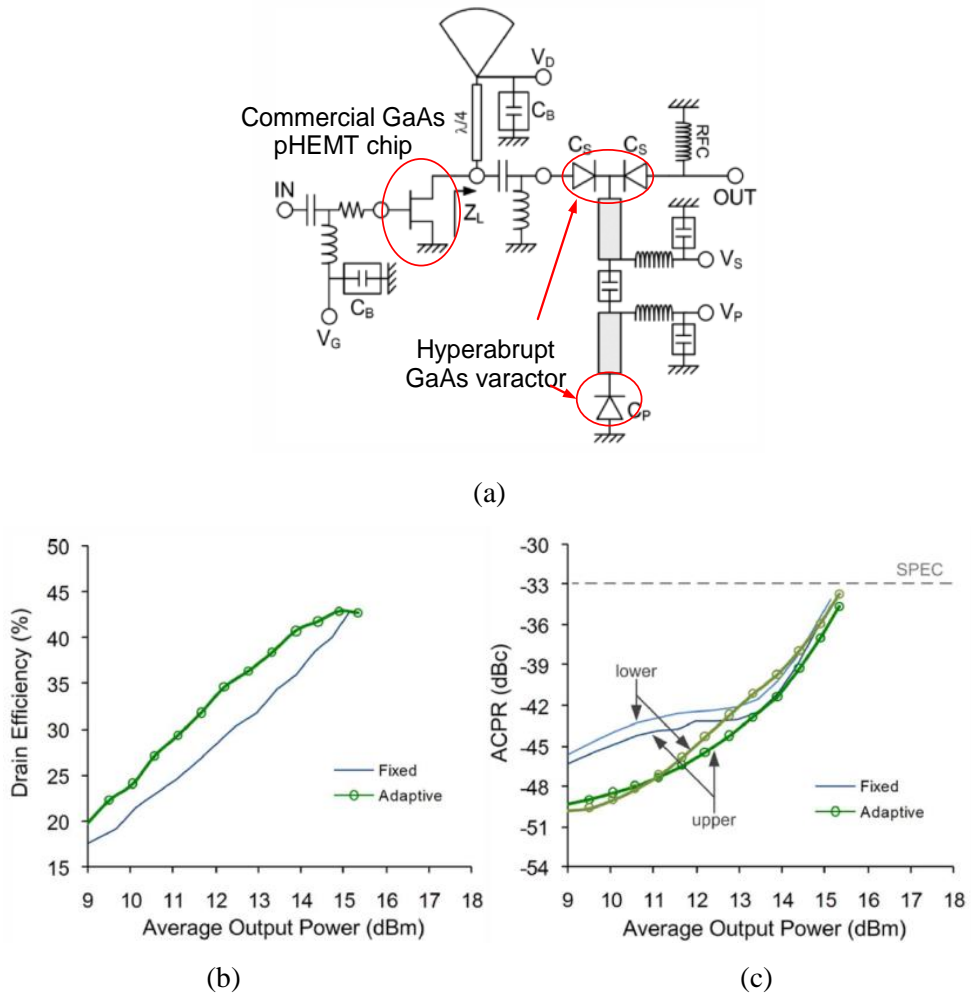
Figure 2.4 (a) Schematic of a varactor-based dynamic load modulation PA. Measured (b) drain efficiency and (c) ACPR of the dynamic load modulation PA under the excitation of the WCDMA signal.

2.3 Discrete-type dynamic load modulation PA

(a)

(b)

(c)
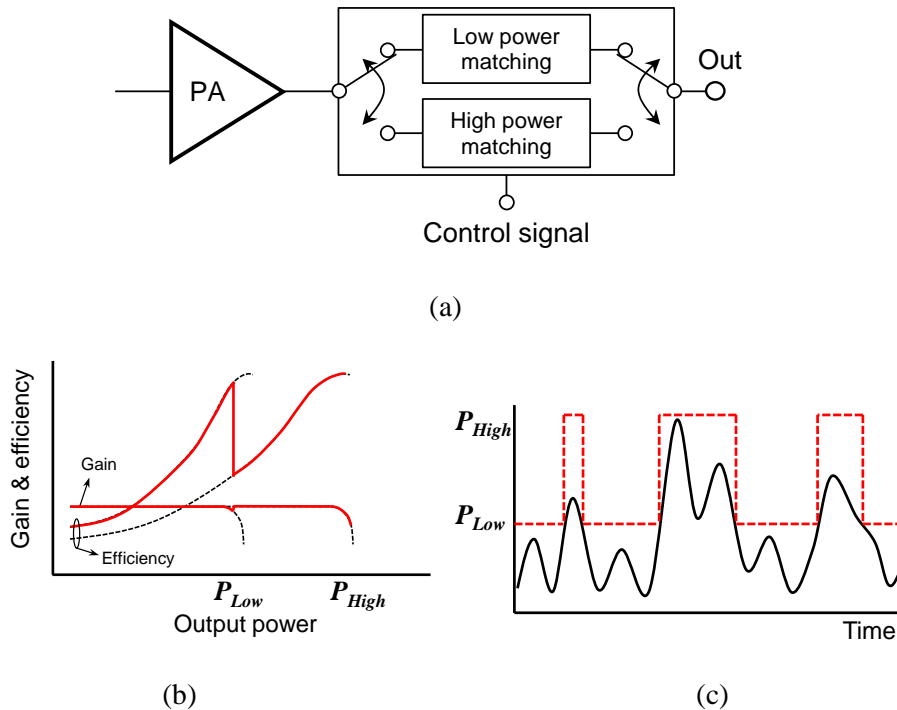
Figure 2.5 (a) Block diagram of the discrete-type dynamic load modulation PA. Conceptual (b) gain and PAE curve and (c) load impedance states according to envelope waveform.

Discrete-type DLM PA switches the load impedance from one value to another using an RF switch as shown in Fig. 2.5(a). The RF switch with low loss and high breakdown voltage can be integrated into the PA IC using high electron mobility transistor (HEMT) or silicon-on-insulator (SOI) CMOS process. Moreover, the linearity issues raised by the continuous-type DLM PA can be mitigated or avoided since the gain and phase distortion occurs only at the switching point. By compensating for the gain and phase discontinuity at this switching power level, the linearity can be preserved regardless of the load variations at the antenna. The discrete-type DLM PA is thus more suited to the handset PA applications. However, the overall efficiency enhancement is quite limited since the PA does not

always operate under the optimal load conditions. As shown in Fig. 2.5(b) and (c), efficiency at between P_{Low} and P_{High} is low since the PA is operated in back-off power condition.

Further efficiency improvement is possible by using multi-bit load impedance switching [10-12], which again comes at the cost of the linearity and system complexity due to the increased number of gain and phase discontinuity points to compensate for.

2.4   Implementation example

In order to accommodate the required linearity specification without using DPD technique, this example adopts a switched-capacitor-type variable load matching circuit. To implement the DLM PA on a single chip, a HBT switch is newly proposed. By integrating HBT switches on a PA die, a small module design is possible. To compensate the gain and phase distortion, an input linearizer is also integrated on the PA die. The demonstrated PA offers competitive or slightly better power added efficiency (PAE) than ever reported PAs [13-15]. This PA is an alternative approach to mobile handset in terms of small and simple structure, no DPD required, no bandwidth limitation and no noise generation. In Section 2.4.1, each components of the proposed DLM PA are explained in detail including the operation of the newly proposed HBT switch. In Section 2.4.2, the effects of the linearizer are compared. Experimental results are presented in Section 2.4.3.
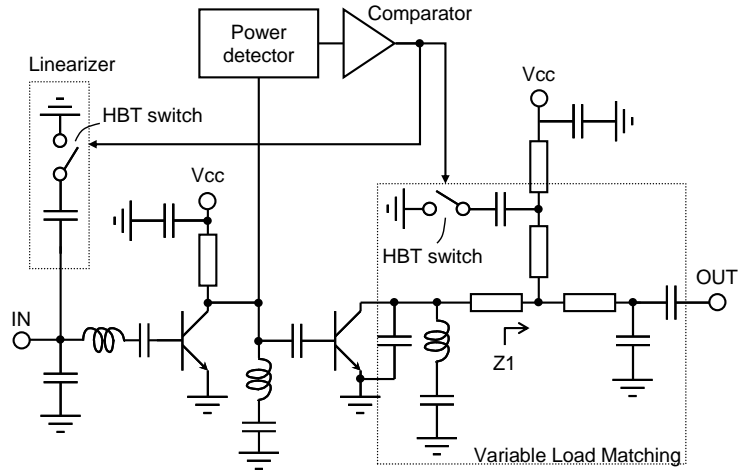
Fig. 2.6.   Schematic of the proposed DLM PA

2.4.1   DLM PA STRUCTURE

A DLM PA offers relatively simple structure. Fig. 2.6 is the schematic of the proposed PA. It comprises of a conventional 2stage PA with variable load matching circuit, a power detector, a comparator and a linearizer. The variable load matching circuit offers two different load impedance states depending on the detected signal level. The power detector filters out RF signal from modulated envelope signal. The comparator compares the detected envelope signal with reference voltage and outputs signals to control two switches, one at the variable load matching circuit and one at the linearizer. The linearizer plays a role of compensating the gain and phase distortion generated by variable load matching circuit. Some of the components will be explained further in the following subsection.
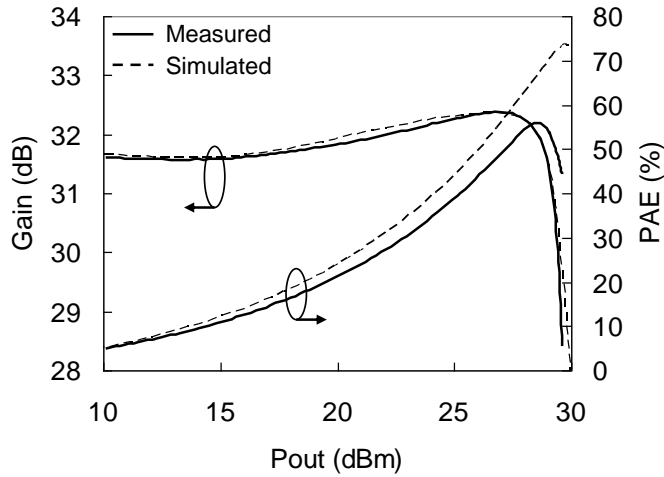
Fig. 2.7. Simulated and measured gain and PAE of conventional PA

A. RF PA Design

In order to realize DLM PA without using digital predistortion, class AB/F PA structure is adopted because of its high efficiency among linear PAs [16]. In Fig. 2.6, two shunt LC resonators are applied at the output and the input of the power stage to short 2nd harmonic term of the signal. Inductors, in the resonator, are implemented using short bonding wire while capacitors are placed outside the die to optimize its performance. The fundamental load impedance is set to 7.2+j0.2 Ω for a 1-dB compression power of 29dBm. The second and the third harmonic impedances are also selected as 0.3+j0.3 Ω and 9+j67 Ω, respectively, to enhance the efficiency according to [16]. During the measurement, the PA is tuned using both single tone signal and WCDMA modulated signal for better linearity although peak PAE has slightly lessen. In Fig. 2.7, gain and PAE of both simulated and measured 2stage PA are compared. Although measured PAE is quite lower than the simulated, peak PAE of 56% was achieved after optimization.

B. *Dynamic Load Modulation (DLM) Scheme*

As explained above, a switched-capacitor type load modulation scheme is adopted to meet the linearity specification without using digital predistortion. In this application, two load impedance states are selected for simplicity.
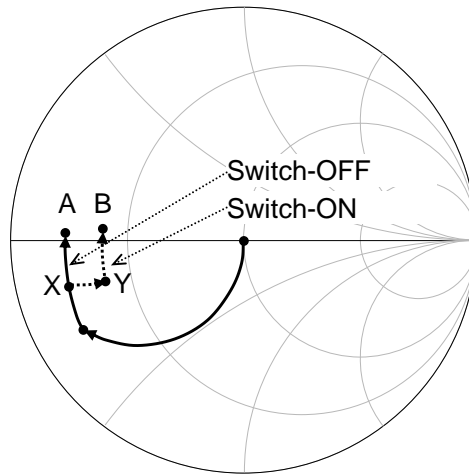
Fig. 2.8. Load impedance trajectory depending on switch status at the variable load matching circuit.

First, carrier frequency component is filtered out from envelope signal at the power detector connected to interstage matching of the PA. The detected envelope signal is then compared to reference voltage at the comparator. The resulted digital control signal is applied to HBT switches at the variable load matching and the linearizer. Fig. 2.8 shows simulated load impedance trajectory according to the switch status. If the envelope signal is larger than pre-defined level, the PA should have load impedance low enough in order to preserve required linearity. Thus, the HBT switch is turned off and the load impedance is set to A. However, if the envelope signal is smaller than the reference level, efficiency of the PA is decreased because the voltage swing does not reach its maximum rail-to-rail swing. In this case, by turning-on the HBT switch, impedance Z1 in Fig.2.6 changes from

X to Y in Fig. 2.8. The load impedance is now shifted from A to B and thus, the voltage swing is improved and better efficiency is resulted compared to before. In this paper, the load impedances in Fig. 2.8 are set to 7.2+j0.2 Ω and 10.9+j0.9 Ω for A and B and simulated 1dB compression output powers are 29dBm and 27dBm for A and B, respectively.

(a)

(b)

ic (A)

0.4

0

-0.4

time

ic_fwd (A)

0.4

0

time

ic_rev (A)

0

-0.4

time

ib_fwd (mA)

5

0

time

ib_rev (mA)

10

5

0

time

(c)

HBT switch

Ideal switch with on-resistance of 1.25 ohm

Vsw (V)

0.5

0

-0.5

time

(d)

20
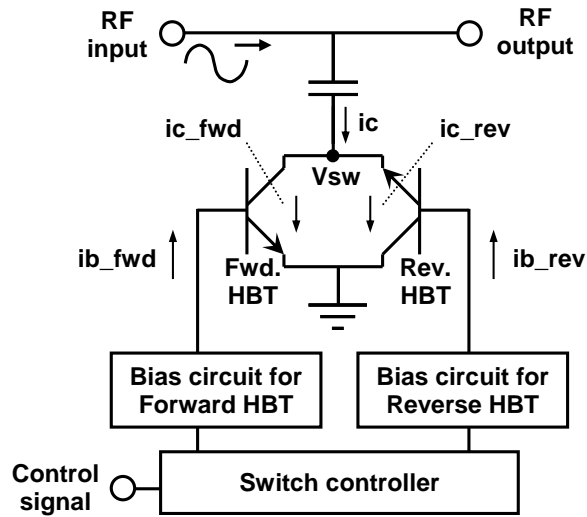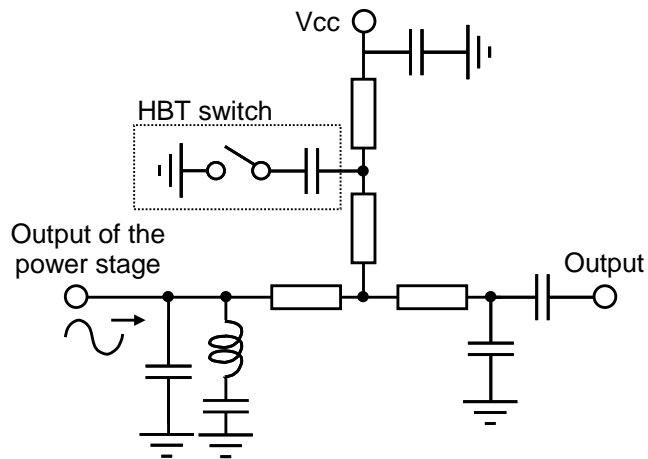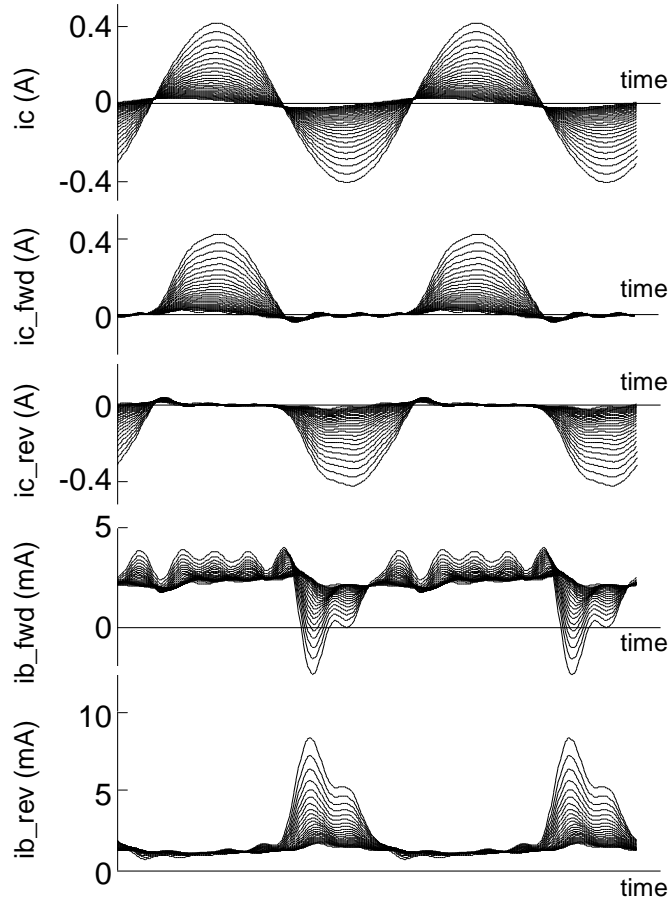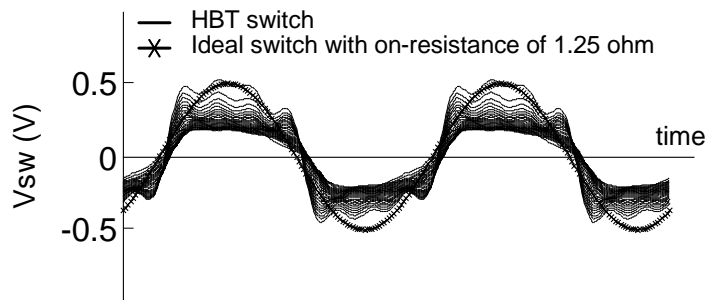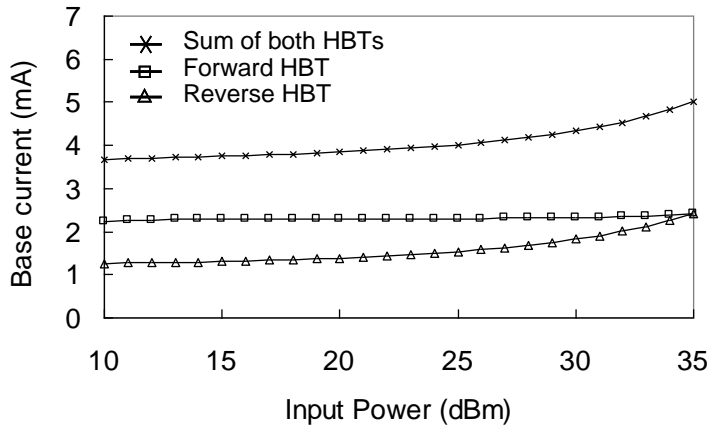
(e)

Fig. 2.9. (a) Schematic of the proposed anti-parallel type HBT switch. (b) Schematic of the variable load matching circuit including the proposed HBT switch. (c) current waveforms of each component shown in (a) as power is applied from 10dBm to 35dBm into the output of the power stage in (b). (d) voltage waveform of Vsw node compared to that of ideal switch with 1.25 ohm of on-resistance. (e) base current of the switch

C. HBT switch

Previous works for DLM PA [9]-[14] adopt varactor-based load modulation scheme. In other words, one or more varactors are used for load modulation and thus, implemented modules inevitably have bulky and costly structures which make the PA difficult to be applied to mobile applications. To overcome this problem, HBT switch is newly developed for integration with PA MMIC.

First, the reason why HBT process is hard to be used as a RF switch, needs to be clarified. Since HBT is not a bi-directional structure, it has relatively high current gain for forward direction while it has less or no current gain for reverse direction. Thus, if HBT is configured as a typical FET switch, the amount of base current for forward current swing becomes quite low and the switch has relatively low on-resistance. Conversely, in case of reverse current swing, base current is

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considerably increased and huge on-resistance is obtained. As a result, overall base current and on-resistance are not acceptable as a RF switch. To correct this problem, anti-parallel type HBT switch is devised as shown in Fig. 2.9(a). For the purpose of a switched capacitor in the variable load matching circuit, the devised HBT switch adopts shunt switch configuration.

In order to test the switch operation, current and voltage waveforms are simulated as applying input power from 10dBm to 35dBm to the variable load matching circuit shown in Fig. 2.9(b). The simulated result is shown in Fig. 2.9(c)-(e). For a positive current swing of capacitor current (ic), the forward HBT draws current swing (ic_fwd) with low base current swing (ib_fwd) and thus, with low on-resistance, while current drawing of the reverse HBT (ic_rev) is maintained almost zero. In case of reverse current swing of capacitor current (ic), the reverse HBT takes the role of current drawing with low base current, while the forward HBT dose not draw any current. Thus, low on-resistance is maintained for both positive and negative current swing and voltage ripple (Vsw) does not exceed 0.5V up to peak capacitor current swing of 400mA as shown in Fig. 2.9(d). Fig. 2.9(d) and 2.9(e) also show that designed HBT switch has around 1.25 ohm of on-resistance and consumes only 3.2 mA of quiescent current. And sum of the base currents is 5mA in case of 400mA of peak capacitor current swing (ic) at 35dBm of input power level. Although proposed HBT switch wastes finite amount of current, it can endure up to more than a watt of RF power level, at which small amount of current such as 5mA does not affect to the overall PA system efficiency. Thus, proposed HBT switch is suitable for integration of DLM PA in one MMIC with proper switching performance.

2.4.2 LINEARIZATION

As briefly introduced in above, the variable load matching structure inevitably brings gain and phase discontinuities. In this paper, a HBT switch is also used at the input of the PA as a linearizer to compensate the discontinuities.

Effects of AM-AM and AM-PM on 3rd order intermodulation (IM3) distortion and its asymmetry have been already investigated in [17]. In general, when 2-tone signal is excited into a PA, output voltage waveform with nonlinearity can be expressed as [18]

$$v_0(t) = \left[a_1 \cos(\Omega t + \Delta) + a_3 \cos 3(\Omega t + \Delta) \right] \cdot \left[\cos\{\omega t + \Phi \cos(2\Omega t)\} \right],$$

(1)

where Ω is the half of the carrier frequency separation, a_1 and a_3 are the power series amplitude distortion coefficients, Φ is the peak amplitude of the AM-to-PM distortion, and ω is the RF carrier frequency. Δ is the envelope time domain phase angle between the occurrence of AM-AM and AM-PM effects. By expanding the equation and simplifying it again with the assumption of Φ to be small enough, so that $\sin\Phi=\Phi$, arranged magnitudes of 3rd order intermodulation terms for upper and lower sideband becomes

$$IM3_{USB} = \left\{ \frac{a_3}{2} \cos 3\Delta + \frac{a_1\Phi}{4} \sin \Delta \right\} \cos \omega_{3U} + \left\{ \frac{a_1\Phi}{4} \cos \Delta - \frac{a_3}{2} \sin 3\Delta \right\} \sin \omega_{3U}$$

(2)

$$IM3_{LSB} = \left\{ \frac{a_3}{2} \cos 3\Delta - \frac{a_1\Phi}{4} \sin \Delta \right\} \cos \omega_{3L} + \left\{ \frac{a_1\Phi}{4} \cos \Delta + \frac{a_3}{2} \sin 3\Delta \right\} \sin \omega_{3L},$$

(3)

where ω_{3U} and ω_{3L} are $\omega+3\Omega$ and $\omega-3\Omega$, respectively. That is, when there is no AM-PM distortion, symmetric IM3 is achievable. However, in general case, which

has AM-PM distortion and some amount of time delay between amplitude and phase distortion exists, IM3 asymmetry can be observed as expressed in (2) and (3). For the DLM PA presented here, phase shift is occurred when the load impedance is changed from one state to the other. Fig. 2.10 shows the measured gain and phase using a vector network analyzer. When the HBT switch for variable load matching is changed from ON-state to OFF-state as output power is increased, 3° of phase is reduced abruptly. The linearizer composed of a capacitor and a HBT switch generates the same amount of phase shift with opposite direction by turning the switch OFF from ON-state as the output power is increased. In this case, a 0.5 pF of capacitor successfully compensates the phase shift as shown in Fig. 2.10. In case of gain discontinuity, no compensation is done due to its small magnitude less than 0.3dB. When the gain discontinuity is not negligible, it can still be compensated by adding a resistor in parallel with the capacitor.
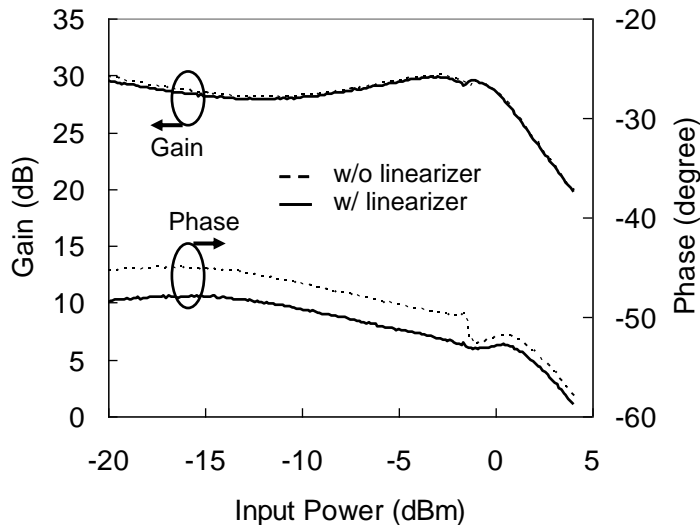
Fig. 2.10. Measured gain and phase with/without linearizer at the input side of the DLM PA

To check the IM3 asymmetry due to the phase discontinuity, WCDMA

modulated signal is applied to the DLM PA before and after compensating the phase shift. Fig. 2.11 shows the output power spectrum at 27.5 dBm for DLM PA and 27dBm for conventional PA. As expected, ACLR asymmetry is observed, which is completely eliminated by using the linearizer at the input of the PA.
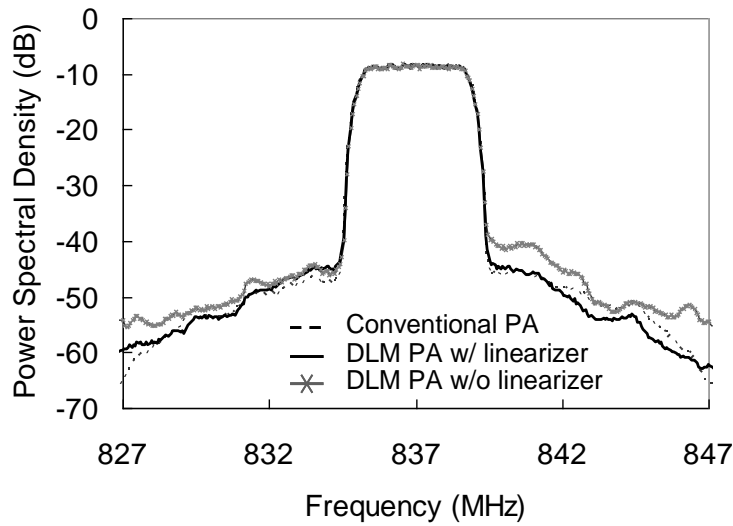
Fig. 2.11. Measured power spectrum at the output power level of 27.5dBm for DLM PA and 27dBm for conventional PA excited with WCDMA modulated signal

2.4.3 EXPERIMENTAL RESULTS

The proposed DLM PA with integrated HBT switch is fabricated with a 2-um InGaP/GaAs HBT process to be operated at 837MHz for handset application. Fig. 2.12 shows the picture of the fabricated MMIC. Overall die size including sawing street is 1.1x1.08 mm^2. For HBT switch in variable load matching circuit, forward and reverse HBT occupy in 0.18x0.17 mm^2 together while each has emitter area of 2000um^2. HBTs with 200um^2 of emitter area are used for the input linearizer. Capacitors for the variable load matching and the linearizer are placed outside the

die for optimization. LC resonators for 2nd harmonic short are implemented with bonding wires and chip capacitors. In case of the PA, 200um2 and 3200um2 of emitter area are selected for driver and power stage, respectively. After evaluation, 52 mA of quiescent current is selected for best efficiency with moderate linearity.
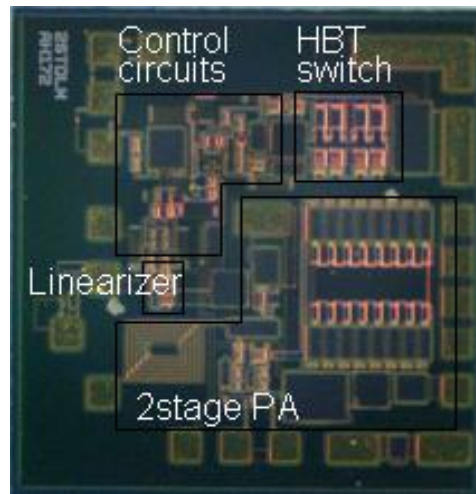
Fig. 2.12. Picture of the fabricated MMIC for DLM PA with integrated HBT switch
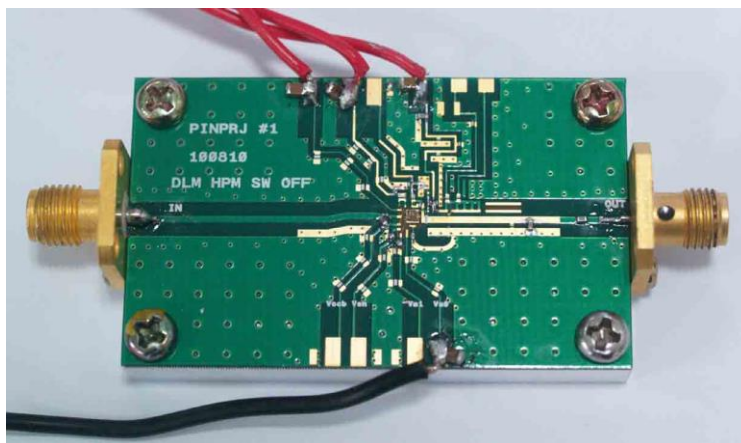
Fig. 2.13. Picture of the implemented DLM PA module

A PA chip is mounted on FR4 printed circuit board as shown in Fig. 2.13. Because most of the functions are integrated on the IC and no digital predistortion

for linearization is required, the module is successfully implemented in a compact size.

For the demonstration of the DLM PA operation, the module is tested with single-tone signal, 3.84MHz-BW, 3.5dB-PAPR WCDMA signal and 10MHz-BW, 50 resource-block, 7.5dB-PAPR, 16 quadrature amplitude modulation (16-QAM) LTE signal. Fig. 2.14 shows the differences in gain and PAE between the DLM PA and conventional PA when using single-tone signal. Peak PAEs are 57% and 56% for DLM PA and conventional PA, respectively. Slight difference comes from the optimization process of compromising PAE and linearity. As output power level is decreased, PAE of the conventional PA is gradually decreased while PAE of the DLM PA jumps up once at 27.7dBm when the load impedance is shifted for high PAE.
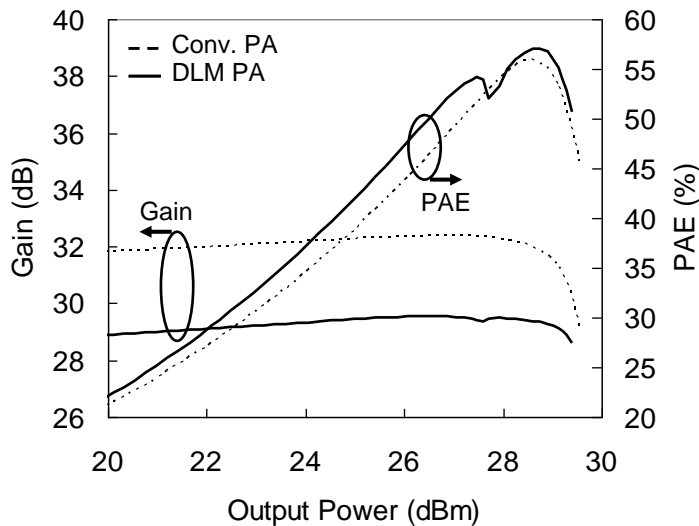
Fig. 2.14. Measured gain and PAE for DLM PA and conventional PA with single-tone signal
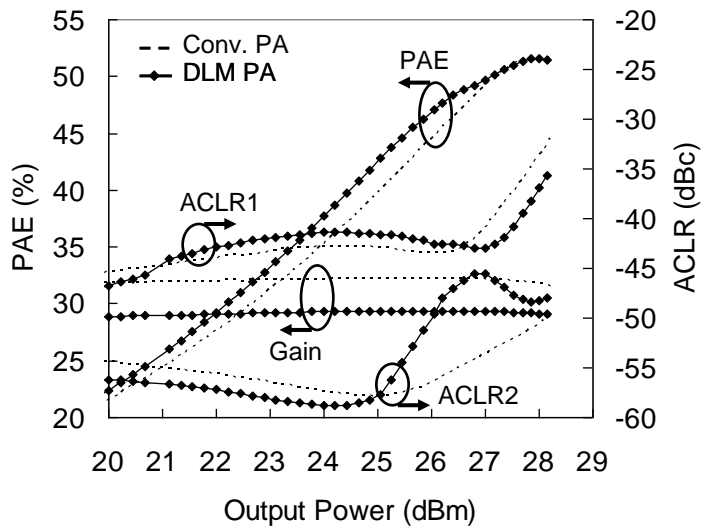
(a)
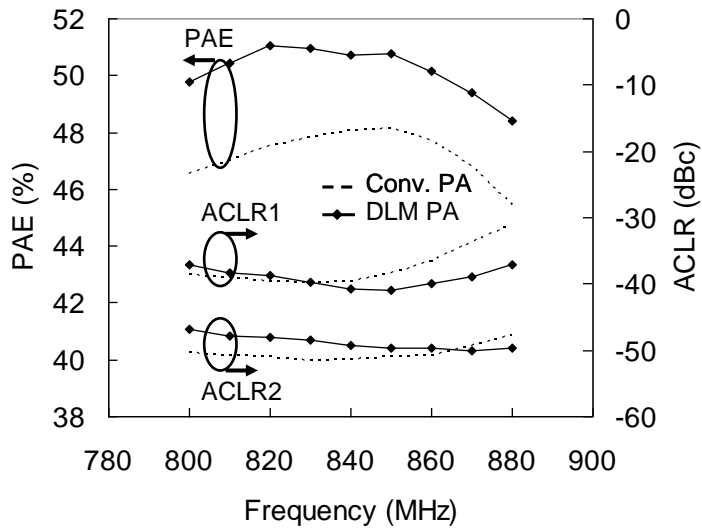
(b)

Fig. 2.15. Measured performance for DLM PA and conventional PA with WCDMA signal: (a) power sweep, (b) frequency sweep at 27.5dBm and 27dBm output power level for DLM PA and conventional PA, respectively
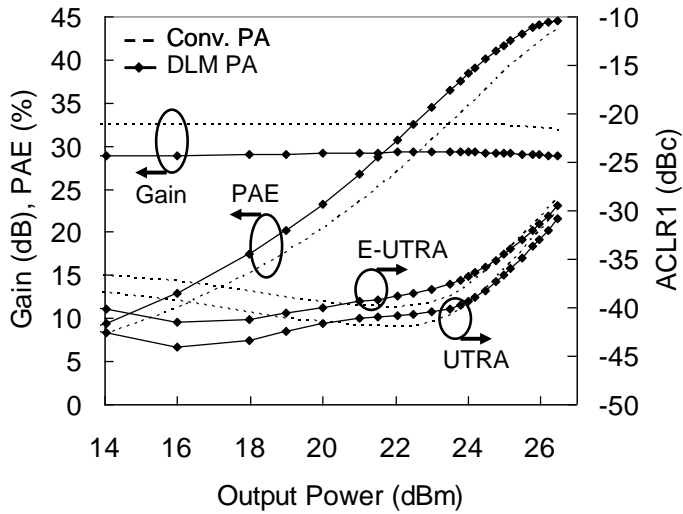
(a)
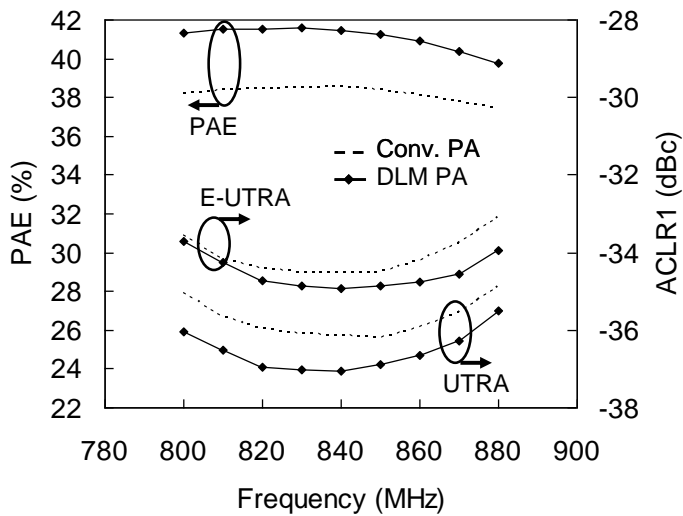
(b)

Fig. 2.16. Measured performance for DLM PA and conventional PA with 10MHz BW 16-QAM LTE signal: (a) power sweep, (b) frequency sweep at 25dBm output power level for DLM PA and conventional PA, respectively

Fig. 2.15 is the measured RF performance according to output power level and frequency when WCDMA signal is excited to both PAs. As the output power level for 0.5dB gain compression is extended from 28.7dBm of the conventional PA to

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29.2dBm of the DLM PA, output power level that intersects -40dBc of ACLR1 is also extended from 27dBm to 27.5dBm, respectively. In addition, PAE is improved from 48% to 51% while obtaining the required linearity with margin. As shown in Fig. 2.15(b), across the wide frequency range, PAE is improved about 2~3% and bandwidth of linearity is rather wider than conventional PA.

TABLE 2.1

Signal	Parameter	DLM PA	Conventional PA
WCDMA	Pout (dBm)	27.5	27
	Gain (dB)	29.3	32.1
	PAE (%)	51	48
	ACLR (dBc)	−40.7	−40.6
10MHz BW 16QAM LTE	Pout (dBm)	25	25
	Gain (dB)	29.2	32.3
	PAE	41.7	38.5
	E-UTRA$_{ACLR1}$ (dBc)	−34.4	−34.6
	UTRA$_{ACLR1}$ (dBc)	−36.8	−36.2

To show that the efficiency of DLM PA is not degrading as modulation signal bandwidth is increased, the PAs are also evaluated using 10MHz BW 16-QAM LTE modulated signal, as shown in Fig. 2.16. For the specification on linearity in LTE modulation, E-UTRA$_{ACLR1}$ and UTRA$_{ACLR1}$ are tested. E-UTRA$_{ACLR1}$ stands for power ratio of assigned LTE signal to adjacent LTE signal and UTRA$_{ACLR1}$ means power ratio of assigned LTE signal to adjacent WCDMA signal [19], [20]. -33dBc and -36dBc are often used as a linearity limitation for E-UTRA$_{ACLR1}$ and UTRA$_{ACLR1}$, respectively, as a 3dB of linearity margin from 3GPP specification. Fig. 2.16(a) shows that 41.7% of PAE with -34.4dBc and -36.6dBc of E-UTRA$_{ACLR1}$ and UTRA$_{ACLR1}$, respectively, is achieved at the output power level of 25dBm. In this case, linear output power level of DLM PA is

TABLE 2.2

PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RESULTS

Reference	Freq. (GHz)	Pout (dBm)	PAE	ACLR1	BW (MHz)	Modulation	DPD	Technology
[14]	1.95	26.3	50.5%	−35dBc	3.84	WCDMA	No	InGaP/GaAs HBT
[15]	1.95	29.3	50.4%	−40dBc	3.84	WCDMA	Yes	GaAs HBT
[13]	1.85	30.1	46%	−40dBc	3.84	WCDMA	No	ET PA : 65nm CMOS for modulator, InGaP/GaAs HBT for PA
	1.85	27.8	39%	−34dBc for E-UTRA	10	16-QAM LTE	No	
This work	0.837	27.5	51%	−40dBc	3.84	WCDMA	No	DLM PA with InGaP/GaAs HBT
	0.837	25	41.7%	−34.4dBc for E-UTRA	10	16-QAM LTE	No	

similar to that of conventional PA. This is because saturation output power dominates overall linearity in LTE modulated signal with high PAPR. Fig. 2.16(b) shows that approximately 3% of PAE is improved across the wide frequency range while meeting the required linearity specification. RF performance of the DLM PA compared to the conventional PA is summarized in Table 2.1.

Based on the similar linearity, the DLM PA offers about 3% of PAE improvement compared to the conventional PA. Performance comparison of the proposed DLM PA with other state-of-art results is summarized in Table 2.2. This data demonstrates that this work is among the highest PAEs for both WCDMA and LTE modulated signal without using DPD or ET technology.

2.4.4   CONCLUSION

By integrating newly proposed HBT switch in a PA MMIC, 1 chip solution for dynamic load modulation PA is successfully implemented with high efficiency and linearity. Without the assistance of digital predistortion, the proposed PA meets the

linearity requirements for WCDMA and 10MHz BW 16-QAM LTE modulation signal. It achieves 51% of PAE at 27.5dBm with -40dBc of ACLR1 for WCDMA modulation signal. And it also shows 41.7% of PAE at 25dBm with -34.4dBc of E-UTRA_ACLR1 for 16-QAM LTE modulation signal. These results show competitive or slightly better performance than other state-of-the-art results such as envelope tracking PA or PA with digital predistortion. By integrating switching components in a single die, the proposed DLM PA will be a good candidate for handset applications which requires highly efficient PA module with small form-factor.

2.5   Limitations

As explained in previous sections, both continuous-type and discrete-type DLM PA have limitations for portable transmitter applications. Discrete-type DLM PA is more advantageous on the aspect of simple and compact implementation and linear operation. As shown in Fig. 2.17, efficiency degradation weakens usefulness of the concept.

To overcome the limitations, a new method of DLM, called pulsed dynamic load modulation (PDLM), is proposed to operate the PA near the optimum impedance across a continuous back-off power range while still benefiting from the advantages offered by the discrete-type DLM PA. In Chapter 3, details of the PDLM PA are discussed.
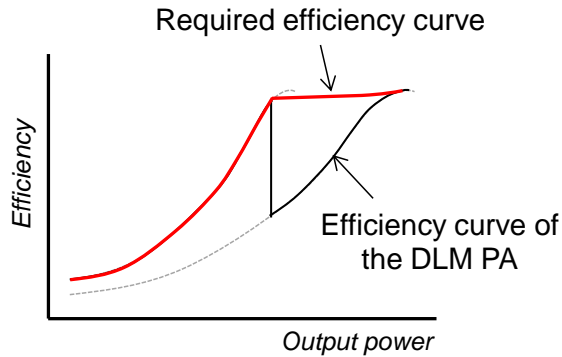
Figure 2.17 Conceptual efficiency curves for discrete-type DLM PA

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Chapter 3

A Pulsed Dynamic Load Modulation Technique for High-Efficiency Linear Transmitters

3.1   Introduction

Strong push for longer battery life time and growing thermal concerns for the modern 3G/4G mobile terminals lead to an ever-growing need for higher efficiencies from the handset power amplifiers (PAs). Furthermore, as the modulation signal bandwidth is increased and more complex modulation schemes are introduced for higher data rate, the peak-to-average power ratio (PAPR) of signals increases and the PA requires more power back-off to meet the stringent linearity requirement. Therefore, the PA design has to address the challenging task of enhancing the efficiencies in the back-off power levels.

Envelope tracking (ET) technique is the most widely used method to enhance the efficiencies in the back-off power region by modulating the supply voltage

according to the magnitude of the envelope signal. It has been successfully demonstrated for various modulation signals including long-term evolution (LTE) using different process technologies such as GaAs HBTs, SiGe HBTs and CMOS FETs [1-7]. However, as the envelope signal bandwidth increases, the efficiency of the supply modulator decreases and the pronounced memory effects may limit the overall system linearity.

Dynamic load modulation (DLM) technique is another method to boost the efficiency of a PA in the back-off output power levels [8-15]. This technique increases the efficiency by adjusting the PA load impedance according to the magnitude of the envelope signal. It can be categorized into two types, continuous and discrete types. Continuous-type DLM PA changes load impedance continuously by changing the capacitance of a varactor used in the load matching circuit. Although the continuous modulation of the load impedance may result in the significant efficiency enhancement, this method generates several problems for the handset PA applications. First, it is not easy to integrate a varactor with low loss and high breakdown voltage on a PA IC [16]. Second, the continuous load variation generates the distortion in the gain and phase of the PA, which degrades the overall system linearity. Moreover, in the practical mobile application, the impedance presented to the antenna varies considerably according to the phone usage patterns, which changes the voltage swing across the varactor and thus its capacitance value [16]. To achieve the required system linearity, complicated circuit techniques such as the complex load matching structure with multiple varactors [13] and memory digital predistortion (DPD) technique [14] should be employed.

Discrete-type DLM PA switches the load impedance from one value to another using an RF switch. The RF switch with low loss and high breakdown voltage can

be integrated into the PA IC using high electron mobility transistor (HEMT) or silicon-on-insulator (SOI) CMOS process. Moreover, the linearity issues raised by the continuous-type DLM PA can be mitigated or avoided since the gain and phase distortion occurs only at the switching point. By compensating for the gain and phase discontinuity at this switching power level, the linearity can be preserved regardless of the load variations at the antenna. The discrete-type DLM PA is thus more suited to the handset PA applications. However, the overall efficiency enhancement is quite limited since the PA does not always operate under the optimal load conditions. Further efficiency improvement is possible by using multi-bit load impedance switching [11, 12, 17], which again comes at the cost of the linearity and system complexity due to the increased number of gain and phase discontinuity points to compensate for.

In this section, a new method of DLM, called pulsed dynamic load modulation (PDLM), is proposed to operate the PA near the optimum impedance across a continuous back-off power range while still benefiting from the advantages offered by the discrete-type DLM PA. PDLM PA combines the concept of Class-S PA with 1-bit discrete load switching. The proposed concept is verified by designing and fabricating a prototype PDLM PA at 837 MHz using SOI CMOS process. The fabricated PDLM PA shows the overall system efficiency enhancement comparable to the widely used envelope tracking PA.

3.2 OPERATION PRINCIPLE OF THE PDLM PA

3.2.1 Concept of the PDLM PA

The discrete-type DLM PA enhances the efficiency at the pre-defined backed-off output power (PBO) by switching the load impedance to an optimum value at PBO.

If the required output power level is higher than the pre-defined power level (PBO), the load matching switches back to the load optimized for the maximum power (Pmax). Thus, between PBO and Pmax, the discrete-type DLM PA operates below saturation, which limits the efficiency improvement.

A proposed PDLM PA solves this problem by operating the PA near saturation for all the power levels between PBO and Pmax. This is achieved by applying pulse width modulation (PWM) signal to the switchable load matching circuit as shown in Fig. 3.1 (a), which toggles the load impedance between two discrete values, ZL,L and ZL,H. As the load changes between these two values, the overall gain of the PA is also adjusted accordingly so that the PA output power can toggle between PBO and Pmax. Fig 3.1(b) shows the PWM-modulated output power waveform. Since the PA does not operate at the intermediate power levels between PBO and Pmax, the efficiency degradation shown in the discrete DLM PA's can be avoided.

The envelope signal can be reconstructed at the output by cascading a PA with a high Q-factor band-pass filter (BPF) that filters out the pulse tones that are much higher than the envelope frequency. This can be understood by the frequency domain spectrum at the output of the PDLM PA shown in Fig. 3.1(c). Post-PA bandpass filters commonly used for the current mobile phones can be used for this purpose. Similar technique of reconstructing the envelope by filtering PWM signals has been demonstrated for pulsed load modulation (PLM) PAs [15].

Switchable load matching circuit

PA

Low power matching

High power matching

High-Q BPF

PWM signal

(a)

Pulse width modulated envelope signal

Required envelope signal

P_{max}

High power state

P_{BO}

Low power state

PDLM operation

Linear operation

Time

(b)

High-Q BPF

BW

Pulse harmonic frequency components

Power spectrum of the envelope signal

f_{RF}-$2 \cdot f_{PWM}$ f_{RF}-f_{PWM} f_{RF} f_{RF}+f_{PWM} f_{RF}+$2 \cdot f_{PWM}$

(c)

Fig. 3.1. (a) Conceptual block diagram, (b) time-domain output power waveform of the PDLM PA and (c) frequency-domain output power spectrum of the PDLM PA.
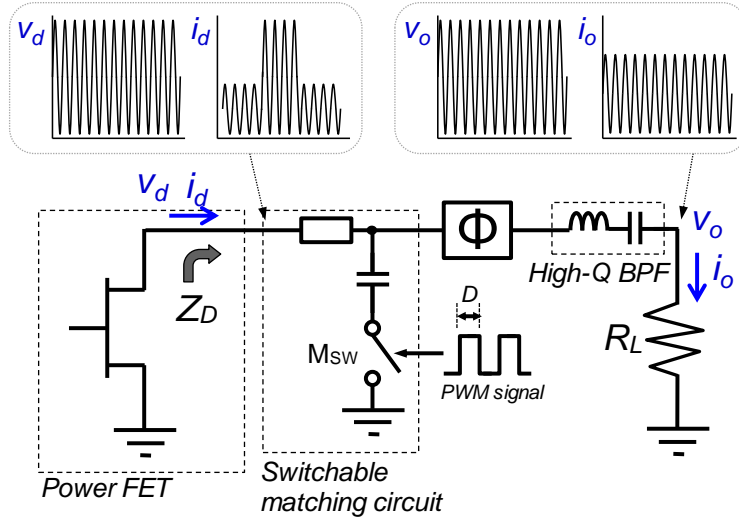
Fig. 3.2. The block diagram of the PDLM PA used for the simplified analysis.

3.2.2   Theoretical Analysis of the PDLM PA

Fig. 3.2 is the block diagram of the PDLM PA used for the analytical analysis. It is composed of a power FET, a switchable load matching circuit, a phase shifter (Φ), and a high-Q BPF centered at the carrier frequency. The fundamental load impedance, Z_D, presented to the power FET changes its states according to the PWM signal applied to the switch, M_{SW}. When the switch is turned-on, Z_D is set to R_{opt} for high power (HP) state, which is the optimum load at P_{max}. When the switch is turned off, Z_D increases to mR_{opt} for low power (LP) state, presenting the optimum load at P_{BO}. m is an impedance ratio ($m>1$). For theoretical analysis, the phase shifter is assumed to provide perfect short circuit to the intrinsic drain node of power FET at all the frequencies other than RF signal frequency. With this assumption, the voltage waveform at the intrinsic drain node is a pure sinusoid at the RF frequency (f_{RF}) as shown in Fig. 3.2. In this way, no power loss to the pulse harmonic frequency components is incurred theoretically. However, in the actual

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implementation, the ideal short conditions cannot be guaranteed at all the pulse harmonic frequencies, resulting in the efficiency degradation. This effect will be discussed in Section 3.4.

(i) High power (HP) state ($P_{out}=P_{max}$)

Let $Z_{D,H}$ be an optimum fundamental load for operation at P_{max}. To achieve the maximum output power, P_{max}, sinusoidal voltage and current swings, $v_{d,H}$, and $i_{d,H,}$ should be $V_{max}/2$ and $I_{max}/2$, respectively, where V_{max} and I_{max} are
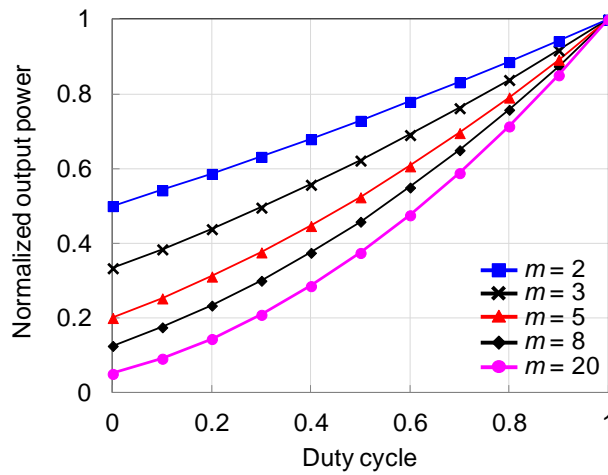
(a)
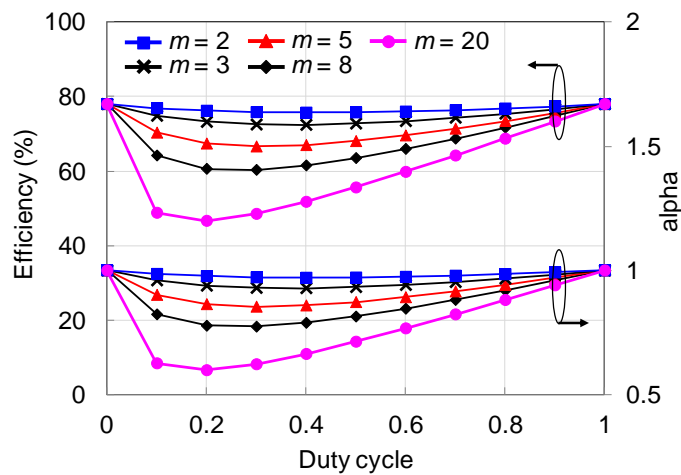
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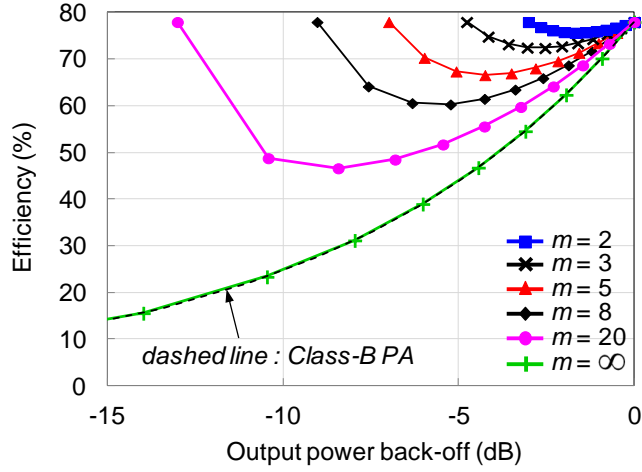
(c)

Fig. 3.3. Calculated (a) output power, (b) efficiency and α as a function of the duty cycle and (c) calculated efficiency curve according to the output power back-off. (Parameters used for calculation : $P_{out,H} = 1$, $\eta_H = 78\%$, $\eta_L = 78\%$)

the maximum voltage and current of the power FET, respectively. $Z_{D,H}$ can then be expressed as

$$Z_{D,H} = R_{opt} = \frac{v_{d,H}}{i_{d,H}} = \frac{V_{\max}}{I_{\max}}. \tag{1}$$

Assuming that the output power from the power FET is delivered to the load, R_L, without any power loss, the output current, $i_{o,H}$, and the output power, $P_{out,H}$, at the PA output are expressed as follows.

$$\frac{1}{2}i_{o,H}{}^2 R_L = \frac{1}{2}i_{d,H}{}^2 R_{opt} \tag{2}$$

$$i_{o,H} = \frac{I_{\max}}{2} \cdot \sqrt{\frac{R_{opt}}{R_L}} \tag{3}$$

$$P_{out,H} = \frac{1}{8}V_{\max} I_{\max} = P_{\max} \tag{4}$$

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(ii) Low Power (LP) State ($P_{out}=P_{BO}$)

In the same way, the fundamental load impedance at low power state, $Z_{D,L}$, can be expressed as

$$Z_{D,L} = mR_{opt} = \frac{v_{d,L}}{i_{d,L}} = \frac{mV_{max}}{I_{max}}.\tag{5}$$

The impedance ratio, m, is determined such that the output power in the low-power state is equal to P_{BO}. Then, the output current swing, $i_{o,L}$, and the output power, $P_{out,L}$, at the low power state are expressed as below.

$$i_{o,L} = \frac{I_{max}}{2} \cdot \sqrt{\frac{R_{opt}}{mR_L}}\tag{6}$$

$$P_{out,L} = \frac{1}{8}\frac{V_{max}I_{max}}{m} = P_{BO}\tag{7}$$

(iii) PDLM mode

When on/off pulse is applied with a duty cycle of D to the switchable matching circuit, the current and voltage swing can be expressed as,

$$v_d = const. = \alpha \cdot \frac{V_{max}}{2}\tag{8}$$

$$i_d = \begin{cases} \dfrac{I_{max}}{2} & \text{when } M_{sw} \text{ is ON} \\ \dfrac{I_{max}}{2m} & \text{when } M_{sw} \text{ is OFF} \end{cases}\tag{9}$$

$$i_o = Di_{o,H} + (1-D)i_{o,L}.\tag{10}$$

where α is the voltage amplitude ratio representing the voltage swing reduction from its maximum rail-to-rail value ($V_{max}/2$). As depicted in Fig. 3.2, the fundamental current swing at the drain current generator (i_d) toggles between $i_{d,H}$ and $i_{d,L}$ when the switch is turned on and off, respectively. Since the load impedance at the intrinsic drain current generator is assumed to be short circuit

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except at f_{RF}, only the sinusoidal voltage with constant amplitude ($\alpha \cdot V_{max}/2$) can exist at the drain as shown in (8).

Unlike the current waveform at the drain (i_d), the current at the output load, i_o, is a pure sinusoid at f_{RF} due to the filtering action of the series L-C resonator in the band-pass filter, and can be expressed as (10). Assuming lossless power transfer from the FET to the load, the output power, P_{out}, and the voltage amplitude ratio, α, can be calculated as

$$P_{out} = \frac{1}{2} v_d \cdot i_d = \frac{1}{2} i_o^2 \cdot R_L \tag{11}$$

$$P_{out} = P_{out,H} \left(D + \frac{1-D}{\sqrt{m}} \right)^2$$
$$= \left(D\sqrt{P_{out,H}} + (1-D)\sqrt{P_{out,L}} \right)^2 \tag{12}$$

$$\alpha = \frac{\left(D + \dfrac{1-D}{\sqrt{m}} \right)^2}{D + \dfrac{1-D}{m}}. \tag{13}$$

(iv) Efficiency calculation

The drain efficiency (DE) of the high- and low- power state, η_H and η_L, can be expressed with dc power (P_{DC}) and RF power (P_{out}) as,

$$\eta_H = \frac{P_{out,H}}{P_{DC,H}}, \quad \eta_L = \frac{P_{out,L}}{P_{DC,L}}. \tag{14}$$

The drain efficiency in the PDLM mode can be expressed using the RF output power and the weighted dc power consumption as

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{P_{DC,H} \cdot D + P_{DC,L} \cdot (1-D)}. \tag{15}$$

By substituting (12) and (14) into (15), η can be expressed with η_H and η_L as

$$\eta = \frac{\left(D + \dfrac{1-D}{\sqrt{m}}\right)^2}{\dfrac{D}{\eta_H} + \dfrac{1-D}{m \cdot \eta_L}}. \tag{16}$$

Using these equations, the output power and efficiency are calculated as a function of the duty cycle, D, for various impedance ratios, m. The results are plotted in Fig. 3.3 (a) and (b). For these simulations, both η_H and η_L are assumed to be 78%, which is the ideal Class-B drain efficiency. The output power increases monotonically with the duty cycle as shown in Fig. 3.3(a), which allows the power control by D. The calculated efficiency and α are plotted in Fig. 3.3(b). When D is 0 ($P = P_{BO}$) and 1 ($P = P_{max}$), the voltage swing hits rail to rail, showing $\alpha = 1$, as expected. However, when D is between 0 and 1, α curve shows sagging, implying that the voltage swing does not reach the rail-to-rail limit. The drain efficiency curve shows the same trend as shown in Fig. 3.3(b). Sagging is more pronounced as m is increased. Fig. 3.3(c) shows the power-dependent drain efficiency at various m values. As m is increased, the low power limit (P_{BO}) becomes smaller and a wider power range is covered by PDLM efficiency enhancement, but the efficiency sagging is more pronounced, especially in the middle of the power range. If m approaches infinity, P_{BO} becomes 0, which makes this PA very similar to PWM PA [18] or voltage-mode class-S PA [19, 20]. The drain efficiency curve, in this case, becomes identical to that of Class-B PA. The simplified analysis of this section clearly shows the overall efficiency enhancement of PDLM mode compared with the class-B PA, and also explains the root cause of the efficiency sagging in the mid-power range and the trade-off between the efficiency boost level and the applicable power range.
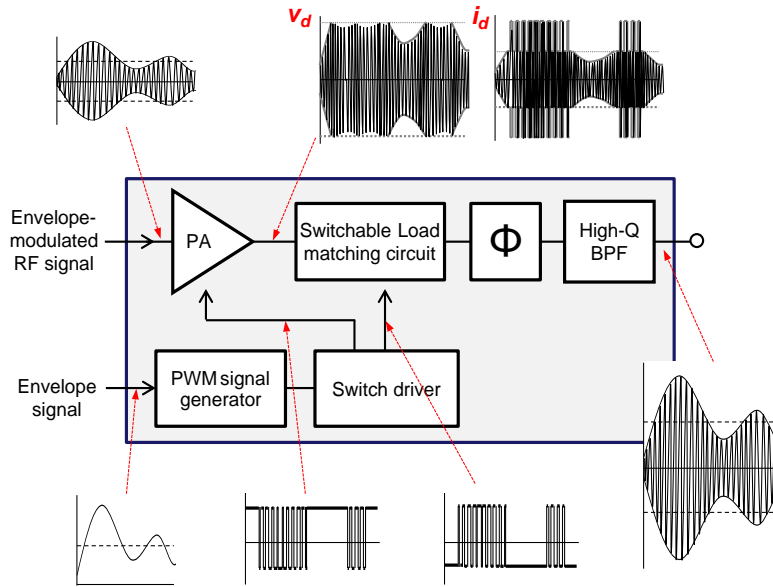
Fig. 3.4. Full block diagram of the PDLM PA and the time-domain waveforms.

3.3 CIRCUIT DESIGN

Fig. 3.4 is an overall block diagram of the proposed PDLM PA. It is composed of a switchable load matching circuit, a phase shifter (Φ), a high-Q BPF, a PWM signal generator, and a switch driver. Envelope-modulated RF signal is applied to the input of the PA while the envelope signal is applied to the PWM signal generator. Timing alignment between RF and envelope signal paths is performed by adjusting time delay in the signal generator. PWM signal generator converts the amplitude information to the pulse width only when the envelope voltage is higher than the predetermined value set by P_{BO} as described in Section 3.2. The converted PWM signal does not only control the switch in the switchable load circuit, but also the switch in the gain switching block through the switch driver (see Fig. 3.9 (a)).

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Fig. 3.5 shows the simulated spectrum of the PDLM PA using the ideal components. f_{PWM} is set at 100 MHz and 10 MHz LTE signal is applied for the simulation. The pulse tones at 737 and 937 MHz as well as the spectral noise outside the passband of BPF (824 - 849 MHz) are suppressed by 60 dB. In this way, the original modulation signal is restored.
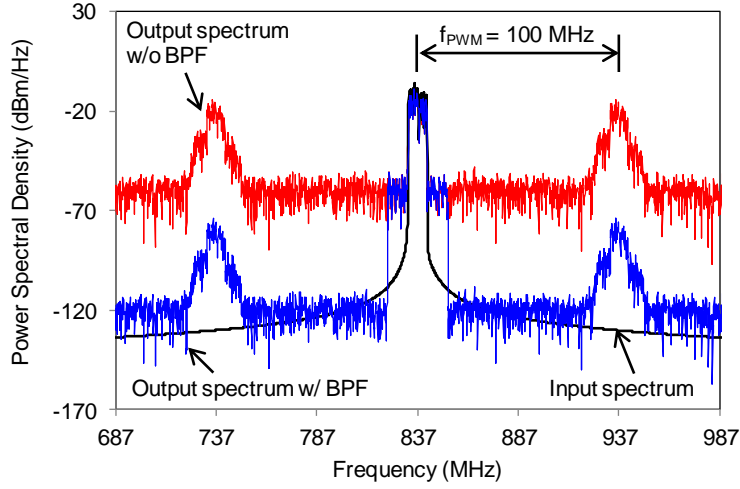
Fig. 3.5. Simulated input and output spectrum of the PDLM PA. Ideal BPF with 60 dB attenuation is applied in the simulation.

For the proof of the PDLM PA concept in this work, a simple PWM signal generator based on the triangle-wave signal is used even though the noise level is relatively high [21, 22]. By using envelop sigma-delta modulation (ESDM) technique [22-25] or more sophisticated modulation techniques [21, 25], the noise level near the carrier frequency can be further suppressed and cleaner modulation signal can be reconstructed.

The PA operates in a fixed-bias linear mode at the power levels below P_{BO}, and enters PDLM mode when the envelope voltage is raised above the predetermined level ($P_{out}>P_{BO}$). In PDLM mode, the switch driver is activated and turns on and off the load switch to modulate the load impedance for efficiency enhancement. The envelope-modulated output signal is reconstructed from the pulse-modulated signal

by filtering out the pulse tones using high-Q BPF. The details of the circuit designs are presented in the following subsections.

3.3.1   2 stage CMOS PA design

CMOS technology is promising for single-chip radio integration for cellular mobile terminals. Power amplifier is one key building block that makes full transceiver system integration very difficult. Besides the isolation issues, CMOS transistors suffers from low breakdown voltage and poor linearity due to relatively large knee voltages [26, 27].

Transformer-based power combining is proposed to overcome the low breakdown voltage limit. For example, an output power of 35 dBm is successfully demonstrated using distributed active transformer (DAT) structure [28]. Stacked FET configuration is another attractive option for power combining of low-breakdown voltage devices, where the voltage swing from each FET is added in phase to achieve high output power [26, 27]. By terminating the gates of common-gate (CG) FETs with proper capacitance, the voltage swing can be maintained below the breakdown voltage limits.

Stacked FET PA is composed of one common-source (CS) FET and multiple CG FETs connected in series, as shown in Fig. 3.6. Small shunt capacitors (C2, C3 and C4) are attached to each gate terminal of CG-FETs instead of large bypass capacitors for RF-grounding.   In this way, the voltage swing is divided between the shunt capacitors and the gate-to-source capacitance (C_{gs}) of CG-FET's, which helps to overcome the low breakdown limits of CMOS transistors [29].

CMOS FET used in the PA design is 0.32μm standard I/O FET in a 0.18μm silicon-on-insulator (SOI) CMOS technology. The breakdown voltage of CMOS FET is 2.5V. To achieve an output power of 1W with 4V supply voltage, the power

stage needs to handle a voltage swing as large as 10V. Quadruple stacked-FET cell is thus selected for the power stage and triple stacked cell for the driver-stage. Fig. 3.6(a) shows the overall circuit schematic of the 2-stage CMOS PA. The transistor size used for the power and the driver stage is 20 mm and 2 mm, respectively. Large-signal simulation was performed to calculate the voltage swing for each FET as a function of the shunt capacitor values. Based on this result, C2, C3, and C4 are

(a)

(b)
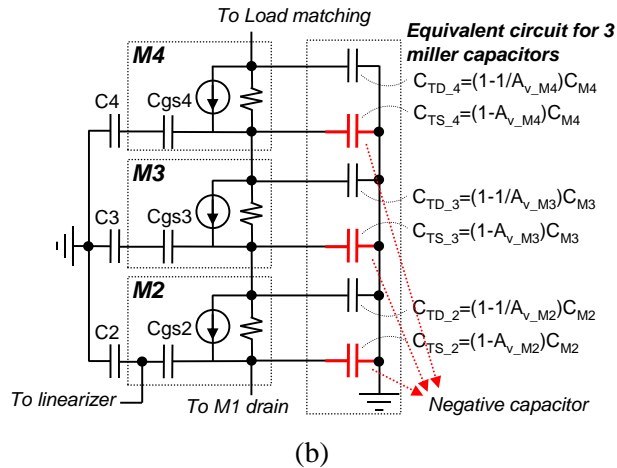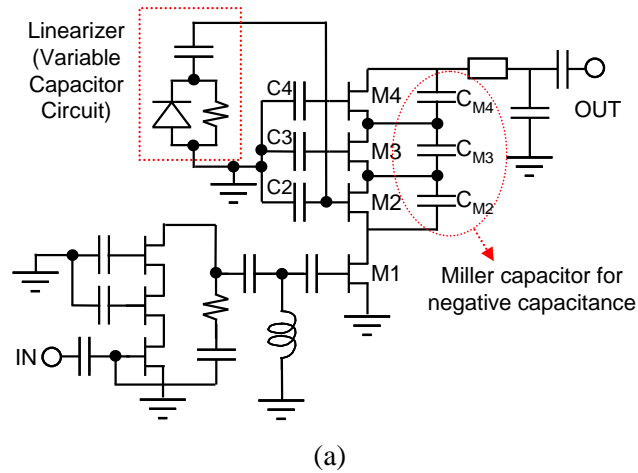
Fig. 3.6. (a) Overall circuit schematic of 2-stage stacked CMOS PA. (b) Simplified equivalent circuit of the CG-FETs used in the power stage.

determined to be 30, 10, and 6pF, respectively.

Fig. 3.6(b) shows the simplified equivalent circuit of the stacked CG-FET cells used for the power stage. To maximize the output power and PAE, the voltage swing from each FET must add in phase. However, large C_{gs} of 20mm FET (~23 pF) virtually prevents in-phase voltage stacking. This problem has been avoided by cancelling out C_{gs} with negative capacitance generated by the Miller capacitors (C_{M2}, C_{M3}, and C_{M4} in Fig. 3.6(a)) [30]. From Miller theorem, three Miller capacitors connected between the source and drain of CG-FETs can be transformed into six shunt capacitors at the source and drain terminals. The transformed capacitances at the source and drain can be expressed as a function of voltage gain, A_v, and Miller capacitor value, C_M, as shown in Fig. 3.6(b). Since CG-FET has a positive voltage gain greater than 1, the transformed capacitances (C_{TS}'s) at the source terminal have negative values.

Each of Miller capacitor value has been determined considering the voltage gain and overall capacitance loading; the upper Miller capacitances are larger than the lower ones since the upper transistor has smaller voltage gain and needs to cancel out additional shunt capacitance due to the lower Miller capacitors. After optimization using the circuit simulators, 3pF, 6pF, and 10pF are determined for C_{M2}, C_{M3}, and C_{M4}, respectively.

Fig. 3.7 shows a photograph of the fabricated PA chip. Die size is 1.0x0.9 mm^2. To minimize the source inductance of CS FET, large ground metal is added on the chip together with 7 ground pads for wire-bonding. Load matching and drain bias circuits are implemented off chip on FR4 substrate to leverage high-Q passive elements.
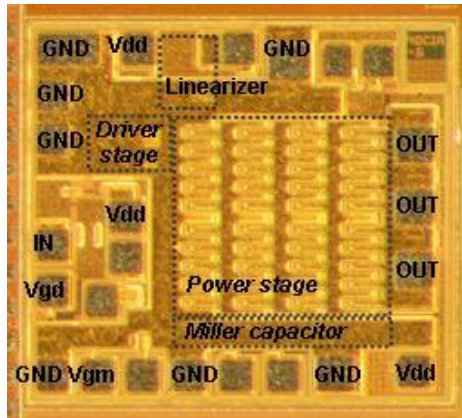
Fig. 3.7. Chip photograph of the fabricated CMOS PA.

To show the effect of the Miller capacitors, two PA modules with and without Miller capacitors are measured using continuous wave (CW) signal. As shown in Fig. 3.8, both simulation and measurement show that PAE can be improved by 6% with the help of capacitance cancellation. The peak CW PAE is 62 % at 1W for the PA with Miller capacitors.
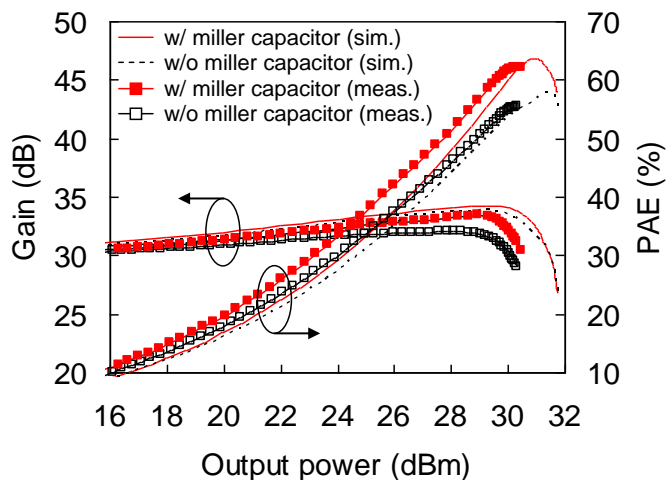
Fig. 3.8. Gain and PAE as a function of output power using CW signal at 837 MHz

To determine P_{BO} and optimum load impedance, load-pull simulation of the power stage is performed while sweeping the input power as shown in Fig. 3.9(b). The drain efficiency higher than 74% can be achieved for the PA output power ranging from 25 to 30 dBm, whereas rapid efficiency degradation is observed at the output power less than 25 dBm. Considering the efficiency-power trade-off, P_{BO} is set to be 25 dBm while P_{max} is set at 30 dBm. This choice is in line with wideband code division multiple access (W-CDMA) and LTE signals with a PAPR of 3.3-7.5 dB. Based on the loadpull simulation, the optimum load impedances at P_{BO} and P_{max} are determined as 26.9 + j13.4 Ω and 8.6 + j3.8 Ω, respectively. These values are the load impedances seen at the intrinsic drain node of the power-stage transistor cell after de-embedding C_{M3} using Miller's theorem.

A 2-section low-pass matching circuit shown in Fig. 3.9(a) is employed to implement the switchable load matching circuit. When the switch is turned on to connect the shunt capacitor (C_X), the load impedance changes from 16.3 + j16.9 Ω to 6.7 + j5 Ω. Since it was impossible to synthesize the optimum load impedances at both P_{BO} and P_{max} simultaneously using a single switchable capacitor, slight compromise is made for the load impedance at P_{BO} while meeting the power and efficiency targets at P_{max}. The loss of the output matching circuit for LP and HP state is simulated as 0.23 dB and 0.36 dB, respectively. To verify the switchable load design, continuous wave (CW) power sweep simulation is performed on the entire power-stage circuit including the switchable load circuit at both switch states. The results are plotted with the broken lines and overlapped with the dots from the loadpull simulations in Fig. 3.9(b). The efficiency degrades slightly at P_{BO} of 25 dBm, but reaches the optimum value at P_{max} of 30 dBm.

M₁ ~ M₃ (W / L = 20 mm / 0.32 μm)
M_D1 ~ M_D3 (W / L = 2 mm / 0.32 μm)
C_X = 6 pF, C_L = 2.4 pF
R_D1, R_M1 (= 7.5, 0.2 kΩ)
L_D, L_M1 (= 18, 15 nH)

C₂, C₃ (= 30, 10 pF)
C_M2, C_M3 (= 3, 4, 4 pF)
C_D2, C_D3 (= 6, 1.5 pF)
C_i1, C_i2 (= 15, 4 pF)
L_in, L_i (= 8, 1.5 nH)

(a)

(b)

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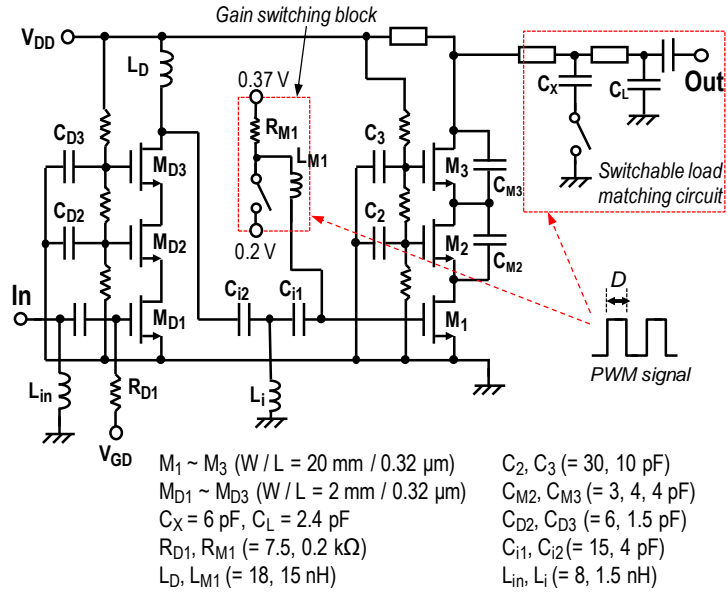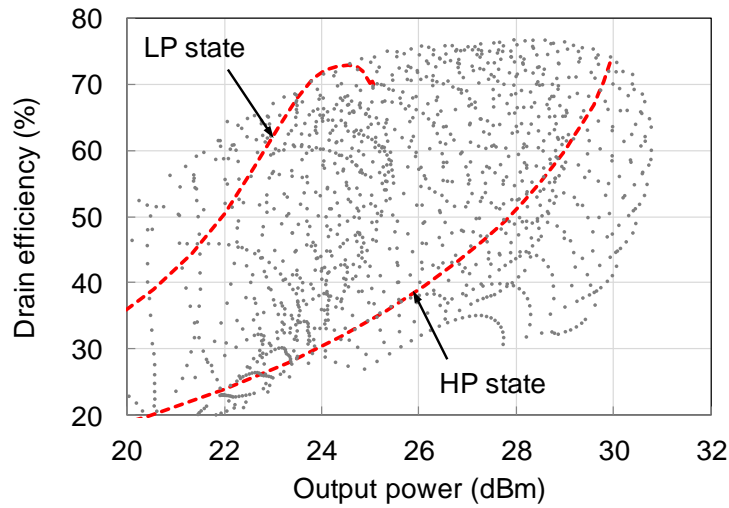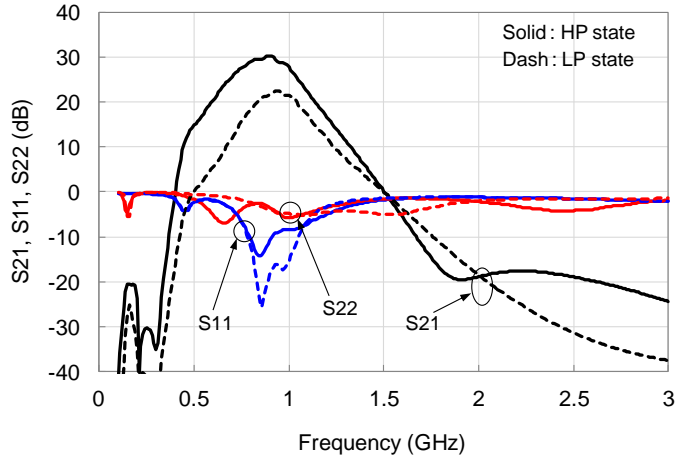
(c)

Fig. 3.9. (a) Circuit schematic and of a 2-stage stacked PA with the switchable load matching circuit, and (b) 1-stage load-pull simulation results while sweeping the power at each power state. (c) Measured S-parameters of the implemented 2-stage PA at each power state
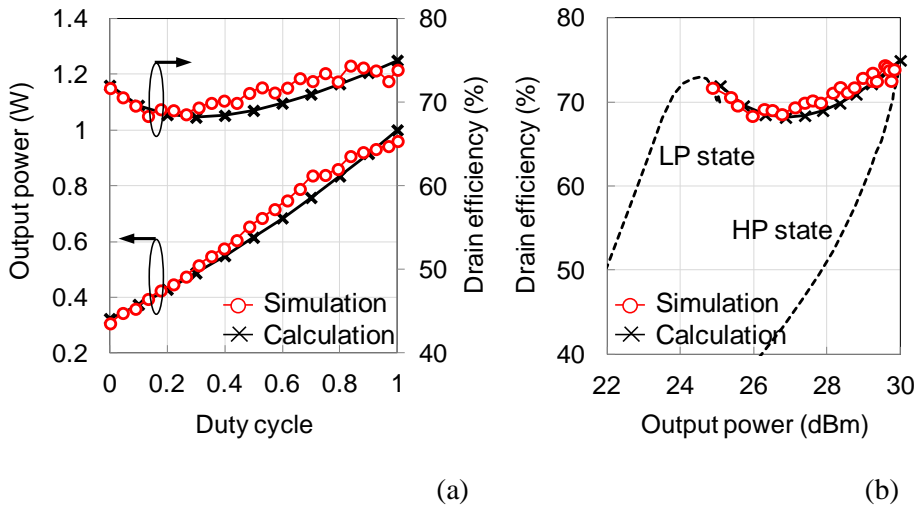
(a)   (b)

Fig. 3.10. Comparison of harmonic balance simulation and theoretical calculation for (a) output power, drain efficiency vs duty cycle and (b) drain efficiency vs output power. ($P_{out,H} = 1$ W, $m = 3$, $\eta_H = 75\%$, $\eta_L = 72\%$)

For PDLM operation, the PWM signal should be applied to the gain switching block as well as the switchable load matching circuit to achieve the rail-to-rail voltage swing at both P_{BO} and P_{max}; if the gain and the input power to the PA stayed

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the same while the load matching circuit was switched from the low-power to high-power state, the output power would not reach P_{max} due to the insufficient input drive level. To solve this problem, the gain switching block is added at the input of the main stage. The overall gain is boosted by changing the gate bias voltage from 0.2 V to 0.37 V when the load matching circuit is switched from the low-power to high-power state as shown in the measured S-parameters in Fig. 3.9(c).

The simplified analysis in Section. 3.2 is verified by comparing the theoretical calculation with harmonic balance simulation using Keysight's advanced design system (ADS). A 1-stage PDLM PA with an ideal RF switch is used for this comparison. Calculated and simulated DE and output power are plotted as a function of duty cycle in Fig. 3.10. Circuit simulation results are in very close agreement with the theoretical prediction except for the slight error near a duty cycle of 0.7. As expected, DE shows two peaks, one (75%) at a duty cycle of 1 corresponding to P_{max}, and the other (72%) at a duty cycle of 0 corresponding to P_{BO}. Between these two peaks, sagging is observed from both theory and simulation, due to the reduction in the voltage swing, reflected in α in Fig. 3.3(b). The excellent correspondence between the simulated and predicted DE vs output power shown in Fig. 3.10(b) validates the proposed concept and theoretical analysis presented in the previous section.
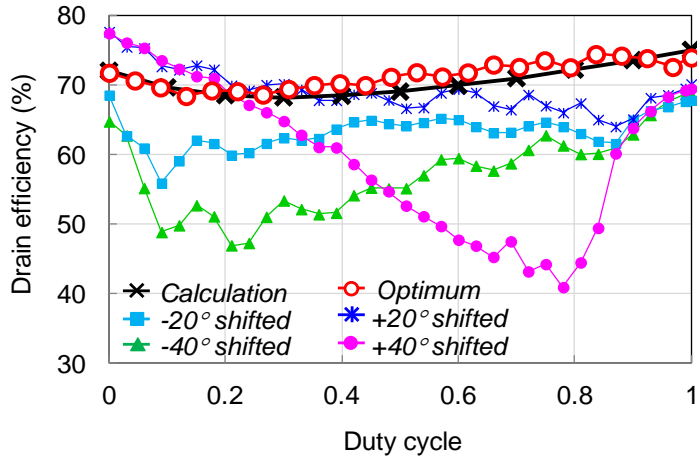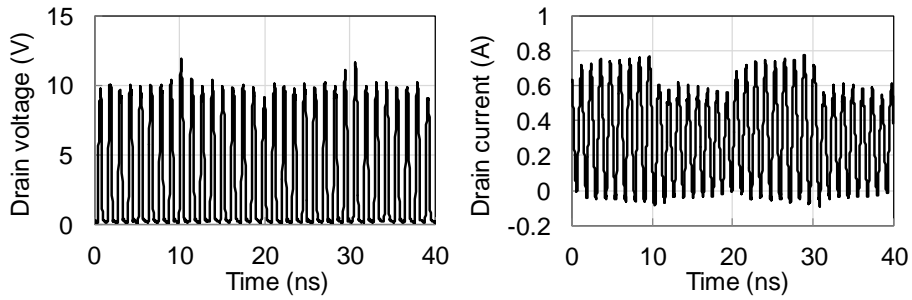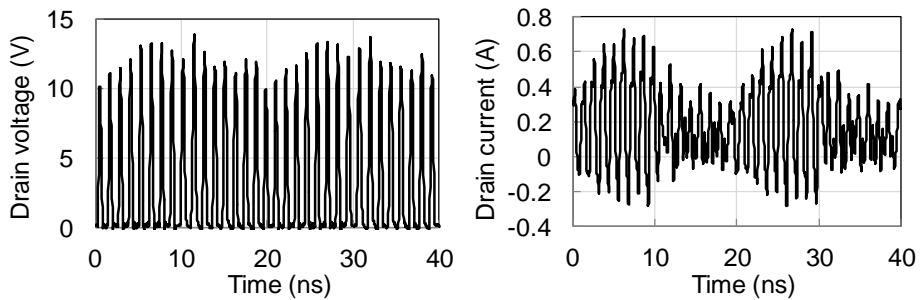
Fig. 3.11. (a) Simulated drain efficiency of the PDLM PA as a function of the duty cycle while changing the phase of the phase shifter. Simulated voltage and current waveforms at the drain node of the power stage (b) when the optimum phase is presented and (c) when the phase is off-tuned by + 40° from the optimum phase. The duty cycle used for the simulation is 0.5.
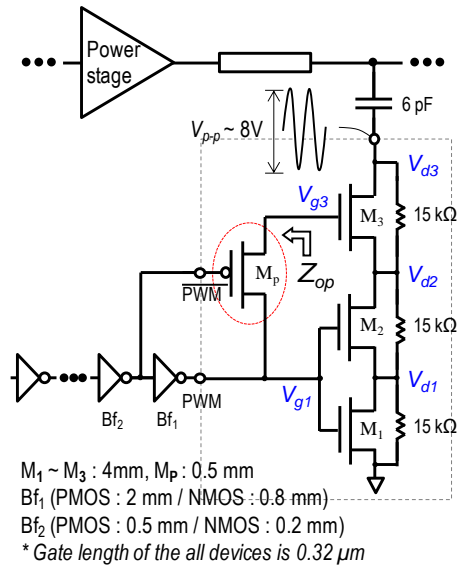
Fig. 3.12. Circuit schematic of the RF switch used for the load switching.
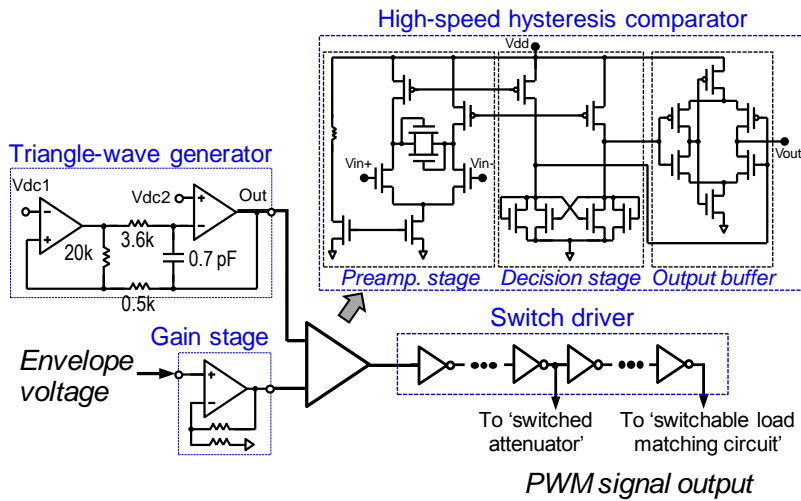
Fig. 3.13. Circuit schematics of the PWM signal generator and the switch driver.

The theoretical analysis assumes ideal short conditions for all the frequencies except for f_{RF}. However, this condition is very difficult to meet in practice for all

the harmonic mixing frequencies of PWM signals. To simulate the effect of non-ideal termination conditions, the phase shifter in Fig. 3.4 is off-tuned to present non-short terminations by applying the phase error. Fig. 3.11(a) shows the drain efficiency as a function of the duty cycle when the phase is off-tuned up to $\pm$ 40° in steps of 20°. As the phase deviates from its optimum, the drain efficiency is heavily degraded. For example, more than 20% of DE degradation is observed with a phase error of $\pm$ 40°. This phenomenon can be explained from the voltage and current waveforms at the intrinsic drain node shown in Fig. 3.11(b) and (c). Fig. 3.11(b) shows the voltage and current waveforms with a duty cycle of 0.5 with almost ideal short-circuit termination. Most of the pulse tones are shorted out and near constant-amplitude voltage swing and pulse-shaped current swing are observed as expected from the theory. Fig. 3.11(c) shows the waveforms with the same duty cycle, but with a phase error of + 40°. Due to the non-short termination, the pulse tones are observed in the voltage waveform; the voltage waveform consists of the RF signal at f_{RF}, and the pulse tones with frequencies of $f_{RF} \pm n f_{PWM}$, which are intermodulation products of RF signal (f_{RF}) and PWM signal (f_{PWM}). The current waveform is also heavily distorted due to the reactance of the load impedance, resulting in significant efficiency degradation. Since the harmonic load impedances of each power state are changed by shifting the phase of the phase shifter, different drain efficiency is exhibited at the duty cycle of 0 and 1 in Fig. 3.11(a). In summary, theoretical prediction shows that presenting near-short termination is important to achieve the maximum efficiency boosting using the proposed PDLM concept. This will be verified experimentally in Section 3.4.

3.3.2   High power RF switch design

For dynamic PA load switching, PDLM PA requires a low-loss RF switch that

can handle large voltage swing with a switching speed fast enough to handle PWM signals without any considerable delay. Stacked FETs are typically used for high-voltage switching applications. However, unlike the case of static switching applications, a simple gate biasing circuit consisting of large resistors [32] cannot be used for dynamic switching applications due to the excessive R-C delay caused by the large bias resistors.

In this work, p-FET-based gate biasing circuit is used for high-speed switching. The detailed circuit schematic of the load switch is shown in Fig. 3.12. Up to 25 dBm output power, the switch remains in the "off" state. The maximum voltage swing across the switch in this state is around 8 V. Considering the safe operating voltage of 3 V, a triple stack configuration has been employed. As shown in Fig. 3.12, a p-FET, M_p, is used to bias the gate of the topmost FET instead of a large resistor to achieve the required switching speed [33]. When M_p is in the off-state, the impedance seen from the gate of M_3, Z_{op}, is highly resistive (> 6 k), and the voltage swing at node V_{d3} is coupled to the node V_{g3} via the capacitance between gate and drain node of M_3. Thus, drain-to-source voltages of M_3 (V_{d3} - V_{d2}) and drain voltage of M_2 (V_{d2}) share the voltage swing across the entire switch. V_{d2} is also divided into drain-to-source voltage of M_2 (V_{d2} - V_{d1}) and drain voltage of M_1 (V_{d1}), but most of the voltage swing is applied across M_2 because smaller gate-to-source voltage is applied to M_2. Simulation shows that the voltage swing across each FET is maintained to be less than 3 V.

When the switch changes its state to "on", M_p is turned on by the switch driver, and the bottom two-stack FETs are turned on directly by the inverter following the switch driver. In this way, the triple-stack FET switch is turned on instantly with a negligible delay.

The same gate width of 4 mm is used for all three FETs in the stack while a

smaller gate width of 0.5 mm is used for M_p. The simulation shows that the rising and falling times are less than 0.2 ns at V_{g1} node when a large voltage swing of 8 V is applied at the node V_{d3}.

3.3.3   PWM signal generator and switch driver

Fig. 3.13 shows the circuit schematic of the PWM signal generator and the switch driver. The PWM signal generator is composed of a simple triangle-wave generator, a gain stage, and a high-speed hysteresis comparator. Using the envelope signal amplified by the gain stage and the triangle-wave signal as two inputs, the comparator generates a PWM signal with the pulse widths proportional to the envelope voltage. The frequency and output voltage range of the triangle-wave generator can be controlled by the applied bias voltages, and the maximum operating frequency is designed to be 200 MHz, which allows distortion-less tracking with 20 MHz LTE signals.

Hysteresis comparator [34] is designed to generate PWM signals with a minimum pulse width of less than 1 ns. The switch driver using the inverter chains offers the current driving capability to drive the switches with large input capacitance. It is worthwhile to note that the method of this work can be applied to wider LTE signals with minimum efficiency degradation by increasing the frequency of the PWM signal.

All the analog circuits are designed for low power consumption. The simulated power dissipation in the PWM signal generator and the switch driver is 15 mW and 20 mW, respectively, at the pulse frequency of 200 MHz.
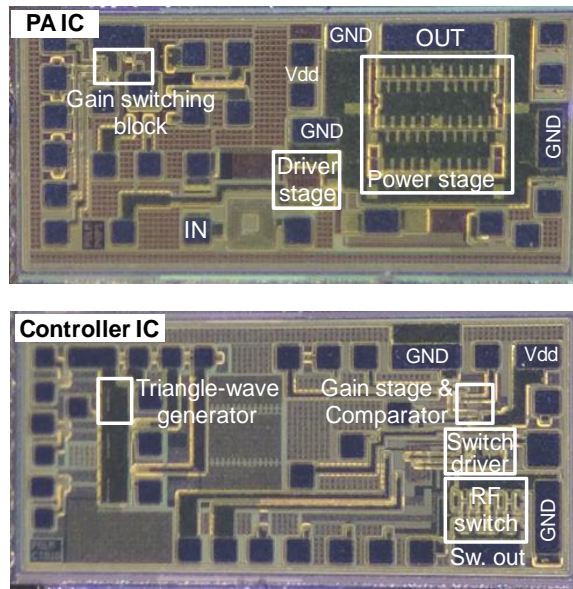
(a)
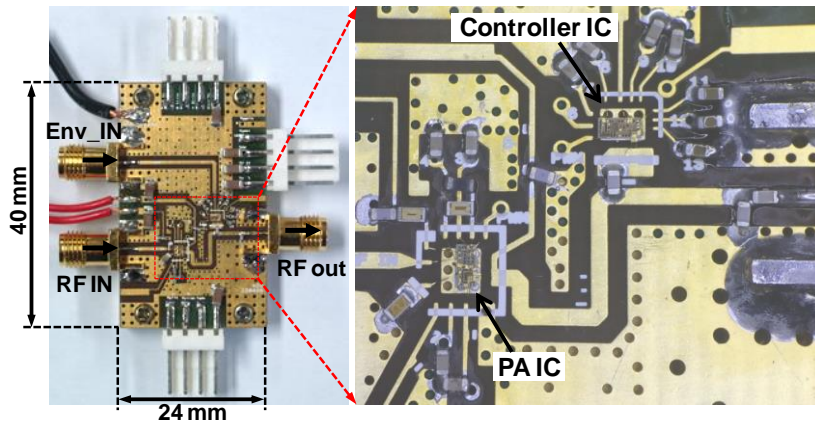
(b)

Fig. 3.14. Photographs of (a) the fabricated PA and controller chips (1.5 mm × 0.68 mm each) and (b) the prototype board with the chips mounted on the PCB.

3.4 EXPERIMENTAL RESULTS
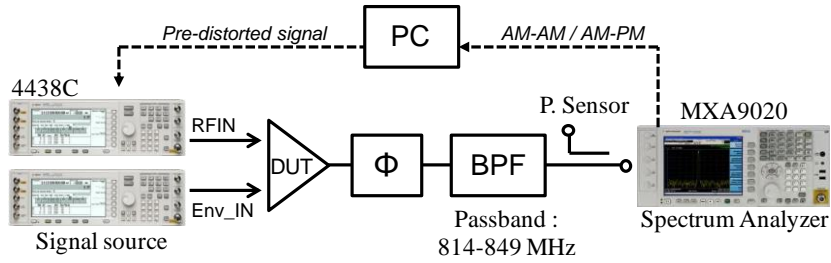
Fig. 3.15. Test setup used to characterize the PDLM PA prototype.
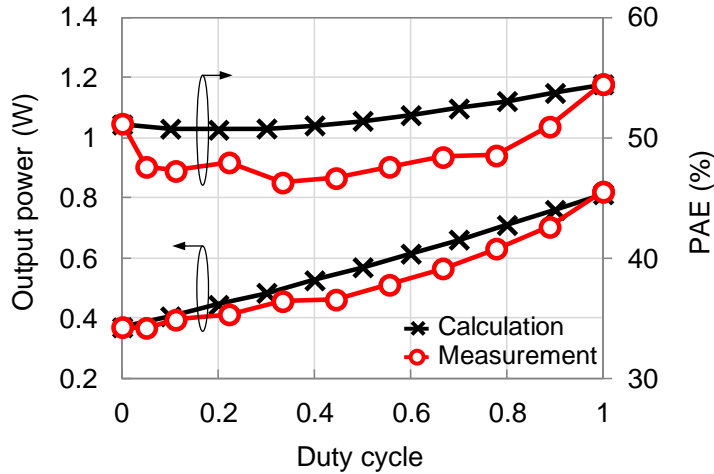
Fig. 3.16. Measured CW output power and PAE as a function of the duty cycle.

The proposed PDLM PA is fabricated using 0.32 μm SOI CMOS process. Fig. 3.14 shows the photographs of the fabricated ICs and the test module. For the proof-of-concept, the entire circuitry is implemented in two chips, a PA monolithic microwave integrated circuit (MMIC) chip operating at 0.837 GHz and a controller IC chip containing all the analog circuits and the RF switch. The size of both chips is 1.5 mm × 0.68 mm including the test patterns and pads. The size of the controller IC can be reduced to 1/4 if it is integrated into the PA chip. For chip evaluation,

both ICs are mounted on a 4-layer FR4 PCB, where the load matching circuit is also realized.

Fig. 3.15 shows the measurement setup of the PDLM PA. Two signal sources are used to generate the envelope signal and the envelope-modulated RF input signal. Dynamic AM-AM and AM-PM data are measured using the spectrum analyzer. For linearity correction, digitally predistorted signal is generated by Matlab and is downloaded to the signal sources. The phase shifter is implemented with RF cables and connectors for the prototype test. The high-Q BPF is realized with a cavity filter with an insertion loss of 1 dB and out-of-band rejection higher than 50 dB. Since most of the current mobile phone systems use high-Q BPFs after the PAs, such as surface acoustic wave (SAW) or film bulk acoustic resonator (FBAR) based duplexer filters for frequency division duplex (FDD) LTE and coexistence BPFs for time division duplex (TDD) LTE systems, the loss of BPF (1 dB) is de-embedded in the efficiency estimation of PDLM PAs while that of the phase shifter (0.2 dB) is included.

The PDLM PA module is first characterized using CW signal. For this measurement, a dc voltage is applied to the envelope signal input, which controls the duty cycle of the PWM signal. The phase delay of the phase shifter is swept to find the optimum phase shift so that the impedance presented to the output-stage transistor at the harmonic pulse tones can be near-short circuited. In the actual PA implementation, the phase shifter can be realized using lumped-element circuits such as a T-circuit consisting of two series inductors and a shunt capacitor, which can be absorbed into the PA load matching circuit. Fig. 3.16 shows the measured output power and PAE of the entire PA module as a function of the duty cycle with a fixed input power of 2.64 dBm. Both the output power and PAE closely follow the theoretical prediction. However, the measured PAE of the complete two-stage

PA module shown in Fig. 3.16 is lower than the simulated DE of a single-stage power cell in Fig. 3.10 since it includes the power consumption of the driver stage and the losses in on-chip interstage and off-chip output matching circuit and phase shifter. Also, PAE sagging is more pronounced in the measurement than the simulation. This is attributed to the non-ideal short termination at the intrinsic drain node of the output transistor, as will be explained later.

(a)

(b)
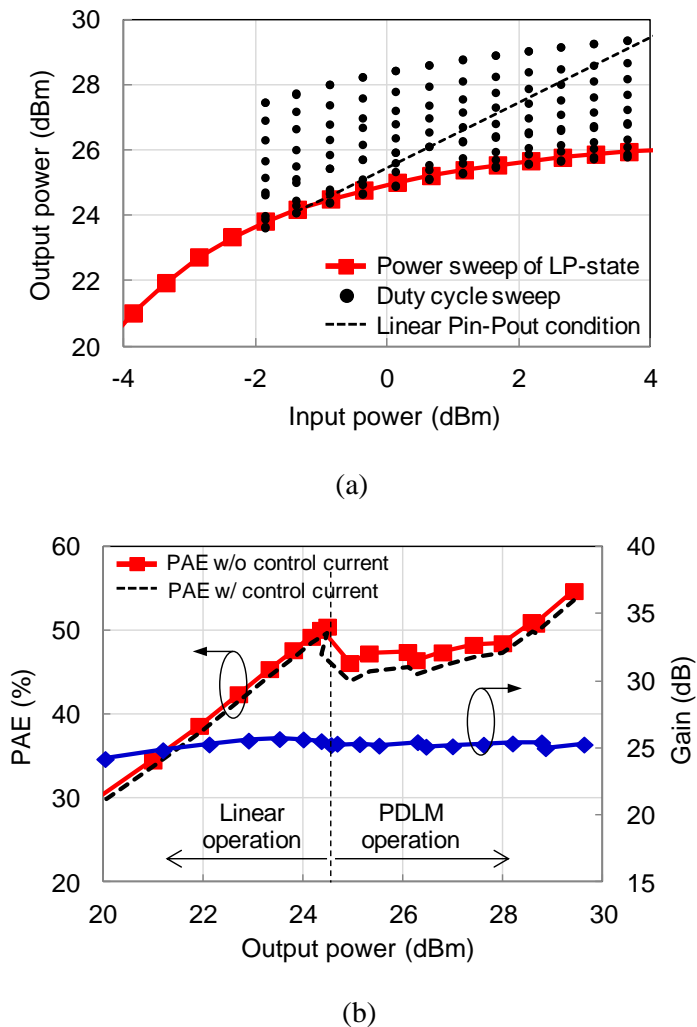
Fig. 3.17. Measured CW power-sweep characteristics of the PDLM PA: (a) output power vs input power while sweeping the duty cycle to extract the shaping table providing the linear P_{in}-P_{out} relationship and (b) PAE and gain vs output power using the extracted shaping table.

TABLE 3.1

SHAPING TABLE LISTING THE INPUT VOLTAGE TO THE PWM SIGNAL
GENERATOR ACCORDING TO THE RF INPUT POWER TO ACHIEVE THE LINEAR
PIN-POUT CHARACTERISTICS

RF input power (dBm)	-0.87	-0.37	0.13	0.64	1.15	1.65	2.15	2.64	3.14	3.65	4.15
Input voltage to the PWM signal generator (V)	0.38	0.42	0.46	0.5	0.54	0.58	0.62	0.66	0.7	0.72	0.74
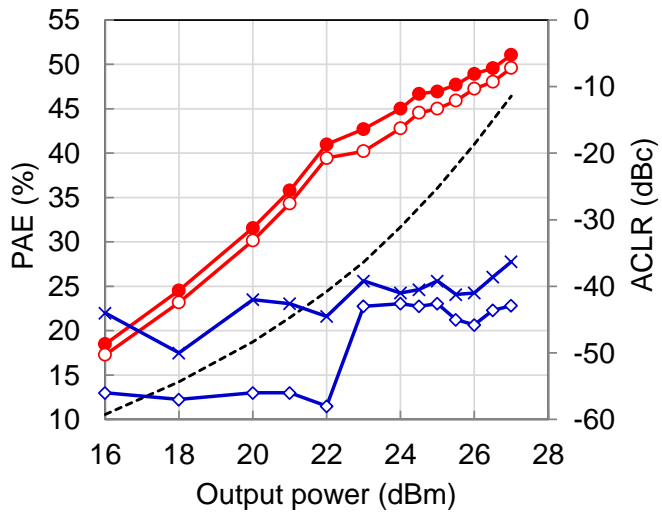
Fig. 3.18. Measured gain, PAE and ACLR as a function of the output power
using WCDMA signal when the cavity filter is applied to the PDLM PA.
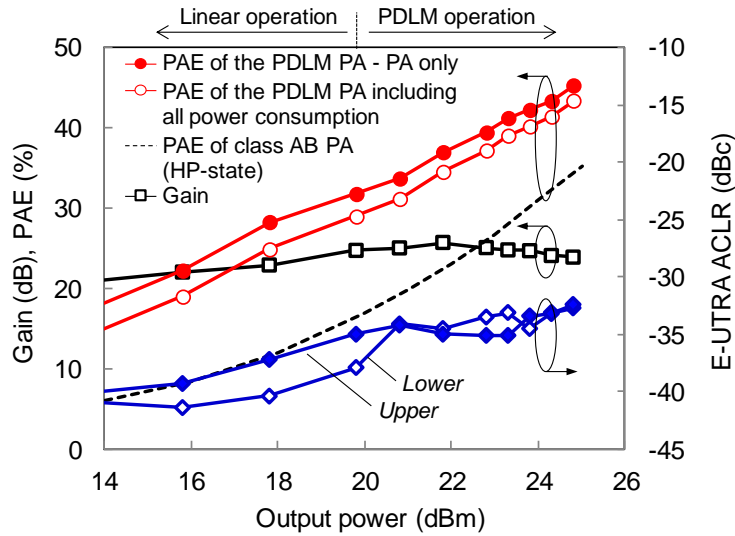
Fig. 3.19. Measured gain, PAE and E-UTRA ACLR as a function of the output power using 10 MHz-bandwidth 16-QAM LTE signal when the cavity filter is applied to the PDLM PA.
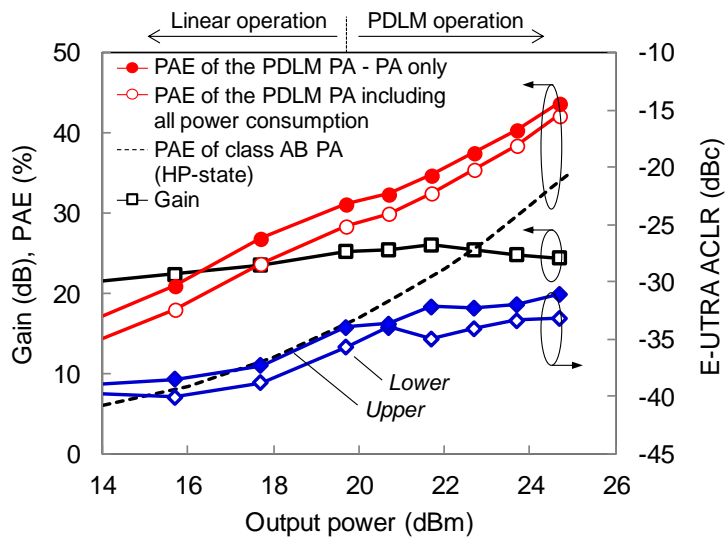
Fig. 3.20. Measured gain, PAE and E-UTRA ACLR as a function of the output power using 10 MHz-bandwidth 16-QAM LTE signal when the SAW duplexer filter is applied instead of the cavity filter.

The output power of PDLM PA depends on both the input power and the duty cycle. For linear PA operation, one needs to find the shaping table that sets the duty

cycle at each input power so that linear P_{in}-P_{out} characteristics can be achieved. The procedure to find the shaping table is explained below. First, CW power sweep is performed in the low power state to derive the baseline compression curve, as shown with a red line in Fig. 3.17(a). If the input power level is large enough to show gain compression, duty cycle sweep is performed at each input power level. Then, a straight line representing linear P_{in}-P_{out} characteristics is drawn as shown with the black dotted line in Fig. 3.17(a). Based on this line, a shaping table can be extracted between the RF input power and the envelope voltage input to the PWM signal generator, as shown in Table 3.1. The measured gain and PAE using the extracted shaping table are shown in Fig. 3.17(b). As expected, the gain is almost flat (25.2 dB ± 0.2 dB) up to an output power of 29.5 dBm. Measured CW PAE higher than 44% is achieved over > 6 dB-power back-off range from 23.2 to 29.5 dBm.

Based on the extracted shaping table, a full envelope-modulated PA test is performed using 3.84 MHz-bandwidth wideband code division multiple access (WCDMA) signals and 10 MHz-bandwidth 7.5 dB-PAPR 16-QAM LTE signals. Fig. 3.18 and Fig. 3.19 show the measured PAE, gain and adjacent channel leakage ratio (ACLR) as a function of the output power. The PA operates in the linear mode for average output power below 22 and 20 dBm, above which the PA switches to PDLM mode for WCDMA and LTE signal, respectively. Also shown in Fig. 3.19 as a dotted line is the reference PAE curve of a fixed bias/load class-AB PA. Compared with the reference, PAE enhancement is more than 10% across the entire power range. In the linear mode (< 20 dBm), the switchable load circuit statically sets the load impedance to an optimum value for 20 dBm. In the PDLM mode (20 ~ 25 dBm), the dynamic load switching allows efficiency boosting by more than 10%, which includes the power dissipation of the control circuits.

To avoid ACLR degradation, the pulse frequency should be at least 7-10 times the signal bandwidth. This also allows the pulse tones to appear outside transmitter passband of the post-PA duplexer filters, which provides more than 30 dB out-of-band rejection. For this test, the pulse frequency of PWM signal generator is set at 140 MHz, and the measured power consumption of the control circuits is 29 mW during PDLM operation. The power consumption reduces to 15 mW in the linear mode since the switch driver does not consume any current in the linear mode. The overall PAE reaches 43.4% at a linear LTE output power of 24.8 dBm, where evolved UMTS terrestrial radio access (E-UTRA) ACLR of -32.4 dBc is achieved. The PA-only PAE, excluding the power consumption of the control circuits, is as high as 45.3% at 24.8 dBm.

To verify that the proposed PDLM PA can work with the bandpass filters widely used in the current mobile phones, we performed PDLM PA test using a commercial SAW duplexer filter, B8099 from TDK instead of the waveguide cavity filter. As shown in Fig. 3.20, due to the reduced Q-factor of SAW filters, the measured peak PAE is reduced by ~1.2% while the worst-case E-UTRA ACLR degrades by ~1.3 dB. However, no abnormalities were found for PDLM operation, which shows that the proposed PDLM PA can be applied to the mobile phones using the existing duplexer filters.

TABLE 3.2

MEASURED S-PARAMETER OF THE LOAD IMPEDANCE

	- 45° shifted		*Optimum*		*+ 45° shifted*	
	LP	HP	LP	HP	LP	HP
$f_{RF} - 2f_{PWM}$	0.97<171°	0.94<167°	0.95<168°	0.87<157°	0.51<177°	0.85<195°
$f_{RF} - f_{PWM}$	0.87<151°	0.78<213°	0.89<188°	0.96<184°	0.97<174°	0.95<173°
f_{RF}	-	-	-	-	-	-
$f_{RF} + f_{PWM}$	0.91<196°	0.97<183°	0.96<174°	0.95<174°	0.82<146°	0.91<192°
$f_{RF} + 2f_{PWM}$	0.88<183°	0.9<180°	0.86<162°	0.79<194°	0.81<203°	0.9<183°
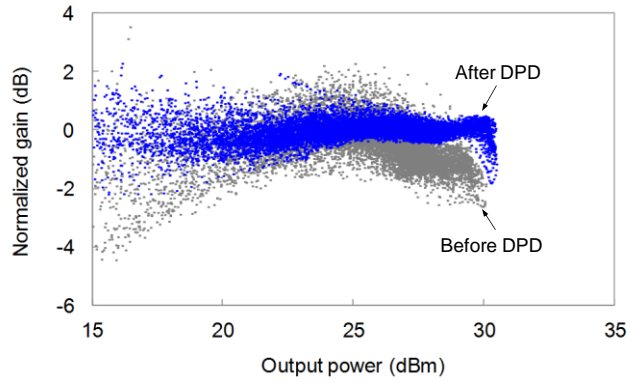
(a)
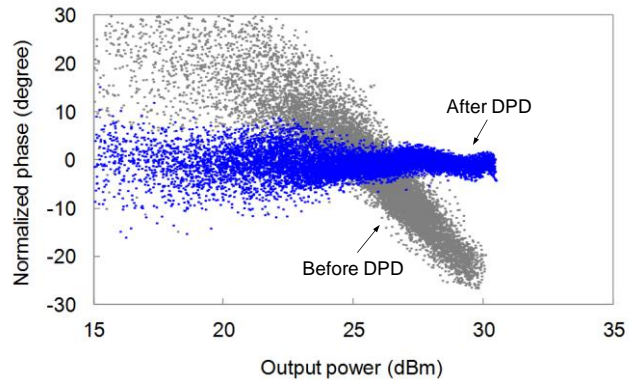
(b)
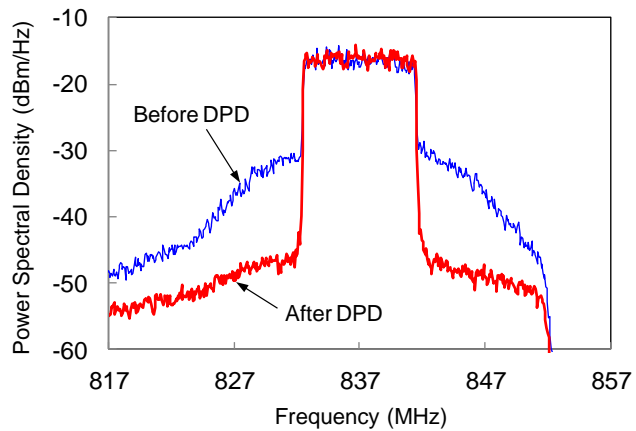
(c)

Fig. 3.21. Measured dynamic (a) AM-AM and (b) AM-PM characteristics and (c) LTE output spectrum of the PDLM PA at the output power of 24.8 dBm.
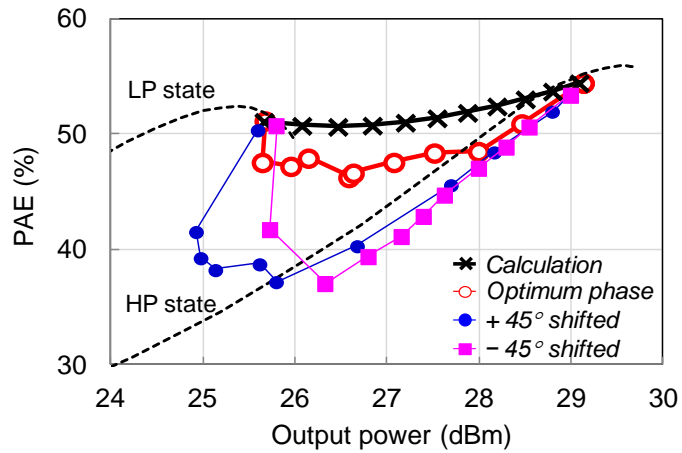
(a)
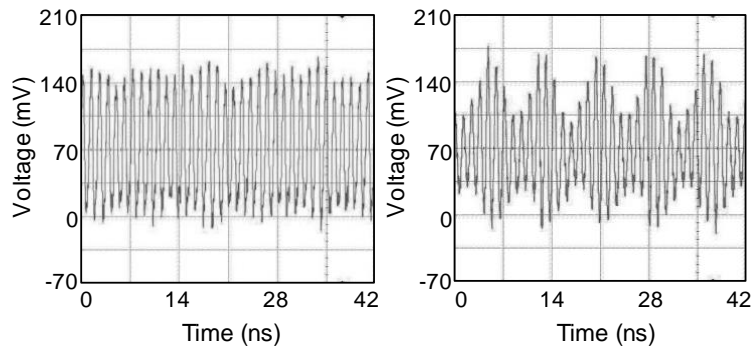
(b)   (c)

Fig. 3.22. (a) Measured efficiency as a function of the output power at various phase offsets of the phase shifter. Measured drain node voltage waveform (b) for the optimum phase condition and (c) for the phase + 45° shifted from the   optimum phase. The duty cycle is 0.5.

TABLE 3.3

PERFORMANCE COMPARISON TABLE AMONG HIGH-EFFICIENCY PAS FOR W-CDMA AND LTE MOBILE TERMINAL APPLICATIONS

Reference	Technique	Frequency (GHz)	Application	Bandwidth (MHz)	PAPR (dB)	PA Technology	PAE (%)	Output power (dBm)	Gain (dB)	ACLR (dBc)	Output matching	DPD
[3]	Envelope tracking	0.7	LTE 16-QAM	10	7.5	0.35 μm SiGe BiCMOS	41.1	28.1	–	5.63% (EVM)	Off-chip	No
[4]	Envelope tracking	0.782	LTE 16-QAM	10	6.6	0.35 μm CMOS SOS	50.1	29.3	20.5	–46.5	Off-chip	Yes
[5]	Envelope tracking	1.85	LTE 16-QAM	10	7.5	0.18 μm CMOS	34.1	26	10	–34.2	Off-chip	No
[35]	Doherty	1.88	LTE 16-QAM	10	7.5	GaAs HBT	45	29	25	–34	Off-chip	No
[13]	Varactor-based Dynamic load modulation	1.75	WCDMA	3.84	3.3	pHEMT	43 (DE)	15	10.5	–33	Off-chip	No
[14]	Varactor-based Dynamic load modulation	1	WCDMA	3.84	7	LDMOS	53	30.9	–	–29 / –43	Off-chip	Yes* Yes**
[36]	Transformer-based Dynamic load modulation	2.2	802.11g 64-QAM	20	6.5	65nm CMOS	24.5 (DE)	16.8	–	–28 dB (EVM)	On-chip	Yes
This work	Pulsed dynamic load modulation	0.837	LTE 16-QAM	10	7.5	0.32 μm CMOS SOI	43.4	24.8	23.9	–32.4	Off-chip	Yes

* Quasi-static inverse model (AM/AM and AM/PM)

** Memory DPD with static inverse model proposed in the paper

Fig. 3.21 (a) and (b) show measured dynamic AM-AM and AM-PM characteristics of PDLM PA before and after DPD. A simple memory-less DPD with 5th order polynomial curve fitting method is used for this proof-of-concept

work. Average gain compression and phase lag are effectively linearized by applying memory-less DPD. However, non-negligible dispersions in dynamic characteristics are observed, indicating the memory effect. This is attributed to non-ideal drain voltage waveform as demonstrated in Fig. 3.11 and limits ACLR improvement. Fig. 3.21(c) is the output spectrum of the PDLM PA with and without DPD. By applying DPD, E-UTRA ACLR is improved by more than 10 dB. The asymmetric spectrum is caused by the high-Q bandpass filter following the PA, which has a pass band of 814-849 MHz.

During PDLM operation, E-UTRA ACLR stays higher than -35 dBc even after DPD linearization. It is attributed to the voltage waveform imperfection as shown in Fig. 8. The failure to short circuit all the pulse tones at the intrinsic drain node of the power FET leads to the fluctuation of the voltage swing and instantaneous output power. This generates the memory effect in the PDLM PA and degrades the linearity of the overall PA as well as the efficiency.

To understand the actual load termination conditions at each pulse tone frequency, the S-parameter of the load impedance is actually measured in both low-power and high-power load states at 4 different pulse tone frequencies, and the results are shown in the center column of Table 3.2. Since the spectral power at 1st order mixing product, $f_{RF} \pm f_{PWM}$ is much larger than that at higher order mixing products, it is important to present near short impedance at $f_{RF} \pm f_{PWM}$. At $f_{RF} \pm f_{PWM}$, the phase error from the perfect short circuit (180°) is less than 8°, but it increases to ~ 23° at second-order mixing product ($f_{RF} \pm 2f_{PWM}$), which causes pronounced PAE sagging during PDLM operation, as shown in Fig. 3.16. To further verify this experimentally, the phase shifter is intentionally off-tuned by ± 45° to introduce excessive phase errors at $f_{RF} \pm f_{PWM}$ while reducing the errors at $f_{RF} \pm 2f_{PWM}$. The measured phase at each pulse tone frequency for - 45° and + 45° offset is

summarized in the first and third columns of Table 3.2, respectively. The phase error is reduced at $f_{RF} \pm 2f_{PWM}$ while increased excessively at $f_{RF} \pm f_{PWM}$. Fig. 3.22(a) compares the measured efficiency as a function of the output power at each phase shifter setting. As expected, severe efficiency degradation is observed when the load deviates from "short" at $f_{RF} \pm f_{PWM}$. To show that the efficiency degradation is indeed due to non-constant voltage swing, the voltage waveform is also measured using a high-impedance probe at the drain node of the main-stage transistor in Fig. 3.22(b) and (c) for two different phase offsets. Almost constant voltage swing is observed for the optimum phase condition whereas the voltage swing shows pulse tones for $\pm$ 45° phase offset. This experiment shows the importance of presenting near short conditions for PDLM PA operation.

It is worthwhile to note that the proposed PDLM PA is sensitive to the time alignment between the envelope and RF input signals as in the case of ET PAs. E-UTRA ACLR degradation of PDLM PAs according to the time misalignment has been characterized and compared with ET PA [7], and very similar sensitivity to time misalignment has been observed.

It is also important to investigate the scalability of the proposed method for the
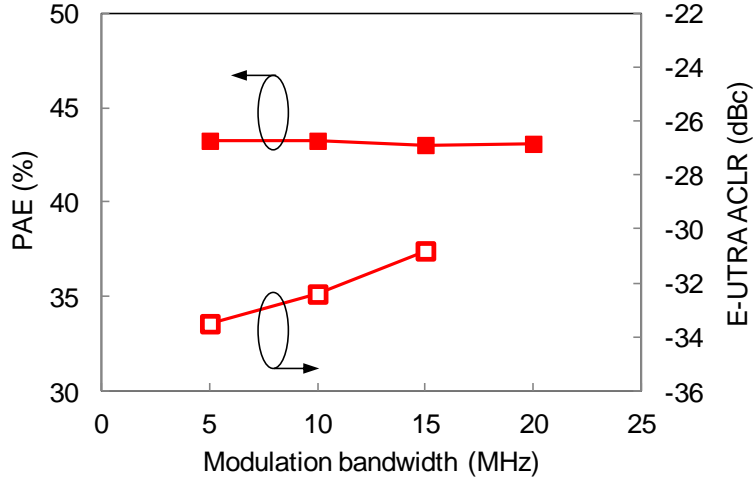
Fig. 3.23. Measured PAE and E-UTRA ACLR of the PDLM PA according to the modulation bandwidth of the LTE signal at the output power of 24.8 dBm.

applications with wider signal bandwidth. For example, the supply modulator for envelope tracking typically shows degraded efficiency for wider-bandwidth LTE signals [3]. We have measured PAE and ACLR of PDLM PA using LTE signals with bandwidths of 5, 10, 15 and 20 MHz in Fig. 3.23. Since the spectral regrowth of 20 MHz LTE signal is attenuated by the high-Q band-pass filter, ACLR data are shown only up to 15 MHz. The PAE stays almost flat while ACLR degrades for wider signal bandwidth due to the pronounced memory effect arising from the increased quantization noise as the signal bandwidth approaches PWM frequency. ACLRs can be further improved by employing memory-DPD and more sophisticated digital modulation techniques with lower noise floor. Also, the band-selective load matching circuits realized with LC resonators will help reduce the phase errors at the harmonic pulse tones, and result in improved ACLR at the expense of increased matching circuit loss.

Performance comparison of the proposed PDLM PA with other state-of-art results is summarized in Table 3.3. Considering the maturity of the envelope

tracking, it is not surprising that one of the latest ET PA works shows better PAE data than the result of this work [4]. However, after de-embedding the loss of the post-PA BPF, the demonstrated PAEs in this proof-of-concept work are comparable to or better than most of the ET results published to date. This work opens a new possibility of eliminating the bulky supply modulator and a potential for supporting LTE signals with wide modulation bandwidth without considerable efficiency degradation.

3.5   Conclusion

A PDLM PA concept is proposed to enhance PA efficiencies in the back-off power levels without using a supply modulator. PDLM concept combines dynamic load switching with Class-S PA concept to operate the PA's near optimum efficiencies in the top ~5 dB power region, which results in the overall PAE improvement for high-PAPR signals such as LTE signals. The proposed concept is realized with low-power control circuits unlike envelope tracking, which requires high-power circuits such as dc-dc converters and linear amplifiers. Hence, the overall PA efficiency does not degrade rapidly as the signal bandwidth increases. By increasing the speed of the control circuits such as PWM signal generator, PDLM PA can potentially handle LTE signals wider than 20 MHz with minimal degradation of the overall efficiencies.

The proof-of-concept experiment has been performed in this work by designing a two-stage PA with switchable load matching using SOI CMOS process. The triple-stacked CMOS FETs are used for both driver and power stages. The PWM generator and switch driver circuit are designed and fabricated using the same SOI CMOS process on separate chips. Both chips are mounted on a PCB, where the load matching circuit is also realized, for characterization using both CW and LTE

signals. Overall CW PAEs higher than 44% are achieved over >6 dB-power back-off range from 23.2 to 29.5 dBm. By extracting a shaping table that sets the proper relationship between the RF input power with the duty cycle of the PWM pulses, a linear PA operation has been demonstrated. LTE tests have shown that the PDLM PA of this work can maintain the overall PA efficiencies around 43.4% with minimal PAE degradation as the LTE signal bandwidth increases from 5 to 20 MHz. Wider-bandwidth LTE operation can be achieved using more sophisticated pulse width modulation techniques and by increasing the speed of the control circuits.

The effect of non-ideal terminations at the intrinsic drain terminal has also been analyzed, showing the importance of eliminating the pulse tones for PDLM operation. The PDLM PA concept of this work can provide a potential solution for high-efficiency PAs for the future mobile terminals using wideband modulation signals.

3.6　References

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Chapter 4

Discussions

4.1   Operation bandwidth of the PDLM PA

As the amount of data communication is explosively expanded in modern communication environment, signal bandwidth (BW) of a modulation scheme is expected to be broadened. Thus, efficiency estimation of the PDLM PA according to the signal BW is simulated and is compared with ET PA.

In case of ET PA, supply modulator is the limiting factor for wideband operation. Hybrid switching amplifier (HSA) is prevalently used for its good efficiency and noise performance, as shown in Fig. 4.1. Since large device periphery is used for the switching amplifier to reduce voltage drop, switching loss proportional to the switching frequency determines large portion of supply modulator efficiency. As the signal BW is increased, switching frequency is increased accordingly and overall modulator efficiency is decreased. Moreover, BW of the linear amplifier in HSA needs to be increased. It can be done by process scaling unless there is no breakdown limitation. However, linear amplifier has to have high gain up to

maximum supply voltage condition over 3V. So, device dimension should be reduced for wideband operation which causes higher switching frequency of the switching amplifier and thus results in further efficiency degradation.
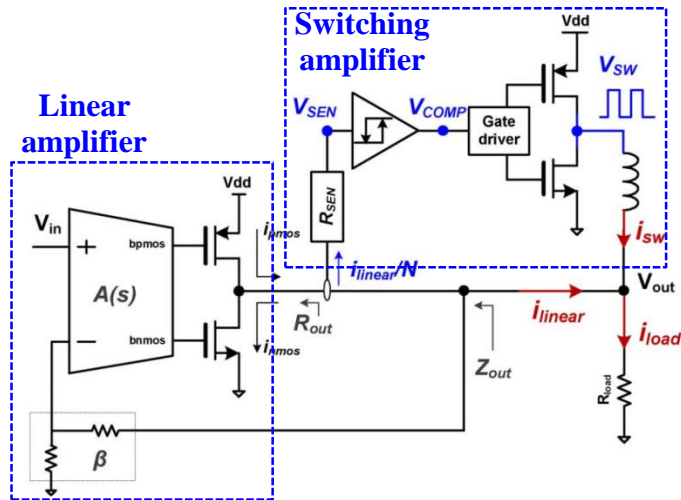
(a)
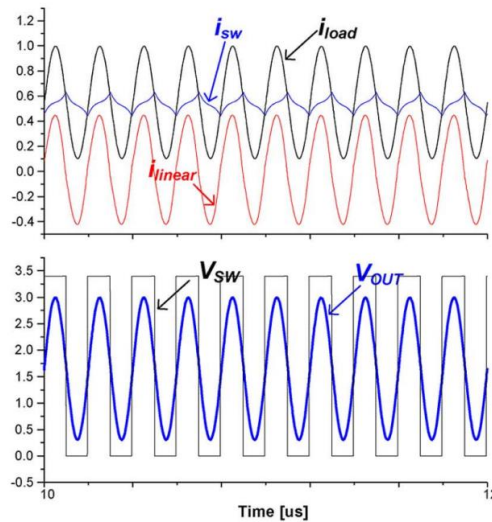
(b)

Figure 4.1 (a) Simplified block diagram and (b) operating waveforms of hybrid supply amplifier (HSA) for envelope tracking PA.
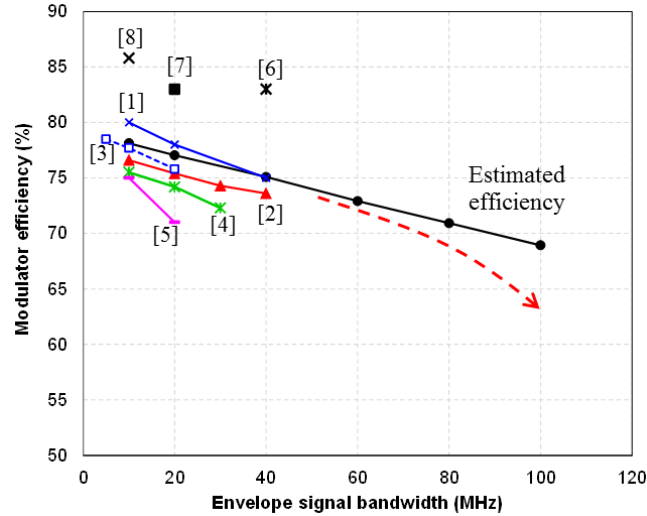
Figure 4.2 Simulated HSA efficiency over envelope signal bandwidth

Fig. 4.2 shows the simulated HSA efficiency as the signal BW is increased up to 100 MHz. There are two assumptions on the simulation. First, efficiency of the linear amplifier is maintained regardless of signal BW by process scaling. Second, switching frequency of the switching amplifier is 60 % of the envelope signal BW. Based on the simulated efficiency of HSA at 20 MHz LTE signal, efficiency of the linear amplifier and the switching amplifier are simulated as 30.4 % and 92.9 %, respectively. As the envelope signal BW is increased from 10 MHz to 100 MHz, efficiency of the supply modulator is degraded from 78.1 % to 68.9 %. In actual case, efficiency should be further degraded as the red dotted line in Fig. 4.2 due to the reasons as explained above.

On the other hand, less efficiency degradation is expected in the PDLM PA since most of the analog circuits are composed of low power and low voltage circuits. PWM signal generator, comparator and operational amplifier should have wide BW as well as low power consumption by process scaling. The RF switch and switch driver are the major power dissipation sources for wideband operation. So, efficiency of the PDLM PA is simulated according to the PWM frequency of 7, 10,

and 15 times the envelope signal BW. To simulate the power dissipation at the switch and its driver, inverters with the size of 4mm/1.6mm, 1mm/0.4mm, 0.32mm/0.16mm are used for driving 4mm RF switch. In case of driving 2mm RF switch, inverter size is reduced in half. For the comparison, ET PA efficiency is also plotted based on the ET PA efficiency at 10 MHz provided in [1] and modulator efficiency in Fig. 4.2.
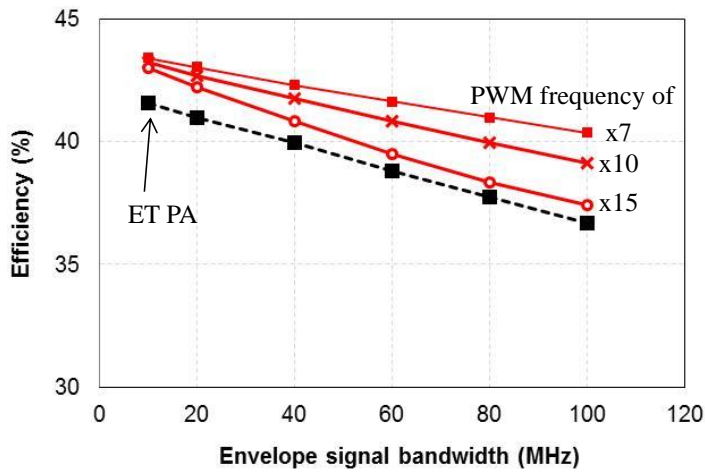
(a)
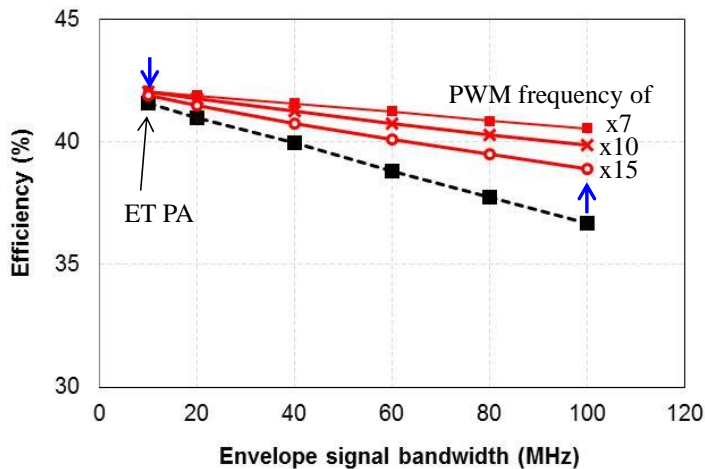
(b)

Figure 4.3 Estimated efficiency of the PDLM PA over envelope signal bandwidth, in case of (a) using original RF switch size and (b) reducing the switch size in half.

As shown in Fig. 4.3(a), efficiency is decreased further by increasing the PWM frequency. In case of PWM frequency of 15 times envelope BW, efficiency degradation of the PDLM PA is larger than that of the ET PA. However, device size of the RF switch is a design factor for best efficiency. By reducing the device size from 4 mm to 2 mm, switching loss is reduced in half and thus, the slope of efficiency degradation is greatly reduced. Due to the increased on-state resistance, simulation shows that efficiency of the PDLM PA is reduced from 43.4 % to 42.1 % at the envelope frequency of 10 MHz. In case of envelope frequency of 100 MHz, however, efficiency is increased from 37.4 % to 38.9 % at the PWM frequency of 15 times envelope signal BW. Depending on envelope signal BW of the application, device size of the RF switch can be selected for optimum efficiency of the PDLM PA.

4.2   Spectral noise reduction method

To determine pulse frequency (f_{PWM}), E-UTRA ACLR is simulated using 10MHz and 20 MHz LTE signals as a function of f_{PWM} in Fig. 4.4. As f_{PWM} is reduced below twice LTE signal bandwidth, severe ACLR degradation is observed as expected. To avoid the ACLR degradation, one needs to set f_{PWM} at more than 7-10 times the signal bandwidth. Then, large output spectral power is generated due to the PWM modulation of the envelope signal.

Fig. 4.5 shows the simulated spectrum of the PDLM PA when f_{PWM} is set at 100 MHz and 10 MHz LTE signal is applied. With the RF input signal at the center channel of Band-V frequency band (837MHz), the pulse tones appear at 837 ± n·100 MHz. Thus, the closes pulse tone is at 737 and 937 MHz, which are both outside the Tx passband (824 – 849 MHz) of Band-V duplexer filters. Since typical SAW filters provide out-of-band rejection higher than 35 dB at frequency offsets

beyond 20 MHz, the pulse tones generated by PDLM operation gets filtered out and the original signal is recovered by the post-PA duplexer filters. However, due to interferences among frequency spectrum and increasing needs for uplink carrier aggregation, stringent emission requirement makes duplexing filter have further attenuation at out-of-band spectrum.
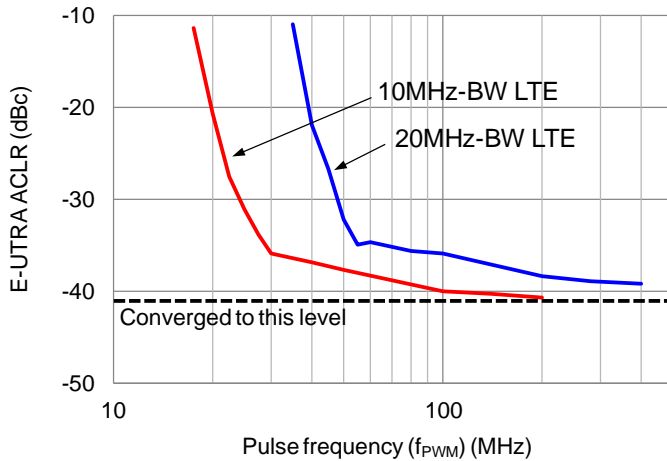

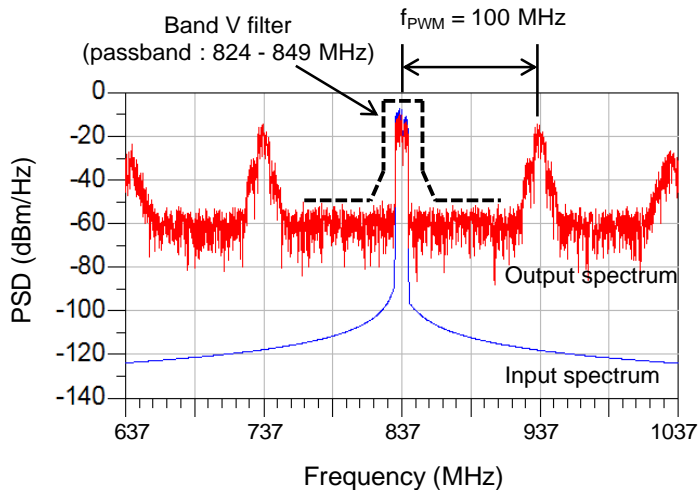Fig. 4.4. Simulated E-UTRA ACLR according to the pulse frequency for 10MHz- and 20MHz-BW LTE signal

Fig. 4.5. Simulated input and output spectrum of the PDLM PA.
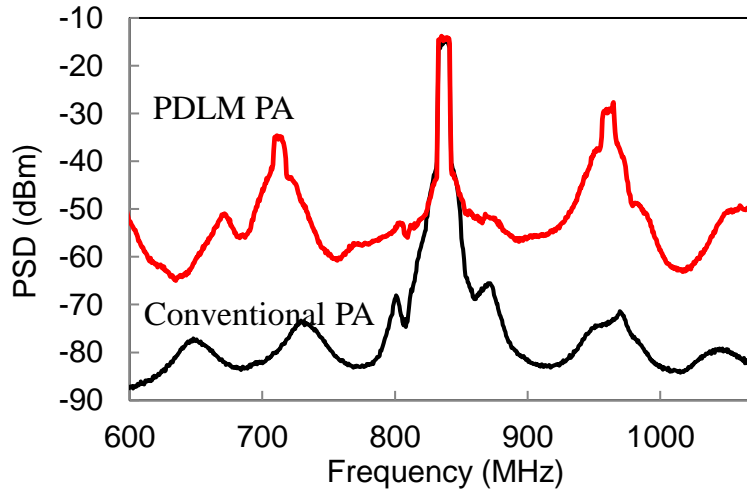
Figure 4.6 Measured output spectrum of the PDLM PA and conventional PA.

Fig. 4.6 is the output spectrum of the PDLM PA measured in front of the BPF. Compared to the conventional PA, the PDLM PA generates almost 20 dB higher spectral noise across the frequency range. Especially, at the frequency of $f_{RF} \pm n f_{PWM}$, high peaks of noise power is shown. BPF lower the level of the spectral power. However, out-of-band attenuation has trade-off relation with passband insertion loss. So, noise power reduction still needs to be endeavored. In this research, a simple PWM technique is used for easy implementation to demonstrate the proof-of-concept of the PDLM PA operation. To show the feasibility of reducing the output noise spectrum, random PWM technique [9] and sigma-delta modulation (SDM) technique [10] is simulated using matlab and is compared with original PWM technique.
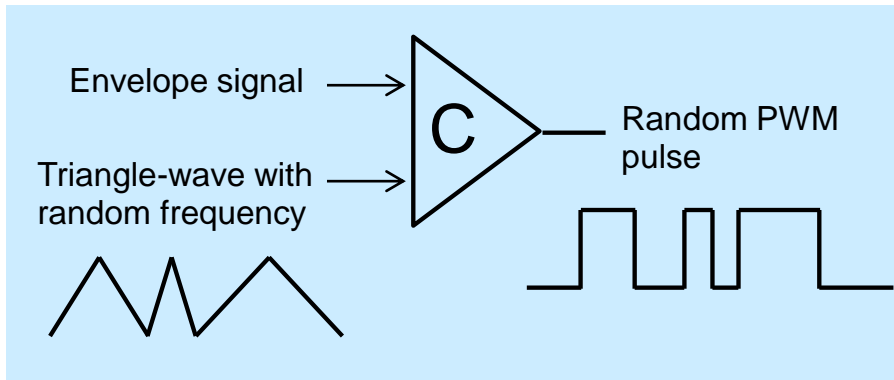
(a)
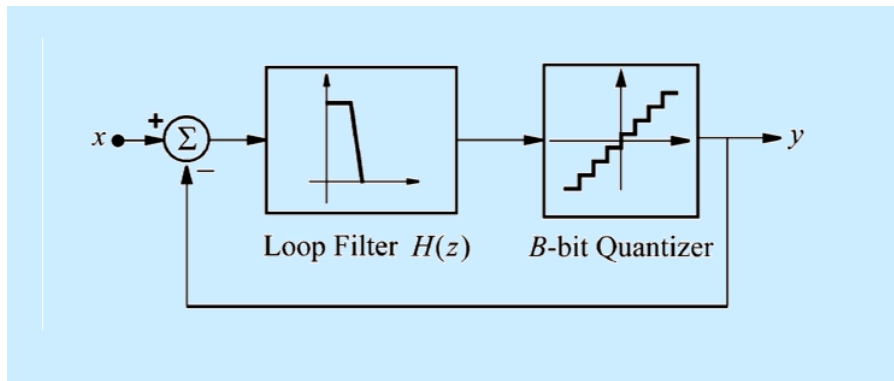
(b)

Figure 4.7 Conceptual block diagram of (a) random PWM technique and (b) SDM technique.

Fig. 4.7 shows the conceptual block diagram of each technique. Random PWM technique changes PWM pulse frequency randomly to spread out the noise power in wide frequency range while maintaining the duty ratio. It has similar switching frequency and ACLR performance to the original PWM technique. However, it has the disadvantage of the complicated circuit implementation.

SDM technique modulates envelope signal into the series of pulses by oversampling and noise shaping at the quantizer and loop filter, respectively. Since most of the circuits are composed of digital circuitry, it can be implemented in compact size. Thanks to the noise shaping, it shows good ACLR performance. However, higher switching frequency is required compared to the PWM technique.
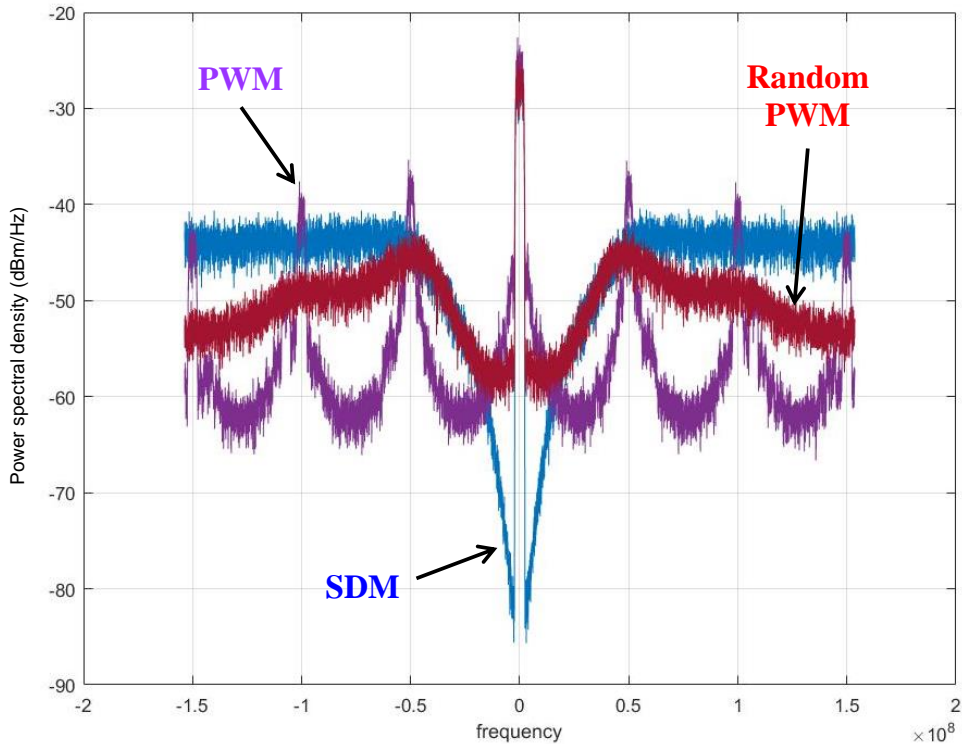
Figure 4.8 Simulated output spectrum according to the modulation technique.

Fig. 4.8 is simulated output spectrum of 3 modulation techniques using 5 MHz LTE signal. In case of the PWM technique, high spectral noise peaks exist similar to the measured one as shown in Fig. 4.4. On the other hand, the random PWM offers the reduction of the spectral peaks whereas the overall noise power is rather increased. In case of the SDM technique, noise power adjacent to the envelope signal frequency is greatly reduced by noise shaping. However, out-of-band spectral noise is higher than that of the random PWM technique.

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Chapter 5

Conclusions

5.1   Research Summary

In this Dissertation, a PDLM PA concept is proposed to enhance PA efficiencies in the back-off power levels without using a supply modulator. PDLM concept combines dynamic load switching with Class-S PA concept to operate the PA's near optimum efficiencies in the top ~5 dB power region, which results in the overall PAE improvement for high-PAPR signals such as LTE signals. The proposed concept is realized with low-power control circuits unlike envelope tracking, which requires high-power circuits such as dc-dc converters and linear amplifiers. Hence, the overall PA efficiency does not degrade rapidly as the signal bandwidth increases. By increasing the speed of the control circuits such as PWM signal generator, PDLM PA can potentially handle LTE signals wider than 20 MHz with minimal degradation of the overall efficiencies.

The proof-of-concept experiment has been performed in this work by designing a two-stage PA with switchable load matching using SOI CMOS process. The triple-

stacked CMOS FETs are used for both driver and power stages. The PWM generator and switch driver circuit are designed and fabricated using the same SOI CMOS process on separate chips. Both chips are mounted on a PCB, where the load matching circuit is also realized, for characterization using both CW and LTE signals. Overall CW PAEs higher than 44% are achieved over >6 dB-power back-off range from 23.2 to 29.5 dBm. By extracting a shaping table that sets the proper relationship between the RF input power with the duty cycle of the PWM pulses, a linear PA operation has been demonstrated. LTE tests have shown that the PDLM PA of this work can maintain the overall PA efficiencies around 43.4% with minimal PAE degradation as the LTE signal bandwidth increases from 5 to 20 MHz. Wider-bandwidth LTE operation can be achieved using more sophisticated pulse width modulation techniques and by increasing the speed of the control circuits.

The effect of non-ideal terminations at the intrinsic drain terminal has also been analyzed, showing the importance of eliminating the pulse tones for PDLM operation. The PDLM PA concept of this work can provide a potential solution for high-efficiency PAs for the future mobile terminals using wideband modulation signals.

5.2   Future Works

As discussed in Chapter 4, further investigation for wideband operation and output spectral noise reduction is required. It may be one solution to increase load switching states. By adopting multi-bit PWM, pulse frequency is going to be lowered to modulate the envelope signal. Then, efficiency degradation due to high speed switching for wideband operation is likely to be mitigated. Also, output spectral noise can be further improved due to the reduced quantization noise. Even

though complex design and analysis procedures are required, the approach makes the PDLM PA to further fit to the future transceiver system providing high efficiency and wideband operation.

초 록

배터리 시간 연장과 열 소모 특성을 개선하기 위하여, 3G/4G 모바일 송신기는 더 높은 효율을 가지는 전력증폭기 (PA) 를 요구하고 있다. 더군다나, 변조신호의 대역폭이 증가되고, 그 변조기법 또한 복잡해짐에 따라, 변조신호의 최고-평균 출력비 (PAPR) 가 증가하게 된다. 이로인한 선형성 확보를 위해서는 PA가 더 낮은 출력 전력에서 동작하여야 한다. 따라서, 더 낮은 출력에서도 높은 효율을 얻을 수 있는 PA의 개발이 필요하다.

본 연구에서는, 이 문제를 개선하기 위해서 동적 부하 변조 (DLM) 기술을 연구하였다. 이 기술은 변조신호의 크기에 따라서 부하 임피던스를 바꾸어 줌으로써 효율을 증가시키는 방법이다. 이는 크게 연속변조 DLM PA와 분리변조 DLM PA로 구분할 수 있다. 첫번째 구조는 varactor를 이용하여 부하 임피던스를 연속적으로 바꾸어줌으로써 큰 효율개선을 얻는 방식이다. 그러나, varactor의 집적이 어렵고, 연속된 이득과 위상의 변화로 인해 좋은 선형성을 얻기 어렵다는 단점이 있다. 두번째 구조는 RF 스위치를 이용하여 부하 임피던스를 스위칭하는 방식이다. switch 집적이 가능하고 선형성 개선이 상대적으로 쉽기 때문에 휴대용 응용에 더 적합한 구조라고 할 수 있다. 하지만 PA가 항상 최적의 효율로 동작하지는 않기 때문에 효율 개선량에 한계가 존재한다.

이러한 이전 DLM 기술의 문제점을 극복하기 위해서, 새로운 방식의 DLM 즉, 펄스에 의한 동적 부하 변조 (PDLM) 기술이 새롭게 제안되었다. 제안된 방식은 Class-S PA 개념과 DLM PA 개념을 결합하여, 분리변조 DLM PA의 장점을 유지하면서도 높은 효율을 얻을 수 있게 된다. 간소화된 등가모델을 이용하여 이론적인 분석을 하였고, 시뮬레이션과 거의 일치하는 결과를 얻었다. 이 새로운 개념을 검증하기

위해서 0.32μm SOI CMOS 공정을 이용하여 837 MHz 에서 동작하는 시제품 모듈을 제작하였다. 큰 PAPR 를 가지는 LTE 신호를 이용하여 실험한 결과, 넓은 출력 영역에서 높은 효율 개선을 얻을 수 있었다.

새롭게 제안된 PDLM PA 로 인한 몇가지 문제점에 대해서도 논의하였다. 펄스 주파수 성분에 대한 불완전한 임피던스 처리로 인한 영향을 시뮬레이션과 측정을 통해 분석하였다. 또한, 펄스 변조로 인해 발생되는 출력 잡음을 감소시키는 방법에 대한 시뮬레이션도 수행하였다.

제안된 PA는 현재 효율 개선을 위해 가장 많이 사용되고 있는 포락선 추적 (ET) PA 와 비교되었다. ET PA는 대신호 회로인 전력 변조기 (supply modulator) 를 사용하기 때문에 넓은 대역폭의 신호를 효율적으로 증폭시키는데 한계가 존재한다. 반면에, 제안된 방식은 저전력 소신호 회로들로 구성되기 때문에 신호의 대역폭이 넓어지더라도 동작의 한계가 줄어들게 된다.

따라서, 제안된 PDLM PA 구조는 넓은 대역폭과 큰 PAPR을 가지는 신호를 증폭하여야 하는 미래 휴대용 기기에 적합한 새로운 해결책이라 할 수 있겠다.

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