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Density-of-States and Stability Analysis of Solution-Processed InGaZnO TFTs with Consideration of Back Channel Surface Potential and Debye Length

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박막트랜지스터의 뒷 채널 전위 및 드바이
길이를 고려한 결함구조밀도와 신뢰성에 대한
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전기·컴퓨터 공학부

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이 논문을 공학박사학위논문으로 제출함

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Abstract

Density-of-States and Stability Analysis of Solution-Processed InGaZnO TFTs with Consideration of Back Channel Surface Potential and Debye Length

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Amorphous metal oxide-based thin film transistors (TFTs) have attracted much attention as a most promising candidate for next generation electronic applications. Especially, amorphous indium gallium zinc oxide (IGZO) TFTs are expected to replace conventional silicon-based TFTs which encounter the limitation of electrical properties such as field-effect mobility, uniformity, and process temperature. In addition, there have been many efforts to fabricate IGZO TFTs using solution process to reduce process cost. However, device physics of solution-processed IGZO TFTs still needs to be investigated for further application. Furthermore, the

effect of back channel surface region has been neglected in the analysis of IGZO TFTs. However, the back channel surface effect cannot be ignored when IGZO active layer is very thin, so that channel properties are affected by back channel surface. Therefore, the back channel surface effect needs to be considered in the analysis of solution-processed IGZO TFTs because solution-processed IGZO TFTs generally have very thin active layer, approximately 10~20 nm. In this thesis, device physical properties such as density-of-states (DOS) and reliability under bias stress of solution-processed IGZO TFTs are investigated with consideration of back channel surface potential and Debye length.

First, the extraction model is developed to extract accurate DOS of solution-processed IGZO TFTs. In most previously reported DOS extraction methods, back channel surface potential (Φ_B) was assumed to be zero. This assumption is appropriate when active layer is sufficiently thick to screen the effect of the applied gate voltage (V_{GS}) on Φ_B. On the contrary, Φ_B is affected by V_{GS} when active layer is thinner than Debye length. The assumption needs to be modified in the case of solution-processed IGZO TFTs, whose active layer is approximately 10 nm. Therefore, previously reported extraction method, which assumed zero potential at back channel surface, needs to be modified with consideration of Φ_B for accurate DOS extraction. The variation of Φ_B with V_{GS} was measured by scanning Kelvin probe microscopy (SKPM) and modeled to be used for modification of conventional field-effect method. The modified field-effect method considering Φ_B exhibited more

consistent activation energy (E_a) extraction result with the measured data than conventional one. Accurate DOS of solution-processed IGZO TFTs was extracted with considering Φ_B while conventional one underestimated the defect DOS.

Second, the effect of process and device parameters on DOS was investigated with varying annealing temperature (T_a), metallic composition ratio or IGZO active layer thickness (t_{active}). The DOS of each device was extracted by the developed model. The electrical characteristics variation along with various process parameters has been analyzed in the aspect of material chemistry. However, the effect of those parameters on the electrical model such as DOS has not been studied yet. The electrical modeling such as DOS variation is required to simulate device operation accurately as process parameters change. As T_a and metallic composition ratio changed, the relatively deep and tail states of DOS were changed. By comparing the extracted DOS with x-ray photoelectron spectroscopy (XPS) results, it is found that relatively deep and tail states are related to oxygen vacancy and residual hydroxide in solution-processed IGZO film, respectively. It was also found that physical defects, such as pin-holes, and disorder affected tail states from the extracted DOS analysis of solution-processed IGZO TFTs with various t_{active}. From the DOS analysis, DOS map of solution-processed IGZO TFTs, which shows origins of relatively deep and tail states, is developed.

Finally, the stability of solution-processed IGZO TFTs under constant gate bias stress is investigated. Under positive gate bias stress, the transfer

characteristics of solution-processed IGZO TFTs were positively shifted and showed similar behavior compared to vacuum-processed IGZO TFTs. However, different behavior of threshold voltage shift (ΔV_{th}) was observed under negative gate bias stress. The time evolution of ΔV_{th} followed linear function. In order to analyze the reliability under negative gate bias stress, the stability of devices with different t_{active} and Debye length of IGZO layer was measured and the effect of adsorbed charged species on the electrical characteristics was simulated by 2-dimensional technology computer-aided design simulation. As a result, it is found that linear shift of V_{th} under negative gate bias stress is attributed to the adsorption of positively charged species on back channel surface region.

Keywords: thin film transistor, oxide semiconductor, density of states, gate bias stress, solution process

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Chapter 1 Introduction

1.1 Recent Flat Panel Display

The applications of electronic displays have been extended to various electronic products such as smart watch, mobile phone, tablet, laptop computer, digital camera, monitor, large area television, and so on. The flat panel display is the main stream of recent electronic display market over the cathode ray tube (CRT), because it is enable to fabricate light-weight and thin display as shown in Figure 1.1 [1]. The flat panel display using active matrix shows superior performances. Because active matrix type displays, such as active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) display, use thin film transistors (TFTs) as switching device in each pixel, the operation of each pixel can be controlled

independently, resulting in achievement of high resolution, high contrast ratio, and full color display.

The electrical performances and reliability of TFTs are essential issues for active matrix display since the carrier mobility and threshold voltage of TFTs can directly affect the operation of active matrix display. For example, the display signal is applied to each pixel through operation of switching TFT. If the threshold voltage, and thus the on/off operation of switching TFT is not stable, pixels do not receive the signal at the right moment. The importance of the electrical performances of TFTs is increased as the size and resolution of display are increased, because electrical signal needs to be stored in pixel capacitor through switching TFTs in shorter time in large and high resolution displays. On the other hand, the role of TFT is not only switching element in AMOLED. In AMOLED, driving TFTs are required to supply current to OLED. Therefore, if the electrical properties such as mobility and threshold voltage of the driving TFTs are changed, it is hard to obtain proper image in AMOLED.

In general, the electrical performance and stability of TFTs are affected by material of semiconductor layer. Usually, hydrogenated amorphous silicon (a-Si:H) has been used for the active layer of switching TFTs in AMLCD. Since a-Si:H can be deposited on large area at low process temperature [2-3], a-Si:H TFTs are suitable for large area display. However, a-Si:H TFTs have several issues of low carrier mobility of under 0.5 $cm^2/V \cdot s$ and reliability under bias and

illumination stress [4-5]. Because a silicon bonding of a-Si:H TFTs has many disorder, different from crystalline silicon, electron transport is impeded by trapping sites, resulting in low carrier mobility [6]. On the other hand, the threshold voltage of a-Si:H TFTs is significantly changed under positive or negative bias stress through charge trapping [7] or defect creation [8-10]. In charge trapping mechanism, the threshold voltage is shifted without change of subthreshold swing (*S.S.*) and the charge trapping in the silicon nitride (SiN_x) gate insulator is responsible for threshold voltage shift of a-Si:H TFTs [7]. On the other hand, the slope of transfer curve is changed when defect creation is dominant mechanism of threshold voltage instability of a-Si:H TFTs [8-10]. The defect creation originates from the breaking of weak Si-Si bond by hydrogen diffusion in a-Si:H layer. To overcome the limits of a-Si:H TFTs, polycrystalline silicon (poly-Si) TFTs have been investigated. The poly-Si TFTs were fabricated by applying excimer laser annealing (ELA) to a-Si film to form locally crystalline silicon [11-12]. Since poly-Si TFTs have crystalline phase in grain boundary, superior electrical performance such as mobility of 30~500 $cm^2/V{\cdot}s$ can be achieved [13]. However, poly-Si TFTs have issues to use in large area display because there is non-uniformity between grains. Since the non-uniformity of grain boundary induces the non-uniformity electrical properties of TFTs, it is difficult to obtain uniform luminance characteristics in AMOLED display panel [14-15]. The additional pixel component and circuit are required to compensate the variance of electrical characteristics of TFTs for

obtaining uniform image [16-18]. Therefore, it is required to investigate other semiconductor materials to simultaneously achieve large area and high resolution display.

Recently, metal-oxide semiconductor TFTs, such as indium gallium zinc oxide (IGZO) TFTs, have attracted much attention because it can exhibit good electrical performance such as high electron mobility of ~10 $cm^2/V \cdot s$ even in amorphous phase [19-26]. Since the electrons are transported through spherical shaped s orbital of metal cation, amorphous metal-oxide semiconductor can achieve good electrical properties [27]. Furthermore, transparent display, which is one of the next generation display, can be developed by using amorphous metal-oxide semiconductor TFTs because of its large band gap of ~3.1 eV [28-29]. From these many advantages of oxide TFTs, display technology based on oxide TFTs have been widely investigated as shown in Figure 1.2. Although the commercial products using oxide TFTs are available in the market, it is required to investigate the device physics and degradation mechanism of oxide semiconductor TFTs for further application.

Figure 1.1 Evolution of display technology.

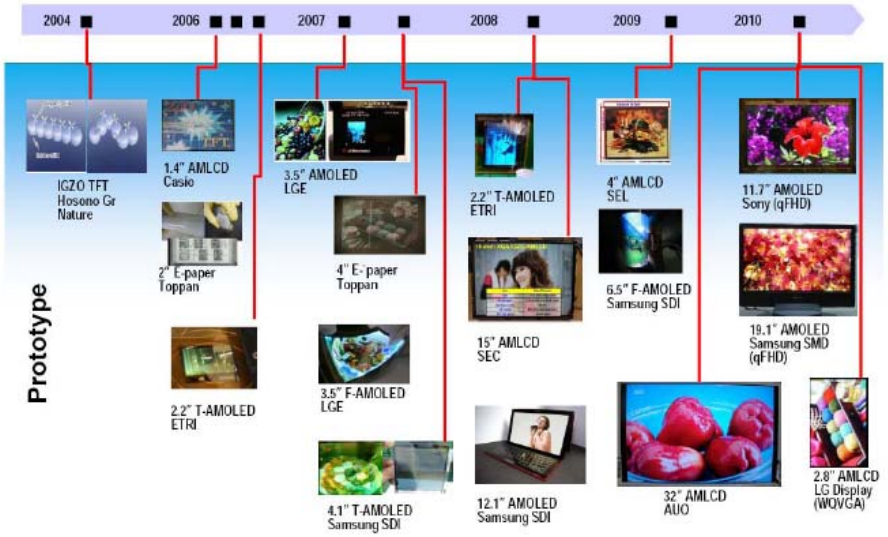


Figure 1.2 Progress of metal-oxide semiconductor TFT technology (Ref. Displaybank).

1.2 Dissertation Organization

The purpose of this thesis is investigation of the development of density-of-states (DOS) extraction model, analysis of DOS with various process parameters based on developed extraction model, and bias reliability study of solution-processed IGZO TFTs with consideration of back channel surface potential and Debye length.

The brief introduction of IGZO TFTs is given in Chapter 2. The various extraction methods of DOS, the effect of process parameters on the electrical characteristics, and the reliability of IGZO TFTs are reviewed.

In Chapter 3, the modified field-effect method to extract accurate DOS of solution-processed IGZO TFTs is developed with consideration of back channel surface potential (Φ_B). The effect of the applied gate voltage (V_{GS}) on the Φ_B is measured by scanning Kelvin probe microscopy. The Φ_B is modeled as a function of V_{GS} based on the measured result and the conventional field-effect method is modified by using the model of Φ_B. The DOS of solution-processed IGZO TFTs is extracted accurately by the modified field-effect method with consideration of Φ_B.

In Chapter 4, the developed DOS extraction model applies to the investigation of the effect of process and device parameters on DOS variation of solution-processed IGZO TFTs. Solution-processed IGZO TFTs with different annealing temperature (T_a), metallic composition

ratio, and thickness of active layer (t_{active}) are fabricated and DOS of each device is extracted by the developed method. By comparing the extracted DOS with the film properties, the origin of deep and tail states of DOS is investigated and DOS map is developed.

In Chapter 5, the stability of solution-processed IGZO TFTs under constant gate bias stress is studied by considering the back channel surface effect. The threshold voltage shift (ΔV_{th}) is similar with vacuum-processed IGZO TFTs under positive gate bias stress, while ΔV_{th} under negative gate bias stress shows different behavior compared to previous results. The degradation mechanism is studied by relating to the adsorption of positively charged species at back channel surface to explain the different behavior.

Finally, the summary of the thesis is described in Chapter 6.

Chapter 2 Review of IGZO TFTs

Recently, metal-oxide semiconductor thin film transistors (TFTs) have been widely investigated to develop next generation large-size displays with high performance. Amorphous indium gallium zinc oxide (a-IGZO) TFTs are considered as one of the promising candidates, and thus are extensively studied due to its relatively good electrical properties such as high electron field-effect mobility, low subthreshold swing and low leakage current, good uniformity and process compatibility in a mass production line.

In this chapter, the review of current issues of IGZO TFTs, such as the DOS extraction method, electrical characteristics, and reliability, is introduced.

2.1 Oxide Semiconductor for TFT Application

Metal-oxide semiconductor in polycrystalline phase, for example, In_2O_3, ZnO, and $SnO_2In_2O_3$ have been introduced for the transparent conductive oxides (TCOs) for solar cells. The TFTs using metal-oxide based semiconductor have been intensively studied as a candidate of the essential elements for high resolution and large size display from early 2000s. Compared to the hydrogenated amorphous silicon (a-Si:H) TFTs, metal-oxide semiconductor TFTs exhibit better electrical performance. For example, ZnO TFTs deposited at room temperature showed high electron mobility of ~20 $cm^2/V{\cdot}s$ [30]. In addition, metal-oxide based semiconductors have higher electrical conductivity compared to a-Si:H because of oxygen vacancy, cation interstitial, and substitutional/interstitial hydrogen, acting as shallow donors [31]. However, it is difficult to use ZnO as active layer of TFTs because of uniformity issue caused by polycrystalline phase.

In 2004, Nomura et al. reported amorphous IGZO TFTs with high electron mobility of ~8.3 $cm^2/V{\cdot}s$ and low off current [27]. IGZO TFTs exhibit high field-effect mobility in amorphous phase unlike silicon based transistors due to the electronic orbital structure of IGZO TFTs. As shown in Figure 2.1, electron transport path of IGZO TFTs is formed by direct overlap between s orbitals of metal cations. Specifically, the conduction band of IGZO TFTs is formed by the overlap of In 5s orbitals. Because In 5s orbital has spherical symmetric structure, the conduction path is not sensitive to

structural disorder, resulting in high electron mobility even in amorphous phase. The properties of TFTs using various semiconductor material are summarized in Table 2.1. Because metal-oxide based TFTs can achieve simultaneously high electrical characteristics and good uniformity as shown in Figure 2.2, amorphous metal-oxide semiconductor TFTs have been considered as a promising candidate for next generation display.

Solution-processed metal-oxide based TFTs have been also widely studied because solution process can reduce process cost with high throughput [32-34]. The previous reports of solution-processed metal-oxide TFTs have focused on the performance improvement [35-37] or the low temperature process to use flexible substrates [38-40]. The electrical performance was improved by changing materials or device structure [35-37]. The process temperature was lowered by using precursors, which can react at low temperature [38], adding components [39], or using deep ultraviolet to form oxide semiconductor layer [40].

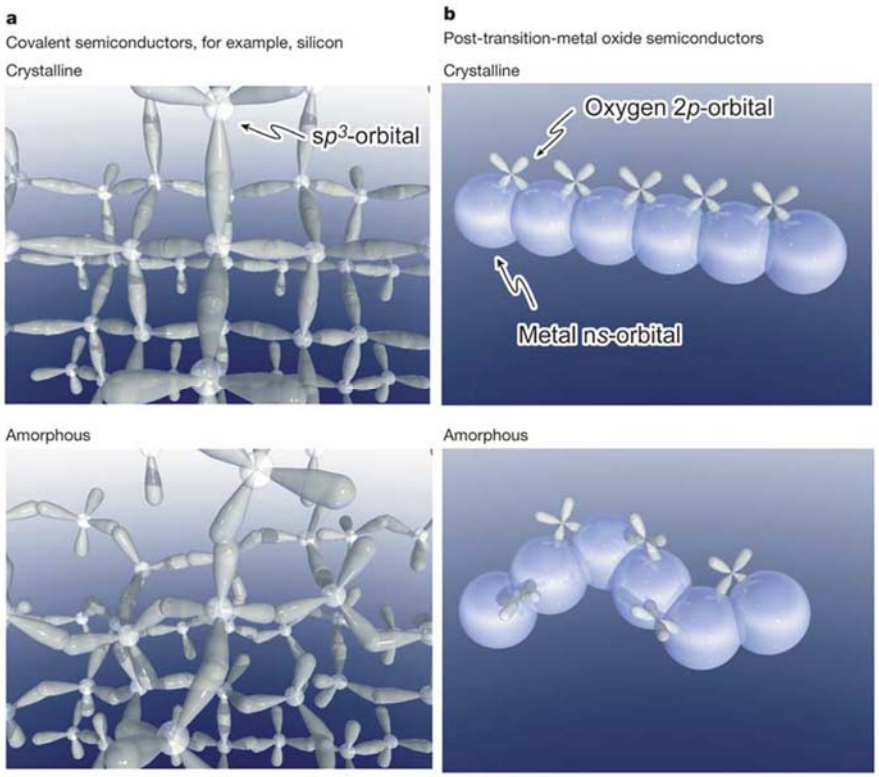


Figure 2.1 Schematic orbital structure of the conduction band minimum in crystalline and amorphous phase of Si and ionic metal-oxide semiconductor [27].

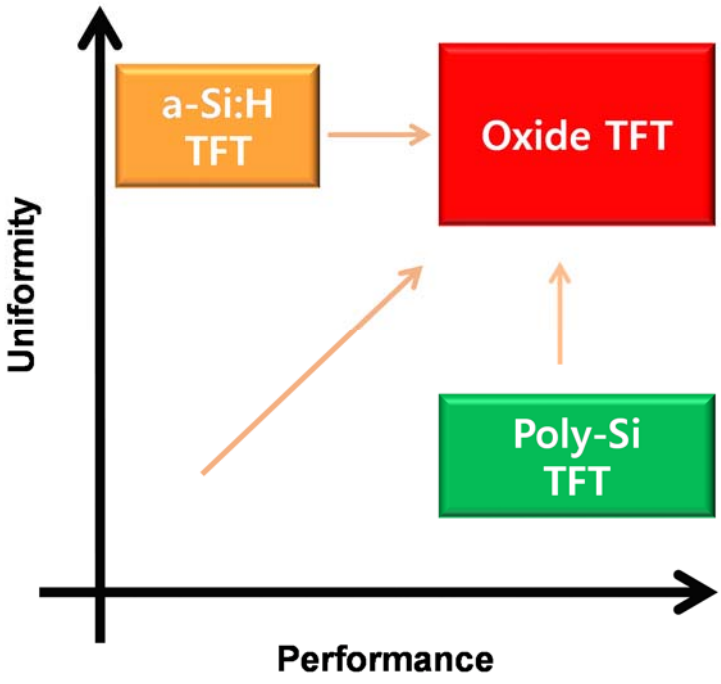


Figure 2.2 Comparison of uniformity and performance between a-Si:H, poly-Si, and oxide TFTs.

Table 2.1 Comparison of various semiconductor material TFTs

	a-Si TFT	Poly-Si TFT (ELA)	nc-Si TFT	Metal-Oxide based TFT
Mobility ($cm^2/V \cdot s$)	0.4~0.8	30~400	0.5~250	5~100
Uniformity	Good	Medium	Good	Med-Good
Stability	Bad	Good	Good	Good
TFT type	NMOS	CMOS	CMOS	NMOS
Technology maturity	High	High	Not yet	Medium

2.2 Various Extraction Methods of Density-of-States of TFTs

In general, different from crystalline silicon based devices, amorphous semiconductor based TFTs have a lot of defect states attributed to structural disorder and dangling bond in bad gap region. The electrical characteristics of amorphous semiconductor based TFTs are crucially affected by density-of-states (DOS) profile in band gap. From the early stage of research for amorphous semiconductor based TFTs, the extraction and modeling of DOS have been a key issue to characterize the device properties.

The DOS of metal-oxide based TFTs has been extracted and analyzed by many groups as summarized in Figure 2.3. One of the extraction method is using capacitance-voltage (C-V) characteristics [41-43]. The general process of DOS extraction using C-V characteristics is started from the semiconductor capacitance (C_S) as following equation,

$$C_s = C_{ins}C_{tot}/\left(C_{ins} - C_{tot}\right), \tag{2.1}$$

where C_{ins} and C_{tot} are gate insulator and total capacitance, respectively. By zero Kelvin approximation, the induced charge can be derived as follow,

$$Q\left(\varphi_S\right) = \sqrt{2\varepsilon_s\varepsilon_0 q\int_0^{\varphi_S}\int_{E_F}^{E_F+qV} N\left(E\right)dE\,dV}\ , \tag{2.2}$$

$$Q(\varphi_S) = \int_0^{\varphi_S} C_S(V)dV\,, \tag{2.3}$$

where φ_S, ε_S, ε_0, q and E_F are the surface potential, relative dielectric constant of semiconductor, vacuum permittivity, electronic charge and Fermi level, respectively. By equating equation (2.2) and (2.3), the following equation can be obtained.

$$N(E_F + q\varphi_S) = \frac{1}{q^2\varepsilon_S\varepsilon_0}\left[C_S(\varphi_S)^2 + (dC_S(\varphi_S)/d\varphi_S)\int_0^{\varphi_S} C_S(V)dV\right] \tag{2.4}$$

The φ_S can be obtained as following equation,

$$\varphi_S = \int_{V_{FB}}^{V_{GS}}\left(1 - \frac{C}{C_{ins}}\right)dV_{GS}\,, \tag{2.5}$$

where V_{FB} and C are the flat band voltage and the measured capacitance in the C-V characteristics, respectively. By assuming zero Kelvin approximation and using equation (2.4) and (2.5), DOS can be extracted.

M. Kimura et al. used C-V measurement and numerical calculation to extract DOS of a-IGZO TFTs [41]. C-V characteristics was measured at very low frequency of 0.1 and 0.5 Hz. The surface electric field and potential were calculated by Gauss's law and equation (2.5). In order to obtain surface potential, the surface potential was calculated by Poisson's equation with the assumed DOS and backside potential until the calculated value was matched with the measured data obtained by C-V characteristics. As a result, they reported DOS distribution composed of tail and deep states. K. Jeon et al. used self-

consistent technique for extraction of DOS using optical response of C-V characteristics [42]. The trapped charges were excited to the conduction band by optical excitation and these excited charges were detected by C-V measurement. The extracted DOS was composed of two exponential functions and each peak value of tail and deep states were 1.2×10^{18} and 9.5×10^{16} $cm^{-3}eV^{-1}$, respectively. S. Lee et al. reported the extraction DOS using multifrequency C-V characteristics [43]. In this method, device was modeled with resistance and capacitance along vertical direction and C-V characteristics was measured as changing frequency from 100 Hz to 1 MHz. Different from optical response C-V characteristics method, nonlinear relation between V_{GS} and surface potential was calculated by frequency-independent C-V characteristics and Gauss's law at the interface between active layer and gate insulator. The final extracted DOS was composed of two exponential functions and maximum values of tail and deep states were 1.1×10^{17} and 4×10^{15} $cm^{-3}eV^{-1}$, respectively. In both methods using optical response and multifrequency C-V characteristics, the back channel surface effect was not considered and the back channel surface potential was assumed to be zero.

Other DOS extraction method is photo-excited charge-collection spectroscopy [44-45]. In this method, the light having different photon energy was illuminated to active layer. Since metal-oxide semiconductor TFTs are generally n-type transistor, the electrons trapped at subgap states are released to conduction band by photo-

excitation process. Consequently, the photo-shifted V_{th} is described as follow with zero Kelvin approximation,

$$V_{th}(\varepsilon) = \varphi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \psi_{S,max} + \frac{Q_G}{C_{ox}}, \quad (2.6)$$

$$Q_{eff}(\varepsilon) = q\int_{E_V}^{E_C-\varepsilon} D_{it}(E)dE - qN_b t_{ox}, \quad (2.7)$$

where ε, ϕ_{ms}, Q_{eff}, C_{ox}, $\psi_{s,max}$, Q_G, D_{it}, N_b, and t_{ox} are the photon energy, the metal-semiconductor work function difference, the effective trap charge, the dielectric capacitance per unit are, the potential due to band bending of the semiconductor, the charge associated with dielectric band bending induced by V_{GS}, the areal DOS at channel/dielectric interface, the density of bulk traps in gate dielectric, and the dielectric thickness, respectively. The areal DOS with respect to conduction band edge (E_C) can be determined as following equation.

$$D_{it}(E_C - \varepsilon) = \frac{C_{ox}}{q}\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} \quad (2.8)$$

Although the interface trap density can be obtained by this method, light absorption property of semiconductor layer can be limitation of this method. If the active layer is too thin to sufficiently absorb photon, the extracted DOS can be underestimated. In addition, the back channel surface potential was not considered, since this method focuses on the extraction of interface trap density.

Other approach for DOS extraction is field-effect method. In field-effect method, DOS can be extracted directly from current-voltage (I-V) characteristics. In field-effect method, there are some assumptions.

(1) The semiconductor layer is uniform in parallel and normal direction to the interface between active layer and gate insulator.

(2) The electric field and potential at back channel surface are zero.

(3) The effect of interfacial states on electric potential distribution in semiconductor layer is ignored.

(4) All electrons of semiconductor layer are trapped in the defect states.

Assumption (1) means the uniformity of active layer. When short range uniformity is sufficiently good, this assumption induces only small error. Assumption (2) is related to the back channel surface effect. When active layer is sufficiently thick, the applied electric field induced by V_{GS} cannot affect the back channel surface. However, when active layer become thinner than Debye length, the back channel surface potential can be varied by V_{GS} and this assumption needs to be modified. Assumption (3) means that the extraction result can be distorted if huge number of interfacial defect states exist since the field-effect method cannot extract separately interface and bulk states. However, the extracted result is still meaningful to understand device physics, since the distribution of the extracted DOS, which is sum of bulk and interface defect states gives physical meaning of the

effect of DOS on the device operation. Assumption (4) is zero Kelvin approximation.

The DOS extraction in field-effect method starts from the Poisson's equation,

$$\frac{d^2U(x)}{dx^2} = \frac{qn}{\varepsilon_S \varepsilon_0}, \tag{2.9}$$

where U, q, n, ε_S, and ε_0 are the electrostatic potential energy, the electronic charge, the charge density, the relative dielectric constant of semiconductor, and the permittivity of vacuum, respectively. The electric field in semiconductor layer can be described as follow.

$$\frac{dU(x)}{dx} = -\sqrt{\frac{2q}{\varepsilon_S \varepsilon_0}\int_0^U n(U)dU} \tag{2.10}$$

The field-effect conductance (G) can be obtained as follow.

$$G = G_0 \int \frac{\exp[qU(x)/kT]}{\sqrt{\frac{2q}{\varepsilon_S \varepsilon_0}\int_0^U n(U)dU}}, \tag{2.11}$$

where k is the Boltzmann constant. The boundary condition at interface between active layer and gate insulator can be described as,

$$\frac{dU(x)}{dx} = \frac{q\varepsilon_{ins}}{d_{ins}\varepsilon_S}\left(V_F - \frac{U_0}{q}\right), \tag{2.12}$$

where ε_{ins}, d_{ins}, V_F and U_0 are the relative dielectric constant of gate insulator, the thickness of gate insulator, the difference between V_{GS}

and flat band voltage (V_{FB}), and surface potential energy, respectively. By differentiating the derivative of equation (2.12) with respect to V_F, a following equation is obtained.

$$n(\varphi_S) = \varepsilon_{ins} \frac{\left[\exp(q\varphi_S / kT) - 1\right]}{d_{ins} d_S} \left(\frac{1}{G_0} \frac{dG}{dV_F} \right)^{-1}, \quad (2.13)$$

The DOS can be extracted by differentiating equation (2.13) with respect to surface potential energy. J. Jeong et al. and C. Chen et al. reported the DOS extraction of IGZO TFTs using field-effect method [46-47]. They used temperature-dependent characteristics and Meyer-Neldel rule to find the nonlinear relation between the movement of Fermi level (E_F) (and thus activation energy) and V_{GS}. The field-effect method combined with Meyer-Neldel rule has a strong point to evaluate the DOS in real device operation, while it has a weak point that device needs to exhibit temperature-dependent characteristics.

The other method of DOS extraction is simulation fitting method [48-49]. The calculation of the electrical characteristics of devices using computer simulation is possible with the improvement of computational capability. H. –H. Hsieh et al. and C. E. Kim et al. reported the DOS modeling of amorphous IGZO TFTs using 2-dimensional (2D) technology computer-aided design (TCAD) simulation (ATLAS, Silvaco). The simulated DOS was composed of exponential tail and Gaussian deep states. Several parameters such as DOS distribution, carrier mobility, and background carrier density

were varied in order to fit the simulated I-V curves to the measured transfer characteristics. This method has several weak points. First, it is time-consuming process and second, it is hard to obtain unique set of parameters including DOS distribution because there are too many fitting parameters.

Although each method has strong and weak points in DOS extraction, the effect of back channel surface, such as back channel surface potential, was not considered in DOS extraction process. The back channel surface potential is not included or assumed to be zero in previously reported DOS extraction methods. However, the back channel surface effect needs to be considered if active layer is very thin, so that V_{GS} can affect the back channel surface potential. In Chapter 3, the modified field-effect method is developed by considering the back channel surface potential to extract accurate DOS of solution-processed IGZO TFTs having very thin active layer. Although the field-effect method is thought to be direct and believable method, conventional field-effect method needs to be modified for accurate DOS extraction of thin active layer. The back channel surface potential was measured directly by scanning Kelvin probe microscopy (SKPM) and modeled to apply modification of field-effect method.

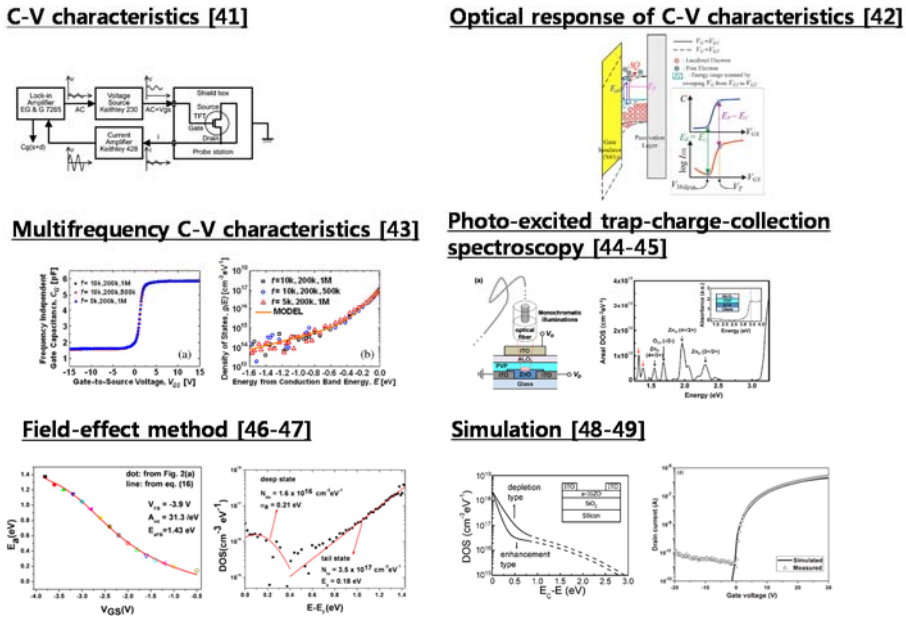


Figure 2.3 Various DOS extraction methods of metal-oxide TFTs [41-49].

2.3 Process Parameter Variation of IGZO TFTs

The effects of process parameter such as annealing temperature (T_a), metallic composition ratio, and thickness of active layer (t_{active}) on the electrical characteristics of IGZO TFTs have been widely investigated to find optimal process condition. Especially, the electrical properties of solution-processed IGZO TFTs based on sol-gel process is seriously affected by T_a. In sol-gel process, metal-oxide structure is formed by reaction between precursor and water molecule and this reaction is dominantly affected by thermal energy supplied during annealing process [50]. Therefore, the properties of film and device based on solution-processed metal-oxide semiconductor are varied by T_a. The film properties and electrical characteristics of solution-processed IGZO TFTs annealed at different temperature have been reported by many groups [32, 51-57]. First, the crystallinity of solution-processed IGZO film is affected by T_a. At high T_a, the crystallinity of solution-processed IGZO film starts to be changed from amorphous to nanocrystalline phase and the critical annealing temperature, at which crystallization is occurred, is affected by composition ratio and precursor used in IGZO film [32, 52]. Second, the electrical properties including field-effect mobility (μ_{FE}) and turn-on voltage (V_{on}) are affected by T_a and the previous studies reported similar effect of T_a on the electrical characteristics of solution-processed IGZO TFTs. As T_a increases, V_{on} and threshold voltage (V_{th}) are negatively shifted and μ_{FE} is increased. This result was investigated based on chemical bonding variation of

solution-processed IGZO film [54]. As mentioned above, sufficient thermal energy is required for complete reaction between metal ligands and water molecules. When T_a increases, residues due to incomplete reaction are reduced and the amount of oxygen vacancy is increased. The oxygen vacancy formation is closely related to carrier generation as following equation [54].

$$O_O^x = \frac{1}{2} O_{2(g)} + V_O^{\bullet\bullet} + 2e^-, \quad (2.14)$$

Therefore, larger carrier density is induced at higher T_a. Consequently, V_{on} is negatively shifted as T_a increases, because larger negative bias is required to fully deplete the channel having larger carrier density [58]. Higher μ_{FE} can be also explained by chemical bonding variation, because μ_{FE} can be enhanced by larger carrier density [59-61]. Although chemical bonding variation due to different T_a can explain carrier density, V_{on}, and μ_{FE} variation, the relation between T_a (and thus chemical bonding variation) and electrical model parameters such as DOS has not been investigated yet. However, electrical modeling of chemical bonding variation is required to accurately simulate device characteristics and effectively optimize fabrication process.

The effect of metallic composition ratio of IGZO TFTs has been also widely investigated. In vacuum-processed IGZO TFTs, the role of each metal component has been studied [27, 62]. Indium enhances μ_{FE} because the conduction path is formed by In 5s orbital. Gallium controls carrier density by suppressing formation of oxygen vacancy.

Zinc affects the subthreshold characteristics by modulation of shallow tail and interfacial states [27, 62]. The effect of metallic composition ratio on the electrical characteristics of solution-processed IGZO TFTs was also studied [34, 54, 63-64] and each component acts similar role compared to vacuum-processed IGZO TFTs. In addition, higher indium ratio decreases the grain size and the surface roughness of solution-processed nanocrystalline IGZO film because more indium oxide ions induce cubic stacking faults in IGZO film [63]. The solution-processed IGZO TFTs can be fabricated at lower T_a with higher gallium ratio, since gallium doping can decrease residual hydroxides and allows to achieve oxide-lattice structure at lower temperature [54]. In previous reports, the effects of composition ratio and role of each component have been investigated based on the relation between the change of chemical structure such as oxygen vacancy and the electrical characteristics. However, how metallic composition ratio can affect the defect DOS has not been analyzed yet. Because the DOS model based on the relation between metallic composition ratio, and thus chemical bonding, and defect profile is useful to effectively analyze and optimize device performance, it is required to develop electrical model related to chemical variation due to composition ratio.

On the other hand, the electrical characteristics is also affected by t_{active}. In vacuum-processed metal-oxide TFTs, V_{on} is negatively shifted as t_{active} increases because larger number of electrons need more negative voltage to turn off the device through full depletion [58]. In addition to

V_{on} variation, other electrical parameters such as μ_{FE} and subthreshold swing (*S.S.*) can be affected by t_{active} in solution-processed metal-oxide TFTs, while other properties except V_{on} are rarely affected in vacuum-processed ones [58, 65-67]. It is related to the film deposition process of solution process. Because vaporization of solvent is occurred during formation of thin film in solution process, physical defects such as pin-holes can be formed in the film. Furthermore, if t_{active} is controlled by multi-stacking process, there are many interface traps between each layer. Since these defects inhibit the electron transport by acting as trap sites, μ_{FE} and on current (I_{on}) are degraded as t_{active} increases [65-67].

As mentioned above, the effects of process condition such as T_a, composition ratio, and t_{active} on the electrical characteristics of solution-processed IGZO TFTs have been investigated based on the aspect of material chemistry. The relation between chemical variation of film and electrical model such as DOS has been rarely analyzed yet. However, analysis of this relation and development of electrical model as chemical and film property variation induced by process parameter variation are useful to effectively analyze and optimize the device characteristics. In Chapter 4, the DOS of solution-processed IGZO TFTs fabricated with different T_a, metallic composition ratio, and t_{active} is extracted by using the modified field-effect method developed in Chapter 3. By comparing the extracted DOS profile with the results of film analysis, the origins of each DOS component are analyzed by relating to chemical bonding or physical defects.

2.4 Reliability of IGZO TFTs

In practical circuit applications, TFTs are exposed to gate or drain bias stress. Although IGZO TFTs exhibit good electrical performance in initial states, the reliability issue needs to be investigated for practical application. In general, the V_{th} of IGZO TFTs is mainly degraded under constant gate bias stress. The V_{th} is positively and negatively shifted under positive and negative gate bias stress, respectively [68-71]. Furthermore, sometimes, transfer curves of IGZO TFTs show bidirectional shift with hump characteristics under positive gate bias stress [72-74]. Generally, the V_{th} instability of IGZO TFTs under gate bias stress has been explained by three mechanisms such as the charge trapping [68-69], the defect creation [70], and the ambient effect [71]. In the charge trapping mechanism, the V_{th} shift is attributed to the positive or negative charge trapping induced by gate bias stress at gate insulator and/or the interface between IGZO semiconductor and gate insulator layer. In general, the transfer curve is shifted with negligible change of subthreshold swing. In addition, the V_{th} shift (ΔV_{th}) can be described by logarithmic or stretched exponential function as follows [7, 68-69, 75],

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right), \tag{2.15}$$

$$\Delta V_{th} = \Delta V_{th0}\left\{1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}, \tag{2.16}$$

where r_0 is a decay rate constant; ΔV_{th0} is the ΔV_{th} at infinite time; τ is the characteristic trapping time; and β is the stretched exponential exponent. In the defect creation mechanism, the DOS in the band gap of the semiconductor layer is changed and subthreshold swing degradation is typically observed. In amorphous semiconductor based TFTs, the ΔV_{th} due to defect creation can be also described by stretched exponential function, equation (2.16) with different definition of each parameters [76]. In addition, because the effect of defect states on electrical characteristics is varied according to type of defects, the change of defect profile can be analyzed by 2D TCAD device simulation [74]. In the ambient effect mechanism, the oxygen or water molecules are attached or detached by the gate bias stress as shown in Figure 2.4. These molecules affect the carrier density of the active layer, resulting in the V_{th} shift. Different from the charge trapping and defect creation mechanism, the analytical model for ambient effect has not been investigated. The ambient effect can be suppressed by using a highly reliable passivation layer [71].

The introduced reliability analyses of IGZO TFTs under gate bias stress have been performed in the case of vacuum-processed devices. The stability of solution-processed IGZO TFTs has not been mainly studied. Though the reliability of solution-processed IGZO TFTs is poor than vacuum-processed ones and may be explained by the reported mechanisms based on vacuum-processed devices, there may be the differences originating from solution-based process.

Especially, solution-processed IGZO TFTs generally have very thin active layer compared to vacuum-processed devices, the back channel surface effect may need to be considered in analysis of stability. In Chapter 5, the reliability of solution-processed IGZO TFTs under constant gate bias stress is investigated with consideration of the reaction and effect of back channel surface region.

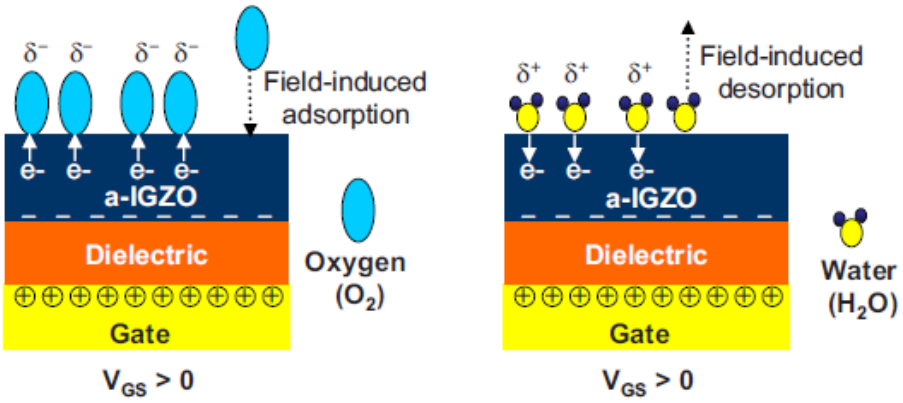


Figure 2.4 Schematic diagram of the electric field-induced adsorption of oxygen molecule from the ambient atmosphere under positive gate bias (left). Schematic diagram of the electric field-induced desorption of water molecule into the ambient atmosphere under positive gate bias (right) [71].

Chapter 3 Development of Modified Field-Effect Method with Consideration of Back Channel Surface Potential

3.1 Introduction

Nowadays, solution-processed IGZO TFTs have been widely studied. However, most studies on the solution-processed metal-oxide TFTs have focused on developing of materials, improving the electrical characteristics or lowering the process temperature. Although it is very important to investigate the device physics such as DOS distribution or contact property for the performance optimization, very few work regarding such topics has been reported for the solution-processed devices.

Among several physical properties, DOS analysis of interface and bulk traps is very helpful to optimize the fabrication process and corresponding device electrical characteristics. In the case of the vacuum-processed metal-oxide TFTs, many groups have conducted the extraction and analysis of the DOS by using capacitance-voltage (C-V) measurement [41], optical response C-V measurement [42], multi-frequency C-V characteristics [43], photo-excited trap-charge-collection spectroscopy [44-45], field-effect method [46-47], and ATLAS simulation fitting [48]. However, the analysis on DOS for the solution-processed metal-oxide TFTs has been rarely conducted. In addition, it is noted that the oxide semiconductor layer of the solution-processed devices is typically much thinner than that of the vacuum-processed ones, causing the back channel surface potential (Φ_B) of TFTs to vary with the applied gate bias. Since the aforementioned methods have not considered the Φ_B, it is not appropriate to use these methods as they are. It is required to consider appropriate boundary conditions at the back channel for more accurate analysis. Among those various methods, a field-effect method can easily adopt the modified boundary conditions into the extraction process because conductance and potential distribution along the semiconductor thickness direction are used during the extraction process. It is noted that the Φ_B is typically assumed to be zero in the conventional field-effect method, but it may not hold for the oxide TFTs with thin semiconductor layer, especially when the layer is thinner than its Debye length.

In this chapter, the modified field-effect method is developed by considering non-zero back channel surface potential. The Φ_B variation of the solution-processed a-IGZO TFTs for the applied gate voltage (V_{GS}) was measured and appropriately modeled by using a scanning Kelvin probe microscopy (SKPM) technique. The distribution of DOS was extracted by the modified field-effect method with consideration of the Φ_B, which showed a better agreement with the measured data.

3.2 Experiment

3.2.1 Fabrication of Solution-Processed IGZO TFTs

Precursor solution was prepared by dissolving of indium acetate [$In(C_2H_3O_2)_3$], gallium nitrate hydrate [$Ga(NO_3)_3 \cdot xH_2O$], and zinc acetate dehydrate [$Zn(CH_3COO)_2 \cdot 2H_2O$] into 2-methoxyethanol [$CH_3OCH_2CH_2OH$] with ethanolamine [$NH_2CH_2CH_2OH$] as stabilizer. Molar ratio of indium, gallium, and zinc was 3:1:2 and total molar concentration of solution was 0.137 M. The precursor solution was stirred at 55 ℃ for 1 hour and aged for 24 hours. The preparation process of precursor solution is summarized in Figure 3.1.

For fabrication of solution-processed IGZO TFTs, heavily doped p-type silicon with thermally grown silicon dioxide (SiO_2, 200 nm) were used as gate and gate insulator, respectively. Si/SiO_2 substrates were cleaned by ultrasonicator in acetone, isopropanol alcohol, and deionized water and treated by UV-ozone cleaner to improve adhesion property. IGZO semiconductor layer was deposited by spin-coating the prepared precursor solution through 0.45 μm membrane filter on substrates at a rotation speed of 4000 rpm for 30 s in the air. The IGZO film was baked at 200 ℃ for 10 min and patterned by conventional photolithography and wet etching process using diluted hydrochloric acid (hydrochloric acid : deionized water = 1 : 100). The IGZO film was annealed at 500 ℃ for 1 hour in the furnace under the ambient air condition. Aluminum electrodes (150 nm) were

deposited by thermal evaporation as source and drain (S/D) electrodes. The fabrication process of solution-processed IGZO TFTs was schematically shown in Figure 3.2 (a). The fabricated devices was annealed at 60 ℃ for 1 hour to improve uniformity. The schematic diagram and the information of each layer of the fabricated solution-processed IGZO TFTs are shown in Figure 3.2 (b) and Table 3.1, respectively.

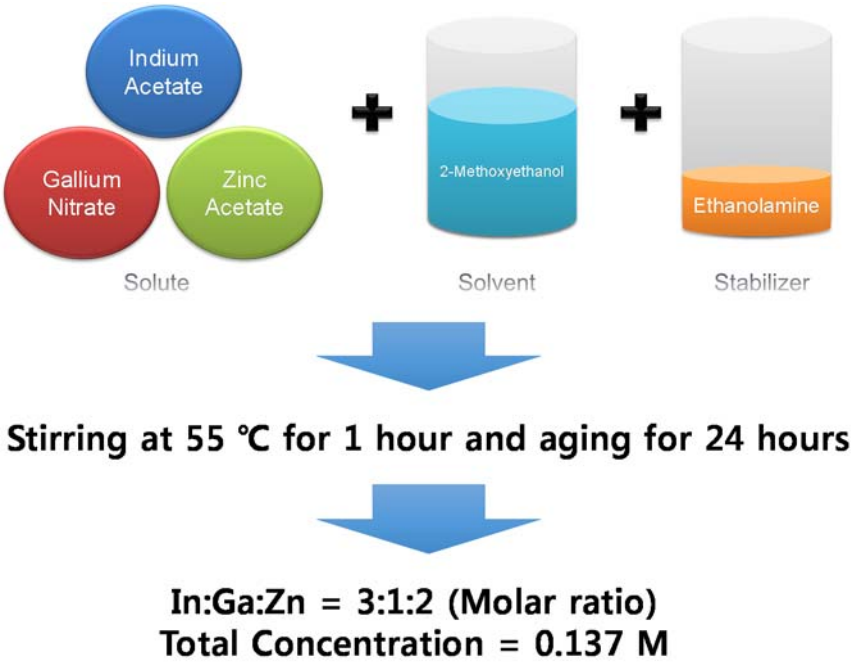
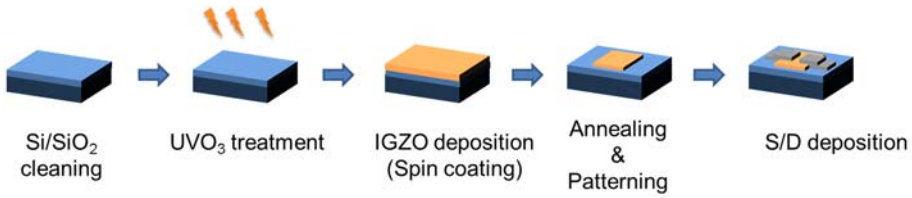
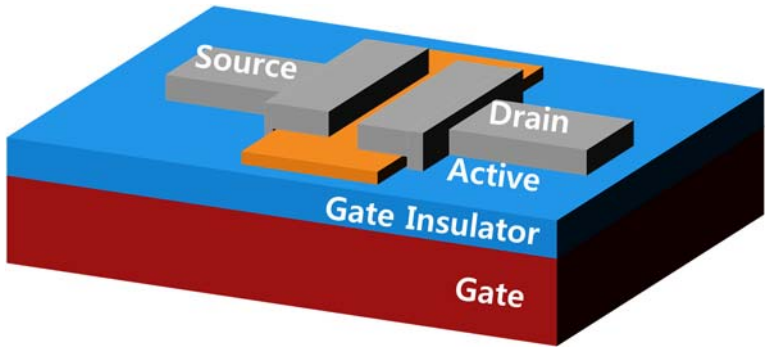


Figure 3.1 Schematic diagram of preparation of IGZO precursor solution.



(a)



(b)

Figure 3.2 Schematic diagram of (a) the fabrication process and (b) the fabricated device structure of solution-processed IGZO TFTs.

Table 3.1 Layer information of the fabricated solution-processed IGZO TFTs

Gate	**P^+ Si**
Gate Insulator	**SiO_2 (200 nm)**
Active	**IGZO (10 nm)**
Source/Drain	**Al (150 nm)**
Width/Length (W/L)	**1000 μm / 200 μm**

3.2.2 Device and IGZO Film Characterization

The current-voltage characteristics were measured by Agilent 4155C semiconductor analyzer in a dark ambient condition. The field-effect mobility (μ_{FE}) at a low drain voltage (V_{DS}) was extracted by $\mu_{FE} = Lg_m / WC_i V_{DS}$, where C_i is gate capacitance per unit area and g_m is transconductance. Threshold voltage (V_{th}) was defined by the V_{GS} at drain current (I_{DS}) of 10 nA and subthreshold swing (*S.S.*) was extracted by $S.S. = \left(d\log(I_{DS})/dV_{GS}\right)^{-1}$ of the range from 50 pA to 500 pA.

The thickness (d_{IGZO}) and relative dielectric constant of IGZO semiconductor layer were measured by ellipsometry (M-2000UI, J. A. Woollam Co., Inc.) in the wavelength range from 245 to 1690 nm. The thickness of semiconductor layer was confirmed by step measurement with atomic force microscopy (AFM). Carrier concentration was measured from Hall measurement using a van der Pauw structure.

3.2.3 Scanning Kelvin Probe Microscopy Measurement

The SKPM measurement was performed by AFM (XE-100, Park Systems) equipment and SR830 DSP dual phase lock-in amplifier (Stanford Research Systems, Inc.). In SKPM measurement, a resonance frequency of cantilever was 132 kHz and a modulation method was amplitude modulation. The device was attached onto a

printed circuit board and gate and S/D electrodes were connected with conductive disk or the patterned gold electrode. The SKPM was conducted in two steps. Firstly, topology of channel area was scanned by AFM mode and then cantilever (NSC14/Cr-Au, Park Systems) was moved to center of the channel. In SKPM mode, AC signal was applied to cantilever. Φ_B at the fixed position was measured for V_{GS} from -10 to 10 V under V_D=V_S=0 V. The schematic diagram of SKPM measurement is shown in Figure 3.3. All procedure of SKPM was conducted in a closed box in ambient air condition.

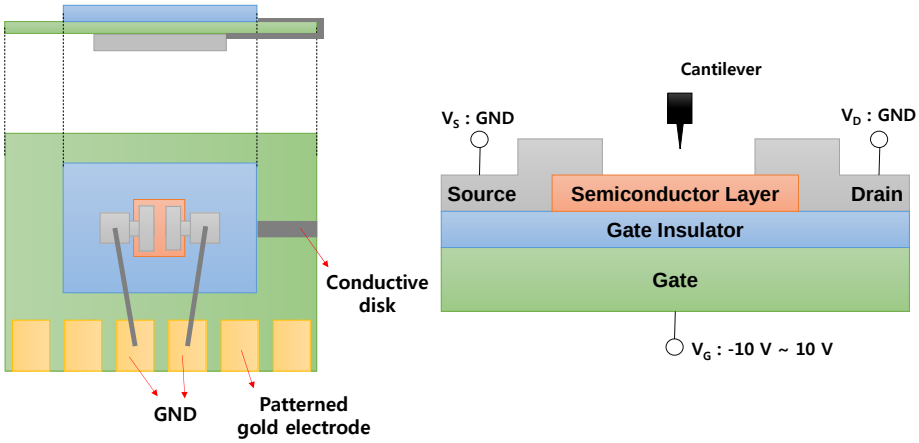


Figure 3.3 Schematic diagram of SKPM measurement.

3.3 Extraction of Density-of-States (DOS) of Solution-Processed IGZO TFTs with Consideration of Back Channel Surface Potential

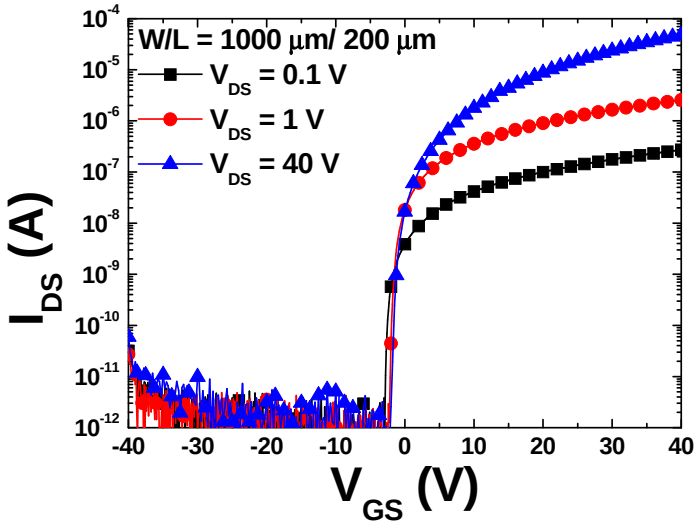
3.3.1 Temperature-Dependent Electrical Characteristics

Figure 3.4 shows transfer and output characteristics of the fabricated solution-processed IGZO TFTs. The fabricated devices exhibited n-type transistor operation and hard saturation. The fabriated device shows a μ_{FE} of ~1.2 $cm^2/V{\cdot}s$, a V_{th} of -0.55 V, a *S.S.* of 320 mV/dec and an on/off current ratio (I_{on}/I_{off}) of greater than 1×10^5. Temperature-dependent electrical characteristics of solution-processed IGZO TFTs was measured to extracted density-of-states (DOS) by field-effect method. For obtaining temperature-dependent characteristics, transfer curves in linear region (V_{DS}=1 V) were measured at temperature ranging from 30 to 80 ℃. Figure 3.5 shows temperature-dependent transfer characteristics of the fabricated devices. When temperature increases, IGZO layer becomes more conductive and V_{th} is negatively shifted. This thermally activated characteristics is well known in semiconductor device physics and especially, for a-IGZO TFTs, the negative shift of V_{th} at higher temperature may originate from thermally activated electrons from the localized states and the generation of defect such as oxygen vacancies that increase with temperature and act as donors [46-47,

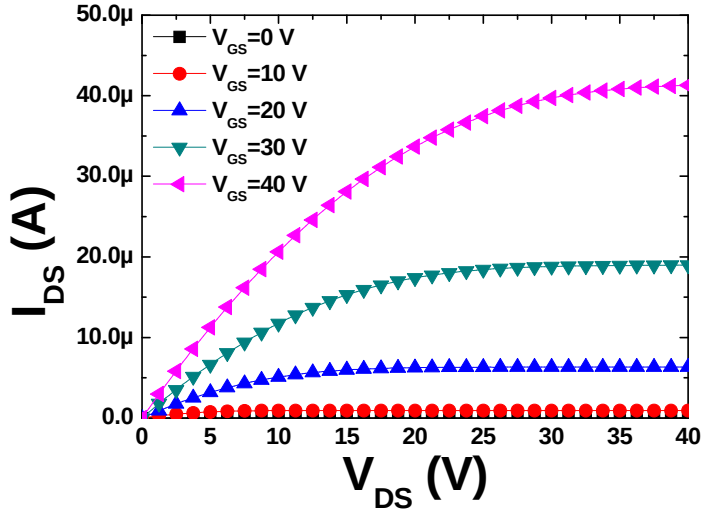
54-55, 77-79]. According to Meyer-Neldel (MN) rule, the drain current near the subthreshold current region can be described as the following equation [47]

$$I_{\mathrm{DS}} = I_{\mathrm{DS0}} exp\left(-\frac{E_{\mathrm{a}}}{kT}\right) = I_{\mathrm{DS00}} exp\left[\left(\frac{1}{E_{\mathrm{MN}}} - \frac{1}{kT}\right)E_{\mathrm{a}}\right], \tag{3.1}$$

where I_{DS0}, I_{DS00} are prefactors for I_{DS}, E_{a} is activation energy, k, T and E_{MN} are the Boltzmann constant, temperature and MN energy, respectively. From these temperature-dependent behaviors and equation (3.1), an Arrhenius plot of log I_{DS} vs $1000/T$ in the subthreshold region and log I_{DS0} vs E_{a} can be obtained as shown in Figure 3.6, and it is found that the fabricated a-IGZO TFTs obey Myer-Neldel (MN) rule and the field-effect method combining MN rule can be applied to the extraction of the DOS distribution [47].



(a)



(b)

Figure 3.4 The electrical characteristics of solution-processed IGZO TFTs. (a) transfer and (b) output characteristics.

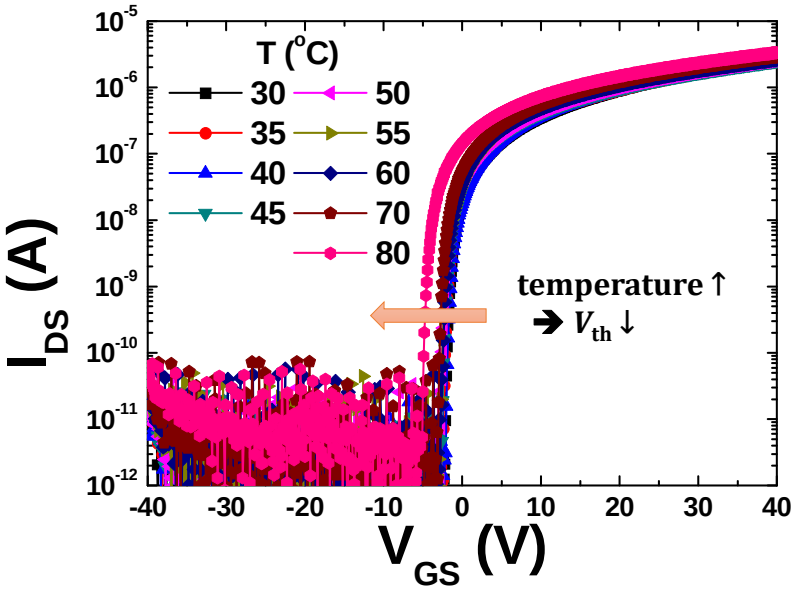


Figure 3.5 Temperature-dependent transfer characteristics of solution-processed IGZO TFTs at temperature ranging from 30 to 80 ℃.

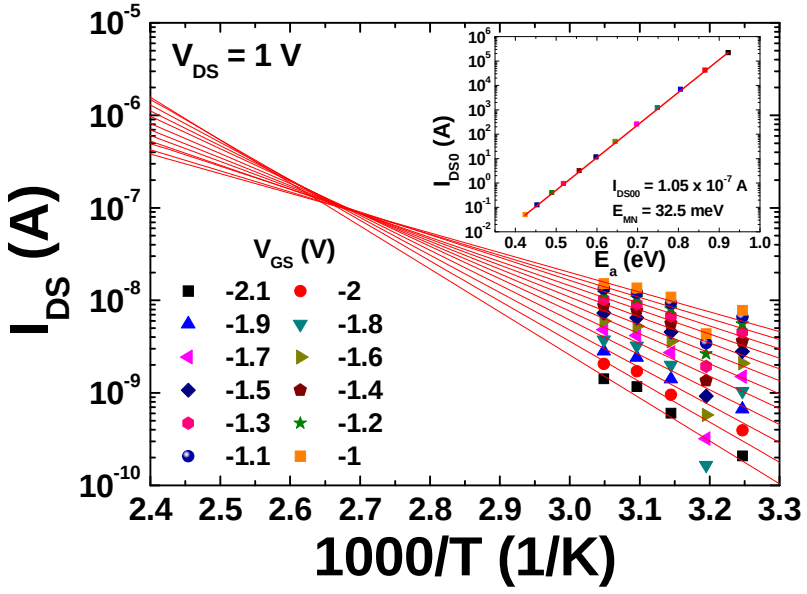


Figure 3.6 Arrhenius plot of solution-processed IGZO TFTs. (inset) the graph of I_{DS0} vs E_a.

3.3.2 Back Channel Surface Potential of Solution-Processed IGZO TFTs

In most cases, one of the assumptions in the conventional field-effect method is zero electric field and zero potential (Φ=0) at the back channel (x=d_{IGZO}) because the semiconductor layer is typically thick enough to fully screen the influence of the applied V_{GS} on the back channel surface as shown in the case of thick active layer in Figure 3.7. However, the assumption of zero potential at the back channel becomes inappropriate when the active layer is thin, since the applied V_{GS} can still change the Φ_B. The critical thickness of the semiconductor layer, at which the Φ_B needs to be considered, is thought to be related to the Debye length which is closely related to charge carrier concentration and DOS [80]. In the subthreshold region, the Debye length is relatively large in comparison with the fully on region since fewer electrons are accumulated before the channel formation. Since the fabricated a-IGZO TFTs have very thin active layer with thickness less than 10 nm, it is assumed that the Φ_B is not zero in the subthreshold region.

For further investigation, scanning Kelvin probe microscopy (SKPM) was used to measure Φ_B of solution-processed IGZO TFTs. The measured Φ_B is represented in Figure 3.8 with the transfer characteristics. The Φ_B linearly increases with the V_{GS} in the subthreshold region (regression line in Figure 3.8) and it is saturated in the above threshold region. This result is closely related to the

operation of transistor. In subthreshold region, electrical channel is formed by accumulation of electrons. Therefore, there is not sufficient number of electrons screening the electric field by V_{GS}, resulting in variation of Φ_B along with V_{GS}. Otherwise, Φ_B is not varied by V_{GS} in above threshold region, since the abundant electrons that exist in channel react to the applied V_{GS}. This indicates that the Φ_B is directly affected by the V_{GS} and there is corresponding band bending in back channel area in subthreshold region.

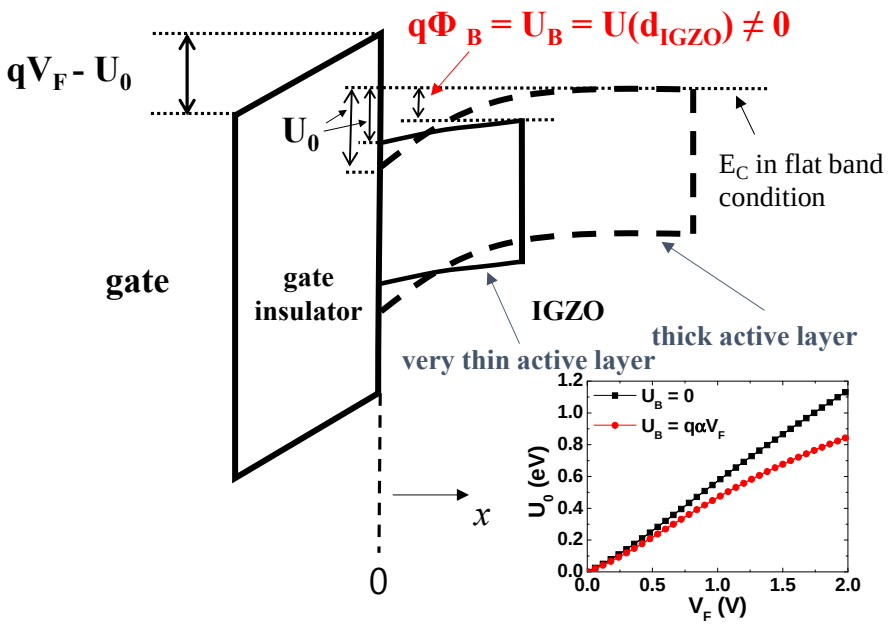


Figure 3.7 Schematic energy band diagram of the modified field effect method with consideration of back channel surface potential: the inset shows the surface potential energy (U_0) calculated by the conventional and modified field-effect method as V_F.

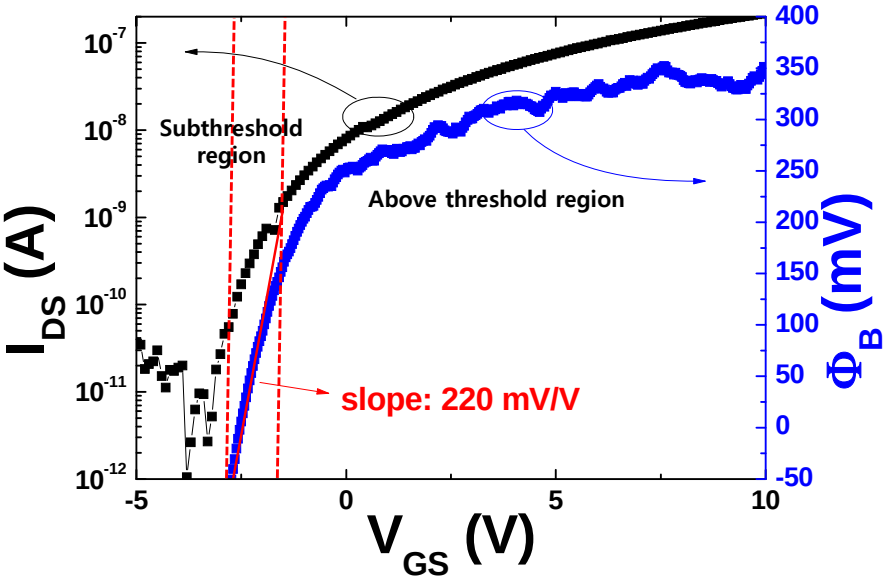


Figure 3.8 Drain current and back channel surface potential variation as V_{GS}.

3.3.3 Modified Field-Effect Method Considering Back Channel Surface Potential

Since the fabricated solution-processed IGZO TFTs have very thin active layer, the back channel surface potential is not zero in solution-processed IGZO TFTs as investigated in previous chapter. Therefore, boundary condition was modified as follow.

$$\frac{dU(x)}{dx} = 0,\ U(x) = U_B = q\Phi_B \qquad \text{if } x=d_{IGZO}, \tag{3.2}$$

$$\frac{dU(x)}{dx} = -\frac{q\varepsilon_{ins}}{d_{ins}\varepsilon_{IGZO}}\left(V_F - \frac{U_0}{q}\right) \qquad \text{if } x=0, \tag{3.3}$$

where $U(x)$ is an electrostatic potential energy caused by band bending; U_B is an electrostatic potential energy at back channel surface; q is an electronic charge; ε_{ins} is the relative dielectric constant of the insulator; d_{ins} is the thickness of the insulator; ε_{IGZO} is the relative dielectric constant of a-IGZO, V_F is difference between V_{GS} and flat band voltage (V_{FB}); and U_0 is surface potential energy. The energy band diagram for the conventional and modified field-effect method and increasing direction of x are represented in Figure 3.7.

Furthermore, based on the results of SKPM measurement, back channel surface potential is modeled as a linear function of the V_{GS} (and thus V_F) as $U_B=q\Phi_B = q\alpha V_F$, where α is the proportional factor. Then, the following equations were obtained,

$$n(U_0) = \frac{\varepsilon_0 \varepsilon_{ins} G_{FB} \left[exp(\beta - A) U_0 - 1 \right]}{d_{ins} d_{IGZO} \, dG_{DS} / dV_F} - \frac{\varepsilon_{ins}^2 \varepsilon_0}{d_{ins}^2 \varepsilon_{IGZO}} \left(V_F - \frac{U_0}{q} \right), \quad (3.4)$$

$$E_a(V_{GS}) = E_{aFB} + \frac{G_{FB}}{G_{DS}(V_{GS}) d_{IGZO}} \sqrt{\frac{\varepsilon_{IGZO} \varepsilon_0}{q}} \times \int_{q\alpha V_F}^{U_0} \frac{U \exp\left[(\beta - A) U \right]}{\sqrt{2 \int_{q\alpha V_F}^{U} n(U) dU}} dU, \quad (3.5)$$

where n is the electron carrier density; ε_0 is the permittivity of vacuum; G_{FB} is flat band conductance; β is $1/kT$; A is a variable used for the extraction of the intrinsic MN energy; G_{DS} is conductance; and E_{aFB} is the Fermi level in the flat band condition. Figure 3.9 shows E_a vs V_{GS} including the measured data (dots) and fitted curves (lines) calculated from conventional (Φ_B=0) and modified (U_B=$q\Phi_B$=$q\alpha V_F$) field-effect methods. It is clearly shown that the measured data is well consistent with the result from the modified field-effect method. From the extraction process of E_a, the important parameters for extracting accurate DOS are obtained. Especially, accurate calculation of E_a is very important in obtaining $G_{DS}(V_{GS})$ and thus $n(U_0)$. If the Φ_B cannot be assumed to be zero, the U_0 will be correspondingly changed because the states of the whole semiconductor layer react to the applied V_{GS}. The modified field-effect method exhibited lower U_0 than the conventional method as shown in the inset of Figure 3.7. Since the U_0 is closely related to the extraction of defect profile of interface and bulk, and thus interface properties and electrical characteristics of metal-oxide TFTs, Φ_B also needs to be considered to understand the electrical operation of solution-processed metal-oxide TFTs.

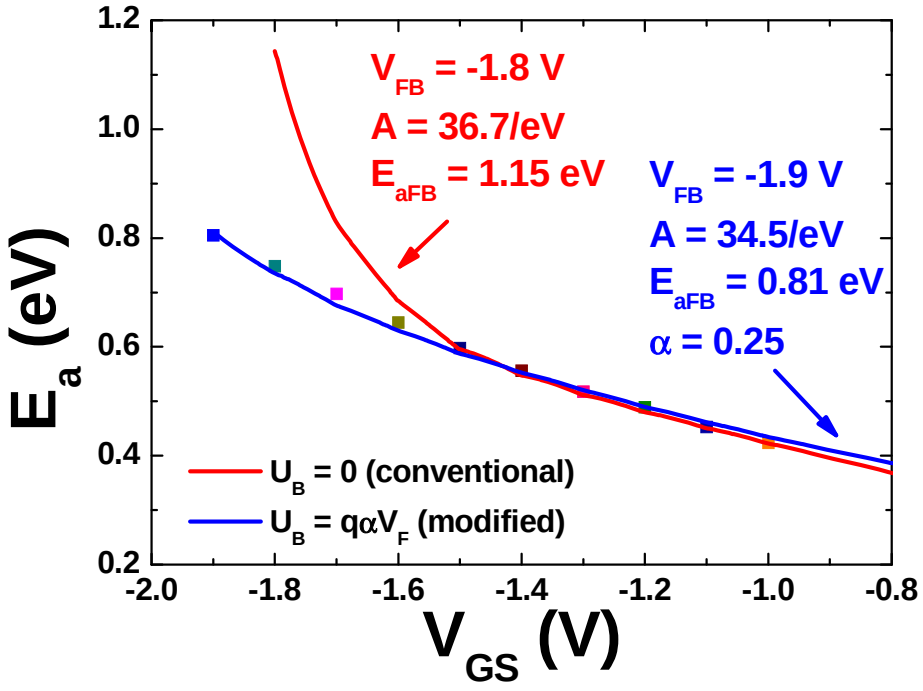


Figure 3.9 The graph of E_a vs V_{GS} with measured data and fitted line by conventional and modified field-effect method with consideration of back channel surface potential.

3.3.4 DOS Extraction of Solution-Processed IGZO TFTs by Modified Field-Effect Method Considering Back Channel Surface Potential

The DOS extracted by the modified field-effect method using V_{FB}=-1.9 V, A=34.5 eV^{-1}, E_{aFB}=0.81 eV, and α=0.25 is shown in Figure 3.10. The value of α was comparable to the measured slope of the SKPM result (Figure 3.8). The extracted DOS can be expressed and well fitted by the exponential tail and Gaussian deep states given by

$$N_{tail}(E) = N_{ta}\exp\left(-\frac{E_C - E}{w_{ta}}\right), \tag{3.6}$$

$$N_{deep}(E) = N_{ga}\,exp\left[-\frac{(E - E_{ga})^2}{w_{ga}^2}\right], \tag{3.7}$$

where N_{ta}, E_C, w_{ta}, N_{ga}, E_{ga} and w_{ga} are the peak value of tail states, the conduction band edge, the characteristic energy of the tail states, the peak value of deep states, the mean value of the deep states and the variance of the deep states, respectively. The fitted parameters of the DOS extracted by conventional and modified field-effect methods are listed in Table 3.2. The obtained values of N_{ta}, N_{ga} and w_{ga} are larger and w_{ta} and E_{ga} are smaller than the ones obtained from the conventional field-effect method (Φ_B=0). Although the error of the deep states are relatively small, the extracted tail states showed large error up to 167 % when the Φ_B is not considered. As a result, the total trap density, N_{total} (integration of the DOS) extracted by the

conventional and the modified field-effect method are 4.90×10^{15} cm^{-3} and 1.45×10^{16} cm^{-3}, respectively, and the error factor is 66 %. Therefore, the consideration on the Φ_B is critical for extracting accurate DOS profile of solution-processed IGZO TFTs with thin active layer.

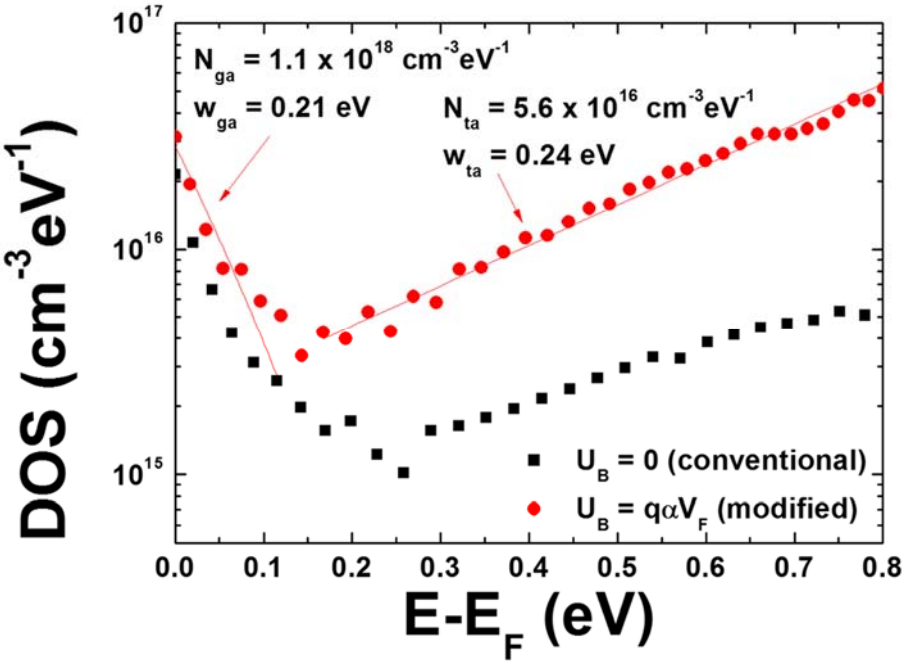


Figure 3.10 The distribution of the solution-processed a-IGZO TFTs extracted by the conventional and modified field effect method including back channel surface potential variation.

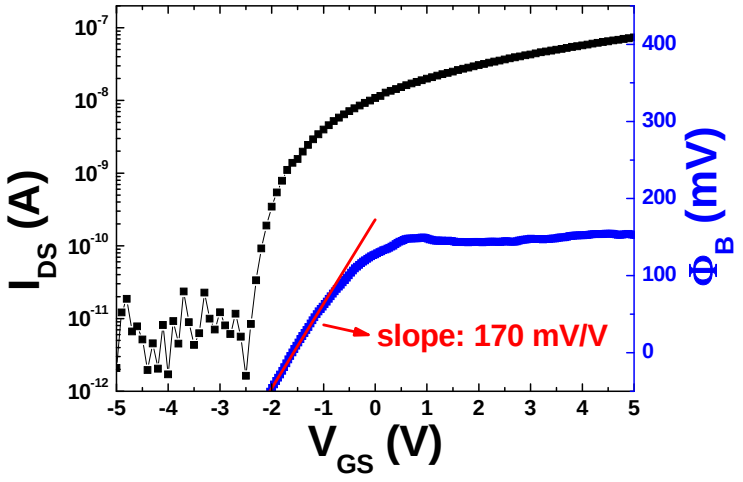
Table 3.2 The fitted parameters of the DOS extracted by the conventional and modified field effect method with error factors

	N_{ta} ($cm^{-1}eV^{-1}$)	w_{ta} (eV)	N_{ga} ($cm^{-1}eV^{-1}$)	w_{ga} (eV)	E_{ga} (eV)	Total trap density (cm^{-3})
Conventional	8.2×10^{15}	0.64	4.3×10^{17}	0.15	-0.27	4.90×10^{15}
Modified	5.6×10^{16}	0.24	1.1×10^{18}	0.21	-0.41	1.45×10^{16}
Error factor	86 %	167 %	61 %	29 %	34 %	66 %

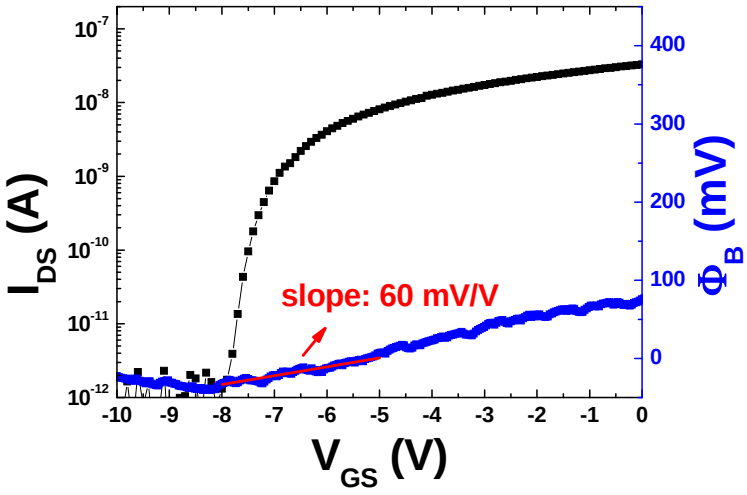
3.3.5 Verification of Assumption of Back Channel Surface Potential

The assumption of the non-zero Φ_B can be revisited by using the extracted DOS parameters and carrier concentration. It is mentioned that the Debye length in the subthreshold region is sufficiently large in comparison with the semiconductor layer thickness. The carrier concentration can be calculated by the relation between V_{on} and concept of full depletion [58]. The calculated carrier concentration is 5.23×10^{15} cm^{-3}, which is similar to the result ($\sim5\times10^{15}$ cm^{-3}) obtained from the Hall measurement and comparable to the previously reported results [34, 63]. Based on the extracted DOS parameters and the carrier concentration, Debye length is calculated to be about 30 nm. The d_{IGZO} ($\sim$8 nm) is smaller than the calculated Debye length. Therefore, it is confirmed that the assumption which the Φ_B is not zero in the subthreshold region is appropriate in the case of solution-processed IGZO TFTs having thin active layer. The Φ_B of devices with different d_{IGZO} was also measured to verify our DOS model and relation between Φ_B and d_{IGZO} as shown in Figure 3.11. If the effect of V_{GS} on Φ_B is related to d_{IGZO} and Debye length, the measured Φ_B and slope of SKPM result is reduced as d_{IGZO} increases because the electric field induced by V_{GS} is sufficiently screened by electrons and defect states in thick IGZO semiconductor layer and cannot affect the back channel surface. By comparing Figure 3.8 and Figure 3.11, it is found that slope of SKPM result and Φ_B is decreased when d_{IGZO} increases.

Specifically, the slope of the SKPM result was reduced from 220 to 60 mV/V as d_{IGZO} increases from ~8 nm to 120 nm. The reason why Φ_B is not zero with d_{IGZO} of 120 nm is that back channel is floated and the Debye length is the exponent of exponential function which describes electrical potential in semiconductor layer. However, Φ_B is negligibly small when d_{IGZO} is larger than Debye length. Furthermore, because the discrepancy between the measured and the fitted data of E_a originated from inaccurate estimation of the movement of E_F due to the assumption of zero electric potential at back channel surface, it is expected that the discrepancy is reduced when d_{IGZO} increases and Φ_B is nearly zero. Figure 3.12 shows the measured data of E_a and the fitted curve without consideration of Φ_B. The discrepancy between the measured and the fitted data of E_a without consideration of Φ_B reduces as d_{IGZO} increases as shown in Figure 3.12. From these results, it is confirmed that Φ_B can be affected by V_{GS} when active layer thickness is smaller than Debye length.

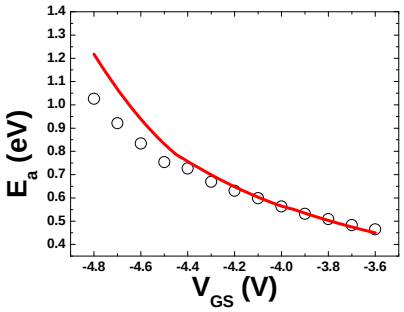


(a)

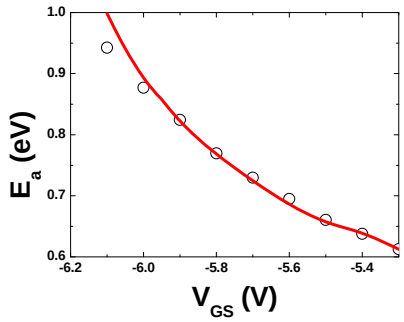


(b)

Figure 3.11 The measured Φ_B with d_{IGZO} of (a) 20 and (b) 120 nm.



(a)



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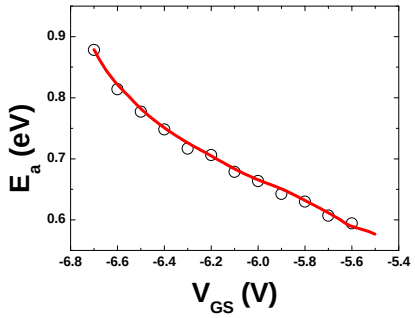


(c)

Figure 3.12 The graph of E_a vs V_{GS} of solution-processed IGZO TFTs with different active layer thickness of (a) 20, (b) 32, and (c) 70 nm. (dot: measured data, line: fitting result without consideration of Φ_B)

3.4 Conclusion

The modified field-effect method is proposed where the variation of the Φ_B was considered in the extraction process of defect DOS for the solution-processed a-IGZO TFTs with an active layer thinner than its Debye length. The Φ_B of the fabricated devices was measured and then modeled as a linear function of the V_{GS} in the subthreshold region. The conventional field-effect method was modified accordingly, resulting in more consistent results with the measured data. While the DOS was underestimated by the conventional field-effect method, more accurate DOS was obtained with the consideration of Φ_B. Since the thickness and DOS of the semiconductor layer in the metal-oxide TFTs are directly related to their performance, accurate extraction of the DOS considering back channel surface potential and active layer thickness effect is very important to investigate the device physics, optimize the fabrication process and enhance the electrical performance of the solution-processed devices.

Chapter 4 Effect of Process Parameters on DOS of Solution-Processed IGZO TFTs

4.1 Introduction

The electrical characteristics of solution-processed IGZO TFTs can be modified by changing process parameters such as annealing temperature (T_a), metallic composition ratio of IGZO layer, and the thickness of IGZO active layer (t_{active}). The effect of these parameters on basic electrical characteristics of solution-processed IGZO TFTs has been reported by many groups [32, 34, 51-57, 63-66]. In general, solution-processed IGZO TFTs annealed at higher temperature exhibit higher field-effect mobility (μ_{FE}) and negatively shifted turn-on voltage (V_{on}) [51, 53-57]. When indium ratio increases, threshold voltage (V_{th}) decreases and μ_{FE} increases [63]. The conductivity of

solution-processed IGZO film is reduced as gallium ratio increases, resulting in positively shifted V_{th} and lower μ_{FE} [54]. When zinc ratio increases, linear μ_{FE} decreases [64]. This variation of electrical properties due to T_a and metallic composition ratio is closely related to the metal-oxide formation mechanism of sol-gel process and the role of each component. Since T_a and composition ratio affect the chemical properties of solution-processed IGZO film, electrical properties such as carrier density, and thus device properties can be changed by process parameters. On the other hand, because the number of carrier is increased and more pin-holes and voids can be existed in solution-processed semiconductor film as t_{active} increases, solution-processed metal-oxide semiconductor TFTs with thicker active layer show lower V_{on} and μ_{FE} [65-67]. In fact, previous reports focused on the relation between chemical variation and electrical characteristics. However, it is required to develop the electrical model related to the process parameters for device optimization and practical electronic application. The defect DOS is the device property that can model device characteristics and be used to simulate device operation in electronic applications. In this chapter, the effects of T_a, metallic composition ratio, and t_{active} on DOS are investigated by comparing DOS with the film properties including chemical bonding variation and physical defects. The modified field-effect method with consideration of back channel surface potential, which is developed in Chapter 3, is used to extract the defect DOS. Furthermore, the origin of DOS is investigated for the development of DOS map.

4.2 Experiment

The overall fabrication process of solution-processed IGZO TFTs investigated in this chapter is similar to process mentioned in Chapter 3. In Chapter 4.3, precursor solution was prepared by dissolving indium acetate, gallium nitrate, and zinc acetate into 2-methoxyethanol with ethanolamine. The molar ratio of indium, gallium and zinc was 3:1:2. The heavily doped p-type silicon and thermally grown silicon dioxide (SiO_2) were used as gate and gate insulator, respectively. The IGZO semiconductor layer was deposited by spin-coating process and annealed at 400, 500, and 600 ℃ for 1 hour to fabricate solution-processed IGZO TFTs with different T_a. Source and drain (S/D) electrodes were deposited by thermal evaporation through metal shadow mask. In Chapter 4.4, composition molar ratio of precursor solution was controlled to fabricate solution-processed IGZO TFTs with different metallic composition ratio. The molar ratio of indium, gallium, and zinc was varied by 7:1:4, 6:2:4, and 5:3:4 and total concentration was fixed at 0.137 M. The heavily doped p-type silicon and thermally grown SiO_2 were used as gate and gate insulator, respectively. The IGZO active layer was deposited by spin coating and annealed at 500 ℃ for 1 hour. Thermal evaporation was used to deposit S/D electrodes. In chapter 4.5, total concentration of precursor solution was changed from 0.137 to 0.685 M to obtain IGZO semiconductor with different thickness. The molar ratio of indium, gallium, and zinc was fixed at 3:1:2. The heavily

doped p-type silicon and thermally grown SiO_2 were used as gate electrode and gate insulator, respectively. The IGZO film was deposited by spin coating process and annealed at 500 ℃ for 1 hour. S/D electrodes were deposited by thermal evaporation. In all samples, IGZO semiconductor layer was patterned by conventional photolithography and wet etching process. More detail fabrication process, measurement, and extraction method were same with those used in Chapter 3.

4.3 Effect of Annealing Temperature on DOS of Solution-Processed IGZO TFTs

4.3.1 Device Characteristics

The transfer and output characteristics of solution-processed IGZO TFTs with different T_a are shown in Figure 4.1. All samples exhibit n-type transistor operation and hard saturation. The interface between IGZO semiconductor layer and aluminum source and drain electrodes shows good contact property without s-shape [81-82]. As T_a increased, V_{on} was negatively shifted and on current (I_{on}) and μ_{FE} increased. Specifically, V_{on} is decreased from 0.65 to -12.13 V, μ_{FE} is increased from 0.25 to 5.35 $cm^2/V{\cdot}s$, and on/off current ratio (I_{on}/I_{off}) is increased from 5.20×10^4 to 5.35×10^5, respectively. The representative electrical parameters are summarized in Table 4.1. The variation of electrical properties is attributed to difference of chemical reaction during annealing process as T_a changes. In sol-gel process, metal-oxide is formed by reaction between metal precursor and water molecule from the ambient air [50]. If sufficient thermal energy is not supplied to the coated film due to low T_a, precursor is transformed incompletely to metal-oxide film, and hydroxyl group and contaminants are remained in the annealed film. Since electron conduction path of IGZO is formed by In 5s orbital and carrier is generated by oxygen vacancy, sufficient metal-oxide bonding and oxygen vacancy are required for proper device operation. In addition,

the residual impurities can degrade the electrical properties by acting as charge trapping sites. Because the amount of metal-oxide bonding, oxygen vacancy, residual hydroxide and other impurities in solution-processed IGZO film is related to thermal energy supplied during annealing process, the electrical properties of solution-processed IGZO TFTs is also affected by T_a. The chemical bonding variation along with T_a is estimated by x-ray photoelectron spectroscopy (XPS) analysis. Figure 4.2 shows the O1s XPS spectra of solution-processed IGZO films annealed at different T_a and O1s peak can be fitted by three Gaussian distribution. The peaks of each Gaussian distribution are centered at 529.8, 531.0, and 532.0 eV and related to metal-oxide bond without oxygen vacancy, metal-oxide bond with oxygen vacancy and hydroxide, respectively. The ratio of each chemical bonding is summarized in Table 4.2. In formation process of solution-processed IGZO film, metal-oxide is formed through dihydroxylation of metal hydroxides by thermal energy and the ratio of metal-oxide lattice and oxygen vacancy generation is affected by T_a [52, 54]. In other words, metal hydroxides are incompletely transformed into metal oxides and a lot of residual hydroxide are remained in solution-processed IGZO film at low T_a. It is also observed in XPS results. The ratio of oxygen vacancy and hydroxide is increased and decreased, respectively, when T_a increases. The variation of electrical characteristics with various T_a can be analyzed based on above XPS analysis result with aspect of material chemistry. From above analysis, it is found that the carrier

concentration is increased as T_a increases because oxygen vacancy is carrier generation mechanism in IGZO semiconductor as equation (2.14). In IGZO TFTs, channel is fully depleted in off state and more negative V_{GS} is required to turn off the IGZO TFT having higher carrier density [58]. Therefore, negatively shifted V_{on} of solution-processed IGZO TFTs annealed at high T_a can be explained by large amount of oxygen vacancy and high electron concentration. High μ_{FE} is attributed to the electron conduction path of solution-processed IGZO TFTs. As mentioned above, the conduction path of IGZO TFTs is formed by In 5s orbital, and it originates from metal-oxide lattice, not metal hydroxides [27, 54]. Since metal hydroxides cannot contribute the carrier conduction, solution-processed IGZO TFTs annealed at low T_a exhibit lower μ_{FE}. In addition, high carrier concentration of devices annealed at high T_a is also origin of high μ_{FE}, because the μ_{FE} of IGZO TFTs can be improved by high carrier concentration based on percolation transport mechanism [59-61].

The crystallinity of solution-processed IGZO film annealed at different temperature was investigated by grazing incidence x-ray diffraction (GI-XRD) analysis of IGZO film deposited on glass substrate. IGZO film annealed at 600 ℃ showed nanocrystalline properties as shown in Figure 4.3. The result of phase change from amorphous to nanocrystalline at high T_a is consistent with the previous reports [32, 52]. As mentioned in Chapter 2.2, one of the assumption of field-effect method is uniform active layer

(Assumption (1)). Due to the grain boundary caused by non-uniform semiconductor layer such as polycrystalline or nanocrystalline phase, the electrical properties cannot be homogeneous resulting in large error of DOS extracted by field-effect method. Consequently, it is inappropriate to directly compare the DOS of solution-processed IGZO TFTs annealed at 600 ℃ with that of other devices using the modified field-effect method. From this reason, solution-processed IGZO TFTs annealed at 600 ℃ is excluded from DOS extraction and analysis in following discussion.

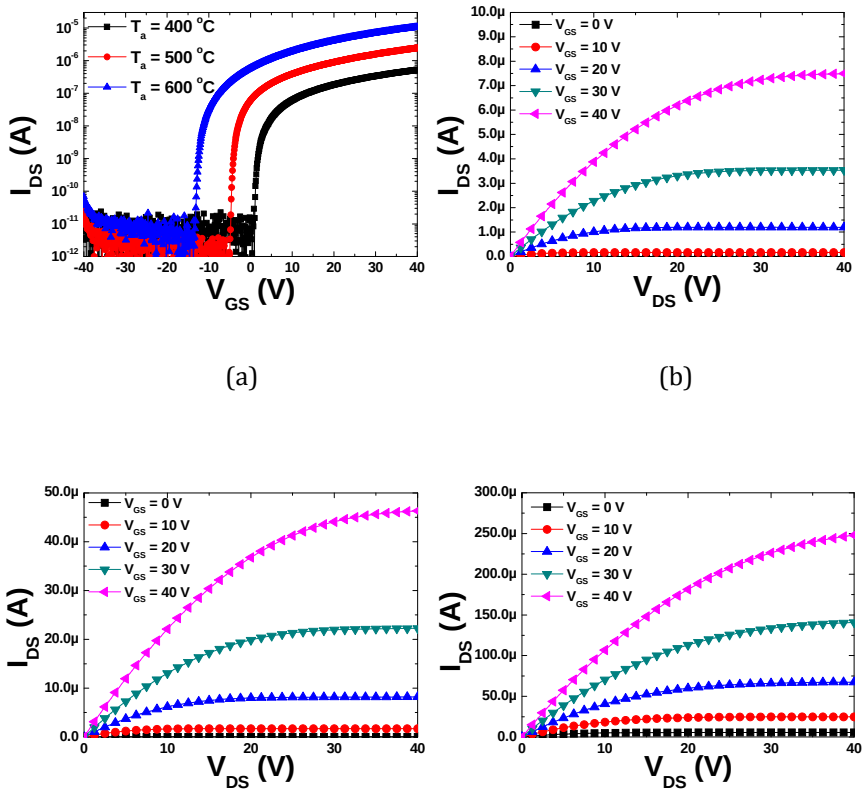
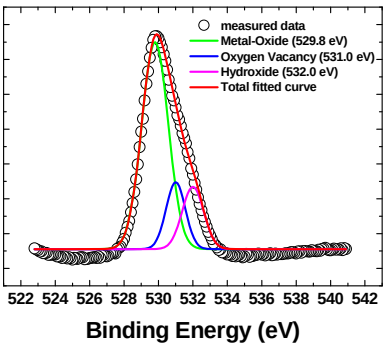


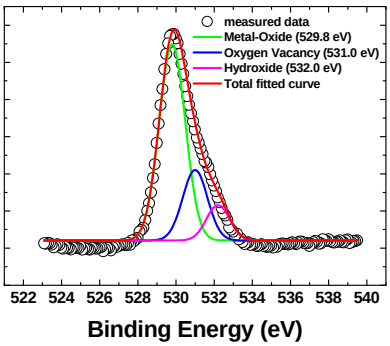
Figure 4.1 (a) Transfer characteristics of solution-processed IGZO TFTs annealed at various temperature, and output characteristics of solution-processed IGZO TFTs annealed at (b) 400, (c) 500, and (d) 600 ℃.

Table 4.1 Electrical Characteristics of solution-processed IGZO TFTs annealed at different temperature

T_a (℃)	400	500	600
V_{on} (V)	0.65	-4.13	-12.13
μ_{FE} ($cm^2/V{\cdot}s$)	0.28	1.24	5.35
V_{th} (V)	1.97	-2.35	-10.3
S.S. (V/dec)	0.438	0.407	0.481
I_{on}/I_{off}	5.2×10^4	1.2×10^5	2.3×10^5



(a)



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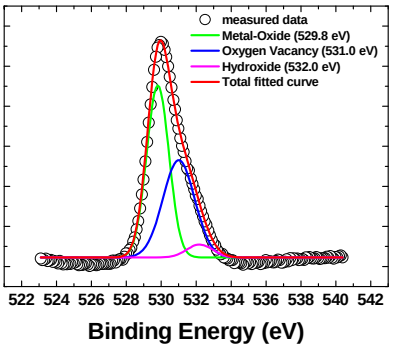
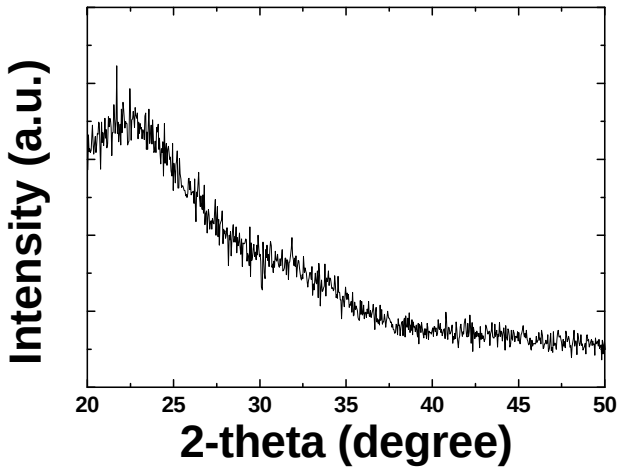


(c)

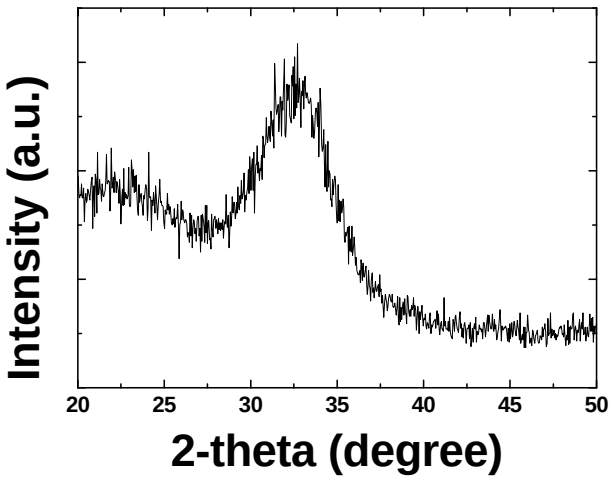
Figure 4.2 O1s XPS spectra of solution-processed IGZO film annealed at (a) 400, (b) 500, and (c) 600 ℃.

Table 4.2 Bonding ratio of solution-processed IGZO film annealed at different temperature

T_a (℃)	Metal-Oxide	Oxygen Vacancy	Hydroxide
400	67.7 %	15.8 %	16.5 %
500	66.5 %	22.9 %	10.6 %
600	52.9 %	42.5 %	4.6 %



(a)



(b)

Figure 4.3 GI-XRD results of solution-processed IGZO film annealed at (a) 500 and (b) 600 ℃.

4.3.2 DOS Extraction Considering Back Channel Surface Potential and Analysis

The DOS of solution-processed IGZO TFTs annealed at 400 and 500 ℃ is extracted by the modified field-effect method developed in Chapter 3. As introduced in Chapter 3, it is required to confirm that the devices show thermally activated characteristics and follow Meyer-Neldel (MN) rule before DOS extraction. Temperature-dependent transfer characteristics were measured by changing temperature from 30 to 80 ℃ as shown in Figure 4.4. The transfer curves show negative shift trend as temperature increases in all samples. The thermally activated characteristics is well known in amorphous IGZO TFTs. It is attributed to the thermally activated electrons from localized states to conduction band and generated defects acting as donors [46-47, 54-55, 77-79]. Arrhenius plot is presented in Figure 4.5 and the activation energy (E_a) is extracted by following equation,

$$I_{DS} = I_{DS0} exp\left(-\frac{E_a}{kT}\right), \quad (4.1)$$

where I_{DS0}, k, and T are the prefactor for I_{DS}, the Boltzmann constant and the temperature, respectively. From Figure 4.5, it is confirmed that the fabricated devices exhibit thermally activated characteristics and the modified-field effect method can be applied to extract the defect DOS. The graph of the extracted E_a vs gate voltage (V_{GS}) are presented in the inset of Figure 4.5. The solid and dashed line

represent fitting curves based on the modified and conventional field-effect method, respectively. It is found that the modified field-effect method shows more consistent fitting result with the measured data. Furthermore, the E_a near the flat band voltage (V_{FB}) is increased as T_a is decreased. It is related to the location of Fermi level (E_F) and it will be explained below. The defect DOS is extracted by same procedure introduced in Chapter 3. The extracted DOS is presented in Figure 4.6. The E_F is closed to conduction band edge (E_C) and tail and relatively deep states exhibit contrary trend as T_a changes. When T_a is increased from 400 to 500 ℃, the relatively deep and tail states are increased and decreased, respectively. The origin of the deep and tail states are analyzed by comparing the extracted DOS with chemical bonding variation as T_a changes. Since oxygen vacancy increases and residual hydroxide decreases as T_a increases, each chemical bond can be matched to the deep and tail states, respectively. Consequently, it can be concluded that deep and tail states are related to oxygen vacancy and residual hydroxide in solution-processed IGZO TFTs, respectively, as shown in Figure 4.6. The electrical characteristics can be explained by the result of DOS analysis.

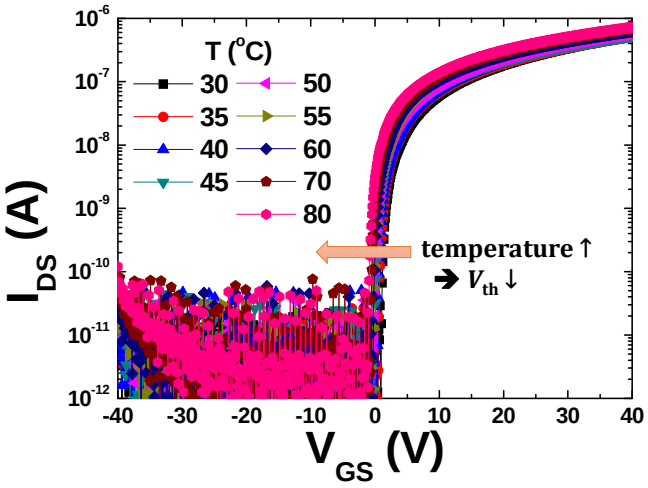
First, more negatively shifted V_{on} of IGZO TFTs annealed at higher temperature is related to the location of E_F and higher deep states. The E_F becomes closer to E_c when T_a increases. In operation of n-type TFTs, E_F is moved to E_C, resulting in the increase of the activated electrons in conduction band, as V_{GS} increases. The relation between

the location of E_F and carrier density can be described by following equation,

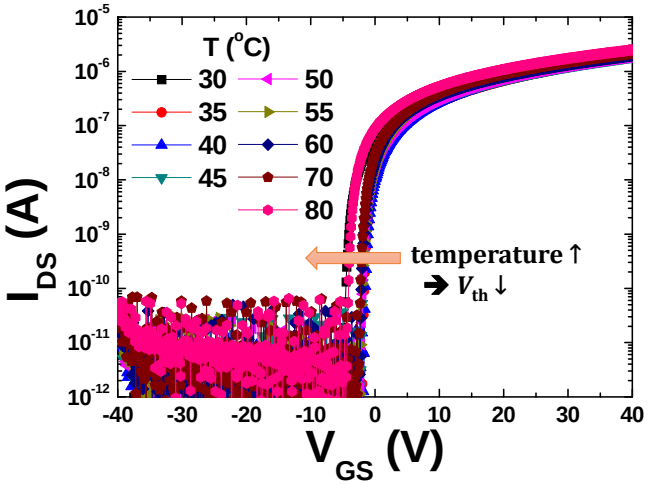
$$n = N_C exp\left(\frac{E_C - E_F}{kT}\right), \quad (4.2)$$

where N_C is the effective density of conduction band states. When electrons are accumulated sufficiently to form channel, current starts to flow through the electron channel. Therefore, E_F located closer to E_C means that electron channel can be formed at lower V_{GS}. Since sufficient electrons to form channel can be accumulated by lower V_{GS}, negatively shifted V_{on} of devices annealed at higher temperature can be explained by this smaller energy difference between E_F and E_C. In addition, higher deep states, which is attributed to oxygen vacancy, are also related to lower V_{on}. Generally, carrier generation of metal-oxide semiconductor is related to oxygen vacancy. Therefore, higher deep states result in larger carrier density. The different carrier density can be also explained by different E_F with equation (4.2). Since more negative voltage is required to fully deplete channel with higher carrier concentration, higher deep states can explain more negatively shifted V_{on}. Second, μ_{FE} can be explained by the tail states. As mentioned above, metal hydroxide cannot contribute the electron conduction path and thus μ_{FE} is degraded with high ratio of hydroxide. In addition to the analysis in chemical aspect, the degraded electron transport property can be electrically explained based on the developed DOS model. From analysis of DOS relating to chemical

variation, it is concluded that the tail states of solution-processed IGZO TFTs are attributed to the residual hydroxides and increased at low T_a. The electron transport through conduction band can be inhibited by the tail states in band gap because electrons can be trapped at the defect states beneath E_C. As a result, the devices with larger tail states show lower μ_{FE} [74]. In other words, from the analysis of the extracted DOS with consideration of Φ_B, the μ_{FE} variation as T_a changes can be electrically modeled by using the different tail state profile.

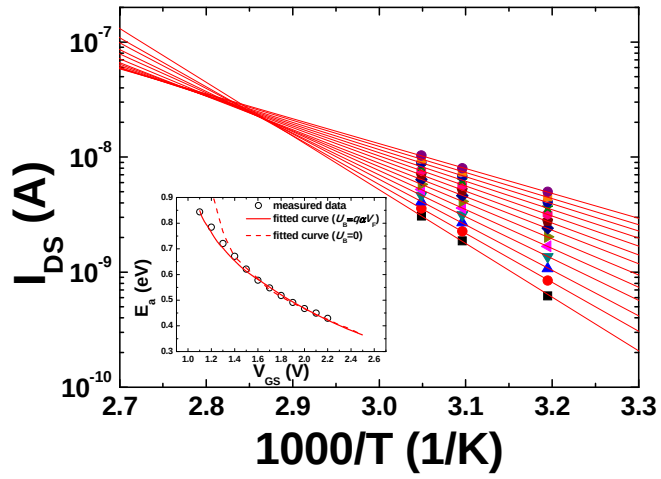


(a)

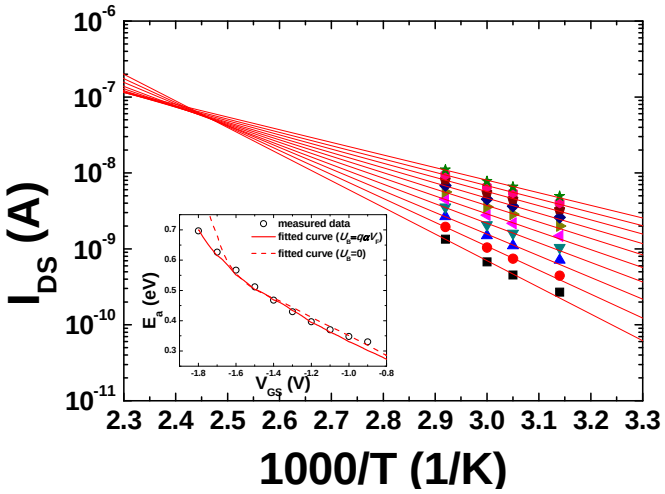


(b)

Figure 4.4 Temperature-dependent transfer curves of solution-processed IGZO TFTs annealed at (a) 400 and (b) 500 ℃.



(a)



(b)

Figure 4.5 Arrhenius plot of solution-processed IGZO TFTs annealed at (a) 400 and (b) 500 ℃.

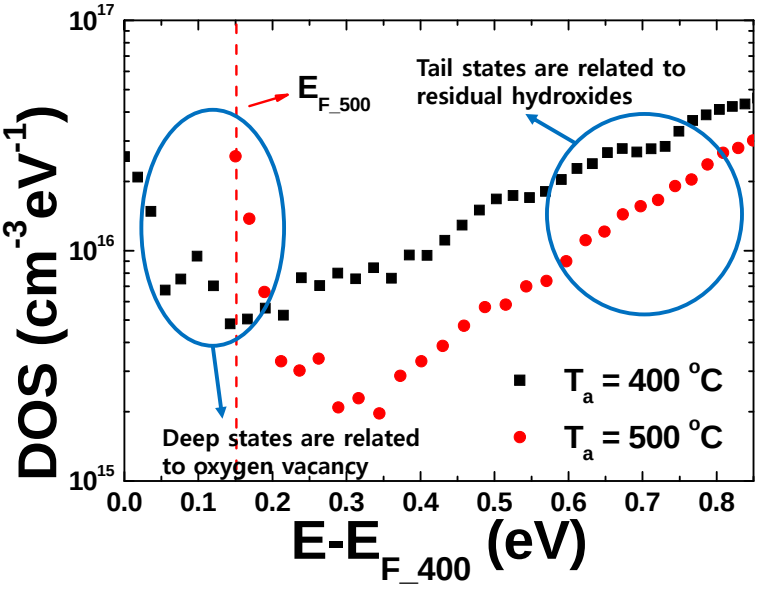


Figure 4.6 The extracted DOS of solution-processed IGZO TFTs annealed at 400 and 500 ℃. The origin of tail and deep states is analyzed based on the extracted DOS and XPS results of solution-processed IGZO TFTs annealed at different temperature.

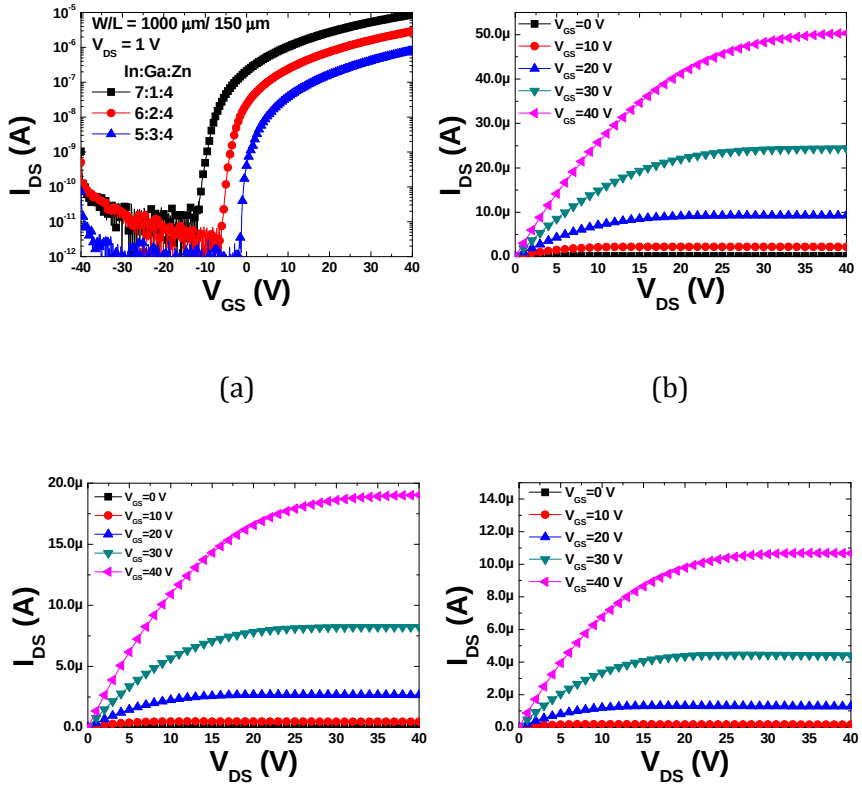
4.4 Effect of Metallic Composition Ratio on DOS of Solution-Processed IGZO TFTs

4.4.1 Device Characteristics

The transfer and output characteristics of solution-processed IGZO TFTs with different metallic composition ratio are shown in Figure 4.7. All samples exhibited typical operation of n-type transistors and hard saturation. The interface between IGZO semiconductor layer and aluminum source and drain electrodes shows good contact property without s-shape [81-82]. When indium ratio increases, V_{on} is negatively shifted and both on and off current (I_{on} and I_{off}) are increased. It is attributed to difference of carrier density due to the variation of metallic composition ratio as explained below. The representative electrical parameters are summarized in Table 4.3. When In/Ga ratio increases, V_{on} and μ_{FE} are decreased and increased, respectively, and this trend of electrical characteristics as the change of composition ratio is consistent with the previously reported results [34, 54, 63-64]. It is related to the variation of chemical bonding ratio due to different composition ratio, resulting in the variation of carrier density, electron transport path and defect states. First, the negatively shifted V_{on} is related to the variation of carrier density. In IGZO semiconductor film, oxygen vacancy is one of the carrier generation mechanism as equation (2.14) and the amount of oxygen vacancy is affected by composition ratio of gallium. Since

gallium can form stronger bond with oxygen than indium and zinc, the formation of oxygen vacancy is suppressed by the increase of gallium ratio [27, 54]. Consequently, the carrier concentration and the conductivity are reduced when higher ratio of gallium is contained in IGZO film. In addition, higher carrier density results in lower V_{on} because active layer needs to be fully depleted to turn off the transistor in IGZO TFTs and more negative voltage is required to deplete more electrons [58]. The enhancement of μ_{FE} in solution-processed IGZO TFTs with higher indium ratio is related to the carrier conduction path in IGZO TFTs. In IGZO semiconductor film, the bottom of conduction band is formed by In 5s orbital. Because the overlap of In 5s orbitals is increased with higher indium ratio, electron transport through conduction band become easier and the improved μ_{FE} is achieved. Furthermore, as indium ratio increases, excess indium can link to other indium atom, resulting in more conducting electron paths and higher electron mobility [63]. In addition, electron mobility is also enhanced with higher carrier density according to percolation transport theory in IGZO film [59-61]. Above explanation is based on the aspect of material chemistry and supported by the XPS results. Figure 4.8 shows the O1s XPS spectra of the solution-processed IGZO TFTs with various metallic composition ratio. The measured O1s peak can be fitted by three Gaussian distribution centered at 529.6, 531.0, and 532.0 eV, respectively. From the smallest binding energy, each peak is related to metal-oxide bond without oxygen vacancy, metal-oxide bond with

oxygen vacancy, and residual hydroxide, respectively. The ratio of each bond is summarized in Table 4.4. The ratio of metal-oxide bond is increased and the ratio of oxygen vacancy and hydroxide is decreased when gallium ratio increases. This trend of O1s spectra as change of composition ratio is similar result with the previous reports [54]. As mentioned above, gallium suppresses the formation of oxygen vacancy due to its higher binding energy with oxygen than other metal components. Therefore, metal-oxide bond is increased while oxygen vacancy is decreased with higher gallium ratio. The reduction of hydroxides with the increase of gallium ratio is attributed to the role of gallium in solution-processed IGZO TFTs. In sol-gel process, metal hydroxides are converted into metal-oxide lattice by thermal energy during annealing process [52, 54] and the formation of metal-oxide lattice dominantly depends on T_a. However, IGZO film has smaller hydroxides than IZO film at low T_a. That is, metal-oxide lattice and the reduction of hydroxides ratio can be achieved by gallium doping [54]. Consequently, the increase of gallium ratio induces the reduction of oxygen vacancy and hydroxides in solution-processed IGZO TFTs.



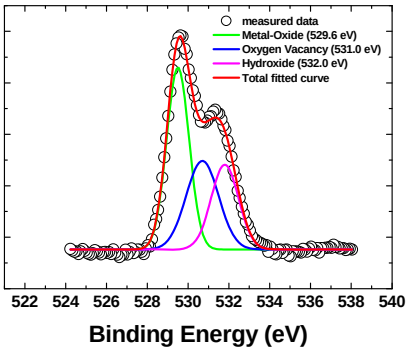
(a) (b)

(c) (d)

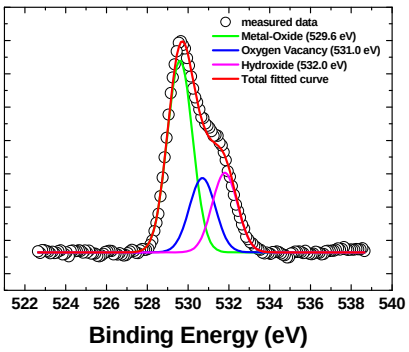
Figure 4.7 (a) Transfer characteristics of solution-processed IGZO TFTs with various metallic composition ratio, and output characteristics of solution-processed IGZO TFTs with In:Ga:Zn ratio of (b) 7:1:4, (c) 6:2:4, and (d) 5:3:4.

Table 4.3 Electrical characteristics of solution-processed IGZO TFTs with different metallic composition ratio

In:Ga:Zn	7:1:4	6:2:4	5:3:4
V_{on} (V)	-11.24	-5.43	-0.08
μ_{FE} ($cm^2/V \cdot s$)	3.46	1.28	0.4
V_{th} (V)	-9.63	-3.9	1.09
S.S. (V/dec)	1.033	0.549	0.497
I_{on}/I_{off}	2.3×10^5	3.8×10^5	2.3×10^5



(a)



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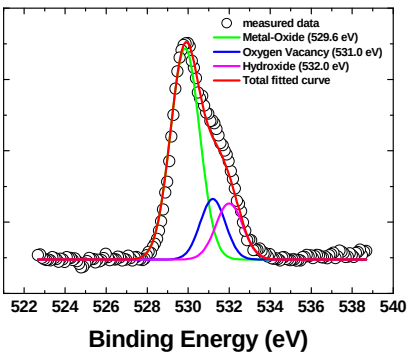


(c)

Figure 4.8 O1s XPS spectra of solution-processed IGZO film composed of different In:Ga:Zn ratio of (a) 7:1:4, (b) 6:2:4, and (c) 5:3:4.

Table 4.4 Bonding ratio of solution-processed IGZO film with different metallic composition ratio

In:Ga:Zn	Metal-Oxide	Oxygen Vacancy	Hydroxide
7:1:4	44.0 %	31.0 %	25.0 %
6:2:4	55.2 %	21.9 %	22.9 %
5:3:4	67.0 %	16.6 %	16.4 %

4.4.2 DOS Extraction Considering Back Channel Surface Potential and Analysis

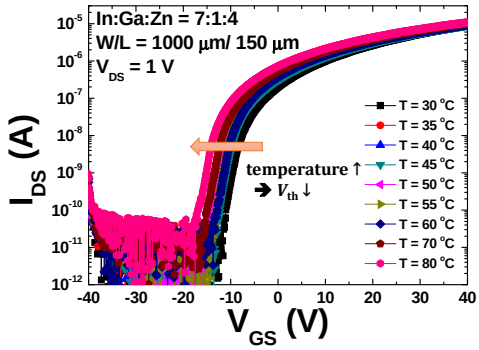
The DOS of each devices is extracted by the modified field-effect method developed in Chapter 3. Before extracting DOS, it is required to confirm that the fabricated devices exhibit thermally activated characteristics and follow MN rule. In order to verify the characteristics of devices at various temperature, the transfer characteristics were measured by changing temperature from 30 to 80 ℃. Temperature-dependent transfer characteristics were shown in Figure 4.9. All samples show thermally activated characteristics, that is, transfer curves are negatively shifted as temperature increases. This negatively shifted transfer curves at higher temperature can be explained by the thermally activated electrons from localized states to conduction band and generated defects acting as donors [46-47, 54-55, 77-79]. Figure 4.10 shows Arrhenius plot and the inset shows graph of E_a vs V_{GS}. It is also verified that the fabricated devices show thermally activated characteristics as following equation (4.1). In the inset of Figure 4.10, both fitting results based on the conventional (dashed line) and the modified field effect method (solid line) are presented with the measured data (dot). In all samples, the modified field-effect method with the consideration of the back channel surface potential (Φ_B) exhibits better fitting result than the conventional method. On the other hand, the deviation between the measured data and the fitted curve by

conventional field-effect method is reduced as indium ratio increases. It can be explained by the variation of Debye length with different carrier concentration. Because more carriers can react the applied electric field, the Debye length is reduced with higher carrier density and the effect of V_{GS} on the Φ_B is also reduced. As a result, it is expected that in the case of higher carrier density, the variation of Φ_B along with V_{GS}, and thus the deviation between the measured data and the fitted result based on the conventional method are reduced. However, these fitting results also support that more accurate DOS of solution-processed IGZO TFTs can be extracted by the modified field-effect method with consideration of Φ_B. The extracted DOS is presented in Figure 4.11. When indium ratio increases, E_F is closed to E_C, and both tail and relatively deep states increase. The origins of tail and deep states are investigated by comparing the variation of DOS with the change of chemical bonding ratio. As a result, it is concluded that the deep and tail states are related to oxygen vacancies and residual hydroxides in solution-processed IGZO TFTs, respectively. The electrical characteristics as the change of metallic composition ratio can be explained by the variation of DOS.

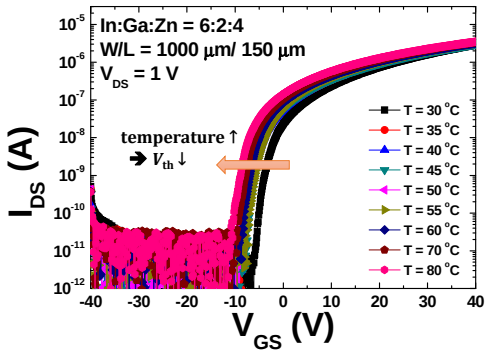
The decrease of V_{on} and V_{th} with the increase of indium ratio is related to the location of E_F. In n-type TFT operation, sufficient electrons need to be accumulated to form electrical channel. When positive V_{GS} is applied to gate electrode, band bending is occurred and E_F is moved to E_C. Then, electrons are activated from localized states

to conduction band and the probability that electrons exist at the states in conduction band is increased. When electrons are sufficiently accumulated, drain current starts to flow through the electron channel. Because the amount of the accumulated electrons can be roughly estimated by equation (4.2), sufficient electrons can be accumulated at lower V_{GS} when E_F is closed to E_C at unbiased state. Therefore, V_{on} and V_{th} are reduced when indium ratio increase. It can be also explained based on the turn-off mechanism of IGZO TFTs. The n-type semiconductor with smaller energy difference between E_F and E_C has more intrinsic carrier density, because the carrier concentration in semiconductor layer can be expressed by the energy difference between E_F and E_C as equation (4.2) in general semiconductor physics. Although the E_F of devices with In:Ga:Zn of 6:2:4 and 5:3:4 is located at similar energy level, it is expected that solution-processed IGZO TFTs with In:Ga:Zn of 6:2:4 have higher carrier concentration because of larger deep states related to oxygen vacancy acting as donor [54]. Since IGZO TFT is turned-off by fully depleting active layer, larger carrier concentration means that more negative V_{GS} is required for off state. Thus, solution-processed IGZO TFTs having higher indium ratio exhibit lower V_{on} and V_{th}. The improvement of μ_{FE} with high indium ratio can be also explained by high carrier density. Because electron conduction in IGZO TFTs can be described by percolation conduction, high μ_{FE} can be achieved by high carrier concentration [59-61]. On the other hand, it is required to explain the reason why solution-processed IGZO TFTs having high

gallium ratio and low tail states exhibit low μ_{FE}, though tail states inhibit carrier conduction. Although overall tail states of devices with high gallium ratio are lower than those with high indium ratio, both devices exhibit similar defect level at E_C. Because the effect of tail states on the electron transport increases as the tail states are located closer to E_C, the difference of overall tail states profile cannot affect dominantly the carrier conduction property. It can be also expected that the tail states are preoccupied by excess carriers in the case of high indium ratio and the effect of tail states on μ_{FE} is reduced. In addition to V_{on}, V_{th} and μ_{FE} variation, I_{off} variation is also explained by the extracted DOS. In Figure 4.7 (a), it is observed that solution-processed IGZO TFTs with higher indium ratio exhibit higher I_{off}. In previous reports, it is explained by high conductivity due to high carrier density. However, the explanation based on only carrier concentration is not sufficient since IGZO layer is fully depleted in off state. It can be related to the E_F pinning phenomenon of IGZO TFTs. When negative V_{GS} is applied to turn off the device, energy band of IGZO layer is bended and E_F is moved toward the valence band edge (E_V). However, E_F of solution-processed IGZO TFTs with high indium ratio is hard to move because there are large amount of deep states [80], and E_F is pinned at higher energy level than that of devices with low indium ratio. It results in high electron concentration in off state and high I_{off}. As analysis of I_{off} variation, the study of DOS extracted by the modified field-effect method allows more detail investigation of device characteristics.



(a)



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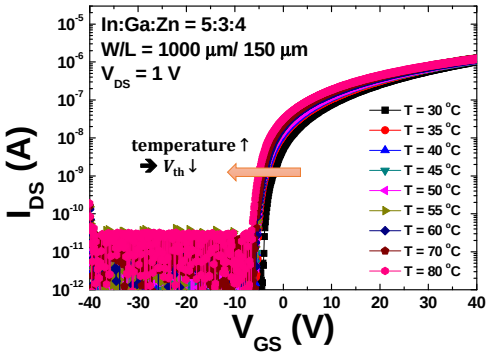
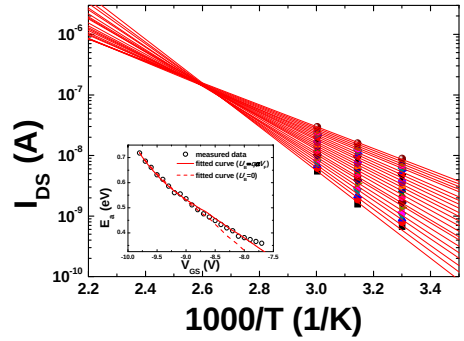
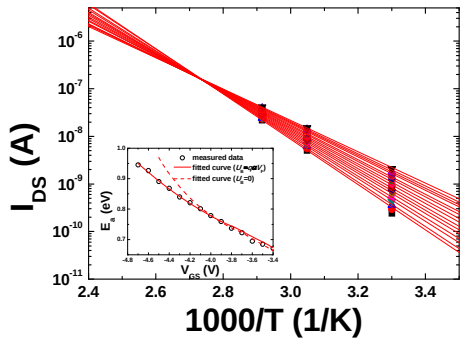


(c)

Figure 4.9 Temperature-dependent transfer characteristics of solution-processed IGZO TFTs with different In:Ga:Zn ratio of (a) 7:1:4, (b) 6:2:4, and (c) 5:3:4.



(a)



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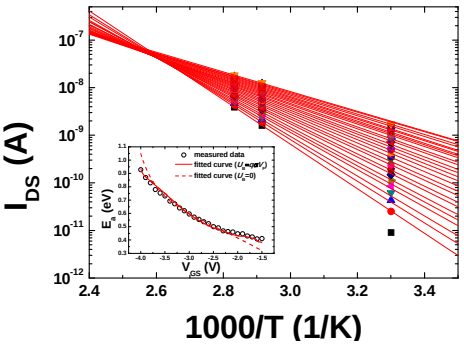


(c)

Figure 4.10 Arrhenius plot and (inset) the graph of E_a vs V_{GS} of solution-processed IGZO TFT with different In:Ga:Zn ratio of (a) 7:1:4, (b) 6:2:4, and (c) 5:3:4.

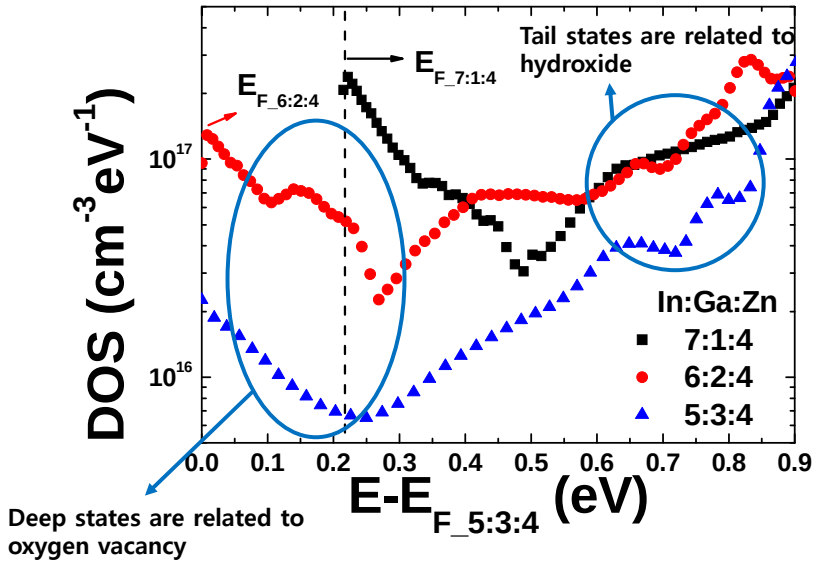


Figure 4.11 The extracted DOS of solution-processed IGZO TFTs with different metallic composition ratio. The origin of tail and deep states is analyzed based on the extracted DOS and XPS results of solution-processed IGZO TFTs with various composition ratio.

4.5 Effect of Active Layer Thickness on DOS of Solution-Processed IGZO TFTs

4.5.1 Device Characteristics

Three types of solution-processed IGZO TFTs were fabricated by changing t_{active} from 10 to 70 nm. The transfer characteristics of the fabricated devices are shown in Figure 4.12 and the representative electrical properties are summarized in Table 4.5. As t_{active} increases, V_{on} is negatively shifted and μ_{FE} is reduced. The V_{on} variation is related to the number of carrier. In IGZO TFTs, channel layer needs to be fully depleted in off state [58]. If the V_{on} is defined as the V_{GS} required to fully deplete channel layer, it is expressed as following equation [58],

$$\left|V_{on} - V_0\right| = \frac{qN_d t_{active}}{C_i} + \frac{qN_d t_{active}}{2\left(\varepsilon_0 K_S / t_{active}\right)}, \quad (4.3)$$

where V_0 is constant related to flat band voltage (V_{FB}); q is electronic charge; N_d is free electron concentration; C_i is gate capacitance per unit area; ε_0 is vacuum permittivity; and K_s is relative dielectric constant of IGZO layer. From equation (4.3), it is found that V_{on} is negatively shifted as the number of electrons increases. Because total number of free electrons increases with t_{active}, V_{on} is negatively shifted when t_{active} increases [58]. On the other hand, μ_{FE} is degraded as solution-processed IGZO layer become thicker. It is different behavior compared to vacuum-processed IGZO TFTs. In vacuum-processed IGZO TFTs, μ_{FE} is rarely affected by t_{active} [58]. The degradation of μ_{FE}

originates from the deposition process of solution-processed IGZO film. Since solvent is evaporated during formation of IGZO film based on solution process, solution-processed IGZO film has the physical defects, related to solvent evaporation, such as pin-holes and pores. Since gradual vaporization process is required to reduce the pores and pin-holes, the probability that these physical defects exist in the film is increased as t_{active} increases. Although these physical defects can be reduced by control thermal treatment process [83] or multi-stacking process [65], it is hard to completely remove these physical defects. In fact, in order to observe obviously the effect of these physical defects on electrical properties, t_{active} was controlled by changing molarity of precursor solution in this chapter and the optimized ramping process was not used in thermal treatment. The porosity of solution-processed IGZO film having different thickness is verified by x-ray reflectivity (XRR) measurement. Figure 4.13 shows the XRR result with different t_{active}. In XRR measurement, the density of film is related to the critical angle. As shown in Figure 4.13, the critical angle is increased as t_{active} decreases, indicating that the thicker solution-processed IGZO film has lower film density. The extracted film density of solution-processed IGZO film with t_{active} of 10, 20, 32, and 70 nm is 5.27, 4.38, 4.27, and 3.85 g/cm^3, respectively, and it is comparable value with previous reported results [65]. The lower film density of thick solution-processed IGZO film is attributed to the physical defects and disorder such as pin-holes, pores, and voids [65-67]. Since these physical defects can interrupt the electron

transport by acting as trap sites, μ_{FE} is reduced through trapping or scattering as t_{active} increases. The trend of μ_{FE} with change of t_{active} is similar result with previous reports [65-67].

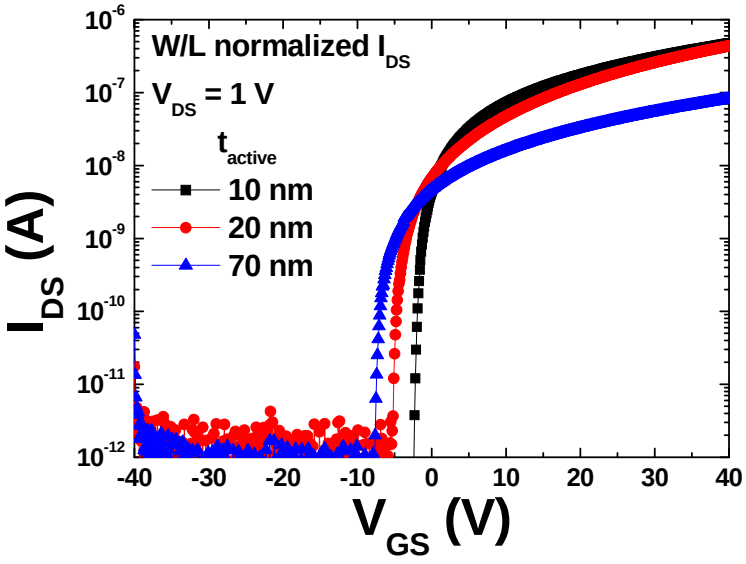


Figure 4.12 Transfer characteristics of solution-processed IGZO TFTs with different thickness of IGZO layer.

Table 4.5 Electrical characteristics of solution-processed IGZO TFTs with different t_{active}

t_{active} (nm)	10	20	70
V_{on} (V)	-2.29	-5.2	-7.48
μ_{FE} ($cm^2/V{\cdot}s$)	1.04	1.16	0.17
V_{th} (V)	-1.73	-4.62	-6.8
S.S. (V/dec)	0.203	0.259	0.373
I_{on}/I_{off}	6.1×10^5	1.2×10^5	1.3×10^4

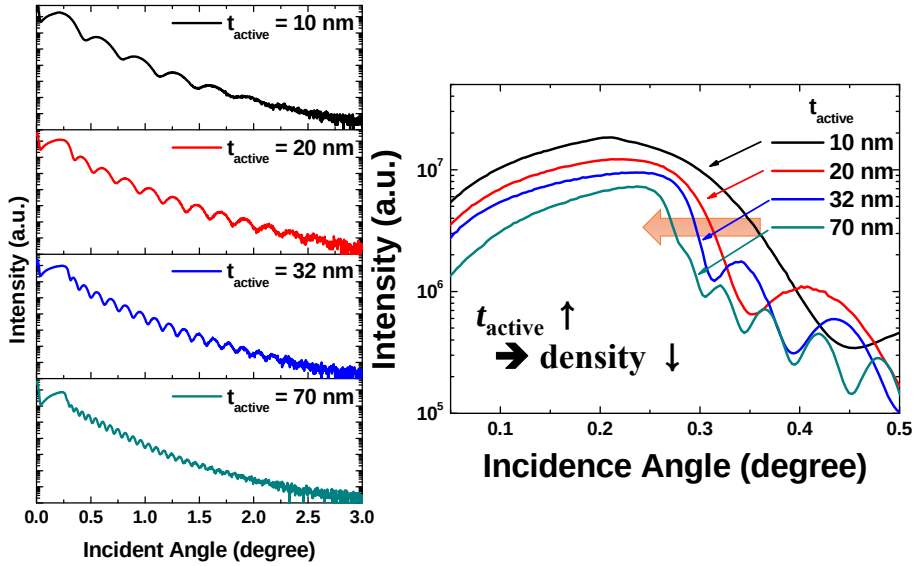


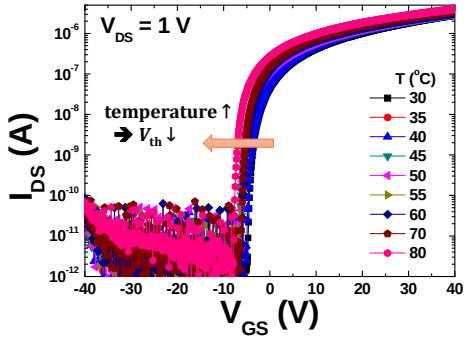
Figure 4.13 XRR results of solution-processed IGZO TFTs with different t_{active}.

4.5.2 DOS Extraction Considering Back Channel Surface Potential and Analysis

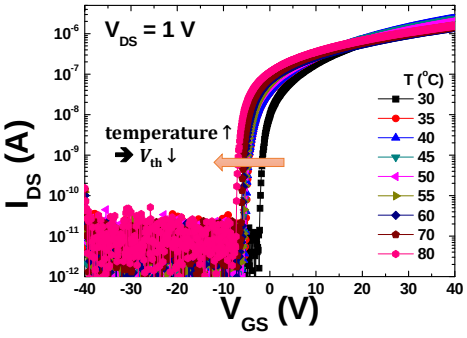
The DOS distribution of the fabricated devices having various t_{active} of 10, 20, and 70 nm is extracted by the modified field-effect method developed in Chapter 3. Before the extraction of DOS, thermally activated characteristics of the devices were verified by measuring the transfer curves at various temperature ranging from 30 to 80 ℃. The measured temperature-dependent transfer characteristics are shown in Figure 4.14. All devices show thermally activated characteristics, that is, transfer curves are negatively shifted as the increase of temperature. As mentioned in previous chapters, it is related to the thermally excited electrons from the states to conduction band and the generation of defects which can act as donors [46-47, 54-55, 77-79]. The thermally activated characteristics can be also confirmed by Arrhenius plot as shown in Figure 4.15. Based on the measured temperature-dependent characteristics, E_a is extracted by using equation (4.1). The inset of Figure 4.15 shows the measured E_a (dot) and the fitted curve using the conventional (dashed line) and the modified field-effect method (solid line) with the consideration of Φ_B. It is observed that the modified field-effect method exhibits more consistent fitting result with the measured data and the consideration of Φ_B needs to extract accurate DOS of solution-processed IGZO TFTs. It is also found that the deviation between the measured data and the fitted result using the

conventional field-effect method is reduced as t_{active} increases. Since the effect of V_{GS} on Φ_B is reduced when t_{active} increases, the difference between the fitted curves by conventional and the modified field-effect method become small as the increase of t_{active}. Figure 4.16 shows the extracted DOS profile of solution-processed IGZO TFTs with different t_{active} using the modified field-effect method. The tail states are increased as t_{active} increases, while the E_F and the deep states are rarely changed. Two properties can be considered as the origin of the variation of the tail states with different t_{active}. One is the uniformity of composition ratio in vertical direction and the other is the porosity of film. The composition ratio along the direction normal to interface between IGZO layer and gate insulator is measured by Auger electron spectroscopy (AES). However, significant difference is not observed as t_{active} changes and solution-processed IGZO films with various t_{active} show uniform composition ratio along vertical direction. As a result, it is expected that the most notable difference between solution-processed IGZO TFTs having different t_{active} is the film density, and thus porosity. As shown in Figure 4.13, the film density of solution-processed IGZO film is reduced as t_{active} increases, indicating that more defects such as pin-holes are contained in thick solution-processed IGZO film than thin one. By comparing the extracted DOS with XRR results of each device, it is concluded that the physical defects and disorder affect the tail states of solution-processed IGZO TFTs. That is, the physical defects and disorder including pin-holes, pores, and voids can be electrically modeled as

the tail states in band gap. The electron conduction through conduction band can be interrupted by the tail states below E_C by trapping process [74]. Consequently, the electrons transport property and μ_{FE} is degraded when large amount of tail state is located in band gap. The reduced μ_{FE} of solution-processed IGZO TFTs with thick active layer can be explained by the high defect level of tail state. On the other hand, above result of DOS analysis is the contrary to vacuum-processed IGZO TFTs. In vacuum-processed IGZO TFTs, the DOS including the tail states is decreased as IGZO layer become thick [84]. Although detail analysis of this result has not been performed, it may originate from the densification and highly packing of thick IGZO film. The different behavior of DOS with various t_{active} between vacuum- and solution-processed IGZO TFTs originates from the different mechanism of film formation. Therefore, it is required to extract and investigate accurate DOS to study the operation of solution-processed IGZO TFTs, although many researches for vacuum-processed device have been already reported.



(a)



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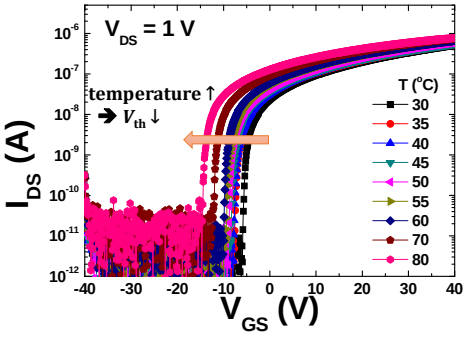
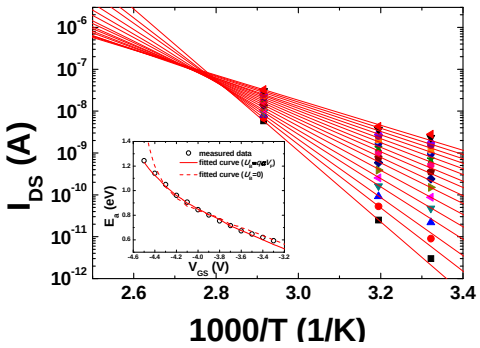
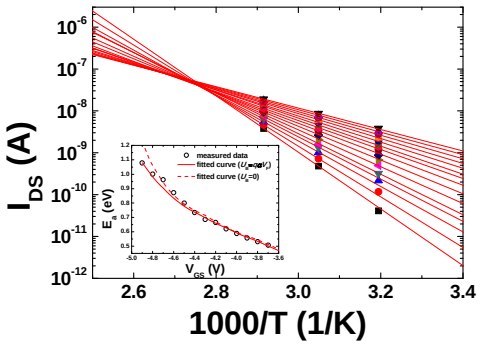


(c)

Figure 4.14 Temperature-dependent transfer characteristics of solution-processed IGZO TFTs with different t_{active} of (a) 10, (b) 20, and (c) 70 nm.



(a)



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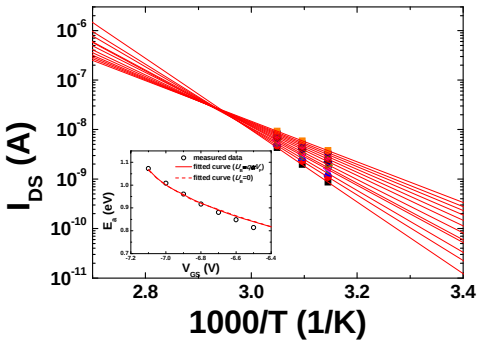


(c)

Figure 4.15 Arrhenius plot and (inset) the graph of E_a vs V_{GS} of solution-processed IGZO TFTs with different active layer thickness of (a) 10, (b) 20, and (c) 70 nm.

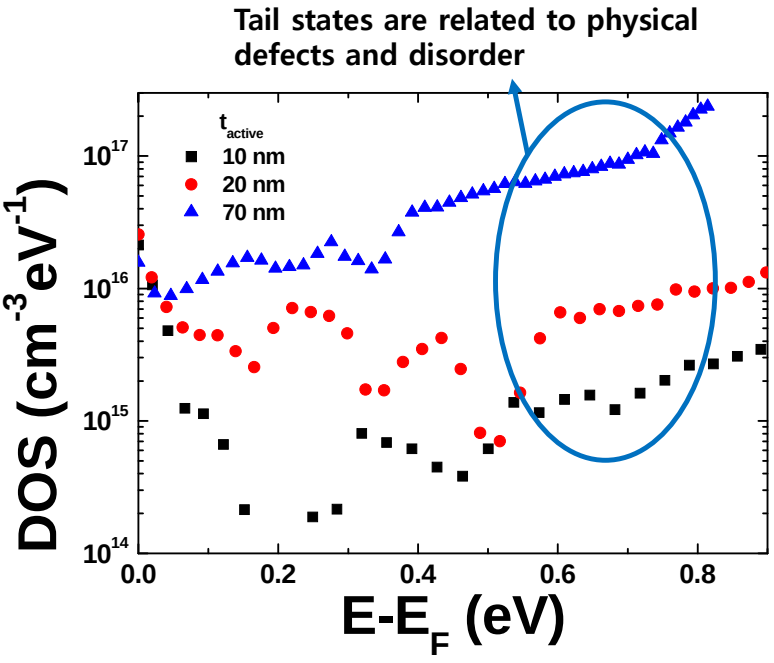


Figure 4.16 The extracted DOS of solution-processed IGZO TFTs with different t_{active}. The origin of defect stats is analyzed based on the extracted DOS and XRR results of solution-processed IGZO TFTs with various t_{active}.

4.6 DOS Mapping

Based on conclusions of Chapter 4.3, 4.4, and 4.5, the component of DOS profile of solution-processed IGZO TFTs can be related to the film properties such as chemical bonding and film porosity. The deep states are related to oxygen vacancy and the tail states are related to hydroxide, physical defects and disorder. Based on these findings, the DOS map, which shows the origin of each states, can be presented as Figure 4.17. Since each origin of DOS is related to process and device parameters such as T_a, metallic composition ratio, and t_{active}, this DOS mapping is helpful to optimize device performance and simulate device and circuit operation based on solution-processed IGZO TFTs in practical applications.

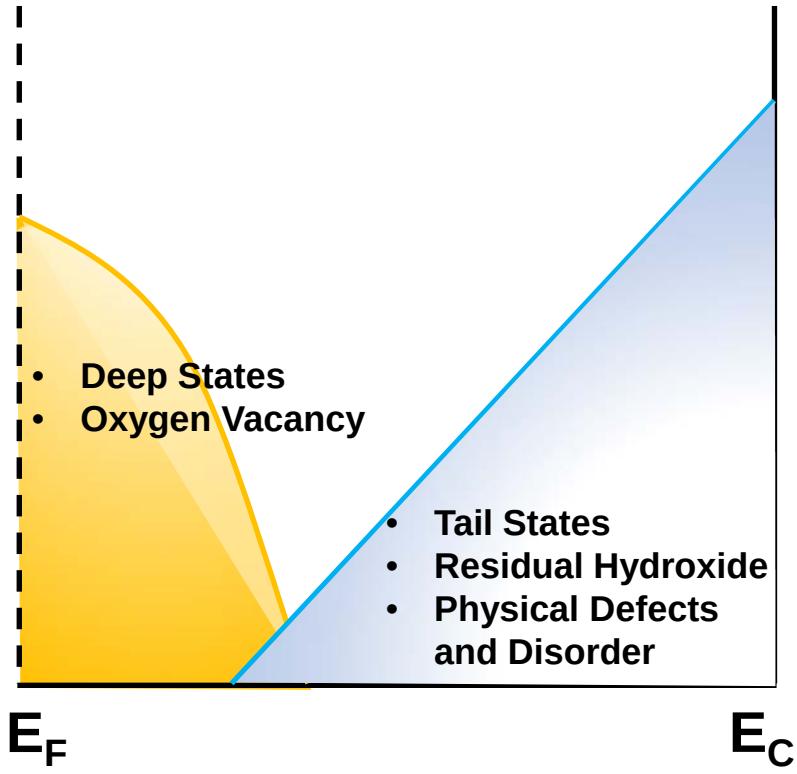


Figure 4.17 The DOS map, which shows the origin of each states, of solution-processed IGZO TFTs.

4.7 Conclusion

In this chapter, the defect DOS of solution-processed IGZO TFTs fabricated with different process and device parameters including T_a, metallic composition ratio, and t_{active} is extracted by the modified field-effect method with the consideration of Φ_B. Furthermore, since these process and device parameters affect the film properties including chemical bonding ratio and porosity, the origin of defect states is also investigated by comparing the extracted DOS with the result of film analysis. As a result, the deep states are attributed to oxygen vacancy and the tail states are related to residual hydroxides, physical defects and disorder. DOS map, which shows the origin of defects, is developed based on this relation. Since process and device parameters affect the chemical bonding and film properties of solution-based IGZO layer, the DOS map can be useful to improve device performance, simulate and optimize the device performance and circuit operation in many practical electronic applications.

Chapter 5 Analysis of Stability of Solution-Processed IGZO TFTs under Constant Gate Bias Stress

5.1 Introduction

The transistors used in circuit are exposed to constant gate or drain voltage during circuit operation. Therefore, the reliability of solution-processed IGZO TFTs under constant bias stress needs to be guaranteed for stable circuit operation. The threshold voltage (V_{th}) stability has been intensively investigated in the case of vacuum-processed IGZO TFTs [68-71]. There are three mechanisms to mainly explain the stability of metal-oxide semiconductor based TFTs, such as the charge trapping [68-69], the defect creation [70] and the ambient effect [71]. In the charge trapping mechanism, the V_{th}

instability is explained by the electrons trapped at gate insulator and/or interface between IGZO semiconductor and gate insulator [68]. Generally, the degradation of subthreshold swing (*S.S.*) is rarely observed in the charge trapping mechanism. In the defect creation mechanism, the V_{th} shift (ΔV_{th}) is attributed to the change of defect distribution in band gap of semiconductor layer [70]. The defect profile can affect the Fermi level (E_F) and the transition property from off to on state. In addition, if the created defects are charged states, the electric field distribution is also changed by the change of defect states. Consequently, V_{th} is affected by the variation of defect states. In general, the change of *S.S.* is simultaneously occurred when the defect creation is dominant degradation mechanism. In the ambient effect, the adsorption and desorption of molecules from the ambient air are the origin of the V_{th} instability. The degradation due to the ambient effect can be reduced by using effective passivation layer [71]. In this chapter the reliability of solution-processed IGZO TFTs with very thin active layer under constant positive or negative gate bias stress is investigated with the consideration of back channel surface effect. Especially, under negative gate bias stress, V_{th} was negatively shifted in linear function respect to stress time, different from vacuum-processed IGZO TFTs. The solution-processed IGZO TFTs with thick active layer or short Debye length exhibited ΔV_{th} of stretched exponential function under negative gate bias stress. It can be concluded that linear shift of V_{th} is related to the adsorption of positively charged species at the back channel surface.

5.2 Experiment

Overall fabrication process is similar to the introduced method in Chapter 3 and Chapter 4. The precursor solution was prepared by using indium acetate, gallium nitrate, and zinc acetate as solute, 2-methoxy ethanol as solvent, and ethanolamine as stabilizer. In fabrication of reference device, the molar ratio of indium, gallium and zinc was 3:1:2 and total concentration of precursor solution was 0.137 M. The mixed solution was stirred at 55 ℃ for 1 hour and aged at room temperature for 24 hours. For fabrication of solution-processed IGZO TFTs, the heavily doped p-type silicon and thermally grown silicon dioxide were used as gate and gate insulator, respectively. After cleaning process and UV-ozone treatment, IGZO semiconductor layer was deposited by spin-coating process and annealed at 500 ℃ for 1hour in the ambient air condition. Finally, aluminum source and drain electrodes were deposited by thermal evaporation. In all samples, IGZO semiconductor layer was patterned by conventional photolithography. For fabrication of solution-processed IGZO TFTs with different active layer thickness (t_{active}), the total concentration of precursor solution was changed from 0.137 to 0.685 M. The molar ratio of indium, gallium, and zinc was fixed at 3:1:2. For fabrication of solution-processed IGZO TFTs with different Debye length, the molar ratio of each component in precursor solution was changed as indium:gallium:zinc of 7:1:4 and total concentration is fixed at 0.137 M. Other fabrication process is same with the reference device.

5.3 Stability under Negative Gate Bias Stress

The stability of fabricated solution-processed IGZO TFTs under constant negative gate bias stress was measured by applying gate voltage (V_{GS}) of -20 V and drain voltage (V_{DS}) of 0 V. Figure 5.1 shows the evolution of transfer characteristics and V_{th} of solution-processed IGZO TFTs under negative gate bias stress. The V_{th} was negatively shifted as stress was progressed. The negative shift of V_{th} under negative gate bias stress is same with vacuum-processed IGZO TFTs, however, the shape of ΔV_{th} is different from previous reports. In previous reports, ΔV_{th} followed the stretched exponential function, which is described as equation (2.16). However, the fabricated solution-processed IGZO TFTs show negatively shifted V_{th} following linear function respect to stress time as shown in Figure 5.1 (b). In order to verify that it is not phenomenon observed in only early stage of stress, the stress time was extended to 50000 s and the linearly shifted V_{th} is also observed in the prolonged stress test. Therefore, it can be concluded that the observed abnormal ΔV_{th} is the intrinsic degradation characteristics of the fabricated solution-processed IGZO TFTs. As introduced in Chapter 2, when ΔV_{th} follows the stretched exponential or logarithmic function, the charge trapping or defect creation are regarded as the dominant degradation mechanism. However, since the fabricated device does not follow these functions, other degradation mechanism is required to explain ΔV_{th}. It is expected that the adsorption process at back channel surface and the

effect of adsorbed species on electron channel area may be enhanced in the fabricated solution-processed IGZO TFTs because of very thin active layer. Therefore, it is assumed that the ambient effect plays critical role in the linearly shifted V_{th} instability of the fabricated solution-processed IGZO TFTs. The positively charged species in the ambient air are attached to the back channel surface area of solution-processed IGZO TFTs by negative gate bias stress. Because the fabricated devices have very thin active layer of approximately 10 nm, the adsorbed positively charged species can affect the electron channel area. More specifically, electrons are pre-accumulated at the channel due to electric field induced by the attached positive charges and electron conduction channel is formed at lower V_{GS}, resulting in negative shift of V_{th}. It is required to verify that V_{th} can be linearly shifted by the adsorbed positive charges in order to support this degradation mechanism. First, the theoretical expression for the amount of adsorbed charged species are studied to verify this assumption. The rate of adsorption can be expressed as follow [85],

$$R_{ads} = S^{(\alpha)}(\theta) \cdot F, \tag{5.1}$$

where S, θ and F are the sticking coefficient, the adsorbate molecule coverage, which is defined as number of adsorbed molecules/number of adsorbed molecules in a complete monolayer, and the flux of the adsorbate molecule, respectively. The sticking coefficient can be expressed as follow,

$$S^{(\alpha)}(\theta) = \left(S^{(\alpha)}(0)\right) \cdot (1-\theta)^{\alpha}, \tag{5.2}$$

where $S^{(\alpha)}(0)$ is the sticking coefficient at zero coverage. If the coverage of adsorbed species is relatively low during stress time, it can be assumed that S is time invariant and constant during stress. Then, total amount of adsorbed positively charged species can be described as following equation,

$$N_{\text{ads}}(t) = \int R_{\text{ads}} dt = S \cdot F \cdot t\,, \tag{5.3}$$

where N_{ads} is the total amount of adsorbed positively charged species. Therefore, it can be concluded that the total number of adsorbed charged species is proportional to stress time. The 2-dimensional (2D) technology computer-aided design (TCAD) simulation using Silvaco ATLAS is performed to investigate the effect of adsorbed charges on the ΔV_{th}. The adsorbed positively charged species are modeled as the fixed charges at back channel surface area and the transfer curves are simulated by changing the amounts of the fixed charges. Figure 5.2 (a) shows the simulated energy band diagram and electron concentration with the fixed charge of 0 and 1×10^{12} cm^{-2}. In Figure 5.2 (a), it is found that the band bending is occurred and electrons are pre-accumulated by the fixed charges at back channel surface, resulting in the increase of electron concentration in IGZO semiconductor layer. Figure 5.2 (b) shows the simulated transfer curves and the extracted ΔV_{th} is presented in the inset of Figure 5.2 (b). The simulated transfer characteristics are negatively shifted as

the amount of the fixed charges increases. It is attributed to the band bending and pre-accumulated electrons due to the fixed charges. The band bending and pre-accumulated electrons mean that the Fermi level (E_F) is moved toward conduction band edge (E_C) before applying V_{GS} as shown in Figure 5.2 (a). Since n-type semiconductor based TFTs are turned on as E_F is moved to E_C, V_{on} is negatively shifted with the fixed positive charges at back channel surface. In the inset of Figure 5.2 (b), the ΔV_{th} is proportional to the amount of the fixed charges. From the simulation result, it is verified that the linearly shifted V_{th} under negative gate bias stress can be attributed to the adsorption of positively charged species at back channel surface region. Consequently, since the adsorbed charged species have proportional relation with stress time as equation (5.3), if the ambient effect is dominant mechanism in the degradation of solution-processed IGZO TFTs under negative bias stress, V_{th} is linearly shifted as stress is progressed.

For further investigation of the degradation mechanism related to the ambient effect, the V_{th} instability under negative gate bias stress was measured by using solution-processed IGZO TFTs having different t_{active} or Debye length. If the electric field induced by the absorbed charged species is the origin of the ΔV_{th}, the ambient effect is reduced by increasing distance between electron channel area and the attached charges. In a similar way, the ambient effect can be decreased by shortening the effective range of the absorbed charges.

Therefore it is expected that the ambient effect is reduced in solution-processed IGZO TFTs with thick active layer and short Debye length and the shape of ΔV_{th} is changed from linear to stretched exponential function respect to stress time.

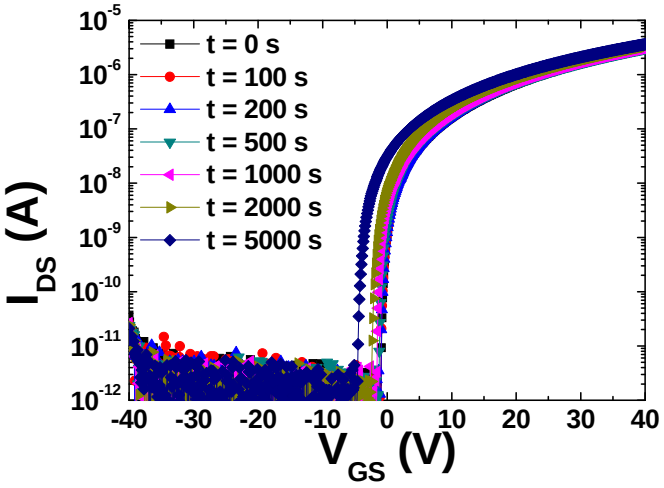
Figure 5.3 (a) shows the ΔV_{th} of solution-processed IGZO TFTs with t_{active} of 10 and 70 nm. Since the V_{on} is different as $t_{active\ changes}$ as investigated in Chapter 4, the difference between V_{on} and negative stress bias ($V_{GS,ST}$) is fixed at 20 V. When t_{active} increases, V_{th} is negatively shifted following stretched exponential function, not linear function. Since the effect of the applied $V_{GS,ST}$ on back channel surface area is reduced, the number of the attached positively charged species is also decreased when t_{active} is increased. Furthermore, channel region is less affected by adsorbed positively charges at back channel surface area because of the increased distance between electron channel and the adsorbed charges. Consequently, the effect of the adsorption of positive charges at back channel surface is reduced and other mechanism such as charge trapping become dominant, resulting in ΔV_{th} does not follow linear function but stretched exponential function.

Figure 5.3 (b) shows the ΔV_{th} of solution-processed IGZO TFTs with different metallic composition ratio. The V_{th} is not linearly shifted as bias stress is progressed, but ΔV_{th} follows stretched exponential as indium ratio increases. As mentioned in Chapter 4, intrinsic carrier concentration increases when indium ratio increases. When intrinsic

carrier density increases, Debye length is reduced because it is described as following equation in off state [60],

$$l_{\mathrm{D}} = \sqrt{\frac{\varepsilon_{\mathrm{IGZO}}}{q^2\left(N_{\mathrm{S}} + \frac{N_{\mathrm{D}}}{kT}\right)}}, \tag{5.4}$$

where l_{D}, $\varepsilon_{\mathrm{IGZO}}$, q, N_{S}, N_{D}, k, and T are the Debye length, the permittivity of IGZO, the electronic charge, the average amount of valence band deep states, the amounts of intrinsic carrier, the Boltzmann constants, and the temperature, respectively. When Debye length is decreased, the electrical effect, including band bending and pre-accumulation of electrons, of the adsorbed positively charged species on the channel area is reduced. That is, V_{th} is less affected by the attached charges. In addition, the amount of absorbed molecules can be also decreased, because of the reduced attraction force, resulted from the less electric potential induced by V_{GS} at back channel surface. Therefore, the effect of adsorbed positively charged species on channel formation is reduced. As a result, ΔV_{th} does not follow linear function but follows stretched exponential function. From the above analysis, it can be concluded that the linearly shifted V_{th} of solution-processed IGZO TFTs under negative bias stress is attributed to the reaction related to the ambient molecule at back channel surface region.



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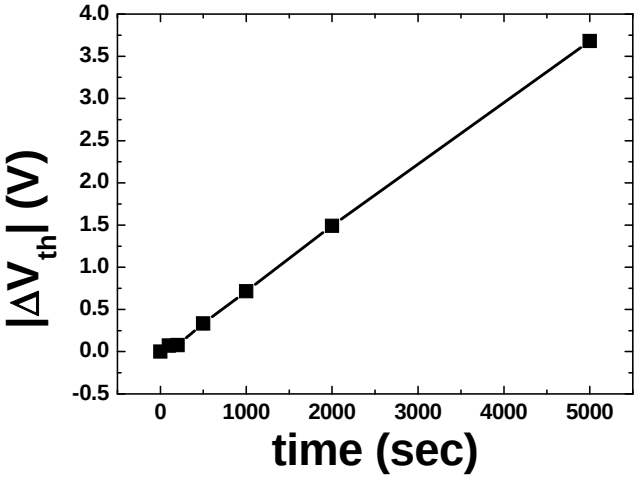
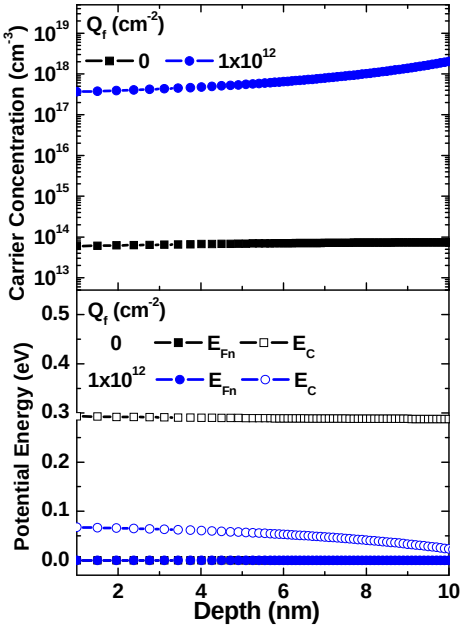


(b)

Figure 5.1 The evolution of transfer characteristics and ΔV_{th} of solution-processed IGZO TFTs under negative gate bias stress of -20 V.



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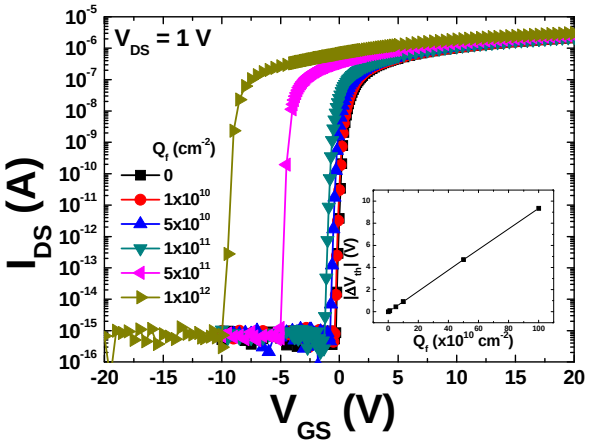
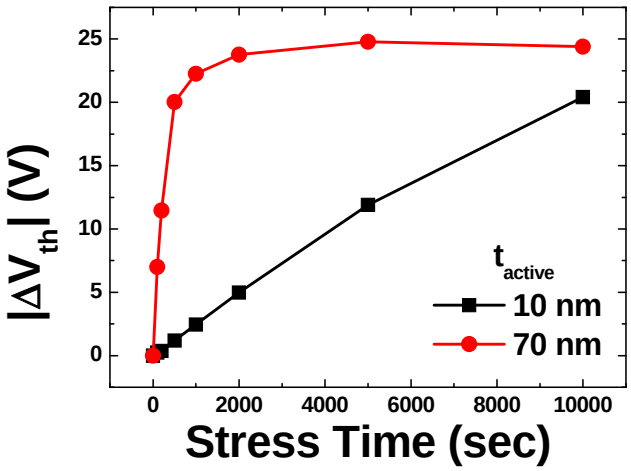


(b)

Figure 5.2 (a) The energy band diagram and carrier concentration of the simulated device with the fixed charge of 0 and 10^{12} cm^{-2} and (b) the simulated transfer characteristics and (inset) the extracted ΔV_{th}.



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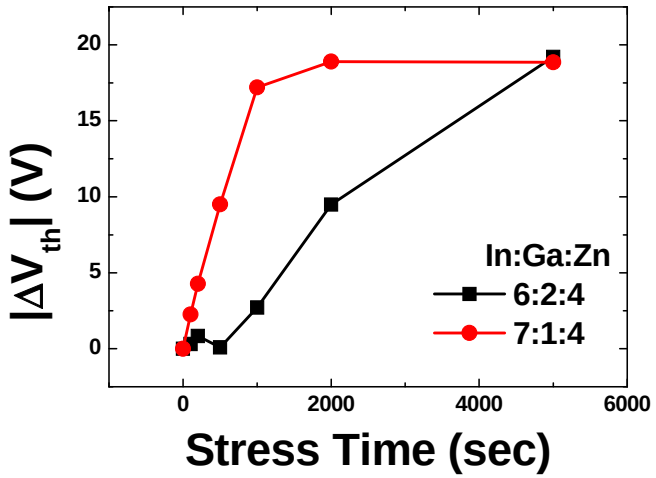


(b)

Figure 5.3 The amounts of ΔV_{th} of solution-processed IGZO TFTs with (a) t_{active} of 10 and 70 nm and (b) metallic composition ratio (In:Ga:Zn) of 7:1:4 and 6:2:4 under negative gate bias stress.

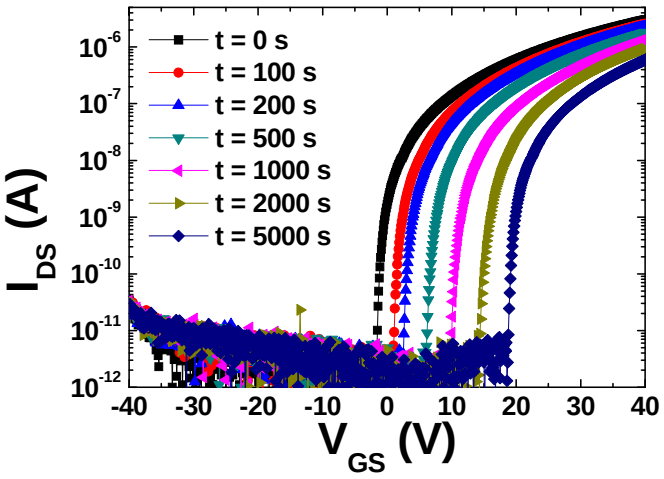
5.4 Stability under Positive Gate Bias Stress

The reliability of solution-processed IGZO TFTs under constant positive gate bias stress is measured by applying V_{GS} of 20 V and V_{DS} of 0 V. Figure 5.4 shows the evolution of transfer characteristics and V_{th} of solution processed IGZO TFTs under positive gate bias stress. The V_{th} was positively shifted and ΔV_{th} followed stretched exponential function (fitted line in Figure 5.4 (b)). It is the similar result compared to the vacuum-processed IGZO TFTs [68-69]. Since the ΔV_{th} follows stretched exponential function, the charge trapping or defect creation can be thought to be the dominant degradation mechanism [69]. Furthermore, because *S.S.* is rarely changed under positive gate bias stress, it is concluded that the defect creation is not dominant mechanism in this case. The V_{th} instability of solution-processed IGZO TFTs under positive gate bias stress is attributed to charge trapping at gate insulator and/or interface between gate insulator and IGZO active layer. The V_{th} instability of solution-processed IGZO TFTs having different t_{active} and Debye length is also measured as shown in Figure 5.5. Different from the reliability under negative gate bias stress, ΔV_{th} follows the stretched exponential function in all samples. It is required to explain the reason why the adsorption at back channel surface cannot dominantly affect the V_{th} reliability under positive gate bias stress. It can be explained by the large amount of electrons reacting to the positive gate bias stress. When positive gate bias stress is applied, abundant electrons are accumulated at the

interface between active layer and gate insulator, while active layer is depleted under negative gate bias stress. Therefore, the probability of charge trapping at the gate insulator and/or interface is increased. As a result, the charge trapping dominantly affect the V_{th} instability not the ambient effect. On the other hand, the more degraded behavior of device with thicker IGZO layer is attributed larger interface states. As mentioned in Chapter 4, the *S.S.* is degraded as t_{active} increases. It means that the solution-processed IGZO TFTs with thicker IGZO layer have larger amount of interface states because the maximum surface states can be expressed as follow [86],

$$N_{SS} = \left(\frac{S.S.log(e)}{kT/q} - 1 \right) \frac{C_i}{q}, \tag{5.5}$$

where N_{SS}, k, T, q, and C_i are the maximum density of interface states, Boltzmann constant, the temperature, the electronic charge, and the gate capacitance per unit area, respectively. Since there are more interface states, larger ΔV_{th} is observed in solution-processed IGZO TFTs with thicker IGZO layer.



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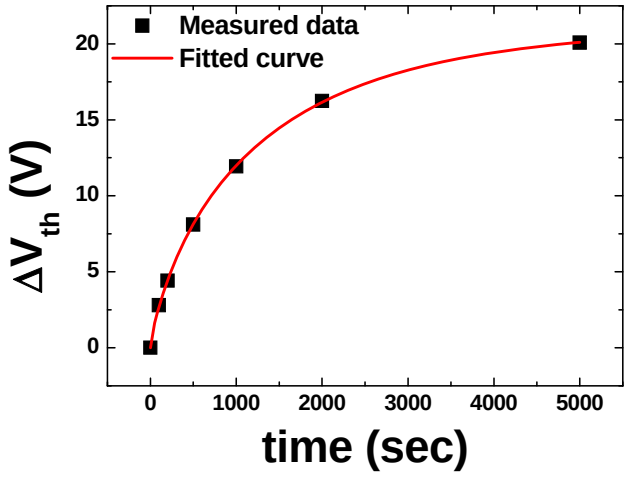
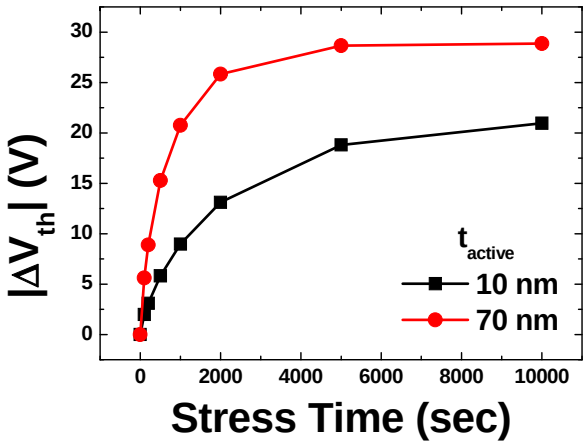


(b)

Figure 5.4 The evolution of transfer characteristics and V_{th} shift of solution-processed IGZO TFTs under positive gate bias stress of 20 V.



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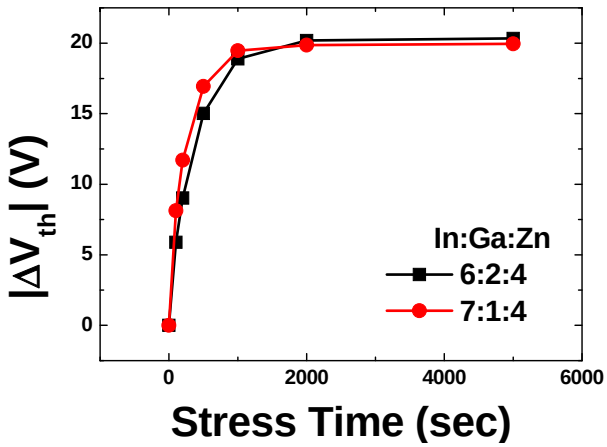


(b)

Figure 5.5 The amount of ΔV_{th} of solution-processed IGZO TFTs with different (a) t_{active} and (b) metallic composition ratio under positive gate bias stress.

5.5 Conclusion

In this chapter, the stability of solution-processed IGZO TFTs under constant gate bias stress is investigated. Solution-processed IGZO TFTs exhibit similar behavior under positive gate bias stress compared to vacuum-processed IGZO TFTs. However, different from previous reports, the V_{th} is linearly shifted respect to stress time under negative gate bias stress. To investigate this phenomenon, theoretical study of molecule adsorption on surface, 2D TCAD simulation, and stability analysis of devices with different t_{active} and Debye length were performed. As a result, it can be concluded that linear shift of V_{th} under negative gate bias stress is attributed to the adsorption of the positively charged species at the back channel surface from the ambient air by the applied gate bias stress. Therefore, the effect of back channel surface needs to be considered in the analysis of the reliability of solution-processed IGZO TFTs having thin active layer.

Chapter 6 Summary

In this thesis, the density-of-state (DOS) and the stability under constant gate bias stress of solution-processed IGZO TFTs are investigated with consideration of back channel surface potential and Debye length.

First, the DOS extraction method is developed with consideration of back channel surface potential (Φ_B) for extracting accurate DOS of solution-processed IGZO TFTs. Since Φ_B of solution-processed IGZO TFTs can be affected by the applied gate voltage (V_{GS}) due to very thin active layer of approximately 10 nm, the conventional field-effect method, which assumes zero potential at back channel surface, needs to be modified to extract accurate DOS of solution-processed IGZO TFTs. The variation of Φ_B as the change of V_{GS} is measured by

scanning Kelvin probe microscopy (SKPM) and properly modeled as linear function respect to V_{GS} based on the measured result. The conventional field-effect method is modified by applying the Φ_B model into the extraction procedure. The modified field-effect method exhibits more consistent results with the measured data compared to the conventional method. The accurate DOS of solution-processed IGZO TFTs is extracted by the modified field-effect method considering Φ_B, while it is found that the DOS is underestimated by conventional field-effect method. Since the thickness and DOS of the semiconductor layer in the metal-oxide semiconductor TFTs are directly related to their performance, accurate extraction of the DOS considering active layer thickness, and thus back channel surface potential, is very important to investigate the device physics, optimize the fabrication process and enhance the electrical performance of the solution-processed devices.

Second, the origins of tail and deep states of solution-processed IGZO TFTs were investigated by analyzing the variation of DOS extracted by the modified field-effect method as the change of process parameters. Solution-processed IGZO TFTs with different annealing temperature (T_a), metallic composition ratio, and the thickness of active layer (t_{active}) were fabricated to analyze the relation between DOS and process parameters. The DOS of each device was extracted and compared to the result of film analysis such as x-ray photoelectron spectroscopy (XPS) and x-ray reflectivity (XRR). When

T_a increases, the tail and deep states are decreased and increased, respectively. As T_a increases, oxygen vacancy and residual hydroxide in solution-processed IGZO film were increased and reduced, respectively. It can be concluded that the tail and deep states are related to residual hydroxide and oxygen vacancy in solution-processed IGZO layer, respectively. When indium ratio increases, both deep and tail states increase, and oxygen vacancy and residual hydroxide are also increased. By comparing the extracted DOS distribution with the change of bonding ratio, it can be concluded that the deep and tail states are related to the oxygen vacancy and residual hydroxide, respectively, and it is consistent result with the DOS analysis of devices annealed at different T_a. On the other hand, as the t_{active} increases, the tail states increase while deep states are rarely changed. The density of solution-processed IGZO film is reduced as the film thickness increases because thick film has more physical defects and disorder such as pin-holes, voids and pores. As a result, it can be concluded that the tail states are related to the physical defects and disorder of solution-processed IGZO layer. The DOS map, which shows the origins of each component of DOS, is developed based on the relation between DOS and film properties such as chemical bonding and film disorder.

Finally, the stability of solution-processed IGZO TFTs under constant gate bias stress was studied. In positive gate bias stress, V_{th} shift shows similar behavior compared to vacuum-processed IGZO TFTs.

However, V_{th} is negatively shifted with linear function respect to stress time under negative gate bias stress, different from vacuum-processed IGZO TFTs. The stability measurement of devices with different t_{active} and Debye length, and 2-dimensional (2D) technology computer-aided design simulation (TCAD) simulation are performed to investigate the degradation mechanism. When t_{active} increases and Debye length of IGZO film decreases, V_{th} shift follows the stretched exponential function, not linear function. As a result, it can be concluded that the linearly shifted V_{th} is attributed to the adsorbed positively charged species at back channel surface by applied negative gate bias stress. Since the solution-processed IGZO TFTs have very thin active layer, the potential distribution induced by adsorbed charges at back channel surface can affect the electron channel characteristics. Therefore, the effect of back channel surface needs to be considered in the reliability analysis of solution-processed IGZO TFTs having very thin active layer.

Appendix A Circuit Application of Solution-Processed IGZO TFTs

A.1 Introduction

In practical applications, TFTs are integrated in actual circuit and operated by DC or AC signal. The circuit application using metal-oxide semiconductor TFTs have been widely investigated [A1-A7]. Until now, the circuit applications of IGZO TFTs have been focused on demonstration of logic circuit such as inverter and ring oscillator. In addition, the shift register has been fabricated on glass substrate using TFTs to reduce fabrication cost. Because IGZO TFTs exhibit high electron mobility, the performance of shift register can be improved by employing IGZO TFTs. Furthermore, it is required to analysis and modeling of small signal to extend circuit application of solution-processed IGZO TFTs. In this chapter, small signal model and circuit application of solution-processed IGZO TFTs are investigated. Although high gain is not obtained in solution-processed IGZO TFTs based amplifier, the possibility of both digital and analog circuit application using solution-processed IGZO TFTs is observed. It is expected that the findings such as small signal modeling can be useful to simulate and develop the circuit based on solution-processed IGZO TFTs.

A.2 Experiment

For process compatibility, heavily doped p-type silicon with thermally grown silicon dioxide (SiO_2, 200 nm) was used as substrate. Aluminum/molybdenum (200 nm/10 nm) bilayer was deposited by

sputtering as gate electrode and patterned by photolithography and wet etching process. Tetraethly orthosilicate (TEOS) was deposited by plasma enhanced chemical vapor deposition (PECVD) as gate insulator. For formation of probing region, TEOS was patterned by photolithography and wet etching process. After annealing at 430 ℃ for 1 hour, IGZO layer and aluminum electrodes were deposited and patterned by same method in Chapter 3. IGZO layer was deposited by spin-coating process and annealed at 500 ℃ for 1 hour in the furnace. 150 nm-thick aluminum electrodes were deposited by thermal evaporation. IGZO layer was patterned by conventional photolithography and wet etching process. The fabrication process is summarized in Figure A.1.

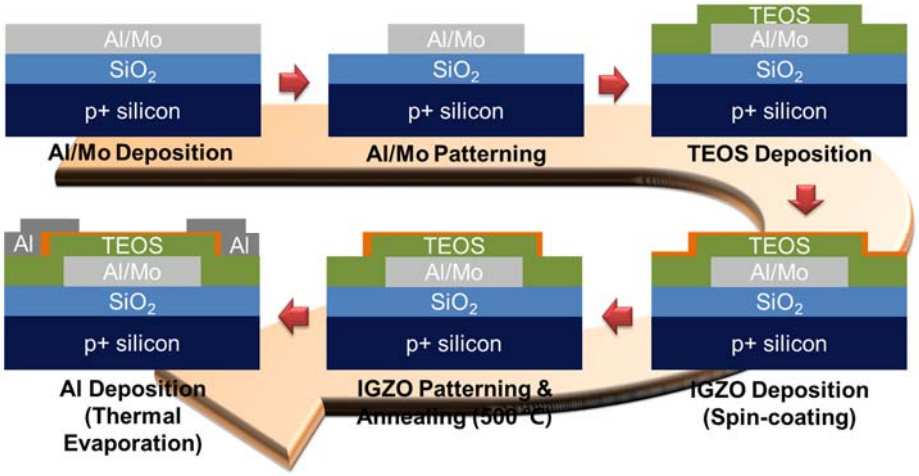


Figure A.1 Schematic diagram of the fabrication process of gate-patterned solution-processed IGZO TFTs.

A.3 Small Signal Modeling

The optical image, transfer, and output characteristics of the fabricated gate-patterned solution-processed IGZO TFTs is shown in Figure A.2. The fabricated solution-processed IGZO TFTs exhibit n-type TFT operation and hard saturation. The fabricated devices show a turn-on voltage of -0.9 V, a field effect mobility of 2.16 $cm^2/V{\cdot}s$, threshold voltage of 0.75 V, subthreshold swing of 0.29 V/dec and current on/off ratio of 7.5×10^5.

The small signal modeling of solution-processed IGZO TFTs was performed based on conventional small signal model of crystalline silicon based MOSFET. To extract transconductance (g_m) and output conductance (g_o), the transfer and output characteristics were measured by changing drain and gate voltage, respectively. g_m and g_o are extracted by following equations.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \tag{A.1}$$

$$g_o = \frac{\partial I_{DS}}{\partial V_{DS}}, \tag{A.2}$$

Figure A.3 shows the measured transfer and output characteristics and the extracted g_m and g_o. As V_{DS} increases, g_m is not affected by V_{DS}, but increases as only V_{GS}, since I_{DS} is affected by only V_{GS} in saturation region. The g_o is estimated by the minimum value at each gate voltage as a first order approximation [A8]. The output resistance r_o is obtained

by $(1/g_o)^{-1}$. The g_m needs to be modeled as a function of V_{GS} and V_{DS} in order to simulate device and circuit operation and design circuit. Because the carrier mobility of IGZO TFTs can increase as V_{GS} due to percolation transport, the g_m is modeled based on the mobility model of IGZO TFTs [60] as follow,

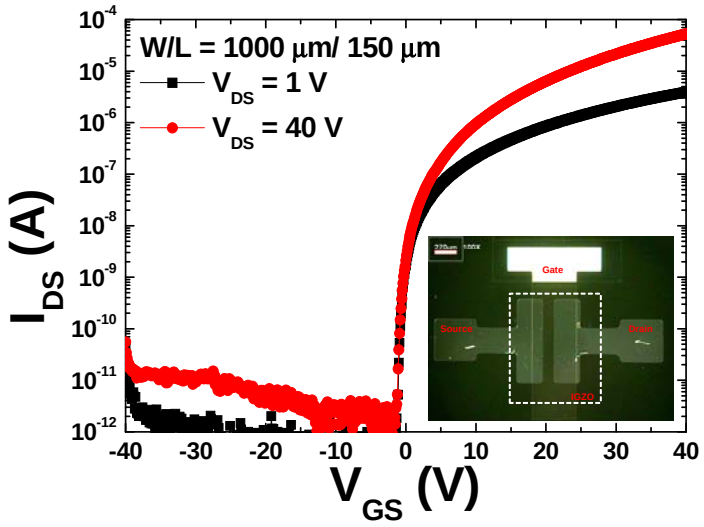
$$g_m = A \cdot exp\left(B + C \cdot ln\left(V_{GS}/D\right)\right), \quad \text{(A.3)}$$

where A is fitting parameter related to intrinsic mobility and device dimension parameters; B is fitting parameter related to the energy barrier of carrier transport; C and D are fitting parameters. Figure A.4 (a) shows the measured data and the fitted curve based on above equation (A.3). Although the model and the physical meaning of each parameter need to be more investigated, the measured data is well fitted by the model. On the other hand, it is expected that the g_m is linear function of V_{DS} in linear region while g_m is almost constant in saturation as discussed above. Figure A.4 (b) shows the graph of g_m vs V_{DS} with linearly fitted curve in linear region. The g_m is well fitted by the linear function of V_{DS}. Consequently, the g_m can be modeled as follow.

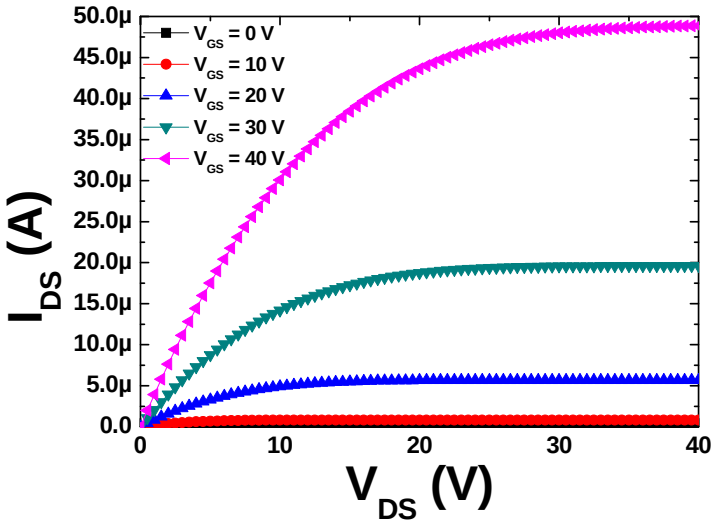
$$g_m = A \cdot exp\left(B + C \cdot ln\left(V_{GS}/D\right)\right) \cdot V_{DS} \text{ in linear region,} \quad \text{(A.4)}$$

$$g_m = A \cdot exp\left(B + C \cdot ln\left(V_{GS}/D\right)\right) \quad \text{in saturation region,} \quad \text{(A.5)}$$

Although the model and physical meaning of each fitting parameters need to be more investigated and verified, it can be useful to develop the model of solution-processed IGZO TFTs for circuit simulation.



(a)



(b)

Figure A.2 (a) The transfer characteristics, (inset) optical image, and (b) output characteristics of gate-patterned solution-processed IGZO TFTs.

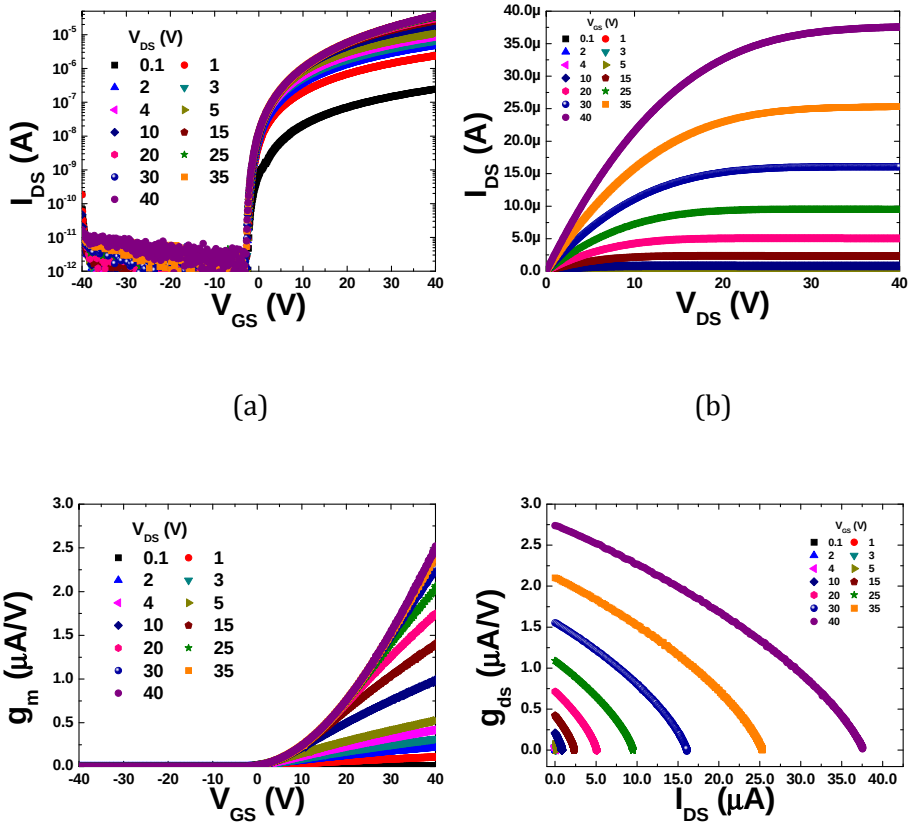
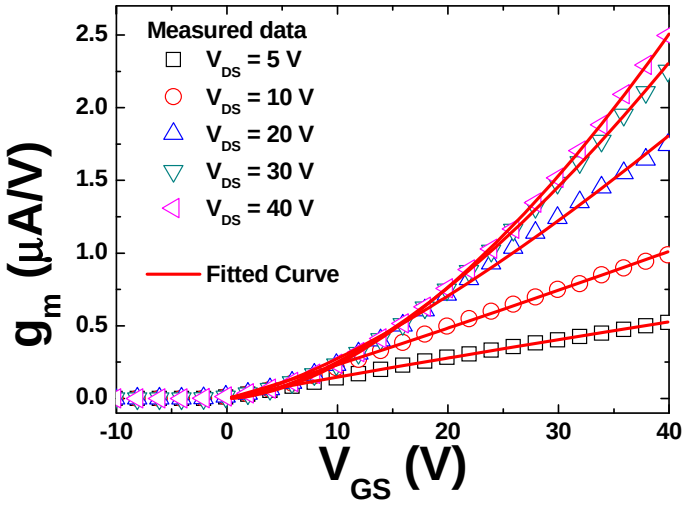
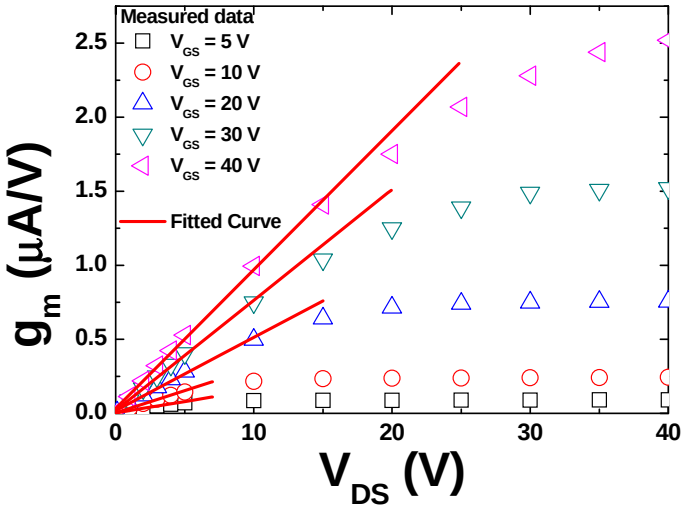


Figure A.3 (a) The transfer characteristics at various V_{DS}, (b) the output characteristics at various $V_{GS,}$ and the extracted (c) g_m and (d) g_o.



(a)



(b)

Figure A.4 The extracted g_m and the fitted curve as function of (a) V_{GS} and (b) V_{DS}.

A.4 Circuit Application

The common source amplifier with load transistor was fabricated using solution-processed IGZO TFTs. The circuit diagram is presented in Figure A.5 (a). The dimension of drive transistor (T1) and load transistor (T2) and is width/length (W/L) of 1000 μm/150 μm and 100 μm/200 μm, respectively. When both transistors are operated in saturation region, the gain is expressed as follow.

$$A_{\text{amp}} = \frac{g_{\text{m1}}}{g_{\text{m2}}} = \frac{\sqrt{2\mu_1 C_{\text{ox}} \frac{W_1}{L_1} I_{\text{DS}}}}{\sqrt{2\mu_2 C_{\text{ox}} \frac{W_2}{L_2} I_{\text{DS}}}} = \frac{\sqrt{\mu_1 \frac{W_1}{L_1}}}{\sqrt{\mu_2 \frac{W_2}{L_2}}}, \tag{A.6}$$

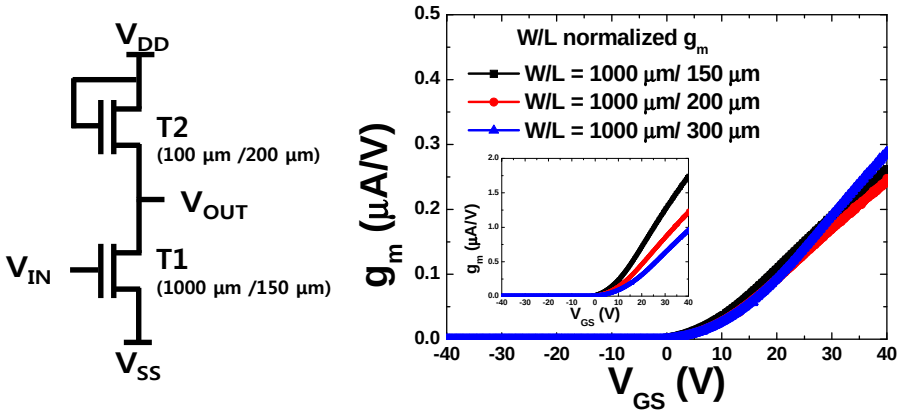
If field-effect mobility of each device is same, gain is described as follow.

$$A_{\text{amp}} = \frac{g_{\text{m1}}}{g_{\text{m2}}} = \frac{\sqrt{\frac{W_1}{L_1}}}{\sqrt{\frac{W_2}{L_2}}}, \tag{A.7}$$

This relation implies that the g_{m} of solution-processed IGZO TFTs is proportional to device dimension factor, W/L. For verifying this assumption, the g_{m} of devices with different W/L was estimated.

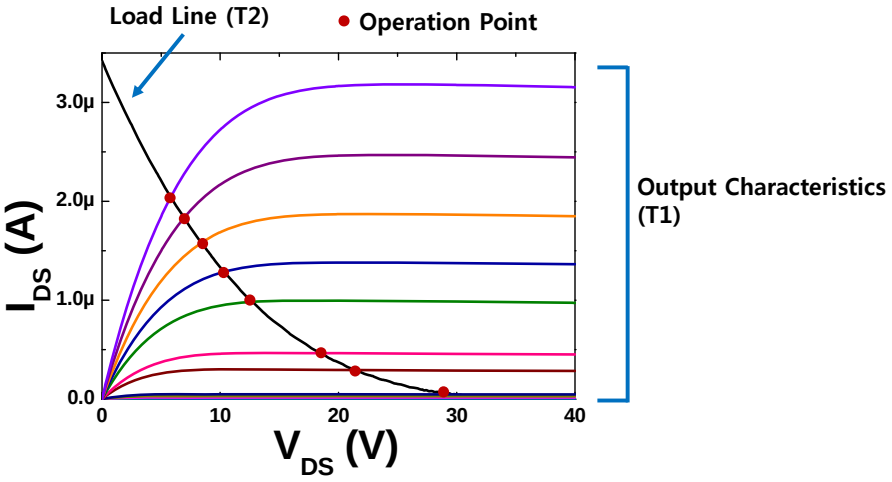
Figure A.5 (b) shows the estimated g_{m} of solution-processed IGZO TFTs with different W/L. When g_{m} is normalized by dimension factor (W/L), devices show similar g_{m} at same gate voltage. As a result, the gain of the fabricated device can be calculated by equation (A.7) as 3.65 V/V.

The operation point can be investigated by combining output curve of T1 and load line related to T2 as shown in Figure A.6 (a). In this measurement, V_{DD} and V_{SS} is set to 40 V and 0 V, respectively. The output voltage of operation point decreased since T2 is normally turn-on and output voltage is changed from V_{DD} to V_{SS} as T1 is turned-on by input voltage. Figure A.6 (b) shows the output characteristics of the fabricated amplifier with V_{DD} and V_{SS} of 40 V and 0 V, respectively. As expected in investigation of operation point, output voltage decreases as input voltage increases. From the measured output voltage, gain was extracted at each operation point as V_{DD} changes as shown in Figure A.7. The maximum gain is obtained as 3.10 V/V at input voltage of 4.1 V. Since this measured gain is similar with the calculated value of 3.65 V/V, it can be concluded that the device and circuit operation are modeled and estimated appropriately.

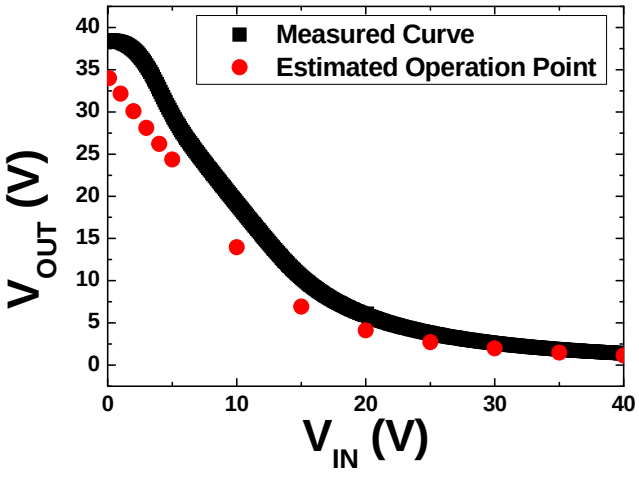


(a) (b)

Figure A.5 (a) The circuit diagram and (b) the extracted g_{m} normalized by W/L. (inset) The extracted g_{m} before normalization.

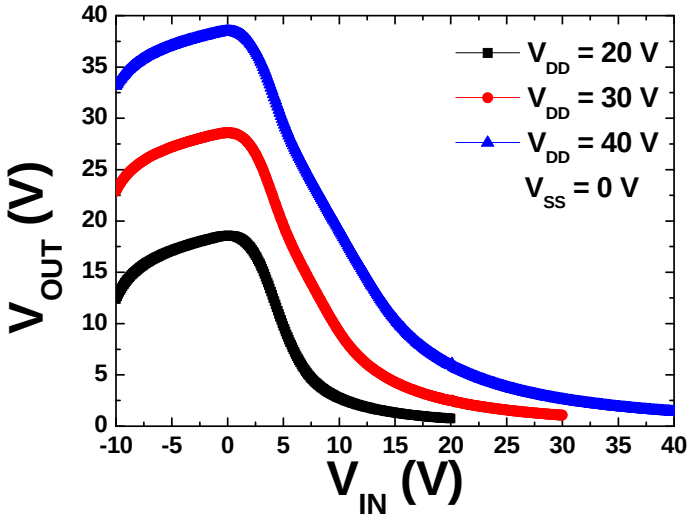


(a)

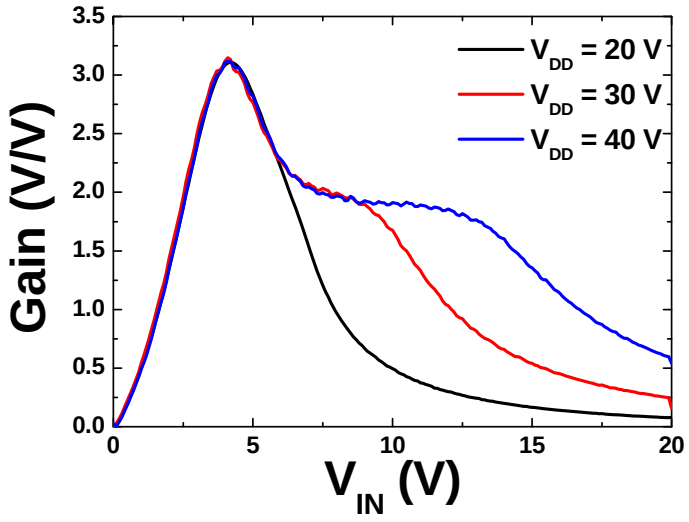


(b)

Figure A.6 (a) Output characteristics of T1 and load line from T2. (b) The measured and estimated operation point



(a)



(b)

Figure A.7 (a) The measured output voltage and (b) the extracted gain with various V_{DD}.

A.5 Conclusion

In this chapter, the small signal model and circuit based on solution-processed IGZO TFTs were investigated. The gate-patterned devices were fabricated and small signal model parameters such as g_{m} and r_{o} were estimated. The common source amplifier with load transistor was fabricated and the operation point and gain were estimated. The estimated value showed similar result with the measured data. Although more accurate modeling such as field effect mobility along with gate voltage needs to be investigated, the result of this chapter can be useful to apply solution-processed IGZO TFTs to various circuit.

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초록

차세대 디스플레이 응용의 핵심 소자로 비정질 산화물 반도체 박막 트랜지스터에 대한 관심이 높아지고 있다. 특히 비정질 인듐갈륨징크 산화물 반도체는 전하 이동도와 같은 전기적 특성, 균일도, 그리고 공정 온도 등에서 한계에 있는 기존의 실리콘 기반 박막트랜지스터를 대체할 수 있을 것으로 기대되고 있다. 이와 더불어 공정 비용 감소를 위해 용액 공정 기반의 인듐갈륨징크 산화물 반도체 박막 트랜지스터에 대한 연구도 많이 이루어지고 있다. 하지만 보다 많은 응용을 위해서는 용액 공정 기반 인듐갈륨징크 산화물 박막트랜지스터의 물리적인 성질에 대한 연구가 필요한 상황이다. 또한 뒷 채널 영역의 소자 특성에 대한 영향은 인듐갈륨징크 산화물 반도체 박막트랜지스터의 분석에서 간과되어 왔으나, 채널 특성이 뒷 채널 영역 특성의 영향을 받을 정도로 반도체 층이 얇을 때에는 뒷 채널 영역의 영향을 무시할 수 없게 된다. 일반적으로 용액 공정 인듐갈륨징크 산화물 반도체 박막트랜지스터의 경우 10~20 nm의 매우 얇은 반도체 층을 갖기 때문에 소자를 분석할 때에 뒷 채널 표면의 영향은 고려되어야 한다. 본 학위 논문에서는 용액 공정 인듐갈륨징크 산화물 박막트랜지스터의 결함구조밀도와 같은 소자 물리적 특성과 정전압 스트레스에서의 신뢰성을 뒷 채널 표면 전위와 드바이 길이를 고려하여 연구 하였다.

먼저, 용액 공정 인듐갈륨징크 산화물 박막트랜지스터의 결함구조밀도를 추출하는 방법에 대해 연구하였다. 기존에 발표된 결함구조밀도 추출 방법들은 뒷 채널 표면 전위를 0으로 가정하였다. 이는 인가되는 게이트 전압의 영향을 충분히 차폐할 수 있을 정도로 반도체 층이 두꺼울 때에는

적절한 가정이다. 하지만 반도체 층이 드바이 길이보다 얇은 경우에는 뒷 채널 표면 전위가 게이트 전압에 의해 영향을 받을 수 있다. 용액 공정 기반 인듐갈륨징크 산화물 박막 트랜지스터의 경우 약 10 nm 정도의 매우 얇은 반도체 층으로 인해 뒷 채널의 표면 전위가 게이트 전압에 의해 영향을 받을 수 있기 때문에 이러한 가정은 수정이 필요하다. 따라서 뒷 채널 표면 전위를 0으로 가정하고 있는 기존의 추출 방법들은 정확한 결함구조밀도 추출을 위해 뒷 채널의 표면 전위를 고려하여 수정될 필요가 있다. 게이트 전압에 따른 뒷 채널 표면 전위의 변화는 스캐닝 켈빈 프로브 마이크로스코피로 측정 하였으며 기존의 필드 이펙트 방법을 수정하는 데에 사용 될 수 있도록 모델링 하였다. 뒷 채널 표면 전위를 고려하여 새롭게 수정된 필드 이펙트 방법은 기존의 방법에 비해 측정된 활성화 에너지 데이터와 더 일치하는 결과를 보여주었다. 기존의 추출 방법에서는 결함구조밀도가 실제보다 작은 수준으로 추출되는 반면, 수정된 필드 이펙트 방법 통해 더욱 정확히 용액 공정 기반 인듐갈륨징크 산화물 박막 트랜지스터의 결함구조밀도를 얻을 수 있었다.

개발한 결함구조밀도 추출 모델을 이용하여, 어닐링 온도, 조성 비율, 그리고 인듐갈륨징크 산화물 반도체 층의 두께 등 공정 및 소자 파라미터가 결함구조밀도에 미치는 영향에 대해 연구하였다. 다양한 공정 파라미터에 의한 소자의 전기적 특성 변화에 대해 재료적인 관점에서의 분석은 이루어졌지만, 이를 결함구조밀도와 같은 전기적으로 모델링을 하고 분석하는 것에 대한 연구는 아직 이루어지지 않은 상황이다. 이러한 파라미터들의 변화에 의한 소자의 동작을 정확히 분석하고 예측하기 위해서는 결함구조밀도의 변화 등을 전기적으로 모델링 할 필요가 있다. 어닐링 온도와 조성 비율이 변화함에 따라 결함구조밀도의 상대적으로 딥

레벨에 위치하는 스테이트와 테일 스테이트가 변화하였으며, 엑스선 광전자 분광법 결과와 비교를 통해 상대적으로 딥 레벨에 위치하는 스테이트는 산소 공핍 결합과, 테일 스테이트는 잔여 수산화물 결합과 각각 관련이 있다는 것을 알 수 있었다. 또한 다양한 두께의 반도체 층을 갖는 용액 공정 기반 인듐갈륨징크 산화물 박막트랜지스터의 결함구조밀도를 분석, 비교함으로써 핀홀과 같은 물리적 결함과 불규칙성이 테일 스테이트에 영향을 준다는 것을 알 수 있었다. 이러한 분석을 바탕으로 용액 공정 기반 인듐갈륨징크 산화물 반도체 박막트랜지스터의 반도체 층 결함의 원인을 나타내는 결함구조밀도 맵을 얻을 수 있었다.

마지막으로, 정전압 스트레스에서의 용액 공정 인듐갈륨징크 산화물 박막트랜지스터의 신뢰성에 대해 연구하였다. 양의 게이트 전압 스트레스에서 문턱 전압은 양의 방향으로 이동하였으며, 진공 증착 기반 인듐갈륨징크 산화물 박막트랜지스터와 비슷한 양상을 보였다. 그러나 음의 전압 스트레스에서는 진공 증착 기반 인듐갈륨징크 산화물 박막트랜지스터와 달리 문턱 전압은 스트레스 시간에 따라 선형적으로 변화하였다. 이러한 열화 현상을 분석하기 위하여, 다른 반도체 층 두께와 드바이 길이를 갖는 소자의 신뢰성 측정, 그리고 흡착된 양 전하 물질이 소자의 전기적 특성에 미치는 영향에 대한 2차원 컴퓨터 시뮬레이션을 수행하였다. 그 결과, 음의 게이트 전압 스트레스에서 문턱전압이 선형적으로 이동하는 열화 현상은 공기 중의 양의 전하를 띄는 물질이 뒷 채널 영역에 흡착하는 것에 의한 것이라는 것을 확인 할 수 있었다.

주요어: 박막트랜지스터, 산화물 반도체, 결함구조밀도, 게이트 전압

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