공학박사학위논문

소용량 수동 소자와 직류단 보조 에너지 저장 회로를 가지는 교류 전동기 구동 시스템에 관한 연구

Study on AC Motor Drive System with Small Passive Components and Auxiliary Energy Storage Circuit in DC-Link

2015 년 8 월

서울대학교 대학원

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지도교수 하 정 익

이 논문을 공학박사 학위논문으로 제출함

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Abstract

In power conversion system, passive components such as grid filter inductor and DC-link capacitor have been widely used. However, they have several problems that they occupy too many spaces in the entire and an electrolytic capacitor which is commonly used in DC-link has a low reliability due to its high failure rate. To reduce or replace them, novel control methods or topologies using extra active devices with low-power-rating have been proposed, and these methods match to a trend of cost reduction of high-performance switching devices.

Hence this dissertation proposes control method for diode rectifier-fed system equipping small passive components and an auxiliary circuit called as DC-link shunt compensator (DSC). Owing to the absence of the electrolytic capacitor, the proposed structure is robust in terms of component failure. Moreover the diode rectifier-fed system using the proposed method can satisfy grid regulations such as IEC 61000-3-12 or -3-2 without power factor correction (PFC) or heavy grid filter inductor. The proposed method includes the grid current shaping and system operating methods which improve grid current harmonics and system performances, respectively.

This dissertation also presents implementation methods by using either motor drive inverter or DSC. The former is the most cost-effective way to realize proposed method but it necessarily degrades output performances such as torque quality and system efficiency. The latter requires auxiliary switching devices and small passive

components, but it has advantages in not only output performances but also system efficiency by cooperation of DSC. The proposed DSC operating strategy is presented in detail and corresponding design guideline is also provided.

In this dissertation, the DSC operating method is considered for both single- and three-phase diode rectifier-fed systems. In the case of the diode rectifier system using small passive components, the waveform of DC-link voltage is totally different in accordance with the gird phase, thus the corresponding control algorithms for both single- and three-phase inputs are also established respectively. This dissertation proposes each dedicated control method and discusses the feasibility. As a practical implementation example, boost converter is selected for the structure of DSC, and the validity of proposed methods are verified by simulation and experimental results.

Keywords : small DC-link capacitor system, DC-link shunt compensator, passive components, power factor correction, motor drive inverter.

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1 Introduction

1.1 Backgrounds and Motivations

Depending on the applicable equipment and system rated power, the power conversion systems should meet relevant various requirements. The requirements are usually established considering the system application environments such as input source and necessary output performance. Generally the power conversion systems which equip diode rectifier use passive components such as grid filter inductor and DC-link capacitor for satisfying system requirements.

In the case of grid connected system, the most important requirement is grid regulations such as such as Institute of Electrical and Electronics Engineers (IEEE) 519 or International Electrotechnical Commission (IEC) 61000 [1]-[5]. They indicate limit value of up to 40^{th} order harmonic in accordance with types of equipment, and compel the power conversion system to attenuate the harmonics into their corresponding limit value. In order to mitigate the harmonics, the grid filter inductor is generally used in most of power conversion system. The grid filter inductor have been evaluated as simple and reliable component, but its size and weight relatively take up large part of entire power conversion system [6]-[10].

Meanwhile, the DC-link capacitor plays a role of energy buffer absorbing

instantaneous power difference between the grid and the load. It regulates the DC-link voltage as smooth constant value and even performs temporary energy source when the grid is disconnected. As the DC-link capacitor, an electrolytic capacitor is commonly used due to its outstanding capacitance per unit volume. However, it has been verified that the high failure rate of the electrolytic capacitor causes a degradation of the system reliability, and many engineers have been investigated the methods for reducing or removing this low reliable component [11]-[55]. They usually replace it with the alternatives such as film and ceramic capacitors which have very small capacitance per unit volume in comparison with the conventional one. Hence, the diode rectifier system equipping alternatives in DC-link node is named as ‘small DC-link capacitor system’ or ‘reduced DC-link capacitor system’ [11]-[26]. In the previous researches, they are concerned about stabilizing the system which becomes unstable due to the reduced DC-link capacitance and negative impedance characteristic caused by constant power load (CPL) [11]-[20]. A key principle of the stabilization control is based on the neutralization of the negative impedance characteristic. This stabilization control can be realized by motor drive inverter or auxiliary circuit [27].

Recently, on the other hand, many researchers have found that the small DC-link capacitor system has another merit besides the implementation of high-reliable system [21]-[26][28][29]. The merit is that the system basically shows low grid

current harmonics because the DC-link capacitor current which primarily pollute the grid current harmonics is significantly decreased. In addition, the grid current harmonics are directly related with the output power when the diode rectifier is conducted. By using this factor, we can even have chance to reduce or remove the bulky and weighty component, grid filter inductor. In [21]-[26], the grid current shaping methods for single-phase diode rectifier system have been proposed and it is verified that the diode rectifier system can sufficiently satisfy the grid regulation without electrolytic capacitor and grid filter inductor. The concept of this control method is not proposed in three-phase diode rectifier system yet, and it will be feasible solution for realizing compact and cost-effective system.

1.2 Objectives

This dissertation proposes a grid current shaping method for three-phase diode rectifier-fed motor drive system. The proposed grid current shaping method based on current injection covers the absence of heavy grid filter inductor, and then the three-phase diode rectifier system can also meet the relevant grid regulation IEC 61000-3-12 without heavy passive components. The absence of heavy grid filter inductor even enhances the system stability which was a problem in the previous small DC-link capacitor system. This dissertation includes the operating principle

of the proposed method with the system stability verification, and analyzes the influence of the proposed method on both grid and motor drive system.

In both single- and three-phase system, if the grid current shaping method is implemented in the inverter without auxiliary circuit, the most cost-effective system can be realized. However, the inverter should secure extra voltage margin for this control method and suffers performance degradation such as output power ripple and total system efficiency reduction. To cope with these problems, this dissertation also proposes the operating method for the system equipping auxiliary circuit named DC-link shunt compensator (DSC) which is composed of small rating components without electrolytic capacitor. With a help of DSC, the entire motor drive system can establish various strategies to enhance system performances such as torque ripple or efficiency. A concept of the topologies introduced in [27] are similar with that of DSC system, but they have obvious difference in the way of control and grid harmonic compensation. The DSC system also differs from other conventional passive component reduction topologies that use power factor correction (PFC) together. The DSC system does not need PFC or filter inductor, thus the entire system can be miniaturized and cost-effective.

In this dissertation, the DSC operating method is dealt with in both three- and single-phase diode rectifier-fed systems. These two systems have different structure and DC-link voltage, thus the relevant operating strategies are totally distinguished

each other. Especially in single-phase system which has insufficient DC-link voltage, DSC strongly supports the motor drive inverter by boosting DC-link voltage and supplying compensation power in a certain duration called as grid-disconnection time. Under the condition that the grid regulation is satisfied, the operating methods for two systems are strategically suggested to improve their feasibility. Simulation and experimental results based on laboratory proto-type motor drive system demonstrate a validity of proposed method comparing with convention counterpart systems.

The conventional researches for the diode rectifier-fed small DC-link capacitor system and challenges that are discussed in this dissertation are summarized in Table 1.1.

Table 1.1 Diode rectifier-fed small DC-link capacitor system:
State of the art and challenges

		Three-phase	**Single-phase**
Stabilization control		[11]-[17]	[27]
Grid current shaping control		***Challenges***	[21]-[26]
Auxiliary circuit	**Stabilization control**	[27]	[27]
	Grid current shaping control	***Challenges***	***Challenges***

1.3 Dissertation Outlines

The outline of this dissertation is as following.

Section 1 presents the motivations and objectives of this research.

Section 2 reviews the purpose of passive components in the diode rectifier-fed motor drive system in detail. This section also analyzes the system constraint and system stability variation in the case that the passive components are reduced or removed. This analysis helps to comprehend main issues for the small DC-link capacitor system. The state of the art of conventional small DC-link system is also summarized, and the conventional systems with auxiliary circuit for reducing passive component are categorized and simply explained.

Section 3 suggests the operating method for three-phase diode rectifier-fed motor drive system with or without the DSC. The principle of proposed grid current shaping method for three-phase system is presented, and its effect on grid and motor is analyzed. The control methods implemented in either inverter or DSC are explained in detail and the design guideline for DSC is also included. To prove the feasibility of proposed methods, the simulations and experiments are conducted in comparison with conventional heavy passive components system and small DC-link capacitor system. The DSC system operating strategies are discussed in consideration of system cost, ripple torque, and efficiency.

The operating method for single-phase DSC system is suggested in Section 4. The grid current shaping method introduced in the conventional small DC-link capacitor system is presented and its limitation is discussed. This section provides the DSC operating method including DC-link boosting control and partial power assistance operation, and explains the corresponding control block diagrams. The DSC design consideration and design guideline are also discussed. Similar with in Section 3, the simulations and experiments are conducted to prove the validity of proposed DSC system in comparison with the conventional small DC-link capacitor system.

Conclusion and future works are given in Section 5.

2 Conventional Motor Drive System

2.1 Review of Motor Drive System with Passive Components

The motor drive systems have been commonly used in various applications such as home appliances, wind power generators, electric vehicles, and so on. Among many systems, three-phase motor and its driving circuit which perform variable speed control have been spotlighted as useful solution in terms of providing good operating efficiency and various control strategies. As the driving circuit, three-phase two-level inverter shown in Fig. 2.1 is most commercialized in every industry area, and has been demonstrated its reliability and feasibility [56]. The inverter synthesizes three-phase output voltages v_{an}, v_{bn}, v_{cn} by using three switching legs and DC-link voltage v_{dc}, and v_{dc} is provided by voltage sources like photovoltaic panel, battery, and grid voltage.

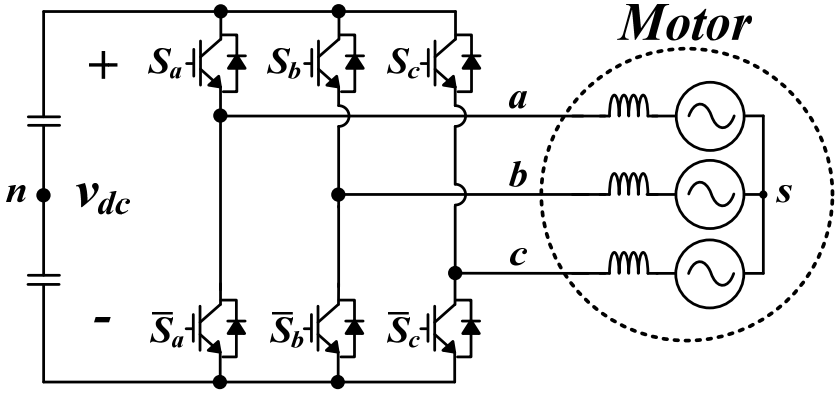

Fig. 2.1 Three-phase two-level motor drive inverter.

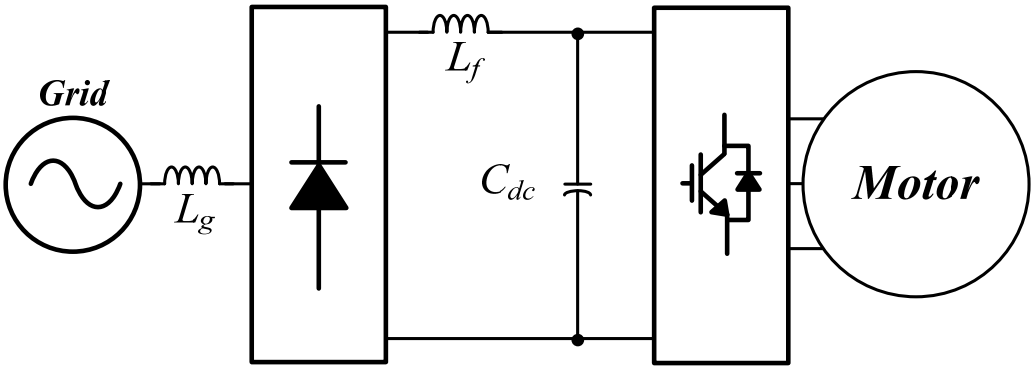

Fig. 2.2 Conventional diode rectifier system with passive components. (L_g: grid internal reactance)

Among them, the grid voltage is one of the easiest solution to utilize, and the diode rectifier system shown in Fig. 2.2 has widely used in the grid connected motor drive system owing to its simple structure and convenience controllability. The diode rectifier system usually uses passive components such as DC-link capacitor C_{dc} and grid filter inductor L_f in order to satisfy system performances. The passive components have merits in easy implementation, but they have several practical problems. In this subsection, the characteristics of passive components are presented, and their limitations are discussed.

2.1.1 DC-Link Capacitor

The purposes of the DC-link capacitor are as follows [11][28]:

■ DC-link voltage (v_{dc}) regulating

■ Switching ripple current absorbing

■ Temporary energy supplying under the grid fault condition

First, as mentioned above, since v_{dc} is used for synthesizing three-phase output voltages, at least v_{dc} should be kept higher than output voltages. Also, it is advantageous to secure v_{dc} as high as possible, but the voltage should be limited considering the maximum voltage rating of switching device. In the case of diode rectifier-fed system with steady state operation, v_{dc} becomes the value of line-to-line grid voltage filtered by L_f and C_{dc}. However, when the motor power is rapidly changed, instantaneous power difference between grid and motor causes variation of v_{dc}. Here, C_{dc} absorbs the power difference and mitigates v_{dc} variation. By using the Kirchhoff's current law (KCL) from Fig. 2.3, v_{dc} variation can be expressed as

$$\frac{dv_{dc}}{dt} = \frac{1}{C_{dc}}(i_{diode} - i_{inv}), \tag{2.1}$$

where i_{diode} is current from diode rectifier, and i_{inv} is average value of inverter current. From (2.1), as C_{dc} becomes larger, amount of the variation becomes smaller.

The second role of C_{dc} is absorbing switching ripple current. This switching ripple current, $i_{inv} + \tilde{i}_{inv}$, generated by the inverter is shown in Fig. 2.4 and

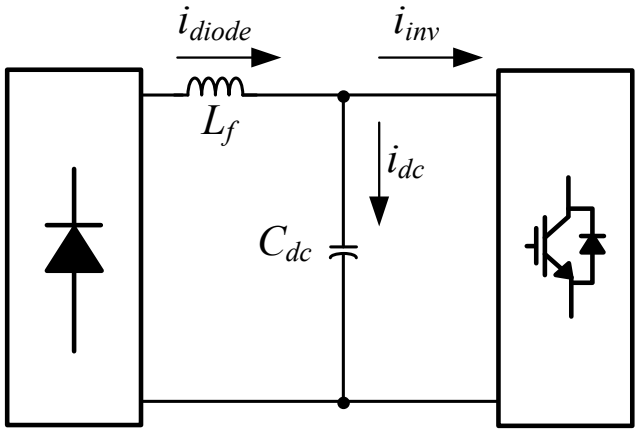

Fig. 2.3 Current flow at DC-link in diode rectifier system.

expressed as

$$i_{inv} + \tilde{i}_{inv} = S_a i_{as} + S_b i_{bs} + S_c i_{cs}, \tag{2.2}$$

where S_a, S_b, S_c are switching states of the inverter in Fig. 2.1 (Switch ON: $S_x = 1$, switch OFF: $S_x = 0$) and i_{as}, i_{bs}, i_{cs} are motor currents. From (2.2), $\tilde{i}_{inv}$ has shape of chopped waveform and is changed in accordance with motor operating condition. Of course, this ripple current causes ripple voltage in v_{dc} and we should select enough amount of C_{dc} considering switching frequency and motor side peak current. In addition, the allowable root mean square (rms) ripple current of practical capacitor is one of the important considerations. This switching ripple current is related with a lifetime of C_{dc}. Fig. 2.5 shows an example of the allowable rms switching ripple current of electrolytic capacitor which is commonly used for DC-

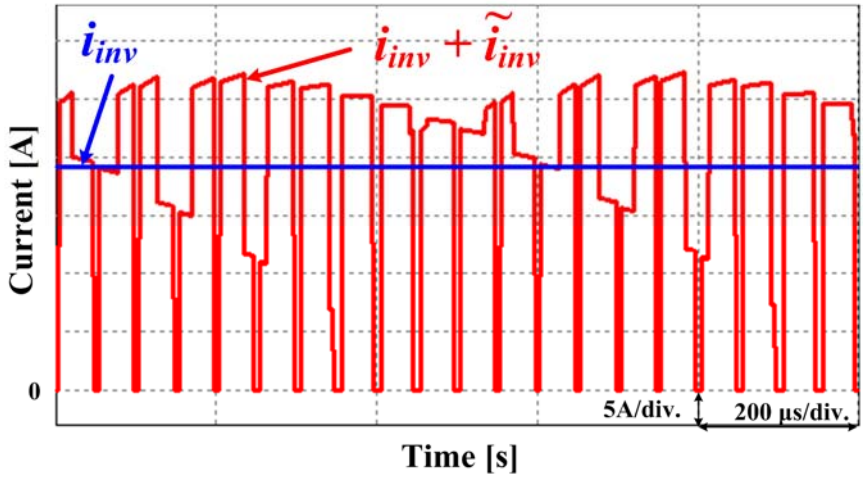

Fig. 2.4 Switching ripple current from the inverter.

link. As shown in this figure, the capable rms switching current of electrolytic capacitor is around 1 A_{rms} (2 A_{rms}) in the case of 100 μF (330 μF). Here, if rms value of $\tilde{i}_{inv}$ is around 10 A_{rms}, we should use at least more than 10 electrolytic capacitors of 100 μF or 5 electrolytic capacitors of 330 μF in order to guarantee expected lifetime of them. Then the total capacitance becomes 1000 μF or 1650 μF.

Lastly, C_{dc} should be designed considering that the system guarantees power supplying to the load when the grid is temporarily disconnected, i.e., a brief grid power interruption occurs. This time that the system is able to maintain supplying output power without grid power is called 'Hold-up time'. The hold-up time is normally required for power supplies and enables the load to keep operating without rebooting during the brief grid fault. Most of relevant applications generally provide

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HJ Snap-in Terminal Type, Series

Solvent Proof WV≦100V

· High voltage, high capacitance series
· Load life of 3000 hours at 85°C
· Complied to the RoHS directive

HC (Long life) ⇨ **HJ** ⇨ HK (Wide temp.)

WV / μF \ ØD	350				400				450			
	22	25.4	30	35	22	25.4	30	35	22	25.4	30	35
56									22×20 0.61			
68					22×20 0.65				22×20 0.71			
82					22×20 0.85				22×25 0.86	25.4×20 0.84		
100	22×20 0.80				22×25 0.99	25.4×20 0.82			22×25 0.95	25.4×25 0.97		
120	22×25 1.04	25.4×20 0.90			22×25 1.09	25.4×20 1.13			22×30 1.07	25.4×25 1.09	30×20 1.12	
150	22×25 1.20	25.4×25 1.22			22×30 1.24	25.4×25 1.27	30×20 1.20		22×35 1.18	25.4×30 1.25	30×25 1.29	
180	22×30 1.34	25.4×25 1.37			22×30 1.41	25.4×25 1.44	30×25 1.52		22×35 1.32	25.4×35 1.40	30×25 1.45	
220	22×30 1.47	25.4×30 1.53	30×25 1.54		22×35 1.58	25.4×30 1.64	30×25 1.66		22×40 1.48	25.4×35 1.59	30×25 1.64	35×25 1.59
270	22×35 1.70	25.4×30 1.73	30×25 1.80		22×40 1.65	25.4×35 1.79	30×30 1.82	35×25 1.63	22×50 1.88	25.4×40 1.87	30×30 1.89	35×25 1.90
330	22×45 1.87	25.4×35 1.97	30×30 2.03	35×25 1.80	22×50 1.95	25.4×40 2.00	30×30 2.05	35×25 2.05		25.4×45 2.12	30×35 2.12	35×30 2.15

Capable ripple current (A_{rms})

Fig. 2.5 Specification data of electrolytic capacitor, SAMWHA-HJ series [57].

over 20 milliseconds of hold-up time. In the diode rectifier system, C_{dc} acts as temporary energy source during hold-up time, and it is calculated as

$$C_{dc} = \frac{2E_{dc}}{V_{dc.nom}^2 - V_{dc.\min}^2}, \tag{2.3}$$

where E_{dc} is capacitor energy, $V_{dc.nom}$ and $V_{dc.min}$ are nominal and minimum available DC-link voltages, respectively. For example, in the case of 1-kW system with $V_{dc.max}$ = 300 V and $V_{dc.min}$ = 200 V, E_{dc} is 1 kW x 20 ms = 20 J and the required C_{dc} is calculated to 800 μF.

2.1.2 Grid Harmonic Regulations and Grid Filter Inductor

If the systems want to connect to the grid, they should satisfy the grid harmonic regulations such as IEEE 519 or IEC 61000. The regulations are usually categorized according to the current level of applied equipment. In IEC 61000 standards, IEC 61000-3-2 is applicable to the equipment which is supplied from the grid with voltage not less than 220V and current up to 16A, and IEC 61000-3-12 is applicable to the equipment with rated current higher than 16A and lower than 75A.

IEC 61000-3-2 standard is applicable to an equipment which is supplied from the grid with voltage not less than 220V and current up to 16A. The equipment can be grouped into one of four classes based on the following criteria as evaluated by the IEC committee [4]:

- Number of pieces of equipment in use
- Duration of use
- Simultaneity of use
- Power consumption
- Harmonics spectrum including phase

After all the above criteria are considered, equipment are classified as follows:

1) Class A
    - Balanced three-phase equipment
    - Household appliances, excluding equipment identified by Class D
    - Tools excluding portable tools
    - Audio equipment
    - Everything else that is not classified as Classes B, C, and D
2) Class B
    - Portable tools
    - Arc welding equipment which is not professional equipment
3) Class C
    - Lighting equipment
4) Class D
    - Personal computers and personal computer monitors
    - Television receivers

Here, the equipment in Class D must have power level 75 W up to and not exceeding 600 W. Table 2.1 shows the harmonic standards of IEC61000-3-2 in accordance with the above classification [3]. The standards represent relevant limit values of the harmonics up to order 40.

Table 2.1 Grid current harmonic regulations of IEC 61000-3-2

Harmonics [n]	Class A [A]	Class B [A]	Class C [% of fund]	Class D [mA/W]
Odd harmonics				
3	2.30	3.45	30 x λ	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
11	0.33	0.495	3	0.35
13	0.21	0.315	3	3.85/13
15 ≤ n ≤ 39	0.15 x 15/n	0.225 x 15/n	3	3.85/n
Even harmonics				
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
8 ≤ n ≤ 40	0.23 x 8/n	0.345 x 8/n	-	-

In IEC61000-3-12, there are three types of limits for equipment:

■ Limits for equipment other than balanced three-phase equipment

■ Limits for balanced three-phase equipment

■ Limits for balanced three-phase equipment under specified conditions

The relevant limit values of the harmonics are shown in Tables 2.2, 2.3, and 2.4 [2]. To calculate short circuit ratio R_{sce} which determines the required limit values, the short circuit power S_{sc} and the rated apparent power of the equipment S_{equ} should be calculated. According to [5], S_{sc} is $V_{nominal}^2/Z$, where $V_{nominal}$ is systematic nominal line voltage and Z is output impedance of the power source at the point of common coupling (PCC). S_{equ} is defined as one of the below equations depending on the type of equipment.

1) $S_{equ} = V_p I_{equ}$ for single-phase equipment and the single-phase components of composite equipment, where V_p is a rated single-phase voltage and I_{equ} is a manufacturer-specified rated line current of the equipment.
2) $S_{equ} = V_i I_{equ}$ for interphase equipment, where V_i is a rated line-to-line voltage.
3) $S_{equ} = \sqrt{3} V_i I_{equ}$ for balanced three-phase equipment and the three-phase components of composite equipment.
4) $S_{equ} = 3 V_p I_{equ.\max}$ for unbalanced three-phase equipment, where $I_{equ.max}$ is a maximum line current value of the three phases.

With the calculated S_{sc} and S_{equ}, R_{sce} can be obtain as one of the following equations

depending on the type of equipment.

1) $R_{sce} = \frac{S_{sc}}{3S_{equ}}$ for single-phase equipment and the single-phase components of composite equipment.

2) $R_{sce} = \frac{S_{sc}}{2S_{equ}}$ for interphase equipment.

3) $R_{sce} = \frac{S_{sc}}{S_{equ}}$ for three-phase equipment and the three-phase components of composite equipment.

Comparing the obtained R_{sce} to a minimum short circuit ratio $R_{sce.min}$ in the standard, the required limit values can be decided. The Table 2.4 is used only if one of the following specified conditions is met:

1) The phase angle of the 5th harmonic current relative to the fundamental phase voltage is in the range of 90º to 150º during the whole observation period
2) The equipment is designed such that the phase angle of the 5th harmonic current has no preferential value over time and can take any value from 0 to 360º.

3) The 5th and 7th harmonic currents are each less than 5% of the reference fundamental current during the whole observation period.

Table 2.2 Grid current harmonic limits of IEC 61000-3-12 (for equipment other than balanced three-phase equipment)

$R_{sce.min}$	33	66	120	250	350
I_2	8 %				
I_3	21.6 %	24 %	27 %	35 %	41 %
I_4	4 %				
I_5	10.7 %	13 %	15 %	20 %	24 %
I_6	2.7 %	2.7 %	2.7 %	2.7 %	2.7 %
I_7	7.2 %	8 %	10 %	13 %	15 %
I_8	2 %				
I_9	3.8 %	5 %	6 %	9 %	12 %
I_{10}	1.6 %				
I_{11}	3.1 %	4 %	5 %	8 %	10 %
I_{12}	1.3 %				
I_{13}	2 %	3 %	4 %	6 %	8 %
THD	23 %	26 %	30 %	40 %	47 %
PWHD	23 %	26 %	30 %	40 %	47 %

* The values are percentage of individual currents (per fundamental current)

Table 2.3 Grid current harmonic limits of IEC 61000-3-12 (for balanced three-phase equipment)

$R_{sce.min}$	33	66	120	250	350
I_2	8 %				
I_4	4 %				
I_5	10.7 %	14 %	19 %	31 %	40 %
I_6	2.7 %	2.7 %	2.7 %	2.7 %	2.7 %
I_7	7.2 %	9 %	12 %	20 %	25 %
I_8	2 %				
I_{10}	1.6 %				
I_{11}	3.1 %	5 %	7 %	12 %	15 %
I_{12}	1.3 %				
I_{13}	2 %	3 %	4 %	7 %	10 %
THD	13 %	16 %	22 %	37 %	48 %
PWHD	22 %	25 %	28 %	38 %	45 %

* The values are percentage of individual currents (per fundamental current)

Table 2.4 Grid current harmonic limits of IEC 61000-3-12 (for balanced three-phase equipment under specified conditions)

$R_{sce.min}$	33	120
I_2	8 %	
I_4	4 %	
I_5	10.7 %	40 %
I_6	2.7 %	2.7 %
I_7	7.2 %	25 %
I_8	2 %	
I_{10}	1.6 %	
I_{11}	3.1 %	15 %
I_{12}	1.3 %	
I_{13}	2 %	10 %
THD	13 %	48 %
PWHD	22 %	45 %

* The values are percentage of individual currents (per fundamental current)

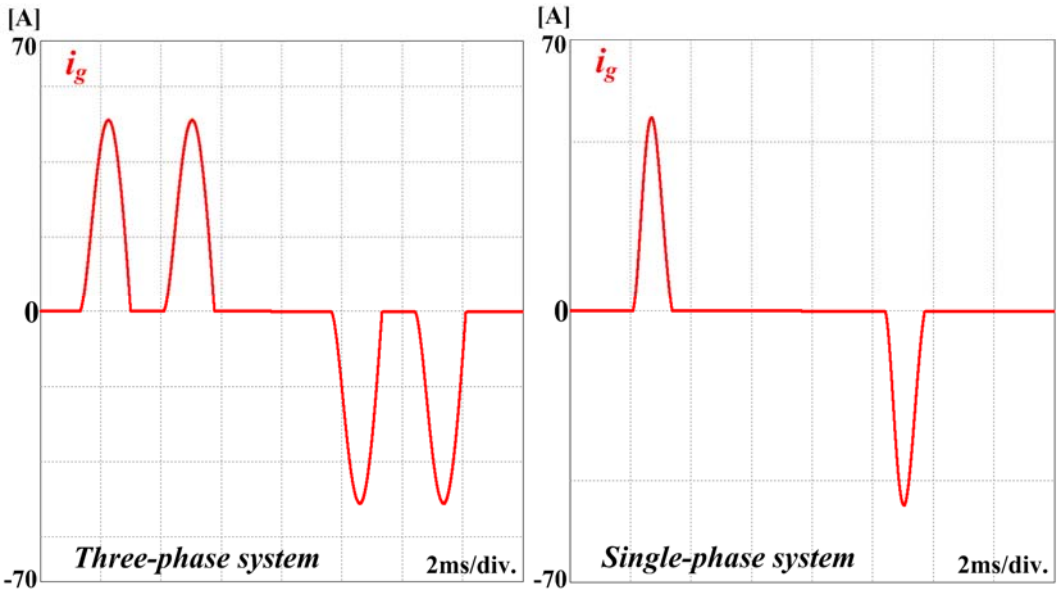


Fig. 2.6 Single- and three-phase grid currents without grid inductor.

In the case of the diode rectifier system shown in Fig. 2.2, as C_{dc} is increased, conduction time of diode rectifier becomes narrow and DC-link capacitor current i_{dc} becomes similar with impulse waveform; then the grid harmonics are gradually deteriorating. Fig. 2.6 shows grid current waveforms of single- and three-phase system where C_{dc} = 2.2 mF without grid filter inductor. Of course, these waveforms cannot satisfy the grid harmonic regulations.

Here, the grid filter inductor is adopted in order to attenuate grid current harmonics. As shown in Fig. 2.7, there are two ways to install the grid inductor according to its position (on the AC or DC lines). In the case of three-phase grid

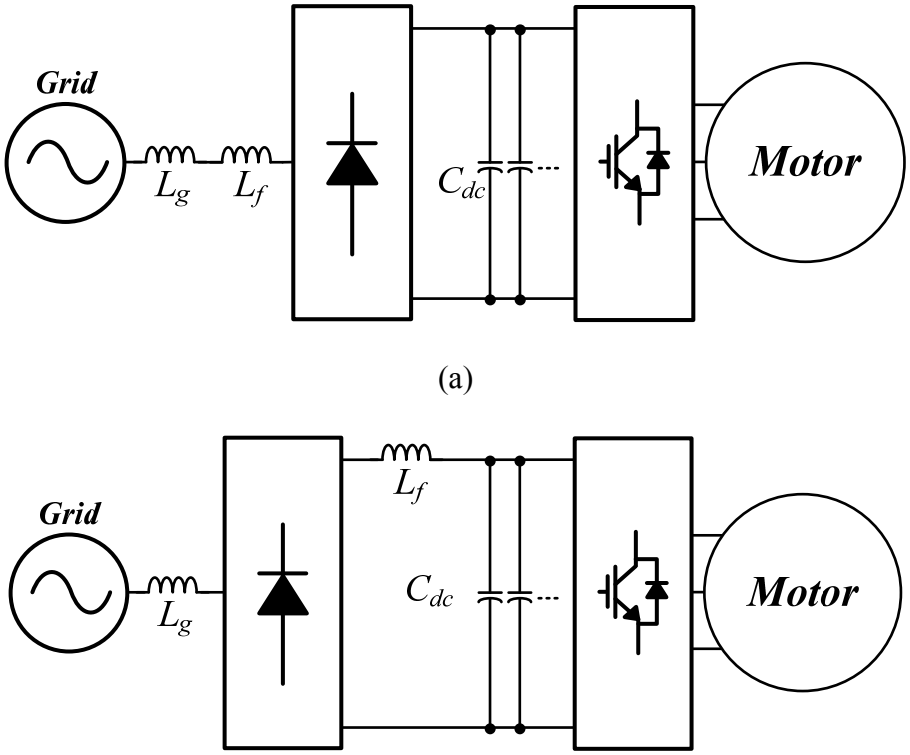


Fig. 2.7 diode rectifier system with (a) AC and (b) DC inductors.

system, the AC inductor shows better harmonic attenuation performance, but the DC inductor has merits in terms of size and cost. After applying the grid inductor, the conduction time of diode rectifier becomes wider, grid harmonics are improved as shown in Fig. 2.8 [62][63]. By adjusting the value of inductance, the diode rectifier system is able to meet the grid harmonic regulation.

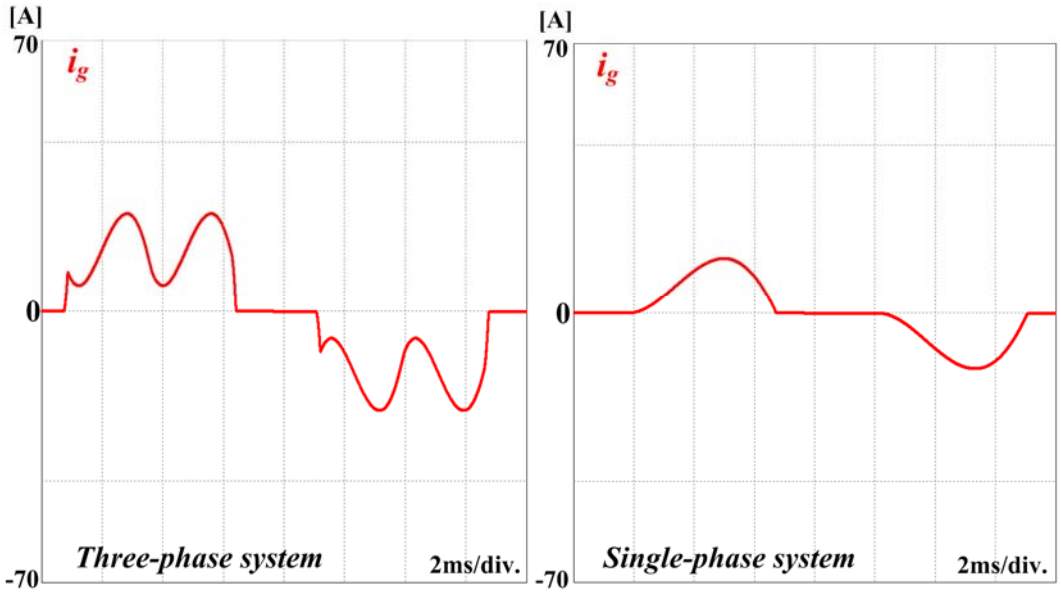


Fig. 2.8 Single- and three-phase grid currents with grid inductor.

2.1.3 Limitation of Passive Components

Although system implementation using passive components has been commonly applied in the industry for a long time, they have several demerits and limitations. First, they occupy too many spaces in power conversion system. The size and weight of whole system are dominantly decided by them and their cost holds a large part of total system cost. Furthermore, the system with large DC-link capacitance needs pre-charging circuit in order to prevent a huge inrush current. By using this circuit, extra cost is charged [11][12][15].

As well as the above problems, many researchers have found out that the

reliability of the system has been degraded owing to the high failure rate of the electrolytic capacitor which is commonly used for DC-link capacitor. The electrolytic capacitor is well known for one of the weakest component in the entire power conversion system. Due to its physical structure for obtaining high capacitance per unit volume, the capacitor has large equivalent series resistance (ESR) and it leads to increasing of internal heat generation. This internal heat brings about rapid evaporation of internal electrolyte and the lifetime of this capacitor becomes shorter. The dissipation power loss P_{heat} caused by the internal heat is related with the ESR and the capacitor ripple current $i_{dc.ripple}$, described as

$$P_{heat} = i_{dc.ripple}^2 ESR , \tag{2.4}$$

so the $i_{dc.ripple}$ is limited in accordance with acceptable P_{heat} and the ESR. Considering this factor, the electrolytic capacitor has about thousand hours of lifetime at 105 ºC, and the lifetime reduces to half for every 10 ºC of the temperature rise [58].

Fig. 2.9 shows failure rate of the components used in the switch-mode power supplies such as H-bridge and resonant fly-back type converters, and Table 2.5 also lists the component failures per million hours in the two-stage (flyback + H-bridge) topology [59]-[61]. From these data, it can be verified that the failure of electrolytic capacitor shows far higher value in comparison with the failure of other components.

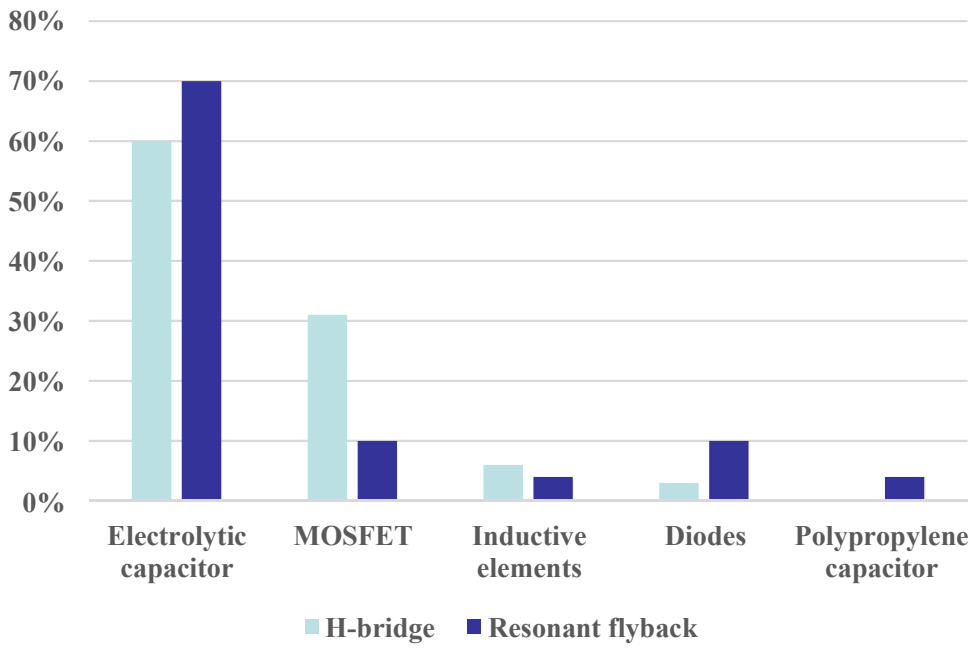


Fig. 2.9 Failure rate of the components in the switchmode power supplies [59][60].

Table 2.5 Failure rate of the components used in two-stage (flyback + H-bridge) topology [61].

Components	Base reliability (failures/million hours)
Electrolytic capacitor	0.0455
MOSFET	0.012
Film capacitor	0.0005

2.2 Diode Rectifier Systems with Small DC-Link Capacitor – State of the Art and Challenges

2.2.1 Review of Conventional Small DC-Link Capacitor System

As mentioned in Section 2.1, the electrolytic capacitor has several problems in terms of size, cost, and reliability. Hence, many researchers have investigated the method to replace the electrolytic capacitor to alternatives such as film and ceramic capacitors. The alternatives have advantageous of ripple current capability and relatively high voltage rating, but they have very small capacitance per unit volume in comparison with conventional one, electrolytic capacitor. Implementing large C_{dc} by using alternatives is significantly disadvantageous to system cost and physical size, so researches about system having small C_{dc} have been investigated and evaluated.

If power conversion system equips small C_{dc}, there is concern that the system becomes sensitive and unstable; thus the small DC-link capacitor system requires additional control method or structure to complement it. Moreover, this system has no capable to provide the basic roles of DC-link capacitor, voltage regulating and temporary energy supplying. For this reason, application area for this system is limited. However it is sufficiently applicable for the areas such as air compressor and pump, which have no rapid load variation and do not require hold-up time.

The control methods for diode rectifier system with small DC-link capacitor can be classified into two cases as follows:

- Small DC-link capacitor system with stabilization control [11]-[17]
- Small DC-link capacitor system with grid current shaping control [21]-[26]

Referring to the conventional researches, two cases are dealt with the different issues each other. Their main difference is decided by two factors: first factor is negative impedance characteristic caused by reduced C_{dc} and CPL, and another is necessity of the grid filter inductor. The first factor has been discussed in many conventional stabilization control studies and will be reviewed in this section. The second factor is related with grid current harmonics of the system. Unlike the other topologies such as cascaded boost PFC and full-bridge converters shown in Fig. 2.10, the diode rectifier system has been relied on grid filter inductor in terms of grid current harmonic. However the diode rectifier system with small C_{dc} has merit in grid current harmonic improvement, since the inverter current i_{inv} directly have influence on the grid current without any disturbance of DC-link capacitor current. Here, if the total output power can be adjusted as we want, the diode current harmonics is also able to be controlled to the direction of reducing them. It means that the role of grid filter inductor is decreased and even it is possible to remove the

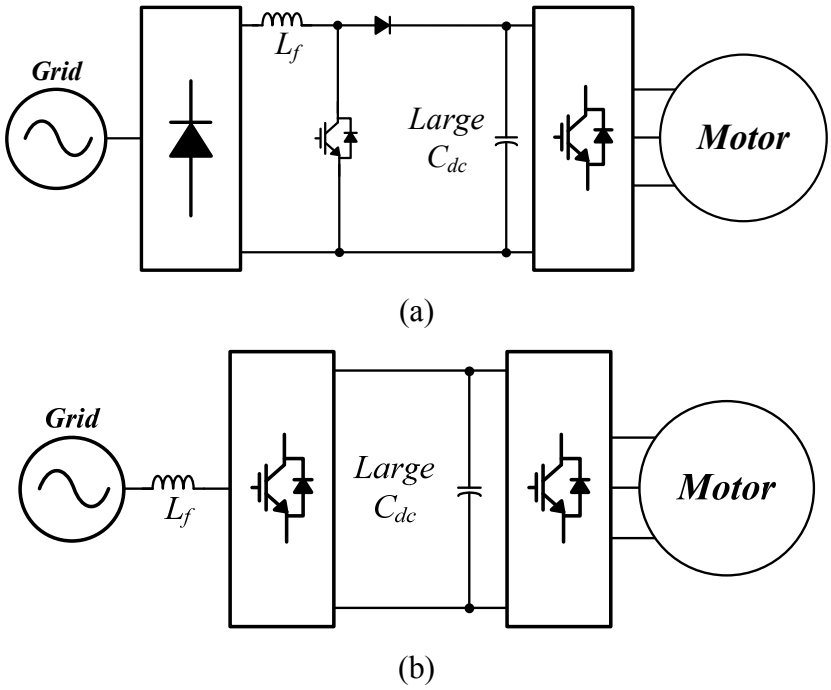


Fig. 2.10 The motor drive systems with (a) cascaded boost PFC converter and (b) full-bridge converter.

inductor. The removal of the inductor changes the system in terms of not only structural way but also the system characteristic. Hence this section discusses the system characteristic with or without grid filter inductor assuming that the output power is constant. The characteristic is discussed considering both three- and single-phase grid connected systems.

The system with the grid filter inductor is classified in detail in accordance with the kind of grid phase and the position of grid filter inductor. The classifications are shown in Fig. 2.11, and the system without the grid filter inductor is illustrated in

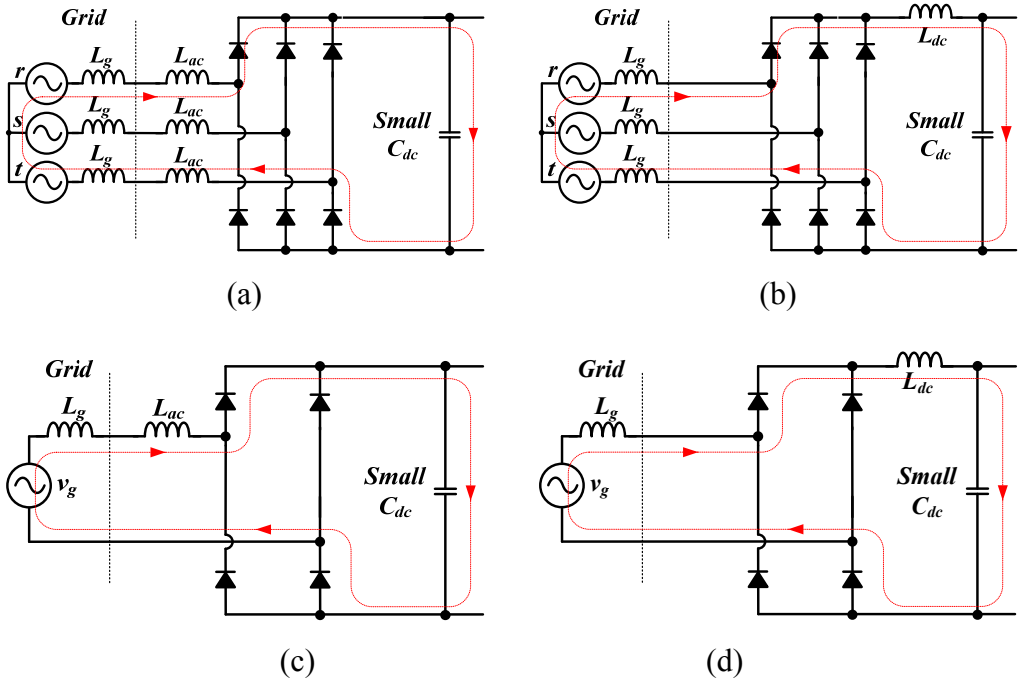
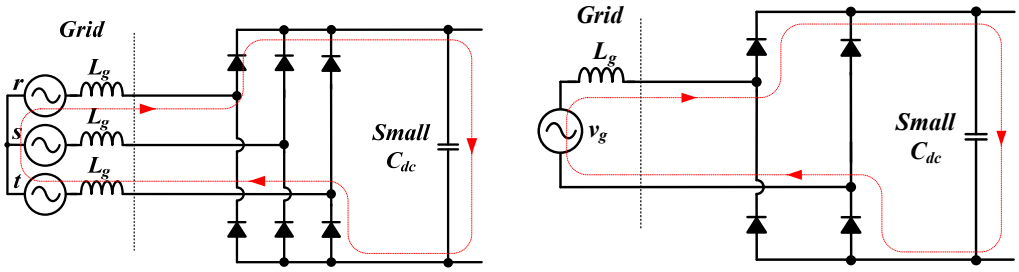


Fig. 2.11 Small DC-link capacitor systems: (a) three-phase grid and AC inductor, (b) three-phase grid and DC inductor, (c) single-phase grid and AC inductor, and (d) single-phase grid and DC inductor.

Fig. 2.12. All cases can be expressed as an equivalent circuit shown in Fig. 2.13. Here, L_{eq} and R_{eq} are equivalent impedances, and it is assumed that the inverter can be replaced by current source i_{inv} and the inverter power P_{inv} is constant. The rectified grid voltage v_{eq} is also assumed to be constant.

In accordance with the cases illustrated in Figs. 2.11 and 2.12, the L_{eq} and R_{eq} are defined as listed in Table 2.6. L_g and R_g are grid impedances, ω_g is grid angular



(a) (b)

Fig. 2.12 Small DC-link capacitor systems without grid filter inductor: (a) three-phase and (b) single-phase grids.

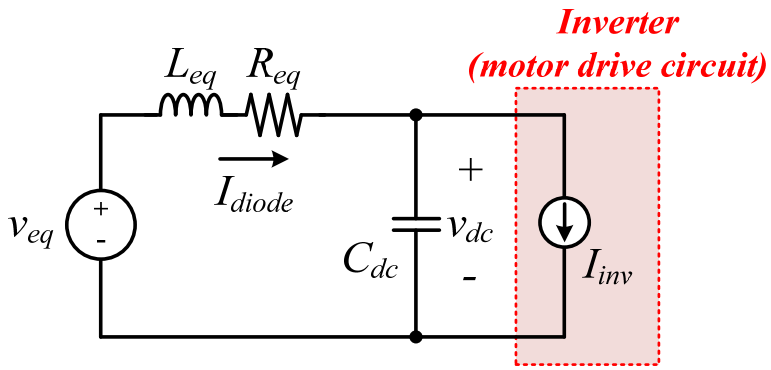


Fig. 2.13 Equivalent circuit of motor drive system.

speed, and $3\omega_g L_g/\pi$ is a term for nonohmic voltage drop due to commutation [13][14].

To verify the characteristic of DC link voltage v_{dc}, its transfer function is derived. Assuming that P_{inv} is constant and i_{inv} equals to P_{inv}/v_{dc}, it can be derived as

$$i_{inv} = \frac{P_{inv}}{v_{dc}} = \frac{P_{inv}}{V_{dc0} + \tilde{v}_{dc}} \approx \frac{P_{inv}}{V_{dc0}} - \frac{P_{inv}}{V_{dc0}^2}\tilde{v}_{dc} \tag{2.5}$$

Table 2.6 Equivalent impedances

in accordance with the kind of grid phase and position of grid inductor

	Three-phase	Single-phase
AC inductor	$R_{eq} = 2(R_g + R_{ac}) + \frac{3\omega_g L_g}{\pi}$ $L_{eq} = 2(L_g + L_{ac})$	$R_{eq} = R_g + R_{ac} + \frac{3\omega_g L_g}{\pi}$ $L_{eq} = L_g + L_{ac}$
DC inductor	$R_{eq} = 2R_g + R_{dc} + \frac{3\omega_g L_g}{\pi}$ $L_{eq} = 2L_g + L_{dc}$	$R_{eq} = R_g + R_{dc} + \frac{3\omega_g L_g}{\pi}$ $L_{eq} = L_g + L_{dc}$
w/o inductor	$R_{eq} = 2R_g + \frac{3\omega_g L_g}{\pi}$ $L_{eq} = 2L_g$	$R_{eq} = R_g + \frac{3\omega_g L_g}{\pi}$ $L_{eq} = L_g$

by Tylor series, where V_{dc0} is average value of v_{dc}. The loop equation from the grid side is

$$v_{eq} = R_{eq} i_{diode} + L_{eq} \frac{di_{diode}}{dt} + v_{dc}, \tag{2.6}$$

and the capacitor equation from the DC-link node is

$$C_{dc} \frac{dv_{dc}}{dt} = i_{diode} - i_{inv}. \tag{2.7}$$

By using Laplace transformation and substituting (2.5) and (2.6) into (2.7), the v_{dc} can be derived as

$$v_{dc} = \frac{\dfrac{v_{eq}V_{dc0} - R_{eq}P_{inv}}{L_{eq}C_{dc}V_{dc0}} - \dfrac{P_{inv}}{C_{dc}V_{dc0}}s}{s^2 + \left(\dfrac{R_{eq}}{L_{eq}} - \dfrac{P_{inv}}{C_{dc}V_{dc0}^2}\right)s + \dfrac{V_{dc0}^2 - P_{inv}R_{eq}}{L_{eq}C_{dc}V_{dc0}^2}}. \tag{2.8}$$

Here, the condition that poles of (2.8) are located on left half plane is

$$C_{dc} > \frac{L_{eq}P_{inv}}{R_{eq}V_{dc0}^2}. \tag{2.9}$$

For example, in the case that the system is connected to three-phase grid with DC inductor (R_g = 0.1 Ω, L_g = 50 μH, ω_g = 377 rad/s, L_{dc} = 0.7 mH, R_{dc} = 0.1 Ω, V_{dc0} = 290 V, and P_{inv} = 5500 W,) the system requires C_{dc} higher than 165 μF to operate itself stably. However, if the film or ceramic capacitors are used, the substantive DC-link capacitance is several tens of microfarad. Therefore, the system becomes unstable and resonant. The resonance frequency f_r is defined as

$$f_r = \frac{1}{\pi\sqrt{L_{eq}C_{dc}}}. \tag{2.10}$$

The main differences of two cases (the small DC-link capacitor system with or without grid filter inductor) are the range of stability condition in (2.9) and the resonance frequency in (2.10). In the case of the small DC-link capacitor system with grid filter inductor, the minimum C_{dc} for stable system is several hundreds of microfarad, while the second case (small DC-link capacitor system without grid filter inductor) shows several tens of microfarad for the minimum C_{dc}. For example,

from the above conditions without L_{dc} and R_{dc}, the minimum C_{dc} is calculated to 30 μF. Therefore, the system without grid filter inductor is much more stable than that with grid filter inductor. For this reason, the goal of the conventional studies is divided in accordance with the existence of grid filter inductor. The studies for the former case have been totally focusing on stabilization control, but those for the latter case have been mainly considering about grid current shaping control in order to improve grid current harmonics [21]-[26].

The stabilization control methods have been widely investigated for a long time, and the basic concept of these methods is to neutralize the negative impedance characteristic caused by CPL such as inverter [11]-[20]. There are two ways to apply the methods into the inverter: inverter current reference or voltage reference direct modification methods. The inverter current reference modification method shown in Fig. 2.14 was firstly introduced owing to its easy approach to implement, but the main drawback of this method is that the modification response is limited by the bandwidth of current controller.

On the other hand, the inverter voltage reference direct modification method shown in Fig. 2.15 has been proposed to overcome previous limitation. In this control method, the current controller regulates the average value of dq-axis currents in the synchronous dq-reference frame, and the voltage reference modification block carries out instantaneous power control by manipulating output

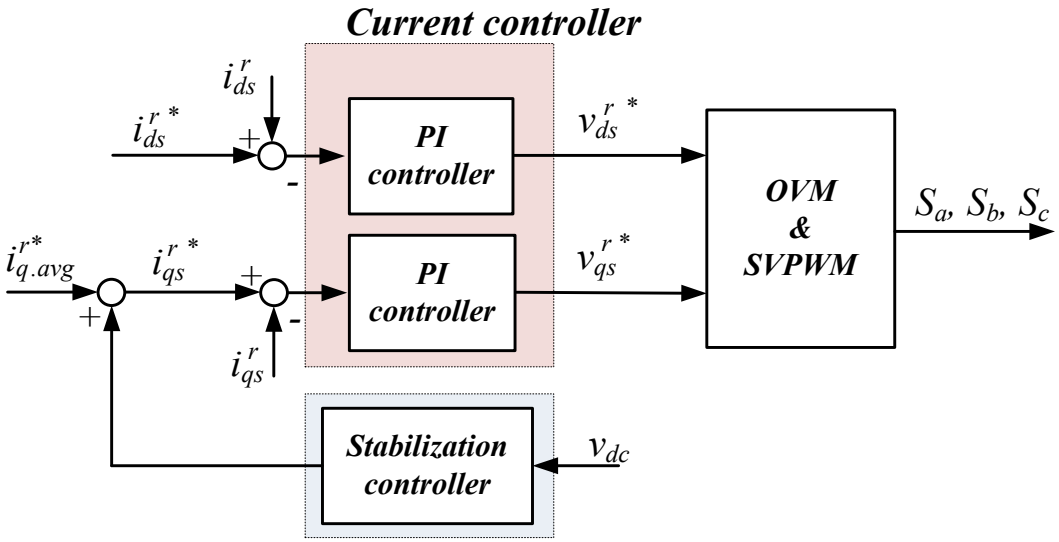


Fig. 2.14 Block diagram of current reference modification method.

voltage of current controller directly. Even though the maximum value of motor current should be contemplated particularly since the current controller does not regulate the value any longer, this method has merits in fast response for suppressing the resonance; so the voltage reference direct modification method has been evaluated to appropriate solution for stabilizing control method, i.e., instantaneous power control method.

In the grid current shaping methods for the small DC-link capacitor system without grid filter inductor, it is important to decide how to control the shape of the inverter power. The methods have been focused on grid current harmonic improvement which was conducted by grid filter inductor L_f. Since it is possible to

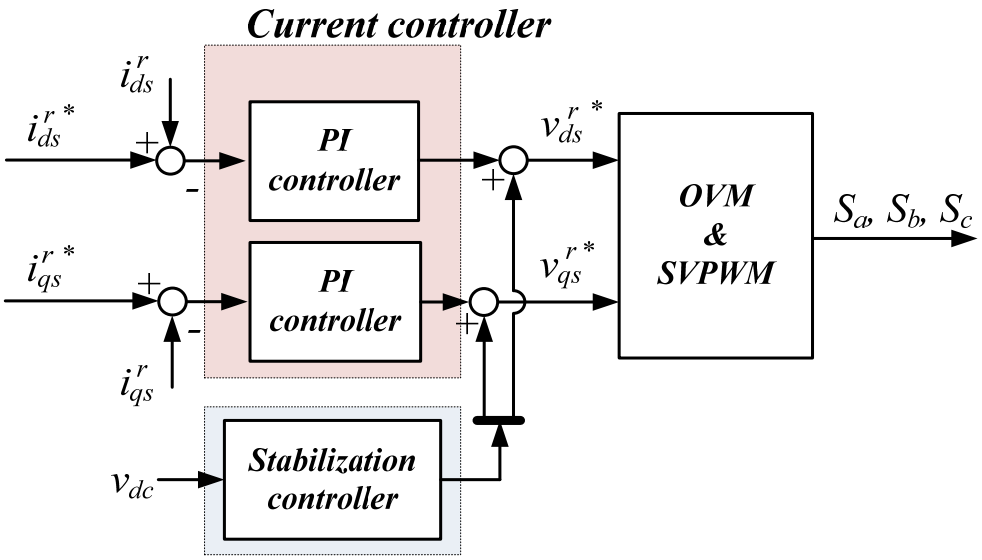


Fig. 2.15 Block diagram of voltage reference direct modification method.

design the system frequencies, such as grid current harmonics and switching frequencies, to avoid the resonance frequency f_r in (2.10), stabilization control is not a crucial problem in this system.

This system has been mainly adopted in the single-phase grid, since it is structurally easy to improve grid current harmonics in comparison with three-phase grid system. By using that the DC-link voltage is similar with the absolute value of grid voltage, the conduction time of the diode bridge can be widely extended, and the diode current, i.e., grid current can be shaped by instantaneous power control of inverter. In [21]-[26], they propose the instantaneous power control method for single-phase grid connected motor drive system. This method aims that the motor

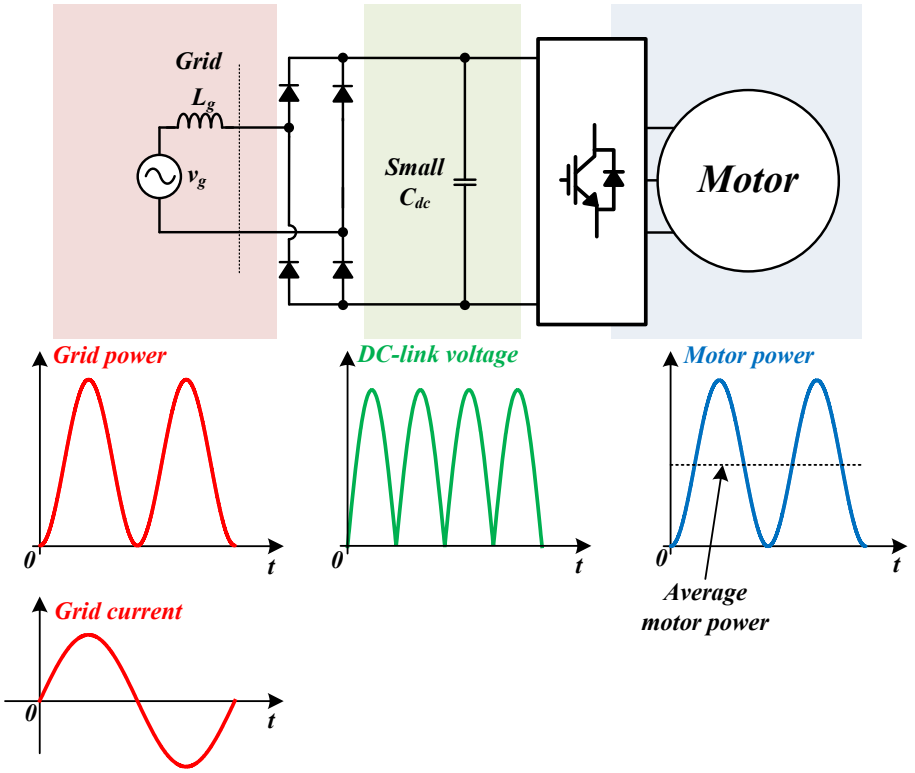


Fig. 2.16 Basic concept of grid current shaping method in single-phase system.

power is controlled as square of sinusoidal waveform synchronized to the grid angle as shown in Fig. 2.16. Then the grid power also becomes square of sinusoidal waveform because DC-link capacitor power is negligible; the grid current is shaped as sinusoidal curve.

This method also can be realized as two ways: current reference or voltage reference direct modification methods as introduced in [21]-[24] and [25][26], respectively. Their pros and cons are similar with the situation of previous

stabilization control methods, but the amount of handling ripple power is relatively very high. The peak value of motor power is two times of the average motor power, and this causes the increase of peak motor current and output torque ripple.

2.2.2 Limitation of Conventional Systems

In the previous methods, stabilization control methods for both single- and three-phase systems have been researched, but grid current shaping methods have been suggested for single-phase system only. The reason is that the three-phase diode rectifier system is impossible to shape sinusoidal grid current owing to its structural operating characteristic that the diode legs of each phase are alternately conducted in every one third of grid period. However, even though the grid current is not sinusoidal waveform, it is possible to satisfy the grid regulation for the applicable area by spending a little effort on the harmonic improving control. By applying this effort, the three-phase diode rectifier system is able to satisfy required grid harmonic regulation without heavy grid filter inductor. One of conventional research proposed the shunt passive filter which mitigates particular harmonic, but this filter needs too many passive components such as inductor and capacitor. Moreover it is hard to implement cost-effective filter since the power rating of shunt passive filter reaches up to 90% of main power [64]-[66].

Meanwhile, the conventional methods such as stabilization or current shaping

controls have common problem that the efficiency of total motor drive system is degraded due to the extra control methods. In the case of stabilization control for three-phase system, it needs extra voltage margin for this extra control. This extra voltage margin decreases maximum available modulation index (MI), and it is disadvantageous for flux-weakening control area where the d-axis current is injected in order to secure the voltage margin. The additional d-axis current caused by the reduced MI degrades the system efficiency. Unlike the three-phase system, on the other hand, the single-phase system has similar waveform of absolute value of grid voltage, and the lack of DC-link voltage occurs at least in every 2 times of grid period. The DC-link voltage lack areas bring about excessive d-axis current injection (flux-weakening control), and this also decreases the efficiency of total motor drive system.

To complement this demerit, the auxiliary circuit linked to DC-link in parallel has been researched, and the inverter can be free from the deterioration caused by extra control method, because the auxiliary circuit performs stabilization control instead of the inverter [27]. Thanks to the aid of auxiliary circuit with high switching frequency, the inverter can fully utilize available DC-link voltage into motor drive. However, in [27], heavy grid filter inductor is in charge of grid current harmonic improvement, and the research for grid current shaping control by using auxiliary circuit has not been investigated. If this research is proposed, cost benefit

and performance improvement are expected by removing heavy grid filter inductor and ensuring motor drive efficiency. The conventional researches and challenges of diode rectifier-fed small DC-link capacitor system are listed in Table 1.1 in Section 1.

2.3 Conventional Systems with Auxiliary Circuit for Reducing Passive Components

In this subsection, the conventional topologies using auxiliary circuit for reducing passive components are introduced. The auxiliary circuit mainly aims to substitute for the role of heavy passive components by using active devices and low rating passive components. Many conventional auxiliary circuits are used along with PFC or cascaded converter, and then total system cost of them may be higher than that of diode rectifier based topology. However, the diode rectifier based topology usually has performance drop such as insufficient DC-link voltage or limitation of grid current harmonic improvement.

In accordance with the connecting types of auxiliary circuit, the conventional topologies are classified into three types: current injection, series compensation, and parallel compensation circuits. In this subsection, the pros and cons of conventional topologies are discussed.

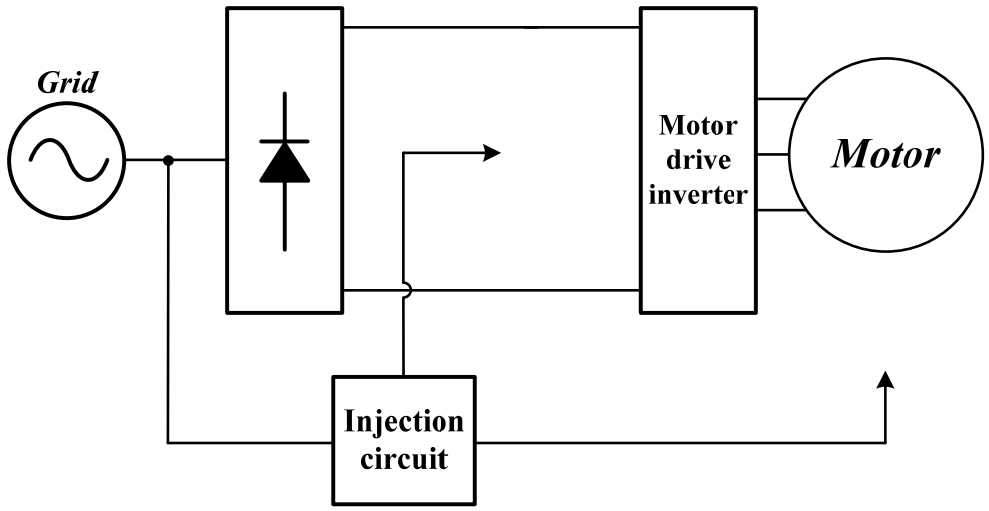
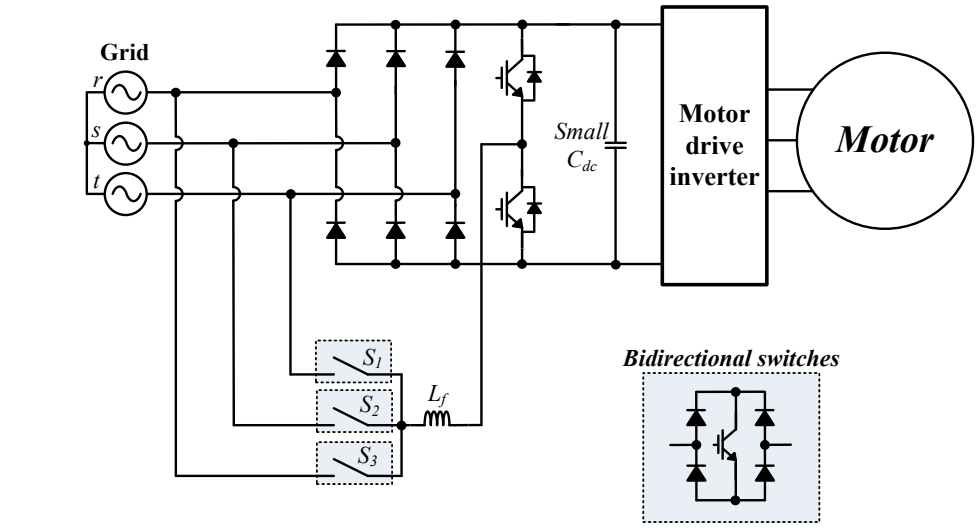


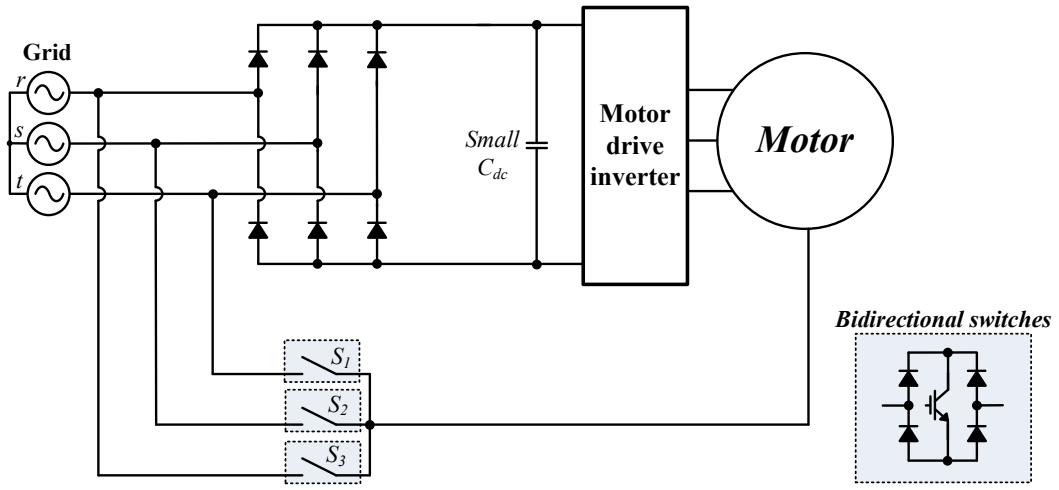
Fig. 2.17 Concept of current injection type topology.

2.3.1 Current Injection Topologies

The basic concept of current injection type topologies is shown in Fig. 2.17 [29]-[33]. These topologies aim to shape three-phase grid current as sinusoidal waveform without heavy grid inductor in the diode rectifier system. Since their auxiliary circuits usually handle smaller power than main power for the load, they can be miniaturized in comparison with full-power-controlled converters such as three-phase full-bridge converter and cascaded boost converter PFC shown in Fig. 2.10. Fig. 2.18 shows examples of current injection method in [29]. The DC-ode connection type like a circuit in Fig. 2.18(a) is most common structure, and we can reduce more components by adopting the second circuit shown in Fig. 2.18(b).



(a)



(b)

Fig. 2.18 Examples of current injection topology: (a) DC-node connection and (b) motor neutral point connection types.

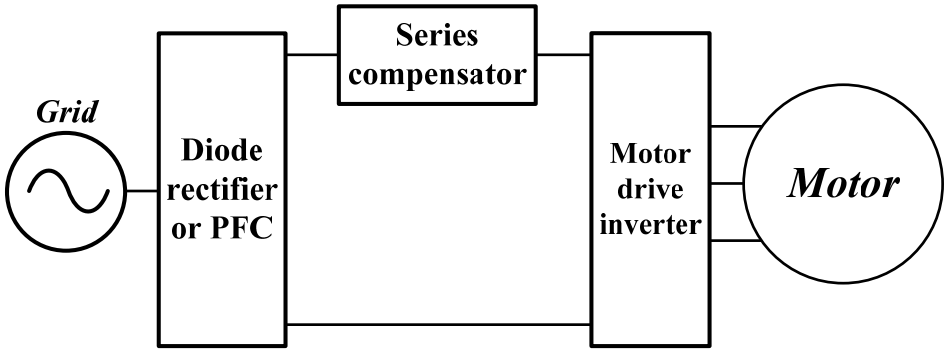


Fig. 2.19 Concept of series compensation topology.

Nevertheless, they still require quite a number of components, since they try to inject the currents into all three-phase paths to make pure sinusoidal grid current. Even though the diode rectifier is used in grid side, total cost is greatly increased considering additional components and their subsidiary circuit such as gate driver circuit. These topologies are suitable for the area where relevant grid regulation requires almost sinusoidal grid current waveform.

2.3.2 Series Compensation Topologies

The series compensation topology shown in Fig. 2.19 is advantageous that the output voltage, i.e., DC-link voltage is able to be regulated by using low voltage rating components [34]-[36]. However the energy buffer capacitance is increased under the same storable energy, and this condition (low voltage and high capacitance) is not appropriate for the film capacitor. Moreover, this topology

should handle main current that directly flows to the load, and this causes relatively high conduction losses.

As a kind of series compensation circuit, the paper [34] introduces 'electric smoothing inductor' which is composed of some active devices and working like

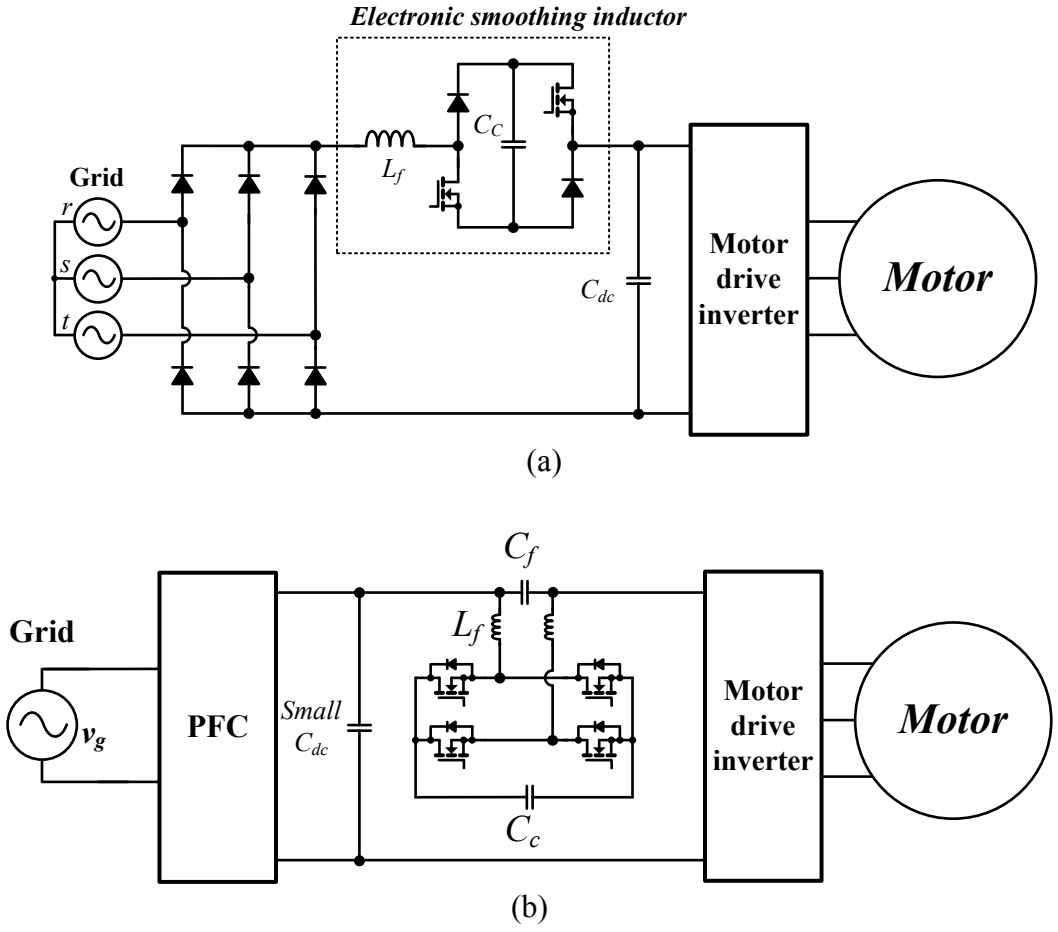


Fig. 2.20 Examples of current injection topology:

(a) electronic smoothing inductor and (b) series voltage compensator.

real inductor in diode rectifier system. The structure is shown in Fig. 2.20(a), and 100-V Metal-oxide semiconductor field-effect transistors (MOSFETs) and storage capacitor C_c of 3 x 680 μF/100 V are used. By using the circuit, flat DC-link voltage and square waveform of grid current can be obtained as if the system equips infinity DC inductor. However, these papers does not consider the substantive grid regulations such as IEEE 519 and IEC 61000, so it needs additional solution in order to satisfy the regulations.

The research in [36] presents control method and design guideline of series voltage compensator which is linked to DC-node in series as shown in Fig. 2.20(b). This circuit is working in order to reduce DC-link capacitance C_{dc} between two converters. In this circuit, electrolytic capacitor of 1000 μF/63 V is used for C_c. By using this circuit, C_{dc} can be replaced from 660 μF to 120 μF.

2.3.3 Parallel Compensation Topologies

The parallel compensation topology shown in Fig. 2.21 is most commonly utilized in passive component reduction methods. This structure is useful in single-phase grid connected system, because the system needs the large capacitance in order to absorb single-phase grid ripple power. Here, the circuit which is a substitute for large capacitance is called power decoupling unit (PDU) [37]-[55]. The PDU is usually utilized along with PFC or grid side converter which perform grid current

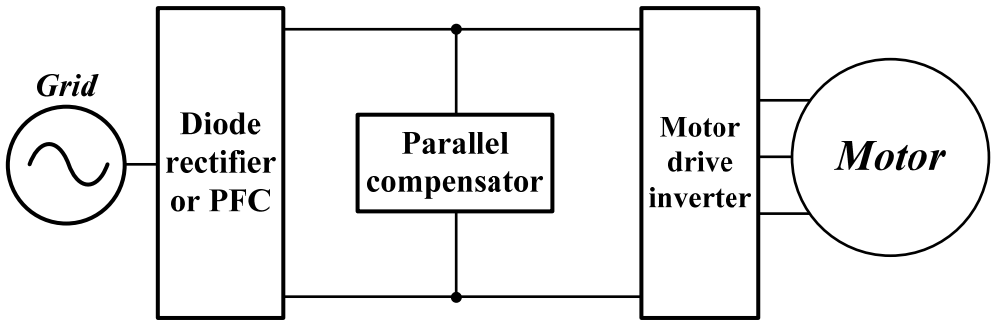


Fig. 2.21 Concept of parallel compensation method.

control, and it only carries out ripple power absorbing.

For example, the circuit shown in Fig. 2.22(a) utilizes a buck converter as the PDU [37]. The capacitance used for ripple energy storage is chosen as several tens of μF and they show the possibility to implement compact energy storage circuit. As aforementioned, however, total system needs quite many components for PFC and PDU. In [38], the research utilizes existing switches from PFC for a PDU as shown in Fig. 2.22(b). This PDU uses an inductor as an energy storage, so they need quite large inductor that makes total system bulky and heavy. In [39], the paper proposes cascaded circuit which consists of diode rectifier, boost converter, and symmetrical half-bridge circuit as illustrated in Fig. 2.22(c). This circuit provides sinusoidal grid current, sufficient DC-link voltage without ripples. However, the system also requires many components: two inductors, three switches, one fast recovery diode, one diode rectifier, and two energy buffer capacitors.

In [44][45], the authors propose the small DC-link capacitor systems with diode rectifier and novel energy buffer. The energy buffer structure in [44] has only one small capacitor and one switch which operation is synchronized with three-phase load inverter, and the structure shown in Fig. 2.23(a) uses charge circuit to improve a voltage transfer ratio defined as ratio of grid voltage peak to average DC-link voltage [45]. These circuits are good solutions compared with other PDU in terms of cost since they can utilize with diode rectifier, but they still use four fast recovery diodes in the rectifier stage because of their operating principle. Moreover, they still have the voltage transfer ratio of 0.707 and this factor might degrade the motor drive performances. The reduced available DC-link voltage inherently occurs in the diode rectifier system. The topology shown in Fig. 2.23 is for stabilization control of small DC-link capacitor system as mentioned in Section 2.2.2 [27]. These researches verify that the circuit linked to DC node in parallel can play a role of active damper. Thanks to its control support, the motor drive circuit can utilize the available DC-link voltage fully.

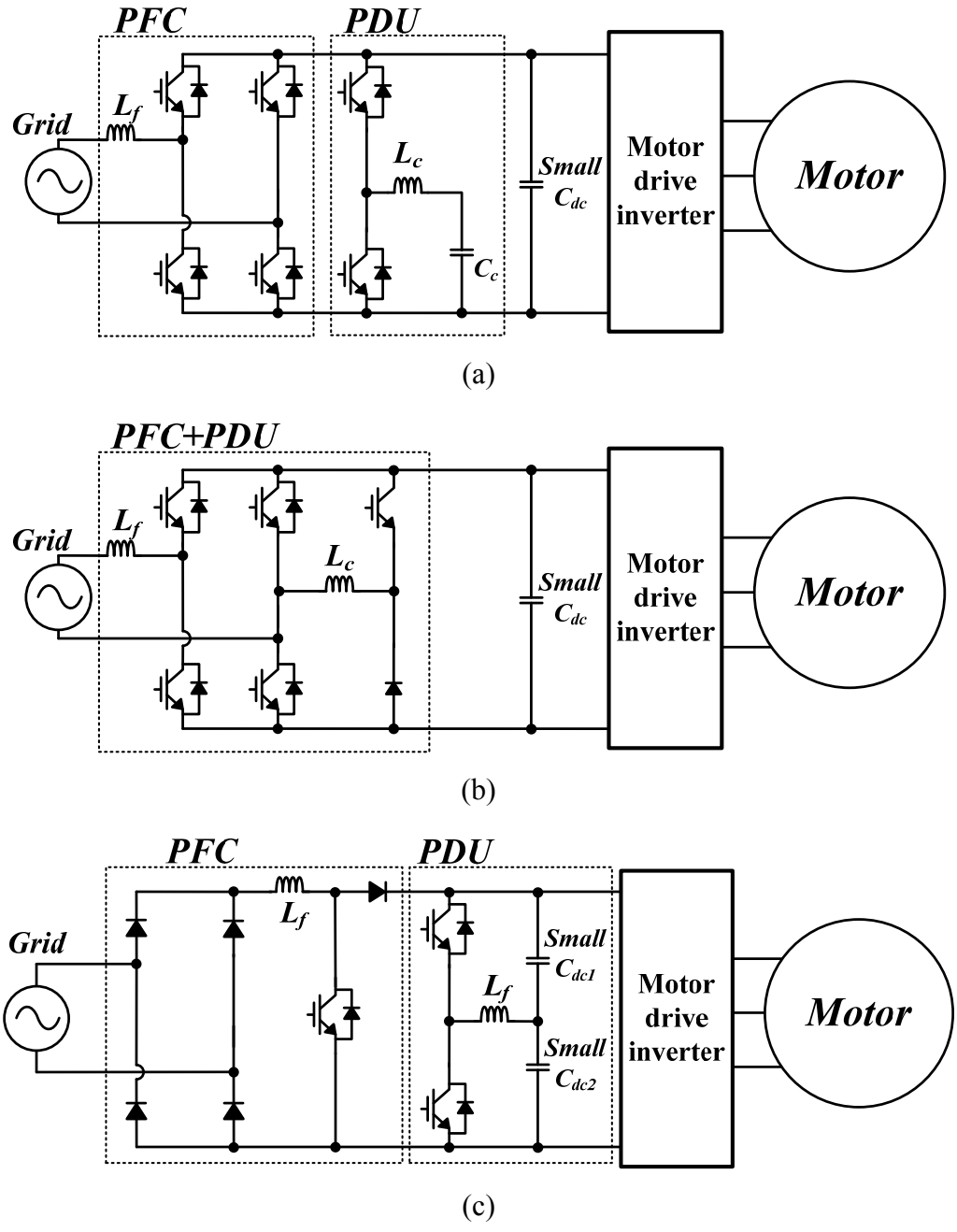
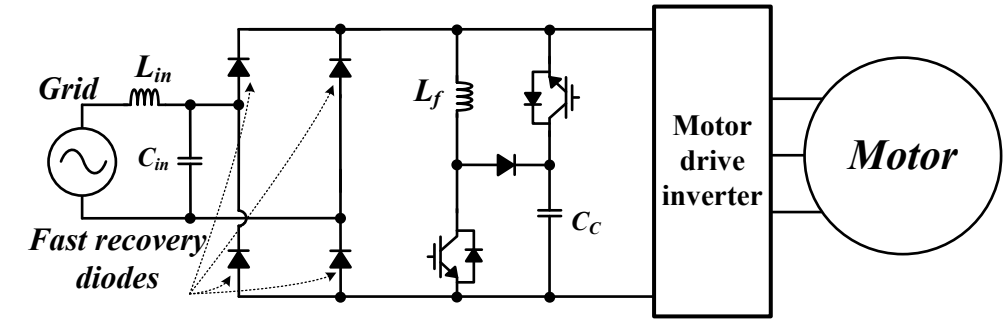
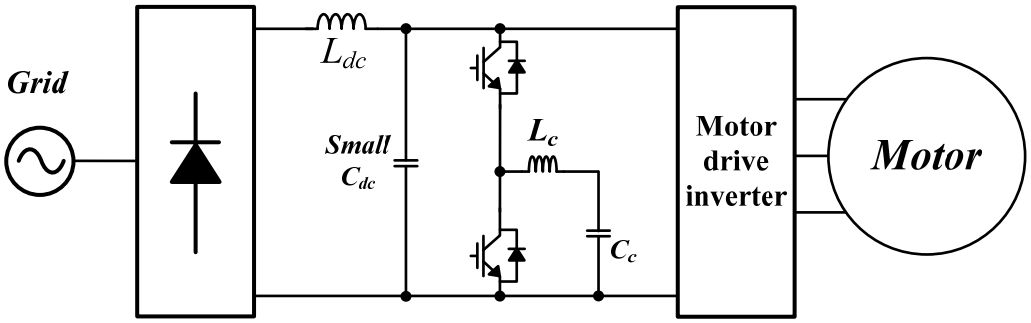


Fig. 2.22 Examples of parallel compensation topology with PFC: (a) PFC with buck type PDU, (b) merging topology (PFC + PDU), and (c) two-stage topology.



(a)



(b)

Fig. 2.23 Examples of parallel compensation topology with diode rectifier: (a) active buffer, (b) auxiliary circuit for system stabilization.

3 Grid Current Shaping and DSC Operating Methods in Three-Phase Diode Rectifier System

In this section, the grid current shaping method for three-phase small DC-link capacitor system without grid filter inductor shown in Fig. 3.1 is proposed. As mentioned in Section 1, the small DC-link capacitor system basically shows low grid current harmonics since the DC-link capacitor current which mainly has bad influence on grid current harmonic is negligible [29]. Indeed, as shown in Fig. 3.2 and Table 3.1, the grid current with constant power output satisfy grid harmonic regulation from IEC61000-3-12 $R_{sce.min}$ = 350 (see Table 2.3) except partial weighted harmonic distortion (PWHD) which is defined as

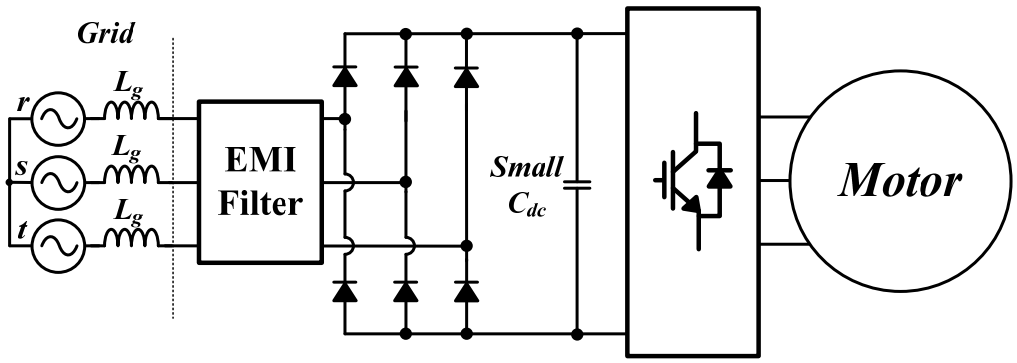


Fig. 3.1 Three-phase diode rectifier-fed small DC-link capacitor system without grid filter inductor.

$$PWHD = \sqrt{\sum_{n=14}^{40} n\left(\frac{I_n}{I_1}\right)^2}\ , \tag{3.1}$$

where I_1 is a magnitude of fundamental grid current and I_n is a magnitude of n order harmonic current. It means that the system can sufficiently satisfy the grid regulation if higher order harmonics of grid current are improved. Therefore if these harmonics are reduced by certain compensation current, system can be applied to industry applications such as air compressor and pump.

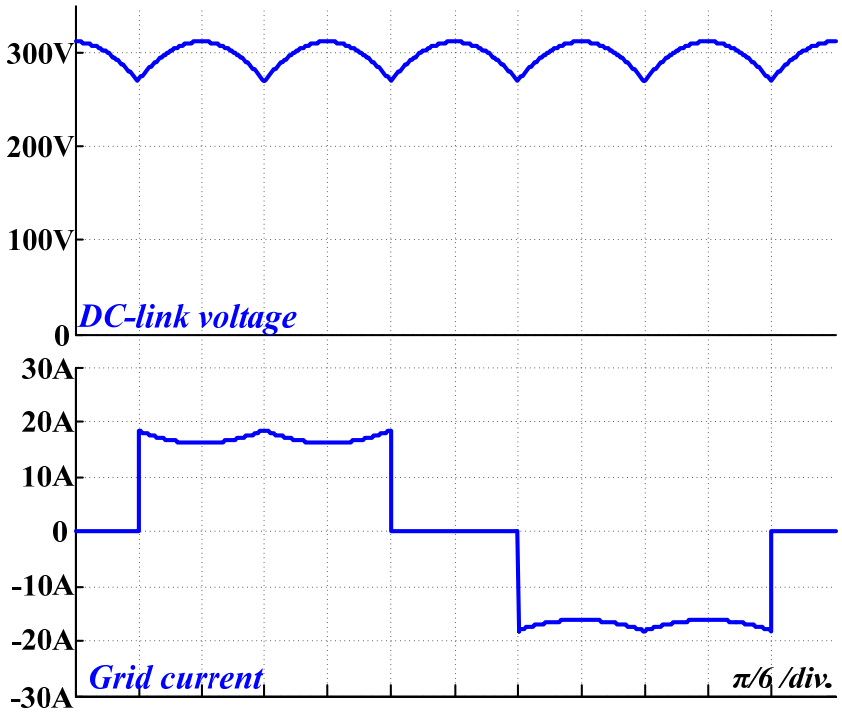


Fig. 3.2 DC-link voltage and grid current of three-phase small DC-link capacitor system without grid filter inductor.

Table 3.1 Grid current harmonics of small DC-link capacitor system with CPL

Odd order harmonics, THD, and PWHD (I_n/I_1, %)						
	I_5	**I_7**	**I_{11}**	**I_{13}**	**THD**	**PWHD**
IEC61000-3-12, $R_{sce.min}$ =350	40	25	15	10	48	45
Small cap. system with CPL	17.59	17.00	9.12	8.80	30.25	***61.91***
Even order harmonics (I_n/I_1, %)						
	I_2	**I_4**	**I_6**	**I_8**	**I_{10}**	**I_{12}**
IEC61000-3-12, $R_{sce.min}$ =350	8	4	2.7	2	1.6	1.3
Small cap. system with CPL	0.03	0.10	0.29	0.12	0.05	0.07

Hence, this dissertation proposes the control method for improving grid current harmonics by using compensation current i_{comp}. The i_{comp} is injected from DC-link side, and the current can be generated by inverter or auxiliary circuit called DC-link shunt compensator (DSC). The DSC, which can be optionally adopted on DC-link in parallel, makes the motor drive system torque-ripple-free and more efficient at flux-weakening area. Since the i_{comp} is dealing with small amount of ripple power to attenuate higher order harmonics, DSC can be designed by using small rating components. Furthermore, the action of i_{comp} enhances to stabilize the entire system

since it neutralizes the negative impedance characteristic caused by CPL. In this section, the control methods implemented in both inverter and DSC are presented. The system stability analysis considering i_{comp} is discussed and system design guideline for DSC is also suggested.

3.1 Grid Current Shaping Method for Three-Phase System

3.1.1 Operating Principle of Proposed Control Method

The equivalent circuit including i_{comp} can be depicted as Fig. 3.3 where L_{eq} and R_{eq} are the case of three-phase system without grid filter inductor in Table 2.6. Since i_{comp} is injected from DC-link side, it is desirable that i_{comp} should be $6m$ harmonics of grid angular frequency (m = 1.2…) in order to inject same amount of harmonics into the three phase. There are various candidates to meet this condition, the waveform proportional to $6m$ harmonics of DC-link voltage is one of the best solution in consideration of maximal utilization of inverter MI and neutralization of negative impedance characteristic caused by CPL. Here, the point of proposed method is that it is possible to adjust the grid current harmonic if i_{comp} is generated as

$$i_{comp} = \alpha \frac{P_{inv}}{V_{dc0}^2} \tilde{v}_{dc}, \tag{3.2}$$

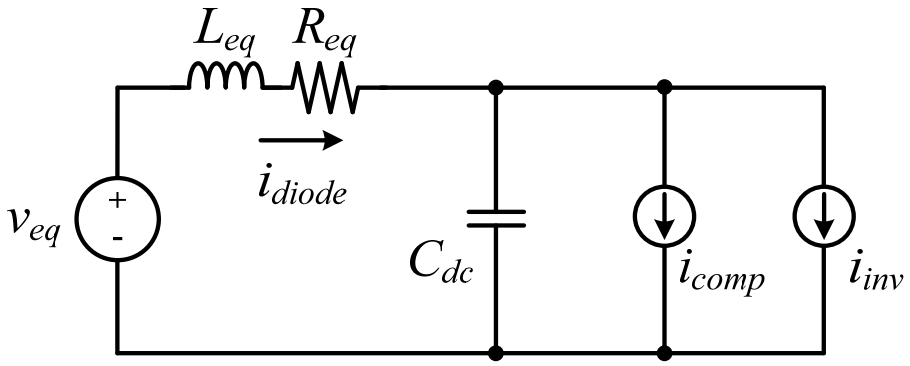


Fig. 3.3 The equivalent circuit including i_{comp}.

where V_{dc0} is average value of main DC-link voltage, α is weighting factor, P_{inv} is load power, and $\tilde{v}_{dc}$ is *6m* harmonics of DC-link voltage filtered by BPF. By using i_{inv} in (2.5), (3.2), and Kirchhoff's current law (KCL) at positive DC-link node in Fig. 3.3, i_{diode} is calculated as

$$i_{diode} \approx i_{inv} + i_{comp} = \frac{P_{inv}}{V_{dc0}} + (\alpha - 1)\frac{P_{inv}}{V_{dc0}^2}\tilde{v}_{dc}. \tag{3.3}$$

Here, it is assumed that DC-link capacitor current i_{dc} is negligible due to significantly small C_{dc}. In (3.3), first term in the right side of the equation is constant value and second term is harmonics proportional to $\tilde{v}_{dc}$. i_{diode} becomes constant value P_{inv}/V_{dc0} where α is 1. If α is higher than unity, however, the second term is increased and it means that the harmonics of grid current are also changed. Since these added harmonics contain *6m* harmonics of grid angle and are even-function, they have equal influence on three-phase grid current. Furthermore, since i_{comp} is

supplied in the form of (3.2), the percentage of harmonic is always maintained. Therefore harmonic influence on grid side is theoretically maintained regardless of output power condition.

i_{diode} in (3.3) becomes each of three-phase grid currents when corresponding diodes are conducting. The waveform of one grid current is shown in Fig. 3.4 on condition that grid side inductance can be negligible. As shown in this figure, the shape of grid current is clear square wave where α = 1, and the smooth waveform is obtained as α is increased.

Assuming that the system is working stable and the grid voltage is $V_m \cdot cos(\omega_g t)$ where V_m is peak value of grid voltage and ω_g is grid angular frequency, $\tilde{v}_{dc}$

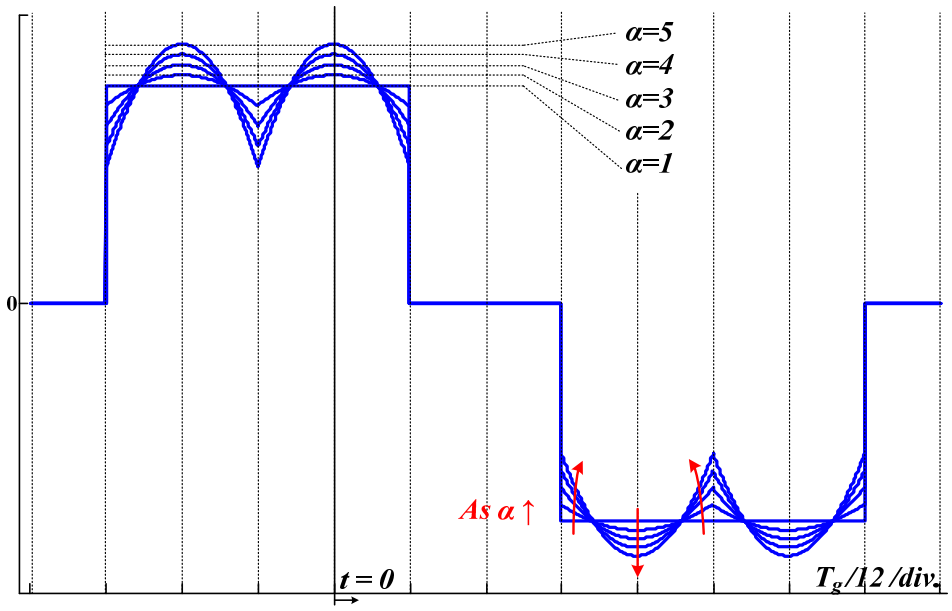


Fig. 3.4 Grid current shape variation according to α.

becomes maximum value of line-to-line grid voltage and expressed as

$$\tilde{v}_{dc} \approx V_m \cos(\omega_g t - (2k-1)\frac{\pi}{6}) - V_{dc0}, \tag{3.4}$$

where $k = 1, 2 \ldots 6$ during one grid period. Here, V_m can be calculated as

$$V_m = \frac{\pi}{3} V_{dc0} \tag{3.5}$$

by using that the average value of (3.4) is zero. From (3.3), i_{diode} can be derived as

$$i_{diode} = x(\alpha) + y(\alpha)\cos(\omega_g t - (2k-1)\frac{\pi}{6}), \tag{3.6}$$

where

$$x(\alpha) = (2-\alpha)\frac{P_{inv}}{V_{dc0}}, \quad y(\alpha) = (\alpha - 1)\frac{\pi}{3}\frac{P_{inv}}{V_{dc0}}. \tag{3.7}$$

Then the grid current i_g shown in Fig. 3.4 can be expressed as

$$i_g = \begin{cases} x(\alpha) + y(\alpha)\cos(\omega_g t - \frac{\pi}{6}) & @\, 0 \le t < \frac{T_g}{6} \\ 0 & @\, \frac{T_g}{6} \le t < \frac{2T_g}{6} \\ -x(\alpha) - y(\alpha)\cos(\omega_g t - \frac{5\pi}{6}) & @\, \frac{2T_g}{6} \le t < \frac{3T_g}{6} \\ -x(\alpha) - y(\alpha)\cos(\omega_g t - \frac{7\pi}{6}) & @\, \frac{3T_g}{6} \le t < \frac{4T_g}{6} \\ 0 & @\, \frac{4T_g}{6} \le t < \frac{5T_g}{6} \\ x(\alpha) + y(\alpha)\cos(\omega_g t - \frac{11\pi}{6}) & @\, \frac{5T_g}{6} \le t < T_g \end{cases}. \tag{3.8}$$

By using (3.8) and Fourier series, i_g can be represented as

$$i_g = a_0 + \sum_{n=1}^{\infty}\left(a_n \cos(n\omega_g t) + b_n \sin(n\omega_g t)\right), \tag{3.9}$$

where a_0 and b_n are zero, and a_n is

$$a_n = x(\alpha)\overbrace{\frac{2}{n\pi}\left(\sin(n\frac{\pi}{3}) + \sin(n\frac{2\pi}{3})\right)}^{O(n)} + y(\alpha)\frac{1}{\pi}\overbrace{\left\{\begin{array}{l}\frac{1}{n-1}\left(\sin(\frac{\pi}{3}n - \frac{\pi}{6}) - \sin\frac{\pi}{6} - \sin(\pi n - \frac{\pi}{6}) + \sin(\frac{2\pi}{3}n + \frac{\pi}{6})\right) \\ +\frac{1}{n+1}\left(\sin(\frac{\pi}{3}n + \frac{\pi}{6}) + \sin\frac{\pi}{6} - \sin(\pi n + \frac{\pi}{6}) + \sin(\frac{2\pi}{3}n - \frac{\pi}{6})\right)\end{array}\right\}}^{P(n)}. \tag{3.10}$$

By using (3.7) and (3.10), magnitude of each harmonics $|i_g(n)|$ is rearranged to

$$\left|i_g(n)\right| = a_n = \left|\begin{array}{l}\frac{P_{inv}}{V_{dc0}}\left(2O(n) - \frac{\pi}{3}P(n)\right) \\ \qquad + \frac{P_{inv}}{V_{dc0}}\left(\frac{\pi}{3}P(n) - O(n)\right)\alpha\end{array}\right|. \tag{3.11}$$

Here, the first and second terms of right side equation have opposite sign from the most of harmonics except 5th and even order harmonics. The magnitudes of high order harmonics are linearly proportional to α, so they keep decreasing or increasing as α is increased. By using this factor, grid current harmonics can be adjusted.

Figs. 3.5 and 3.6 show odd and even order harmonics, respectively, and Fig. 3.7 describes total harmonic distortion (THD) and PWHD. As α is increased, most of odd order harmonics shown in Fig. 3.5 are reduced except 5th order harmonic,

whereas even order harmonics shown in Fig. 3.6 are slightly increased. The increments of even order harmonics are relatively small in comparison with variations of odd order harmonics. From these figures, the point is that the harmonics are increased again when their sign is reversed. The magnitudes of 7^{th} and 13^{th} order harmonics rebound at $\alpha \geq 6.5$ and $\alpha \geq 8$ respectively, and the rebounded points of higher order harmonics are located further away. As shown in Fig. 3.7, therefore, the PWHD is steadily decreased since higher order harmonics over 14^{th} are decreased all.

For example, Fig. 3.8 shows the fast Fourier transform (FFT) results of the waveforms in comparison with grid regulation IEC61000-3-12 $R_{sce.min} = 350$. In the case of square wave ($\alpha = 1$), the harmonics of the waveform meets grid regulation except partial weighted harmonic distortion (PWHD). However, in case that $\alpha > 1$, PWHD is gradually decreased and satisfies the grid regulation of 45% at $\alpha = 3.7$ (PWHD = 44.96%). Although 5^{th} order and even-order harmonics are increased, they still have enough margin to reach grid regulations. Therefore, the system can satisfy grid regulation where $\alpha > 3.7$. By adopting this proposed method, the system always provides same harmonic spectrum regardless of P_{inv} since compensation harmonics is proportional to P_{inv}.

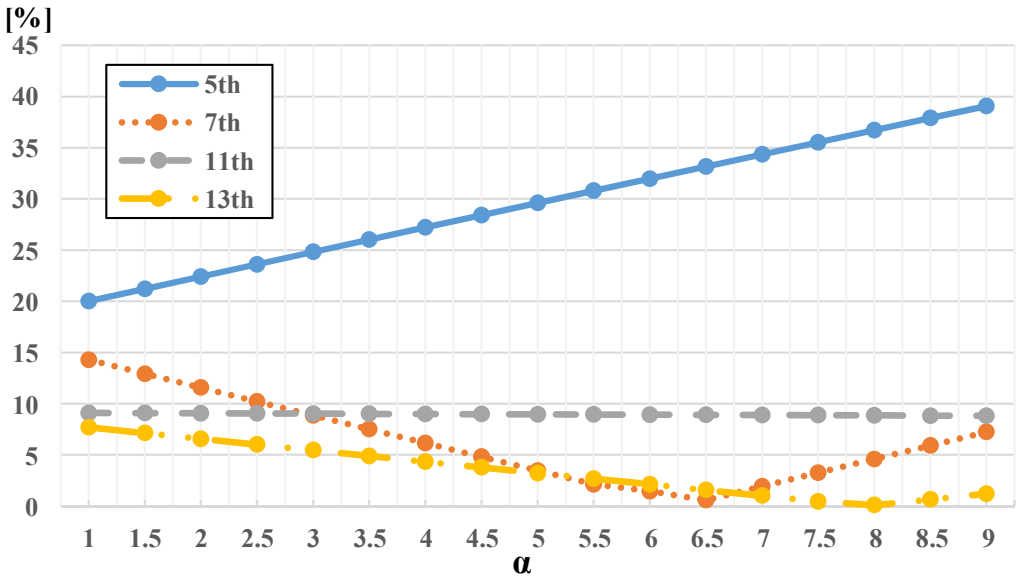


Fig. 3.5 Grid current odd order harmonics variations according to α.

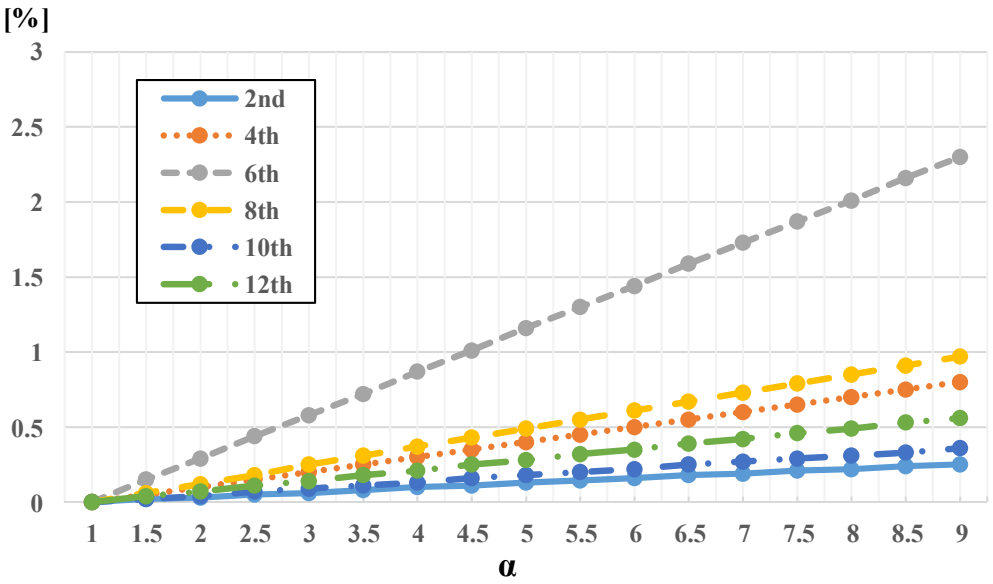


Fig. 3.6 Grid current even order harmonics variations according to α.

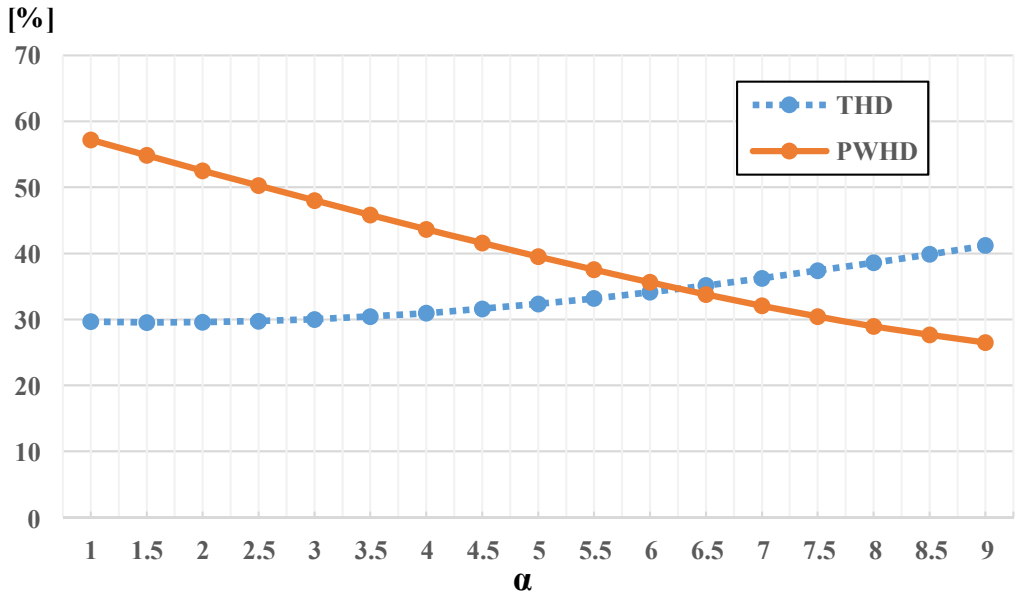


Fig. 3.7 Grid current THD and PWHD variations according to α.

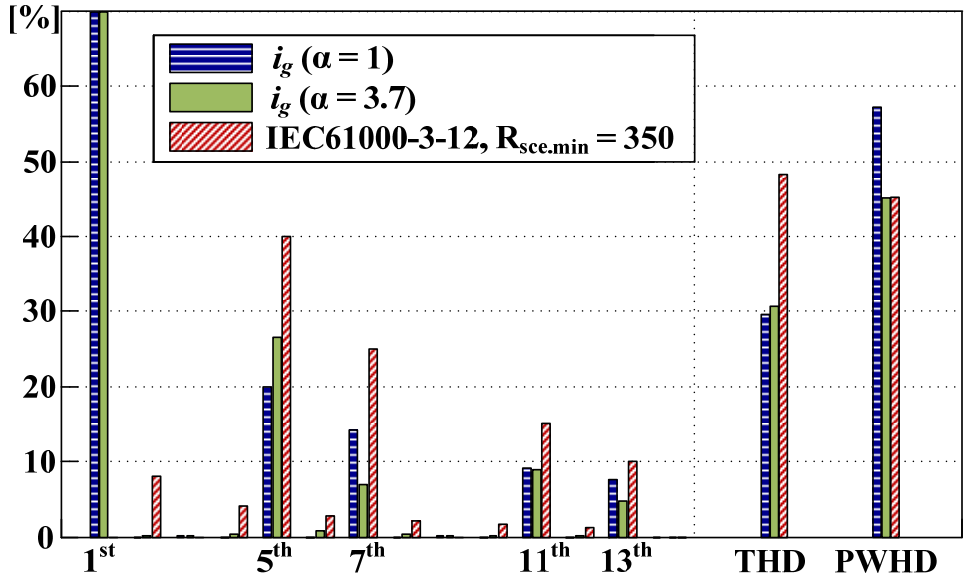


Fig. 3.8 Grid current harmonics where α = 1 and 3.7.

3.1.2 System Stability Analysis

In the proposed method, i_{comp} in (3.2) basically play a role of neutralizing the negative impedance characteristic of CPL. To verify it, the characteristic equation of this system can be derived by using equivalent circuit for diode rectifier system with CPL. In the equivalent circuit shown in Fig. 3.3, the loop equation from diode rectifier side is

$$v_{eq} = R_{eq} i_{diode} + L_{eq} \frac{di_{diode}}{dt} + v_{dc}, \tag{3.12}$$

And from the DC-link node, the capacitor equation is

$$C_{dc} \frac{dv_{dc}}{dt} = i_{diode} - i_{inv} - i_{comp}. \tag{3.13}$$

By substituting (3.13), (3.2), and (2.5) into (3.12), v_{dc} can be derived as

$$v_{dc} = \frac{\dfrac{v_{eq} V_{dc0} - R_{eq} P_{inv}}{L_{eq} C_{dc} V_{dc0}} - \dfrac{P_{inv}}{C_{dc} V_{dc0}} s}{s^2 + \left(\dfrac{R_{eq}}{L_{eq}} + \dfrac{(\alpha - 1) P_{inv}}{C_{dc} V_{dc0}^2} \right) s + \dfrac{V_{dc0}^2 + (\alpha - 1) P_{inv} R_{eq}}{L_{eq} C_{dc} V_{dc0}^2}}. \tag{3.14}$$

From (3.14), the system pole placement in accordance with varying α is shown in Fig. 3.9. The system is unstable at $\alpha = 0$ since the poles are on right half plain. Here, the system stability condition where the poles of (3.14) are located on left half plain can be calculated as

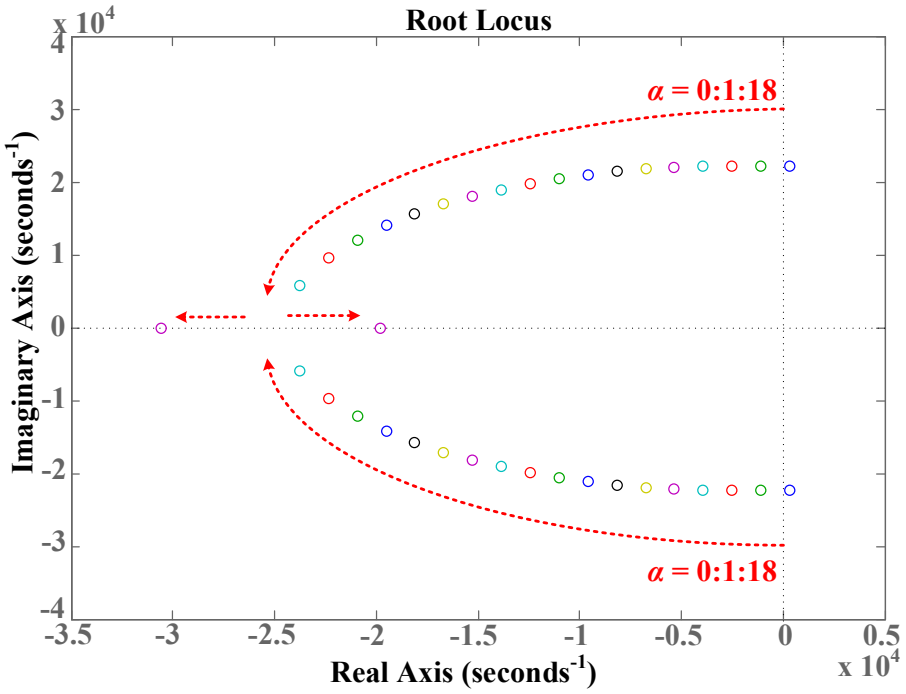


Fig. 3.9 Pole placement in accordance with varying α.

$$\alpha > 1 - \frac{R_{eq} C_{dc} V_{dc0}^2}{P_{inv} L_{eq}}. \tag{3.15}$$

For example, on the conditions that $R_g = 0.1\ \Omega$, $L_g = 50\ \mu H$ ($R_{eq} = 0.218\ \Omega$, $L_{eq} = 100\ \mu H$), $C_{dc} = 20\ \mu F$, $P_{inv} = 5.5$ kW, the system is stable where $\alpha > 0.31$. Therefore it is demonstrated that system stability is encouraged by harmonic compensation control which uses the range of $\alpha > 3.7$.

Since α is related to system design factor such as maximum available MI or capacity of DSC, it is recommended to choose the value as small as possible under

the condition that the system satisfies above two requirements: stability and harmonic regulations. By using circuit equations with chosen α, we can expect the specific values of voltages and currents, and it is possible to design the system parameters.

3.2 Implementation Based on Motor Drive Inverter

If the proposed i_{comp} injection method is implemented in the inverter, i_{comp} is generated by the inverter as shown in Fig. 3.10, and motor side power is not constant any longer. This implementation method is the best solution in terms of cost, but the motor drive operation is restricted since the inverter requires extra control margin for generating i_{comp}. This subsection presents the implementation method and relevant effects on the motor drive.

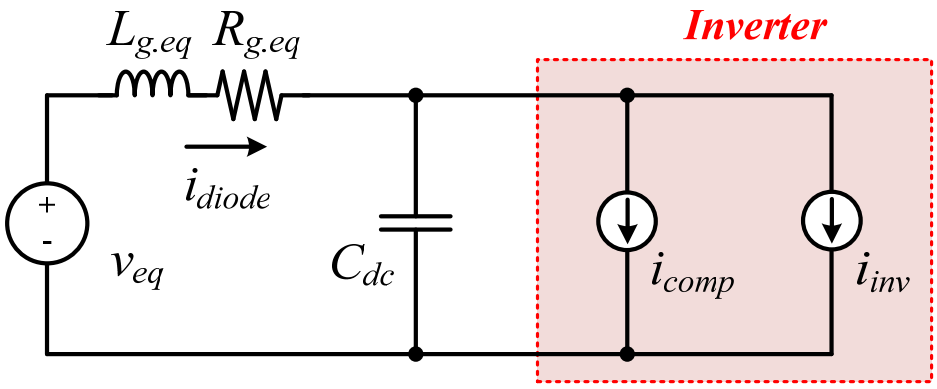


Fig. 3.10 Equivalent circuit for the proposed method implemented in the inverter.

3.2.1 Control Block Diagram

The control block diagram of proposed method for the inverter implementation is shown in Fig. 3.11. The blocks are divided into three parts: speed & current controller, grid current shaping, and voltage compensation blocks. The speed & current controller using dq-axis reference frame is widely used for the motor drive inverter, and each controller is composed of proportional-integral (PI) regulator [67]. In this cascaded control loop, the bandwidth of outer loop (speed control loop) ω_{sc} is much slower than that of inner loop (current control loop) ω_{cc}. Generally, ω_{sc} is set to several tens of rad/s and ω_{cc} is set to several hundreds of rad/s.

The proposed grid current shaping method requires high control bandwidth to generate *6m* harmonics ripple current, thus it adopts the voltage reference direct modification method that does not pass current control loop as explained in Section 2. The specific block diagram is described in Fig. 3.12. The *6m* harmonics of DC-link voltage is extracted by the BPF which has the Bode plot shown in Fig. 3.13. In this figure, the bandwidth of BPF ω_{BPF} is 360Hz and the damping ratio ζ_{BPF} shows the values of 1, 3, 5, and 10. If ζ_{BPF} is too small ($\zeta_{BPF} = 1$), *6m* harmonics are not clearly extracted, thus it is recommenced that ζ_{BPF} is set to be higher than 3. To apply the concept of i_{comp} into the dq-axis voltages, the ripple power relevant to i_{comp} is firstly required. The compensation power P_{comp} can be calculated as

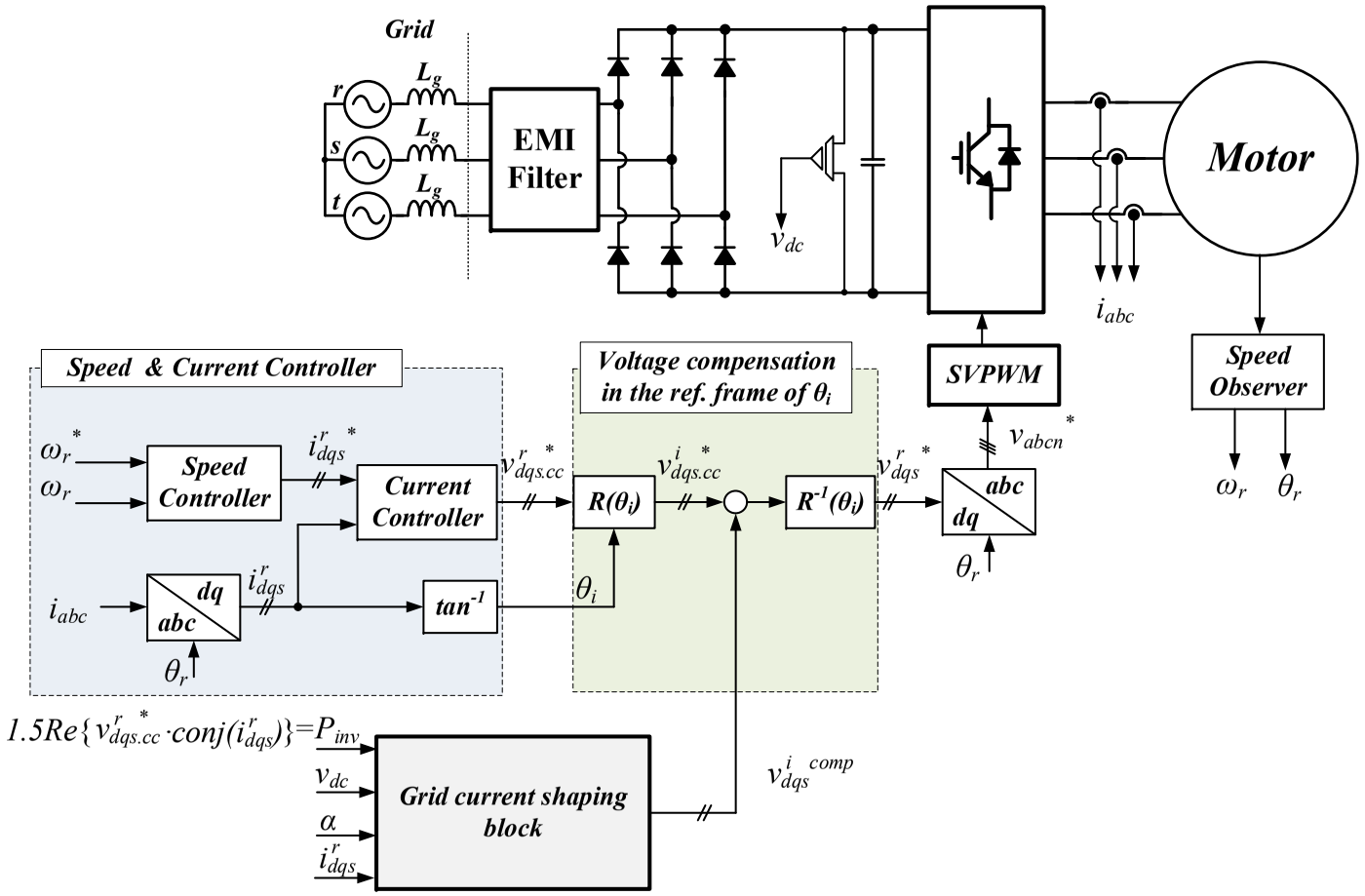


Fig. 3.11 Block diagram of proposed method implemented in the inverter.

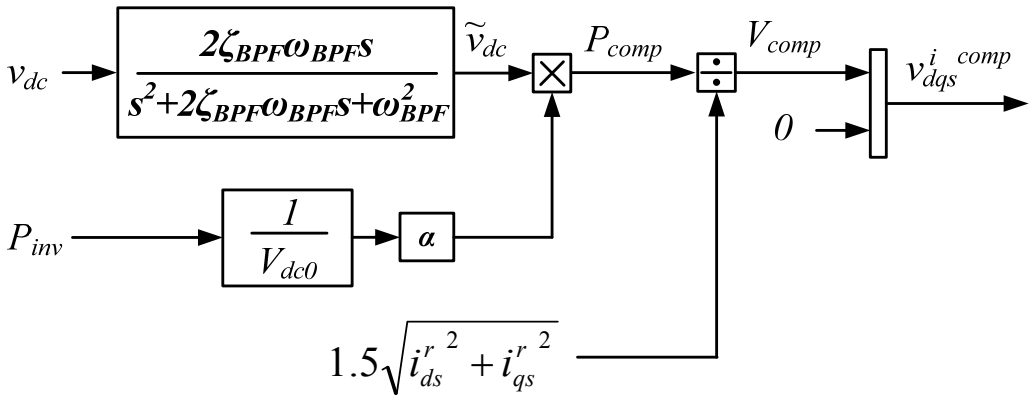


Fig. 3.12 Grid current shaping block for inverter implementation.

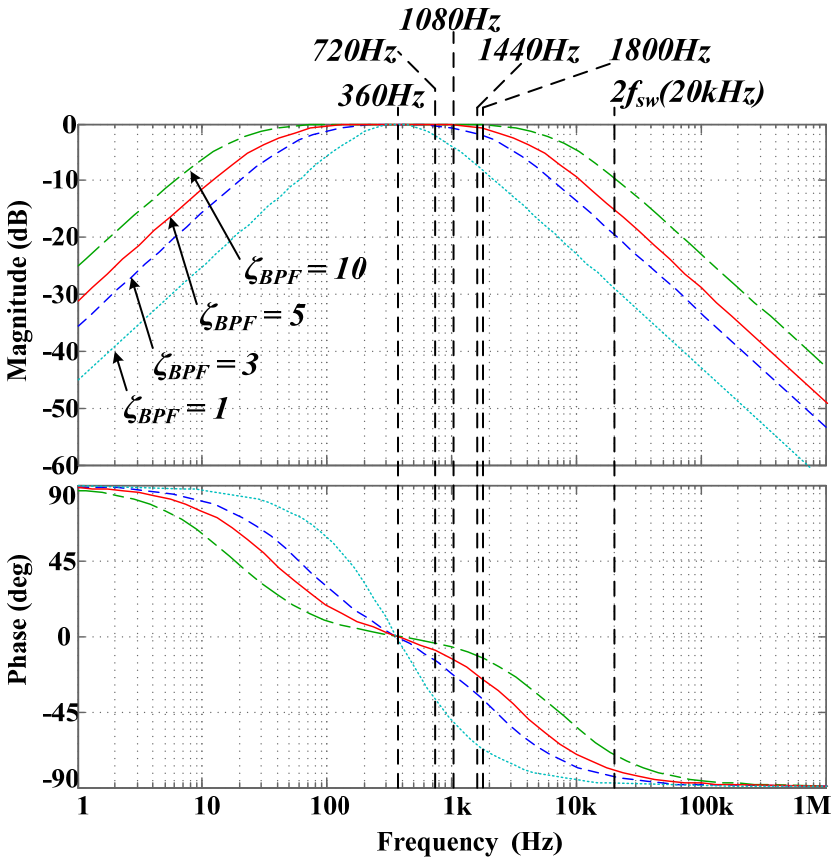


Fig. 3.13 Bode plot of band pass filter with various damping ratio.

$$P_{comp} = v_{dc} \cdot i_{comp} = \alpha \frac{P_{inv}}{V_{dc0}^2} v_{dc} \tilde{v}_{dc} . \tag{3.16}$$

The magnitude of compensation voltage V_{comp} in Fig. 3.12 is a scalar value that makes P_{comp} from the motor side. Thus, by using the magnitude of motor current, V_{comp} can be calculated as

$$V_{comp} = \frac{P_{comp}}{1.5\left|i_{dqs}^r\right|} = \frac{P_{comp}}{1.5\sqrt{{i_{ds}^r}^2 + {i_{qs}^r}^2}} . \tag{3.17}$$

where 1.5 is correction value for three-axis-to-two-axis transformation. As shown in Fig. 3.14, there are many candidates to satisfy the conditions that their magnitude is V_{comp} and the P_{comp} can be generated by multiplying motor current and them. Among them, the vector which is aligned to motor current vector is the shortest one that satisfies the above condition. It means that the compensation voltage can be minimized if the angle of compensation voltage is same with motor current vector. It can be easily realized that the V_{comp} totally becomes d-axis value in the reference frame of motor current angle θ_i. The d- and q-axes in the motor current vector reference frame are represented for d^i and q^i, respectively. Finally dq-axis compensation voltages ${v^i}_{dqs}^{comp}$ can be obtained as shown in Fig. 3.12, and they are added to the dq-axis current controller output voltages ${v^i}_{dqs.cc}^{*}$ which are transformed by rotation matrix of θ_i expressed as

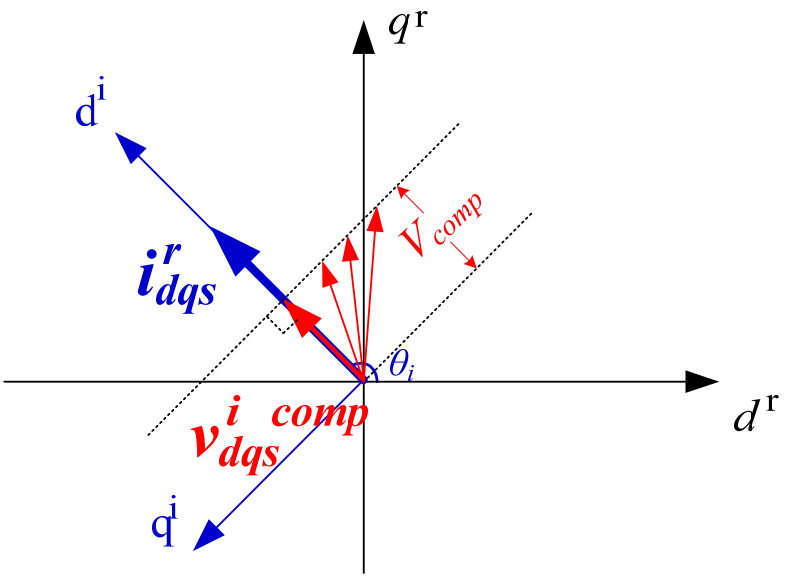


Fig. 3.14 Compensation voltage and motor current vector in the synchronous reference frame.

$$\begin{bmatrix} v^{i}_{ds.cc}{}^{*} \\ v^{i}_{qs.cc}{}^{*} \end{bmatrix} = \begin{bmatrix} \cos\theta_i & \sin\theta_i \\ -\sin\theta_i & \cos\theta_i \end{bmatrix} \begin{bmatrix} v^{r}_{ds.cc}{}^{*} \\ v^{r}_{qs.cc}{}^{*} \end{bmatrix}. \tag{3.18}$$

By using reverse-rotating transformation, the dq-axis reference voltages $v^{r}_{dqs}{}^{*}$ in the synchronous reference frame can be obtained as

$$\begin{bmatrix} v^{r}_{ds}{}^{*} \\ v^{r}_{qs}{}^{*} \end{bmatrix} = \begin{bmatrix} \cos\theta_i & -\sin\theta_i \\ \sin\theta_i & \cos\theta_i \end{bmatrix} \begin{bmatrix} v^{i}_{ds.cc}{}^{*} + v^{i}_{ds}{}^{comp} \\ v^{i}_{qs.cc}{}^{*} + v^{i}_{qs}{}^{comp} \end{bmatrix}. \tag{3.19}$$

where $v^{i}_{ds}{}^{comp} = V_{comp}$, $v^{i}_{qs}{}^{comp} = 0$. By synthesizing these voltage through SVPWM, the proposed method is successfully implemented in the inverter.

3.2.2 Effect on the Motor Drive System

As aforementioned, the motor drive system suffers performance degradation such as torque ripple and efficiency drop due to the grid current harmonics control. First, the toque ripple caused by P_{comp} can be calculated as follows. From the inverter side, power equation including P_{comp} is

$$P_{inv} + P_{comp} = 1.5(v_{ds}^r i_{ds}^r + v_{qs}^r i_{qs}^r) . \tag{3.20}$$

By using the motor voltage equation represented as

$$\begin{aligned} v_{ds}^r &= R_d i_{ds}^r + L_d \frac{di_{ds}^r}{dt} - \omega_r L_q i_{qs}^r \\ v_{qs}^r &= R_q i_{qs}^r + L_q \frac{di_{qs}^r}{dt} + \omega_r (L_d i_{ds}^r + \lambda_{pm}) \end{aligned} , \tag{3.21}$$

power equation in (3.20) is derived as

$$\begin{aligned} P_{inv} + P_{comp} &= 1.5 \begin{pmatrix} R_d {i_{ds}^r}^2 + R_q {i_{qs}^r}^2 + L_d i_{ds}^r \frac{di_{ds}^r}{dt} + L_q i_{qs}^r \frac{di_{qs}^r}{dt} \\ + \omega_r ((L_d - L_q) i_{ds}^r + \lambda_{pm}) i_{qs}^r \end{pmatrix}, \\ &= P_R + P_L + P_M \end{aligned} \tag{3.22}$$

where ω_r is motor electrical angular speed, and motor copper loss P_R, motor inductor power P_L, and motor output power P_M are

$$\begin{aligned} P_R &= 1.5(R_d {i_{ds}^r}^2 + R_q {i_{qs}^r}^2) \\ P_L &= 1.5(L_d i_{ds}^r \frac{di_{ds}^r}{dt} + L_q i_{qs}^r \frac{di_{qs}^r}{dt}) \\ P_M &= 1.5\omega_r ((L_d - L_q) i_{ds}^r + \lambda_{pm}) i_{qs}^r \end{aligned} . \tag{3.23}$$

By using P_M in (3.23), the motor torque T_e is represented as

$$T_e = \frac{P_M}{\omega_{rm}} = \frac{3}{4} P((L_d - L_q) i_{ds}^r + \lambda_{pm}) i_{qs}^r , \tag{3.24}$$

where P is pole of motor, ω_{rm} is motor mechanical angular speed, and $\omega_r = 0.5P\,\omega_{rm}$. To obtain P_M and T_e, we should calculate i^r_{dqs}. However, the differential equations from (3.20) and (3.21) are too complicated to solve exactly, so some assumption and iterative method are performed. At first, assuming that P_R and P_L are negligible, P_M can be represented as

$$P_M \approx P_{inv} + P_{comp} . \tag{3.25}$$

Then T_e and i^r_{qs} are calculated as (3.26) and (3.27), respectively.

$$T_e = \frac{P_M}{\omega_{rm}} \approx \frac{P_{inv} + P_{comp}}{\omega_{rm}} . \tag{3.26}$$

$$i_{qs}^r \approx \frac{T_e}{\frac{3P}{4}((L_d - L_q) i_{ds}^r + \lambda_{pm})} . \tag{3.27}$$

Assuming that i^r_{ds} is constant value which limits $|v^r_{dqs}|$ into $v_{dc}/\sqrt{3}$, i^r_{dqs} are obtained by using (3.20), (3.21), and (3.27). With i^r_{dqs}, P_R and P_L in (3.23) can be calculated and P_M is recalculated as

$$P_M = P_{inv} + P_{comp} - P_R - P_L . \tag{3.28}$$

Through the iterative calculation using (3.26), (3.27), and (3.28), relatively exact T_e

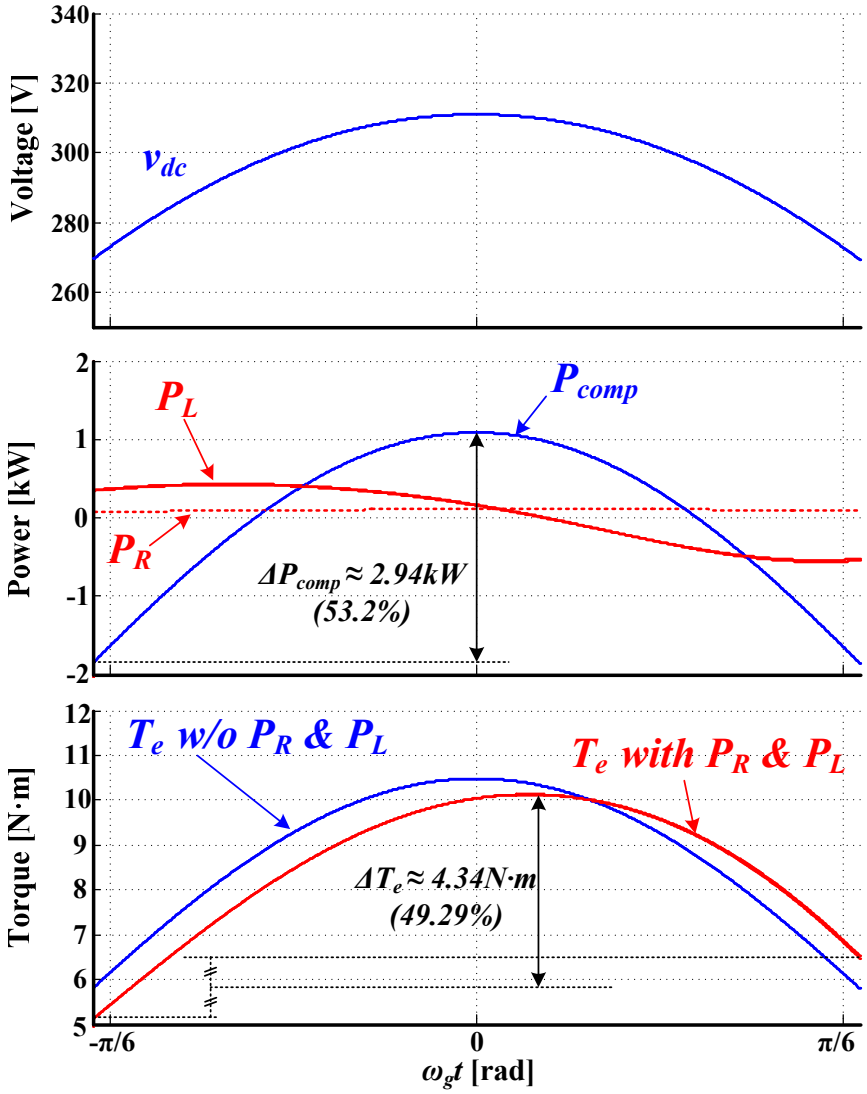


Fig. 3.15 DC-link voltage, compensation power, and load torque.

and i^r_{qs} can be calculated.

Fig. 3.15 shows the v_{dc}, P_{comp}, and T_e, where P_{inv} = 5.5 kW, V_m =311 V, P = 6, ω_r = 200π rad/s and α = 4. As shown in this figure, the waveform of T_e is different

from that of P_{comp} due to the effect of P_L. This situation highly depends on motor inductances, L_d and L_q. Here, it is seen that $T_e(-\pi/6)$ and $T_e(\pi/6)$ are not same since i^r_{ds} is assumed to be constant. In the simulation or experiment where the controller accurately modifies i^r_{ds}, they may be compensated and have same value. Based on the average value of two points, the system shows torque ripple of 49.29%.

Next, the increased magnitude of dq-axis reference voltages $|v^r_{dqs}|$ which is a

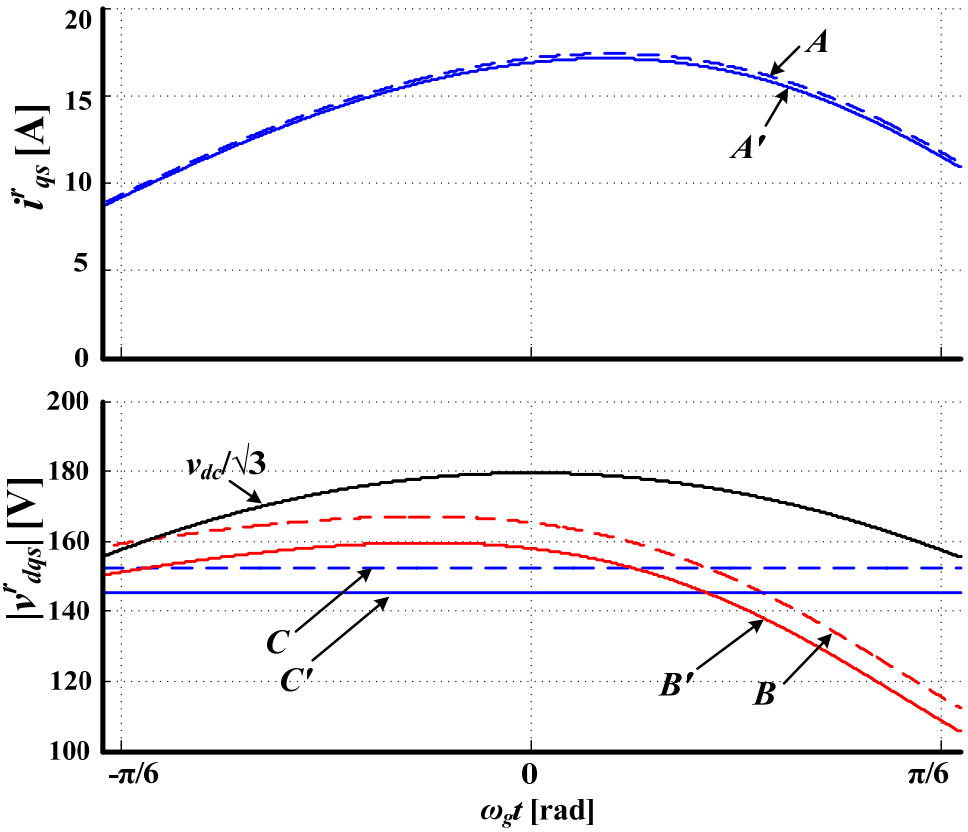


Fig. 3.16 q-axis current and the magnitude of output voltage.

demerit in the flux weakening area can be estimated. v^r_{dqs} is calculated by substituting i^r_{qs} obtained from above iterative calculation into (3.21), and then $|v^r_{dqs}|$ is illustrated as in Fig. 3.16 where L_d = 2.16 mH, L_q = 3.12 mH, λ_{pm} = 0.1097 V/(rad/s), R_d = 0.1 Ω, R_q = 0.1 Ω, V_{dc0} = 297 V, P_{inv} = 5500 W, and α = 4.

In this figure, dash and solid lines are drawn under the condition that i^r_{ds} = -21 A (*A*, *B*, *C*) and -23 A (*A'*, *B'*, *C'*), respectively. *A* and *A'* are i^r_{qs} curves, *B* and *B'* represent $|v^r_{dqs}|$ curves. In addition, *C* and *C'* are $|v^r_{dqs}|$ curves where i^r_{ds} and i^r_{qs} are constant values that provide P_{inv}. From the lower graph, it is verified that curve *B* exceeds the maximum available voltage boundary, $v_{dc}/\sqrt{3}$. To secure voltage margin, magnitude of flux weakening current (d-axis current) $|i^r_{ds}|$ should be increased, and then $|v^r_{dqs}|$ reaches to curve *B'*. On the other hand, in the case of the conventional output voltage on the condition of constant power, conventional $|v^r_{dqs}|$ is drawn as curve *C*, and the curve does not exceed $v_{dc}/\sqrt{3}$ in spite of relatively low d-axis current. This result demonstrates that the proposed method needs extra d-axis current in comparison with constant power output operation.

3.3 Three-Phase System with DSC

As mentioned in Section 3.2, the proposed method implemented in the inverter shows several degradations and limitations. They might lead to secondary problems

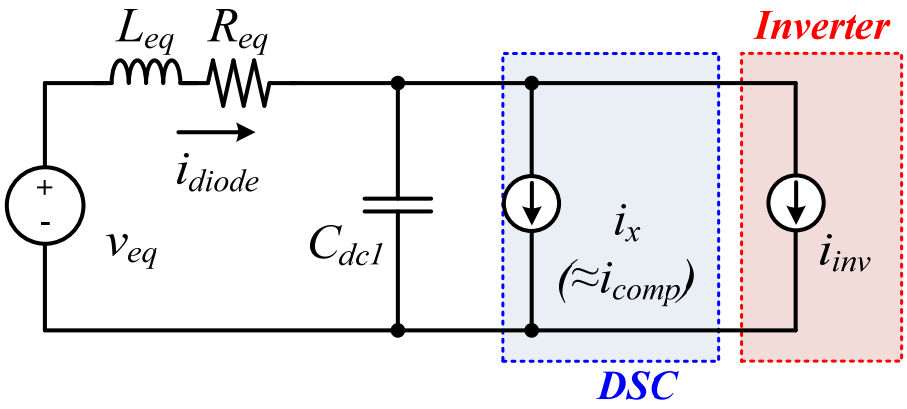


Fig. 3.17 Equivalent circuit for the proposed method implemented in the DSC.

such as efficiency drop or physical vibration. To cover them, the DSC which is a kind of parallel compensation is proposed. By introducing the DSC, the inverter and DSC separately manage i_{inv} and i_{comp}, respectively, as shown Fig. 3.17. Even though extra cost is charged due to the DSC, the previous inverter performance degradation can be resolved. Moreover, this current separating strategy even gives extra benefits in accordance with operating condition.

3.3.1 System Configuration

The configuration of total system including DSC is shown in Fig. 3.19. In comparison with the conventional diode rectifier system, the heavy DC inductor and DC-link capacitor are replaced with DSC. For the DSC, it is possible to adopt the converters that can transfer the power to floating capacitor C_{dc2}, for example,

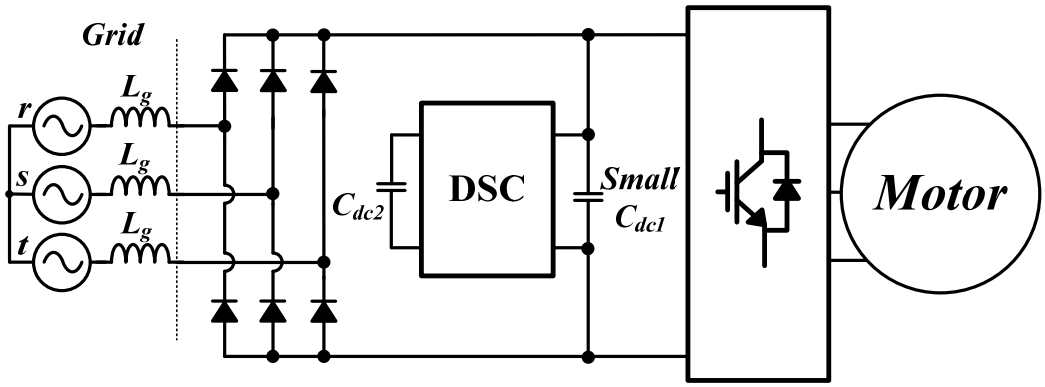
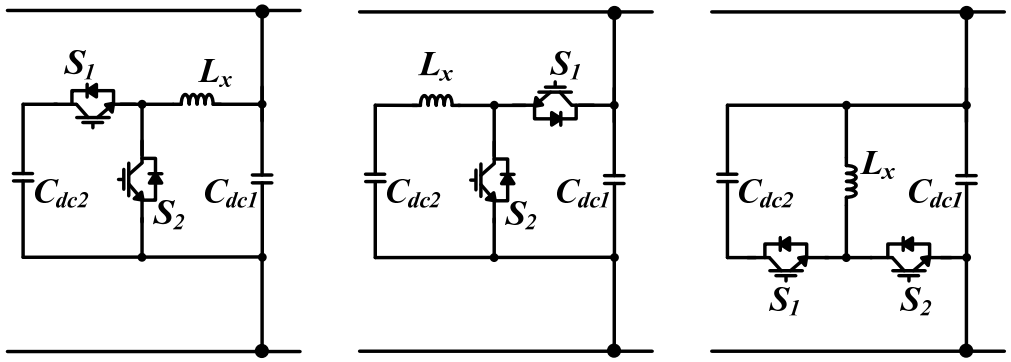


Fig. 3.19 Configuration of three-phase motor drive system with DSC.



(a) (b) (c)

Fig. 3.18 Various DSC structures: (a) boost, (b) buck, (c) buck-boost converters.

boost, buck, and buck-boost converters shown in Fig. 3.18. There are two important considerations to decide type of DSC: One is energy capacity and another is system miniaturization. For example, in cases of boost and buck converters, their capable energy can be calculated by using capacitor energy capacity,

$$E = \frac{1}{2} C_{dc2} (V_{dc2.\max}^2 - V_{dc2.\min}^2), \tag{3.29}$$

where maximum and minimum available capacitor voltages are $V_{dc2.max}$ and $V_{dc2.min}$. In the former case, E is 31950·C_{dc2} J where $V_{dc2.max}$ = 400V and $V_{dc2.min}$ = 310V, considering 220-V system with 600-V device. In contrast, E of the latter is 31250·C_{dc2} J where $V_{dc2.max}$ and $V_{dc2.min}$ are 250V and 0V. Therefore, the former has slightly high energy capacity. Furthermore, the DSC characteristics such as efficiency and design factor are changed because inductor current of the latter is higher than that of the former assuming that the average output current is same. Finally, the former has continuous output current which is great merit for the proposed control method, since the method is based on current injection. Thus this dissertation chooses boost converter as a DSC structure.

3.3.2 Control Method

The control block diagram for motor drive system including DSC is described in Fig. 3.20. The speed and current controller for inverter is exactly same as conventional one, and the control blocks for DSC are added. The blocks are divided into three parts: floating capacitor voltage v_{dc2} controller, grid current shaping block, and inductor current i_x controller.

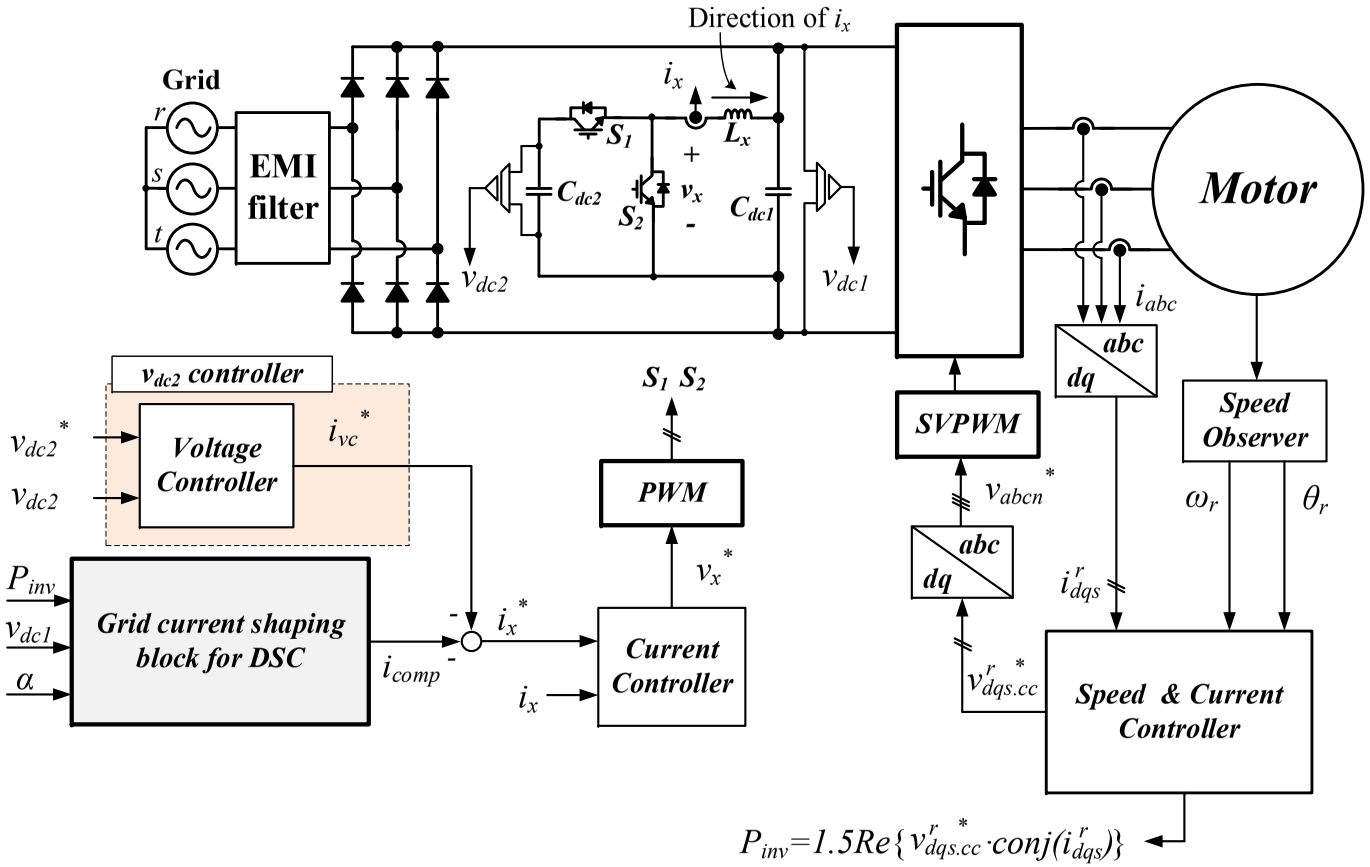


Fig. 3.20 Block diagram of proposed method implemented in the DSC.

In v_{dc2} controller whose specific block diagram is shown in Fig. 3.21, the average value of v_{dc2} is regulated as its reference value v_{dc2}^*. PI controller is used for the regulator, and the feedforward term $i_{dc2.ff}$ is added to the voltage controller output $i_{dc2.fb}$. The derivation of feedforward term is explained in following Section 3.3.3. Finally, the C_{dc2} current reference i_{vc}^* is generated after passing a notch filter which is designed for removing ripples which come from v_{dc2}. Since the main frequency of this ripple is $6\omega_g$ (ω_g =120π rad/s), the bandwidth of notch filter ω_{NF} is designed as 720π rad/s and damping ration ζ_{NF} is set to 0.707.

To design two gains of voltage controller, $k_{i.vc}$ and $k_{p.vc}$, the transfer function of voltage controller can be derived as (3.30). Here, the notch filter is neglected considering that the bandwidth of voltage controller ω_{vc} is much smaller than ω_{NF}. Therefore transfer function of notch filter can be assumed unity near ω_{vc}.

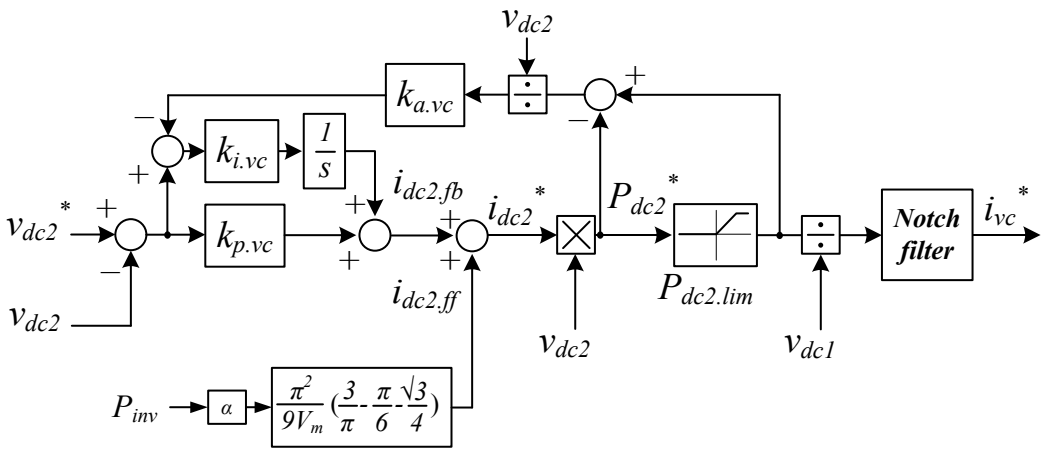


Fig. 3.21 Control block diagram of v_{dc2} controller.

$$\frac{v_{dc2}}{v_{dc2}^*} = \frac{\frac{k_{p.vc}}{C_{dc2}}s + \frac{k_{i.vc}}{C_{dc2}}}{s^2 + \frac{k_{p.vc}}{C_{dc2}}s + \frac{k_{i.vc}}{C_{dc2}}}. \tag{3.30}$$

Comparing with the general form of second order transfer function represented as

$$\frac{v_{dc2}}{v_{dc2}^*} = \frac{2\zeta_{vc}\omega_{vc}s + \omega_{vc}^2}{s^2 + 2\zeta_{vc}\omega_{vc}s + \omega_{vc}^2}, \tag{3.31}$$

the $k_{p.vc}$ and $k_{i.vc}$ are set to

$$k_{p.vc} = 2C_{dc2}\zeta_{vc}\omega_{vc}, \quad k_{i.vc} = C_{dc2}\omega_{vc}^2, \tag{3.32}$$

respectively. Here, the $k_{a.vc}$ is set to $1/k_{p.vc}$.

The transfer function including notch filter is derived as

$$\frac{v_{dc2}}{v_{dc2}^*} = \frac{\frac{k_{p.vc}}{C_{dc2}}s^3 + \frac{k_{i.vc}}{C_{dc2}}s^2 + \frac{\omega_{NF}^2 k_{p.vc}}{C_{dc2}}s + \frac{\omega_{NF}^2 k_{i.vc}}{C_{dc2}}}{s^4 + (2\zeta_{NF}\omega_{NF} + \frac{k_{p.vc}}{C_{dc2}})s^3 + (\omega_{NF}^2 + \frac{k_{i.vc}}{C_{dc2}})s^2 + \frac{\omega_{NF}^2 k_{p.vc}}{C_{dc2}}s + \frac{\omega_{NF}^2 k_{i.vc}}{C_{dc2}}}, \tag{3.33}$$

and its Bode plot is shown in Fig. 3.22, where ω_{vc} is 20π rad/s and ζ_{vc} is varied from 0.707 to 5. As shown in this figure, if ζ_{vc} is too small, transfer function shows overshoot near ω_{vc}. To mitigate it, it is good to set ζ_{vc} high enough. However, the gain of high frequency region becomes higher as ζ_{vc} is increased, thus it is recommended to design ζ_{vc} around 3~5.

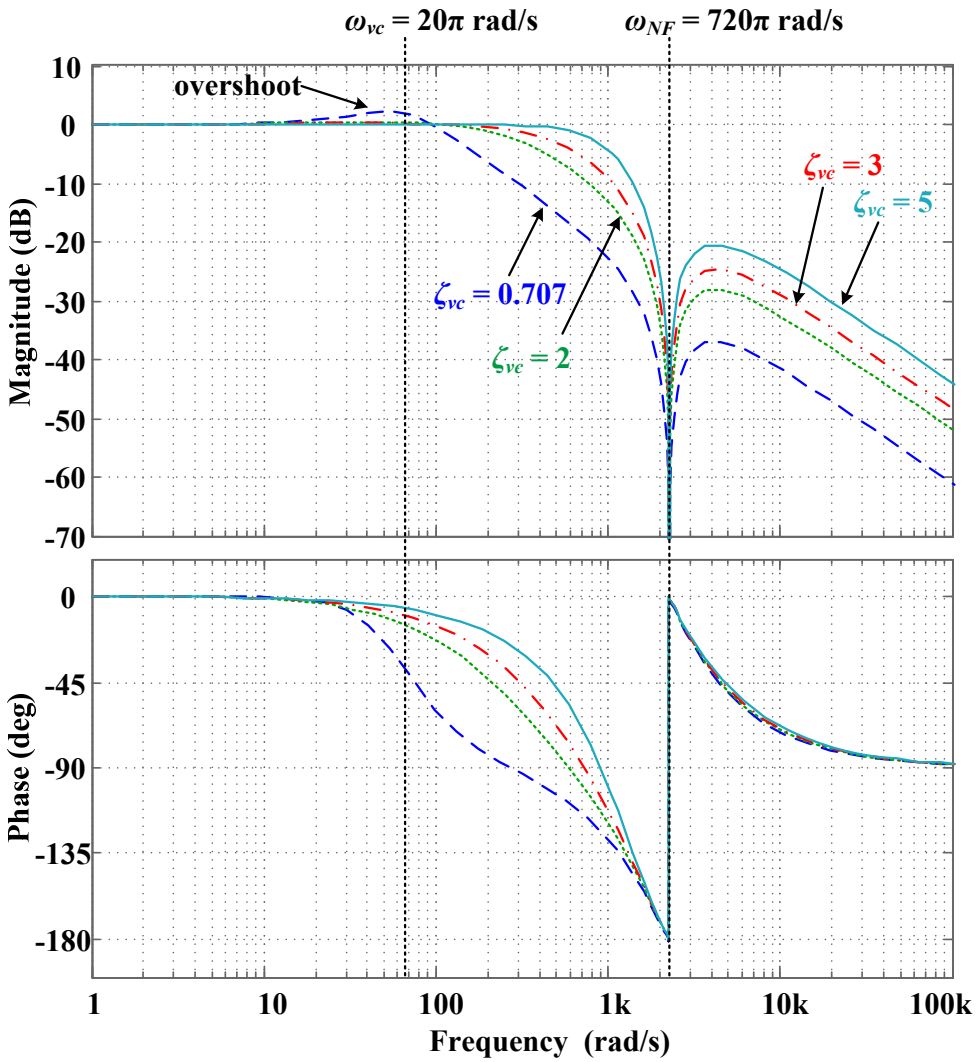


Fig. 3.22 Bode plot of v_{dc2} controller with various ζ_{vc}.

The grid current shaping block products compensation current, i_{comp} which is key idea as explained in Section 3.1. The block diagram is shown in Fig. 3.23 in detail. The BPF is designed same as Fig. 3.13, and i_{comp} can be calculated as (3.2).

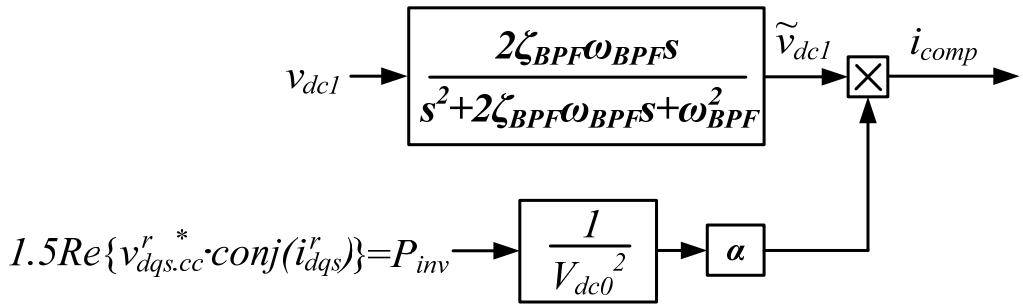


Fig. 3.23 Control block diagram of grid current shaping implemented in DSC.

The outputs of two above controllers becomes DSC current reference i_x^* as expressed in

$$i_x^* = -(i_{vc}^* + i_{comp}). \tag{3.34}$$

Considering the current direction, the minus sign is added in (3.34). Even though i_{vc}^* is additionally included, i_{vc}^* rarely effects on grid current harmonic since it is small enough in comparison with i_{comp}. i_x^* becomes the input of current controller, and its block diagram is illustrated in Fig. 3.24. The PI controller is also used, and three gains, $k_{p.cc}$, $k_{i.cc}$ and $k_{a.cc,}$ are set to

$$k_{p.cc} = L_x\omega_{cc},\ \ k_{i.cc} = R_x\omega_{cc}, \text{ and } \ k_{a.cc} = 1/k_{p.cc}, \tag{3.35}$$

respectively, where L_x is inductor, R_x is ESR of L_x, and ω_{cc} is the bandwidth of current controller. Then the transfer function of this controller is

$$\frac{i_x}{i_x^*} = \frac{\omega_{cc}}{s+\omega_{cc}}. \tag{3.36}$$

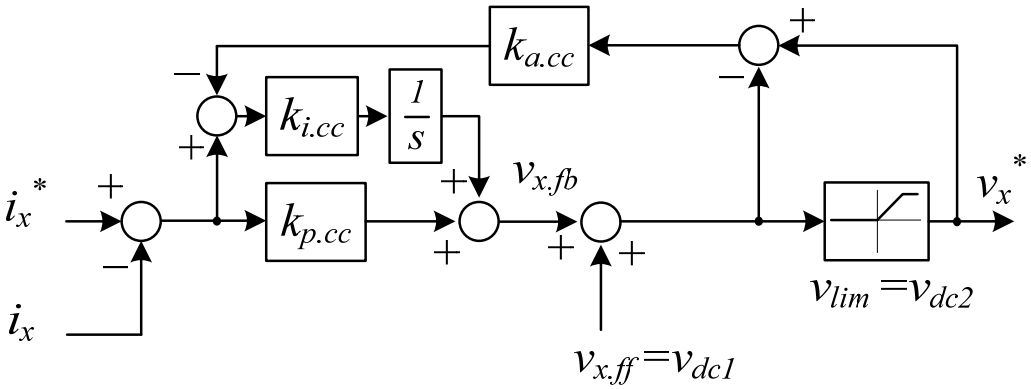


Fig. 3.24 Control block diagram of i_x current controller.

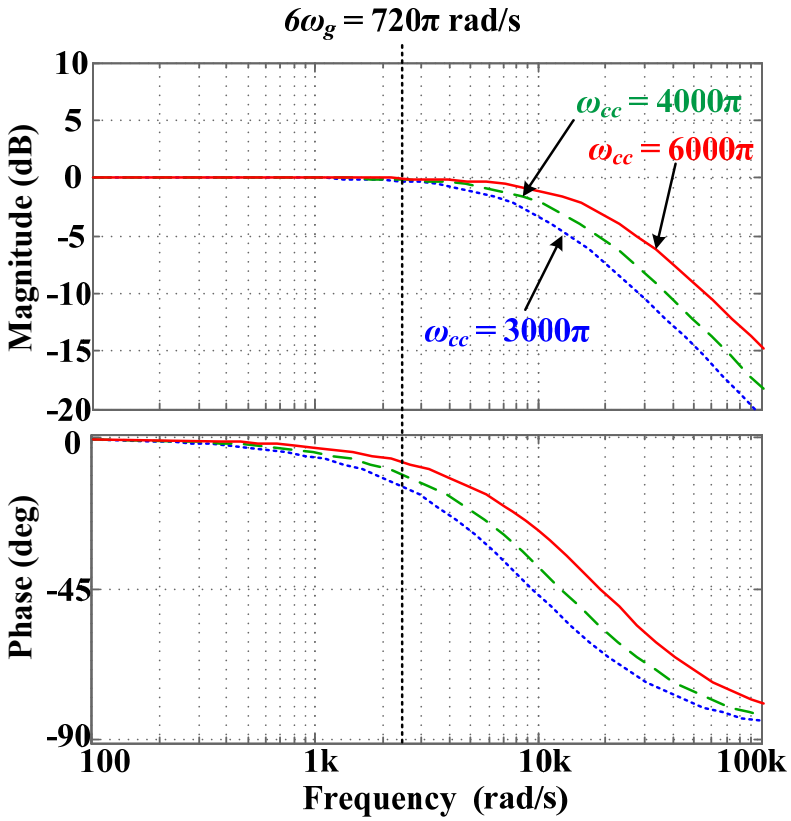


Fig. 3.25 Bode plot of i_x current controller with various ω_{cc}.

From Bode plot of current controller shown in Fig. 3.25, it is desired to design ω_{cc} as high as possible, because i_x^* contains $6m$ harmonics of ω_g. However, the switching frequency of DSC should be also considered when we design ω_{cc}.

3.3.3 System Design Guideline

i) C_{dc2} design

In the DSC system, the role of C_{dc2} is to absorb the ripple, and the capacitance should be designed considering a variation of the v_{dc2} caused by the ripple. A maximum available voltage $V_{dc2.max}$ is commonly decided by the voltage rating of used components such as the switching device or capacitor, and a minimum voltage limitation $V_{dc2.min}$ is decided as a value higher than v_{dc1}. The minimum limitation is related to the duty margin of boost type DSC, in other words, the duty of DSC should be maintained under the unity. For example, in the case of 220-V three-phase grid tied system, 600-V switching devices are used, and v_{dc1} is maximum value of line-to-line voltage and its peak value is 311 V. Then the $V_{dc2.max}$ is set to 400 V considering safety level against voltage spiking from each switching device, and $V_{dc2.min}$ is chosen as 320 V considering voltage ripples in v_{dc1} owing to the switching current.

Assuming that i_x is well controlled as (3.34), the capacitor energy equation from C_{dc2} is

$$\frac{1}{2}C_{dc2}v_{dc2}^2 = \int(-v_x i_x)dt + C\,, \tag{3.37}$$

where v_x is an average leg output voltage in Fig. 3.20 and C is integral coefficient. Assuming that ESR of L_x is neglected, v_x is derived as

$$v_x = L_x\frac{di_x}{dt} + v_{dc1}\,. \tag{3.38}$$

By substituting (3.34) and (3.38) into (3.37), v_{dc2} is calculated in (3.39) during $-\pi/6 < \omega_g t < \pi/6$.

$$v_{dc2} = \sqrt{\frac{2}{C_{dc2}}\left\{\begin{array}{l}\alpha\dfrac{\pi^2 P_{inv}}{9}\left(\begin{array}{l}\dfrac{1}{2}t + \dfrac{1}{4\omega_g}\sin 2\omega_g t - \dfrac{\alpha L_x \pi^2 P_{inv}}{36V_m^2}\cos 2\omega_g t \\ + \dfrac{\alpha L_x \pi P_{inv}}{3V_m^2}\cos\omega_g t - \dfrac{3}{\pi\omega_g}\sin\omega_g t\end{array}\right) \\ - I_{dc2}\left(\dfrac{\alpha L_x \pi^2 P_{inv}}{9V_m}\cos\omega_g t - \dfrac{V_m}{\omega_g}\sin\omega_g t\right)\end{array}\right\} + \frac{2C}{C_{dc2}}}\,. \tag{3.39}$$

Here, v_{dc1} is assumed as $V_m cos(\omega_g t)$ for the convenient calculation. In (3.39), I_{dc2} is not neglected because it is necessary to maintain balance of capacitor energy from (3.37). By using that $v_{dc2}(-\pi/(6\omega_g))$ and $v_{dc2}(\pi/(6\omega_g))$ should be same, I_{dc2} is expressed as

$$I_{dc2} = \frac{\alpha\pi^2 P_{inv}}{9V_m}\left(\frac{3}{\pi} - \frac{\pi}{6} - \frac{\sqrt{3}}{4}\right) \equiv i_{dc2\_ff}\,. \tag{3.40}$$

For example, I_{dc2} is -0.13 A where P_{inv} = 5.5 kW, V_m = 311 V, α = 4. This value is negligible in comparison with i_{comp}, but it keeps energy of C_{dc2} be balanced. Since

I_{dc2} is covered by voltage controller in Fig. 3.21, the value in (3.40) is used for feedforward of this controller. From (3.39), C is calculated as (3.41) by using that the average value of v_{dc2} is v_{dc2}^*.

$$C = \frac{C_{dc2} v_{dc2}^{*\,2}}{2} - \left(\frac{\alpha^2 \pi^4 L_x P_{inv}^2}{324 V_m^2} (\frac{\pi}{\sqrt{3}} + 1) \right). \tag{3.41}$$

Fig. 3.26 shows v_{dc2} in accordance with various C_{dc2}. From (3.39), the peak value of v_{dc2} becomes 400 V where C_{dc2} is around 38μF. Therefore v_{dc2} is bounded between $V_{dc2.max}$ and $V_{dc2.min}$ where $C_{dc2} \geq 38$ μF. The duty of DSC D_x expressed in (3.42) is also illustrated in Fig. 3.26.

$$D_x = \frac{v_x}{v_{dc2}}. \tag{3.42}$$

In the case that $C_{dc2} > 38$ μF, since v_{dc2} is always higher than v_{dc1}, it is guaranteed that D_x is not exceed unity.

ii) L_x and C_{dc1} design

L_x from DSC system is related with current synthesis and switching ripple current of i_x. Since i_x is varied sharply and the basic concept of proposed control is current injection, it is advantageous to choose high switching frequency $f_{sw.DSC}$. By using inductor voltage equation at boost converter turn-on state, the value of L_x is calculated as

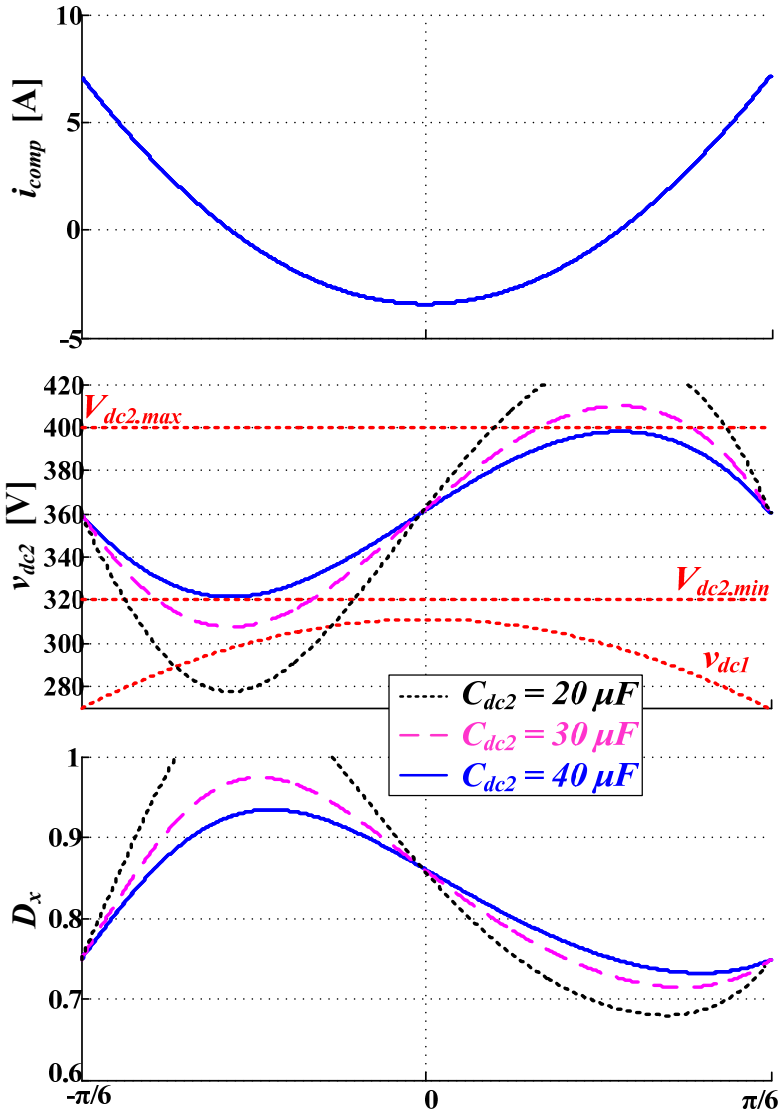


Fig. 3.26 v_{dc2} variation in accordance with various C_{dc2} where P_{inv} = 5.5kW, v_{dc2}^* = 360V, and α.

$$L_x = \frac{(v_{dc2} - v_{dc1})T_{sw}D_x}{\Delta i_x}, \tag{3.43}$$

where Δi_x is switching ripple of i_x. Here, $f_{sw.DSC}$ is set to 20 kHz considering maximum switching frequency of IGBT, and the Δi_x is chosen as 4 A in order that peak value of $(i_x + 0.5\Delta i_x)$ should not be exceed 10 A. And then L_x becomes 0.9 mH.

C_{dc1} in DSC system plays a role of switching ripple absorbing filter. The switching ripples come from both motor drive circuit and DSC, but the ripple from motor drive circuit is normally much higher than that from DSC. C_{dc1} is usually chosen sufficient value in order that the peak value of v_{dc1} is not exceed $V_{dc2.min}$. However, if the value of C_{dc1} is too high, it has notorious influence on grid current harmonic. In addition, it is advantageous to place f_r over 2.4 kHz (40^{th} order harmonic) to avoid grid harmonic regulation. Thus C_{dc1} is chosen as 20 μF and f_r becomes 3.56 kHz.

3.4 Simulation and Experimental Results

In the simulation and experiment, 220-V 5.5-kW laboratory prototype motor drive system was executed. The system conditions are shown in Table 3.2. For the simulation tool, PSIM is used and four systems are compared: conventional diode rectifier system with heavy passive components, conventional small DC-link capacitor system with or without grid filter inductor, and the DSC system.

Fig. 3.27 shows the simulation results of the diode rectifier system which uses DC inductor of 0.7 mH and DC-link capacitor of 2.2 mF. The three-phase grid

Table 3.2 System conditions and parameters

Condition	Value
Grid voltage	220 V
Grid angular frequency, ω_g	377 rad/s
Maximum speed, $\omega_{rpm.max}$	6000 r/min
Rated power, P_{rated}	5500 W
Inverter switching frequency, $f_{sw.inv}$	10 kHz
DSC switching frequency, $f_{sw.DSC}$	20 kHz
DC-link capacitor, C_{dc1}	20 μF
Floating capacitor, C_{dc2}	47μF
DSC inductor, L_x	0.9 mH
Motor parameter	
d-axis inductance, L_d	2.16 mH
q-axis inductance, L_q	3.12 mH
Phase resistance, R_s	0.1 Ω
Flux linkage, λ_{pm}	0.1097 V/(rad/s)
Pole, P	6

currents indicated in Fig. 3.27(a) have values of 29 A_{peak} and 16 A_{rms}, and they satisfy the grid regulation and the system shows high quality of output torque in Fig. 3.27(c). The DC-link voltage is slightly decreased owing to the voltage drop in DC inductor, so it has average value of 295 V.

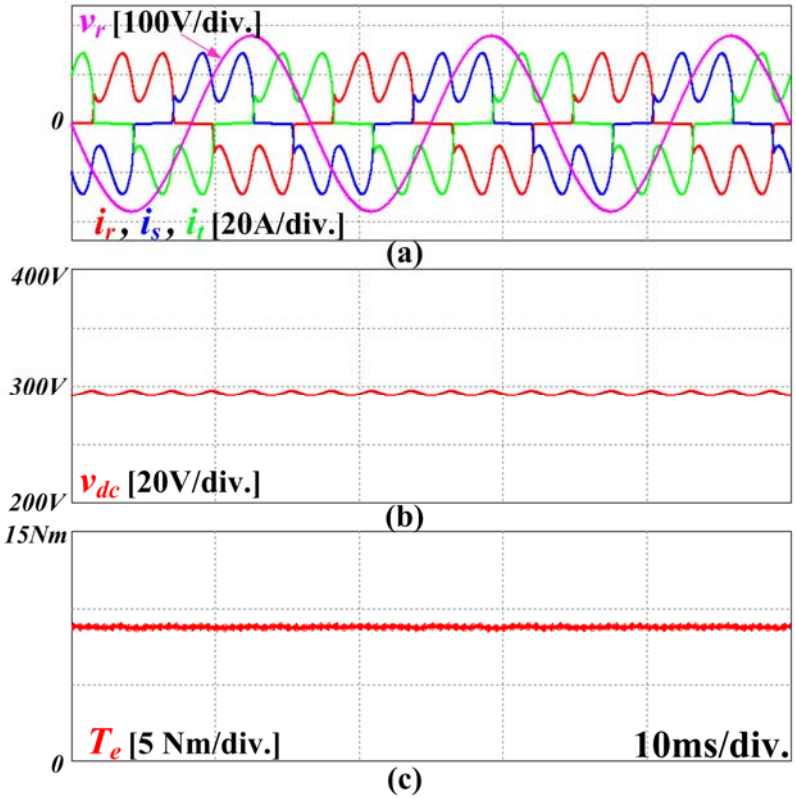


Fig. 3.27 Simulation results of conventional diode rectifier system with heavy passive components.

Fig. 3.28 exhibits the simulation results of diode rectifier system with DC-link voltage stabilization control where the capacitance is 20 μF and the value of DC inductor is 0.7 mH. The system is operated stably and satisfies grid regulation with reduced passive components, but motor side output performances are inevitably degraded due to the stabilization control in [11][12]. The output torque in Fig. 3.28(c) shows 18% increased peak value and contains 45% ripple per rated torque.

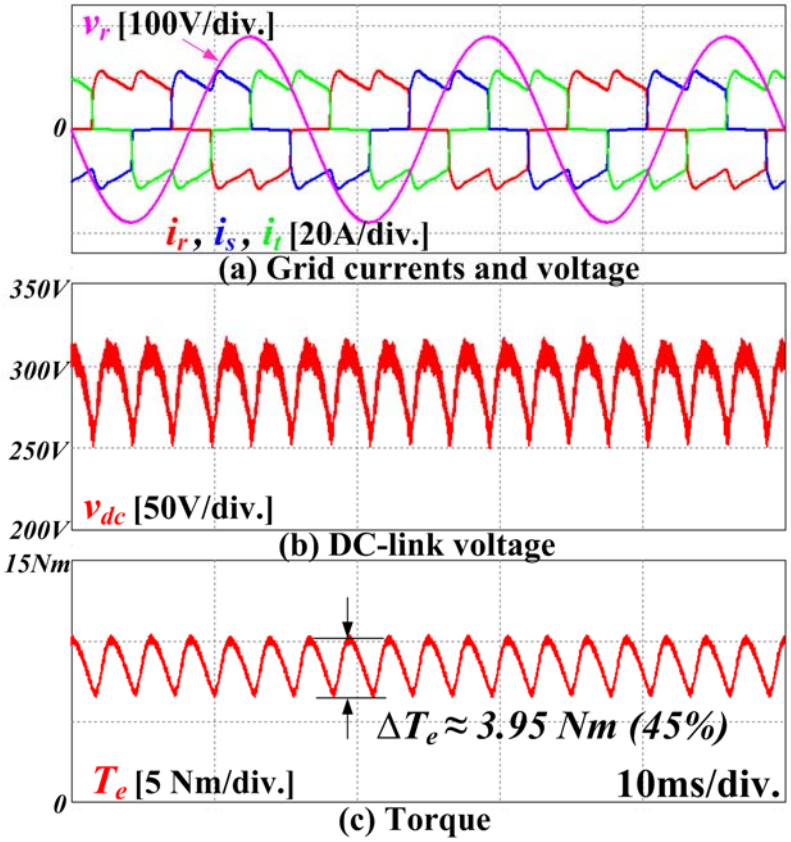


Fig. 3.28 Simulation results of small DC-link capacitor system with DC-link voltage stabilization control.

In Figs. 3.29 and 3.30, the simulation results of grid current shaping method implemented in the inverter and DSC, where P_{inv} = 5.5 kW and α = 4. In these systems, 20 μF of main DC-link capacitor is used and the grid filter inductor is removed. In the case of DSC system, two switching devices of 600-V&10-A, an inductor L_x which has value of 0.9 mH with greatly reduced current rating, and two

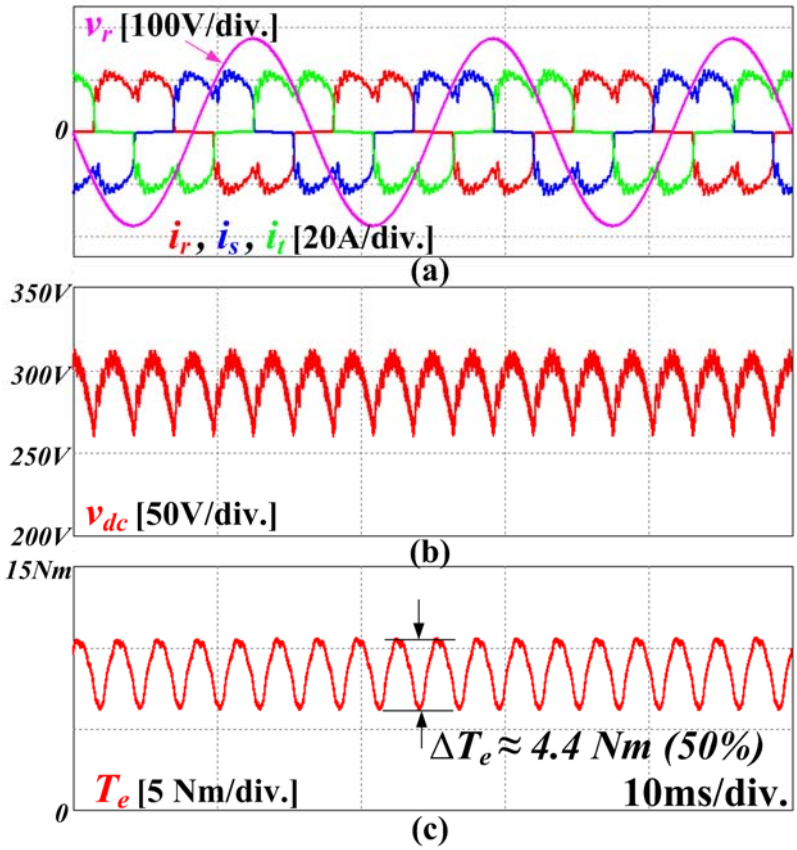


Fig. 3.29 Simulation results of grid current shaping control implemented in the inverter.

capacitors (20 μF, 47 μF) are used.

The Figs. 3.29(a) and 3.30(a) illustrate the *r*-phase grid voltage v_r and three-phase grid currents i_r, i_s, i_t. The currents are smoothly controlled as desired value shown in Fig. 3.4 and they have the values of 24 A_{peak} and 16 A_{rms}. In Figs. 3.29(b) and 3.30(b), it is verified that the main DC-link voltage is regulated as maximum of

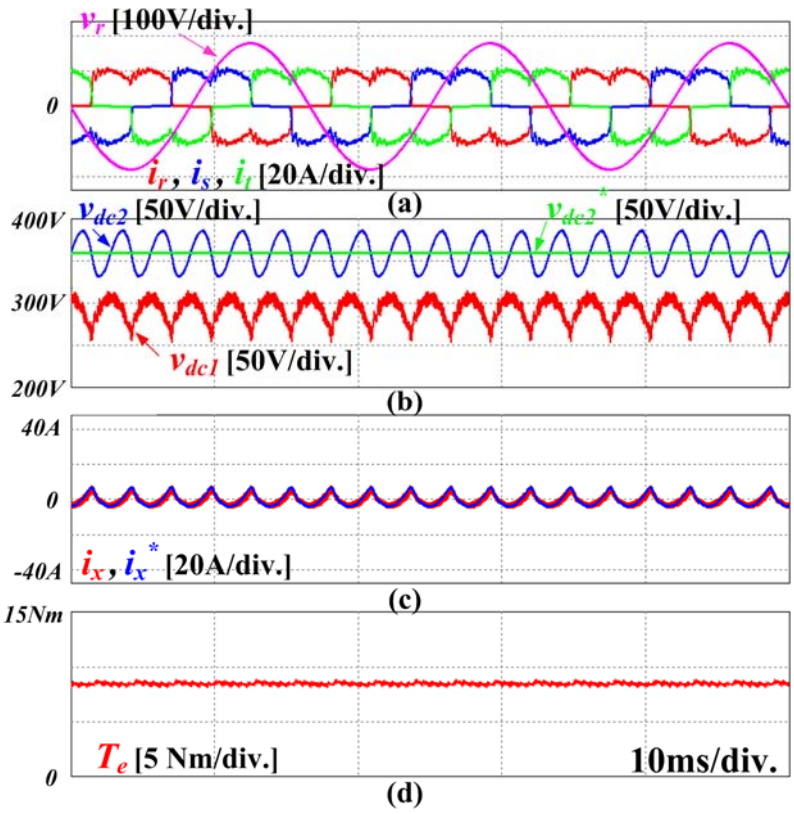


Fig. 3.30 Simulation results of grid current shaping control implemented in DSC.

line-to-line grid voltages without unstable oscillation, and the DSC system shows that v_{dc2} which absorbs ripple energy is bounded into the range from $V_{dc2.min}$ (320 V) to $V_{dc2.max}$ (400 V) as we desired. This range is able to be adjusted by designing the value of C_{dc2}. Fig. 3.30(c) shows i_x which has values of 8 A_{peak} and 3.4 A_{rms}. In Fig. 3.29(c), as explained in Section 3.2.2, motor has about 50% torque ripple, while the DSC system can obtain smooth output torque as shown in Fig. 3.30(d).

In the experimental results, the system conditions were established as same as that in case of simulation. TMS320F28335 was used for digital signal processor and the interior permanent magnet synchronous motor (IPMSM) for air compressor was tested. The motor-generator laboratory set (MG set) was built and generator was controlled by back-to-back converter tied to the three-phase grid as shown in Fig. 3.31. Electromagnetic interference (EMI) filter was adopted in all systems.

Fig. 3.32 shows the experimental waveforms of the conventional systems mentioned above. The waveforms demonstrate the validity of simulation results and it means that the torque ripple shown in Fig. 3.28(c) also occurs in the motor. Fig.

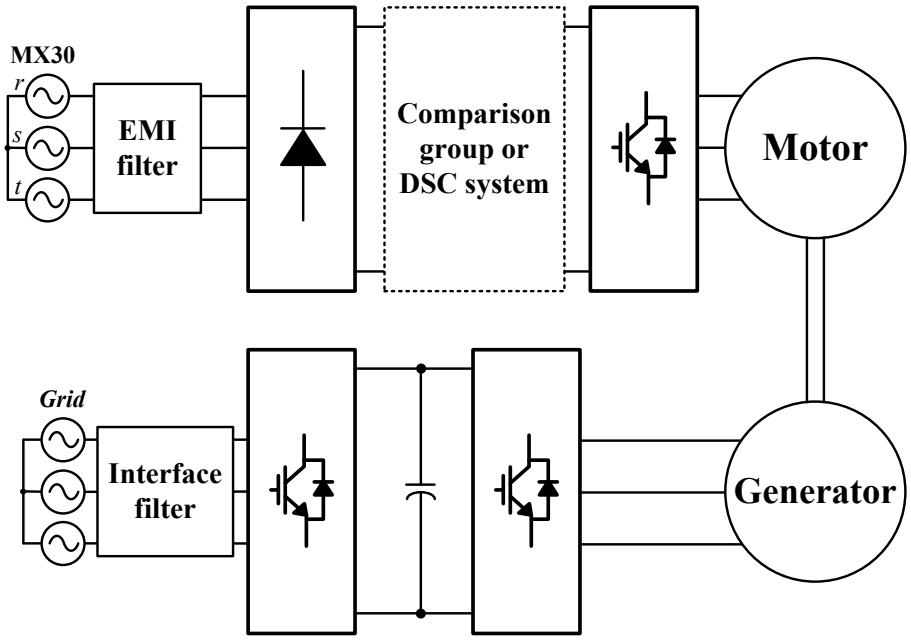
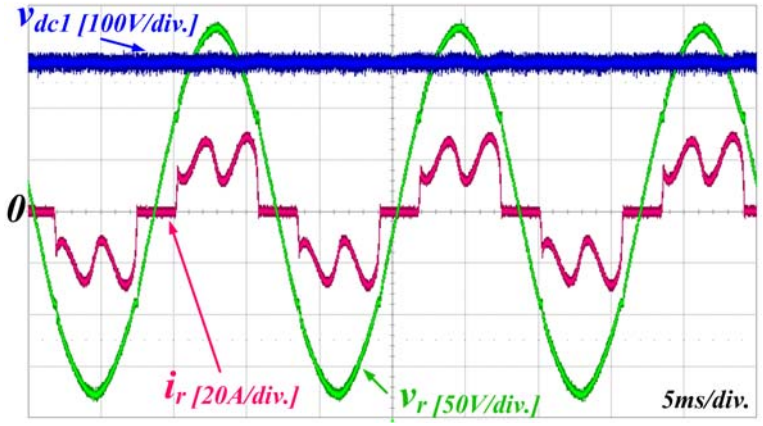
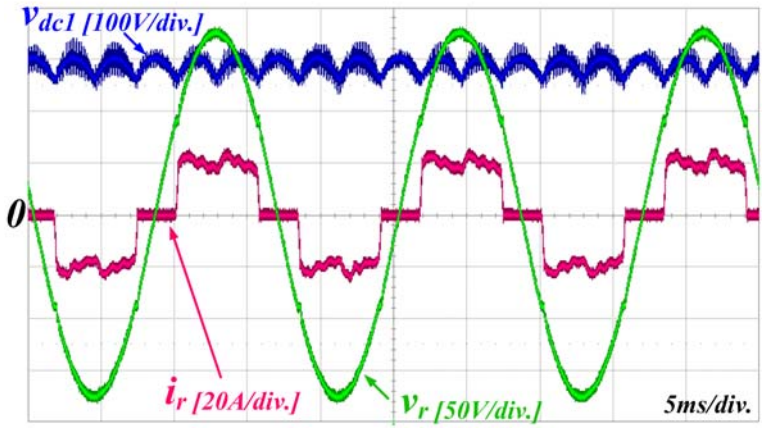


Fig. 3.31 Laboratory experimental set-up.



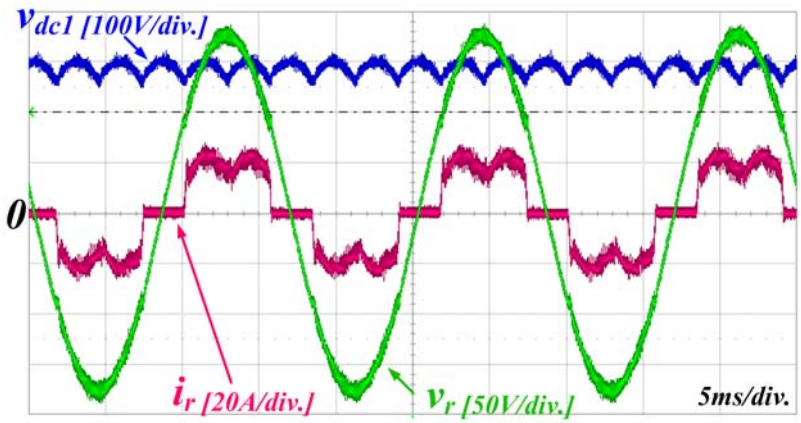
(a)



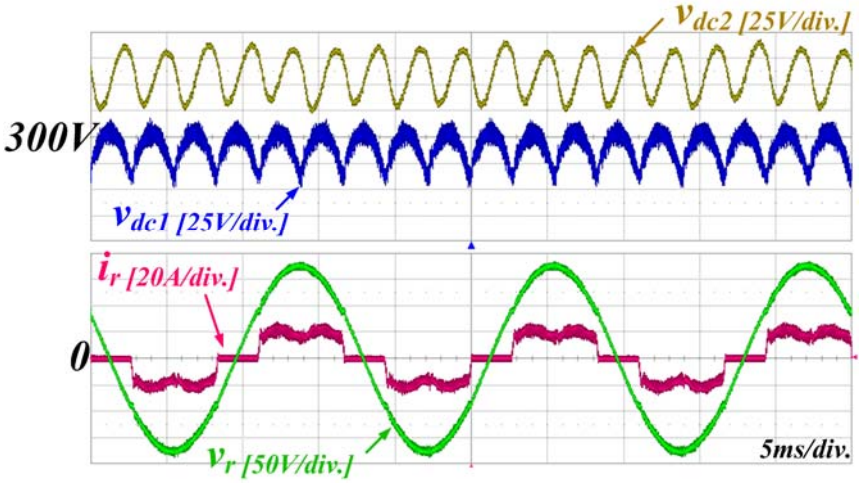
(b)

Fig. 3.32 Experimental results of (a) heavy passive components system and (b) small DC-link capacitor system with stabilization control.

3.33 illustrates the experimental results of proposed methods implemented in two ways. In the DSC system, v_{dc2} is sufficiently bounded in the desired range since C_{dc2} chosen as 47 μF considering available component is much higher than 38 μF mentioned in Section 3.3.3.



(a)



(b)

Fig. 3.33 Experimental results of proposed methods (a) implemented in the inverter and (b) implemented in DSC: v_{dc2}, v_{dc1}, v_r, and i_r @ $\alpha = 4$.

Moreover, it is verified that the shape of grid currents is able to be smoothly adjusted as expected in both cases. Since the operation of proposed method enhances system stability as explained in Section 3.1.1, both DC-link voltages

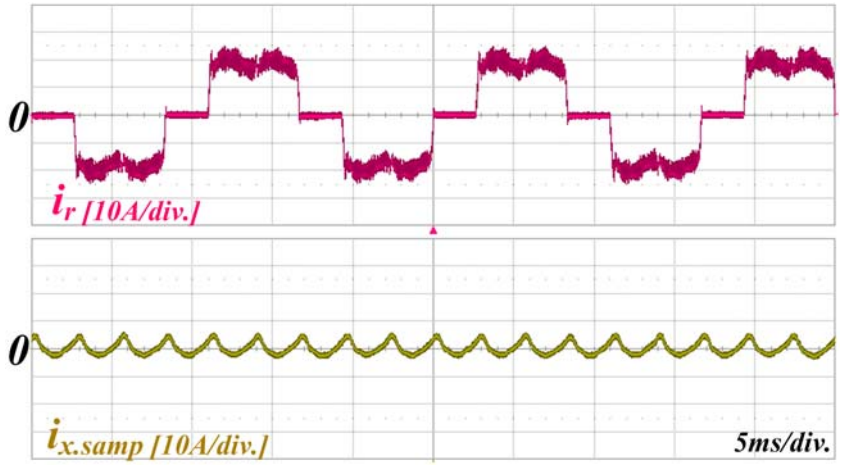


Fig. 3.34 Experimental results: i_r and $i_{x.samp}$ @ $\alpha = 4$.

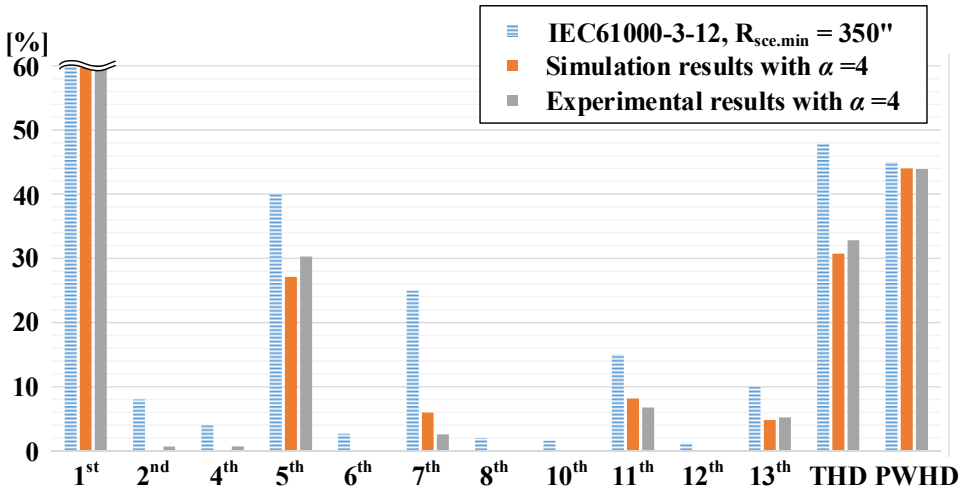


Fig. 3.35 Grid current harmonics with grid regulation.

exhibit clear line-to-line value of grid voltage without oscillation. In Fig. 3.34, the sampled inductor current $i_{x.samp}$ from DSC system and i_r are compared in the same division, 10 A/div..

Fig. 3.35 shows the grid current harmonics of proposed systems. As proved in Section 3.1.1, the PWHD becomes lower than the value of grid regulation, 45 %, where $\alpha = 4$. In the experimental results, the harmonics were measured as similar with simulation results, and it was verified that the system satisfies all grid regulations including PWHD.

By using power meter PM6000, the input and output powers were measured in a way of three-phase three-wiring configuration from both side of power conversion system as shown in Fig. 3.36. Therefore the motor losses are not included in these results. The measuring points were established by using the relationship of practical air compressor load: output power is proportional to square of motor speed. The

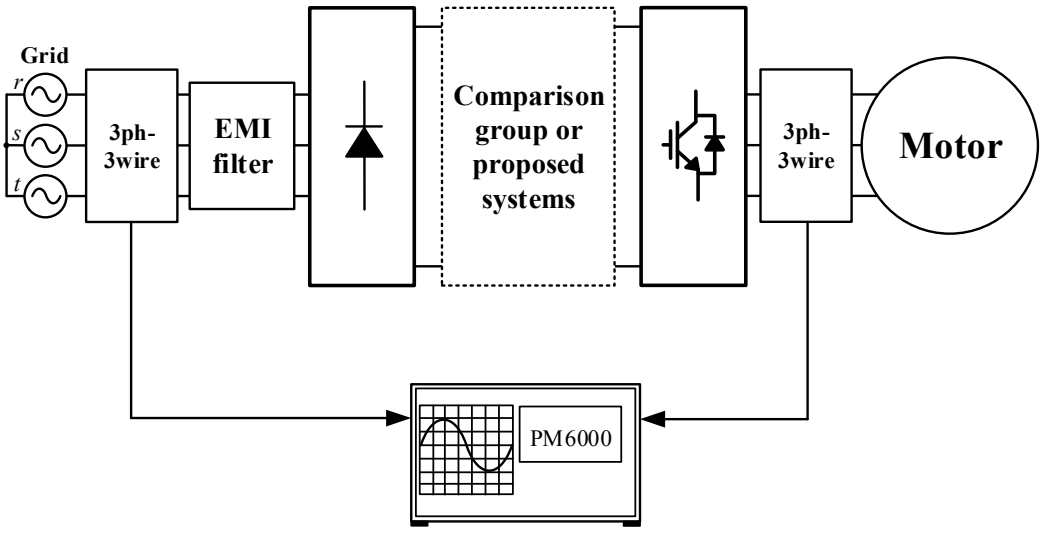


Fig. 3.36 Efficiency measuring configuration - power conversion circuit.

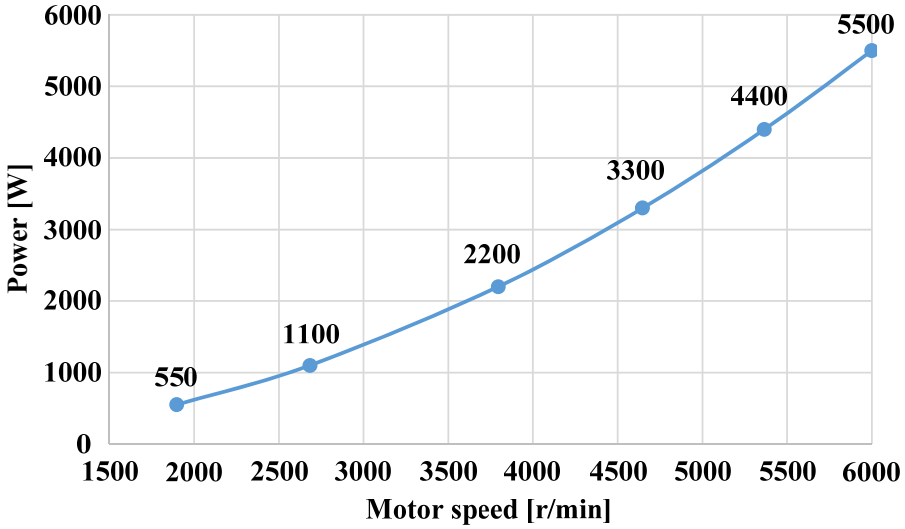


Fig. 3.37 Power measuring points in accordance with motor speed.

points are 100%, 80%, 60%, 40%, 20%, 10% of rated power as shown in Fig. 3.37.

The efficiencies of power conversion circuits are illustrated in Fig. 3.38. In this figure, small DC-link capacitor systems without auxiliary circuit (proposed method 1 and conventional system 2) show better efficiency at low power where the switching losses are dominant since the systems have relatively low average DC-link voltage. DSC system (proposed method 2) also has same DC-link voltage waveform, but its efficiency is slightly dropped since the losses from DSC are added. However, as the power is increased, since the conduction loss of L_{dc} becomes larger, the efficiency difference between DSC and other systems becomes smaller. The difference is less than 1.5% and even less than 0.2% at high power region.

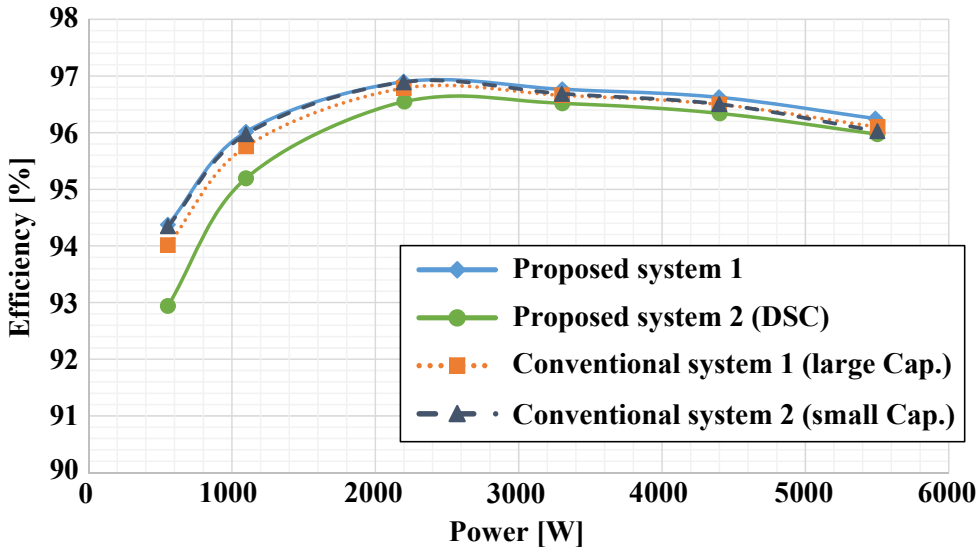


Fig. 3.38 Power conversion circuit efficiencies excluding motor losses.

In order to see the influence of motor losses, the input and output powers were measured from different nodes as shown in Fig. 3.39: one is three-phase grid input of power conversion system and another is three-phase generator output lines. Even though the losses of generator are also included in measuring losses, they are evenly included in all cases: thus it can be expected that the tendency of efficiency curves can be kept same.

Fig. 3.40 shows the efficiencies of four systems in a measuring way mentioned above. Where MI of motor drive circuit is under unity, in other word, before flux-weakening control area, three system has almost same motor losses, thus the efficiency depends on the losses of power conversion circuit. Owing to the

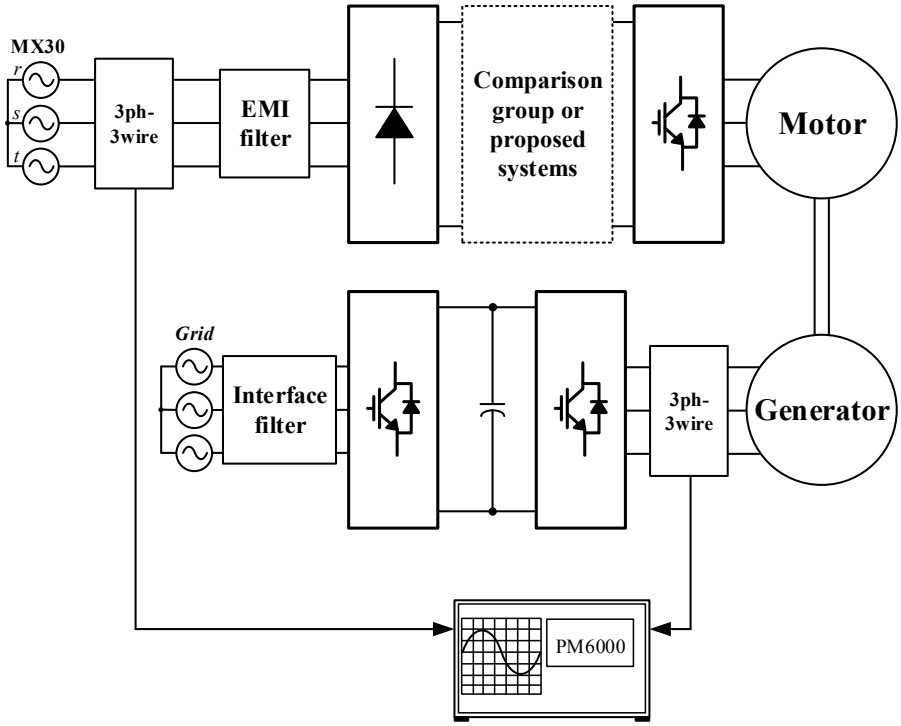


Fig. 3.39 Efficiency measuring configuration – To reveal a tendency of total motor drive system efficiency.

relatively low DC-link voltage of small DC-link capacitor systems (proposed methods 1, 2, and conventional system 2), however, they should carry out flux weakening control a little earlier (the power is around 2500W, i.e., motor speed is around 4000 r/min), and then the magnitude of d-axis current and corresponding losses should be also increased. Moreover, in cases of proposed method 1 and conventional system 2, the system should secure extra voltage margin for additional controls by increasing d-axis current more.

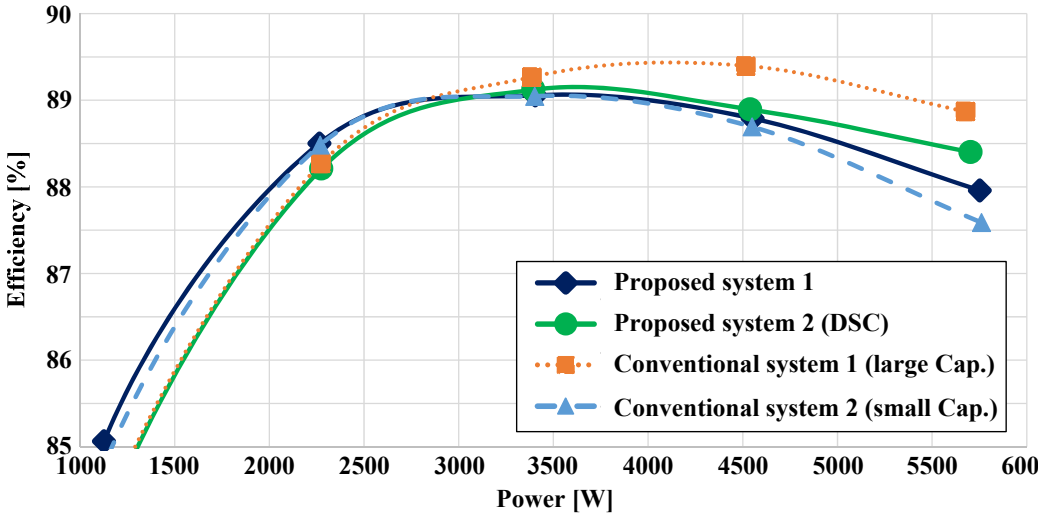


Fig. 3.40 Motor drive system efficiency tendencies including motor/generator losses.

In contrast, because DSC performs harmonic injection and system stabilization control in place of the inverter, the losses for securing additional voltage margin can be saved. This losses are dominant in this operating area, so the efficiency of DSC system is higher than that of conventional small DC-link capacitor system as shown in Fig. 3.40. Where output power is 5.5 kW, the efficiencies of four systems (proposed methods 1, 2, and conventional systems 1, 2) are 87.95%, 88.4%, 88.87%, and 87.59%, respectively.

3.5 Discussions

Through the experimental results, the validity of proposed methods has been

demonstrated. Since it is possible to implement the proposed control method in both inverter and DSC, This factor can be strategically utilized. Based on the concept of removing electrolytic capacitor from the system, the proposed method can provide extra strategies: cost-effective, torque-ripple-free, and efficiency improving strategies.

1) Cost-effective strategy

To realize this strategy, the DSC is removed and the inverter carries out all controls as shown in Fig. 3.11. In comparison with the conventional small DC-link capacitor system, the grid filter inductor can be additionally removed. In spite of that, the system can stably operate and satisfy grid harmonic regulation. However, the system has efficiency degradation at flux-weakening area like conventional small DC-link capacitor system, and suffers around 50% of torque ripple at rated power.

2) Torque-ripple-free strategy

In this strategy, the DSC is turning on in overall operating area. Since the DSC totally performs grid current shaping control, the inverter can work constant power motor driving control without other concerns. As shown in Fig. 3.40, this operation shows nice efficiency at flux-weakening area, but the efficiency is quite degraded

at low power area owing to the switching loss of DSC.

3) Efficiency improvement strategy

The merit of parallel connected circuit is that the circuit can be freely turning on and off as we want. This strategy utilizes this merit in terms of total system efficiency. Therefore, the DSC is turning on where the motor drive system is operated in flux-weakening area, and turning off at other operating areas. Then the efficiency curve will follow the higher value between two graphs of proposed methods 1 and 2.

In 2) and 3), even though DSC is added, the cost of total DSC system can be reduced in comparison with that of conventional heavy passive components system. The case study of implementation cost is presented in Appendix A.1.

4 Grid Current Shaping and DSC Operating Methods in Single-Phase Diode Rectifier System

Since the single-phase grid fundamentally provides huge ripple power, large DC-link capacitance has been used in order to absorb it. However, the single-phase diode rectifier system with large DC-link capacitance has to equip heavy gird filter inductor for meeting grid regulation; for example, 1-kW system having 1 mF of DC-link capacitance requires around 7.5 mH of grid filter inductance.

In the case of diode rectifier system with small DC-link capacitor, on the other hand, the grid current harmonics are greatly improved due to the absence of large DC-link capacitance, and the conventional researches have proven that the system is able to satisfy grid regulation such as IEC 61000-3-2 without heavy inductor [21]-[26]. However, since the system has no energy buffer to absorb grid ripple power, the motor necessarily absorbs the ripple power and suffers high torque ripple. This brings about reduction of operating area and system efficiency.

In this section, the conventional control method for single-phase small DC-link capacitor system is introduced and the DSC for covering the demerits of single-phase diode rectifier-fed motor drive system is proposed. The control method for single-phase DSC system is totally different from that for three-phase case owing

to the difference of DC-link voltage shape. Therefore this section presents the control method and operating strategy suited for single-phase system.

4.1 Conventional Single-Phase Small DC-Link Capacitor System

4.1.1 Control Method [26]

The diode rectifier-fed small DC-link capacitor system is shown in Fig. 4.1. The purpose of input inductor L_{in} is for filtering switching ripples by building low pass filter with DC-link capacitor C_{dc}. Since the purpose of L_{in} is different from conventional grid filter inductor L_f whose purpose is for attenuating relatively low order harmonics (under 2.4 kHz), the L_{in} can be designed as quite small value.

Unlike the case of three-phase grid-connected system, the single-phase system is possible to shape pure sinusoidal grid current owing to its structural advantage. In this case, the diode bridge is always conducted and the DC-link voltage v_{dc} becomes the absolute value of grid voltage v_g as expressed in

$$v_{dc} \approx \left| v_g \right| = \left| V_g \sin \theta_g \right|, \tag{4.1}$$

where V_g is a peak value of gird voltage, θ_g is a phase angle of the grid. Since the diode rectifier is conducted during most of the grid period, the shape of inverter output power P_{inv} determines the shape of grid current. Assuming that the grid current is sinusoidal, the grid power is given by

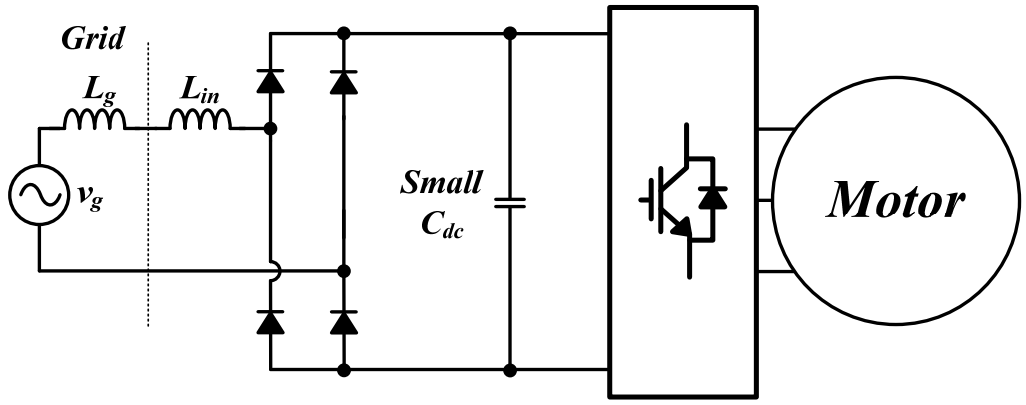


Fig. 4.1 Single-phase diode rectifier-fed small DC-link capacitor system.

$$P_g = v_g \cdot i_g = (V_g \sin\theta_g) \cdot (I_g \sin\theta_g) = V_g I_g \sin^2 \theta_g, \tag{4.2}$$

where I_g is a peak value of grid current. Next, the active power of DC-link capacitor can be calculated as

$$P_{dc} = v_{dc} i_{dc} = C_{dc} v_{dc} \frac{dv_{dc}}{dt} = 0.5\omega_g C_{dc} V_g^2 \sin(2\theta_g), \tag{4.3}$$

where ω_g is an grid angular speed. By using (4.2) and (4.3), the required inverter power P_{inv}^* to make grid current sinusoidal can be obtained as

$$P_{inv}^* = P_g - P_{dc}. \tag{4.4}$$

Since C_{dc} is quite small value, P_{inv}^* equals to P_g and shows the square of sinusoidal waveform. To trace this fluctuated waveform, it is good to use voltage reference direct modification method whose block diagram is shown in Fig. 4.2. From this figure, the output power of current controller $P_{inv.cc}$ is calculated as

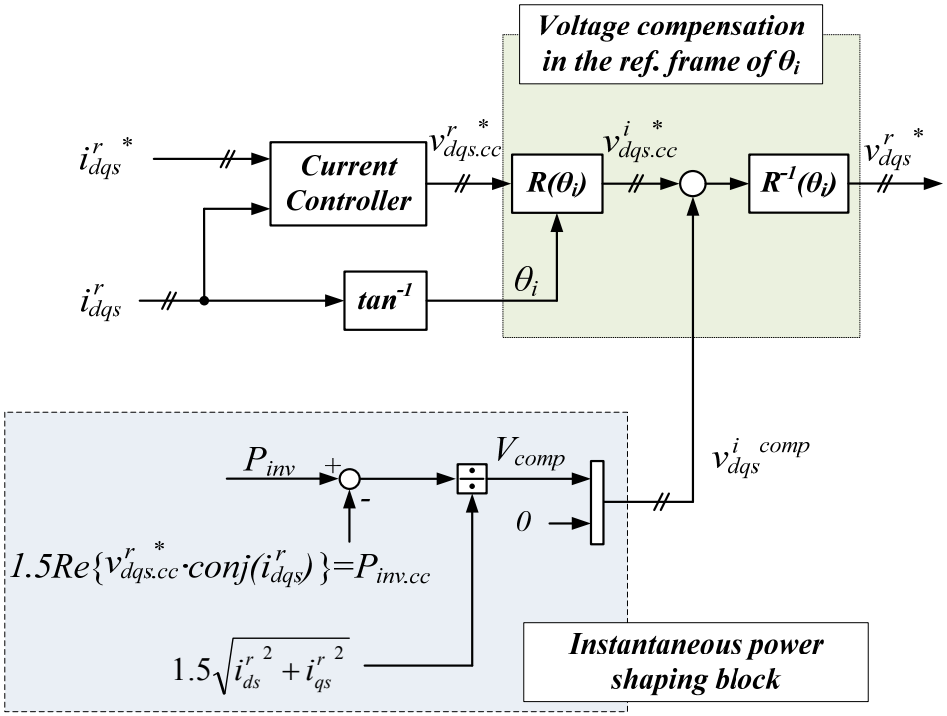


Fig. 4.2 Block diagram of conventional voltage reference modification method for single-phase system.

$$P_{inv.cc} = 1.5(v^{r}_{ds.cc}{}^{*} i^{r}_{ds} + v^{r}_{qs.cc}{}^{*} i^{r}_{qs}), \tag{4.5}$$

where i^{r}_{ds} and i^{r}_{qs} are dq-axis motor currents, and $v^{r}_{ds.cc}{}^{*}$ and $v^{r}_{qs.cc}{}^{*}$ are the dq-axis reference voltages from current controller. Here, the difference between $P_{inv}{}^{*}$ and $P_{inv.cc}$ is covered by instantaneous power shaping block. In this block, the magnitude of compensation voltage V_{comp} can be derived as

$$V_{comp} = \frac{P^{*}_{inv} - P_{inv.cc}}{1.5\left|i^{r}_{dqs}\right|} = \frac{P^{*}_{inv} - P_{inv.cc}}{1.5\sqrt{i^{r}_{ds}{}^{2} + i^{r}_{qs}{}^{2}}}. \tag{4.6}$$

Here, the method to deciding dq-axis compensation voltages $v^{i}_{dqs}{}^{comp}$ and adding them to $v^{i}_{dqs.cc}{}^{*}$ are same with the way in Section 3.2. Therefore, by using (3.18) and (3.19), the dq-axis output voltages $v^{r}_{dqs}{}^{*}$ can be represented as

$$\begin{bmatrix} v^{r}_{ds}{}^{*} \\ v^{r}_{qs}{}^{*} \end{bmatrix} = \begin{bmatrix} \cos\theta_i & -\sin\theta_i \\ \sin\theta_i & \cos\theta_i \end{bmatrix} \begin{bmatrix} v^{i}_{ds.cc}{}^{*} + V_{comp} \\ v^{i}_{qs.cc}{}^{*} \end{bmatrix} = \begin{bmatrix} v^{r}_{ds.cc}{}^{*} + V_{comp}\cos\theta_i \\ v^{r}_{qs.cc}{}^{*} + V_{comp}\sin\theta_i \end{bmatrix}. \quad (4.7)$$

Since this method is able to manipulate $v^{r}_{dqs}{}^{*}$ much faster than the current controller, it is suitable for handling the fluctuated power in (4.4).

4.1.2 Limitation of Single-Phase Small DC-Link Capacitor System

By using the above control method, the small DC-link capacitor system with single-phase grid can successfully satisfy grid regulation without heavy passive components. However, the system inherently has a problem in system efficiency degradation. This degradation is caused by its insufficient v_{dc} expressed in (4.1). The v_{dc} drops to zero and it periodically becomes lower than the back EMF of motor. During this duration, the motor drive system should perform flux-weakening control to secure the available DC-link voltage. Then excessive flux-weakening current (d-axis current) increases the condition loss of motor. Besides, since the system should handle the ripple power in (4.4), peak values of current and torque are unavoidably increased.

4.2 Single-Phase System with DSC

To solve the above problems, the DSC and its control method are proposed for the single-phase grid-connected system. The DSC supports both grid current shaping and motor driving controls. By adopting the DSC, the small DC-link capacitor system can feature improved torque ripple and even constant value in accordance with system condition, and this also leads to reduction of motor current peak. Furthermore, since DSC is able to boost the DC-link voltage during T_{GD}, the motor drive circuit can secure DC-link voltage margin. These DSC's actions cover the demerits of small DC-link capacitor system.

4.2.1 System Configuration

The total motor drive system including DSC is shown in Fig. 4.3. Like in the case of DSC in three-phase system, the structure can be implemented to various topologies such as boost and buck converters which can transfer the power from main DC-link capacitor C_{dc1} to energy buffer capacitor C_{dc2}. Here, the amount of their storable energies are one of the key consideration because it decides the capacitance of C_{dc2}. The formal can store the energy where a floating capacitor voltage (voltage across C_{dc2}) v_{dc2} is lower than a main DC-link voltage (voltage across C_{dc1}) v_{dc1} and the latter can transfer the energy where v_{dc2} is higher than v_{dc1}.

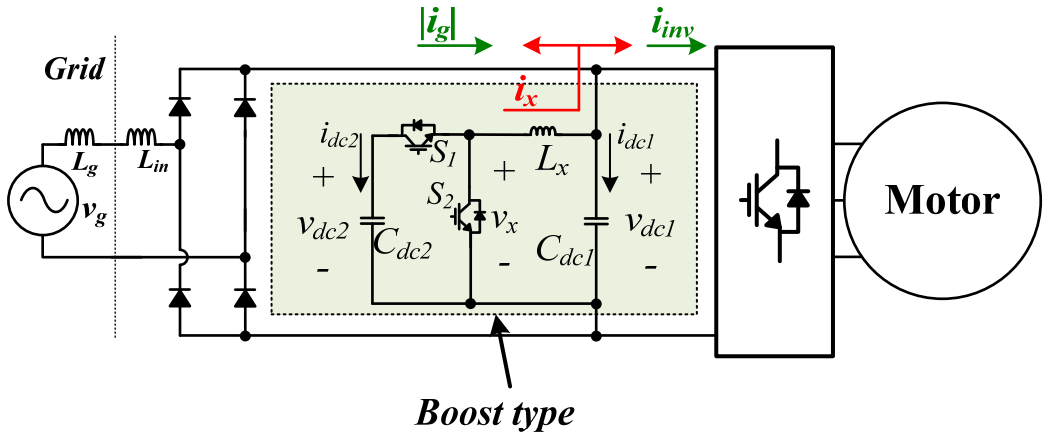


Fig. 4.3 The configuration of single-phase DSC system.

In the single-phase small DC-link capacitor system, as aforementioned, C_{dc1} is basically designed as quite small value and the v_{dc1} is similar to the waveform of (4.1). Therefore, v_{dc1} can be decreased to very low value even zero, and this condition is very tough to a buck converter. Of course, v_{dc1} would not be dropped up to zero owing to v_{dc1} boosting control of DSC, but it is clear that the boost converter is more suitable than the buck converter as DSC for single-phase system.

The storable energy of C_{dc2} can be calculated as

$$E = \frac{1}{2} C_{dc2} (V_{dc2.\max}^2 - V_{dc2.\min}^2), \tag{4.8}$$

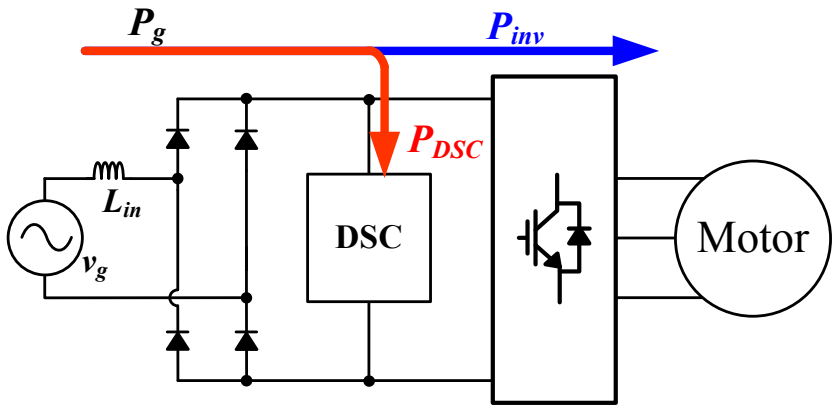
where $V_{dc2.max}$ and $V_{dc2.min}$ are maximum and minimum allowable voltage, respectively. $V_{dc2.max}$ is usually decided by voltage rating of electric components such as switches S_1, S_2, and capacitor C_{dc2} in Fig. 4.3. For example, if the system is

connected to 220-V grid, switching devices of 600-V voltage rating are commonly used. In this condition, $V_{dc2.max}$ can be decided as 400 V (2/3 of voltage rating), considering margin for voltage overshoot during turn-off. And $V_{dc2.min}$ have only to be larger than v_{dc1} in order to guarantee modulation index of DSC.

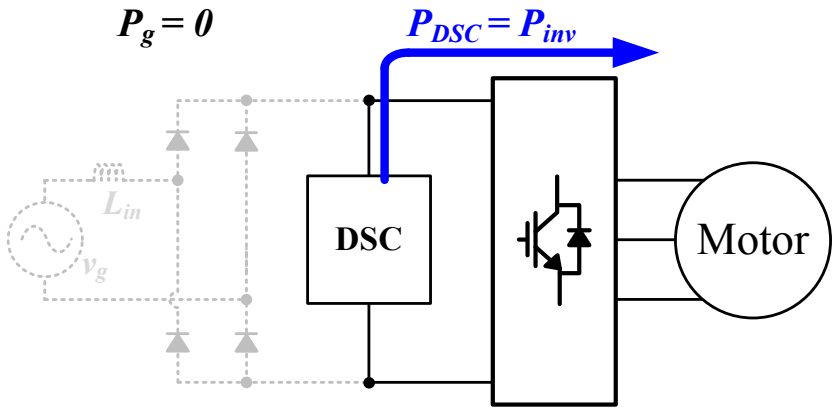
The boost converter which shares the ground with main system also have many merits in low-cost system implementations such as gate power supply with bootstrap circuit, voltage sensing without photocoupler or isolation sensor, and inductor current sensing by using shunt resistor. In summary, it is desirable for adopting the boost converter as DSC, considering substantive circuit design and the operating conditions of proposed control method.

4.2.2 Operating Concept

The key point of proposed operation method is that the DSC performs grid current shaping during grid connection time T_{GC} (Fig. 4.4(a)) and supports the motor drive during grid disconnection time T_{GD} (Fig. 4.4(b)). Here, the energy in C_{dc2} is charged and discharged at T_{GC} and T_{GD}, respectively. In the T_{GC}, v_{dc1} is regulated to the voltage similar with (4.1), and DSC adjusts compensation current in order to control grid current into desired value. On the other hand, the T_{GD} is started when DSC boosts the DC-link voltage into minimum DC-link voltage $V_{dc1.min}$. In this time, the grid current becomes zero and DSC supplies required load



(a)



(b)

Fig. 4.4 Power flow during (a) T_{GC} ($v_g > V_{dc1.min}$) and (b) T_{GD} ($v_g \leq V_{dc1.min}$).

power to the inverter. Therefore, the resultant DC-link voltage reference v_{dc1}^* can be described as

$$v_{dc1}^* = \begin{cases} \left| V_g \sin\theta_g \right| & @T_{GC} \\ V_{dc1.\min} & @T_{GD} \end{cases} \tag{4.9}$$

and the expected absolute value of grid current $|i_g^*|$ is

$$\left|i_g^*\right| = \begin{cases} I_m\left(\left|\sin\theta_g\right| - \dfrac{V_{dc1.\min}}{V_g}\right) & @\,T_{GC} \\ 0 & @\,T_{GD} \end{cases}, \tag{4.10}$$

where I_m is magnitude of grid current which can be calculated from the energy equation expressed as

$$\int_o^{T_g} v_g i_g^* dt = \int_o^{T_g} P_{inv} dt\,, \tag{4.11}$$

where T_g is grid period. Assuming that P_{inv} is constant, I_m is derived as

$$I_m = \frac{P_{inv} T_g}{\left(\begin{array}{l} V_g(T_2 - T_1) - \dfrac{V_g}{2\omega_g}\left\{\sin(2\omega_g T_2) - \sin(2\omega_g T_1)\right\} \\ + \dfrac{2V_{dc1.\min}}{\omega_g}\left\{\cos(\omega_g T_2) - \cos(\omega_g T_1)\right\} \end{array} \right)}, \tag{4.12}$$

where

$$T_2 = \frac{1}{\omega_g}\sin^{-1}\left(\frac{V_{dc1.\min}}{V_g}\right) = \frac{T_{GD}}{2} \quad \text{and} \quad T_1 = \frac{T_g}{2} - T_2\,. \tag{4.13}$$

In this operation, it is important that even though the grid current becomes zero during T_{GD}, it is able to satisfy the grid regulation in accordance with $V_{dc1.min}$. If the $V_{dc1.min}$ is decreased, the grid current becomes similar to sinusoid but the motor drive performances are degraded in terms of available output power and flux weakening control. Therefore it is important to find appropriate $V_{dc1.min}$ to secure load output performances on condition that the grid current satisfies grid regulation.

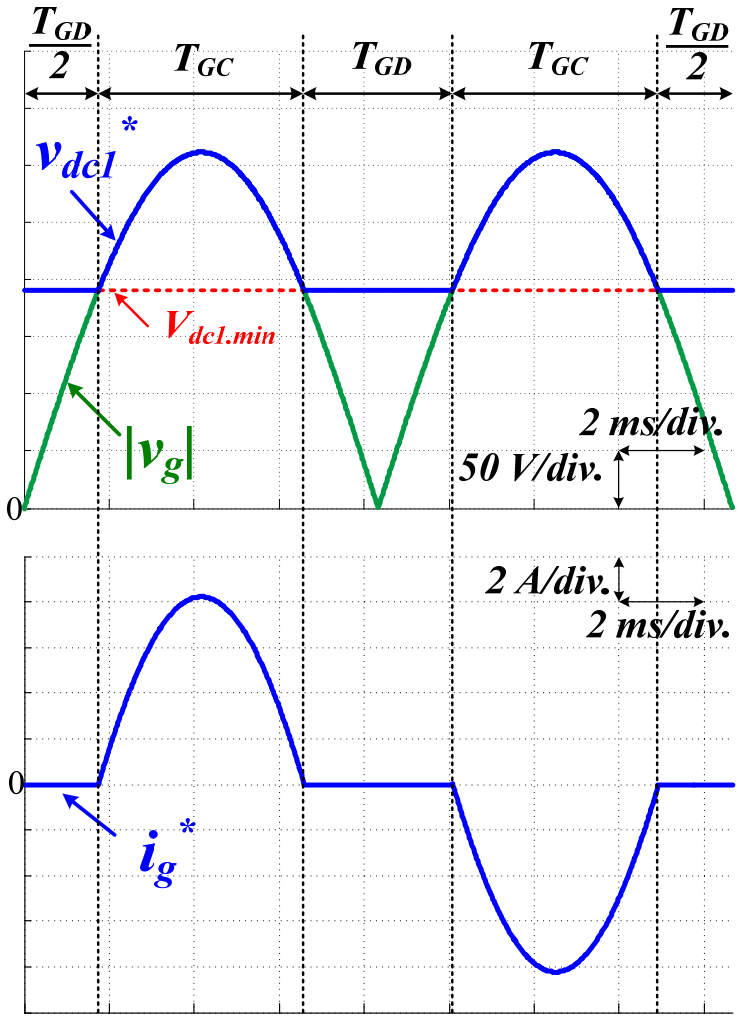


Fig. 4.5 The waveforms of v_{dc1}^* and i_g^* according to the durations, T_{GC} and T_{GD}.

The waveforms of (4.9) and (4.10) are shown in Fig. 4.5. As aforementioned, even though the grid current waveform is not sinusoidal, it is enough to satisfy the grid regulation; it depends on the length of T_{GD}, i.e., the level of $V_{dc1.min}$. Lower $V_{dc1.min}$ provides better grid current harmonics and reduces the value of C_{dc2}, but it

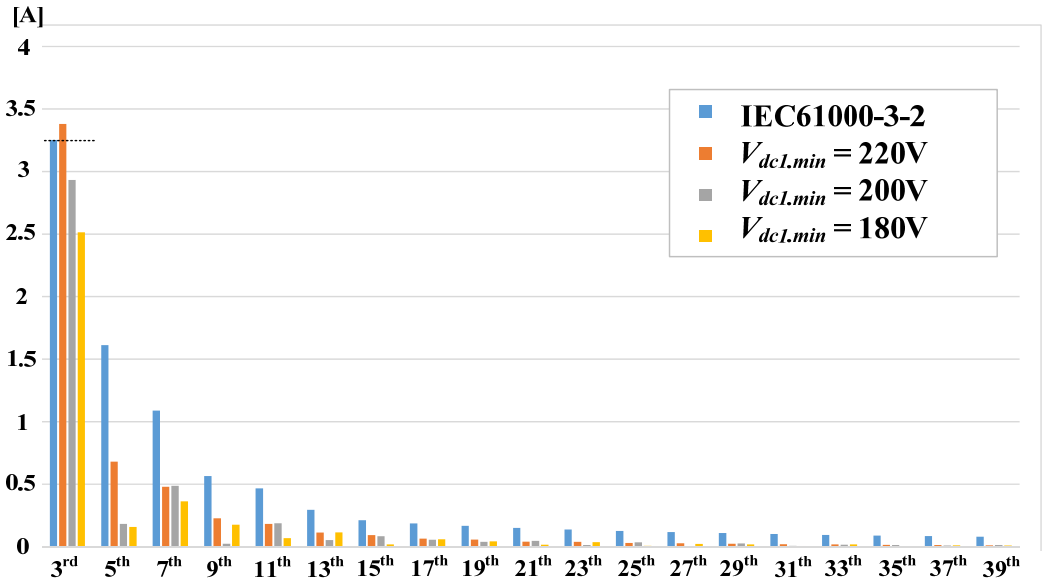


Fig. 4.6 Grid current harmonics with various $V_{dc1.min}$ and limits of grid regulation, IEC 61000-3-2 Class A.

decreases available v_{dc1} which decides maximum motor drive region. Fig. 4.6 illustrates the grid current harmonic variations and limits of grid regulation, IEC 61000-3-2 Class A where $P_{inv.avg}$ = 800 W and $V_{dc1.min}$ is varied from 180 V to 220 V. The even harmonics are not marked since they are rarely existed in all conditions. As shown in this figure, the harmonics are enough to satisfy the regulation except the condition where $V_{dc1.min}$ = 200~210 V. Considering the available v_{dc1} for the load, it is recommended that $V_{dc1.min}$ is chosen as high as possible, in other words, up to around 190 V.

4.2.3 Partial Power Assistance Operating Strategy

From the proposed operating concept, defining that the output powers during T_{GC} and T_{GD} are $P_{inv.GC}$ and $P_{inv.GD}$ respectively, the DSC entirely supplies $P_{inv.GD}$ during T_{GD}. It means that the capacity of DSC is dominantly decided by $P_{inv.GD}$. If the system requires constant output power $P_{con.out}$ at all times, it is necessary to design DSC for absorbing the energy of $P_{con.out} \cdot T_{GD}$. However, if the load environment is generous to ripple power or torque, this factor can be strategically utilized to improve the feasibility of single-phase DSC system.

As shown in Fig. 4.5, v_{dc1} of DSC system is not constant value. It means that the available v_{dc1} is varied in accordance with the durations, T_{GC} and T_{GD}. If the power difference between two durations is acceptable, it is advantageous that $P_{inv.GC}$ is higher than $P_{inv.GD}$ in terms of utilization of available v_{dc1}. Moreover, under the condition that the inverter average power $P_{inv.avg}$ is maintained, DSC is able to be miniaturized since $P_{inv.GD}$ becomes lower than $P_{inv.avg}$.

Defining that the assistance factor γ_{AF} is

$$\gamma_{AF} = \frac{P_{inv.GD}}{P_{inv.avg}}, \tag{4.14}$$

the inverter power reference P_{inv}^{*} can be represented as

$$P_{inv}^{*} = \begin{cases} P_{inv.GC} = P_{pk}\left(\sin^2\theta_g - \left(V_{dc1.\min}/V_g\right)^2\right) + \gamma_{AF}P_{inv.avg} & @T_{GC} \\ P_{inv.GD} = \gamma_{AF}P_{inv.avg} & @T_{GD} \end{cases}, \tag{4.15}$$

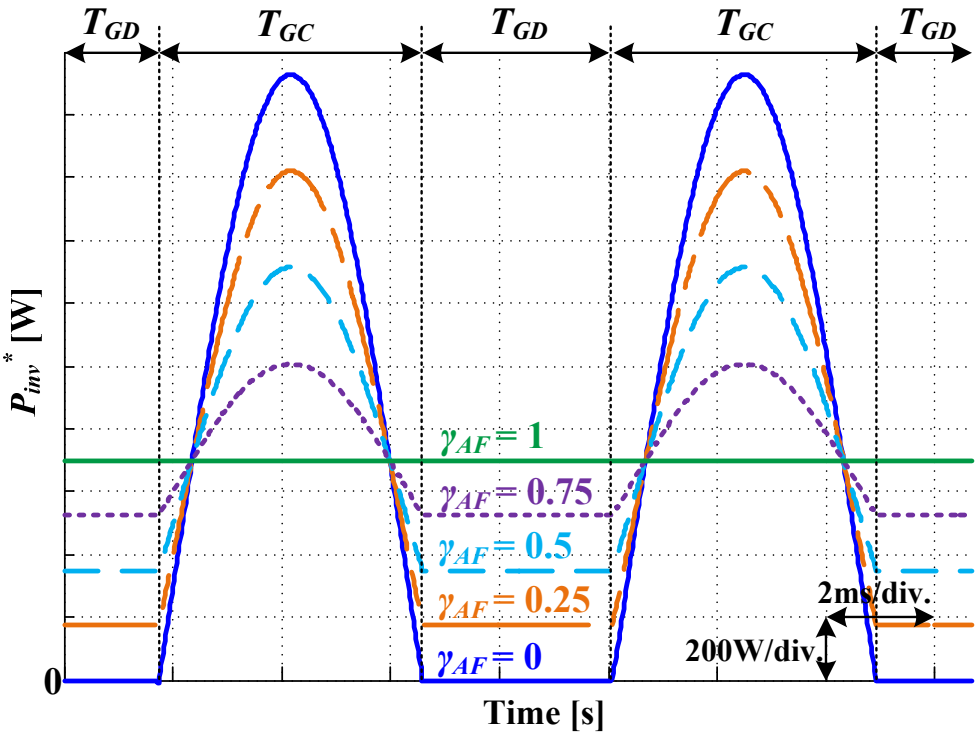


Fig. 4.7 Inverter power reference in accordance with various γ_{AF}.

where P_{pk} is

$$P_{pk} = \frac{0.5T_g P_{inv.avg}(1 - 0.25T_g T_1 \gamma_{AF} - 0.5T_g (T_2 - T_1)\gamma_{AF})}{(T_2 - T_1)(0.5 - \sin^2 \theta_g) - \frac{1}{4\omega_g}\left(\sin(2\omega_g T_2) - \sin(2\omega_g T_1)\right)}. \quad (4.16)$$

The shapes of $P_{inv.GC}$ is designed as similar waveform of grid power in order to ease a burden of the DSC. The resultant waveform of (4.15) is shown in Fig. 4.7, where $V_{dc1.min}$ is set to 190 V. As γ_{AF} is decreasing, the $P_{inv.GD}$, which is same as DSC power P_{DSC}, is proportionally reduced, whereas the peak of $P_{inv.GC}$ is necessarily increased.

On the contrary, $P_{inv.GD}$ becomes larger as γ_{AF} is increased, and finally P_{inv}^* becomes constant where $\gamma_{AF} = 1$.

If we are focused on the miniaturization of DSC, γ_{AF} might be chosen as small as possible. However if we think the improvement of total system efficiency, the value of γ_{AF} can be strategically utilized depending on the motor operating conditions. The motor operating conditions can be classified to two cases:

$$\sqrt{\left(v_{ds}^{r\,*}\right)^2 + \left(v_{qs}^{r\,*}\right)^2}\Bigg|_{i_{ds}^r = i_{ds.MTPA}^{r*}} < \frac{V_{dc1.\min}}{\sqrt{3}}, \tag{4.17}$$

$$\sqrt{\left(v_{ds}^{r\,*}\right)^2 + \left(v_{qs}^{r\,*}\right)^2}\Bigg|_{i_{ds}^r = i_{ds.MTPA}^{r*}} \geq \frac{V_{dc1.\min}}{\sqrt{3}}, \tag{4.18}$$

where $v^r_{ds}{}^*$ and $v^r_{qs}{}^*$ note the dq- axis reference voltages of the inverter, i^r_{ds} is d-axis motor current, $i^r_{ds.MTPA}{}^*$ is d-axis reference current for maximum-torque-per-ampere (MTPA), and $V_{dc1.min}/\sqrt{3}$ means maximum available DC-link voltage during T_{GD}. In the case of (4.17), the motor drive system do not conduct flux-weakening control, so the operation of $\gamma_{AF} < 1$ may unnecessarily increase motor copper losses which occupy huge part of total system losses. In the case of (4.18), on the other hand, the inverter carries out the flux-weakening control in order to secure MI during every T_{GD}, so the motor drive has to inject d-axis (flux-axis) motor current considering the level of $V_{dc1.min}$. If γ_{AF} is lower than unity, however, the required $v^r_{dqs}{}^*$ are

reduced during T_{GD}, and then the system can secure MI with relatively low d-axis motor current. As a result, it contributes to the reduction of total motor copper loss in comparison with the operation of γ_{AF} =1. Furthermore, the DSC loss is also decreased due to the low $P_{inv.GD}$.

This operating strategy also have positive influence on the design of DSC. One example of system design sequence is as follows:

1) Select $V_{dc1.min}$ in order to meet grid regulation at rated power operation.
2) Find motor drive operating point which satisfies the condition of (4.17).
3) Calculate required $P_{inv.GD}$ at this operating point.
4) Design DSC in consideration of the $P_{inv.GD}$.

If we design DSC by this procedure, the DSC has enough capability to perform γ_{AF} =1 operation in the operating area of (4.17). Since it is obvious that the calculated power in 3) is smaller than the system rated power, this DSC is miniaturized in comparison with full-power handling DSC. Here, in the condition of (4.18) where the DSC system is working on γ_{AF} <1 operation, it should be keep in mind that maximum P_{DSC} has not to be exceed the calculated power in 3).

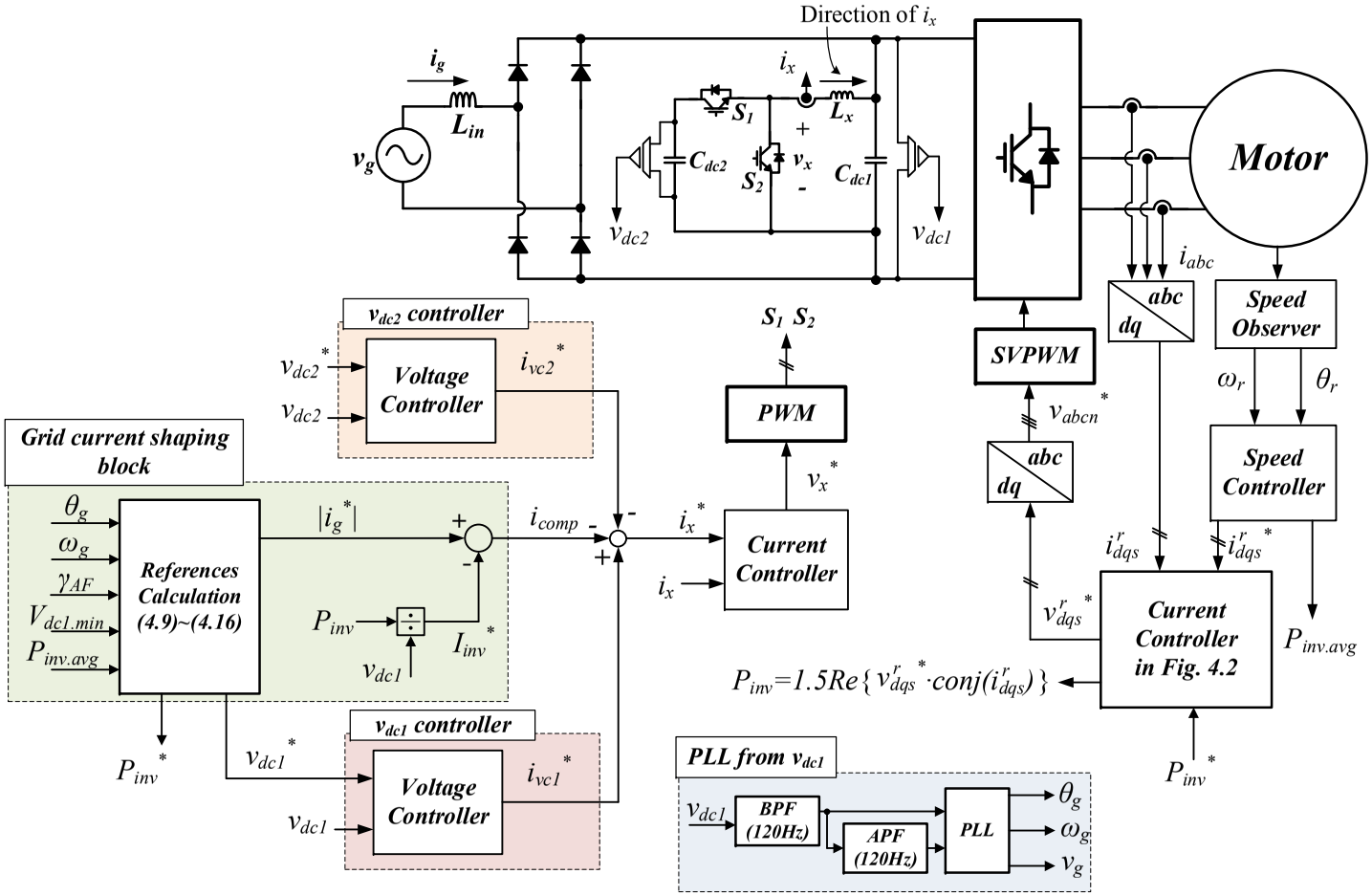


Fig. 4.8 Block diagram of the proposed method for single-phase DSC system.

4.2.4 Control Method

The control block diagram for the proposed method is shown in Fig. 4.8. The proposed control blocks are divided into five parts: phase locked loop (PLL), v_{dc2} voltage controller, v_{dc1} voltage controller, grid current shaping block, and current controller. For the grid angle detection method in PLL, any isolated voltage sensor is not required since θ_g can be detected from v_{dc1} which is equal to v_g during T_{GC}. Fig. 4.9 shows the specific block diagram of PLL. The 120Hz harmonic of v_{dc1} is extracted by band pass filter (BPF) of 120Hz with narrow bandwidth, and it is expressed in virtual orthogonal frame by using all pass filter (APF). From this virtual orthogonal frame, the angle of 120Hz is estimated and the absolute magnitude of sinusoidal wave with grid angle $|sin\theta_g|$ can be obtained. This kind of

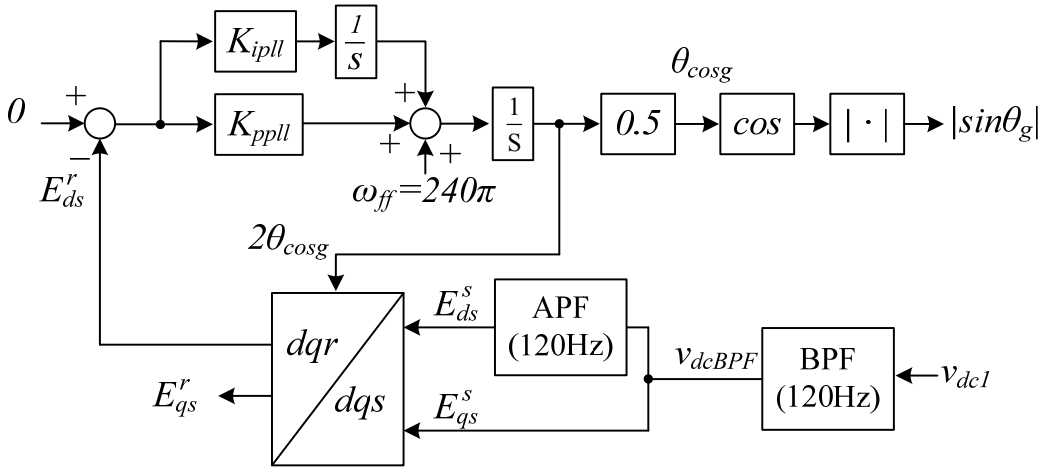


Fig. 4.9 Specific control block diagram of PLL.

single-phase PLL using DC-link voltage has been widely used in small DC-link capacitor system, and this block can be also replaced to SOGI PLL [24][68]-[70].

By using the angle information from the PLL block, other references related with grid side can be established in the grid current shaping block. From (4.10) and the inverter current reference i_{inv}^* which is given by

$$i_{inv}^* = \frac{P_{inv}}{v_{dc1}} = \frac{1.5(v_{ds}^{r\,*} i_{ds}^r + v_{qs}^{r\,*} i_{qs}^r)}{v_{dc1}}, \tag{4.19}$$

the compensation current i_{comp} can be calculated as

$$i_{comp} = \left|i_g^*\right| - i_{inv}^*. \tag{4.20}$$

This i_{comp} adjusts the ripple power between the grid and the inverter in order to shape i_g as i_g^* whatever the shape of i_{inv}^* is.

In addition to this i_{comp}, there are extra two currents that need to be controlled; they are the outputs of two voltage controllers, i_{vc1}^* and i_{vc2}^*. The former is for controlling v_{dc1} to $V_{dc1.min}$ and the latter is for regulating the average level of v_{dc2} to its reference voltage v_{dc2}^*. Ironically, however, these two currents want to control the input and output voltages of the DSC, i.e., boost converter. It obviously causes a conflict since they try to move opposite direction in order to achieve their own goals. Therefore, to avoid this conflict, two voltage controller need to be activated alternately. Since the v_{dc1} controller must be activated during T_{GD}, the v_{dc2} controller

is working during the rest of the time, i.e., T_{GC}. It means that the average value of v_{dc2} is temporarily uncontrolled during T_{GD}. This results in extra v_{dc2} ripples but it does not matter because v_{dc2} is originally supposed to be fluctuated by i_{comp}. Just considering this fact, it is good to give margin when we design C_{dc2}. In the v_{dc1} control, on the other hand, since the grid is strongly tied to DC-link during T_{GC}, temporary stop of the v_{dc1} controller is not a problem. As a result, the control loops during two times, T_{GC} and T_{GD}, can be illustrated as Fig. 4.10(a) and Fig. 4.10(b), respectively.

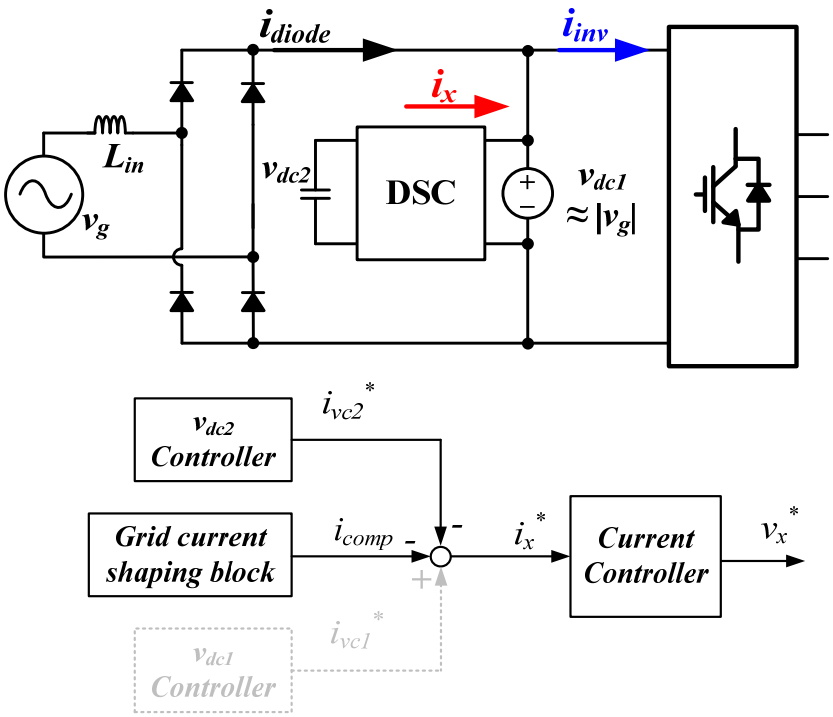


Fig. 4.10(a) Circuit diagram and control loop blocks during T_{GC}.

The specific control block diagram of two voltage controllers is same as the voltage controller of three-phase DSC system shown in Fig. 3.21. In the case of v_{dc1} controller, however, there is no need to use the notch filter which was employed for filtering ripple components from floating capacitor voltage, and it is recommended that the bandwidth ω_{vc1} is set as high as possible since the response time of v_{dc1} controller determines the starting points of T_{GD}. Thus the gains of v_{dc1} controller, $k_{p.vc1}$, $k_{i.vc1}$, and $k_{a.vc1}$, are

$$k_{p.vc1} = 2C_{dc1}\zeta_{vc1}\omega_{vc1}, \quad k_{i.vc1} = C_{dc1}\omega_{vc1}^2, \text{ and } \quad k_{a.vc1} = 1/k_{p.vc1}. \tag{4.21}$$

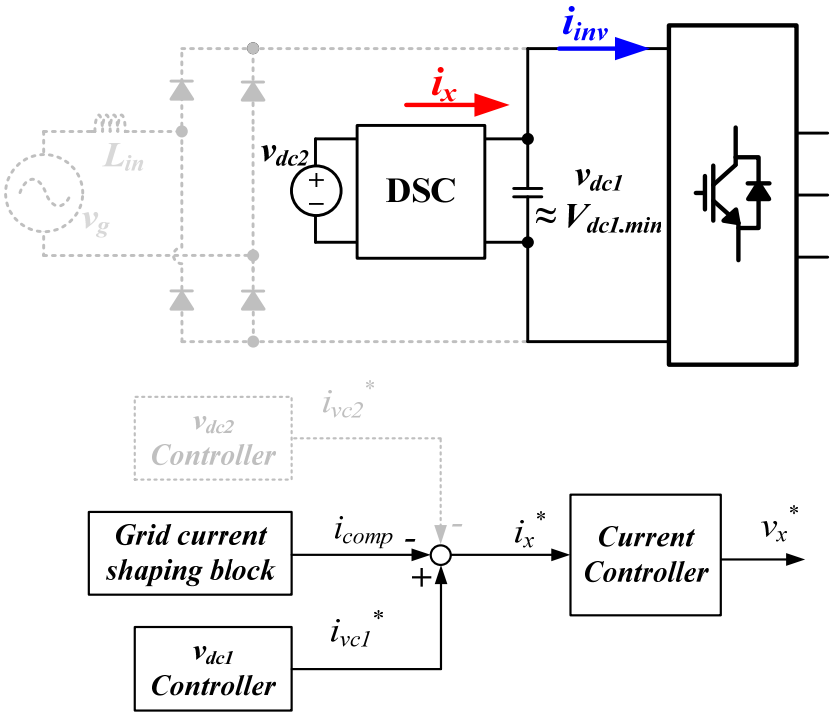


Fig. 4.10(b) Circuit diagram and control loop blocks during T_{GD}.

Where ω_{vc1} is 200π rad/s, the Bode plot of v_{dc1} controller is shown in Fig. 4.11. The relevant transfer function is in (3.30) where the gains are replaced to (4.21). Here as elsewhere, if the damping ratio ζ_{vc1} is too low, the overshoot occurs near ω_{vc1}. Thus it is good to choose the value more than 3. The gains of v_{dc2} controller can be set in same way with the bandwidth ω_{vc2} and damping ratio ζ_{vc2}. In this case, the notch filter is used, and the bandwidth ω_{NF} and damping ratio ζ_{NF} are 240π rad/s and 0.707, respectively.

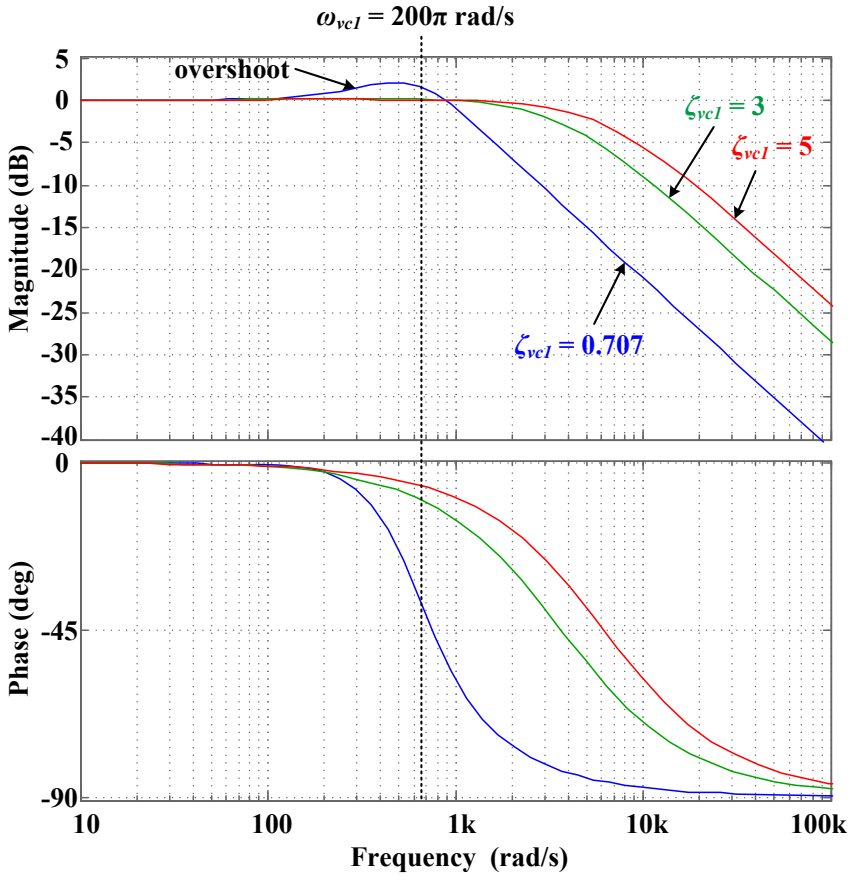


Fig. 4.11 Bode plot of v_{dc1} controller in accordance with various ζ_{vc1}.

Finally, the current controller regulates the DSC's inductor current i_x as the reference i_x^* given by

$$i_x^* = -(i_{comp} + i_{vc2}^* - i_{vc1}^*). \tag{4.22}$$

Assuming that the i_{vc2}^* are negligible, i_x^* becomes $-i_{comp}$, and then i_g is shaped as in Fig. 4.5. The design of current controller is totally same as in the case of three-phase DSC system.

4.2.5 System Design Guideline

In the proposed system, we have two capacitors: C_{dc1}, C_{dc2}. The capacitance of C_{dc1} is involved in switching ripple current absorbing and instantaneous power control of DSC. From (4.22), it is verified that i_x^* will be increased if i_{vc1}^* proportional to C_{dc1} is increased. This means that DSC should supply more current to the main system in order to control grid current. Therefore, it is recommended that C_{dc1} is set to value of several micro farad. This paper selects C_{dc1} as 5 μF, where the system is connected to 220-V grid and the switching frequency is 20 kHz.

C_{dc2}, which is main energy storage of DSC, is designed so that v_{dc2} is limited from $V_{dc2.min}$ to $V_{dc2.max}$. As mentioned in Section 4.2.1, $V_{dc2.min}$ and $V_{dc2.max}$ are 310 V (peak of v_{dc1}) and 400 V, respectively. At first, assuming that i_x is accurately controlled by (4.22), the output power of DSC, P_{DSC}, is

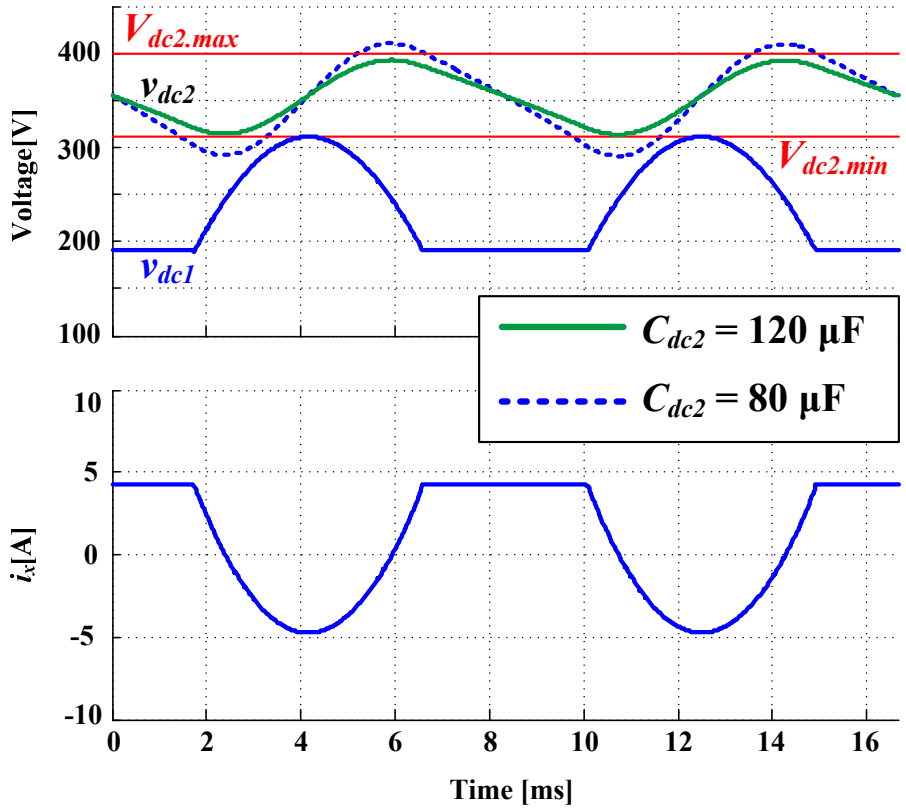


Fig. 4.12 v_{dc2} in accordance with various $C_{dc2.}$

$$P_{DSC} = v_x i_x = R_x i_x^2 + L_x i_x \frac{di_x}{dt} + v_{dc1} i_x \approx v_{dc1} i_x , \tag{4.23}$$

where L_x is interface inductor and R_x is equivalent series resistor of L_x, By substituting (4.9), (4.10) and (4.22) into (4.23), P_{DSC} can be written as

$$P_{DSC} = \begin{cases} V_g I_m \sin^2 \theta_g - V_{dc1.\min} I_m \sin \theta_g - P_{inv.GC} & @\, T_{GC} \\ - P_{inv.GD} & @\, T_{GD} \end{cases} . \tag{4.24}$$

Here, using the fact that P_{DSC} is transferred to C_{dc2}, v_{dc2} can be represented as

$$v_{dc2} = \sqrt{\left(v_{dc2}^{*}\right)^2 - \frac{2}{C_{dc2}} \int P_{DSC}\, d\tau} \ . \tag{4.25}$$

Fig. 4.12 shows key waveforms of DSC system where v_{dc2}^{*} is 355 V and $P_{inv.max}$ is 800 W. In the case of v_{dc2}, since v_{dc2} exceeds the boundary line on the condition that C_{dc2} is lower than around 120 μF, DSC is operated in over-modulation area and it might be damaged due to the over-voltage problem. In this condition, therefore, it is recommended that C_{dc2} is set as at least 120 μF considering $V_{dc2.min}$ = 310 V.

4.3 Simulation and Experimental Results

The simulations is conducted with the motor drive system and the system conditions and parameters are shown in Table 4.1. The interior permanent magnet synchronous motor (IPMSM) is used and the motor rated speed is 3600 r/min. In this condition, the C_{dc2} can be set as at least 120 μF if we consider γ_{AF} =1 operation at overall operating area.

Fig. 4.13 shows the simulation results where the motor speed is operated at rated speed. $V_{dc1.min}$ is set to 190V and it is verified that the grid current is enough to satisfy the grid regulations as we expected. It exhibits up to 0.95 power factor. v_{dc2}^{*} is adjusted to 355 V and v_{dc2} is well bounded between $V_{dc2.min}$ (310 V) and $V_{dc2.max}$ (400 V).

Table 4.1 System conditions and parameters

Condition	Value
Grid voltage	220 V
Grid angular frequency, ω_g	377 rad/s
Rated speed, $\omega_{rpm.rated}$	3600 r/min
Rated power, $P_{inv.max}$	800 W
Main DC-link capacitor, C_{dc1}	5 μF
DSC interface inductor, L_x	2 mH
Grid input filter inductor, L_{in}	300 μH
Inverter switching frequency, $f_{sw.inv}$	10 kHz
DSC switching frequency, $f_{sw.DSC}$	20 kHz
Motor parameter	
d-axis inductance, L_d	8.7 mH
q-axis inductance, L_q	12.75 mH
Phase resistance, R_s	1.07 Ω
Flux linkage, λ_{pm}	0.0947 V/(rad/s)
Pole, P	6

Fig. 4.14 shows the motor current and load torque waveforms of two systems: DSC system and conventional small DC-link capacitor system in [26]. On the condition that the $V_{dc1.max}$ is 190V, the peak motor current is 5.7 A since d-axis current of motor side is significantly reduced. In contrast, the peak current of

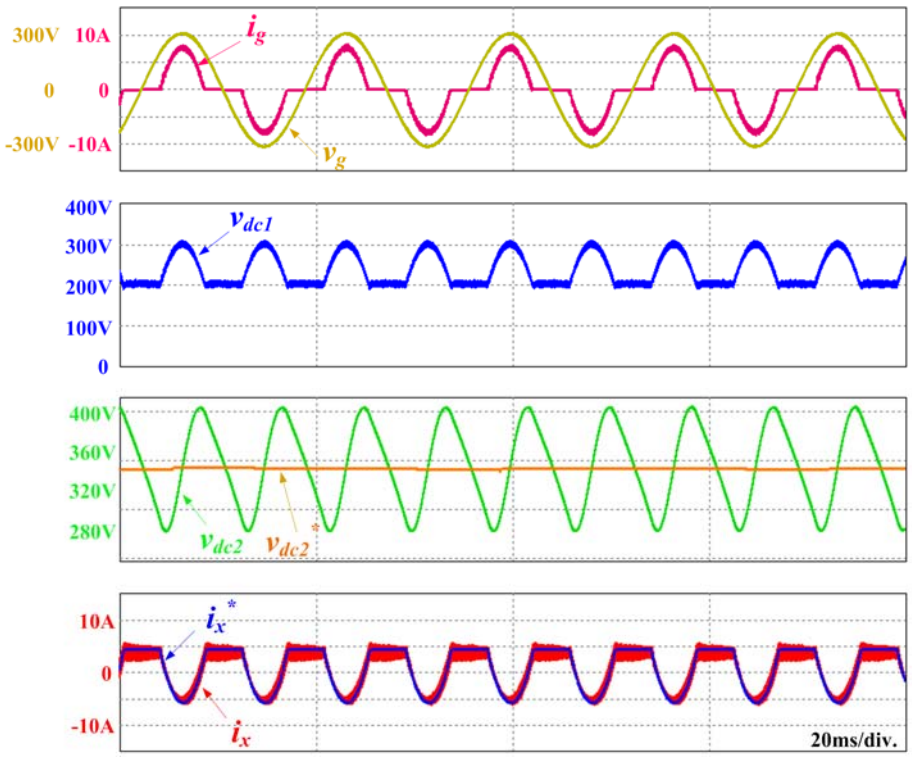


Fig. 4.13 Simulation results of motor drive system with DSC

where $P_{inv.avg}$ = 800 W and $V_{dc1.min}$ = 190 V.

conventional small DC-link capacitor system shows 11 A. Furthermore, the waveform of load torque shows almost constant value, whereas conventional system has significantly fluctuated load torque which has almost 6 N·m variation with 2.1 N·m average value. Although additional current i_x flows to DSC, the system is able to exhibit outstanding performances such as the high quality torque, reduced motor current peak.

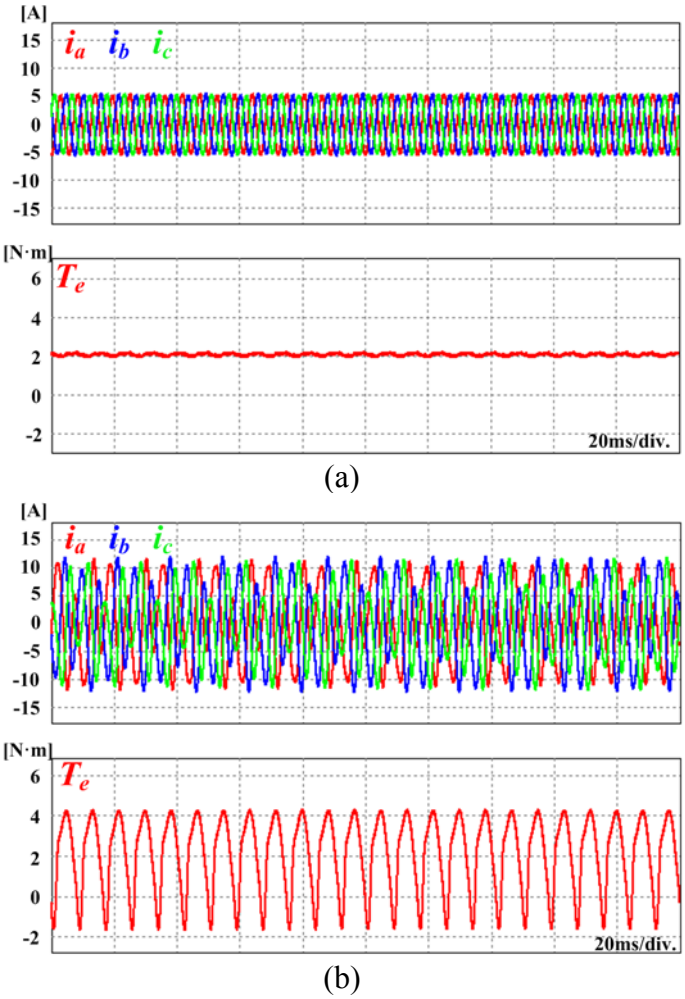


Fig. 4.14 Simulation results: motor currents and load torque from (a) the DSC system, and (b) the conventional small DC-link capacitor system.

In the experiments, the MG set was employed and the diode rectifier with dynamic breaker was used for operating generator as shown in Fig. 4.15. The inverter and DSC were operated by their own digital signal processors (DSPs), TMS320C28346 and TMS320F28335, respectively. C_{dc2} has value of 141 μF (47

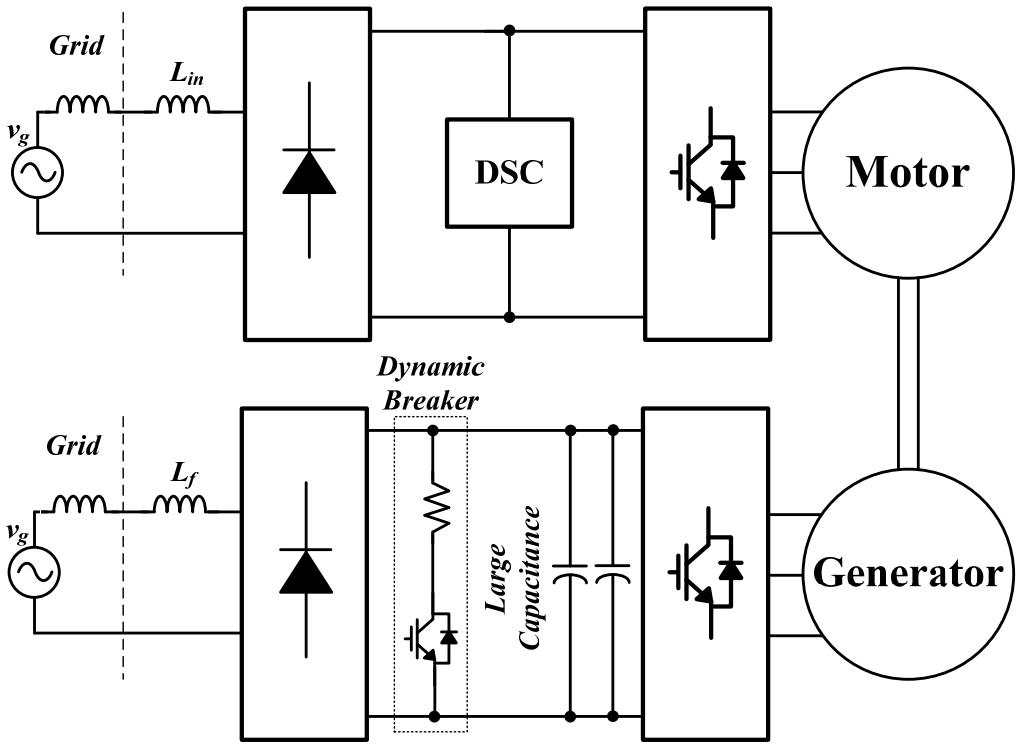


Fig. 4.15 Laboratory experimental set-up for single-phase system.

μF x 3) for the experiment test.

Fig. 4.16 shows the experimental waveform where the DSC system starts up. As shown in this figure, i_g has significant harmonics when the DSC is not applied. However, after the DSC is working, the shape of i_g is highly improved. Also in the case of v_{dc2}, it can be verified that the average value is well controlled as v_{dc2}^* as we desired.

Figs. 4.17 and 4.18 exhibit the experimental waveforms where the $P_{inv.avg}$ is 450 W and 800 W, respectively. In Fig. 4.17, since the grid current harmonic and the

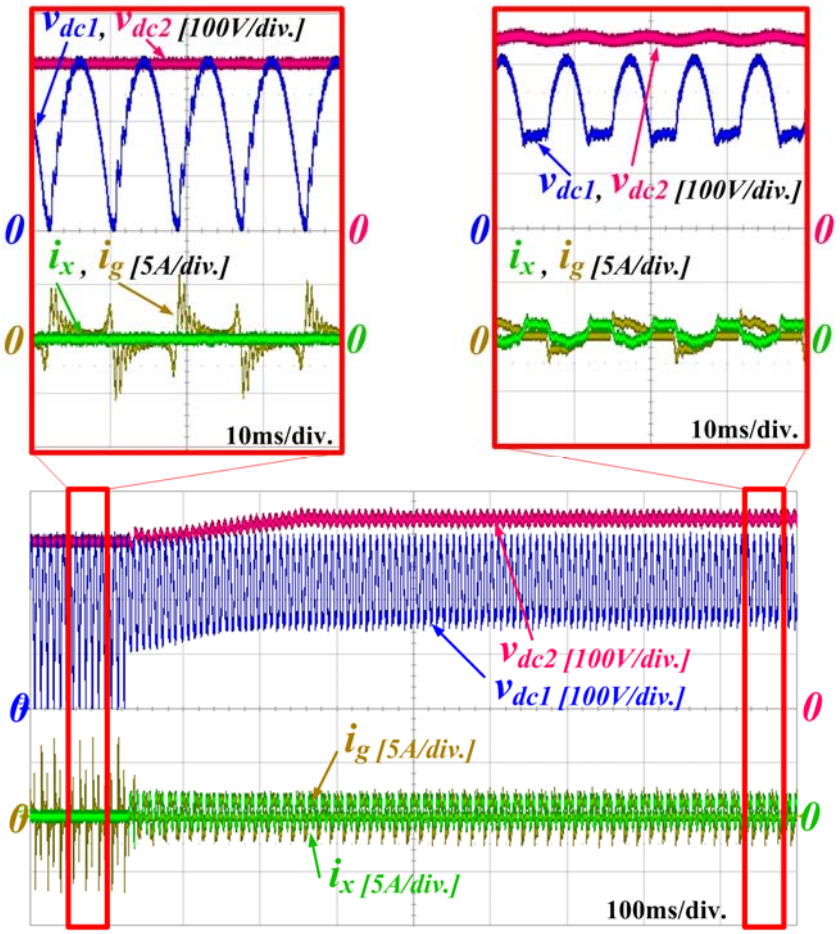


Fig. 4.16 Experimental results: start-up waveforms.

inverter MI have an enough margin, $V_{dc1.min}$ can be set to lower value in order to reduce system switching losses. Here, $V_{dc1.min}$ is set as 150 V. In Fig. 4.18, the motor speed is 3600 r/min and $V_{dc1.min}$ has value of 190 V. In this condition, the inverter is operated in (4.18) and performs flux-weakening control. The v_{dc2} is well bounded into the desired range, $V_{dc2.min}$ (311 V) to $V_{dc2.max}$ (400 V).

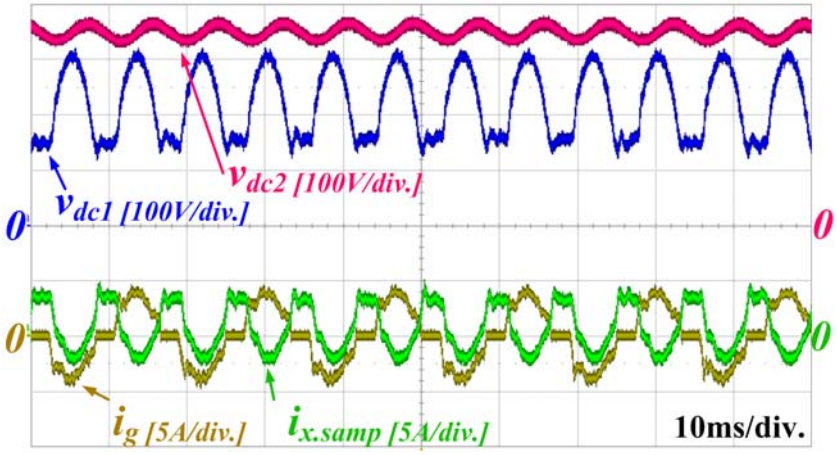


Fig. 4.17 Experimental results: $P_{inv.avg}$ = 450 W (0.5 p.u.), $V_{dc1.min}$ = 150 V.

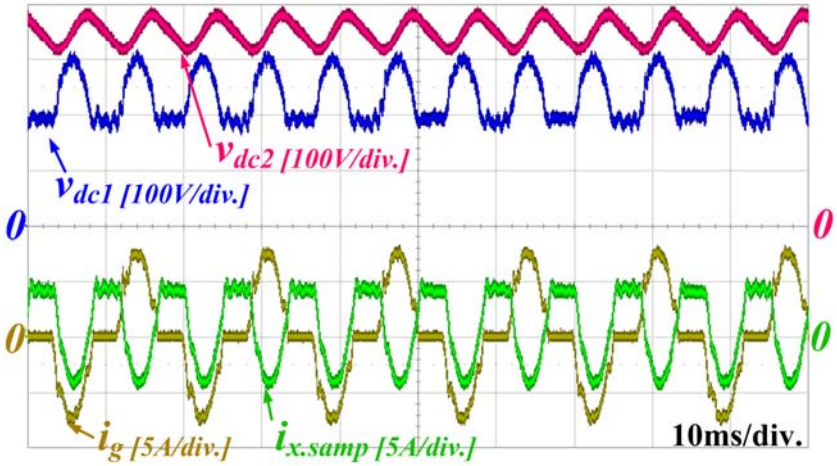


Fig. 4.18 Experimental results: $P_{inv.avg}$ = 800 W (1 p.u.), $V_{dc1.min}$ = 190 V.

In fact, from the simulation results shown in Fig. 4.6, $V_{dc1.min}$ can be theoretically set as higher value considering gird harmonic margin. As $V_{dc1.}$min is increased, the 3rd harmonic of grid current firstly reaches to corresponding regulation value.

However in the experimental results as shown in Fig. 4.19, higher order harmonics such as 13^{th}, 15^{th}, and 17^{th}, were quickly increased and they reached to their harmonic regulation values first. As a results, where $V_{dc1.min}$ is 190 V, the system barely satisfies the grid regulation IEC 61000-3-2. There are several reasons. First, in this experimental set-up, the DSPs for the inverter and DSC are not communicated each other. Owing to this, the DSC could not completely compensate the exact harmonics from the inverter. Second, i_x is not perfectly regulated by current controller owing to its bandwidth and phase delay. Moreover the ignored i_{vc2}^* also has a bad influence on the harmonics. These things degrade the quality of harmonic compensation. Lastly, the undesirable harmonics caused by practical implementations such as parasitic impedances and dead time of DSC contaminate the grid current.

In order to measure the system efficiency, the input power is measured by power meter PM6000, and the output power is obtained from the speed controller of the load machine-driven inverter. The measuring points are 3600, 2880, 2160, 1440, and 720 r/min where the relevant calculated powers are 800, 600, 450, 300, and 110 W, respectively. Under the condition that the average output power is same in both two cases, grid voltage and current are measured.

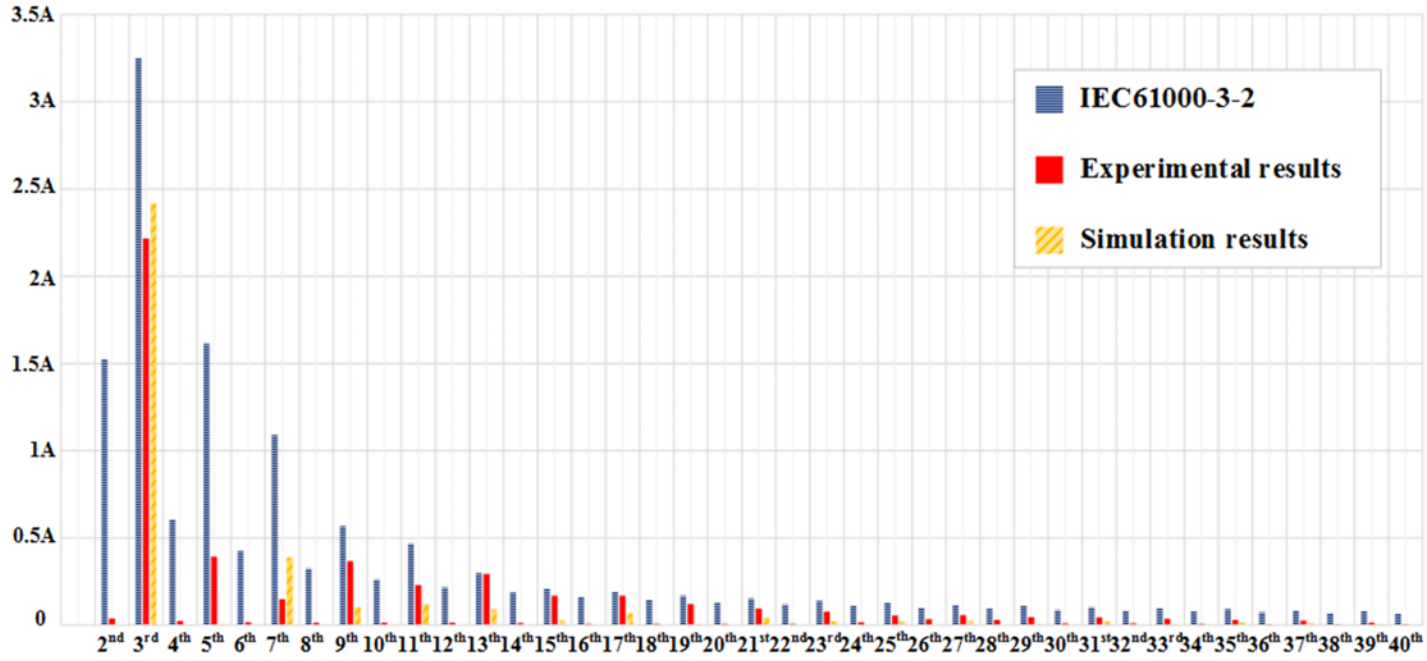


Fig. 4.19 Experimental results: Grid current harmonic and grid regulation, IEC61000-3-2

where $P_{inv.avg}$ = 800 W and $V_{dc1.min}$ = 190 V.

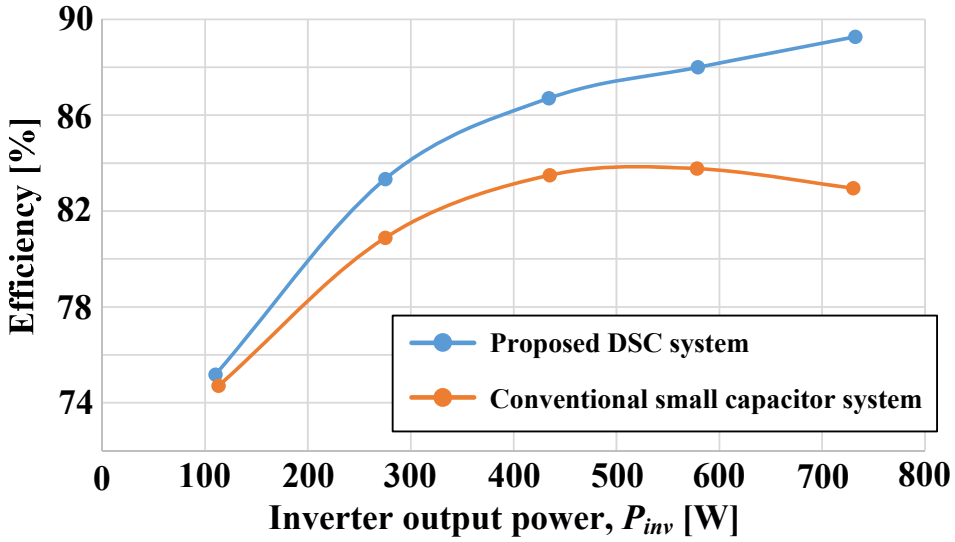


Fig. 4.20 System efficiencies: DSC and small DC-link capacitor system.

In Fig. 4.20, the efficiencies of the DSC system and conventional small DC-link capacitor system are plotted. The DSC system shows overall high efficiency in comparison with conventional small DC-link capacitor system. The difference is relatively small at low power region since the average flux-weakening current is small owing to the relatively low back EMF. However, the conventional system, which has the DC-link voltage of (4.1), still need small amount of flux-weakening current, whereas the proposed DSC system which has the DC-link voltage of (4.9) does not need flux-weakening control in this operating point. The DSC system can even offer the constant output torque if the system conducts γ_{AF} =1 operation. In high power region, on the other hand, the DSC system shows remarkable efficiency

thanks to the extended DC-link voltage.

In this experiment conditions, the area of (4.18) starts where $P_{inv.avg}$ = 600 W, ω_{rms} = 2880 r/min. According to the design guideline in Section 4.2.3, the γ_{AF} is set to 0.75 ($P_{inv.GD}/P_{inv.max}$ = 600/800 = 0.75) and the C_{dc2} can be reduced to 90 μF. The C_{dc2} is obviously proportional to γ_{AF} by the equation given by

$$C_{dc2} = \frac{2P_{DSC}T_{GD}}{V_{dc2.\max}^2 - V_{dc2.\min}^2} = \frac{2\gamma_{AF}P_{inv.avg}T_{GD}}{V_{dc2.\max}^2 - V_{dc2.\min}^2}. \quad (4.26)$$

The simulated system efficiency including γ_{AF} = 0.75 operation is shown in Fig. 4.21 where IGCM15F60GA (Infineon) and STGPL6NC60D (STMicroelectronics) are used for the inverter and DSC, respectively. The simulation is conducted by PLECS simulator and the specific parameters are referred to in their datasheet. The calculated losses include inverter losses (switching and conduction losses), DSC losses (ESR or L_x, switching and conduction losses), and motor conduction loss. In comparison with the experimental results, the efficiency tendency is similar with the experimental one, but the values show some difference at high power region where the portion of motor core loss which is not included in simulation results is increased. As shown in this figure, the efficiency curves of two cases, γ_{AF} = 1 and 0.75, look like almost same where $P_{inv.avg} \leq$ 600 W, whereas they show difference of 1 % where $P_{inv.avg}$ = 800 W (91.24% and 92.22% at γ_{AF} = 1 and 0.75, respectively). This is because the rms value of motor current is reduced at γ_{AF} = 0.75 as explained

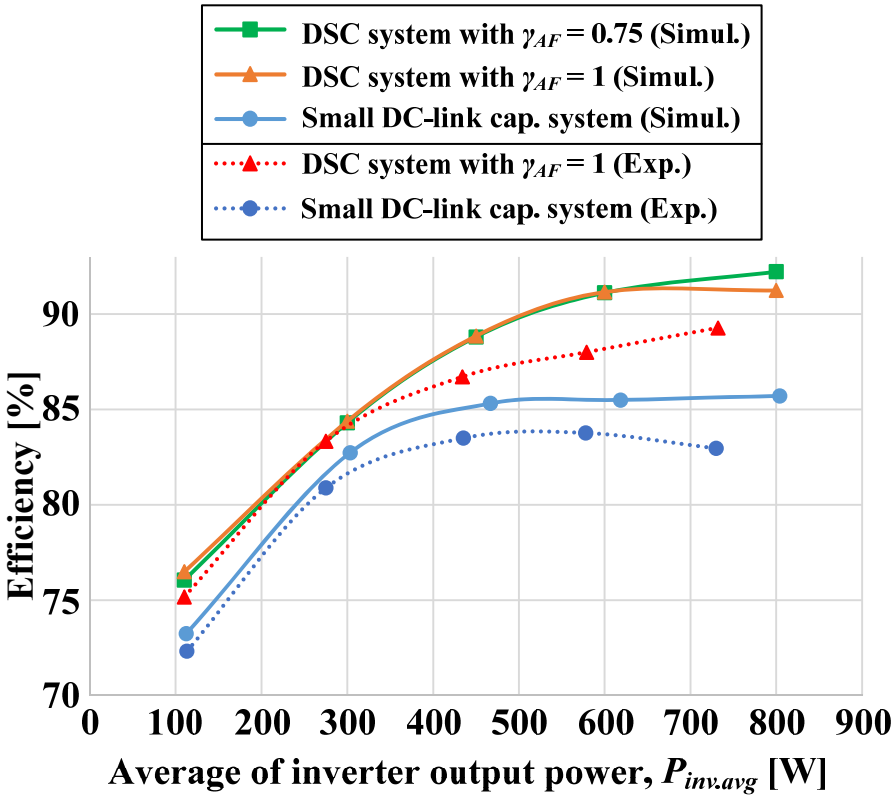


Fig. 4.21 Simulated system efficiencies: DSC with γ_{AF} = 1 and 0.75, and small DC-link capacitor system.

in Section 4.2.3. With the reduction of motor current rms, the losses of DSC is also decreased due to the reduced P_{DSC}, thus the total system loss is obviously reduced. Fig. 4.22 shows the estimated power losses in the DSC system at $P_{inv.avg}$ = 800 W, where $P_{inv.SW}$, $P_{inv.CON}$, $P_{DSC.SW}$, $P_{DSC.CON}$, $P_{DSC.Lx}$, and $P_{M.CON}$ represent inverter switching loss, inverter conduction loss, DSC switching loss, DSC conduction loss, ESR of L_x conduction loss, and motor conduction loss, respectively.

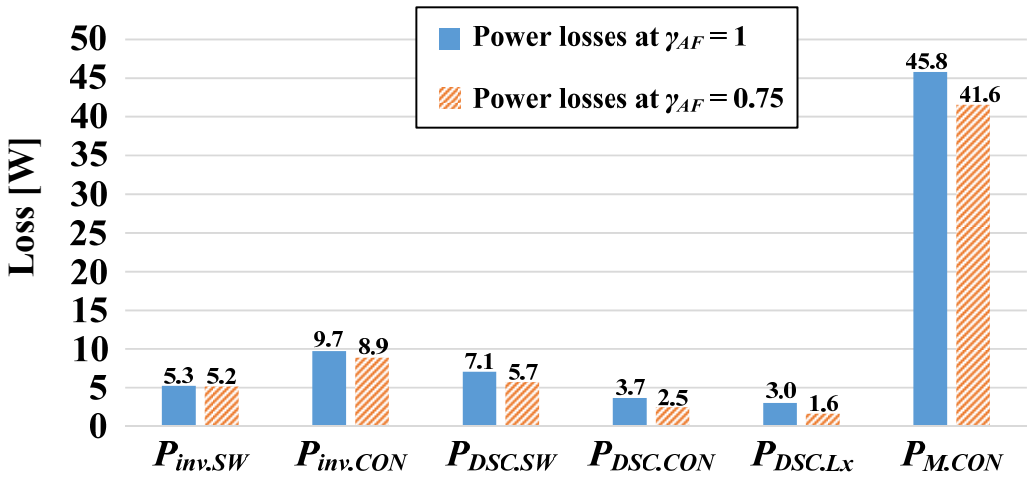


Fig. 4.22 Estimated power losses in DSC system at 0.8 kW operation.

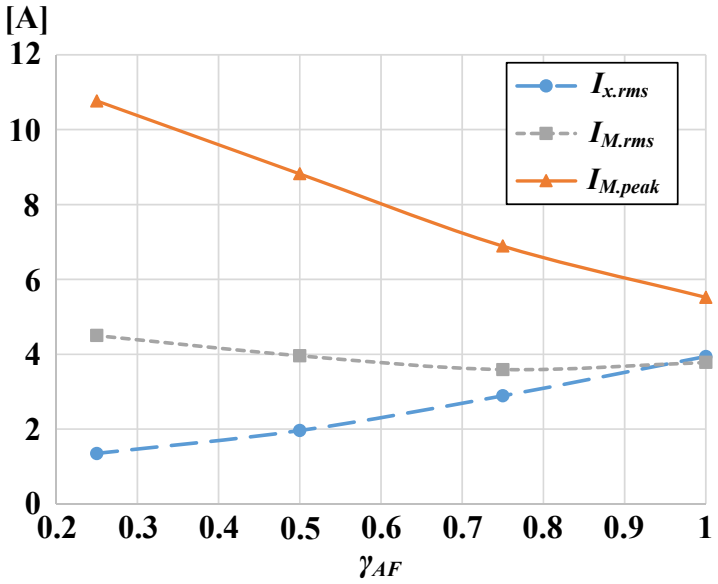


Fig. 4.23 $I_{x.rms}$, $I_{M.rms}$, and $I_{M.peak}$ in accordance with γ_{AF}.

Fig. 4.23 shows simulation results of the motor peak current and i_x variation where $P_{inv.avg}$ = 800 W and γ_{AF} is varied from 0.25 to 1. As α is decreased, the motor

peak current and rms value of i_x are gradually increased and decreased respectively, but the rms value of motor current $I_{M.rms}$ shows the minimum value at $\gamma_{AF} = 0.75$. Since term of di^r_{qs}/dt becomes much larger at $\gamma_{AF} < 0.75$, it requires extra flux-weakening current to secure MI during T_{GC}. This factor highly depends on the motor parameters, especially L_d and L_q. Fortunately, in this experiment condition, the $I_{M.rms}$ minimizing point matches to the point of (4.17).

In Appendix A.2, case study on the implementation cost of single-phase DSC system depending on γ_{AF} is presented. Considering the practical values based on the simulation and experimental results, the components are selected and compared with conventional diode rectifier system with heavy passive components.

4.4 Discussions

4.4.1 System Operating Strategies

In this section, the DSC for single-phase system and its operation have been proposed and demonstrated. Thanks to the DC-link voltage boosting and partial power assistance controls of DSC, the system could have benefits in terms of the flexible power control and the system efficiency. The partial power assistance control related to the γ_{AF} also lighten the power burden from DSC, and it has a

positive influence on DSC design.

There are design considerations for the DSC: The DSC capacity, the motor peak current (torque ripple), maximum $V_{dc1.min}$. Depending on the primary goal, DSC's strong point is changed and it is able to be flexibly modified.

1) Torque-ripple-free operation

It can be realized if the DSC system is working on the condition that γ_{AF} is equal to unity in overall operating area. This system is able to provide constant output power $P_{inv.avg}$ and the peak value of motor current is obviously minimized. However, the system cost and size are inevitably increased, since the capacity of DSC is designed with the assumption that the DSC should supply $P_{inv.avg}$ during T_{GD}. Moreover, in (4.18), excessive d-axis current degrades the system efficiency. As the motor speed becomes higher, the d-axis current becomes much larger and the efficiency might be rapidly decreased. Therefore, this operation is recommended to the system which requires high quality output and is mainly operated in low speed area.

2) Efficiency improvement operation

As aforementioned, if the DSC system can utilize $\gamma_{AF} < 1$ operation, the merits of DSC are maximized. Since the target applications such as air compressor and pump

are generous to the ripple output, this operation is able to be fully adopted. By utilizing the available DC-link voltage maximally, the DSC system can save d-axis current that causes extra motor conduction loss. In comparison with the torque-ripple-free operation, the DSC power P_{DSC} is reduced as $\gamma_{AF} \cdot P_{inv.avg}$ during T_{GD}, thus the energy storage capacitor C_{dc2} is also miniaturized with the ratio of γ_{AF}. However, it should be noted that the peak current of motor side is also increased as γ_{AF} is decreased. Therefore considering the maximum available peak current of the motor drive circuit, γ_{AF} should be chosen carefully. If the system is designed by using the design guideline mentioned in Section 4.2.3, the peak value of motor current can be minimized under the condition that the system efficiency is maximized.

4.4.2 Availability of single-phase DSC system

In this dissertation, 800-W single-phase DSC system has been tested and evaluated. However, if the rated power becomes larger, maximum available $V_{dc1.min}$ for satisfying grid regulation is varied. The maximum available $V_{dc1.min}$ is one of the most important factors to decide the feasibility of proposed method since it is directly related with available MI of the motor drive inverter. Fig. 4.24 shows the variations of $V_{dc1.min}$ and required maximum DSC energy $E_{DSC.MAX}$ in accordance with the inverter output power. $E_{DSC.MAX}$ is given by

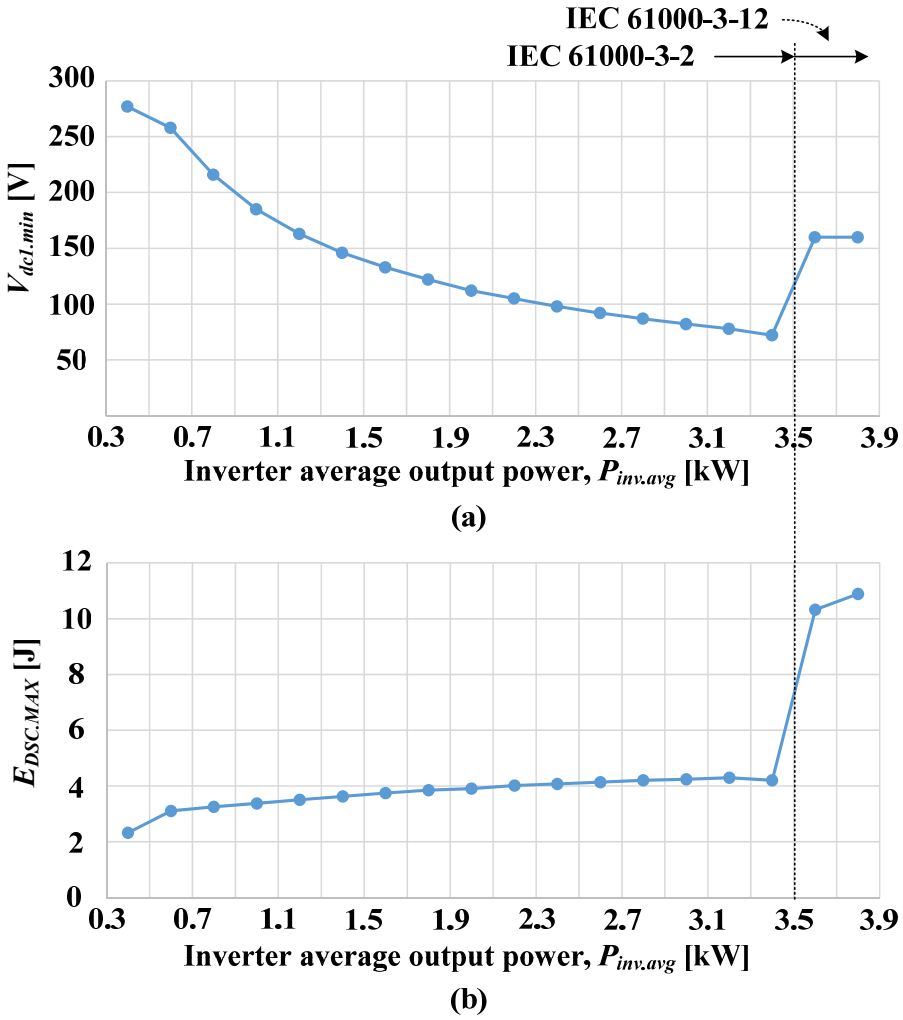


Fig. 4.24 The maximum available values of (a) $V_{dc1.min}$ and (b) $E_{DSC.MAX}$ in accordance with inverter average output power.

$$E_{DSC.MAX} = T_{GD} P_{inv.avg} . \tag{4.27}$$

Where $P_{inv.avg}$ is lower than 3.5 kW ($\approx$ 220 V·16 A), the limit values of IEC 61000-3-2 Class A shown in Table 2.1 is applied, and the limits of 'IEC 61000-3-12 $R_{sce.min}$

= 350, equipment for other than balanced three-phase equipment' shown in Table 2.2 is applied where $P_{inv.avg}$ is over 3.5kW. The Fig. 4.24(a) can be obtained by comparing FFT results of grid current in (4.10) and the relevant limit values with 10% margin.

As mentioned in Section 4.2.3, the motor drive inverter should perform flux-weakening control in operating area of (4.18) and suffers efficiency drop due to the d-axis current. As shown in Fig. 4.24(a), however, $V_{dc1.min}$ is gradually reduced as $P_{inv.avg}$ becomes larger where $P_{inv.avg} < 3.5$ kW. Because of the reduced $V_{dc1.min}$, the operating area of (4.18) is widened and the effectiveness of single-phase DSC system is undermined. Moreover, C_{dc2} should be increased in proportion to $E_{DSC.MAX}$ shown in Fig. 4.24(b). The required C_{dc2} can be represented as (4.28) by substituting (4.27) into (4.26).

$$C_{dc2} = \frac{2\gamma_{AF} E_{DSC.MAX}}{V_{dc2.\max}^2 - V_{dc2.\min}^2}. \tag{4.28}$$

On the other hand, in the power range that the system follows IEC 61000-3-12 which requires percentage limit values (individual current per fundamental current), the ratio of harmonics is equally maintained regardless of $P_{inv.avg}$ with respect to same $V_{dc1.min}$. In this region, $V_{dc1.min}$ can be increased up to 160 V which is greatly increased value comparing with 72 V ($V_{dc1.min}$ where $P_{inv.avg} = 3.4$ kW). Even though $E_{DSC.MAX}$ is considerably increased, C_{dc2} is adjustable by designing γ_{AF} or range of

v_{dc2}. If 1200-V devices are used for DSC, $V_{dc2.max}$ can be extended up to 800 V (2/3 x 1200) and it is possible to design C_{dc2} as $38\gamma_{AF}$ μF. Here, $V_{dc2.min}$ is set to 320 V considering peak value of v_{dc1} is 311 V.

To summarize, the single-phase DSC system is able to show remarkable performance where $P_{inv.avg}$ is low enough or higher than 3.5 kW. The proper 'low' rated power is not clearly defined since the performance of DSC system depends on system conditions such as motor parameters and operating point. However, it is obviously disadvantageous to design DSC system under the condition that $P_{inv.avg}$ is slightly lower than 3.5 kW.

5 Conclusion and Future Works

This dissertation proposes grid current shaping and DSC operating methods in the diode rectifier-fed motor drive system. Starting on the elimination of the electrolytic capacitor, the motor drive system without heavy grid filter inductor fulfills circuit compactness and robustness against component failure. The grid current shaping method is proposed to cover the absence of the grid filter inductor, and the method can be implemented in both inverter and DSC. If DSC is utilized, the performances of motor drive system are able to be improved. Depending on the desired performance among the cost reduction, power ripple reduction, and efficiency improvement, the system can be flexibly designed.

The proposed operating method using DSC can be employed in both three- and single-phase systems. Considering the conditions and requirements for each system, the operating methods have been analyzed and evaluated in this dissertation. For the three-phase system, the compensation current for mitigating high order grid current harmonics was suggested and its effect on grid current was analyzed. The compensation current is able to be generated by the inverter or DSC. If the inverter makes it, the most cost-effective system is realized but the effort to make compensation current degrades output torque quality. On the other hand, the DSC can cover these drawbacks and even improve total system efficiency in high speed area where the air compressor is mainly operated. From the experimental results,

efficiencies with and without DSC indicate 87.57 % and 88.4 %. Moreover, since the compensation current is about five times smaller than the main flow current, the DSC components such as switches and interface inductor can be miniaturized. The proposed compensation method implemented in both inverter and DSC were suggested, and the feasibility was verified by the comparative experiments with the conventional systems.

The operating method for single-phase DSC system was also proposed in this dissertation. In the case of the DSC employed in single-phase system, its DC-link boosting and motor power supporting controls excellently improve the system efficiency in comparison with the conventional small DC-link capacitor system. Through the partial power assistance operation, the rated power of DSC can be flexibly adjusted, and it help to design the DSC system. Here, there are some design considerations such as DSC capacity, motor peak current, and available $V_{dc1.min}$. Among them, the available $V_{dc1.min}$ is the most important factor that determines a system usefulness. If the applicable regulation is generous to grid current harmonics, the feasibility of single-phase DSC is maximized. On the contrary, if the regulation requires grid current similar with sinusoidal waveform, the effectiveness might be reduced. In the laboratory experimental condition, it was enough to show the worth of DSC. It was verified that the efficiency of DSC system is much higher than that of the conventional small DC-link capacitor system. Even the value shows around

6 % difference at rated power, exhibiting each values of 89.3 % and 83 %.

For further works, efficiency optimization of the DSC should be fulfilled. Applying zero-voltage-switching (ZVS) or zero-voltage-transition (ZVT) auxiliary networks may help to reduce the switching loss of the semiconductors in the DSC. In addition, for the duality, the series type compensation circuit which performs grid current shaping and motor drive supporting controls should be considered. The DSC in this dissertation is a kind of parallel compensation circuit and has advantages in reduced current rating and flexible ON/OFF control. On the other hand, the series compensation circuit has merits in low voltage rating and DC-link voltage controllability which have influence on motor drive efficiency. By using similar concept of the conventional topology called electric smoothing inductor, the electrolytic capacitor-less series compensation circuit can be implemented.

Appendix

A.1 Case Study 1: Implementation Cost of Three-Phase DSC System

Based on the simulation and experimental results in Section 3, implementation cost for three-phase DSC system can be approximately expected. Considering that the system rated power is 5.5-kW and α in proposed system is 4, the component costs of both DSC and conventional heavy passive components systems are listed in Table A.1 and Table A.2, respectively. The costs are based on the single purchase price of available commercialized components in on-line market [71][72]. In both cases, they need additional circuits which are not listed in two tables. The DSC system needs gate drive circuit for S_1 and S_2, and the conventional system also requires pre-charging circuit for preventing inrush current. Excluding all these minor costs, this case study lists and compares power components that are differently used in both systems.

As shown in these tables, the cost of the proposed system is smaller than that of conventional system even if inductor cost is excluded. Moreover, since L_x in DSC system can be designed much smaller and cheaper than L_{dc} in conventional system, three-phase DSC system can achieve remarkable cost reduction in power components.

Table A.1 Implementation cost of proposed three-phase DSC system

Component	Value	Part No.	Quantity	Unit Price (KRW)	Price (KRW)
Film Capacitor (C_{dc1})	4.7 μF /450V	ECW-FD2W475J	4	1,453	5,812
Film Capacitor (C_{dc2})	40 μF /450V	B32776G4406K	1	17,711	17,711
Switching Device (S_1, S_2)	14 A /600V	STGPL6NC60D	2	922	1,844
Inductor (L_x)	0.9 mH, 20 kHz, 3.4 A_{rms}		1	-	-
Total cost			25,367 (KRW) + cost of L_x		

Table A.2 Implementation cost of conventional three-phase system with heavy passive components

Component	Value	Part No.	Quantity	Unit Price (KRW)	Price (KRW)
Electrolytic Capacitor (C_{dc})	680 μF /400V	LLG2G681MELB45	4	7,904	31,616
Film Capacitor	0.1 μF /450V	ECW-FD2W104JQ	1	567	567
Inductor (L_{dc})	0.7 mH, 360 Hz, 16 A_{rms}		1	-	-
Total cost			32,183 (KRW) + cost of L_{dc}		

A.2 Case Study 2: Implementation Cost of Single-Phase DSC System

In the case that the system rated power is 800-W which is same condition of experiment, implementation cost of single-phase DSC system is listed in Table A.3. Each component cost is based on the single purchase price of available commercialized product, similar with in case of three-phase DSC system [71][72]. The cost is estimated in two cases, γ_{AF} = 1 and 0.25. Two cases require C_{dc2} of 120 μF and 30 μF, respectively. Other components are selected under the condition that the components can cover the values of $I_{M.peak}$ and $I_{x.rms}$ in Fig. 4.23.

As shown in Table A.3, the film capacitor for C_{dc2} is the most important component which dominantly decides total system cost. By reducing it through the partial power assistance operating, the total cost of DSC system with γ_{AF} = 0.25 approximately becomes similar with that of conventional diode rectifier system with heavy passive filter shown in Table A.4 except the inductors L_x and L_{dc}. The total cost of DSC system may have cost competitiveness if the inductor is taken into account. Here, it is noted that the intelligent power modules (IPMs) of 6 A and 15 A show small cost difference in this power area. By using this factor, we can reduce γ_{AF} more on condition that $I_{M.peak}$ is lower than 15 A. In this case, the total cost is obviously reduced, but we should consider practical problems such as system

efficiency, v_{dc2} controllability or switching ripples in v_{dc2}.

Table A.3 Implementation cost of proposed single-phase DSC system

Component	Value	Part No.	Quantity	Unit Price (KRW)	Price (KRW)
Film Capacitor (C_{dc1})	4.7 μF /450V	ECW-FD2W475J	1	1,453	1,453
Film Capacitor (C_{dc2})	30 μF /700V	MKP1848S63070JY5F	4 (γ_{AF} = 1)	10,182	40,728
			1 (γ_{AF} = 0.25)		10,182
Switching Device (S_1, S_2)	14 A /600V	STGPL6NC60D	2	922	1,844
Intelligent Power Module (IPM) (Inverter)	6 A /600V	IGCM06F60GA (γ_{AF} = 1)	1	14,026	14,026
	15 A /600V	IGCM15F60GA (γ_{AF} = 0.25)	1	14,999	14,999
Inductor (L_x)	2 mH, 20 kHz, 4 A_{rms} (γ_{AF} = 1)		1	-	-
	2 mH, 20 kHz, 1.3 A_{rms} (γ_{AF} = 0.25)				
Total cost		γ_{AF} = 1	58,051 (KRW) + cost of L_x		
		γ_{AF} = 0.25	28,478 (KRW) + cost of L_x		

Table A.4 Implementation cost of conventional single-phase system with heavy passive components

Component	Value	Part No.	Quantity	Unit Price (KRW)	Price (KRW)
Electrolytic Capacitor (C_{dc})	390 μF /450V	EKMQ451VSN391MR50S	2	6,865	13,730
Film Capacitor	0.1 μF /450V	ECW-FD2W104JQ	1	567	567
IPM (Inverter)	6 A /600V	IGCM06F60GA	1	14,026	14,026
Inductor (L_{dc})	7.5 mH, 120 Hz, 4 A_{rms}		1	-	-
Total cost			28,323 (KRW) + cost of L_{dc}		

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초 록

계통 필터 인덕터나 직류단 캐패시터와 같은 수동소자들은 간단한 구현 방식으로 인해 전력 변환 시스템에서 널리 사용되어 왔으나, 전체 시스템에서의 부피 및 가격 비중이 상당히 크고, 특히 직류단에 사용되는 전해 캐패시터의 경우 높은 고장률로 인해 전체 시스템의 신뢰성을 저하시키는 문제가 있다. 따라서 이들을 줄이기 위해 새로운 제어 방식 또는 낮은 정격 용량의 능동 소자를 이용한 토폴로지들이 제안되어 왔으며, 이러한 방식들은 능동 소자들의 고성능화 및 저가격화 동향에 부합하며 그 효용성이 나날이 높아지고 있다.

이에 본 논문은 소용량 수동 소자와 직류단 병렬 회로(DC-link shunt compensator, DSC)를 가지는 다이오드 정류기 연계형 전동기 구동 시스템에서 제어 방식에 대해 제안한다. 제안된 시스템은 전해 캐패시터를 사용하지 않아 보다 높은 신뢰성을 가지며, 제안된 방식을 사용한 다이오드 정류기 시스템은 역률 보상기(power factor correction, PFC)나 대용량 계통 필터 인덕터 없이도 충분히 IEC 61000-3-12 또는 3-2와 같은 계통 규정을 만족시킬 수 있다. 제안된 방식에는 계통 고조파 보상을 위한 계통 전류 합성 방식과 시스템 성능 개선을 위한 시스템 운영 방식이 포함되어 있다.

본 논문은 계통 전류 보상 방식을 추가 회로 없이 전동기 구동 시스템에서 구현하는 것과 직류단에 병렬로 연결된 DSC에 의해서 구현하는 방식 모두에 대해 제공한다. 전자는 제안된 제어를 구현할 수 있는 가장 가격 경쟁력 있는 방식이지만, 필연적으로 전동기 운전 영역이나 토크 리플과 같은 출력 성능이 저하된다. 후자는 DSC 구현을 위한 소량의 스위칭 소자 및 수동 소자가

추가되지만, DSC의 협력 제어를 통해 전동기 출력 품질 또는 전체 시스템 효율 개선에 대한 다양한 자유도를 가질 수 있다. 본 논문에서는 이러한 시스템 운전 방식에 대해 상세히 언급하고, 각 방식에 대한 시스템 설계 지침에 대해서도 제공한다.

DSC 운전 방식은 단상 및 3상 다이오드 정류기 시스템 각각에 대해 제안된다. 소용량 수동 소자를 사용한 시스템의 경우 단상 및 3상 입력에 따른 직류단 전압의 형태가 매우 다르기 때문에, 그에 따른 제어 방식 또한 다르게 수립된다. 본 논문에서는 각 시스템에서의 제어 방식에 대해 언급하며, 이를 통한 시스템 효용성에 대해서도 논의한다. DSC의 실시예로서 승압형 컨버터를 선정했으며, 모의실험 및 실험을 통해 그 타당성을 검증한다.

주요어 : 소용량 직류단 캐패시터 시스템, 직류단 병렬 보상기, 수동 소자, 역률 보상 회로, 전동기 구동 인버터.

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