Ph.D. DISSERTATION

A Guard Ring for Suppressing Coupling Noise Utilizing Inversion Layer for Through Silicon Via

Through Silicon Via의 Coupling Noise를 억제하는 반전 전하층을 이용한 Guard Ring 제작 및 분석

BY

KYUNGDO KIM

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DEPARTMENT OF ELECTRICAL ENGINEERING AND
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SEOUL NATIONAL UNIVERSITY

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指導敎授 李宗昊

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Abstract

As technology shrinks, the implementation of high-density chip with a two-dimensional (2-D) planar architecture is becoming more difficult due to the limitation of lithography process. To overcome such scale-down limitations, a three-dimensional (3-D) package has been investigated. Among the various 3-D package technologies, a through silicon via (TSV) is a promising technology in which several chips are stacked vertically and electrically. This 3-D package can enhance the memory capacity, and implement a system with different functional chips. Although TSVs offer many advantages when used to achieve a high-density package, they also have several disadvantages, such as coupling noise. A high-frequency signal applied to a TSV induces noise in transistors near the TSV due to electrical coupling. Another issue is that copper (Cu) which is used as a conducting material of the TSV generates trap density caused by large diffusivity of Cu atoms.

In this dissertation, we propose a new guard ring which consists of a shallow n^+ region, a deep *n*-well, and an inversion layer formed along the interface between the oxide surrounding the TSV (TSV oxide) and the *p*-substrate. The proposed guard ring utilizes an inversion charge induced by a positive oxide charge located at the interface of the TSV oxide. We characterize

quantitatively a TSV with a guard ring which is used to reduce the coupling noise from the TSV by utilizing an inversion layer as a shield layer. It is shown that a transient current due to the coupling is clearly reduced when the proposed guard ring is used. The proposed method is compared with a conventional guard ring method in terms of the drain current of a victim nMOSFET. The effective depth of the inversion layer with the signal frequency is also characterized. It is demonstrated that the high-frequency response of the guard ring can be modeled as an *RC* equivalent circuit. The proposed guard ring is effective in shielding the coupling noise and can be fabricated easily by modifying the ion implantation mask layer.

A TSV conducting material requires high conductivity for low power consumption and high-speed operation. Cu is widely used as a TSV conducting material, but Cu atoms diffuse to the adjacent silicon substrate and transistors easily and generate traps during a low temperature annealing process. It is very important to suppress Cu diffusion and to devise a proper method to measure how many Cu atoms diffuse due to annealing. However, the characteristics of traps induced by Cu diffusion in a TSV are not easily measured because TSVs are typically located some distance away from the silicon surface, reaching a depth of tens of micrometers. For this reason, the deep part of a TSV cannot be measured. We suggest a measurement method which can be used to evaluate the trap density generated by Cu diffusion through the use of the proposed guard

ring and analyze Cu diffusion as a parameter of the thickness of the barrier metal.

Key Words: Through silicon via, TSV, guard ring, coupling noise, inversion layer shielding, copper diffusion

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Contents

Chapter 1

Introduction

1.1 Background of TSV

To fabricate high-density memory, it is necessary to reduce the gate lengths of the transistors and the widths of the interconnection lines. As the gate length decreases, a short channel effect which makes the off-leakage current increase becomes worse. It is necessary to increase the effective gate length to suppress the short channel effect. As shown in Fig. 1.1 [1], the recess channel [2], the spherical recess channel [3], and the fin-shaped recess channel [4] have been adopted in the cell transistors of DRAM. Moreover, a vertical channel can also be used to enlarge the effective gate length [5]. Despite the development of all of these structures, as technology shrinks, the down-scaling of transistors becomes more difficult due to the limitation of lithography process [6]. To overcome

these scale-down limitations, a three-dimensional (3-D) package using a through silicon via (TSV) is a promising technology [7-8]. The TSV is used to stack several chips vertically and electrically (Figs. 1.2 and 1.3) [9-10]. It consists of conducting materials which fill a deep trench and which are isolated electrically by a dielectric material. Through the conductor materials, the electrical power and signal are delivered. The 3-D package stacked with TSVs can enhance the memory capacity [9] and lead to the realization of a system with different functional chips. For example, the central processing unit (CPU) and the memory are combined in a single chip while maintaining a small package volume without a loss of performance [11]. Although a TSV has many advantages when used to achieve a high-density package, it also has several disadvantages, such as becoming a source of mechanical stress on transistors (Fig. 1.4) [12] and generating traps due to copper (Cu) contamination (Fig. 1.5) [13] caused by the large diffusivity of Cu atoms (Fig. 1.6) [14]. Furthermore, TSVs produce coupling noise. They can also serve as paths for power delivery and for high-frequency signals, such as a clock. A high-frequency signal applied to a TSV induces noise in transistors near the TSV due to the electrical coupling (Fig. 1.7) [15]. To reduce this coupling noise, it is necessary to create a guard ring near the TSV. A metal guard ring can be used to reduce the coupling noise, but this complicates the fabrication of the TSV given the double metal layer.

In the present work, we propose a new guard ring method which utilizes the

inversion charge induced by a positive oxide charge located at the interface between the *p*-substrate and the TSV oxide surrounding the TSV (TSV interface). The proposed guard ring has a shallow n^+ region formed in an *n*-well butted to the TSV oxide surrounding the TSV. The proposed guard ring can effectively reduce the coupling noise simply by modifying the ion implantation mask without an additional process. Moreover, we can measure the diode and gated diode currents, the charge pumping current, and *C-V* to analyze the effect with the proposed guard ring accurately. Our approach is demonstrated to be very useful by investigating the Cu diffusion effect in samples with two different barrier metal thicknesses.

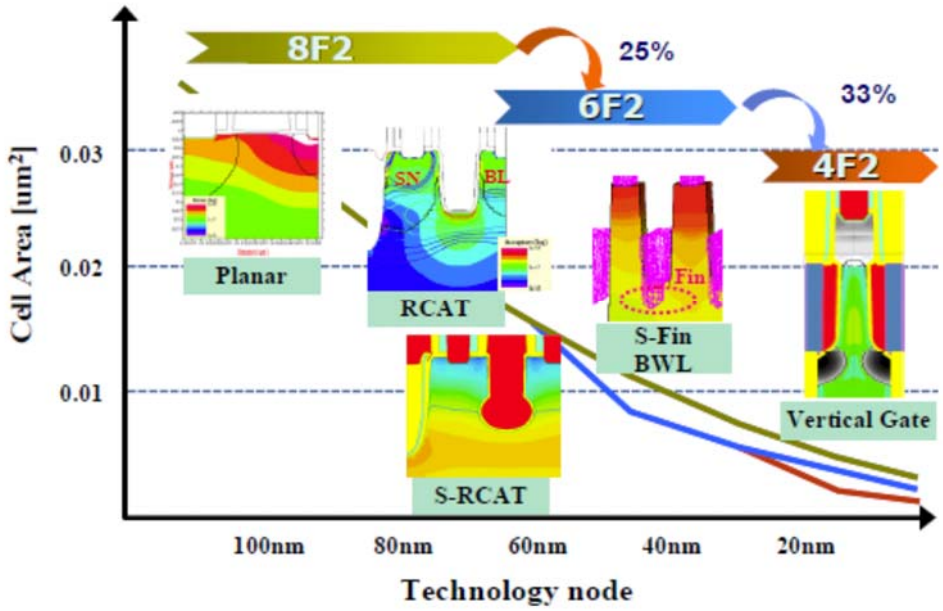


Fig. 1.1. Trend of cell transistor scheme with technology node [1].

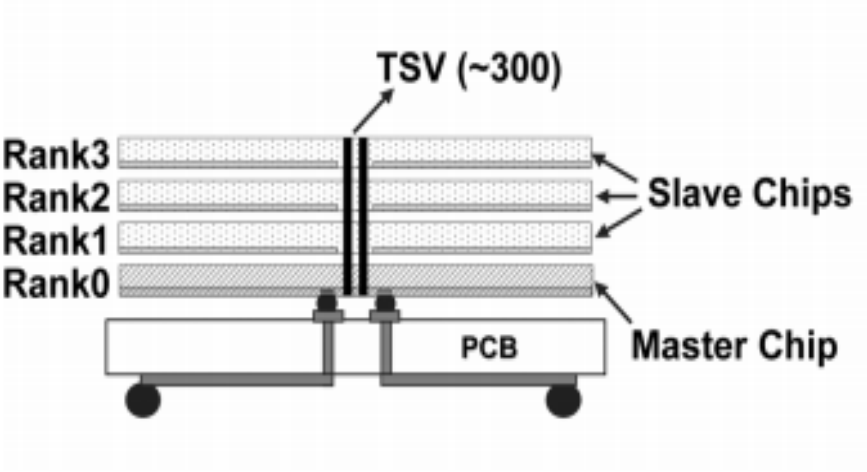


Fig. 1.2. Conceptual image of high-density DRAM with TSVs [9].

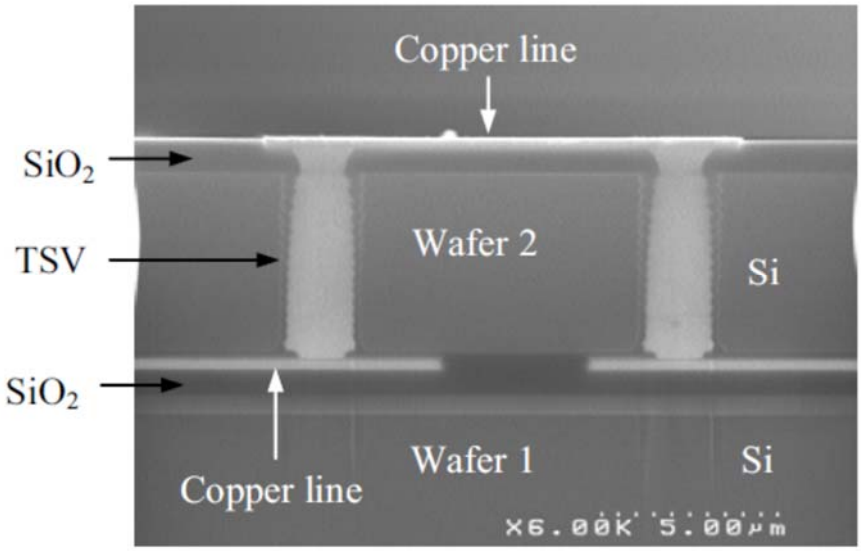


Fig. 1.3. Cross sectional TEM image of TSVs [10].

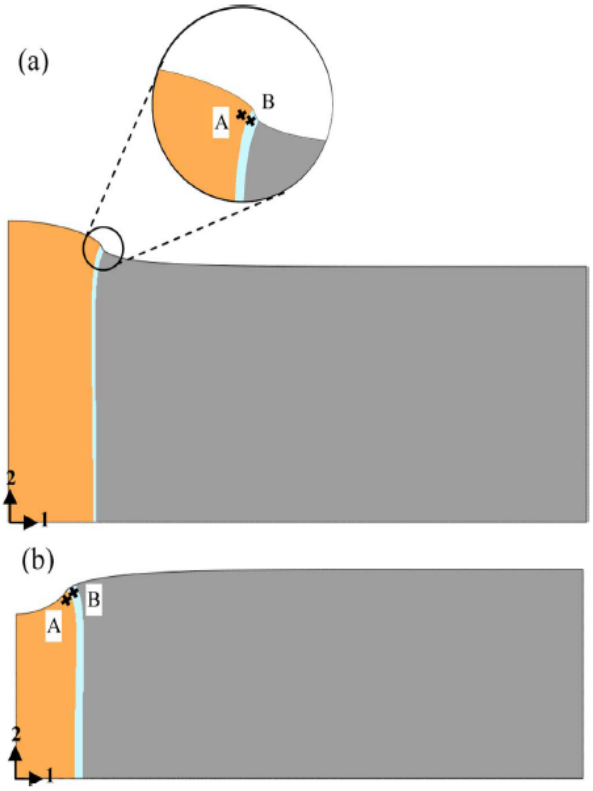


Fig. 1.4. Mechanical stress on silicon wafer near TSV due to the difference of the coefficient of thermal expansion between Cu and silicon. Conceptual deformation of TSV and silicon (a) at high temperature (125 ˚C) (b) at low temperature (–40 ˚C) [12].

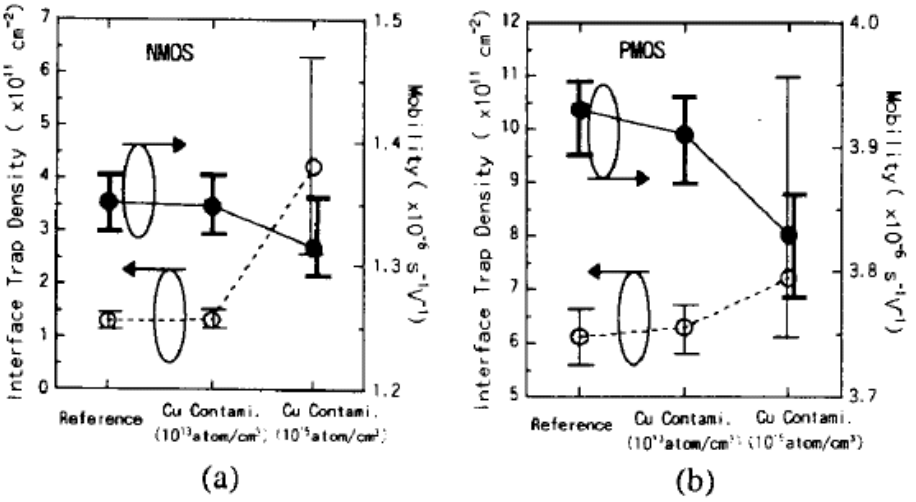


Fig. 1.5. Interface trap density and mobility of (a) nMOSFET and (b) pMOSFET for different Cu density [13].

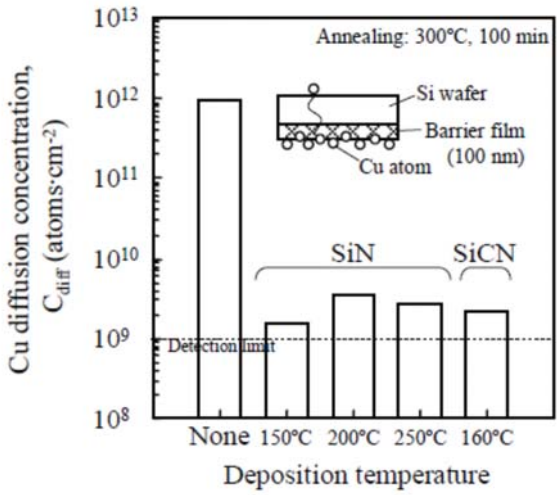


Fig. 1.6. Cu diffusion concentration from backside to front side of various barrier-film wafers [14].

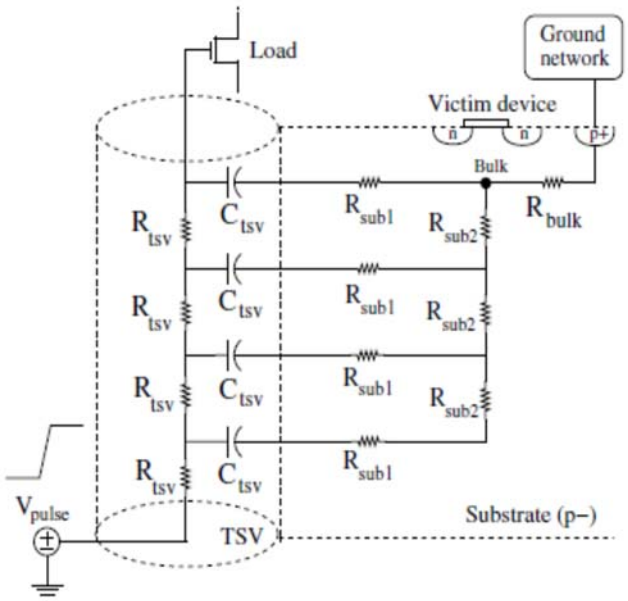


Fig. 1.7. Circuit model to represent noise coupling into the substrate by a TSV [15].

1.2 Motivation for the research

A TSV is an excellent solution because it can reduce the lengths of metal connections between chips which are integrated vertically. However, the coupling noise from the TSV becomes severe as the operating frequency increases. The high-frequency signal passes through the TSV, and the TSV and the peripheral devices near the TSV are coupled by the resistance and capacitance. The reduction of the coupling by means of low-depletion capacitance near the TSV has been reported [16]. However, to the best of our knowledge, there has been no report of a shielding method of the entire side surface of a TSV without additional process steps. In this work, we propose a simple shield technique to suppress the coupling noise and demonstrate device characteristics related to the technique and performance gain.

The second issue related to TSVs is Cu diffusion. Cu, which is used as a conductor in TSVs, can diffuse easily from the TSV to peripheral devices even at a low temperature, resulting in trap generation in the peripheral devices. Thus, it is necessary to characterize the effect of Cu diffusion electrically. Although a transient capacitance (*C*-*t*) method has been reported [17], it is limited in terms of its ability to profile the traps and identify the surface and bulk traps. The proposed guard ring is very efficient when used to analyze precisely the trap profile induced by Cu diffusion, and we verify experimentally its effectiveness.

Chapter 2

Structure of the guard ring and the TSV

2.1 Introduction

A TSV consists of the conductive material and the TSV oxide, which separates the TSV conductor from a *p*-substrate silicon, as shown in Fig. 2.1. A TSV requires a guard ring to suppress coupling noise. A metal guard ring can effectively suppress coupling noise, but its fabrication is very complicated, and a large area is needed for the guard ring [18]. A dopant-type guard ring is easy to fabricate, but its shielding ability is lower that of a metal guard ring [16]. We suggest a very effective guard ring structure. The proposed guard ring is implemented by forming a shallow n^+ doping region in an *n*-well in the active region surrounding the TSV. This is referred to as the n^+/n guard ring henceforth. Fig. 2.2 shows a cross-sectional and a top view of the proposed guard ring. The shallow n^+ region is identical to the source and drain of an nMOSFET, and the *n*-

well is identical to a well of pMOSFET. Therefore, changes to only the ion implantation mask and the active-define mask are needed and extra processes are not required. A TSV without an *n*-well region was also prepared for comparison and the *p*-halo doping is implemented to cover the n^+ region to create the shallow junction shown in Fig. 2.3. The conventional TSV is implemented in the STI region, but the proposed guard ring is formed in the active region in order to use the junction guard ring. Two types of guard ring are butted to the TSV oxide.

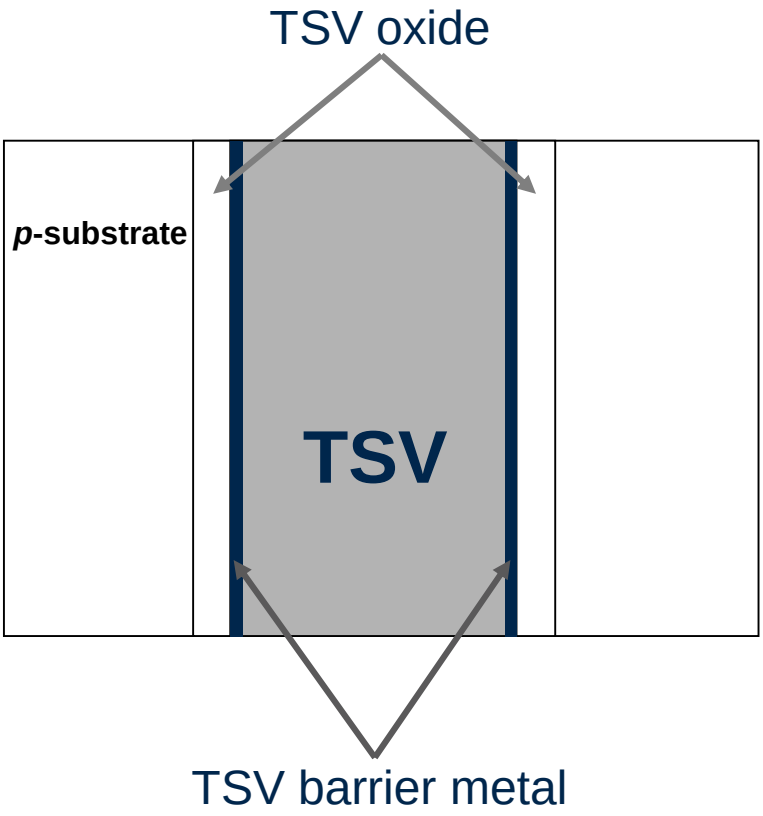
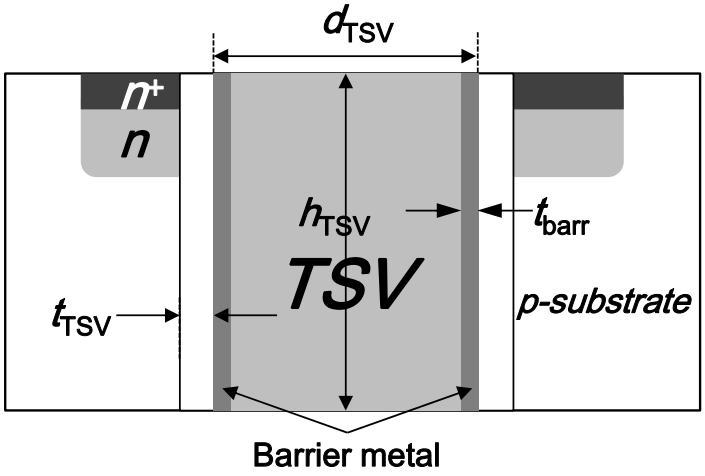
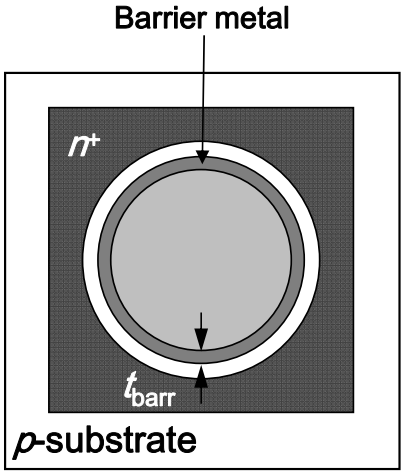


Fig. 2.1. Cross section of conventional TSV. A TSV conducting material is made of Cu and the TSV is separated from the *p*-substrate by the TSV oxide.



(a)



(b)

Fig. 2.2. Cross-sectional view (a) and top view (b) of the schematic of the proposed guard ring (n^+/n guard ring). The d_{TSV} and the h_{TSV} are the diameter and the height of the TSV, respectively. The t_{TSV} is the thickness of the TSV oxide, and t_{barr} is the thickness of barrier metal of the TSV.

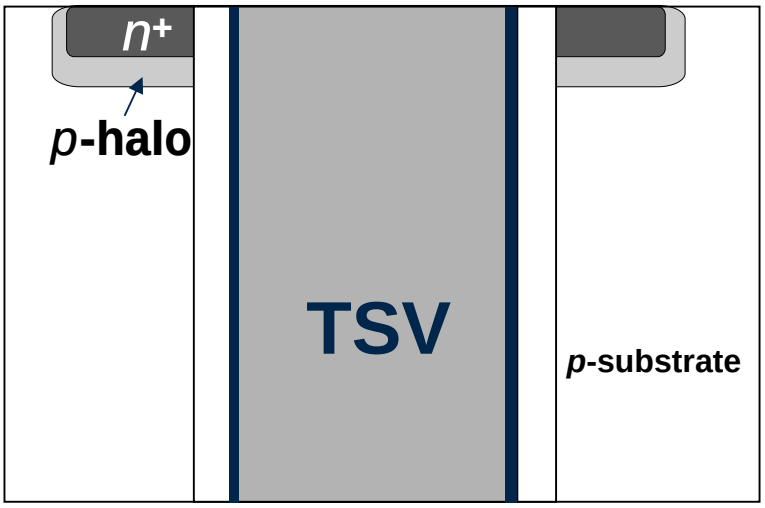


Fig. 2.3. Schematic cross-sectional views of n^+ guard ring. The shallow *p*-halo dopant covers the n^+ region instead of the *n*-well of n^+/n guard ring.

2.2 Process flow of fabricating TSV and guard ring

Test devices were fabricated using a conventional DRAM process. The test patterns of the proposed guard ring with the TSVs were fabricated on the *p*-substrate. Cylindrical TSVs were formed after front end process. Fig. 2.4 shows the process flow of fabrication of the TSV. The TSV is formed in the active region and the active-define mask should be modified for the guard ring. The *n*-well of the guard ring is formed the same as the well of pMOSFETs and the n^+ region is formed the same as the source and drain of nMOSFETs simultaneously. This means that additional process is not necessary. After forming transistor, the via-hole for the TSV was formed by reactive ion etch (RIE). After forming the TSV holes, a layer of SiO_2 for a TSV dielectric (TSV oxide) was deposited by chemical vapor deposition (CVD). Because the thickness of the TSV oxide should be over 100 nm, the TSV oxide is formed by CVD process instead of thermal oxidation. The barrier metal is formed by titanium nitride (TiN) and a conducting material is formed on the TSV oxide inside the via-holes. Cu is used as a conducting material because of the low resistivity [19]. After forming TSV metal, the interconnection line is formed to be connected to the electrical pad, then forming gas anneal is performed to passivate the trap and increase the reliability of devices. The key processes of the proposed guard ring are the ion implantation, RIE, and CVD oxidation.

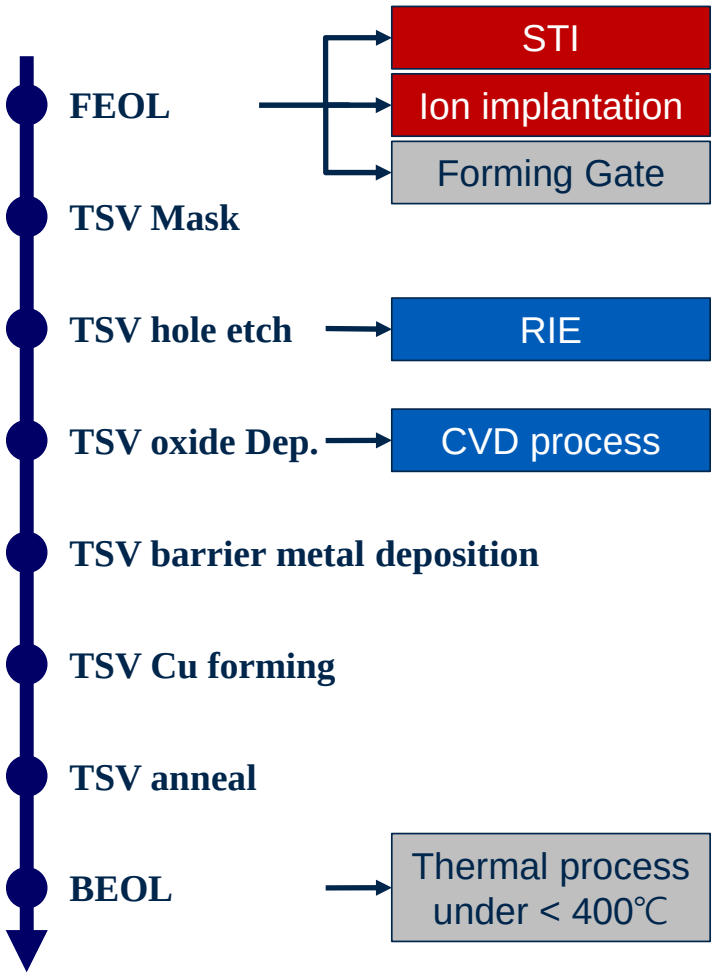


Fig. 2.4. Process flow of forming the TSV and the guard ring. The proposed guard ring is formed by modifying the active-define mask and the ion implantation mask.

Fig. 2.5 shows the process flow that TSVs penetrate the silicon wafer from the front side to the backside with forming a backside bump. Because the thickness of wafer is about 700 μm while the diameter of wafer is 300 μm, it is impossible to etch the TSV hole directly for penetrating entire wafer. Fig. 2.5 (a) shows the silicon wafer after the fabrication of the device and TSVs. To make TSVs penetrate the silicon wafer, the backside of the silicon wafer is processed in Fig. 2.5 (b) – Fig. 2.5 (i). The backside of the silicon wafer is polished (Fig. 2.5 (c)) and etched to make TSVs exposed without lithography (Fig. 2.5 (d)). After etching, silicon nitride (Si_3N_4) and silicon dioxide (SiO_2) are deposited on the wafer (Fig. 2.5 (e)). To make TSVs exposed, the backside of the silicon wafer is polished again (Fig. 2.5 (f)). After polishing, lithography is performed to define a bump region (Fig. 2.5 (g)), and Cu for the backside bump is formed in the bump region (Fig. 2.5 (h)). After removing the photo resist (Fig. 2.5 (i)), the silicon wafer with the TSVs and the backside bump in Fig. 2.5 (j) can be stacked with the other wafers to fabricate multi-chip package with TSVs.

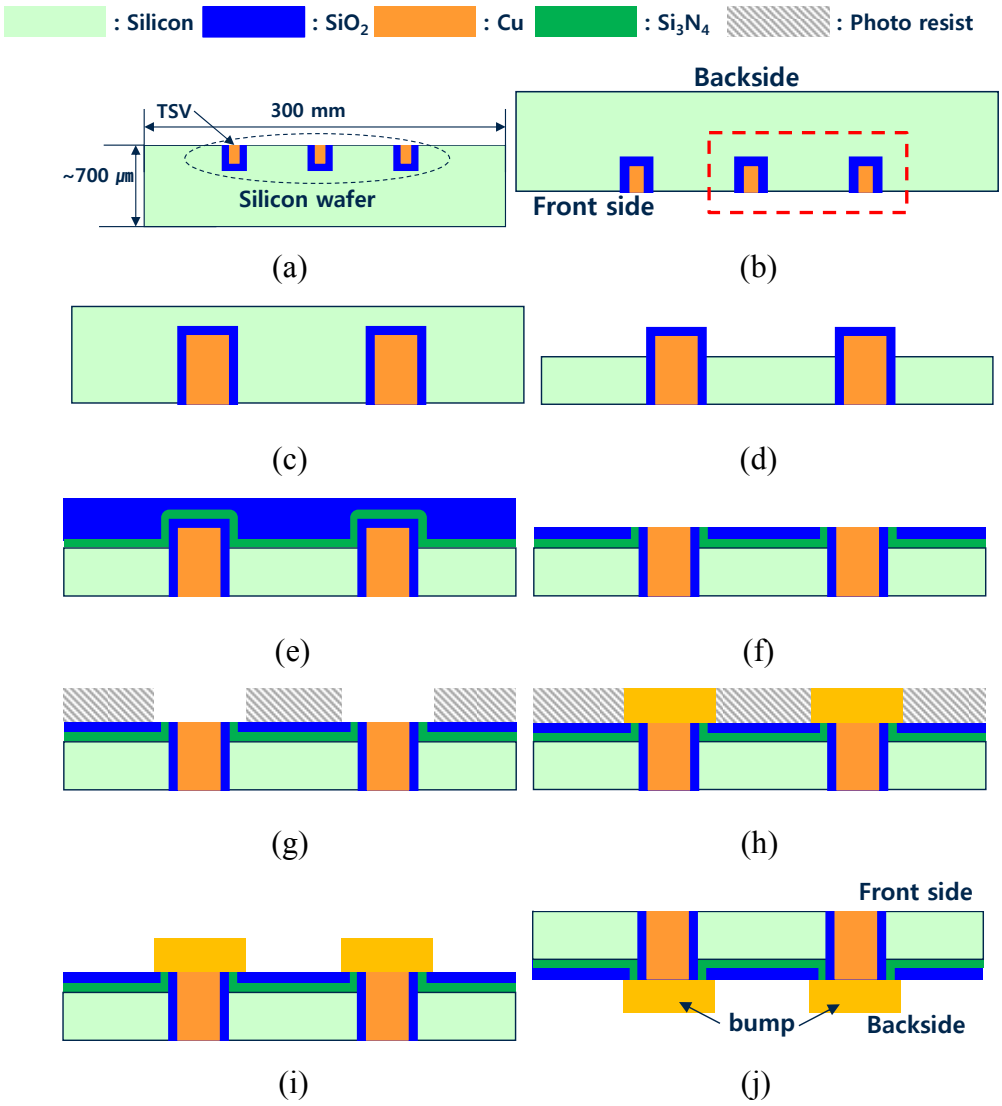


Fig. 2.5. Process flow that TSVs penetrate the silicon wafer. (a) silicon wafer after the fabrication of the device and TSVs, (b) turning the wafer upside down, (c) polishing, (d) etching the wafer without mask patterning, (e) depositing Si_3N_4 and SiO_2, (f) polishing, (g) mask patterning for opening bump, (h) Cu forming, (i) remove photo resist, and (j) the silicon wafer with TSVs and the back side bump.

2.3 Structure of the TSV and the proposed guard ring

Figs. 2.6 and 2.7 show the cross sectional TEM image of TSV. The height (h_{TSV}) and diameter (d_{TSV}) of the TSVs are several tens of micrometers and several micrometers, respectively. The conventional TSV is formed in the STI region, and the STI region is shown around the TSV in Fig. 2.6. But the proposed guard ring and the TSV are formed in the active region shown in Fig. 2.7. The n^+ source region formed in the *n*-well doping (n^+/n guard ring) butted to the TSV oxide, and the other guard ring has only the n^+ source formed on a shallow *p*-type dopant (n^+ guard ring). The *n*-well doping is equivalent to *n*-type dopant of the peripheral pMOSFET, and the n^+ doping is equivalent to *n*-type dopant of the peripheral nMOSFET in n^+/n guard ring. The *p*-type dopant in the n^+ guard ring is equivalent to the *p*-type halo to suppress the short channel effect of the peripheral nMOSFETs.

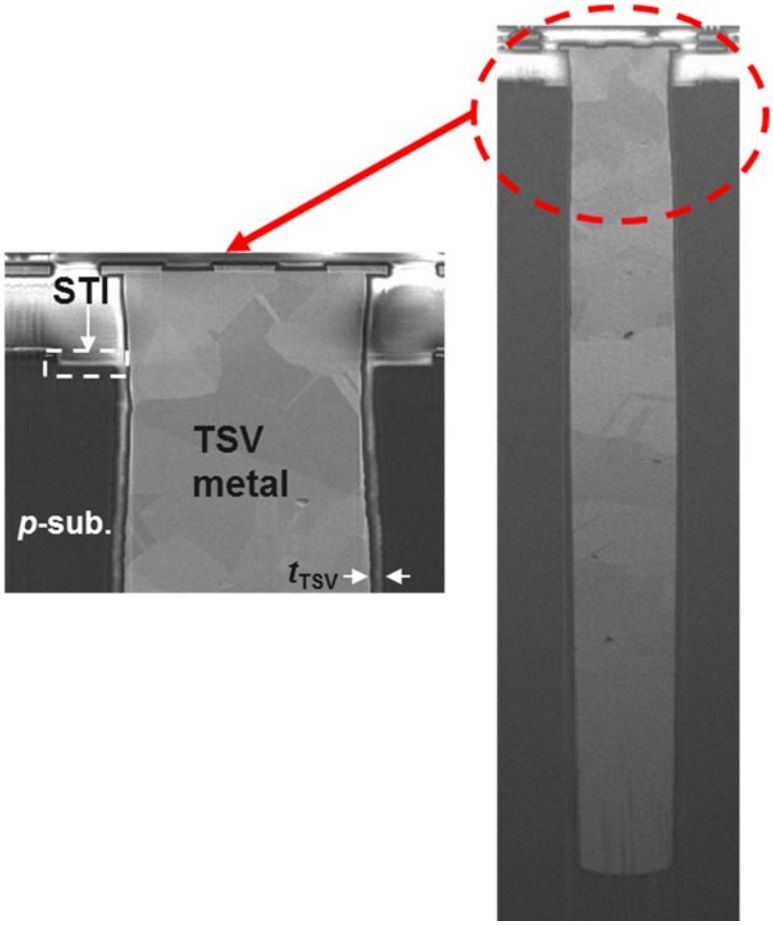


Fig. 2.6. Cross sectional TEM images of conventional TSV which is formed in the STI region.

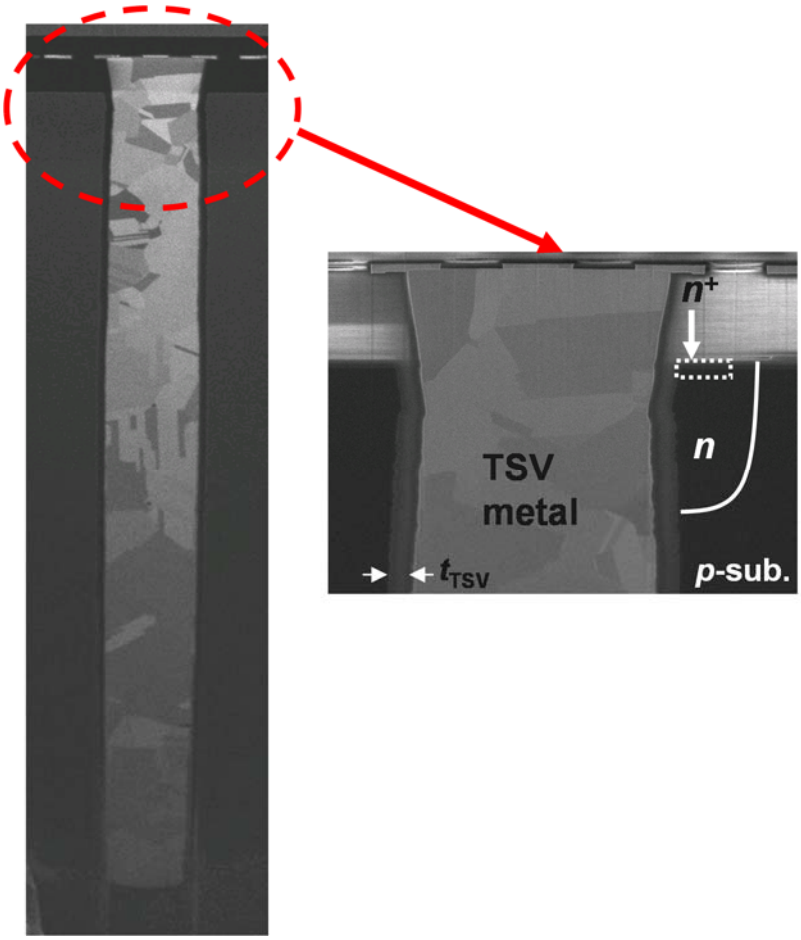


Fig. 2.7. Cross sectional TEM images of the proposed guard ring and the TSV which is formed on the n^+/n-well in the active region.

Chapter 3

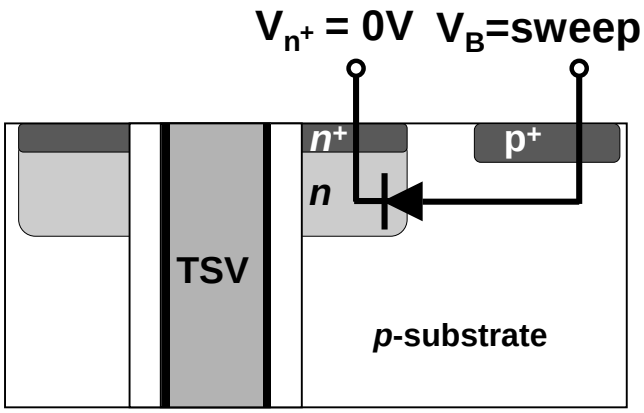
Characteristics of the proposed guard ring

3.1 Introduction

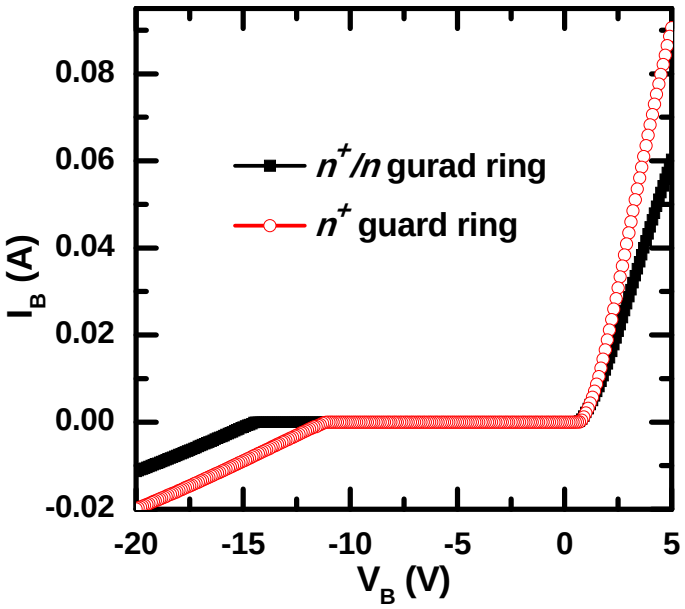
In a previous chapter, we fabricated a new guard ring and a TSV to verify its ability to reduce the coupling noise induced by a TSV. In this chapter, the basic characteristics of the proposed guard ring and the TSV are analyzed and simulated. The device simulator “ATLAS” (Silvaco Data Systems Inc.) was used for the simulation. The TSV, *p*-substrate, and n^+/n guard ring create the inversion charges surrounding the TSV, and this inversion charge is the key characteristic of the effective shielding method of the proposed guard ring.

3.2 Junction characteristics of the proposed guard ring

Figs. 2.2 and 2.3 show the cross sectional images of the n^+/n and the n^+ guard ring, and the *n*-type dopant and the *p*-substrate make *p*-*n* junction. Fig. 3.1 (a) shows the test condition to measure the diode current of the proposed guard ring. Fig 3.1 (b) shows the *I*-*V* curves of *p*-*n* junction diodes of two different guard rings. The breakdown voltage of the n^+/n guard ring is larger than that of n^+ guard ring while forward current of the n^+/n guard ring is smaller than that of n^+ guard ring due to gradual doping of the *n*-well. Fig. 3.2 (a) shows the test condition to measure the gated-diode current (I_{n+}) in the proposed guard ring. Fig. 3.2 (b) shows the I_{n+} of the n^+/n guard ring as a parameter of body bias (V_B) at different temperatures. The generation currents of the guard ring increase with the increase of $|V_B|$ and temperature because the traps in the interface between the TSV oxide and the *p*-substrate (TSV interface) and in the bulk of the depletion region in the *p*-substrate surrounding TSV make thermal generation current. Thus, the gated-diode current of the proposed guard ring can be used to characterize the trap density, and it will be analyzed to investigate Cu diffusion in chapter 4.

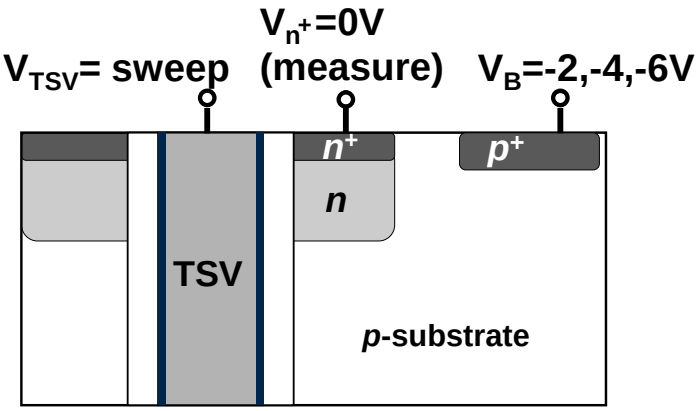


(a)

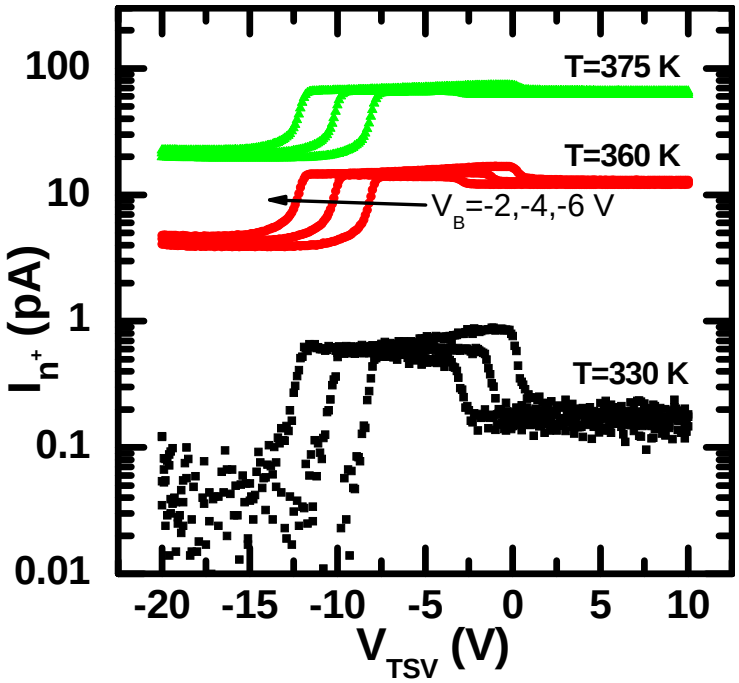


(b)

Fig. 3.1. (a) Method of measuring *p-n* diode in the TSV and the proposed guard ring and (b) *I-V* curves of two guard ring schemes.



(a)



(b)

Fig. 3.2. (a) Method of measuring gated-diode current and (b) gated-diode currents as a parameter of body bias (V_B) and temperature in the n^+/n guard ring.

3.3 C-V characteristics of the proposed guard ring

The proposed guard ring is composed of the TSV, the n^+/n region, and the *p*-substrate. Thus, these components collectively are similar to the 3-terminal MOS capacitor. Fig. 3.3 (a) shows the method to measure the *C-V* of the TSV and the guard ring where the n^+ region and *p*-substrate are grounded. Figs. 3.3 (b) and (c) show the measured and simulated *C-V* curves of two types of guard rings. The flat band voltage (V_{fb}) and the threshold voltage (V_{th}) of the n^+/n guard ring are about −11 V and –3.5 V, respectively. It is interesting to note that the V_{th} of the n^+ guard ring is over 15 V while keeping no change in V_{fb}. It is well known that V_{fb} is determined by the work-function difference (φ_{ms}) between the TSV metal and the substrate in Eq. (1) and changes by an equivalent oxide charge at the interface in Eq. (2).

$$V_{fb} = \varphi_{ms} = \varphi_m - \varphi_s \qquad (1)$$

$$\Delta V_{fb} = -\frac{Q_{ox}}{C_{ox}} \qquad (2)$$

where V_{fb} is the flat band voltage, φ_{ms} is the work-function difference between the TSV metal and the silicon substrate, φ_m is the work-function of the TSV, φ_s is the work-function of the *p*-substrate, Q_{ox} is the oxide charge at the interface between the TSV oxide and the *p*-substrate, and C_{ox} is the TSV oxide

capacitance.

Therefore both guard rings have nearly the same oxide charge and φ_{ms}. In this case, the V_{th} difference between the n^+/n guard ring and the n^+ guard ring in *C-V* curves is attributed to the halo doping (~10^{18} cm^{-3}). As mentioned above, the n^+ guard ring has the *p*-halo just under the n^+ region where the halo is butted to thick TSV oxide. Therefore, the halo is the main cause of higher V_{th} in the n^+ guard ring and separates electrically the n^+ region, and the inversion layer which cannot be formed at the surface of the *p*-substrate. However, the *n*-well in the n^+/n guard ring connects the n^+ region and the inversion layer. The φ_{ms} only cannot make V_{th} –3.5 V in the n^+/n guard ring formed in normal *p*-substrate. Therefore the interface trap and oxide charge should be considered.

As described in Chapter 2, the guard ring consists of shallow n^+ region in deep *n*-well butted to the TSV oxide in the *p*-doped active region. The structure of the guard ring with the TSV is similar to that of a three-terminal MOS capacitor with the TSV (gate), the n^+ region, and the *p*-substrate. The positive charge along the TSV interface is nearly 10 times larger than that in conventional MOSFET, as the via-hole etch and the subsequent oxide deposition steps generate a large interface charge. The V_{th} is expressed as Eq. (3), and the shift of the V_{th} is expressed as Eq. (4).

$$V_{th} = V_{fb} + 2\varphi_{fp} + \frac{\sqrt{4qN_a\varepsilon_s\varphi_{fp}}}{C_{ox}} \qquad (3)$$

where φ_{fp} is the difference between intrinsic fermi level and fermi level of a *p*-substrate, N_a is the acceptor doping concentration of a *p*-substrate, and ε_s is the permittivity of silicon.

$$\Delta V_{th} = -\frac{Q_{ox}}{C_{ox}} \qquad (4)$$

Substituting Eq. (4) into Eq. (3), the V_{th} is expressed as

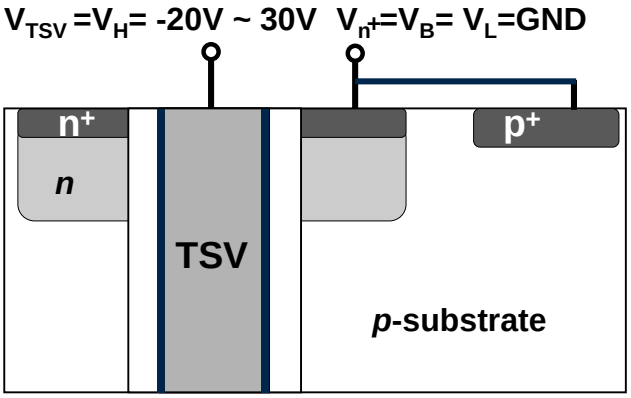
$$V_{th} = V_{fb} + 2\varphi_{fp} + \frac{\sqrt{4qN_a\varepsilon_s\varphi_{fp}} - Q_{ox}}{C_{ox}} \quad (5)$$

When the Q_{ox} is larger than the depletion charge in the *p*-substrate surrounding TSV (which means $\sqrt{4qN_a\varepsilon_s\varphi_{fp}} - Q_{ox} < 0$ in Eq. (5)), the V_{th} decreases to be negative value due to the Q_{ox}. The Q_{ox} will be extracted by simulation. Moreover, a thick TSV oxide means the small oxide capacitance of the TSV which is smaller than that of MOS transistor by ~100 times, which raises the contribution of the interface charge in the V_{fb} and the V_{th} of the MOS capacitor. As a result, the V_{fb} and the V_{th} of the TSV and the guard ring is shifted negatively when the n^+ region is grounded. An inversion layer can be formed on

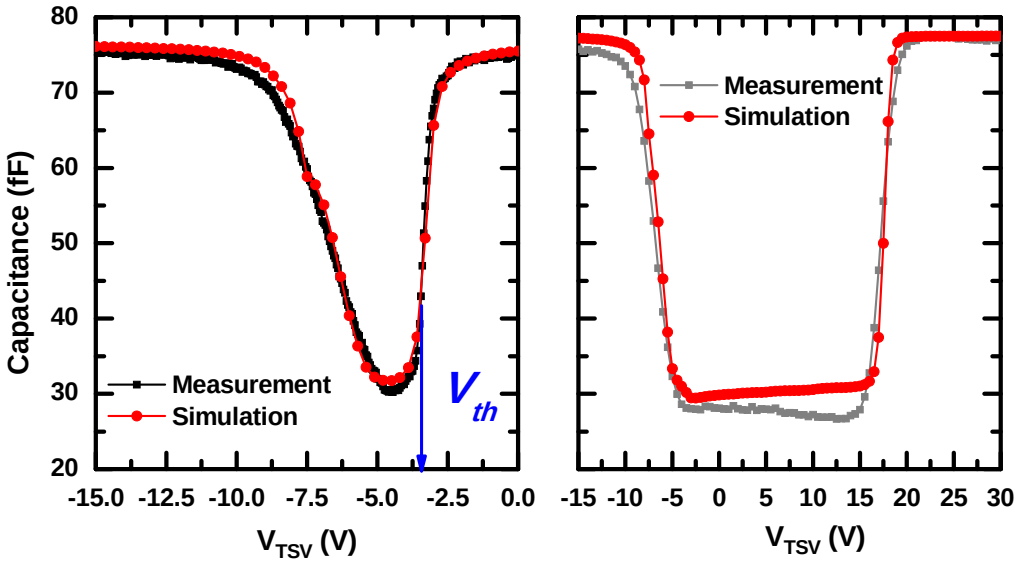
the silicon surface surrounding the TSV due to negative V_{th}, even when the TSV bias is 0 V. This inversion charge effectively suppresses the coupling noise.

The V_{fb} of the n^+ guard ring is about –11 V which is same as that of the n^+/n guard ring but the V_{th} is over 15 V in Fig. 3.3 (c). The *p*-type halo of the n^+ guard ring prevents the inversion charge supplied from n^+ region which is the main cause of higher V_{th} in the n^+ guard ring and the inversion charge from n^+ region cannot response the TSV bias.

Fig. 3.4 (a) shows the *C-V* curves of the n^+/n guard ring with an acceptor-like trap density near 0.7 eV from valence band. In our work, a peak density of 7×10^{11} cm^{-2} eV^{-1} gives the best fitting to the *C-V* curve near V_{th}. The slope near V_{fb} is determined by donor-like traps, and the measured *C-V* curve is well fitted using the donor-like trap profile, as shown in Fig. 3.5 (e). Fig. 3.4 (b) shows the *C-V* curves with oxide charge (Q_{ox}) at the interface between the *p*-substrate and the TSV oxide. As the Q_{ox} increases, the V_{fb} and V_{th} decrease sensitively because of thick TSV oxide. A Q_{ox} of 3.8×10^{11} cm^{-2} gives the best fitting in this work. With the same Q_{ox} and the interface trap density (D_{it}) in both guard rings, simulated *C-V* curves are well matched with measured data (Fig. 3.3). To confirm the D_{it} extracted by simulation, the D_{it} is extracted by using the conductance method [20] and the charge pumping method [21]. Figs. 3.5 (a) – (d) show the conductance loss (G/ω) for different temperatures (T), and Fig. 3.5 (e) shows that the extracted D_{it} profiles are similar to the simulated result.

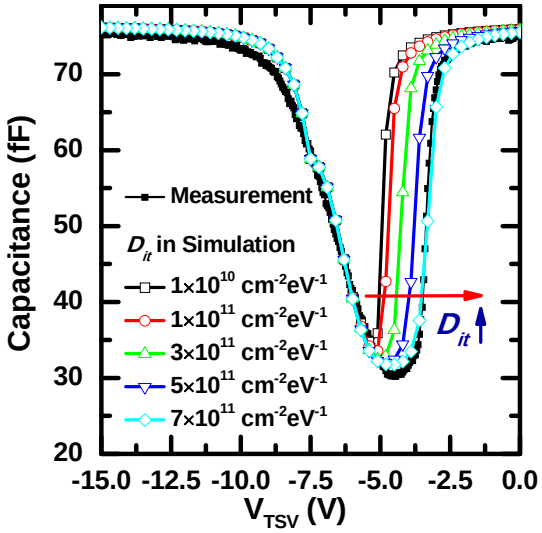


(a)

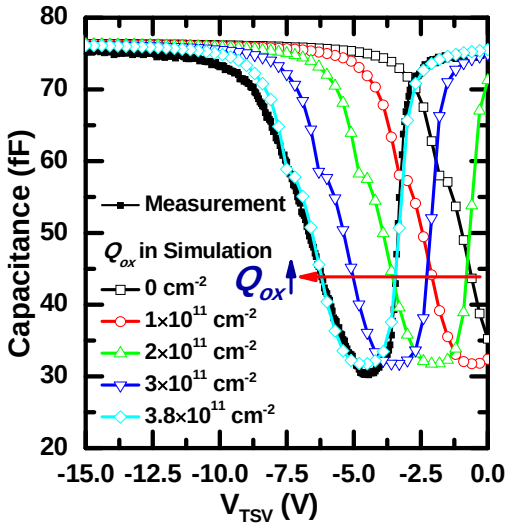


(b) (c)

Fig. 3.3. (a) Method of measuring *C-V* curves of the TSV and the guard ring. Measured and simulated *C-V* curves of (b) n^+/n guard ring and (c) n^+ guard ring.



(a)



(b)

Fig. 3.4. Simulated *C-V* curves of the n^+/n guard ring with a peak acceptor-like trap density (a) and with oxide charge at the TSV interface (b).

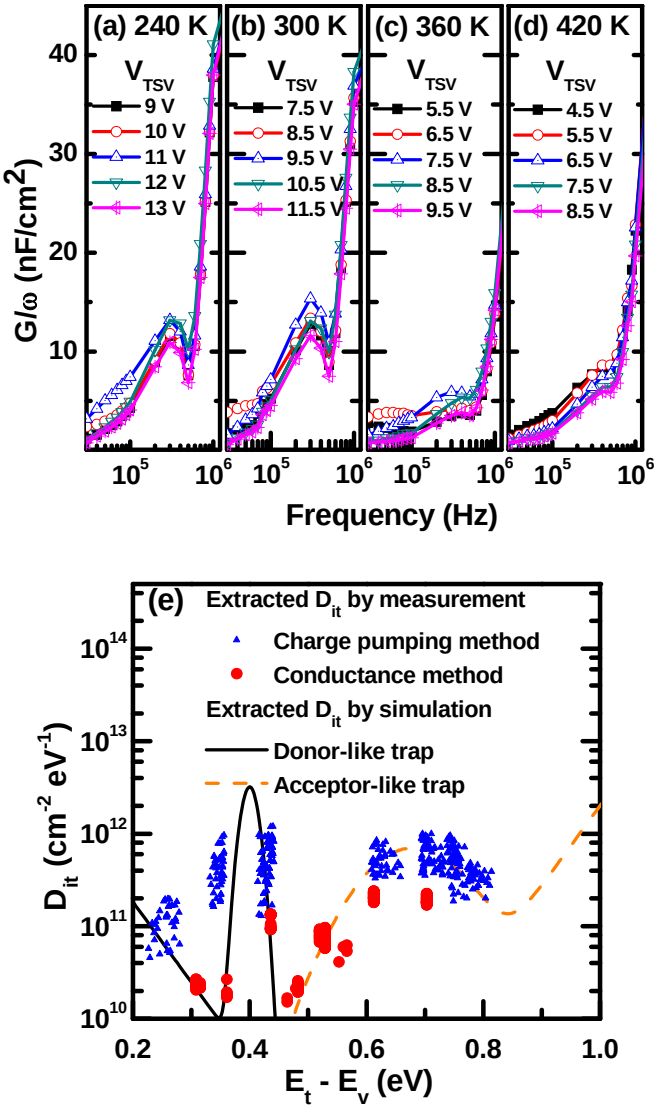


Fig. 3.5. G/ω of the TSV capacitor for different temperatures. (a) 240 K, (b) 300 K, (c) 360 K, and (d) 420 K. (e) Comparison of the interface trap density extracted by measurement and simulation.

Since a thick TSV oxide enhances the contribution of the interface charge in the V_{fb}, the V_{th} of the TSV capacitor is shifted negatively when the n^+ region is grounded. An inversion layer can be formed on the silicon surface surrounding the TSV due to negative V_{th}, as shown in Fig. 3.6, even when the TSV bias is 0 V. The inversion charge effectively suppresses the coupling noise from the TSV electrode.

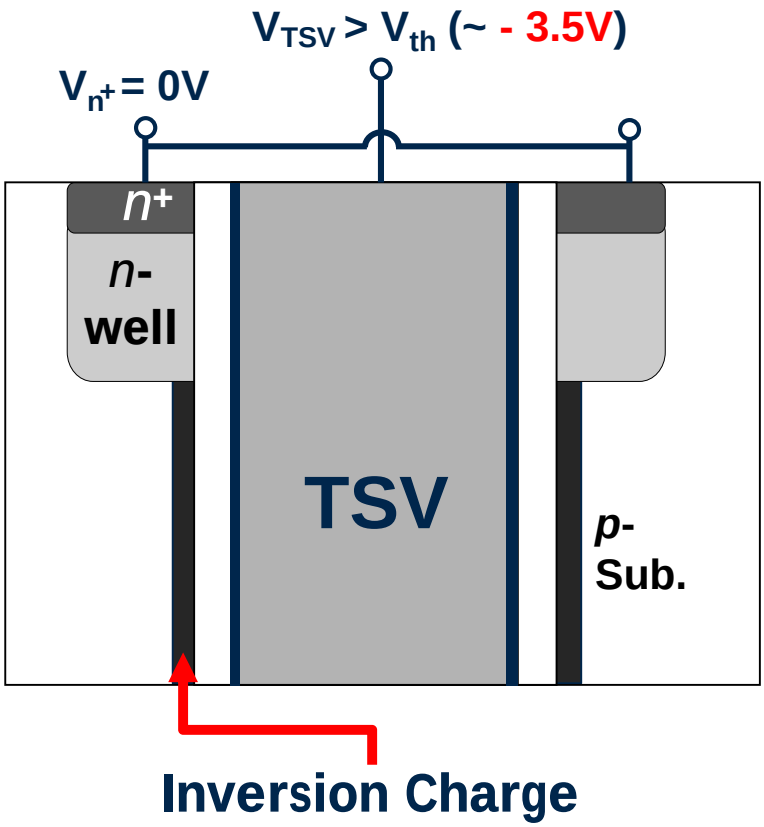


Fig. 3.6. Operation of the proposed guard ring to suppress the coupling noise by the inversion charge surrounding the TSV oxide when the TSV bias is applied over the threshold voltage of the TSV capacitor.

Chapter 4

Effective method to analyze the trap density

4.1 Introduction

The TSV has been considered as a key technology in the 3-D packaging, overcoming the limitation of 2-D planar architecture with regard to integration density. Because the TSV is the path for high-frequency signal and power line, highly conductive material is necessary to ensure that the operation speed and the power consumption are not degraded. Cu has commonly been used as a TSV electrode due to its high conductivity, but it has a high diffusivity even at low temperatures, which results in trap generation in peripheral devices [13]. Thus, electrical characterization of the effect of Cu diffusion must be performed. Although a transient capacitance (*C*-*t*) method has been reported [17], it is limited in its ability to profile traps and to identify the surface and bulk traps. In this chapter, we propose a new test method that provides a very efficient and

precise analysis of the trap profile, and verify its effectiveness experimentally. To characterize electrically the effect of Cu diffusion in TSV, the analysis with the proposed guard ring of n^+/n-well is proposed. We can measure the diode and gated diode currents, the charge pumping current, and *C*-*V* to accurately analyze the effect. Our approach is demonstrated to be very useful by investigating the effect of Cu diffusion in samples with two different barrier metal thicknesses.

4.2 Characteristics of Cu diffusion with barrier metal thickness

The test samples are prepared with a layer of tantalum (Ta) as a barrier metal which is formed with two different thicknesses of 35 nm and 100 nm and process flow is shown in Fig. 4.1. Fig. 4.2 shows the *I-V* curves of the *p-n* diode measured from the test pattern for different values of the barrier metal thickness (t_{barr}). The diodes exhibit excellent *I-V* property, which guarantees that no problems occur in device fabrication. Fig. 4.3 shows the gated-diode current (I_{n+}) versus TSV bias (V_{TSV}) for different body bias (V_B) at 360K. The TSV and the guard ring become a gated-diode where the I_{n+} is composed of the generation current components at the TSV interface and in depletion region. The gated-diode with t_{barr} = 35 nm (sample A) shows a larger I_{n+} than that of the device with t_{barr} = 100 nm (sample B), which means that Cu penetration in the sample A is appreciable during the heat cycle after TSV formation. This result cannot be achieved using the reported method [17]. In Fig. 4.4, MOS *C-V* curves are measured and simulated from samples A and B that have a MOS consisting of the TSV electrode, oxide, and *p*-substrate when the n^+ region and body are grounded. The simulated *C-V* curves show good agreement with the measured *C-V* curves, as shown in Fig. 4.4, by optimizing the trap profile, as shown in Figs. 4.5 and 4.6. The V_{th} is less than –3 V due to the interface trap generated by RIE and CVD process for the TSV oxide. The sample A shows a distortion around

the V_{fb} due to generated traps. To understand the traps responsible for the *C-V* curves, we investigate the behavior of the acceptor-like trap and donor-like trap at the interface. As shown in Fig. 4.5, the V_{th} rises with increasing acceptor-like trap density. In Fig. 4.6, the distortion of the *C-V* curve near V_{fb} is attributed to the donor-like trap at $E_t - E_v$ of 0.41 eV. To confirm the trap density (D_{it}) obtained by simulation, the D_{it} is extracted using the conductance method. Fig. 4.7 shows that the D_{it} extracted by the simulation (lines) and measurement (symbols), respectively. Although the D_{it} profiles extracted from the samples A and B are limited in energy, reasonable agreement is found between the simulation and measurement. Figs. 4.8 (a) and (b) show the method of measuring charge pumping current in the TSV with n^+/n region and pulse waveform for charge pumping, respectively. Figs. 4.9 (a) and (b) show the charge pumping current (I_{cp}) versus rising time (t_r) with the peak voltage of TSV (V_{peak}) and the base voltage of TSV (V_{base}), respectively. As V_{peak} becomes larger than V_{th}, I_{cp} increases significantly. From the data in Figs. 4.4 and 4.9 (a), the V_{th} of sample A are approximately –3.5 V. Similarly, V_{fb} is extracted to be approximately –11 V from the data in Fig. 4.9 (b). Sample A shows higher I_{cp} versus V_{base} than that of sample B, as shown in Fig. 4.10. The results of the sample A (thinner t_{barr}) is now understood as evidence of appreciable Cu diffusion which results in the trap generation at the TSV interface and the silicon body.

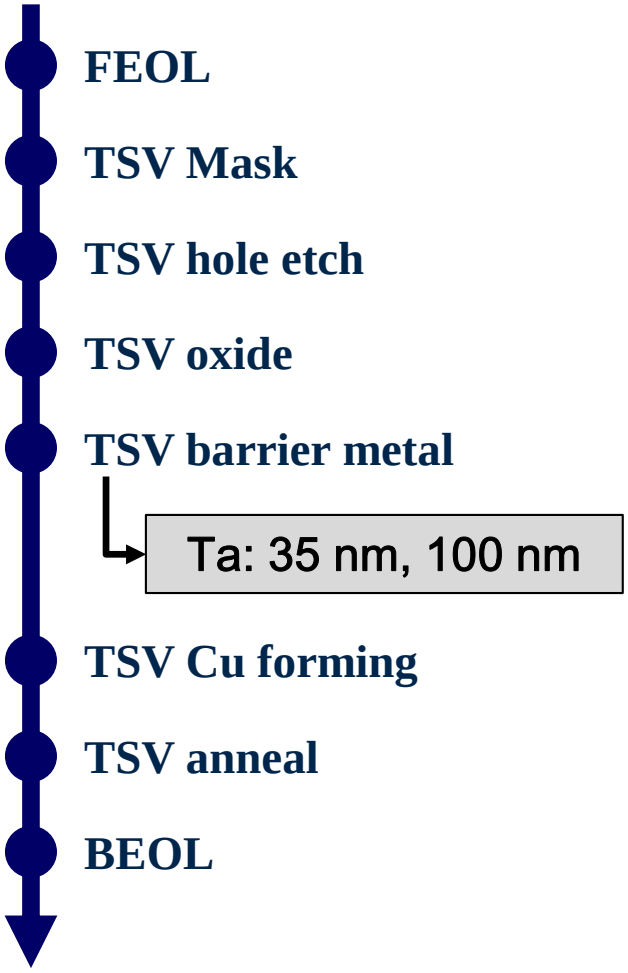
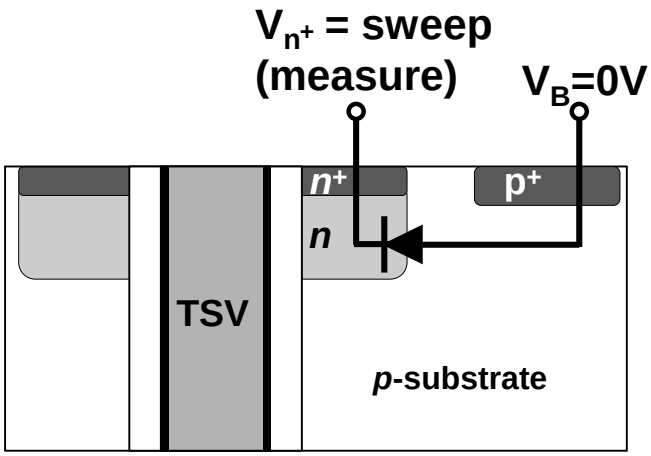
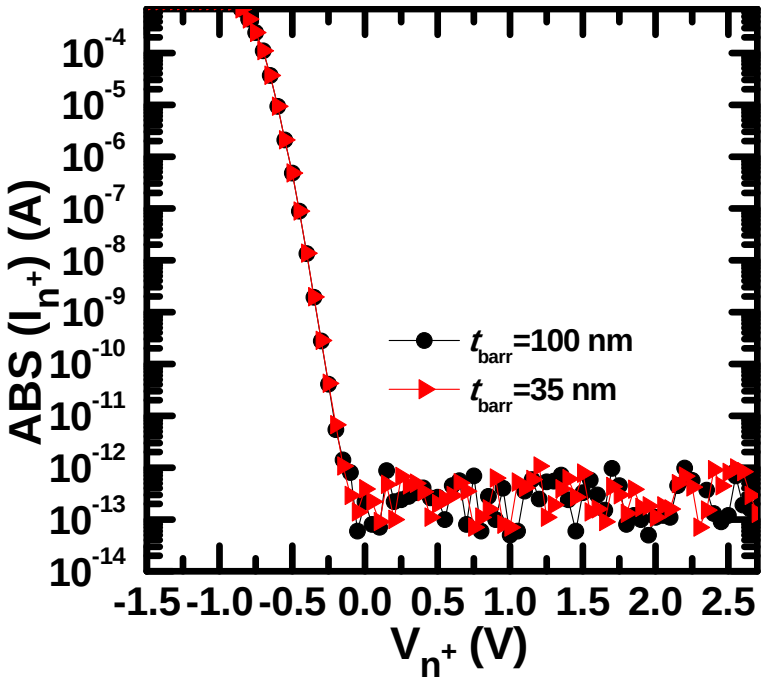


Fig. 4.1. Fabrication flow of test wafers for different barrier metal thickness with TSVs. The thicknesses of the tantalum (Ta) barrier metal (t_{barr}) surrounding the TSV metal are 35 nm and 100 nm.

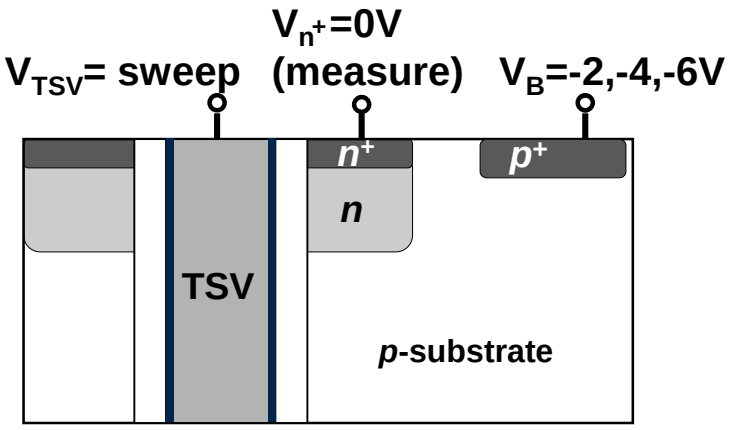


(a)

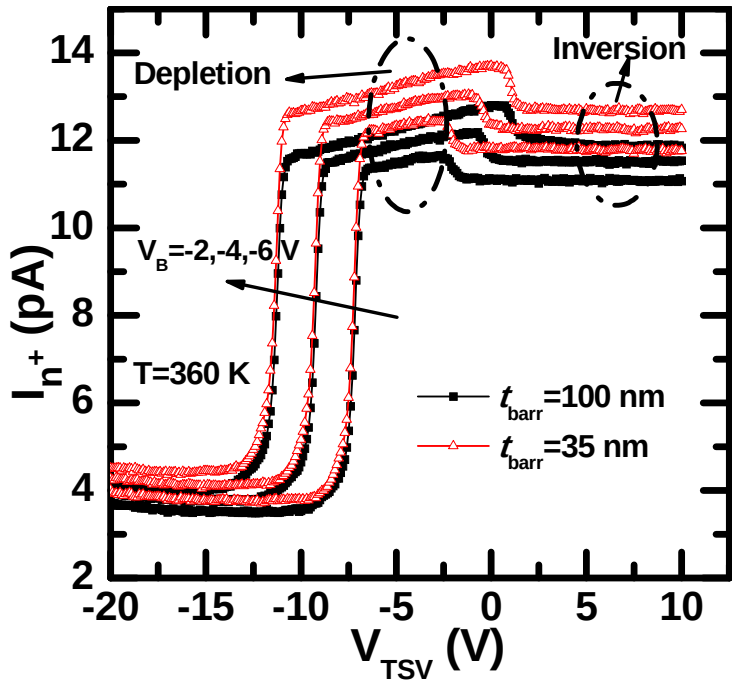


(b)

Fig. 4.2. (a) Method of measuring *p*-*n* junction diode consisting of the n^+/n region and *p*-substrate and (b) *I*-*V* curves of the *p*-*n* junction diode with the t_{barr}.



(a)



(b)

Fig. 4.3. (a) Method of measuring gated-diode current and (b) gated-diode currents of the test pattern versus V_{TSV} as a parameter body bias (V_B) with t_{barr}.

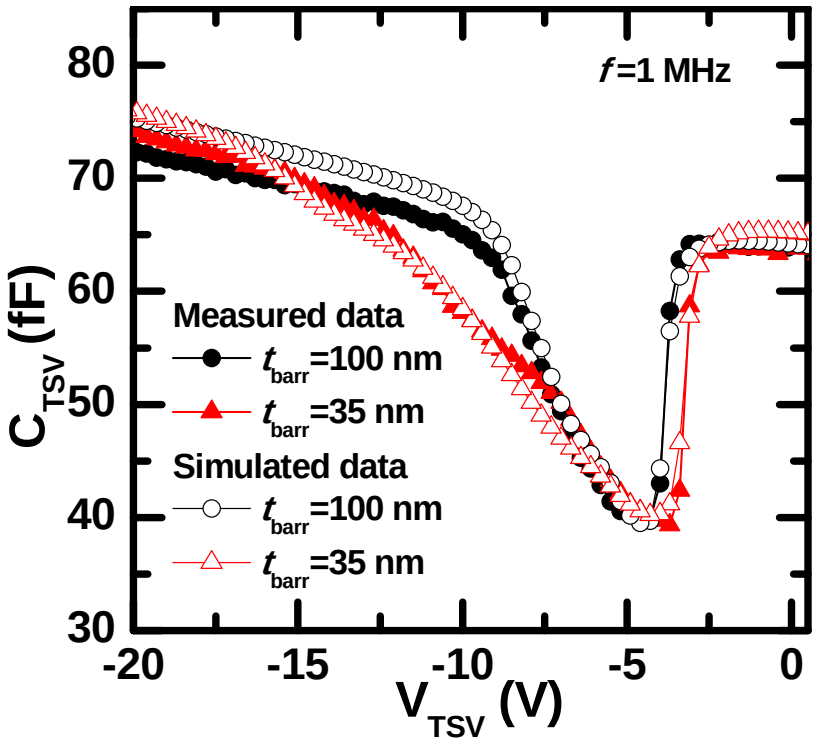
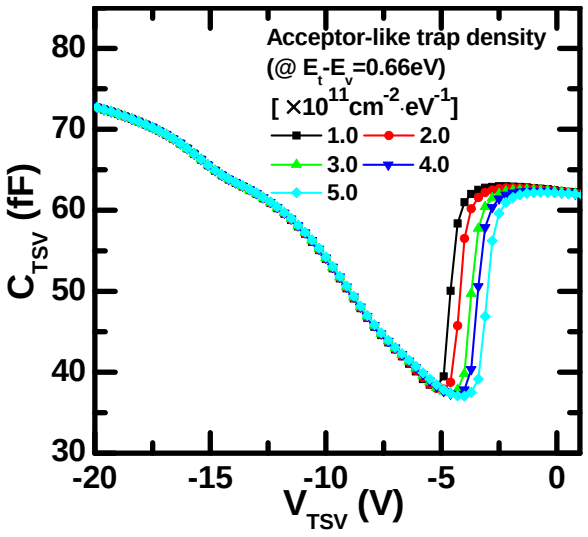
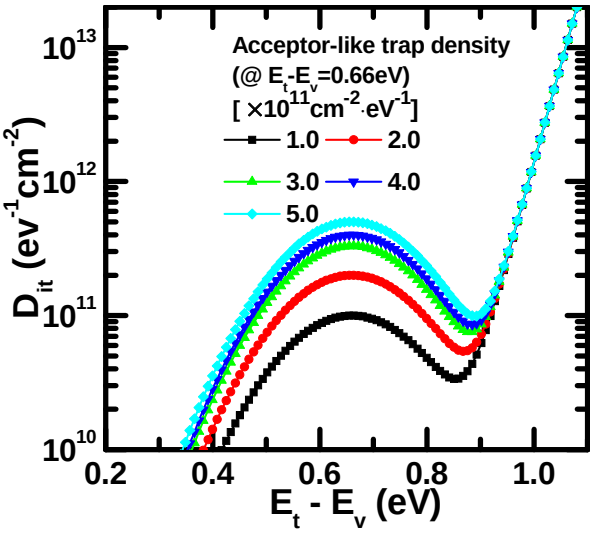


Fig. 4.4. Measured and simulated *C-V* curves of the TSV with t_{barr} when the n^+/n region and *p*-substrate are grounded.

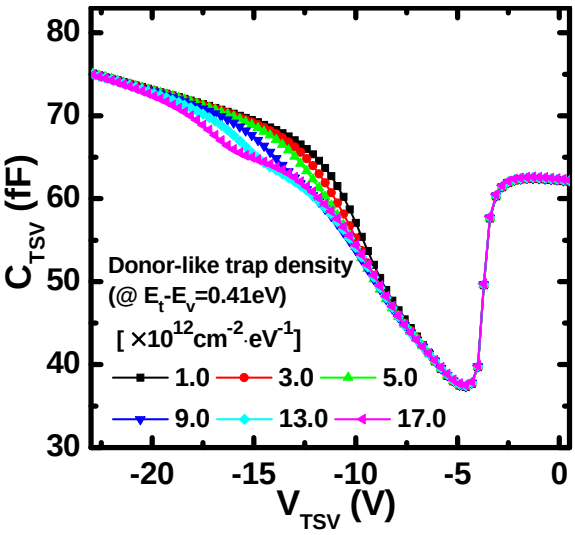


(a)

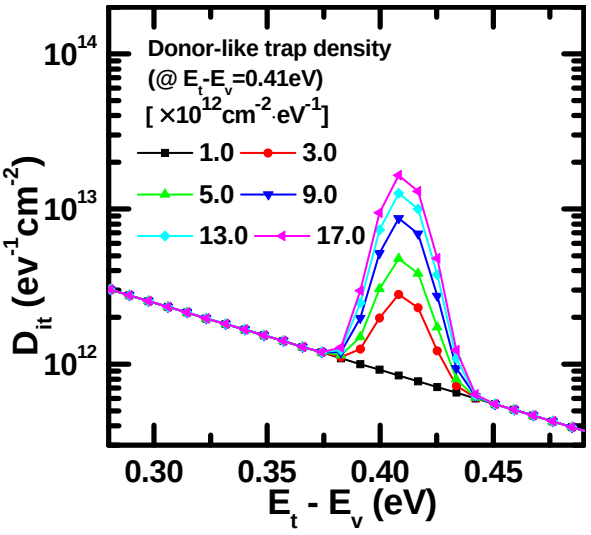


(b)

Fig. 4.5. Simulated *C-V* curves of the test patterns with the acceptor-like trap density (a) and corresponding trap profiles (b).



(a)



(b)

Fig. 4.6. Simulated *C-V* curves of the test patterns with the donor-like trap density (a) and corresponding trap profiles (b).

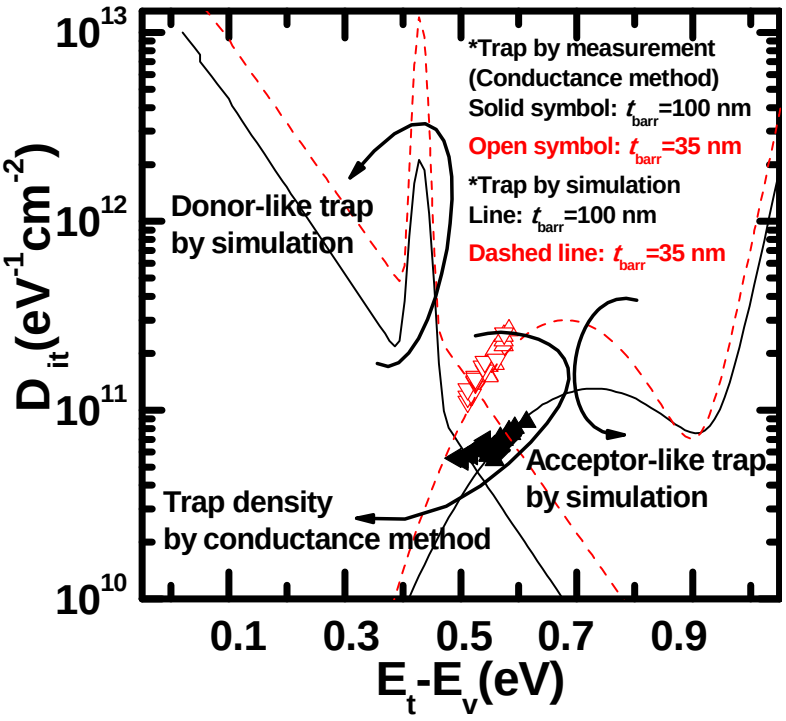
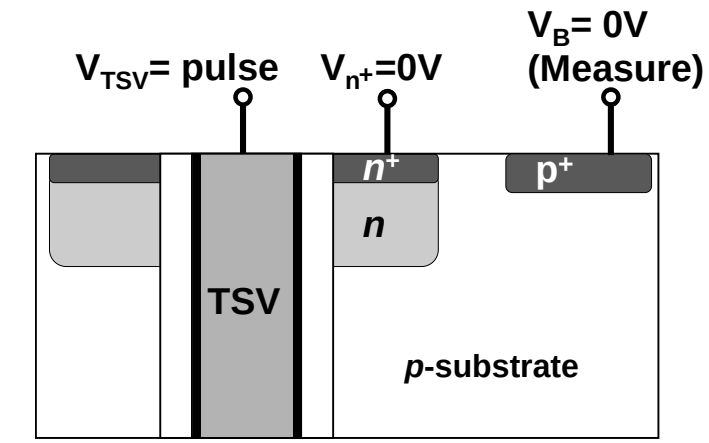
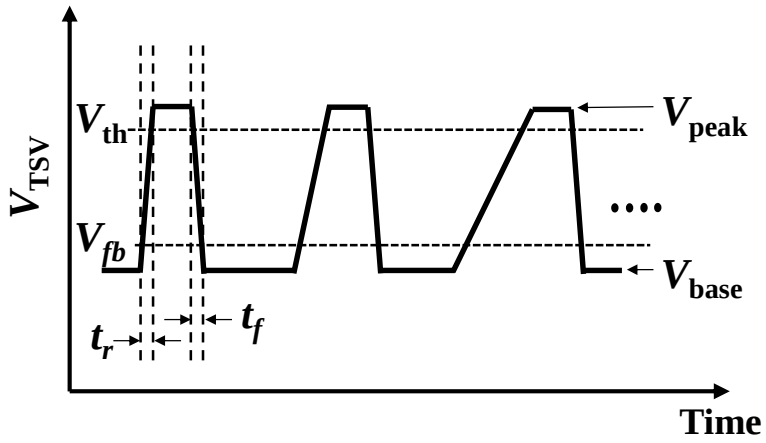


Fig. 4.7. Trap density extracted by the conductance method (symbols) and simulation (solid and dashed lines).



(a)



(b)

Fig. 4.8. (a) Method of measuring charge pumping current in the TSV with the n^+/n region and (b) the pulse waveform for charge pumping.

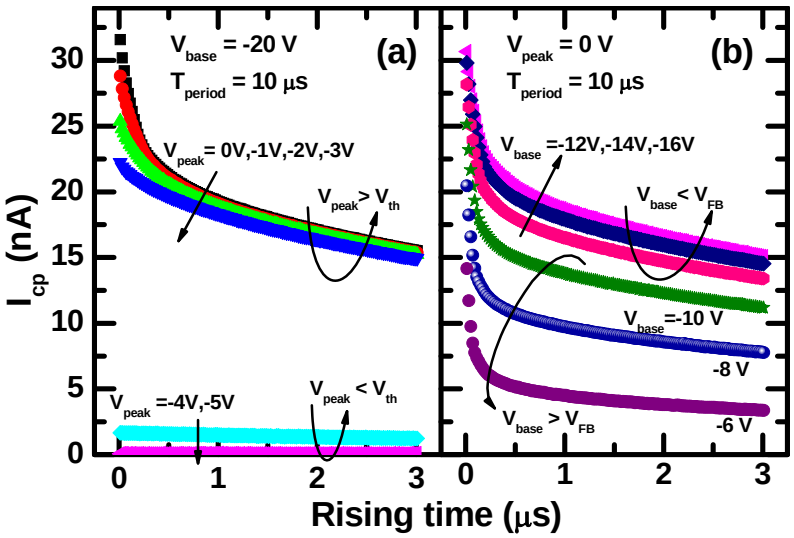


Fig. 4.9. Charge pumping current (I_{cp}) versus rising time (t_r) for different V_{peak} (a) and V_{base} (b).

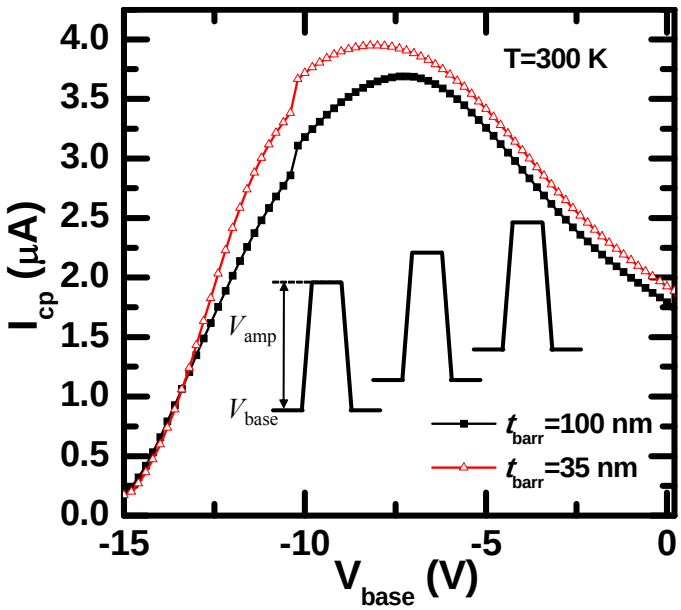


Fig. 4.10. I_{cp} versus V_{base} for different t_{barr} at V_{amp}=10 V and f=20 MHz.

4.3 Effect of Cu diffusion enhanced by additional annealing

We investigate the effect of Cu diffusion with an additional annealing step. Fig. 4.11 shows the transient capacitance (*C*-*t*) curves of samples A and B before and after annealing (400 °C for 4 hours). The *C*-*t* curves are plotted as a function of a normalized C/C_f versus a measuring time where C is a measured capacitance at high frequency in the deep depletion condition and C_f is a steady state capacitance in the inversion condition. The C/C_f of sample A before annealing increases slower, but increases faster after ~30 sec than that of sample B, and consequently saturates faster than that of sample B. However, the difference of C/C_f between samples A and B is not significant before annealing. The C/C_f of sample A after annealing increases clearly and reaches the saturation value faster than that of sample B. Fig. 4.12 compares the I_{cp} versus V_{base} curves of samples A and B before and after annealing (400 °C for 4 hours). The value of I_{cp} increases clearly after the annealing step. The results of *C*-*t* and I_{cp} after annealing are the evidence that Cu atoms diffuse easily through thin barrier metal and generate the trap density after annealing.

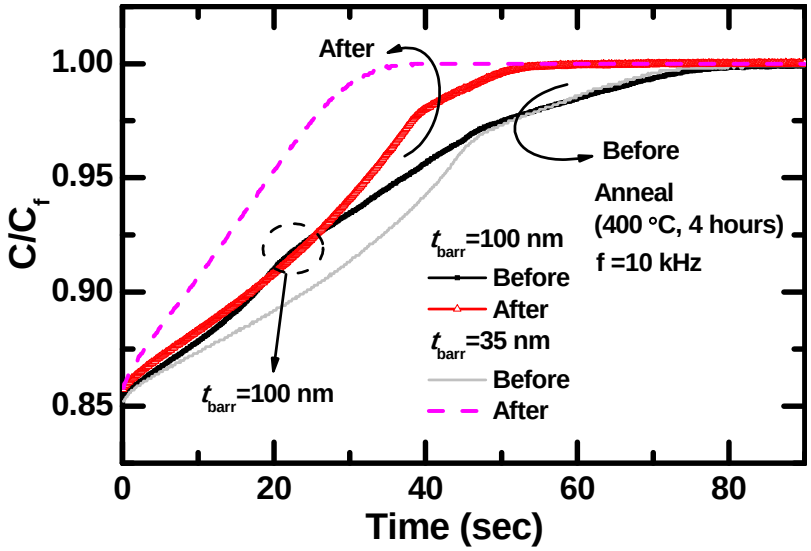


Fig. 4.11. Capacitance ratio (C/C_f) by transient capacitance (C-t) for different t_{barr} before and after annealing.

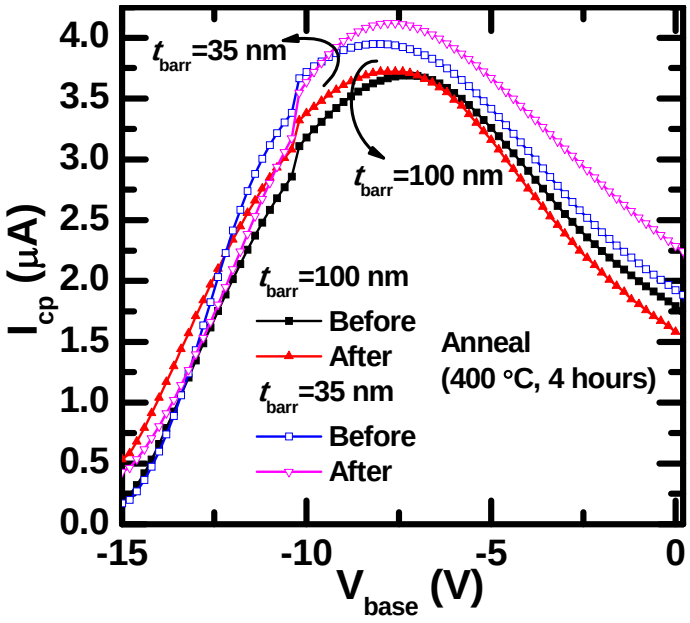


Fig. 4.12. I_{cp} versus V_{base} for different t_{barr} before and after annealing.

The gated-diode currents (I_{n+}) versus V_{TSV} curves of samples A and B with annealing are shown in Fig. 4.13 as a parameter of V_B. The peak I_{n+} of sample A is larger than that of sample B by 4.3 % before annealing, as shown in Fig. 4.13 (a), but increases up to 40 % after annealing (400 °C for 4 hours), as shown in Fig. 4.13 (b). By comparing the results before and after annealing, we understand that the increase of I_{n+} is more significant at the interface than in the depletion region because the value of I_{n+} in the inversion exhibits a smaller difference before and after the annealing. The increase of I_{n+} in the depletion region with V_B in Fig. 4.13 (b) can be explained by the increase of the depletion width in the *p*-substrate with increasing $|V_B|$, as shown in Fig. 4.14 (a). Fig. 4.14 (b) shows the activation energy (E_a) extracted from the Arrhenius equation based on the peak I_{n+} in the depletion with temperature. The difference of E_a (ΔE_a) between samples A and B is approximately 0.04 eV before annealing, and increases to 0.12 eV after annealing due to the more significant Cu diffusion in sample A. Fig. 4.15 (a) shows the schematic cross section of a virtual diode consisting of the n^+/n-well/inversion and *p*-substrate at $V_{TSV} = 0$ V. The inversion layer is formed at the interface because the V_{th} is less than –3 V. Figs. 4.15 (b) and (c) show the measured *I-V* curves of the diodes as a parameter of V_B for samples B and A, respectively. The diode in sample A shows significantly increased reverse current and degraded forward current after annealing (500 °C for 1 hour). The ideality factor (*n*) in sample A increases from 1.14 to 2.06 with

the annealing step because more traps are generated due to the increased Cu diffusion.

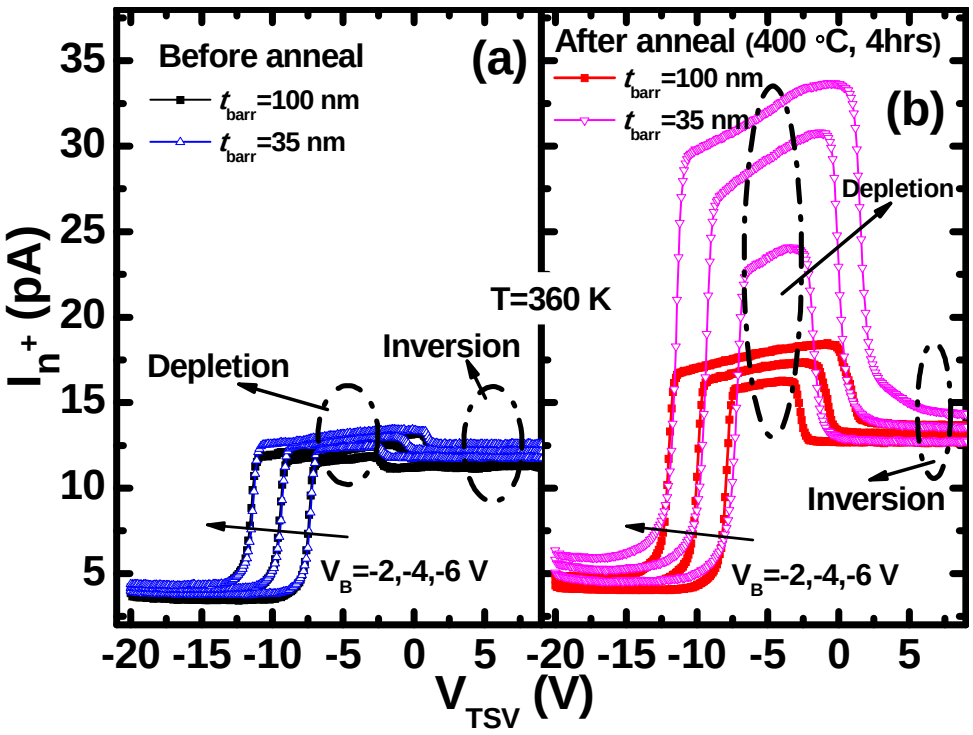
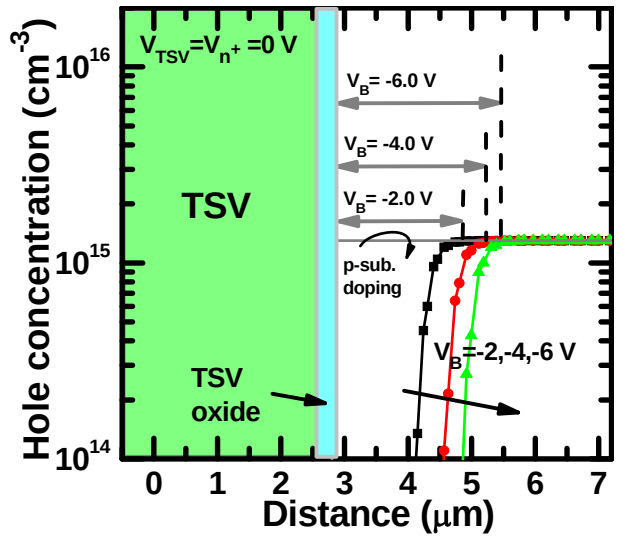
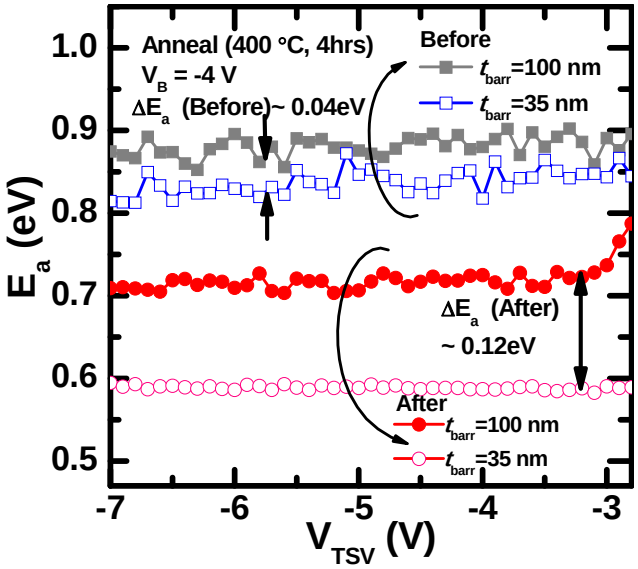


Fig. 4.13. Gated-diode currents measured at 360 K for different t_{barr} and body bias before (a) and after (b) annealing (400 °C for 4 hours).

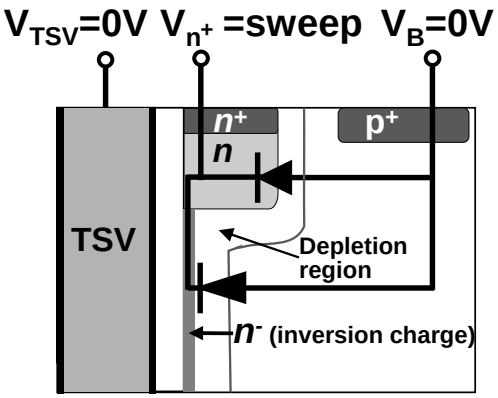


(a)



(b)

Fig. 4.14. (a) Simulated hole concentrations to see the depletion region width with the body bias when V_{TSV} and V_{n+} are 0 V and (b) activation energies obtained from the gated-diode before and after annealing.



$$I = I_0(e^{\frac{V}{nk_BT}} - 1)$$

$$n: ideality\ factor$$

(a)

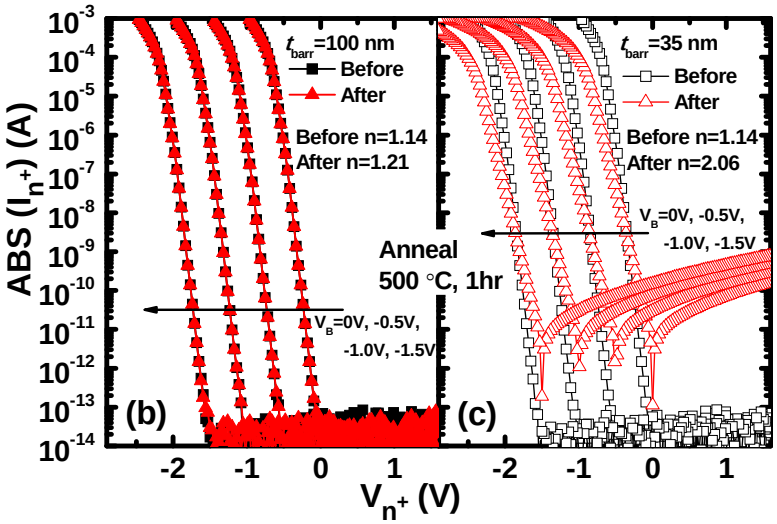


Fig. 4.15. Cross section of the test pattern for virtual diode current (a) and *I-V* curves of the test pattern having the t_{barr}s values of 100 nm (b) and 35 nm (c) as parameters of body bias and annealing (500 °C for 1 hour).

We investigate the effect of Cu diffusion on a victim nMOSFET at a distance 5 μm away from the TSV, as shown in Fig. 4.16. Figs. 4.17 (a) and (b) show the I_D-V_G curves of the victim and normal nMOSFET in samples A and B, respectively. The normal nMOSFET is a distance of ~ 2000 μm from the TSV, consequently it is not affected by Cu diffusion. After annealing at 500 °C for 1 hour, sample B shows a negligible change between the victim and the normal devices. However, we observed a very significant change in the subthreshold current of the victim device of sample A (see solid circles in Fig. 4.17 (b)). To identify the origin of such leakage, the terminal currents of the victim device in the sample A are plotted in Fig. 4.18. The drain current (I_D) is the same as the source current (I_S) in the subthreshold region, as shown in Fig. 4.18 (a). Although the body current (I_B) of sample A increases by ~100 times than that of sample B, as shown in Fig. 4.18 (b), the I_B is too small to increase I_D, which means there is a strong leakage path between the source and drain due to Cu diffusion. Fig. 4.19 shows the normalized noise spectral density (S_{id}/i_d^2) measured from the victim devices before and after annealing (500 °C for 1 hour) where i_d is the drain current of the victim nMOSFET when V_G= 0.6 V, V_D= 0.1 V, and V_B= 0.0 V. After the annealing, samples A and B show increased S_{id}/i_d^2, and the increase is more significant in the device of sample A.

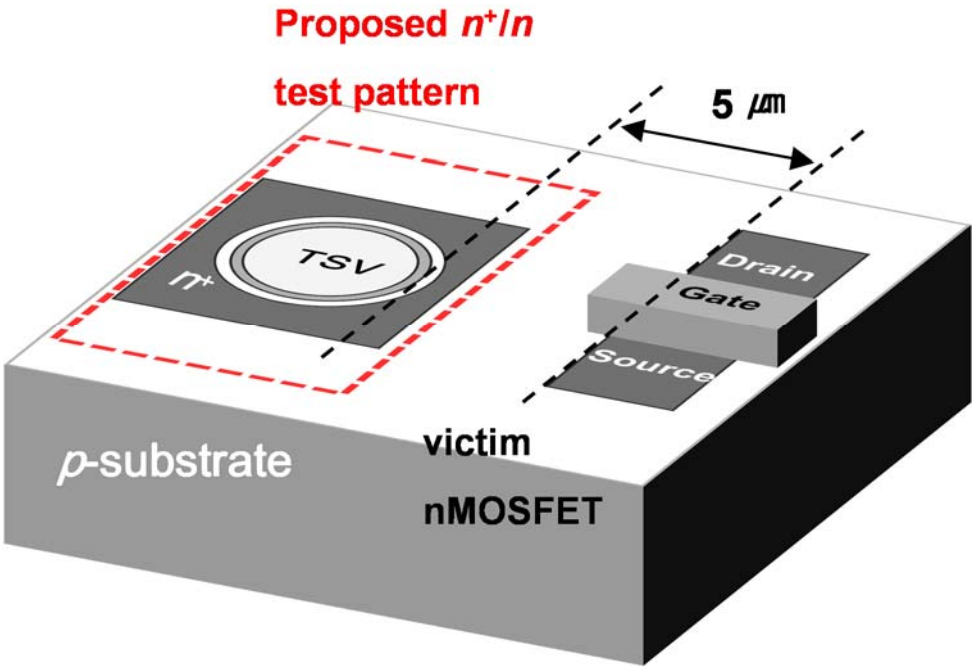


Fig. 4.16. Schematic view of TSV test pattern and a victim nMOSFET (W/L=10 μm / 50 nm). The distance between the TSV and the nMOSFET is 5 μm.

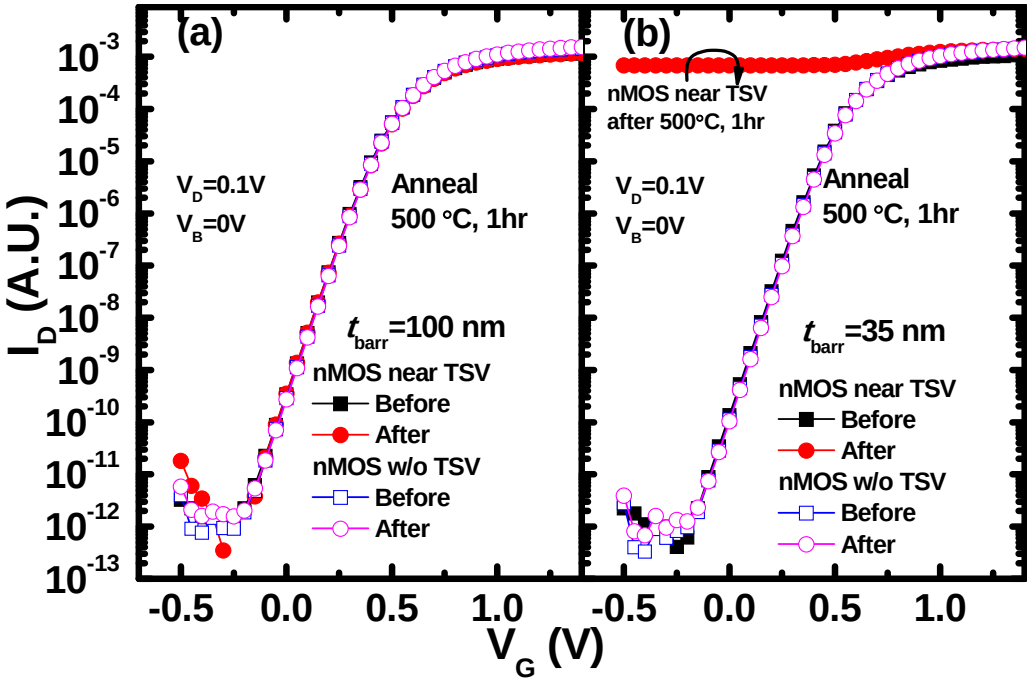


Fig. 4.17 I_D-V_G curves of victim and normal nMOSFETs for (a) t_{barr} = 100 nm and (b) t_{barr} = 35nm as a parameter of annealing (500 °C for 1 hour). The normal nMOSFET is located far away from the TSV.

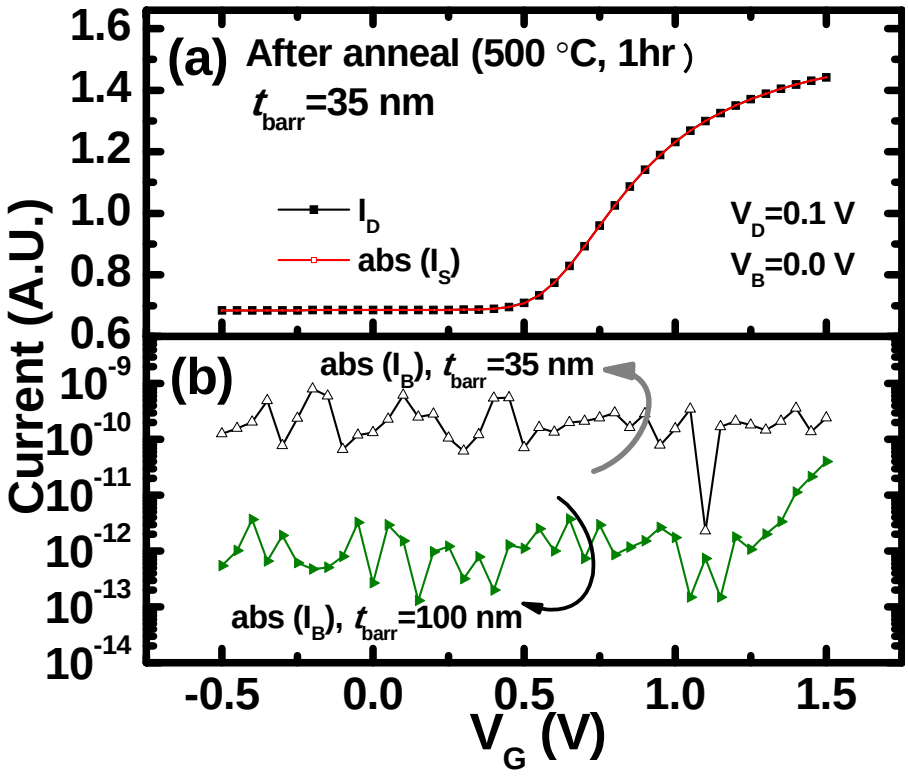


Fig. 4.18. I_D and I_S of victim nMOSFET with a t_{barr} of 35 nm (a) and I_B versus V_G curves of a victim device for different t_{barr} values (b) after annealing (500 °C for 1 hour).

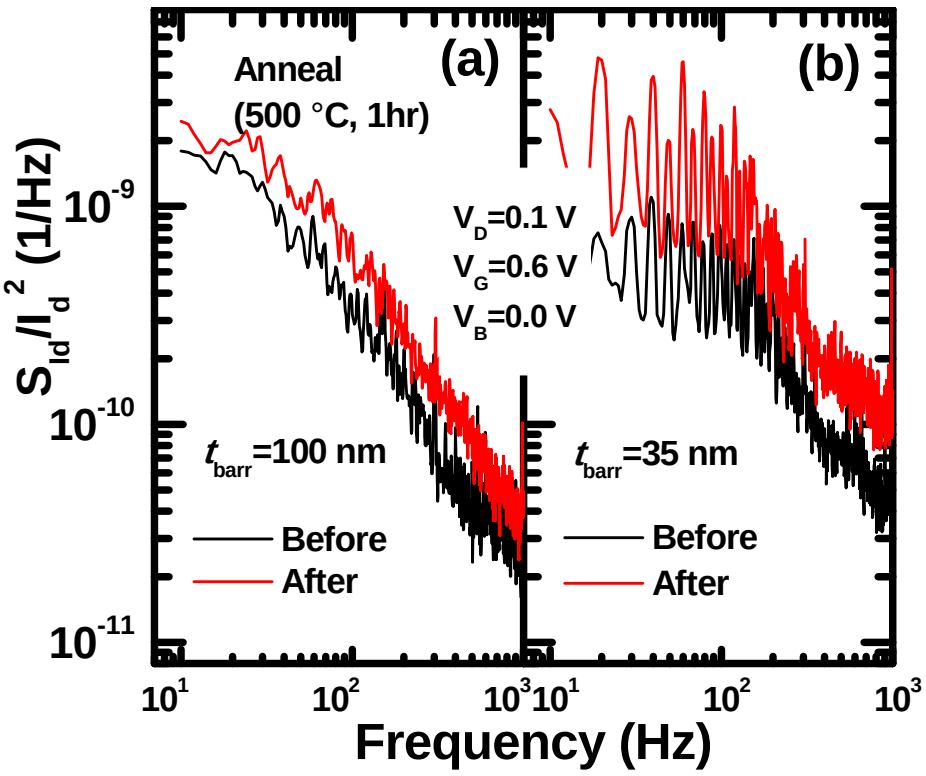


Fig. 4.19. Normalized noise power spectral density (S_{id}/i_d^2) of victim nMOSFET for (a) t_{barr} = 100 nm and (b) t_{barr} = 35nm before and after annealing (500℃ for 1 hour).

Chapter 5

Shielding ability of the proposed guard ring

5.1 Introduction

The proposed guard ring is composed of a *p*-substrate, a shallow n^+ and deep *n*-well region, and a TSV. The TSV and the guard ring collectively are similar to a three-terminal MOS capacitor, and an inversion charge is induced along the TSV interface when the bias of the TSV is applied at even 0 V due to the positive oxide charge and the small TSV oxide capacitance. The TSV is the path of the high-frequency signal, and the coupling noise is induced by the TSV pulse. Therefore, the guard ring is necessary to suppress the coupling noise. Two types of guard rings have been developed. The first is a metal type of guard rings such as a coaxial-type [18], as shown in Fig. 5.1, and an additional grounded TSV [15], as shown in Fig. 5.2. The metal guard ring is very effective when used to shield against the coupling noise, but its fabrication process is very

complicated, and it must occupy a large area for effective shielding [22]. The second is a dopant type of guard ring [15]. When the p^+ guard ring near the TSV is grounded, the coupling noise is reduced because the potential of the *p*-substrate is grounded. It is simple to create the p^+ guard ring by modifying the ion implantation mask, but its shielding ability cannot suppress the coupling noise induced by the TSV sufficiently. We evaluate the shielding ability of the proposed guard ring by measurements and a simulation. The current fluctuation of a victim nMOSFET is measured and analyzed in the simulation. The drain current fluctuation is evaluated with respect to the TSV pulse. The keep-out zone (KOZ) is extracted by the simulation with the distance between the TSV and the victim nMOSFET and the response of the guard ring at a high frequency is analyzed.

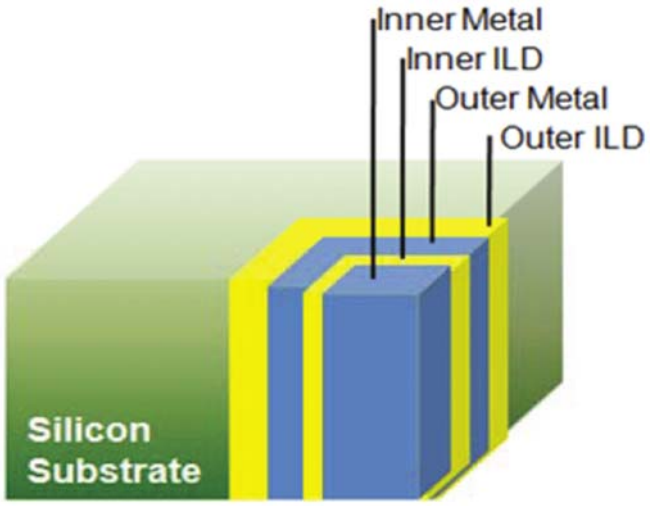


Fig. 5.1. Cross-section view of schematic illustration of a metal coaxial TSV in a Si substrate [18].

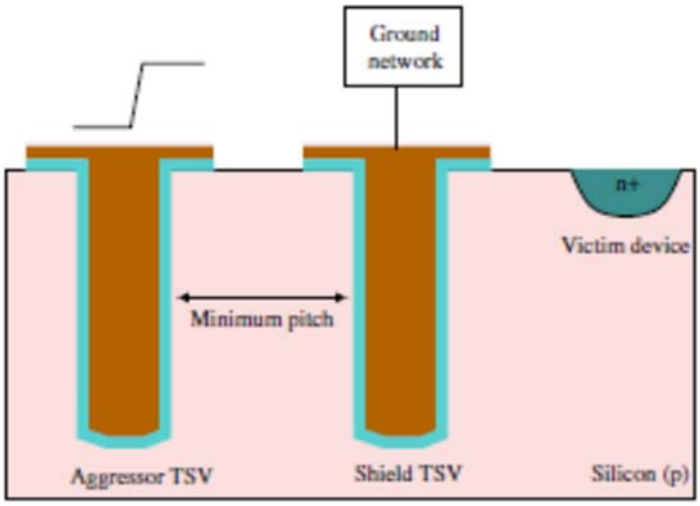


Fig. 5.2. A shield TSV connected to a ground network near an aggressor TSV to alleviate noise coupling [15].

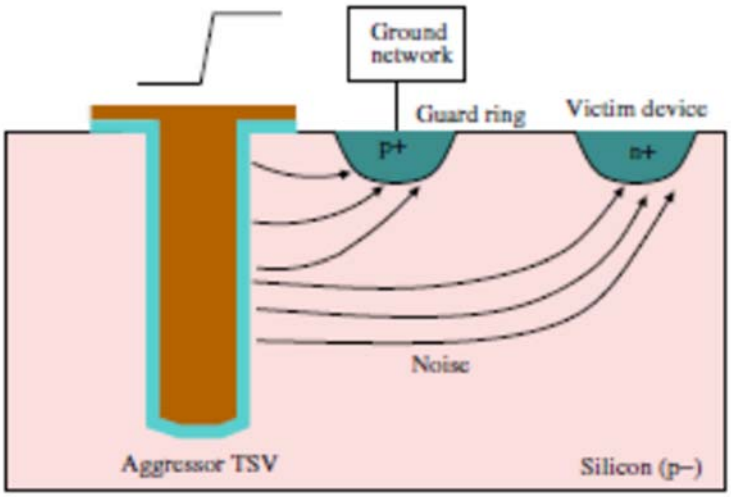


Fig. 5.3. P^+ dopant type of a guard ring near the aggressor TSV to alleviate noise coupling [15].

5.2 Shielding ability of the proposed guard ring

To confirm the shielding effect, Fig. 5.4 shows the n^+/n guard ring and the test pattern to verify the reduction of the coupling noise and describes the operating condition of the victim nMOSFET. D_G is the distance between the TSV and the victim nMOSFET. The TSV and the victim nMOSFET are connected by the capacitance and resistance, as shown in Fig. 5.4. To investigate the effect of TSV on the victim nMOSFET, the victim nMOSFET works in steady state mode. While the victim nMOSFET operates, the periodic pulse is applied to the TSV electrode. The transient drain current (I_D) of the victim nMOSFET is measured immediately after applying a step pulse (V_{TSV}) to the TSV electrode. The guard ring (V_{GR}) and substrate contact (V_{sub}) were grounded during the measurement and the simulation.

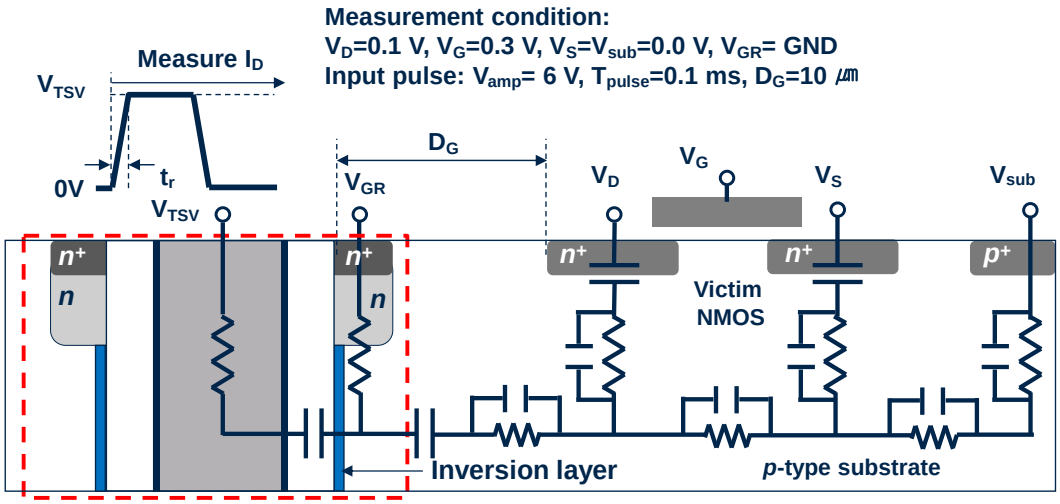
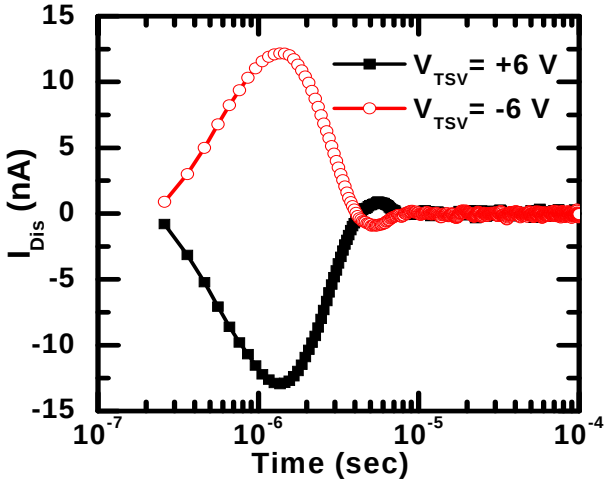
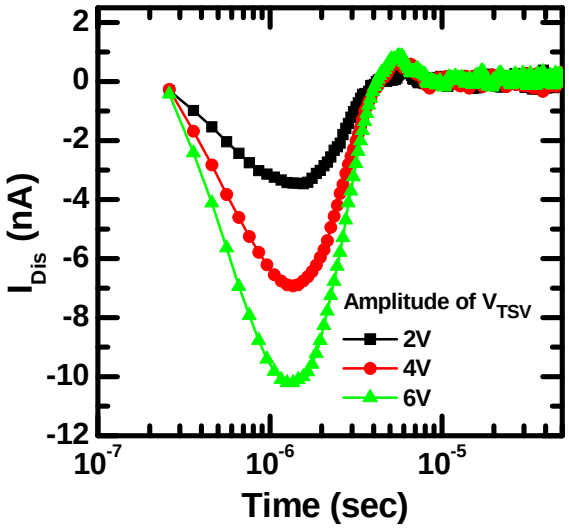


Fig. 5.4. Schematic of the TSV test pattern and the proposed (n^+/n) guard ring (in the dashed box) for measuring shielding ability of the proposed guard ring. A victim nMOSFET was used to estimate the shielding ability of the guard ring. Test condition is described to measure the shielding effect.

Fig. 5.5 shows the I_D behavior in time with the polarity and the amplitude of V_{TSV} where D_G is 10 μm. A displacement current of the drain (I_{Dis}) was measured at the victim nMOSFET with the n^+/n guard ring while the V_{TSV} rises. The smaller I_{Dis} means the better shielding ability. The V_{TSV} is positive, the I_{Dis} is negative and vice versa. The I_{Dis} is proportional to the V_{TSV}. Fig. 5.6 shows the shielding ability when the n^+/n region is floating and grounded. When the n^+/n region is grounded, the shielding ability is better. Fig. 5.7 shows the shielding ability of the proposed guard ring where D_G is 10 μm. When there is the n^+/n region near the TSV although it is floating, the I_{Dis} decreases. If the n^+/n region is grounded, the shielding ability is the best among 3 cases, as shown in Fig. 5.7. The simulation result in Fig. 5.8 shows that the grounded n^+/n guard ring reduces coupling noise (=S_{21}) by 10 dB (~3 times) compared to that without guard ring, and suppresses more effectively the noise by 5 dB (~1.8 times) than the n^+ guard ring in the frequency range of 0.1 – 2 GHz where the distance between the input port and the out port is 10 μm.



(a)



(b)

Fig. 5.5. Displacement current of the drain in the victim nMOSFET just after applying step pulse (V_{TSV}) to the TSV electrode with polarity (a) and with amplitude (b) of V_{TSV} where D_G = 10 μm.

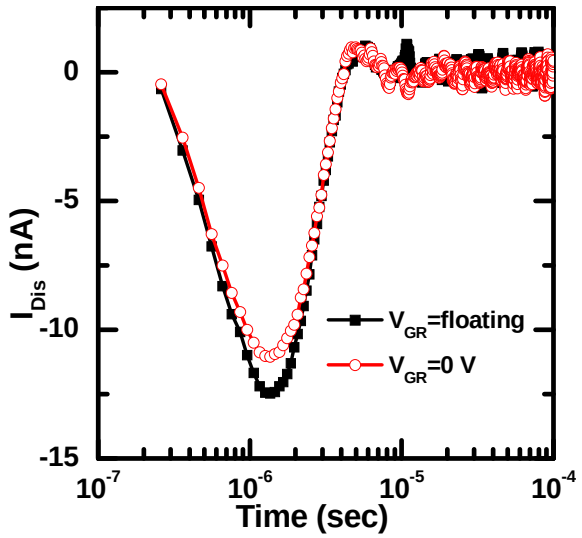


Fig. 5.6. Shielding ability of grounded n^+/n region where D_G = 10 μm.

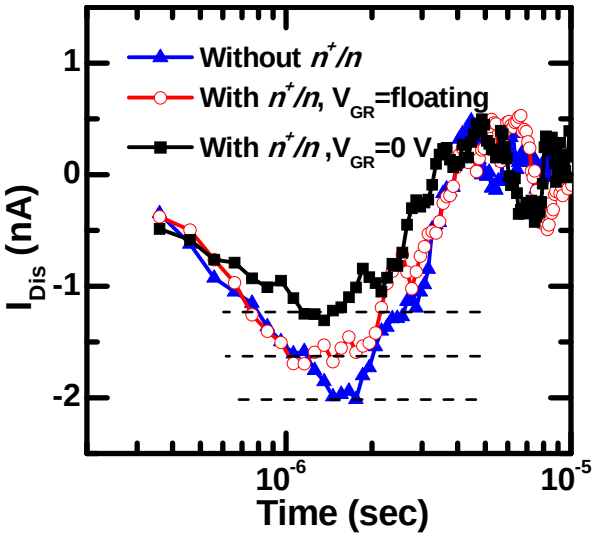
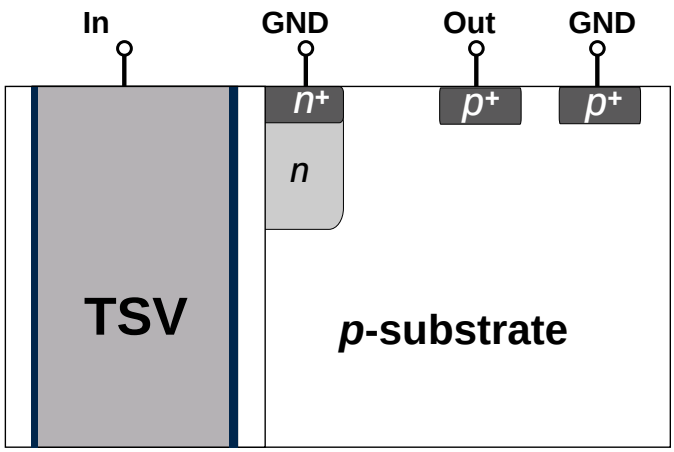
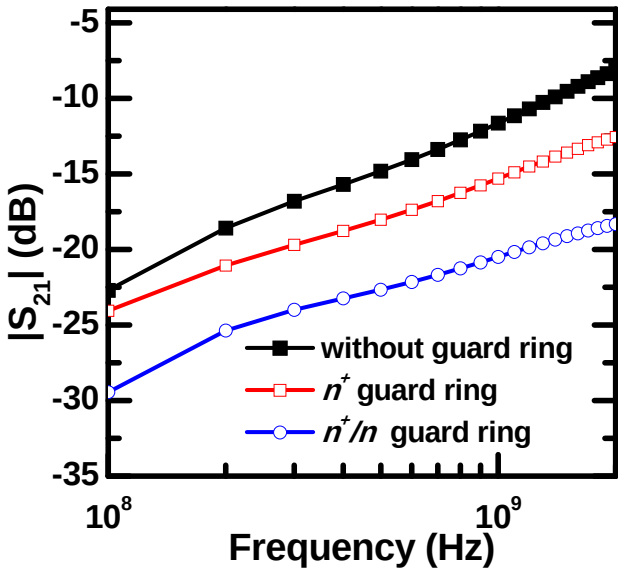


Fig. 5.7. Shielding ability of floating and grounded n^+/n region where D_G = 55 μm.



(a)

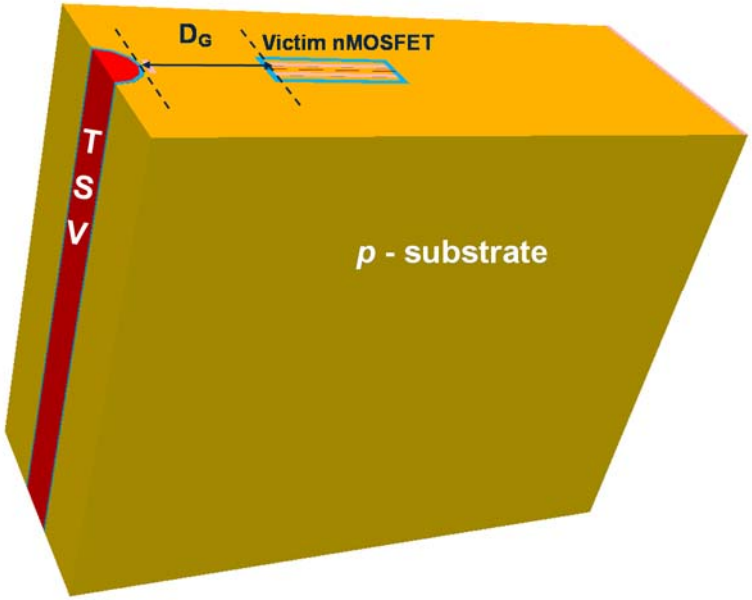


(b)

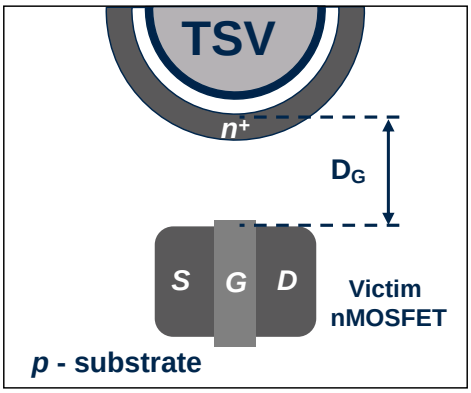
Fig. 5.8. (a) Simulation structure for extracting S_{21} parameter for the shielding ability of guard rings and (b) simulated S_{21} versus frequency with different guard rings where the distance between the input port and the out port is 10 μm.

5.3 Effectiveness of the proposed guard ring

To investigate the drain current fluctuation of the victim nMOSFET by the coupling noise from the TSV, a 3-D structure is simulated as shown in Fig. 5.9 (a). The drain current fluctuation is simulated as a parameter of the distance between the TSV and the victim nMOSFET (D_G) in Fig. 5.9 (b). The simulation condition is described in Fig. 5.10. The victim nMOSFET operates in steady state mode, when V_D = 0.1 V, V_G = 0.7 V, V_S = 0.0 V, and V_B = 0.0 V. The victim nMOSFET is located at the distance from TSV by 10 μm. The TSV pulse (V_{TSV}) is applied to the TSV electrode.



(a)



(b)

Fig. 5.9. (a) 3-D simulation structure to verify the drain current fluctuation of the victim nMOSFET induced by the pulse of TSV and (b) top view of the test pattern to extract the drain current fluctuation of the victim nMOSFET for different distance between the TSV and the victim nMOSFET (D_G).

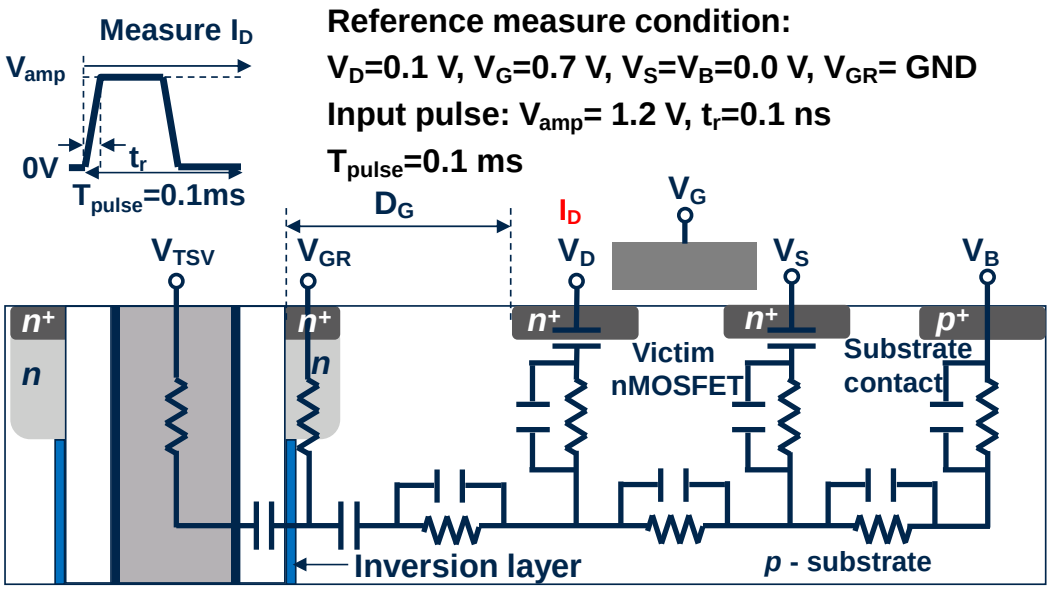


Fig. 5.10. Bias condition of simulation to extract the drain current fluctuation of victim nMOSFET for different guard ring schemes.

Fig. 5.11 shows the conceptual schematic when the V_{TSV} is applied to TSV electrode. When the pulse is applied, the TSV potential rises, and the holes moves toward the peripheral device for the charge neutrality. This hole flux from the depletion region affects the peripheral devices. The proposed guard ring supplies the inversion charge to the interface between the TSV oxide and the silicon substrate, which helps the charge neutrality with generating smaller hole flux compared without n^+/n guard ring. As a result, the hole flux decreases compared to the case without guard ring, and the n^+/n guard ring reduces the coupling noise. Fig. 5.11 shows the two kinds of effects of the hole flux. The holes reaching the peripheral device change the body potential and the junction capacitance of the source and the drain of the victim nMOSFET, and which result in the channel current and the displacement current of the victim nMOSFET.

The results of 3-D simulation in Fig. 5.12 demonstrate the current flow and the change of the body potential of the victim nMOSFET (V_B) induced by the V_{TSV} when the n^+/n guard ring is applied. The V_B without the n^+/n guard ring is also plotted for comparison. The amplitude and rising time (t_r) of V_{TSV} are 1.2 V and 0.1 ns, respectively, at the given drain bias (V_D) of 0.1 V and gate bias (V_G) of 0.7 V in the victim nMOSFET. At time t_1, V_B starts to increase due to the capacitance coupling between the TSV and the *p*-substrate [23]. This reduces the threshold voltage of the victim nMOSFET (V_{thN}), and increases the I_D and the

source current (I_S). Right after t_1, I_D changes due to the displacement current which flows through the drain junctions. The rising V_B reduces the potential barrier at the junction between the source and drain (S/D) and the *p*-substrate, so that electrons are supplied from the S/D. The changes of I_D and I_S (ΔI_D and ΔI_S) caused by the change of V_B are determined by the displacement current and the channel current change caused by the change of V_{thN}. The displacement currents of the source ($I_{S.dis}$) and drain ($I_{D.dis}$) are negative from t_1 to t_2. Both I_D and I_S take on negative values immediately at t_1 due to $I_{S.dis}$ and $I_{D.dis}$. From t_1 to t_2, V_B increases linearly with time, and $I_{S.dis}$ and $I_{D.dis}$ are nearly constant. The channel current rises with time due to the increase in V_B. Immediately after V_{TSV} reaches 1.2 V, the depletion width of the S/D junction at t_2 increases, and the electrons charged in the S/D junction capacitance flow out to the S/D electrodes. As a result, $I_{D.dis}$ and $I_{S.dis}$ become positive but diminish immediately. At t_3, V_B reaches its maximum, and I_D is maximized. After t_3, V_B decreases slowly and I_D converges to a steady state value. The V_B without a guard ring is larger than that with the n^+/n guard ring and it reaches a peak at t_4. Fig. 5.13 shows the measured ΔI_D with t_r. To measure the current change clearly, the amplitude of V_{TSV} is set to 6 V at a given V_D of 0.1 V and V_G of 0.3 V. The ΔI_D with the n^+/n guard ring is smaller than that without a guard ring by nearly one order of magnitude. The ΔI_D decreases with an increase of t_r because the ΔI_D is the displacement current and is inversely proportional to t_r.

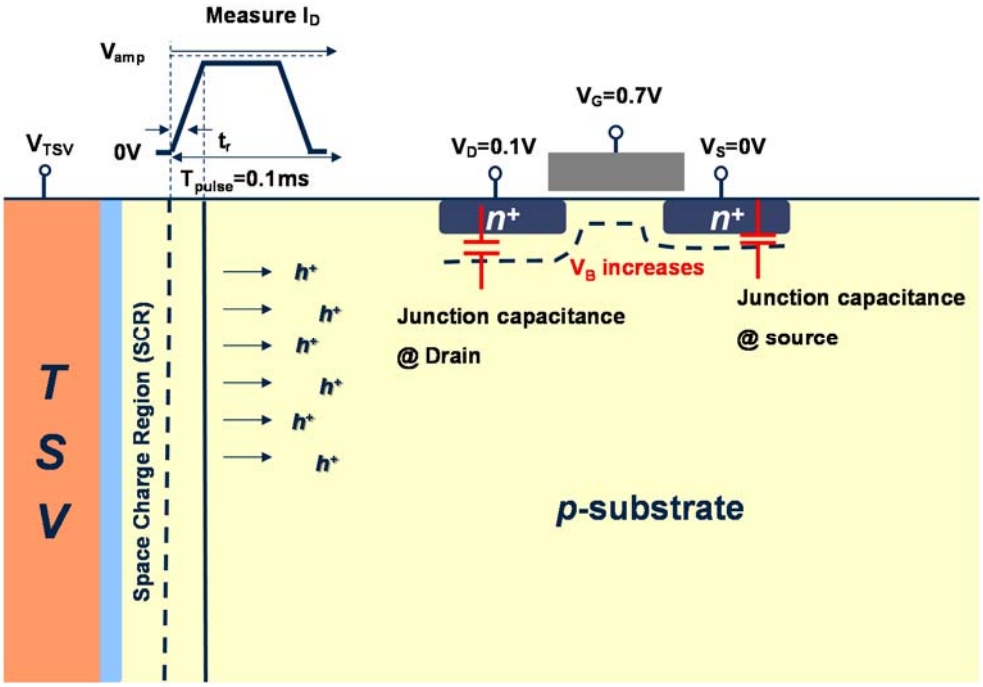


Fig. 5.11. Schematic diagram of degradation in a victim nMOSFET by the TSV pulse. The drain current fluctuation of the victim nMOSFET results from the channel current increased by the rise of body potential and the displacement current at the source and drain electrode due to the TSV pulse.

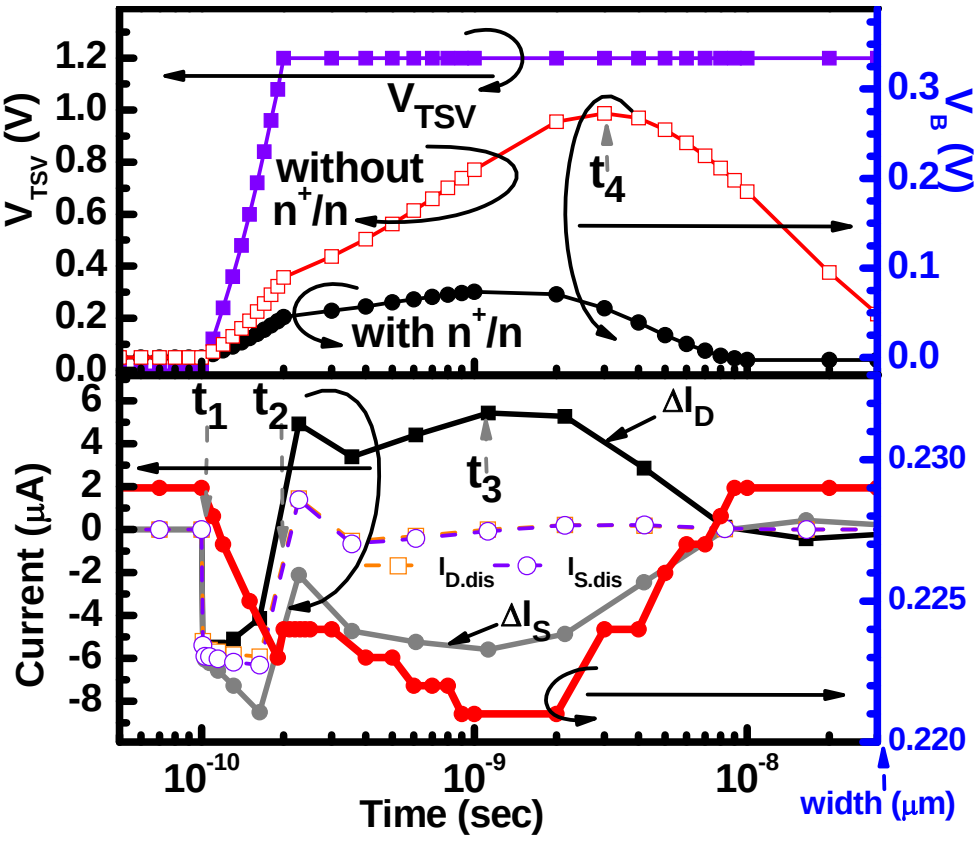


Fig. 5.12. Simulated V_{TSV}, V_B, $I_{S.dis}$, and $I_{D.dis}$ ($I_{S.dis}$ at V_D=V_S=V_G=0 V, $I_{D.dis}$ when V_D=V_S=0.1 V and V_G=0 V); the changes of I_D and I_S, and the depletion width of the source and drain versus time.

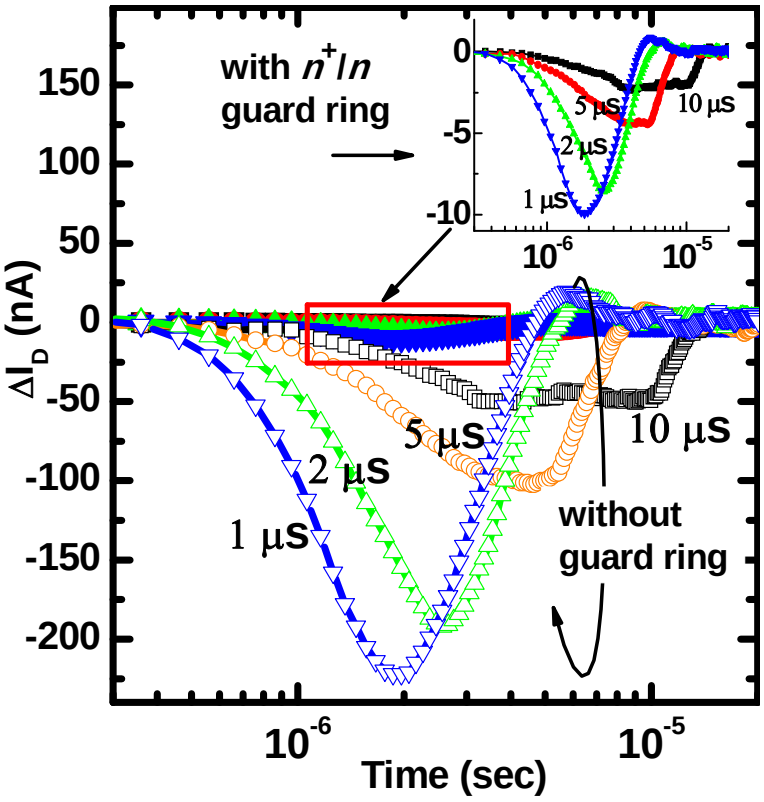
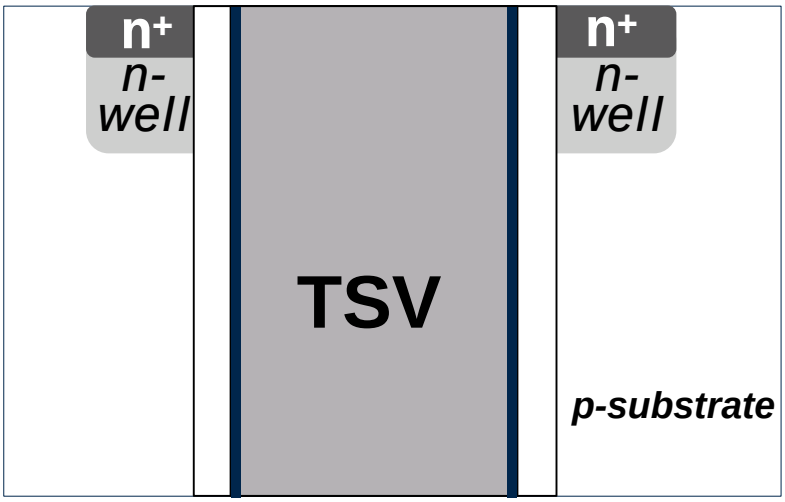
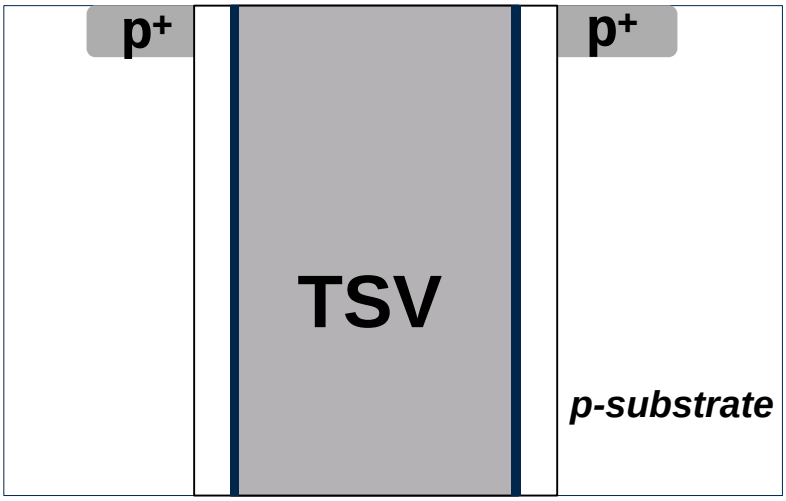


Fig. 5.13. Measured drain current fluctuation of victim nMOSFET (ΔI_D) with the rising time of V_{TSV}. The ΔI_D with the n^+/n guard ring is smaller than that without a guard ring by nearly one order of magnitude.

The fluctuation of I_D with the distance between the TSV and the victim nMOSFET (D_G in Fig. 5.9) was simulated to determine the performance of the n^+/n guard ring in comparison with cases without a guard ring and with a conventional p^+ guard ring [15], where the p^+ region surrounds the TSV. The proposed n^+/n guard ring and p^+ guard ring are shown in Fig. 5.14. The bias condition of the simulation is identical to that shown in Fig. 5.10 except that V_D is 1.0 V. Fig. 5.15 (a) shows the transient I_D as parameters of D_G and the guard ring schemes. To observe the change clearly, we define a fluctuation ratio as the maximum change of I_D (max I_D - I_D at DC bias) over I_D at a DC bias. In Fig. 5.15 (b), the ratio with the n^+/n guard ring decreases by ~71% and by ~61%, respectively, comparing to the cases without guard ring and with the p^+ guard ring. The keep-out zone (KOZ) is defined as the minimum distance to guarantee that V_B increases by 10% of the V_{TSV}, which is equivalent to the fluctuation ratio of 2.7% at the given bias. The KOZ with the n^+/n guard ring is about 0 μm, but the KOZ without a guard ring and with the p^+ guard ring exceeds 30 μm. Thus, our method effectively suppresses the coupling noise.

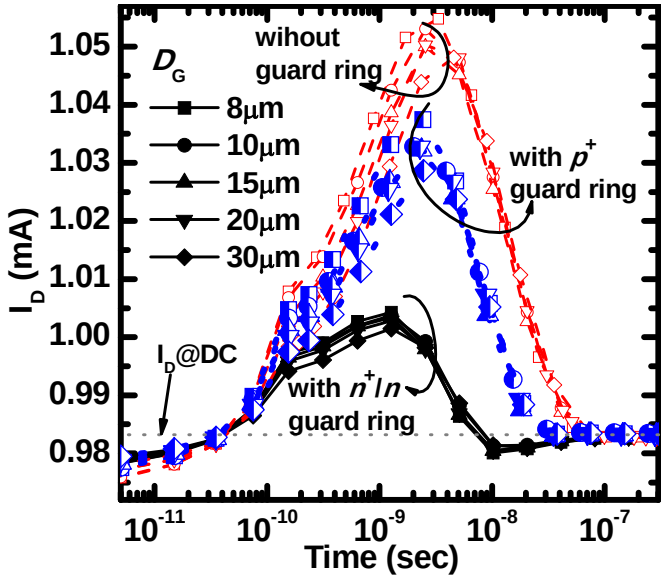


(a)

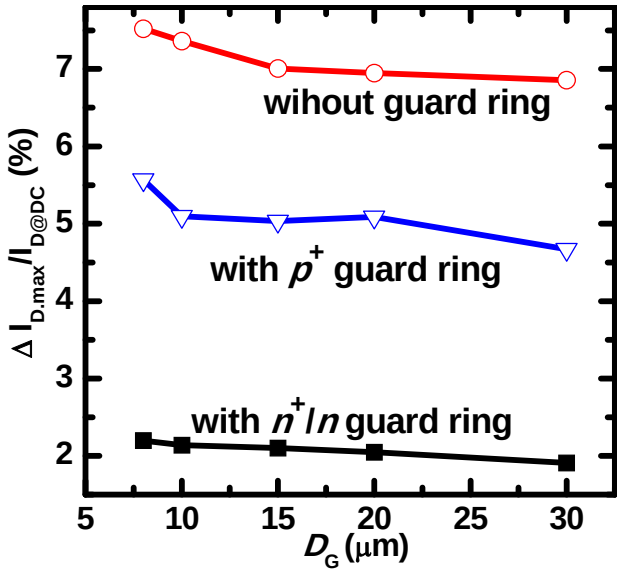


(b)

Fig. 5.14. Simulation structure of the proposed guard ring (a) and conventional p^+ guard ring (b).



(a)

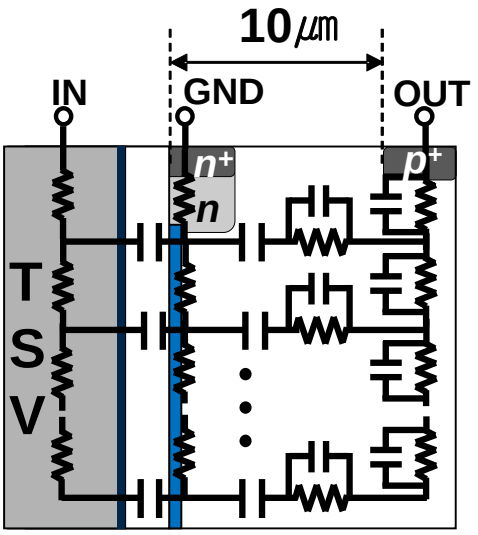


(b)

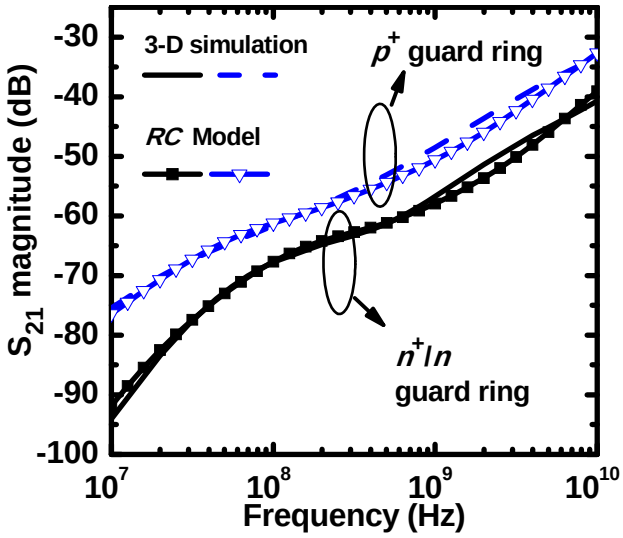
Fig. 5.15. (a) Transient drain current as parameters of the distance between the TSV and the victim nMOSFET (D_G = 8, 10, 15, 20, and 30 μm), and the guard ring schemes. (b) Fluctuation ratio of I_D ($\Delta I_{D,max}/I_{D@DC}$) with D_G.

5.4 Characteristics of the proposed guard ring by RC modeling

To investigate the shielding ability of the n^+/n guard ring with an increase in the signal frequency passing through the TSV, the *S*-parameter of the guard ring was simulated by 3-D device simulator and modeled by distributed *RC* model shown in Fig. 5.16 (a). To reflect the resistance of the inversion layer, resistors are added along the Si surface surrounding the TSV in the *RC* model. The input port is the TSV and the output port is the p^+ electrode. The *RC* model shows excellent agreement with the simulated result. Fig. 5.16 (b) shows that the transmission parameter (S_{21}) of the n^+/n guard ring is smaller than that of the p^+ guard ring by ~19 dB at 10 MHz and by ~7 dB at 10 GHz. The difference in S_{21} between the n^+/n and p^+ guard rings becomes smaller with an increase in the frequency. The inversion charge far from the n^+ source cannot respond to a high-frequency TSV signal due to the *RC* delay. Thus, the coupling noise from the lower part of the TSV cannot be suppressed.



(a)



(b)

Fig. 5.16. (a) Distributed *RC* model of the TSV and the guard ring and (b) S_{21} magnitudes with guard ring schemes obtained by 3-D device simulator and proposed distributed *RC* model.

To characterize the effective depth of the inversion layer with the frequency, an inversion capacitance ratio is defined as the inversion capacitance (C_{inv}) at various small signal frequencies over the inversion capacitance at a frequency of 1 MHz ($C_{inv\ @f=1MHz}$). Fig. 5.17 shows the simulated inversion capacitance ratio and the effective depth of inversion layer which is obtained by multiplying the total depth of the TSV by the inversion capacitance ratio for the n^+/n guard ring. As the frequency increases, the effective area of the shielding layer decreases, resulting in a decrease of C_{inv}. As a result, the inversion capacitance ratio and the effective depth of the inversion layer decreases, as shown in Fig. 5.17.

To analyze the signal transmission of the proposed guard ring, the simulation is performed by the distributed *RC* model in Fig. 5.18 (a). The input port is the top of the TSV, and the output port is the bottom of the TSV. Fig. 5.18 (b) shows that the signal transmission (S_{21}) of the n^+/n guard ring is smaller than that of the p^+ guard ring by ~0.019 dB at 10 GHz because the TSV capacitance of the n^+/n guard ring increases due the inversion capacitance, and the inversion charge far from the n^+ source cannot respond to a high-frequency TSV signal due to the *RC* delay. Thus, the transmission ability of the proposed guard ring decreases at the high frequency, but it is not significant.

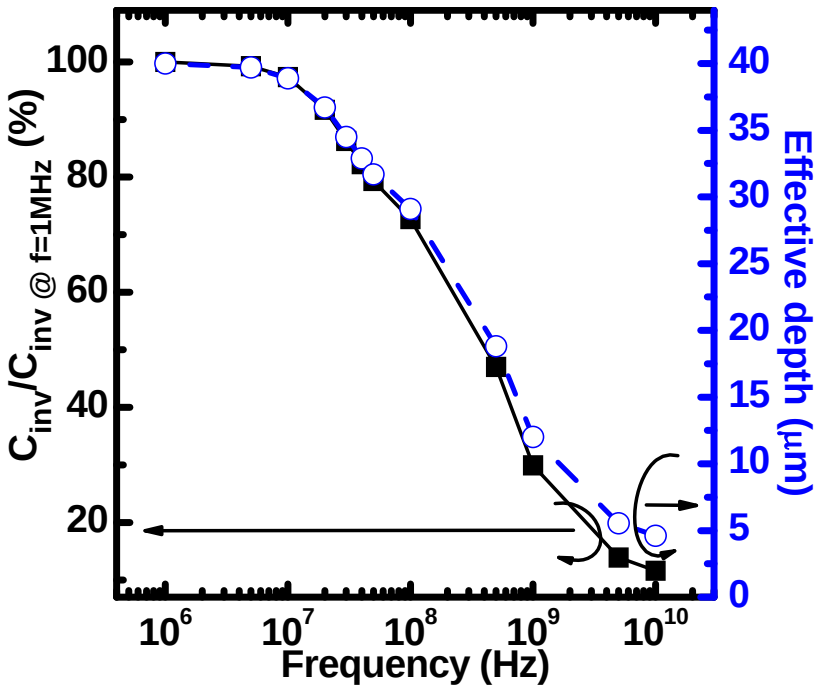
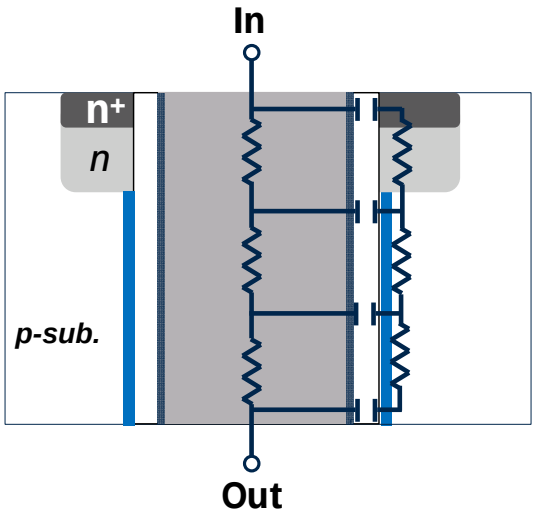
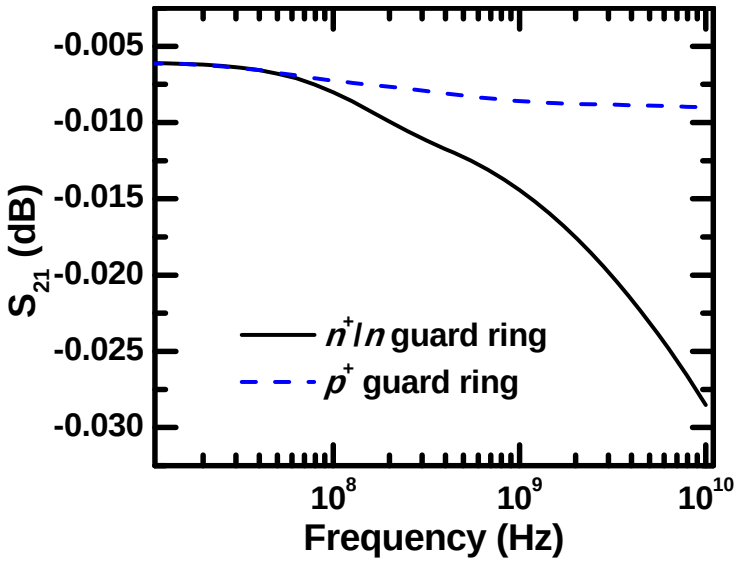


Fig. 5.17. Inversion capacitance ratio ($C_{inv}/C_{inv\ @f=1MHz}$) and the effective depth of the inversion layer of the n^+/n guard ring.



(a)



(b)

Fig. 5.18. (a) Distributed *RC* model of the TSV and guard ring and (b) signal transmission parameter (S_{21}) magnitudes with guard ring schemes obtained by distributed *RC* model.

Conclusions

In this dissertation, we propose a new guard ring to suppress the coupling noise from a TSV and investigate the characteristics and the shielding ability of the proposed guard ring. The proposed guard ring reduces the coupling noise from the TSV utilizing an inversion layer. The coupling noise induced by the TSV is reduced by approximately one order of magnitude in the near-threshold region of a victim nMOSFET, which is located 10 μm away from the TSV. The proposed guard ring is characterized in terms of the distance between the TSV and the victim nMOSFET in comparison with cases without a guard ring and with a conventional p^+ guard ring. The proposed method reduces the drain current fluctuation by approximately 61% compared to the case with the conventional p^+ guard ring. The proposed guard ring only changes the drain current of the victim nMOSFET by ~ 2.2%. The p^+ guard ring cannot achieve this result regardless of the distance between the TSV and the victim nMOSFET. At a high frequency, the shielding ability of the proposed guard ring decreases, but it is still better than that of the p^+ guard ring. This is caused by the inversion charge, which does not reach the bottom of the TSV due to the *RC* delay of the inversion layer. The proposed guard ring is easily fabricated by modifying the

active and ion implantation mask without additional process steps, making it easy to implement in conventional devices.

The proposed guard ring can be used for an electrical characterization of the effect of Cu diffusion in the TSV and verified its usefulness. Using the proposed guard ring, we could obtain the *C-V* curves, the gated-diode current, and the charge pumping current from the samples with thin and thick barrier metals, and accurately analyze the trap position and the trap profile. Thus, the pattern is very effective when used to characterize Cu diffusion.

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초 록

최근 반도체 소자의 회로 선폭이 감소함에 따라 2차원 구조를 이용한 고집적 반도체 칩의 제작은 한계에 가까워 지고 있다. 이는 현재의 반도체 기술로는 더 작은 선폭의 lithography 공정이 어렵기 때문이다. 미세화 기술에 따른 한계를 극복하기 위해 3차원 패키지 기술이 연구되고 있는데, 여러 가지 3차원 패키지 기술 중에 through silicon via (TSV) 기술이 가장 전도 유망한 것으로 각광 받고 있다. TSV는 여러 개의 반도체 칩을 수직방향으로 증착하고 TSV 전도체를 통해 각 반도체 칩을 전기적으로 연결시켜 한 개의 패키지로 제작하는 기술이다. 3차원 패키지 기술은 고용량 메모리를 만드는데 유리할뿐더러 다른 기능을 가진 반도체 칩을 한 개의 패키지로 만들 수 있는 장점을 가지고 있다. TSV는 이를 이용한 3차원 구조의 고집적 반도체 칩을 만들 수 있는 장점에도 불구하고, 몇 가지 단점을 가지고 있다. 가장 중요한 것이 coupling noise에 의한 TSV 주변소자의 특성 열화이다. TSV는 high-frequency signal이 지나가는 통로가 되는데 이때 TSV주변에 위치하는 반도체 소자와 TSV가 coupling 되어 TSV를 통과하는 signal에 의해 주변소자의 동작이 영향을 받게 된다. 이를 억제하기 위해 가드링을 제작 하는 등의 기술이 필요하다. 또한, TSV는 전도체로 사용되는 구리에 의해 주변소자를 열화 시키는 단점을 갖고 있다. 구리는 큰 확산계수를 갖고 있어 열공정에 의해 주변소자로 쉽게 확산이 되고, 이는 주변소자에 trap을 생성시켜 TSV를 사용한 반도체 칩의 신뢰성에 문제를 일으킬 수 있다.

본 논문에서는 coupling noise를 억제하는 새로운 가드링(guard ring) 구조를

제안하였다. 제안된 가드링은 실리콘 활성영역에 얕은 n^+ 불순물 영역과 깊은 n-well불순물 영역을 가진 구조로 제작되었다. 제안된 TSV와 가드링 구조의 제작 의도는 TSV를 감싸는 oxide에 존재하는 positive charge에 의해 TSV 주변에 반전 전하층 (inversion layer)이 생성되고, 생성된 반전 전하층을 이용하여 coupling noise를 차폐하는 가드링으로 활용하기 위함이다. 본 논문에서는 제안된 가드링의 특성을 정량적으로 분석하였고, coupling noise 감소 특성 분석을 위해 주변소자에서의 transient 특성을 측정하여 그 효과를 명확히 증명하였다. 또한, 3차원 구조에서의 simulation을 통해 TSV 주변소자의 drain 전류를 분석하여 coupling noise효과를 상세히 기술하였고, 동일한 방법으로 통상의 p^+ 가드링 구조와 coupling noise 감소 효과를 비교하여 제안된 가드링의 효과를 입증하였다. 또한, 제안된 가드링 구조에서 반전 전하층의 유효 깊이에 대해 분석하였으며, RC modeling을 통해 coupling noise 차단 효과와 TSV 신호 전달 특성을 분석하였다. 제안된 가드링은 기존의 junction type 가드링보다 개선된 coupling noise 차폐특성을 갖고 있으며, 이온주입 mask와 active define mask의 변경만으로 쉽게 제작할 수 있는 큰 장점을 가지고 있다.

TSV 전도체는 저전력 동작을 위해 높은 전도성을 가진 물질로 제작되어야 한다. 구리는 TSV의 전도체 물질로 많이 사용되지만, 구리 원자는 주변의 silicon substrate와 주변 소자로 확산이 쉽게 되어 주변소자에 trap을 생성시키며, 이는 낮은 온도의 열처리 공정에도 확산이 잘 일어나서 주변소자의 신뢰성에 문제를 일으킬 수 있다. 따라서 구리의 확산을 억제하는 것이 매우 중요할뿐더러 구리 원자가 주변으로 얼마나 확산되는지 측정하는 것도 중요하다. 하지만 구리의 확산에

의해 생성되는 trap의 특성을 측정 하는 것에 어려움이 있는데, 이는 TSV가 silicon wafer표면으로부터 수십 마이크로 미터 깊이까지 생성되기 때문에 TSV 전체의 특성을 측정하는 것이 쉽지 않다. 본 연구에서는 제안된 가드링 구조를 이용하여 구리 확산에 의해 생성되는 trap을 직접 측정하고, barrier metal 두께에 따른 구리 확산의 전기적 평가를 수행하였다.

이상과 같이 본 논문에서는 새로운 TSV용 가드링 구조를 제안하고 측정과 시뮬레이션을 통해 그 효과를 검증하였다. 또한, TSV전도체로 이용되는 구리의 확산을 분석하는 효과적인 방법을 제안하였다. 제안된 가드링의 적용을 통해 TSV의 신뢰성을 높이고, 특성을 평가하는데 큰 도움이 될 것이다.

주요어: TSV, 가드링, 커플링 노이즈, 반전 전하층 차폐, 구리 확산

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