Ph.D. DISSERTATION

Reliability in Floating-Gate NAND Flash Memory Devices

Floating-Gate를 갖는 Flash Memory 소자의 신뢰성분석

BY

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Abstract

As flash memory cells continue to decrease in scale, random telegraph noise (RTN) caused by electron capture or emission at trap sites has become an important issue. Fluctuations in the threshold voltage (ΔV_{th}) due to RTN can cause serious problems, such as read errors and device instability. As the thickness of the inter-poly dielectric IPD continues to decrease, the traps in the IPD also lead to reliability issues related to the leakage current and data retention.

In this thesis, we investigate the reliability of NAND flash memory with respect to traps not only in the tunneling oxide but also in the IPD of the cell device.

We first focus on traps that produce RTN in the tunneling oxide during a read operation. The trap position with respect to the channel surface and the floating-gate (x_T) and the trap position along the channel length direction (y_T) in the fabricated NAND flash memories were obtained by considering the channel resistance of the pass cells. The RTN in the floating-gate NAND flash cell strings interfered with the adjacent bit-line cell, and the effects of such on the fluctuations in the bit-line current (ΔI_{BL}= high I_{BL} – low I_{BL}) were characterized.

The electron current density (J_e) of a read cell was found to be appreciably different depending on the position in the channel width direction relative to the

interference produced by the adjacent bit-line cells. We verified that ΔI_{BL} due to RTN increases as a high J_e position is controlled to be close to a trap position in 32 nm NAND flash memory strings. The adjacent cell interference was shown to affect not only ΔI_{BL} but also the ratio between the capture and the emission time constants [$\ln(\tau_c/\tau_e)$]. We used the interference between the adjacent bit-lines (BLs) to obtain the trap position along the width direction and to represent the 3-D position of the traps in 32 nm and 26 nm NAND flash memory cells for the first time. We propose a new read method that reduces the effects on ΔI_{BL} resulting from RTN. The pre-bias is controlled in the μs range, and our method was confirmed to effectively suppress the effect of the RTN during read operations in NAND flash memory. Second of all, we investigate the hysteresis phenomenon in the floating-gate NAND flash memory strings, which originates from the traps in the bottom oxide of the oxide/nitride/oxide blocking dielectric (IPD). The hysteresis phenomenon in the floating-gate NAND flash memory strings is analyzed by measuring pulsed *I-V* and fast transient I_{BL}. A new read method that suppresses the effect of the hysteresis phenomena was also proposed in order to reduce the read failures in NAND flash memory. In the Appendix, ΔI_{BL} is modeled with the trap position as a parameter for the state (program or erase) of the adjacent bit-line cells, and it is observed to appreciably affect the current density distribution. ΔI_{BL} is modeled by determining the integrated electron current density [$J_0=f(z)$] and the electric blockade length (L_t) by considering the

effect of the interference on the adjacent cells. A characteristic function [$g(z)$] with a Gaussian functional form is defined based on L_t and the trap position within the tunneling oxide from the channel surface (x_T). Finally, ΔI_{BL} is extracted by integrating $f(z)$ and $g(z)$. Our model accurately predicts ΔI_{BL}, with the trap position as a parameter of the state of the bit-line cells, showing good agreement with data from a 3-D simulation.

Key Words: Reliability, NAND flash memory, Random Telegraph Noise, Bit-line interference, Bit-line current fluctuation, Floating-gate, Inter-poly dielectrics (IPD), Hysteresis.

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Chapter 1

Introduction

1.1 Reliability issues in NAND flash memory

Currently, NAND flash memory has evolved as a result of the increase in diversity in computing environments. NAND flash memory has been extensively adopted as the main storage device for mobile and multimedia products due to its smaller dimensions, lower power consumption, and higher access speed relative to magnetic core memory. Moreover, hard disk drives (HDD) will be completely replaced with solid state drives (SSD) in the near future. The reason for such success can be explained by the rapid reduction in the feature size of memory cells and multi-level-cell (MLC) operation, which have led to a reduction in the cost per bit and a resulting increase in consumer demand. The 2013 International Technology Roadmap for Semiconductors (ITRS) projects

that the physical gate length of NAND flash memory can be scaled down to 12 nm and that the maximum number of bits per cell will be three bits due to the lower cost per bit that can be achieved in 2015 [1]. However, as the dimensions of NAND flash memory cells are reduced near the final scaling limit in the nanometer regime and the maximum number of bits per cell increases, NAND flash memory has begun to face challenges related to reliability.

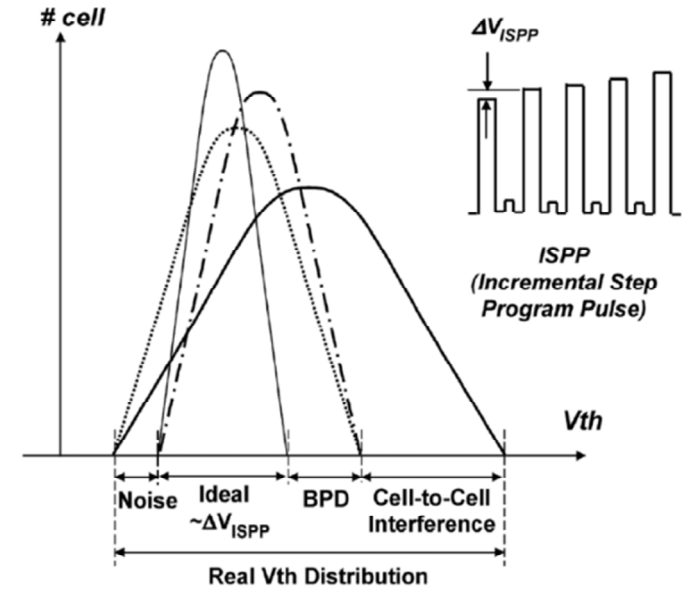
In contrast with NOR flash memory, NAND flash memory suffers from various problems – such as cell-to-cell interference, background pattern dependency, read disturbance and so on – due to the intrinsic characteristics of its architecture and the corresponding operating scheme. These problems cause a broad distribution in V_{th} and influence the read operations, as shown in Fig. 1.1 [2, 3]. In order to overcome these issues, many groups have studied new solutions from an operation standpoint as well as from an architectural point of view. However, these solutions have led to an increase in the complexity of the algorithms used in the operation scheme as well as in the manufacturing process.

Fundamental physical limits have led to a reduction in the number of electrons that are stored per bit in the floating-gate, resulting in a discreteness of the cell state in NAND flash memory strings. Table I and Fig. 1.2 show the locations of the charge in the floating-gate flash memory cell as well as the number of electrons required to produce a shift of 100 mV in the threshold voltage (ΔV_{th}) at each location as a function of the technology node [3]. As

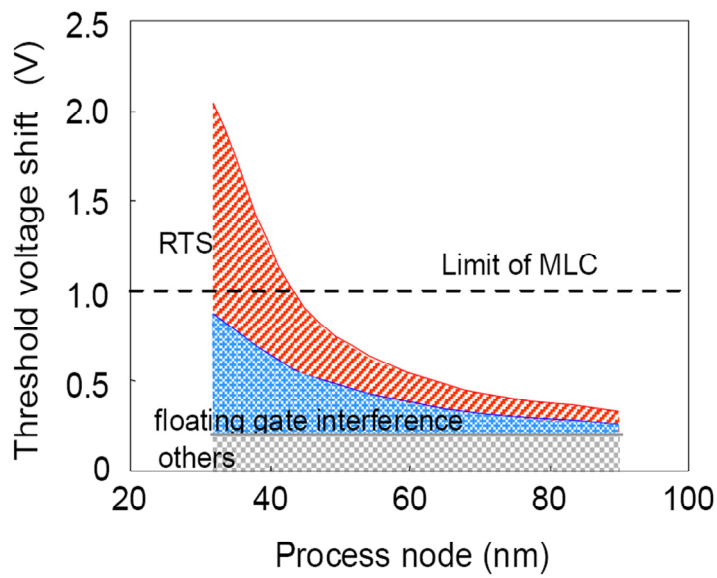
shown in Fig. 1.2, the number of electrons that produce a ΔV_{th} of 100 mV are dramatically reduced as the devices are scaled further down, and the V_{th} of the cell becomes more sensitive to a charge trapped in each location. In addition, a severe failure can occur during cell state verification if a charge loss from floating-gate occurs during the read operation. Fig. 1.3 shows the cumulative probability of the retention time for the floating-gate flash memory with a reduced number of electrons per bit [4]. As the devices are scaled down, the impact of a single electron has a tremendous influence on the retention characteristics because the amplitude of ΔV_{th} due to a single electron increases.

Random telegraph noise (RTN) causes a capture/emission of an electron at a trap site, and it has become a critical issue for NAND flash memory because it can cause an error during read operations that will make the memory become unreliable. The effect of RTN is known to be more severe in floating-gate NAND flash memories because they have a thicker tunnel oxide relative to other CMOS devices. The effect of RTN would be more significant in a device that is scaled down, and the ΔV_{th} reported as a result of RTN was of ~0.3 V in 50 nm NAND flash memory, as shown in Fig. 1.4. [6]. Since there is a positional effect in a NAND cell string, a cell located closer to the bit-line has a higher ΔV_{th} due to the RTN because it has a lower trans-conductance due to a higher equivalent source resistance [7]. Furthermore, the power of the low-frequency noise (LFN) and the ΔV_{th} of a cell string have been reportedly influenced by the state of the

cells in the bit-line (BL) direction, the bias conditions, and the program/erase (P/E) cycling [8], [9].



(a)



(b)

Fig. 1.1. (a) Parasitic effects on distribution of V_{th} in NAND flash memory [2].

(b) ΔV_{th} due to parasitic effects as a parameter of the technology node [3].

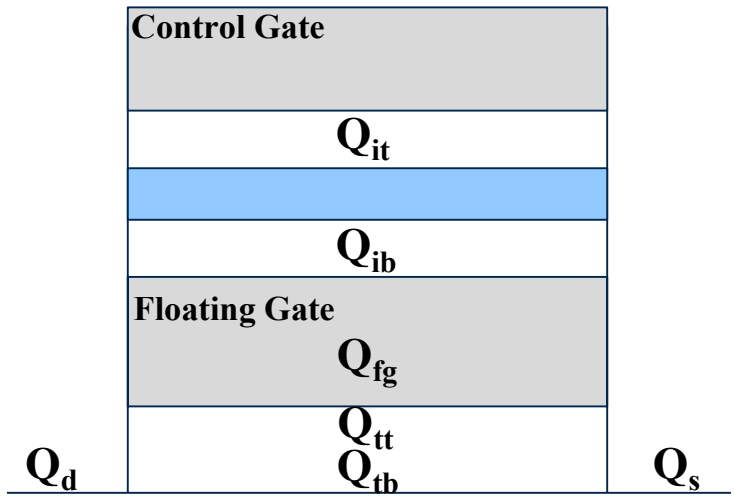


Fig. 1.2. Locations of charge in a floating-gate flash memory cell [4].

	50 nm	35 nm	20 nm
Q_{tb}	4	2	1
Q_{tt}	9	7	4
Q_{ib}	22	17	9
Q_{it}	149	103	100
Q_s	33	9	5
Q_d	61	16	10
Q_{fg}	18	12	10

Table I. Number of electrons required for threshold voltage shift (ΔV_{th}) of 100 mV at each location as a function of the technology node [4].

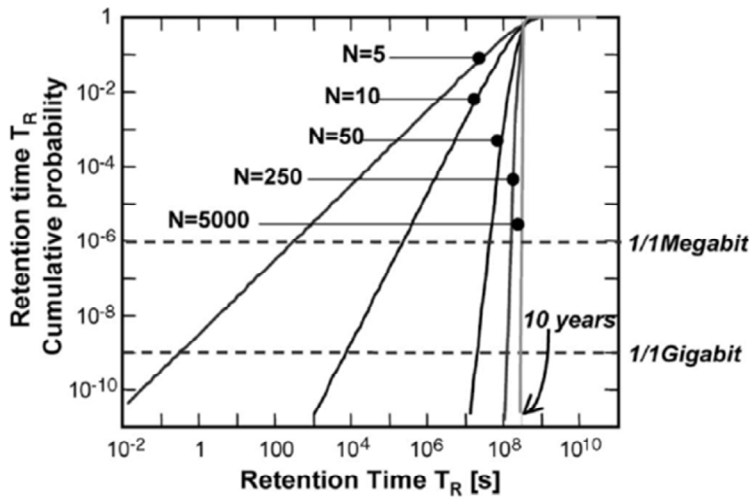


Fig. 1.3. Cumulative probability of retention time of floating-gate memories with reduced number of electrons per bit [5]

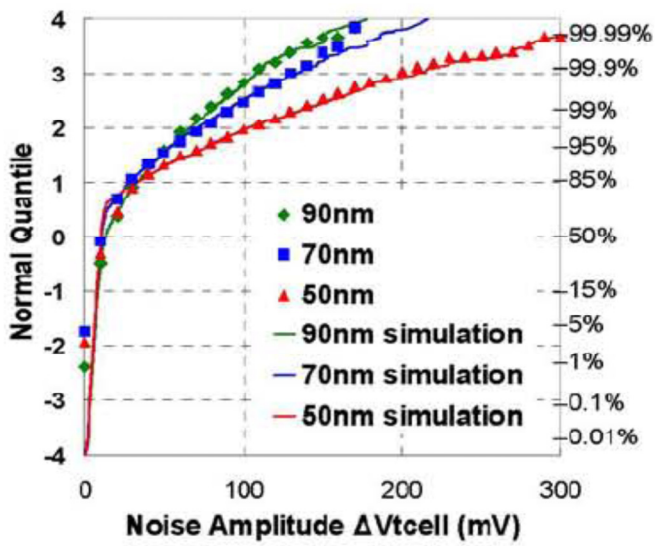


Fig. 1.4. Cumulative distributions of ΔV_{th} due to RTN at each technology node in NAND flash memory [6].

1.2 Motivation and organization

As previously mentioned, reliability issues are one of the major concerns that arise when scaling down technology, so extensive research has focused on addressing the reliability of such devices, particularly for RTN due to traps in the insulator of the cell. Previous studies have usually observed a distribution in ΔV_{th} due to RTN when scaling down and have focused on extracting the trap location in the tunneling oxide of a cell. However, such studies have investigated the characteristic of RTN without considering the effects of the channel resistance of the pass cells and the adjacent bit-line cell interference, which originates from the characteristic of the NAND structure. Therefore, it is necessary to study the RTN in NAND flash memory by considering these effects. In addition, reliability problems and their causes due to traps in the inter-poly dielectric (IPD) are studied since no other paper has presented a systematic report that investigates these cases in NAND flash memory with a $SiO_2/Si_xN_y/SiO_2$ (ONO) stack as the IPD, even if the ONO stack is still used as the IPD by the industry.

This dissertation consists of the following four chapters. In Chapter 2, the trap positions (x_T and y_T) that cause channel resistance in the pass cells are obtained. Chapter 3 discusses the effects of the adjacent bit-line cell interference on RTN in NAND flash memory and also determines the trap position along the

channel width direction (z_T). The x_T, y_T and z_T of the traps, which are obtained for 32 nm and 26 nm NAND flash memory cell strings, are illustrated in a 3-D plot. In Chapter 4, we propose a new read method that reduces the effects of ΔI_{BL} due to RTN. In Chapter 5, the hysteresis phenomenon due to the traps in the IPD is introduced and is systematically investigated through a pulsed *I-V* and a fast transient bit-line current (I_{BL}) measurement in the NAND flash memory strings.

The Appendix at the end of the dissertation provides an explanation of the modeling used for the bit-line current fluctuation (ΔI_{BL}= high I_{BL} – low I_{BL}) due to RTN, by considering the bit-line interference in the NAND flash memory.

Chapter 2

Extraction of trap profiles considering channel resistance of pass cells

2.1 Introduction

As scaling down in the flash memory cell, random telegraph noise (RTN) leads to broaden threshold voltage distribution [3]. Especially in a NAND flash memory string, there is a cell position dependence of threshold voltage change (ΔV_{th}) due to the RTN [10]. This indicates that the channel resistances of pass cells in a cell string are affecting to RTN characteristics of a selected cell. Until now, trap positions from the channel surface to the floating-gate (x_T) and along channel length direction (y_T) has never been tried to extract with considering channel resistances of pass cells. In this work, we extracted the exact position and energy of a trap with considering channel resistances of pass cells for the first time.

2.2 Device structure and measurement method

The floating-gate NAND flash memory in this work was fabricated at a semiconductor company by applying 32 nm and 48 nm technology. As shown in Fig. 2.1 (a), a 32 nm NAND string consists of sixty-four unit cells, two dummy cells, a drain select line (DSL) transistor and a source select line (SSL) transistor. The cross-sectional TEM view of the 32 nm NAND flash memory cells in the WL direction is shown in Fig. 2.1 (b). Cells of NAND flash memories in this work have nearly the same channel length (L) and width (W). Tunneling oxide thickness is 8.7 nm, and inter-poly O/N/O layer has a stack of 4/4/6 nm.

The block diagram of noise measurement system is represented in Fig. 2.2. To observe the bit-line current fluctuation (ΔI_{BL}= high I_{BL} – low I_{BL}) exactly, the biases are applied to Word-Lines (WLs) and Bit-Line (BL) in the string by using a DC power source (batteries are shielded by grounded metal box). The ΔI_{BL} is amplified by the low-noise amplifier (LNA) and is displayed on the dynamic signal analyzer (Agilent 35670A).

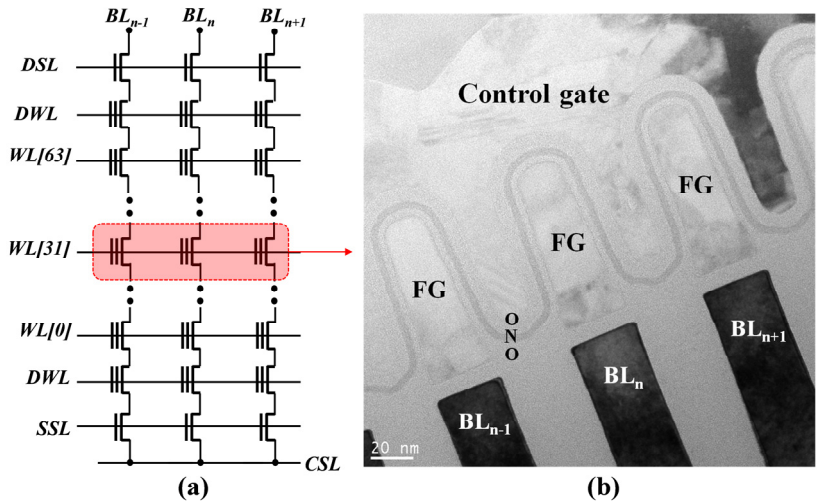


Fig. 2.1. (a) Schematic view of NAND flash memory strings and (b) Cross-sectional TEM view of 32nm NAND flash memory cells in the WL direction.

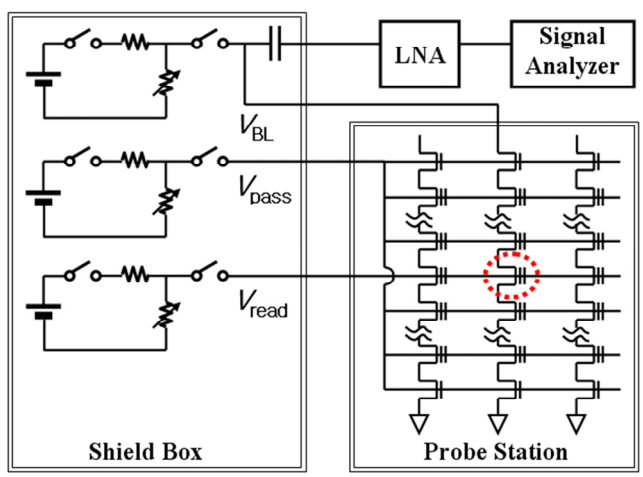


Fig. 2.2. Block diagram of the low frequency noise measurement system. The selected cell is represented by a dotted circle. Control-gate bias (V_{CG}) and V_{pass} were applied to the WL of a selected cell and unselected cells in the string, respectively.

2.3 Equations of trap profiles in a NAND flash memory string

Fig.2.3 shows the schematic circuit diagram showing three NAND cell strings and an equivalent circuit of a string when a cell is read. A NAND string can be analyzed with an equivalent circuit shown in of Fig. 2.3. When we read a cell in a cell string by applying a read voltage to the WL corresponding to the read cell, pass cells biased by a pass voltage (V_{pass}) have channel resistances. For this reason, the pass cells except a read cell can be modeled as linear resistors [11]. When we read a cell in the string, remaining pass cells become equivalent resistance which gives significant error in extracting RTN profile (position and energy).

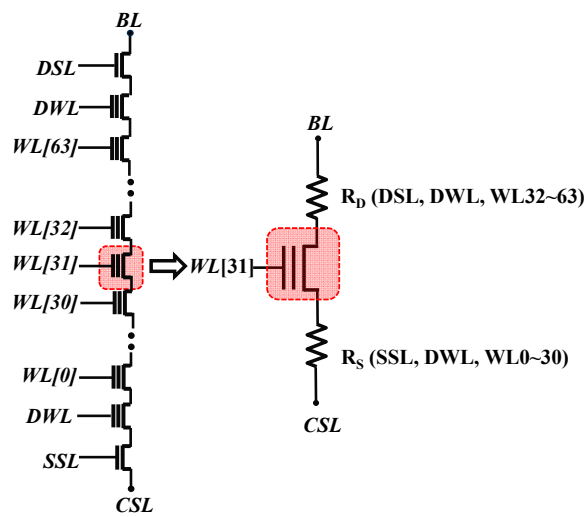


Fig. 2.3. Schematic circuit view of a NAND cell string and its equivalent model.

As the control gate voltage increases, potential drops at the drain and source of a read cell gradually increase due to voltage drop across the channel resistances of pass cells. So, the surface potential (Ψ_s) slightly increases by the source voltage (V_S) and the channel potential (V_C) decreases due to voltage drop across the channel resistances of pass cells. Fig. 2.4 shows the energy band diagram of a read cell, which is used to extract the trap profile of a trap in the tunnel oxide. This figure includes the effect of source voltage (V_S) and channel potential variation (dV_C/dV_{GB}) due to the channel resistances of pass cells.

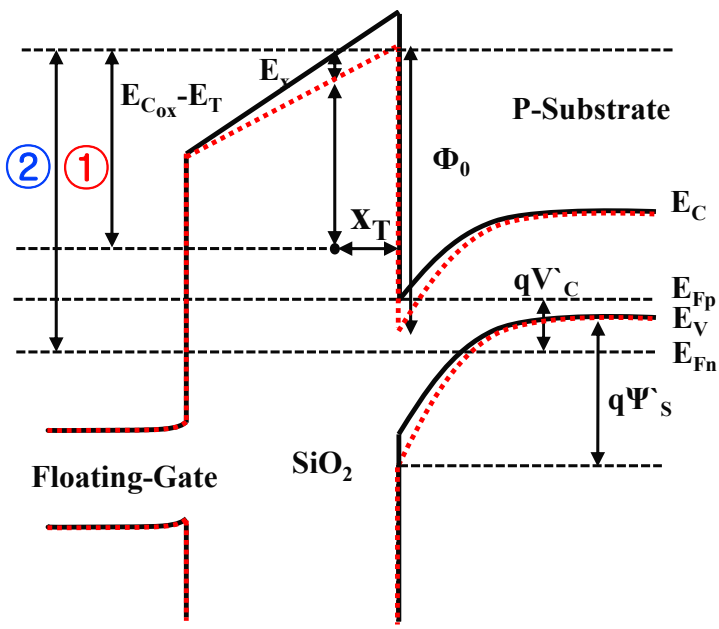


Fig. 2.4. Energy band diagram including the effect of the channel resistance of pass cells.

In order to extract the trap profiles, the relationship between time constants and trap energy level usually is used as following Eq. (2.1),

$$\frac{\tau_c}{\tau_e} = g \cdot \exp\left(\frac{E_T - E_F}{k_B T} \right) \qquad \text{Eq. (2.1)}$$

where, g is the degeneracy factor, k is the Boltzmann constant, T is the temperature, τ_c and τ_e are the mean capture and emission time, respectively, E_T is trap energy level and, E_F is Fermi energy level. Eq. (2.1) can rewrite Eq. (2.2) as,

$$\begin{aligned} k_B T \ln \frac{\tau_c}{\tau_e} &= \left[\varphi_0 - q\psi_s - qV_C + (E_C - E_{Fp} + qV_C) \right] \\ &- \left[q \frac{x_T}{T_{ox}} \left(V_{GS} - V_{FB} - \psi_p - \psi_s - V_C \right) + (E_{Cox} - E_T) \right] \end{aligned} \qquad \text{Eq. (2.2)}$$

where, E_{Cox} is the conduction band edge of the oxide, E_C is the conduction band edge of silicon, φ_0 is the difference between the electron affinities of silicon and SiO_2, V_{FB} is the flat-band voltage, x_T is the trap position from the channel surface to the floating-gate and T_{ox} is the tunneling oxide thickness.

In a NAND flash memory cell string, the drop of potential at drain and source side of a cell gradually occurs as increasing V_{CG} due to R_S and R_D. So, Ψ_s

slightly increases as increasing V_S. Using approximation of gradual V_C, the term of V_C is also dependent of V_{GB} because V_C can express as $[y_T\{V_D-I_D(R_S+R_D)\}]/L_{eff}$. Here, y_T and L_{eff} are the trap position along channel length direction and the effective gate length, respectively. Consequently, $d\ln(\tau_c/\tau_e)/dV_{GB}$ is represent by Eq. (2.3),

$$\frac{d\ln\frac{\tau_c}{\tau_e}}{dV_{GB}} = -\frac{1}{k_B T}\left[\frac{d\psi_{S0}}{dV_{GB}} + q\frac{x_T}{T_{ox}}\left(1-\frac{d\psi_p}{dV_{GB}}-\frac{d\psi_{S0}}{dV_{GB}}-\frac{dV_s}{d(V_{GB})}-\frac{dV_C}{dV_{GB}}\right)\right] \quad \text{Eq. (2.3)}$$

Where, where g is the degeneracy factor, k is the Boltzmann constant, T is the temperature, τ_c and τ_e are the mean capture and emission time, respectively, E_T is trap energy level and, E_F is Fermi energy level. From the Eq. (2.3), x_T can express as Eq. (2.4) and Eq. (2.5).

$$x_T = \frac{T_{ox}\left(\frac{kT}{q}\left(\frac{d\ln\frac{\tau_c}{\tau_e}}{d(V_{GB})}\right)_f + \left(\frac{d\psi_S}{d(V_{GB})}\right)_f\right)}{\left(\left(\frac{dV_{C\_forward}}{d(V_{GB})}\right)_f + \left(\frac{d\psi_P}{d(V_{GB})}\right)_f + \left(\frac{d\psi_S}{d(V_{GB})}\right)_f + \left(\frac{dV_S}{d(V_{GB})}\right)_f - 1\right)} \quad \text{Eq. (2.4)}$$

$$x_T = \frac{T_{ox}\left(\frac{kT}{q}\left(\frac{d\ln\frac{\tau_c}{\tau_e}}{d(V_{GB})}\right)_r + \left(\frac{d\psi_S}{d(V_{GB})}\right)_r\right)}{\left(\left(\frac{dV_{C\_reverse}}{d(V_{GB})}\right)_r + \left(\frac{d\psi_p}{d(V_{GB})}\right)_r + \left(\frac{d\psi_S}{d(V_{GB})}\right)_r + \left(\frac{dV_S}{d(V_{GB})}\right)_r - 1\right)} \quad \text{Eq. (2.5)}$$

where, $V_{C\_forward}$ is the channel potential of a selected cell when selected BL and common source line (CSL) are biased to V_{CC} and ground, respectively, and $V_{C\_reverse}$ is the channel potential of a selected cell when selected BL and common source line (CSL) are biased to ground and V_{CC}, respectively. Here, $V_{C\_forward}$ and $V_{C\_reverse}$ can express as $[y_T\{V_D\text{-}I_D(R_S+R_D)\}]/L_{eff}$ and $[(L_{eff}\text{-}y_T)\{V_D\text{-}I_D(R_S+R_D)\}]/L_{eff}$, respectively. So, we can obtain accurate x_T and y_T by solving these simultaneous equations.

2.4 Verification of proposed equations

To verify clearly the effect of source potential variation (dV_S/dV_{GB}) and channel potential variation (dV_C/dV_{GB}) with gate bias, two resistors (R_S, R_D = 20 kΩ) are connected to the drain and the source of an MOSFET (test device), respectively. The test device has L and W of 110 nm and 130 nm, respectively, and 2.5 nm thick SiO_2 as a gate insulator. Fig. 2.5 shows the changes of slope of $\ln(\tau_c/\tau_e)$ with respect to gate bias ($d\ln(\tau_c/\tau_e)/dV_{GB}$) in the test device. Solid symbols and open symbols stand for the value of $\ln(\tau_c/\tau_e)$ in the device with and without the resistors, respectively. Square symbols and circle symbols represent the value of $\ln(\tau_c/\tau_e)$ with the forward and reverse drain biases, respectively. When the resistors are connected to the test device, $d\ln(\tau_c/\tau_e)/dV_{GB}$s with the forward and reverse drain bias are changed as shown in Fig. 2.5. In Fig. 2.6, the $d\ln(\tau_c/\tau_e)/dV_{GB}$ with the forward and reverse BL bias also changes in a cell of 48nm NAND flash memory string. From the results of Fig. 2.5 and Fig. 2.6, we can notice that the slope of $\ln(\tau_c/\tau_e)$ are changed due to source potential variation and channel potential since $d\ln(\tau_c/\tau_e)/dV_{GB}$ is a dominant parameter to extract the trap profile. So, the resistance effect should be considered when the trap profiles are extracted in a NAND flash memory string.

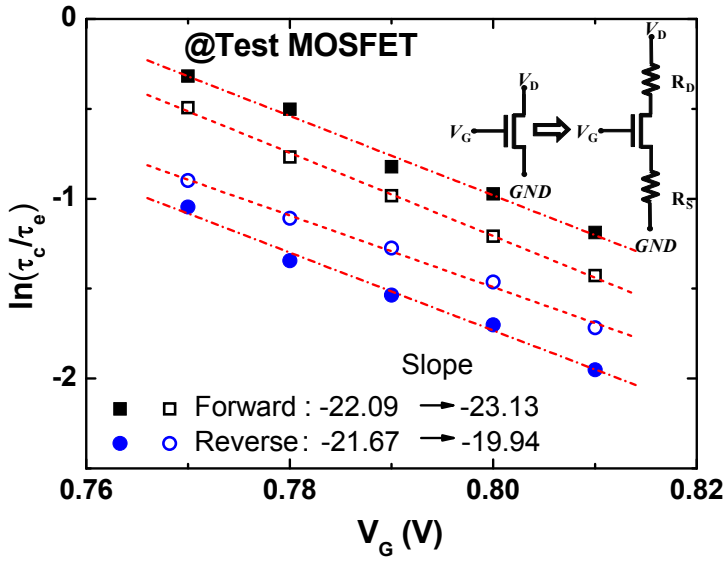


Fig. 2.5. Changes of $d\ln(\tau_c/\tau_e)/dV_{GB}$ in a test MOSFET with and without series resistors.

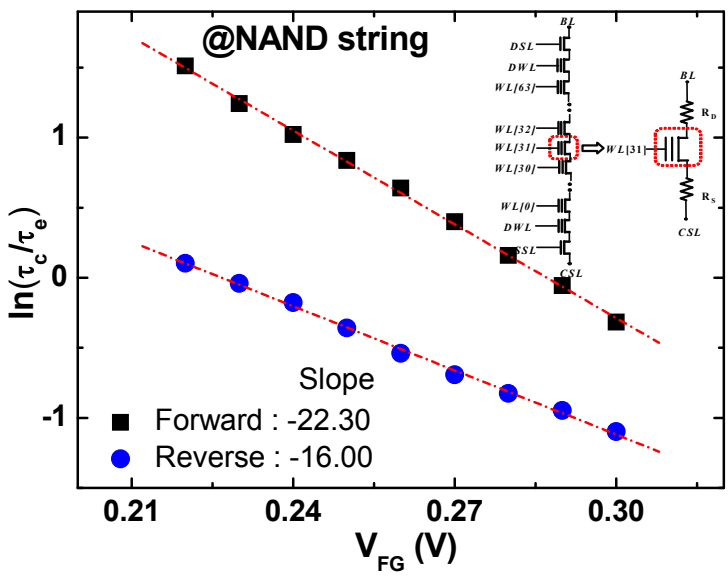


Fig. 2.6. Changes of $d\ln(\tau_c/\tau_e)/dV_{GB}$ in a cell of a NAND cell string with forward and reverse BL-bias.

Figs. 2.7 and 2.8 compare x_T, y_T and E_{COX}-E_T extracted from conventional and proposed equations, respectively, in the test device with and without the resistors. The reference (exact) values are extracted by using conventional equation when Rs and R_D are not connected to the test device. As shown in Figs. 2.7 and 2.8, x_T, y_T and E_{COX}-E_T extracted by using proposed equations are more accurate than those from conventional equation. Thus we verified proposed equations are more accurate. Finally, Figs. 2.9 and 2.10 compare x_T, y_T and E_{COX}-E_T obtained from conventional and proposed equations in NAND flash memory strings.

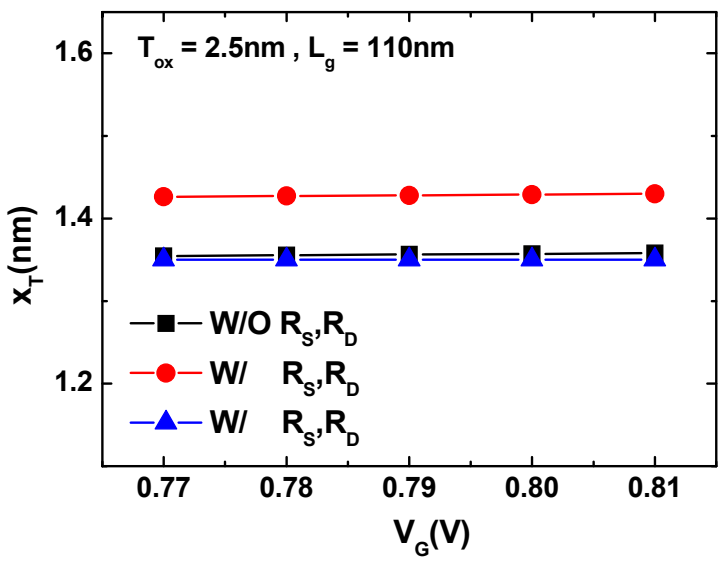


Fig. 2.7. x_T extracted from conventional and proposed equation in a test MOSFET.

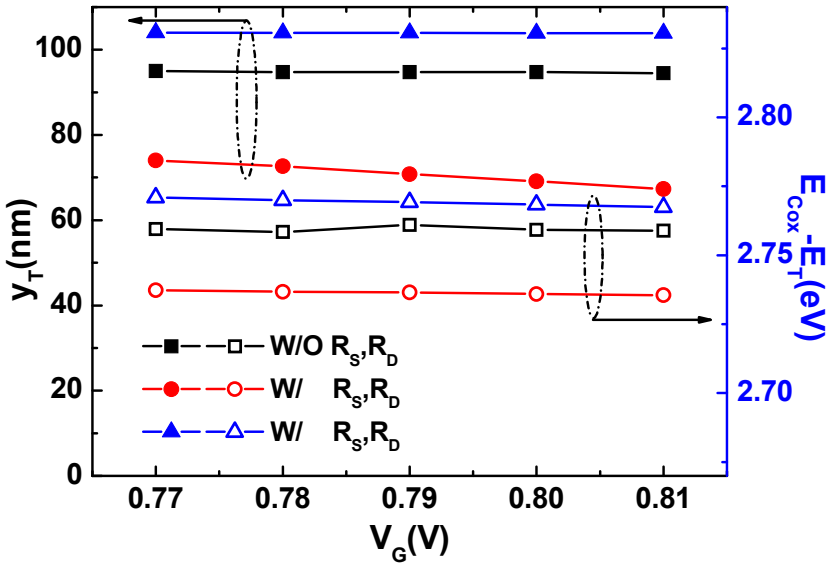


Fig. 2.8. y_T and E_{COX}-E_T extracted from conventional and proposed equations in a test MOSFET.

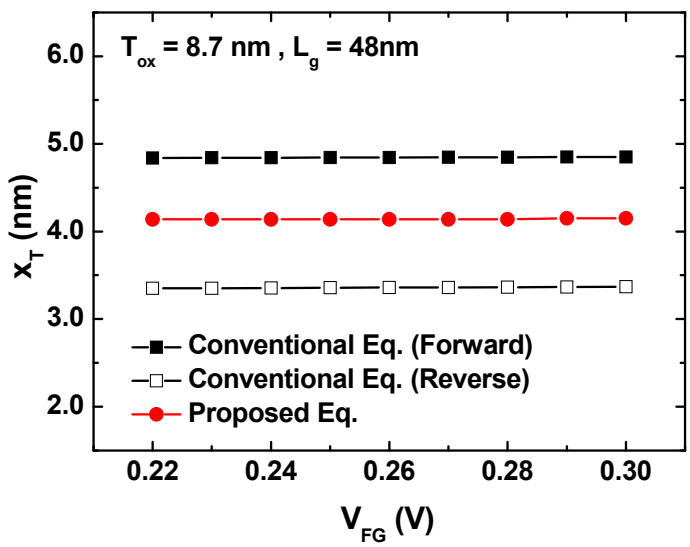


Fig. 2.9. x_T extracted from conventional and proposed equation in a 48nm NAND flash memory string.

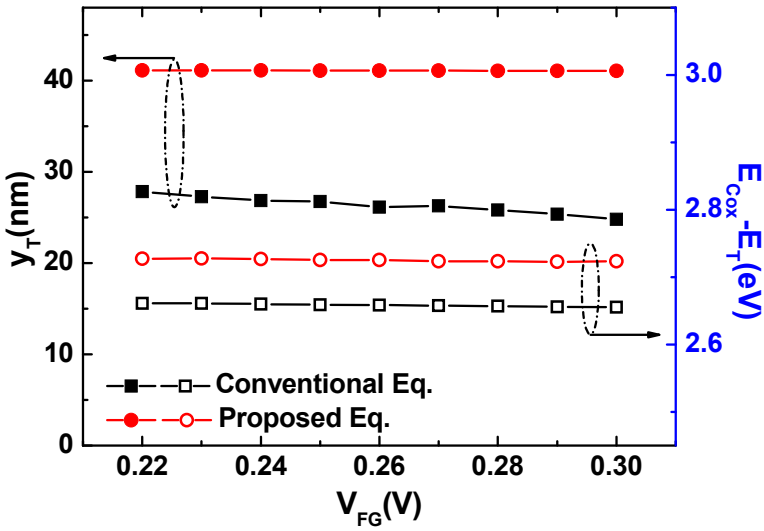


Fig. 2.10. y_T and E_{COX}-E_T extracted from conventional and proposed equations in a 48nm NAND flash memory string.

2.5 Distribution of trap positions in tunneling oxide of NAND flash memory

It is meaningful to study the distribution of position of traps responsible for RTN. We extracted the position of traps (x_T, y_T) by using the proposed equations. Fig. 2.11 shows the extracted x_T and y_T from process induced traps with 30 samples. We understand the traps are roughly located around both edges of the channel because of double etch damage during the fabrication and the negative charge buildup on the sidewall of the dielectric due to the ion sheath during the etch process, resulting in the bent of the trajectories of ions and their bombardment on the sidewall [12].

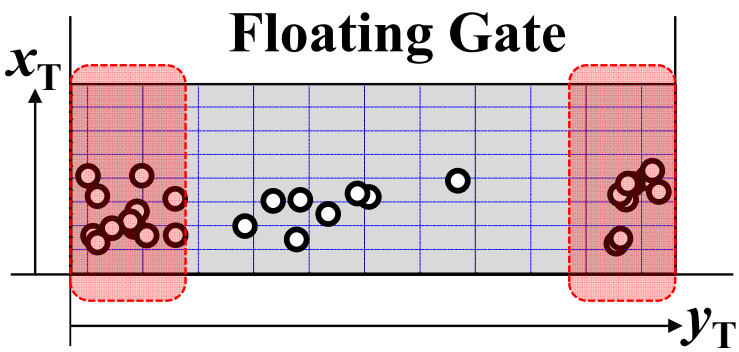


Fig. 2.11 Distribution of extracted trap position (x_T, y_T) of process induced traps in the tunneling oxide.

Chapter 3

Effect of bit-line interference on RTN in NAND flash memory

3.1 Introduction

In a previous section, we introduced a methodology to extract the trap position by considering the effect of series channel resistance of pass cells. In this section, we focus on a detailed explanation about the effect of adjacent BL cell interference on a read cell by using 3-D TCAD simulation, and also measure the bit-line current fluctuation (ΔI_{BL}= high I_{BL} – low I_{BL}) due to RTN of a read cell in a NAND flash cell string by changing state (program (P) or erase (E)) of adjacent BL cells in the word-line (WL) direction. In addition, we investigate the effect of adjacent BL cell interference on the relationship between ΔI_{BL} and the ratio of mean capture and emission time constants ($\ln(\tau_c/\tau_e)$).

3.2 Device structure and simulation condition

The floating-gate NAND flash memory in this work was fabricated at a semiconductor company by applying 32 nm technology and has the same structure as mentioned in the chapter 2. For 3-dimensional (3-D) device simulation, a NAND flash memory cell array which consists of one word-line (WL) and 3 BLs was prepared to have the same structure as the measured device. The cells in the simulation have channel length and width of 32 nm, tunneling oxide thickness of 7.9 nm, constant channel doping of 2×10^{17} cm^{-3}, and peak source/drain doping of 1×10^{19} cm^{-3}. The simulation data are obtained by solving the Poisson and drift-diffusion equations at the read condition (BL bias (V_{BL})=0.5 V, control-gate bias for an I_{BL} of 100 nA). Although the boron ion segregation depends on the process and following heat cycles, we assumed constant body doping in this work.

3.3 Results of 3-D TCAD simulation

NAND flash memories are influenced by the severe cell-to-cell interference due to increased parasitic capacitances with the continued scaling of NAND flash memory beyond 50 nm [13]-[16]. The effect of adjacent BL cell's state (P or E) on the read cell (BL_n cell) is investigated by using 3-D TCAD simulation.

Since each of adjacent BL cells (BL_{n-1} and BL_{n+1} cells) has P or E state, we can consider four different modes (E/E, E/P, P/E, and P/P). Here, adjacent BL cells are programmed to have a V_{th} of 3 V or erased to have a V_{th} of -3 V. As shown in Fig. 3.1, a part of a control-gate in NAND flash memories is inserted between floating-gates of adjacent BL cells to increase the coupling ratio and minimize the floating -gate interference. And there is the tip effect at the edges in *z*-direction because the corner of the active area is sharp as shown in Fig. 3.1. Therefore the distribution of the electrostatic potential and electron current density (J_e) along the channel width direction (*z*-direction) in the read cell (particularly near the edges in *z*-direction) are influenced not only by the electric field from the floating-gate of adjacent BL cells but also by that from the recessed control-gate and the tip effect [17]. Before discussing the effect of adjacent BL cell's state on a read cell, we need to investigate the effect of the electric-field from the recessed control-gate on the read cell. To see the effect, the distribution of electrostatic potential and J_e in a read cell was checked by changing the state of adjacent BL cells. Fig. 3.1 shows simulation results depicting the electrostatic potential and J_e of a read cell when adjacent BL cells are in a fresh state (zero net charge in the floating-gate) or E/P mode. Here, the read cell was controlled to have a V_{th} of nearly 0 V by which a WL bias of 0 V is applied to the control-gate of the read and two adjacent BL cells during read operation. By doing so, the electric field from the recessed control-gate can be

minimized, which minimizes the channel modulation of the read cell. Consequently, we can observe clearly the effect of the state of adjacent BL cells. The distribution of electrostatic potential and J_e is extracted at 1 Å below the channel surface along the *z*-direction when I_{BL} is 100 nA at a given BL bias (V_{BL}) of 0.5 V. As shown in Fig. 3.1, the J_e and electrostatic potential at the channel edge region are slightly increased due to the tip effect and the effect of the electric field from the recessed control-gate when adjacent BL cells are in a fresh state. But, we can notice that the electric field from the floating-gate of adjacent BL cells is more dominant by comparing the electrostatic potential and J_e in the fresh state with those in E/P mode when a V_{th} of the read cell is nearly 0 V [16].

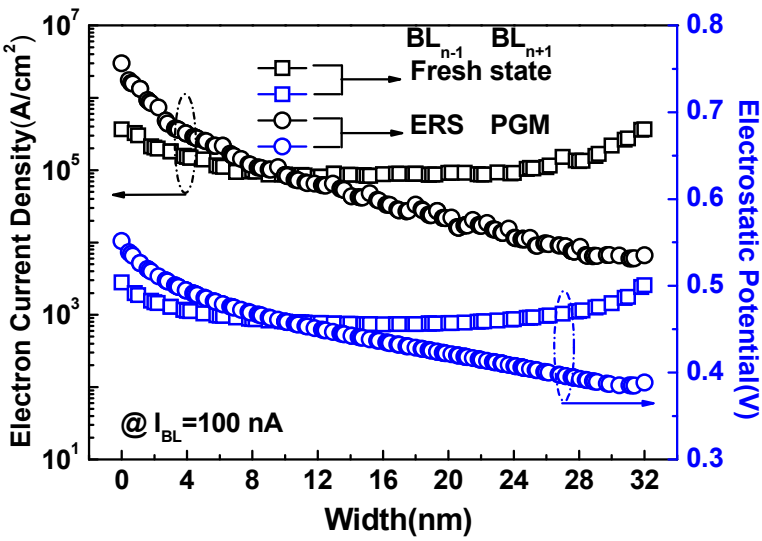


Fig. 3.1. Simulated electrostatic potential and J_e of a read cell along the channel width (*z*) direction when adjacent BL cells are in a fresh state or in E/P mode, respectively.

Fig. 3.2 shows the simulated distribution of J_e along the z-direction with 4 different modes of the state of adjacent BL cells. Each distribution of J_e is extracted at 1 Å below the surface along the z-direction when I_{BL} is 100 nA at a given V_{BL} of 0.5 V. From the results of Fig. 3.2, J_e along z-direction in a read cell is changed significantly with the state of adjacent BL cells. Since the distance between the channel of a read cell and the floating-gate of adjacent BL cells is so close, the distribution of J_e along the z-direction in the read cell is directly changed by the electric field from the floating-gate of adjacent BL cells when adjacent BL cells are programmed or erased [13]-[17]. For example, J_e of a read cell is crowded toward the BL_{n-1} side (a position from the center to the left edge of the channel width) in z-direction as shown by open triangles in Fig. 3.2 when BL_{n-1} and BL_{n+1} cells are erased and programmed, respectively.

Fig. 3.3 (a) and (b) show the distribution of J_e without and with a trapped electron in E/P state as an example, respectively. Here, the trap position from the channel surface to the floating-gate (x_T), the trap position along the channel length direction (y_T), and a trap position along the channel width direction (z_T) are 1 Å, 16 nm, and 4nm, respectively. Bias conditions in Fig. 3.3 are exactly the same as those in Fig. 3.2. When an electron is captured into a trap in the tunneling oxide, J_e under a trapped electron decreases dramatically as shown in Fig. 3.3 (b), which leads to the decrease of I_{BL}.

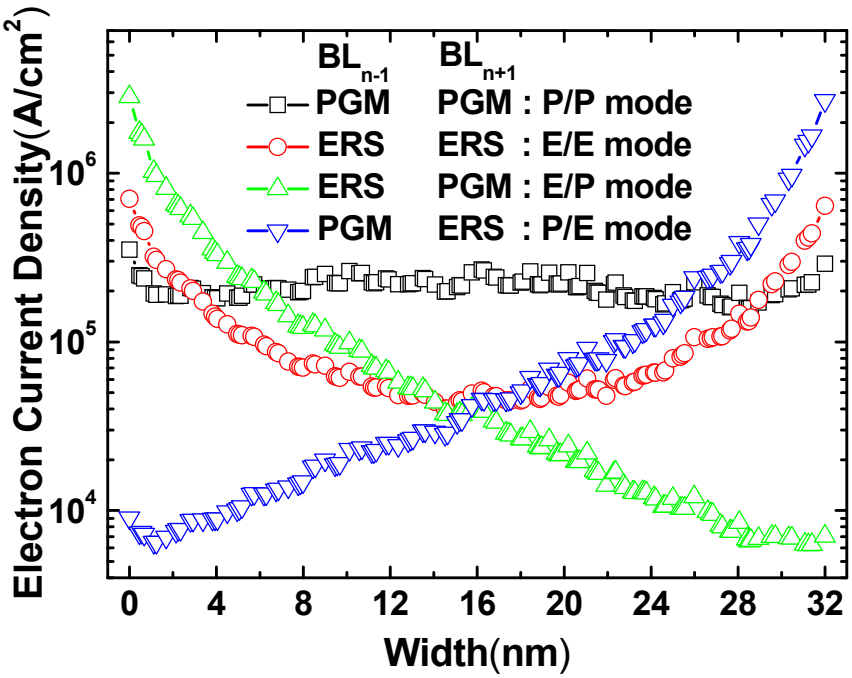


Fig. 3.2. Simulated distribution of J_e along the z-direction with four different modes of the state of adjacent BL cells. Each distribution of J_e is extracted at 1 Å below from the channel surface along the z-direction.

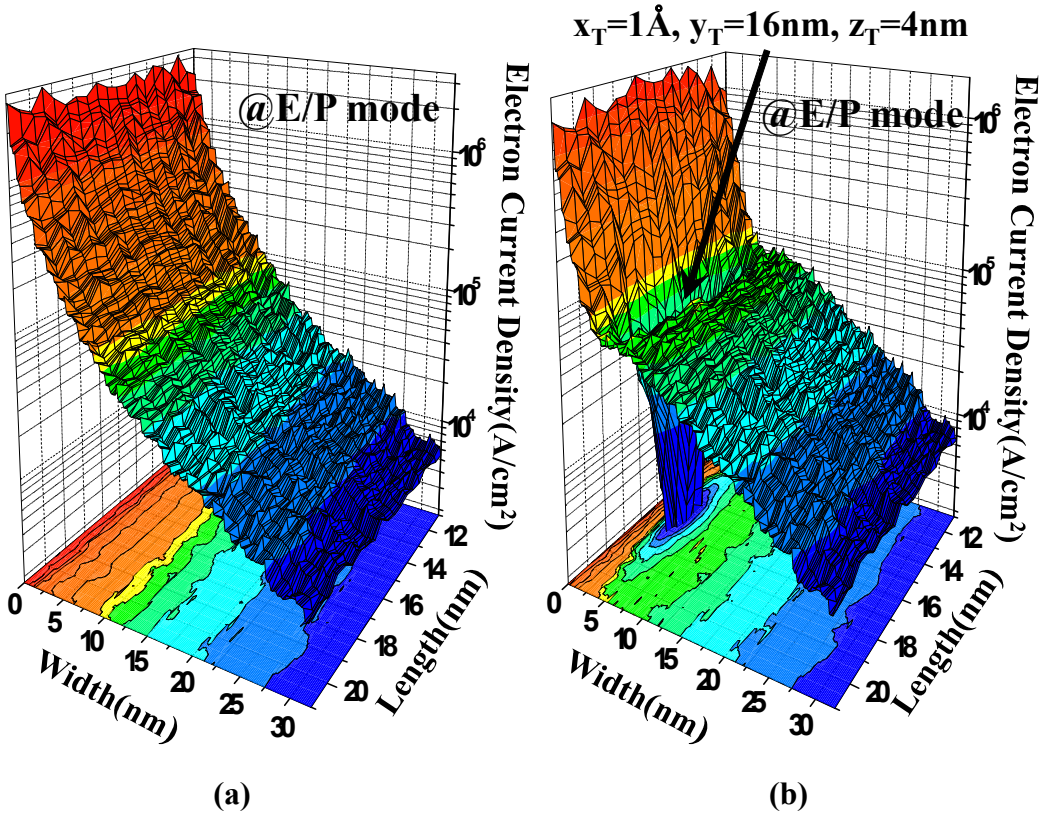


Fig. 3.3. Simulated distribution of J_e (a) without and (b) with an electron trap in the tunneling oxide when adjacent BL cells are in E/P mode. Here, x_T, y_T, and z_T are 1 Å, 16 nm, and 4 nm, respectively. J_e is extracted at 1 Å below from the channel surface along the z-direction.

Fig. 3.4 (a) and (b) show the change of simulated ΔI_{BL} with z_T as a parameter of the state of adjacent BL cells when x_T is 1 Å and 3 nm, respectively. The ΔI_{BL}s are obtained at an I_{BL} of 100 nA. Bias conditions are exactly the same as those in Fig. 3.2. From the results of Figs. 3.2 and 3.4, we can understand that an electron trap existing above higher J_e region gives the larger ΔI_{BL} at a fixed x_T. A trap located closer to the surface makes the larger ΔI_{BL} at a fixed z_T. Thus the state of adjacent BL cells can control a sort of percolation path (~high J_e region) along z-direction and the ΔI_{BL} of a read cell becomes a maximum value when the path is aligned to z_T. There were several reports that a trap which is closely located above a percolation path increases the amplitude of RTN [18]-[19]. For example, when an electron trap is located near z_T of 0 nm, the E/P mode gives much larger ΔI_{BL} than the P/E mode because E/P mode makes a percolation path near z_T of 0 nm as shown by open triangles in Fig. 3.2. Furthermore, the effect of random dopant fluctuations (RDF) which leads to the percolation path in the channel has been studied by using the "atomistic" doping method and the RDF is the important to analyze the characteristics of RTN in the nano-scale devices. [20], [21]. Because the simulation was done with the continuous doping in this work, the distribution of ΔI_{BL}s as shown in Fig. 3.4 can be changed if we include the effect of RDF. We predict that maximum ΔI_{BL} for each mode will be increased when the effect of adjacent bit-line interference is superimposed on the effect of RDF.

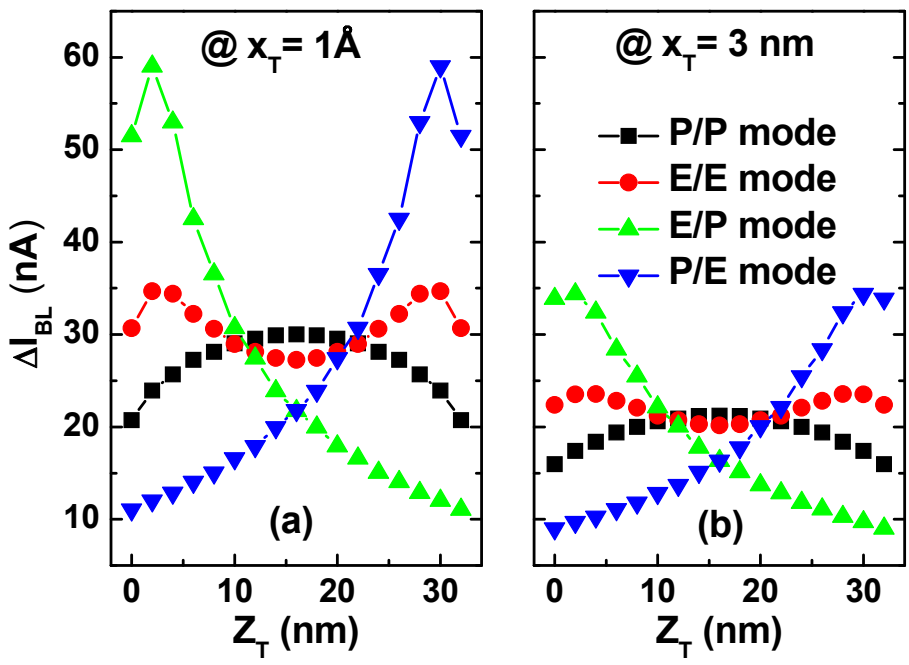
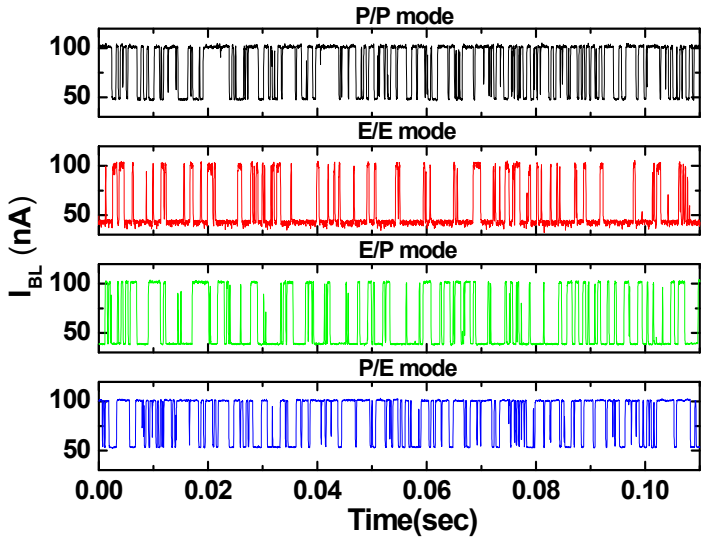


Fig. 3.4. Simulated ΔI_{BL} with a trap position (z_T) along the z-direction as a parameter of the state of adjacent BL cells when the trap position (x_T) from the channel surface to the floating-gate is 1 Å (a) and 3 nm (b).

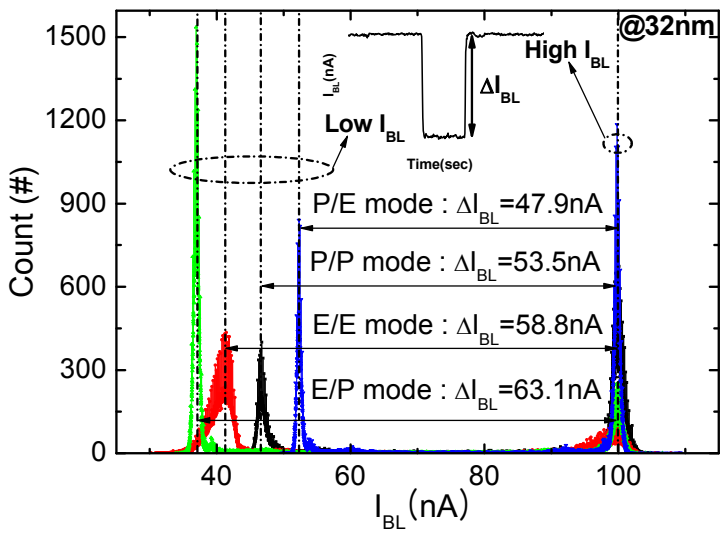
3.4 RTN measurement results with the state of adjacent bit-line cells

Fig. 3.5 shows an example of measured ΔI_{BL} with the state of adjacent BL cells in a 32 nm NAND flash memory cell string. Fig. 3.5 (a) shows the ΔI_{BL} of a

read cell with 4 different modes of the state of adjacent BL cells in time domain. Fig. 3.5 (b) shows the distribution of ΔI_{BL} extracted from the results of Fig. 3.5 (a). The inset of Fig. 3.5 (b) represents a part of measured RTN waveform where the low I_{BL} is changed with the state of adjacent BL cells. Here, low and high I_{BL}s correspond to the capture and emission of an electron at a trap, respectively. To observe the effect of adjacent BL cell interference on ΔI_{BL} due to RTN, the adjacent BL cells are programmed to have a V_{th} of 3 V or erased to have a V_{th} of -3 V. The read cell is set to have a V_{th} of 0 V. Here, high I_{BL} was fixed at 100 nA by controlling the control-gate bias of the read cell at a V_{BL} of 0.8 V and a pass bias (V_{pass}) of 6.5 V. In this example, ΔI_{BL} due to RTN ranges from ~48 nA to ~63 nA with 4 different modes of the state of adjacent BL cells. From the result in Fig. 3.5, ΔI_{BL} increases by about 30 % when the mode of adjacent BL cells is changed from P/E mode to E/P mode. We can notice that the trap responsible for the ΔI_{BL} behavior in Fig. 3.5 is estimated roughly to be located near the BL_{n-1} side in *z*-direction by considering the results of Figs. 3.4 and 3.5. As the cell size scales down further, the change of ΔI_{BL} would be more severe due to the increased interference of adjacent BL cell when the state of adjacent BL cells changes.



(a)



(b)

Fig. 3.5. (a) Measured ΔI_{BL} of a read cell with four different modes of the state of adjacent BL cells in time domain and (b) distribution of ΔI_{BL} extracted from the results of Fig. 3.5 (a).

Fig. 3.6 shows the ΔI_{BL} relationship between E/P and P/E modes extracted from 33 cells in 32 nm NAND flash memory strings. The strength of color of circular symbol shows the $\Delta\ln(\tau_c/\tau_e)$, which is to subtract the $\ln(\tau_c/\tau_e)$ in P/E mode from that in E/P mode. Bias condition for measurement is the same as that mentioned in Fig. 3.5. The dashed line represents the point where the ΔI_{BL}s in E/P and P/E modes are the same. For example, a symbol is located below the dashed line when the ΔI_{BL} in E/P mode is larger than that in P/E mode. By comparing the simulation result in Fig. 3.4 with the measured result in Fig. 3.6, we can notice that the percolation path exists in the channel of cells due to the intrinsic parameter fluctuation [22]. At least, the cells showing more than ~60 nA are affected by the percolation path. In Fig. 3.6, the strength of color of symbols below the dashed line is generally bright, which means the $\ln(\tau_c/\tau_e)$s in P/E mode are larger than those in E/P mode. From the result of Fig. 3.6, we can notice that the correlation between the ΔI_{BL} and $\ln(\tau_c/\tau_e)$ obviously exists with changing the state of adjacent BL cells.

For more detailed explanation of the results of Fig. 3.6, we prepared RTN of a read cell for both E/P and P/E modes as shown in Fig. 3.7. Bias condition for measurement is the same as those mentioned in Fig. 3.5. Here, ΔI_{BL}s in E/P mode and P/E modes are 32 nA and 26 nA, respectively. When the state of adjacent BL cells changes from E/P mode to P/E mode, $\ln(\tau_c/\tau_e)$ changes from 1.20 to 5.99. These results will be explained as follows. By considering the

results of Figs. 3.4 and 3.7, we can estimate that a trap which generates RTN in Fig. 3.7 is located near the BL_{n-1} side in *z*-direction.

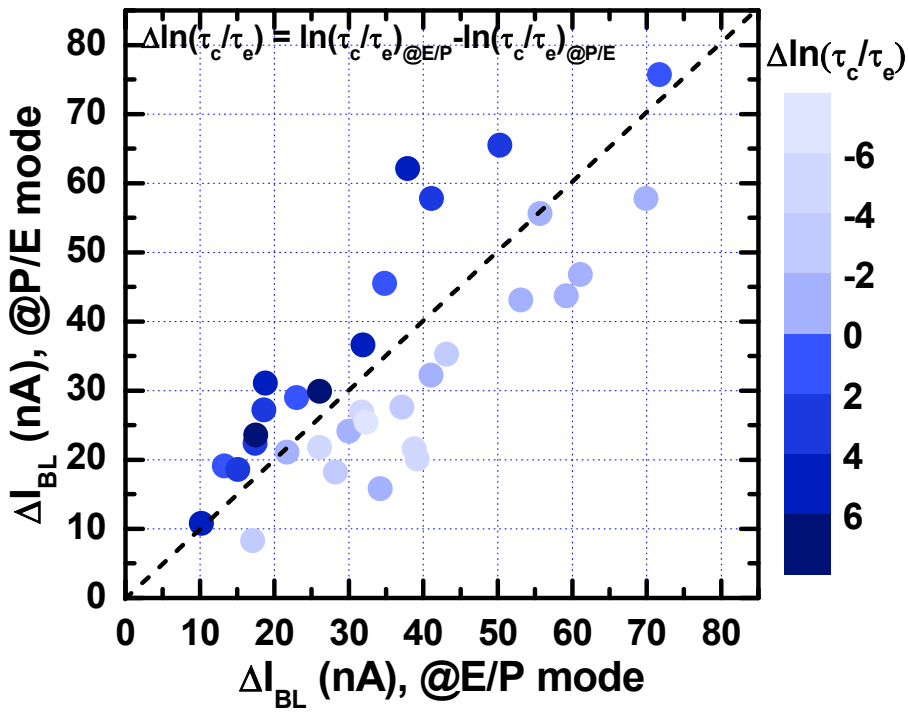


Fig. 3.6. ΔI_{BL} relationship between E/P and P/E modes extracted from 33 cells in 32 nm NAND flash memory strings. The strength of color of circular symbol shows the $\Delta\ln(\tau_c/\tau_e)$, which is to subtract the $\ln(\tau_c/\tau_e)$ in P/E mode from that in E/P mode. The dashed line represents the point where the ΔI_{BL}s in E/P mode and P/E mode are the same.

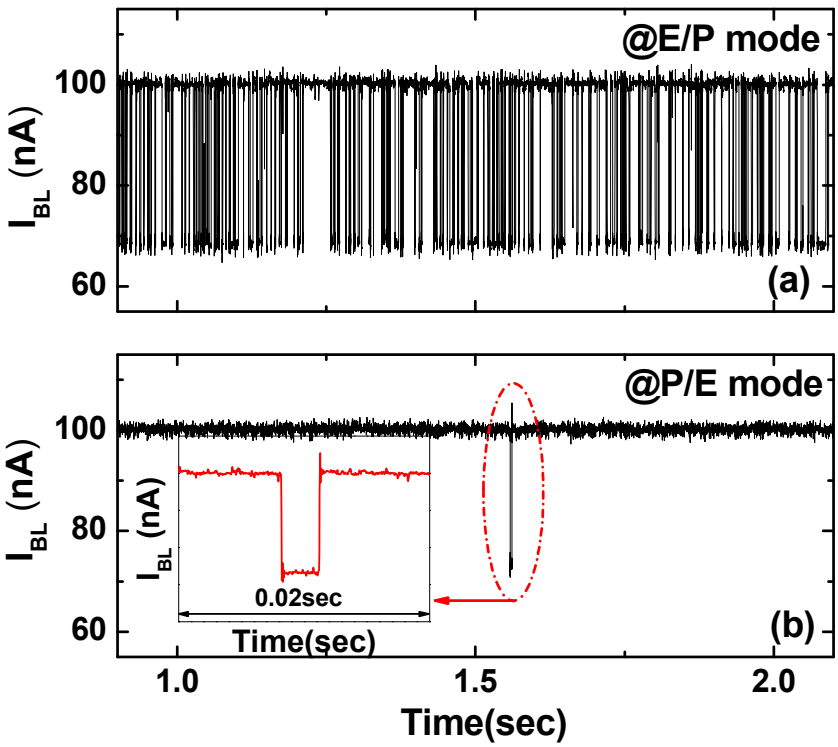


Fig. 3.7. Measured ΔI_{BL} due to RTN in the time domain when a read cell is in (a)E/P mode and (b) P/E mode, respectively. The inset of Fig. 3.7 (b) shows the magnified I_{BL} versus time.

In order to explain this more detail, we prepare the energy band diagram of a read cell cut along A-A' (closer to BL_{n-1}) in the inset of Fig. 3.8 when the read cell is in E/P and P/E modes as shown in Fig. 3.8. Here, V_{BL} of the read cell is 0.5 V and I_{BL} is adjusted to have 100 nA by controlling V_{CG} (V_{CG}=0.47 V) in both cases. In Fig. 3.8, the conduction and valence bands of the read cell in E/P

mode are more bended than those in P/E mode due to the increased electric field from the floating-gate of erased adjacent cell (BL_{n-1} cell). Thus, the electric field from the floating-gate of adjacent BL cell has an direct influence on the difference between the trap energy level (E_T) and the Fermi level (E_F), which leads to the change of $\ln(\tau_c/\tau_e)$. In this cell, E_T is quite close to E_F in E/P mode (E_T - E_F ≈31 meV), but higher than E_F in P/E mode (E_T - E_F ≈156 meV). This change of $\ln(\tau_c/\tau_e)$ due to the state of adjacent BL cells can lead to the significant error in NAND flash memory strings. Before shipping out NAND flash memories, failure tests, which is to check program or erase operation, charge loss, the distribution of V_{th}, and etc should be done in the security block which stores the error correction code (ECC). In the case of Fig. 3.7, the capture event occurs much less frequently in P/E mode, which means that it is hard to detect the failed cell in the security block during the failure tests. From these results, it can be understood that the state of adjacent BL cells affects ΔI_{BL} and $\ln(\tau_c/\tau_e)$ in a cell at the same time. We can also roughly estimate z_T by using not only the behavior of ΔI_{BL} but also the behavior of $\ln(\tau_c/\tau_e)$. When we correct the failed cells, it is needed to consider both ΔI_{BL} and $\ln(\tau_c/\tau_e)$ of the RTN, which are affected by the states of adjacent BL cells.

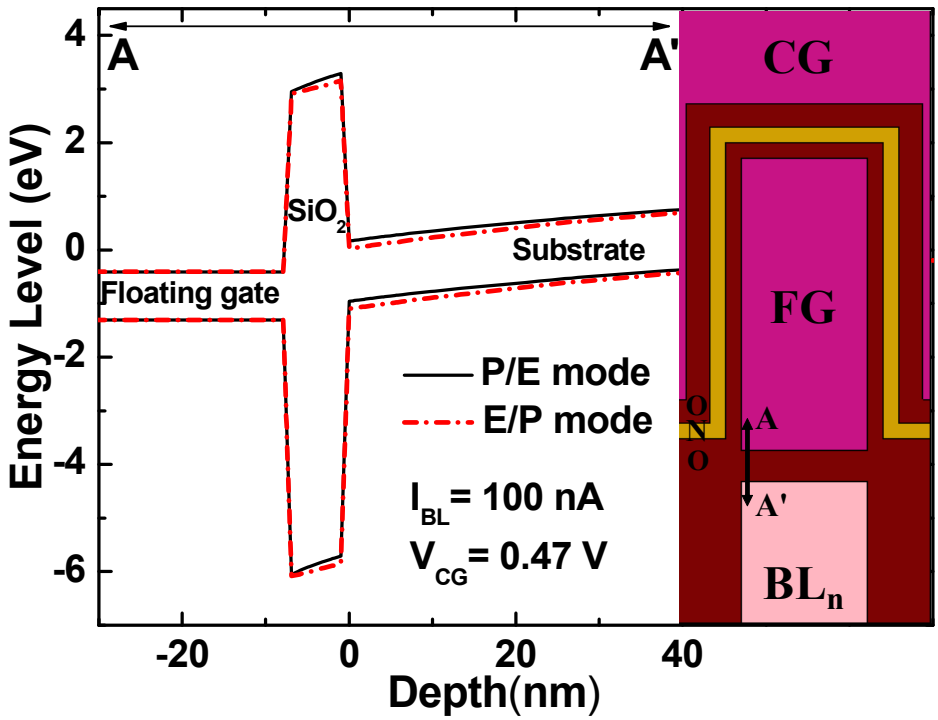


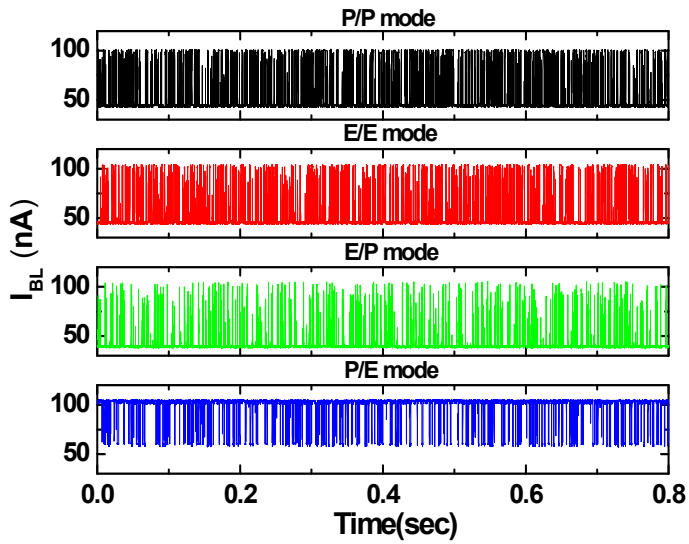
Fig. 3.8. Energy band diagram of a read cell cut along A-A' in the inset when the read cell is in E/P mode and P/E mode. The dash-dot line represents the diagram in E/P mode. The inset shows the simulation structure.

3.5 3-D trap position in tunneling oxide

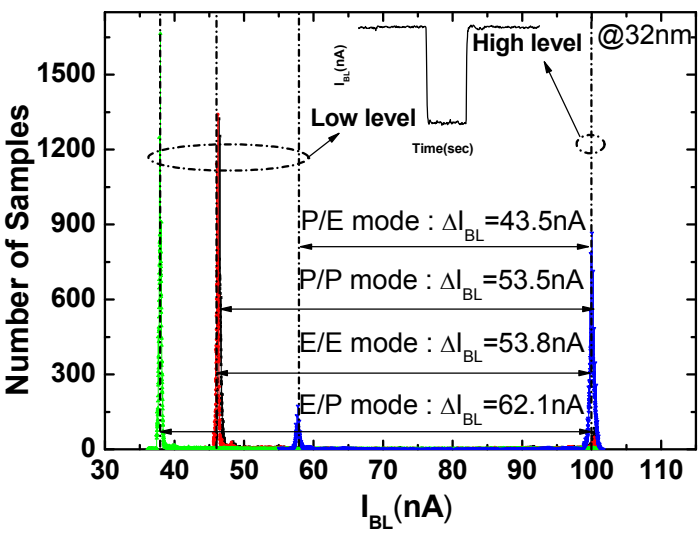
As mentioned in the section 3.4, the state of adjacent BL cells affects ΔI_{BL} due to RTN, which can be a key fingerprint to extract z_T. When the adjacent cells are programmed or erased, J_e distribution is changed along the z direction of the

read cell by bit-line interference. When a single electron is trapped at 1 Å from the channel surface, J_e under the trapped electron is changed dramatically. Due to the variation of J_e distribution with the states of adjacent cells, the ΔI_{BL} due to RTN in the read cell is affected at I_{BL}. Here, the changes of ΔI_{BL} with the state of adjacent cells, x_T, and z_T are shown in Fig. 3.4. As shown in Fig. 3.3 and 3.4, a trapped electron inside the tunnel oxide existing above higher J_e region gives the larger ΔI_{BL}. For example, when a trapped electron is located near both edges of the channel width in E/P mode, the ΔI_{BL} for z_T~0 nm is the larger than that near z_T~32 nm due to asymmetric J_e distribution as shown by solid inverse triangles in Fig. 3.2. Comparing the result of Fig.3.4 with Fig. 3.9, the z_T in this example can be roughly extracted (~8 nm).

By using the proposal equation as mentioned in the chapter 2 and the effect of adjacent bit-line interference, 3-D trap position can be extracted in NAND flash memory strings as shown in Fig. 3.10.

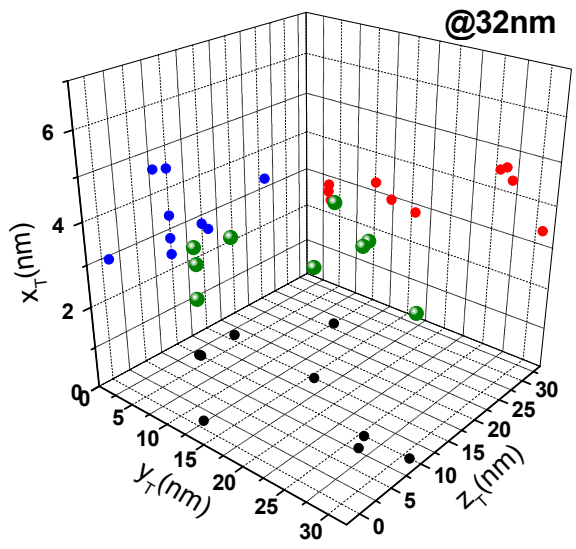


(a)

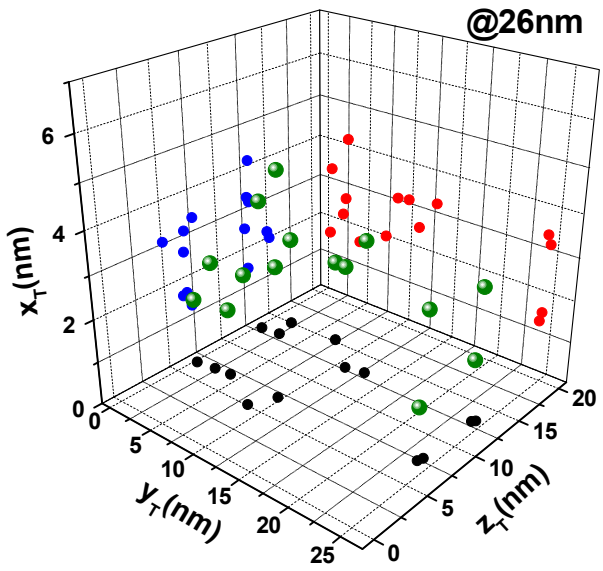


(b)

Fig. 3.9. (a) Measured ΔI_{BL} of a read cell with four different modes of the state of adjacent BL cells in time domain and (b) distribution of ΔI_{BL} extracted from the results of Fig. 3.9 (a).



(a)



(b)

Fig. 3.10. Distribution of extracted x_T, y_T and z_T of traps in the tunneling oxide of (a) 32 nm and (b) 26 nm NAND flash memories (big dots). Small dots represent projected trap position on each plane (ex: y_T-z_T)

Chapter 4

A new read method suppressing random telegraph noise

4.1 Introduction

As mentioned in the chapter 2 and 3, Random telegraph noise (RTN) caused by electron capture/ emission at traps has been an issue as the device cell size scales down. The current fluctuation due to RTN can make serious problems, such as wide V_{TH} distribution and device instability. Especially, tight control of V_{TH} distribution of multi- level cell (MLC) NAND flash memory device is very important. There have been some reports to extract the position of trap generating RTN and to investigate current behavior with temperature (T) and gate bias [9], [23]. It is the best way to suppress completely the RTN so that we can reduce V_{th} distribution greatly. However, there has been no report on a method to reduce or suppress RTN during read operation. In this work, we propose a new gate biasing scheme to read bit-line current (I_{BL}) during read

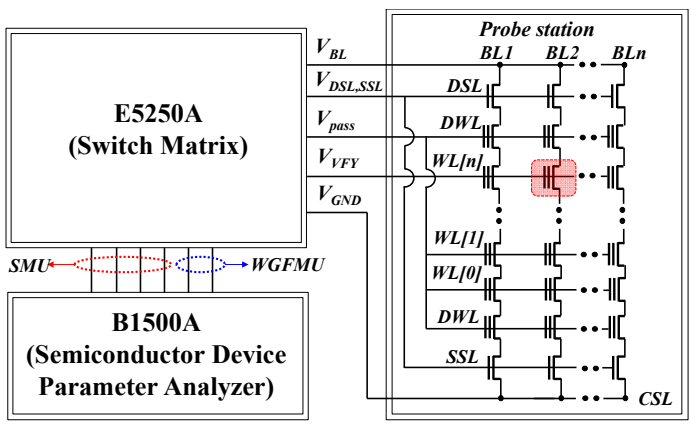
operation with extremely low probability of RTN, and investigate the RTN behavior for three different RTN cases.

4.2 Device structure and measurement setup

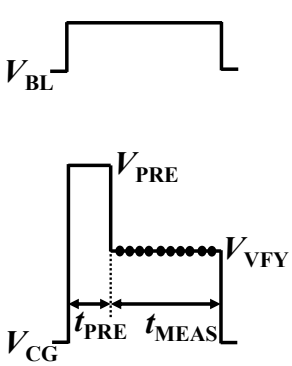
The floating-gate NAND flash memory in this work was fabricated at a semiconductor company by applying 26 nm technology. The NAND flash memory string consists of sixty-four unit cells, two dummy cells, a drain select line (DSL) transistor and a source select line (SSL) transistor.

Since NAND flash memory strings actually are biased under dynamic signals during the short operation time (~μs), it is appropriate to measure the electrical properties of trap in a short time. In order to observe the behavior of trap in a short time, the I_{BL} is set to be measured in ~μs by using WGFMU modules that integrates arbitrary linear waveform generation capability with high-speed current and voltage measurement. The block diagram of pulsed *I-V* and fast transient I_{BL} measurement system is represented in Fig. 4.1 (a). To show the transient characteristic by adopting proposed reading method, the pulse waveform in Fig. 4.1 (b) is used. The V_{PRE} was applied to the control gate of a selected cell for t_{PRE} before read operation and then I_{BL} is measured at a V_{VFY} for t_{MEAS}. I_{BL} is measured by 1k times according to the method in Fig. 4.1 (c). A V_{read} is applied right after V_{PRE} is applied, and I_{BL} is sampled for 1μs after t_{delay}.

The I_{BL} sampling is repeated by 1k times. Fig. 4.1 (d) shows the pulse waveform to measure pulsed *I-V*. The V_{PRE} is applied to the control gate for t_{PRE} before applying a sweep voltage (V_{sweep}). Then, the V_{sweep} is applied and I_{BL} is sampled. Here, we can control the V_{PRE}, and use V_{PRE}s of -5, 0 and 5V in this work as shown in Fig. 4.1 (d). Since read time is several μs in conventional NAND flash memory, B1530A module is used for measuring I_{BL} and generating gate pulse in μs range.



(a)



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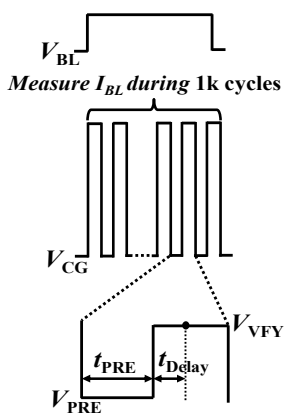


(c)

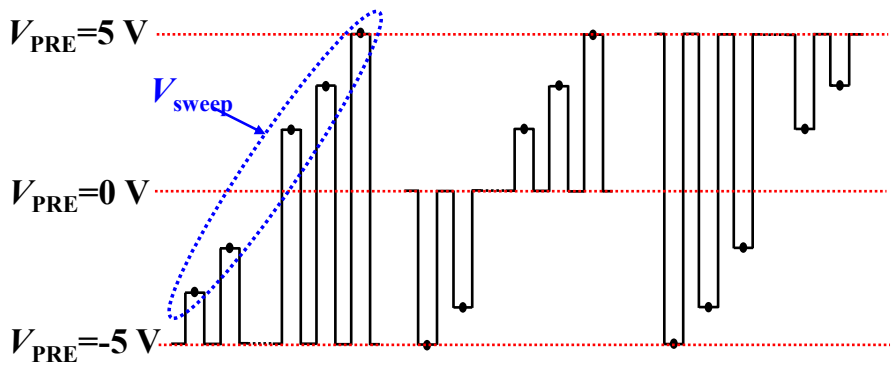
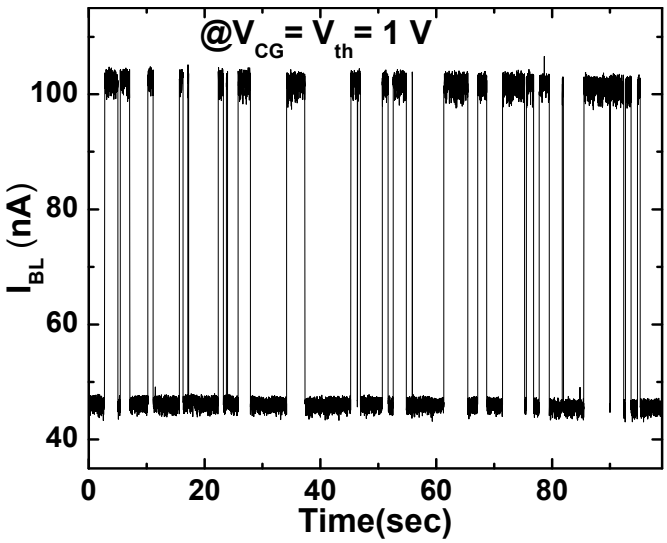


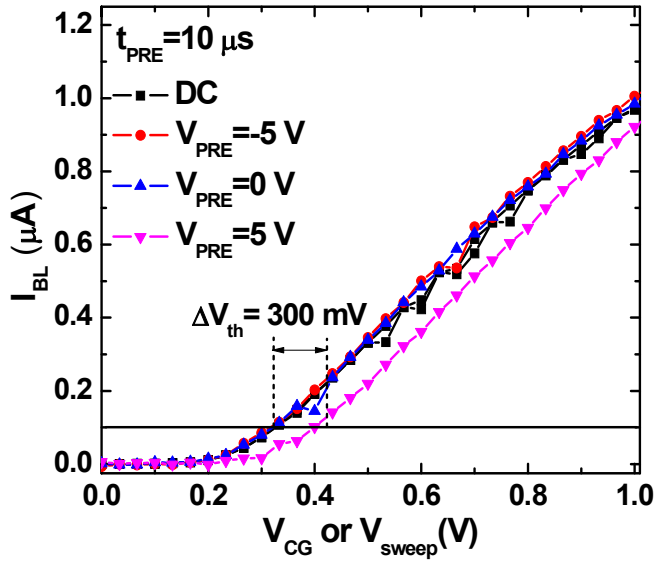
Fig. 4.1. (a) Block diagram of the measurement system. The selected cell is represented by a red square. Pulse waveform of control gate bias voltage (V_{CG}) for (b) transient bit-line current (I_{BL}) measurement, (c) 1k times of I_{BL} sampling at read bias (V_{read}) and (d) pulsed *I-V* measurement.

4.3 Measurement results and discussion

A cell with two level current fluctuation due to RTN shown in Fig. 2 (a) is measured at V_{CG}=V_{VFY}. In Fig. 2 (b), pulsed *I-V* curves show different V_{th}s as V_{PRE} changes due to hysteretic effect of RTN. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. t_{PRE} is 10 μs and V_{PRE} is changed to have -5 V, 0V, and 5 V. When V_{PRE} is 5 V, the V_{th} of a selected cell becomes higher compared to V_{th}s of a selected cell when V_{PRE} is -5 V or 0 V.



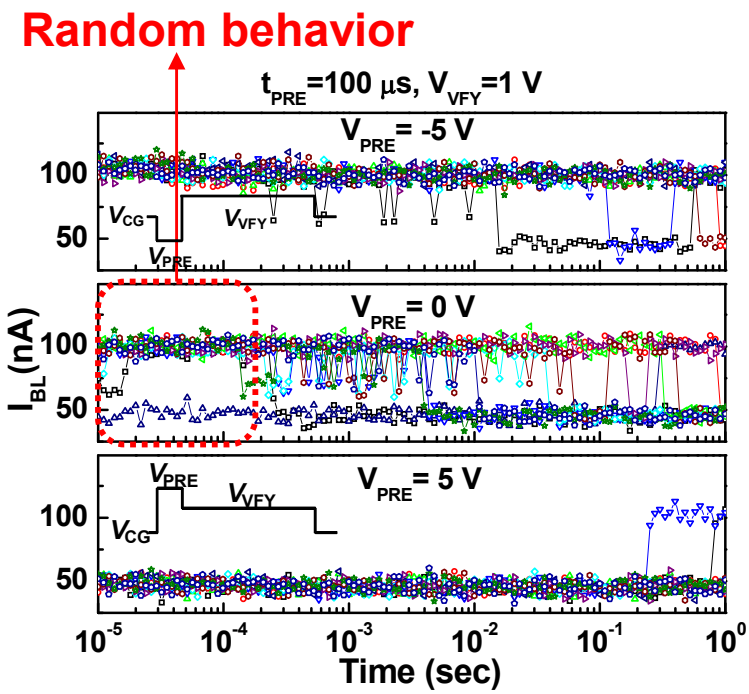
(a)



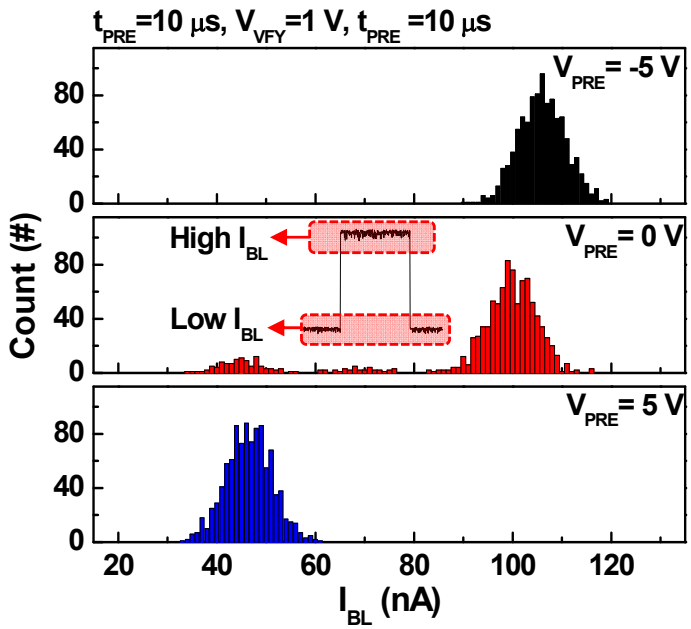
(b)

Fig. 4.2. (a) RTN waveform of I_{BL} (b) DC and pulsed *I-V* curves with pre-bias voltage (V_{PRE}) (-5, 0 and 5 V).

Fig. 4.3 (a) shows transient currents measured by 10 times at V_{PRE}s of -5, 0 and 5V. The inset shows a pulse waveform showing V_{PRE} and V_{VFY} while the pulse is applied to the control gate. Here, t_{PRE} and V_{VFY} is 100 μs and 1 V, respectively. $V_{DSL,SSL}$,V_{pass}, and V_{BL} are same conditions as mentioned in Fig. 4.2. Whereas the high or low level I_{BL} appears randomly at a V_{PRE} of 0 V, only high level and only low level I_{BL} are observed at V_{PRE}s of -5 and 5 V, respectively. Fig. 3 (b) shows histogram of 1k sampled I_{BL}s at three V_{PRE}s of -5, 0, and 5 V. Both t_{PRE} and t_{delay} are 10 μs. At V_{PRE}s of -5 and 5 V, only low or high level I_{BL} distribution is observed. At a V_{PRE} of 0 V, low and high level I_{BL} distributions are observed although frequency count is different.



(a)



(b)

Fig. 3 (a) Transient I_{BL} characteristics after V_{CG} changes from V_{PRE} to V_{VFY}. (b) histogram of 1k sampled I_{BL} with V_{PRE} (-5, 0, 5 V). The inset shows the pulse waveform of V_{CG}.

Proposed read method is applied in three cases related with the E_t position relative to E_f shown in Fig. 4.4. At a V_{CG}=V_{VFY}, cases 1, 2 and 3 represent $E_T \approx E_F$, $E_T > E_F$, and $E_T < E_F$, respectively. Fig. 4.5 (a), (b) and (c) show the RTN waveforms measured in three different cells which represent cases 1, 2, and 3, respectively.

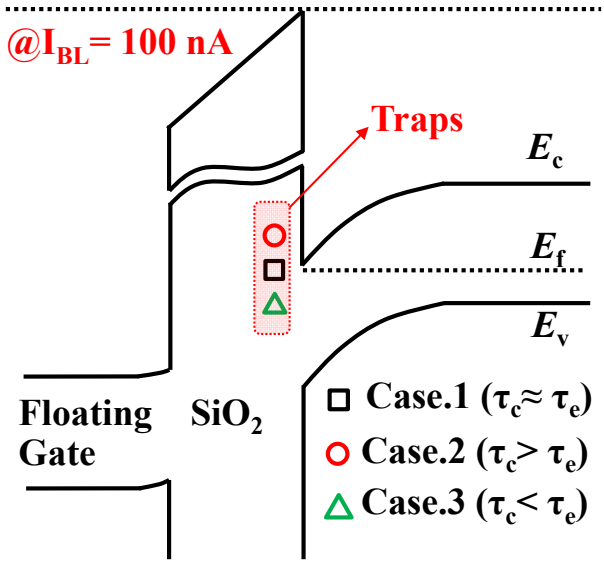


Fig. 4.4. Energy band diagram showing trap energy level (E_t) in tunneling oxide as case 1, 2 and 3 at V_{CG}=V_{VFY}.

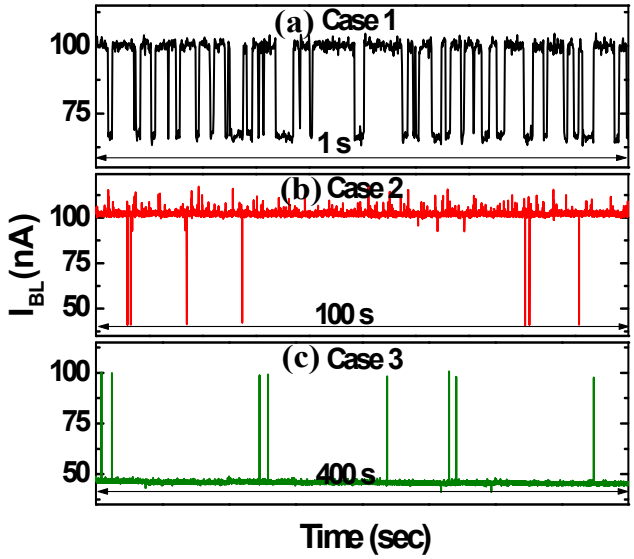


Fig. 4.5. RTN waveforms of I_{BL} at V_{CG}=V_{VFY} in cases (a) 1, (b) 2 and (c) 3. In cases 1, 2 and 3.

Fig. 4.6 shows the pulsed *I-V* curves in three cells which have different V_{th}s with the V_{PRE} in all cells. As the same result in Fig. 4.2, the hysteretic effect of RTN observed in all cases. Fig. 4.7 shows the transient I_{BL} characteristics with V_{PRE} in three cells. Here, transient I_{BL}s were measured by 10 times and for 100 ms at given a V_{PRE}. V_{PRE}s were applied to the control gate for 100 μs.As a result of Fig. 4.7, random fluctuation of I_{BL} disappeared within the short time (~10 μs). Fig. 4,8 show the histogram of 1k sampled I_{BL} with V_{PRE} (-5, 0, and 5 V) in cases (a) 1, (b) 2 and (c) 3. Here, both t_{delay} and t_{PRE} are 10 μs. In three cases of Fig. 4.8, while only high I_{BL} distribution is observed at V_{PRE} = -5 V, only low I_{BL} distribution is observed at 5 V. At a V_{PRE} of 0 V, high and low I_{BL}s are observed randomly. Applying sufficient high or low V_{PRE} before applying V_{VFY} can reduce the effect of RTN in three representative cases regardless of E_T.

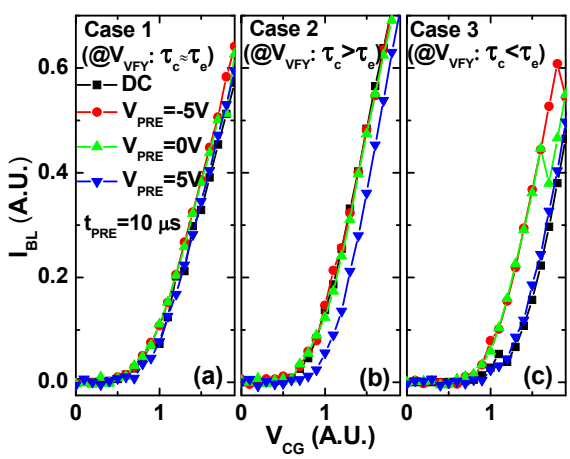


Fig. 4.6. DC and pulsed *I-V* curves for cases 1, 2 and 3 with V_{PRE} (-5, 0 and 5 V).

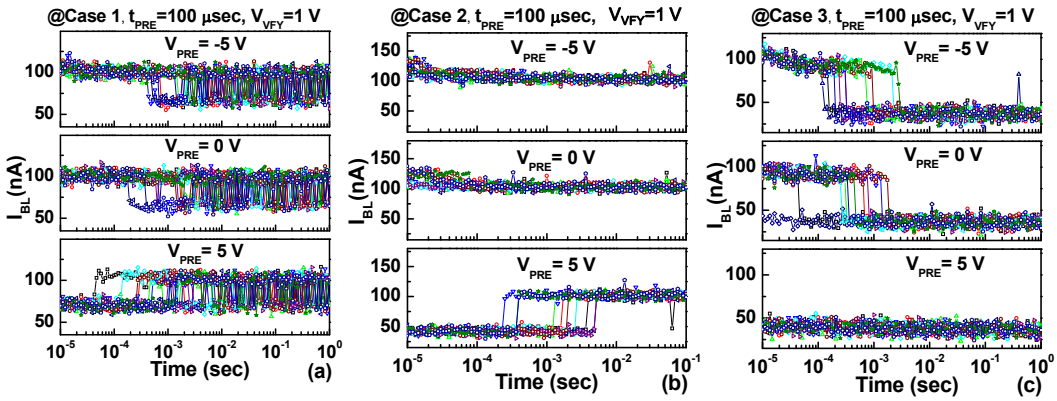


Fig. 4.7. Transient I_{BL} characteristics with V_{PRE} (-5, 0, 5 V) in case (a) 1, (b) 2, and (c) 3. Here, transient I_{BL}s were measured by 10 times and for 100 ms at given a V_{PRE}. V_{PRE}s were applied to the control gate for 100 µs.

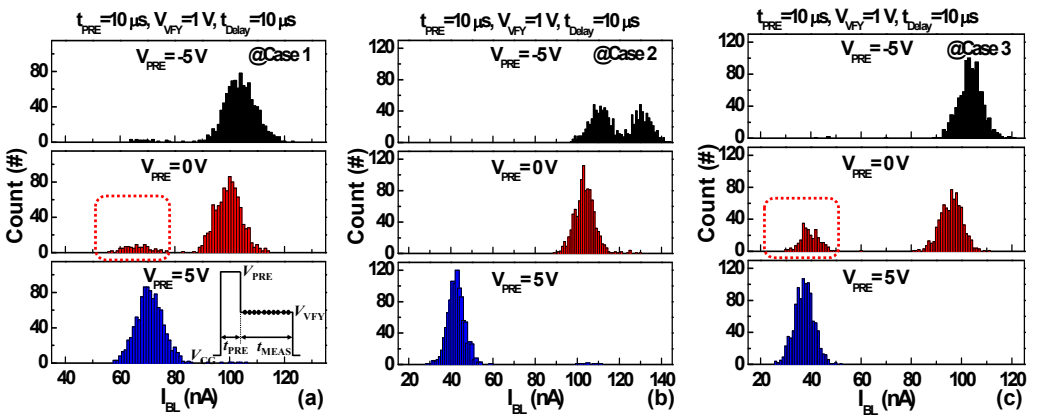


Fig. 4.8. Histogram of 1k sampled I_{BL} with V_{PRE} (-5, 0, and 5 V) in cases (a) 1, (b) 2 and (c) 3. Here, both t_{delay} and t_{PRE} are 10 µs.

Figure (a) in Figs. 4.9-4.11 shows the dependency of τ_c and τ_e behavior on the V_{CG}. Here, V_{CG}s are controlled intentionally to change slightly E_T relative to E_F. Here, both t_{delay} and t_{PRE} are 10 μs. V_{VFY} is 1 V. The τ_c and τ_e behavior in three (a)s of Figs. 4.9-4.11 show general DC characteristics of RTN with respect to V_{CG}. In three (b)s of Figs. 4.9-4.11, the frequency count of high or low I_{BL} changes as the V_{PRE} changes. At V_{PRE}s of Figs. 9-11, E_T is close to E_F in each case.

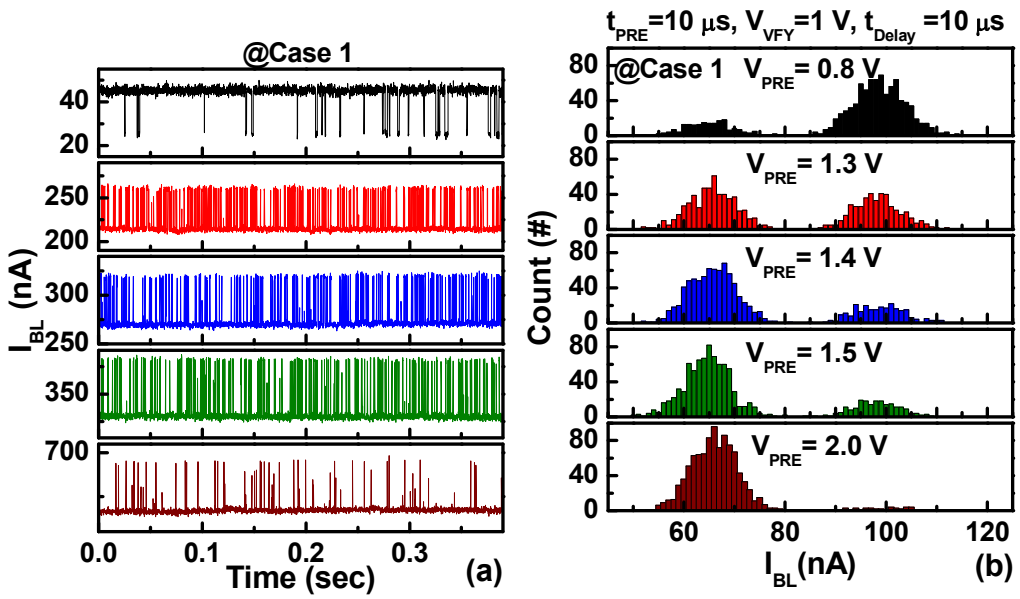


Fig. 4.9 (a) RTN waveforms of I_{BL} and (b) histogram of 1k sampled I_{BL} with V_{CG} (0.8, 1.3, 1.4, 1.5 and 2 V) in case 1.

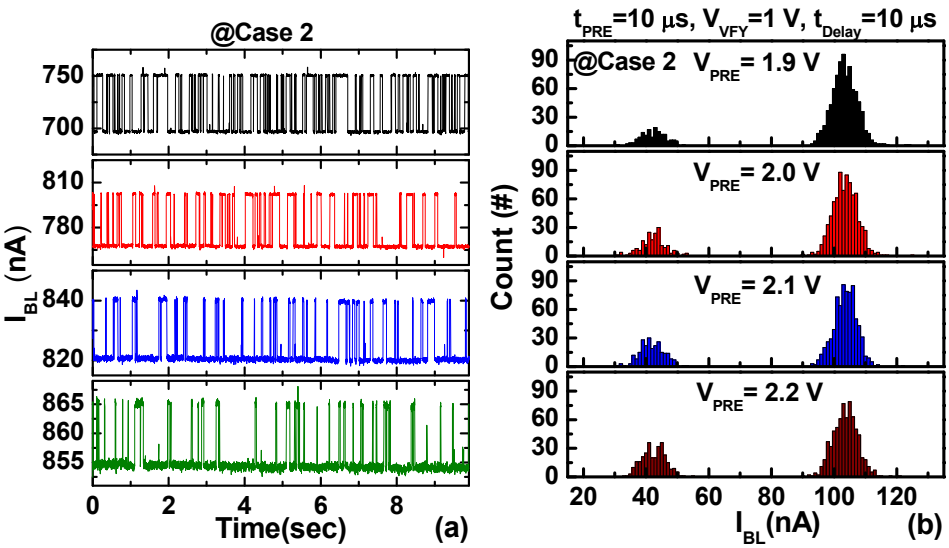


Fig. 4.10 (a) RTN waveforms of I_{BL} and (b) histogram of 1k sampled I_{BL} with V_{CG} (1.9, 2, 2.1 and 2.2 V) in case 2.

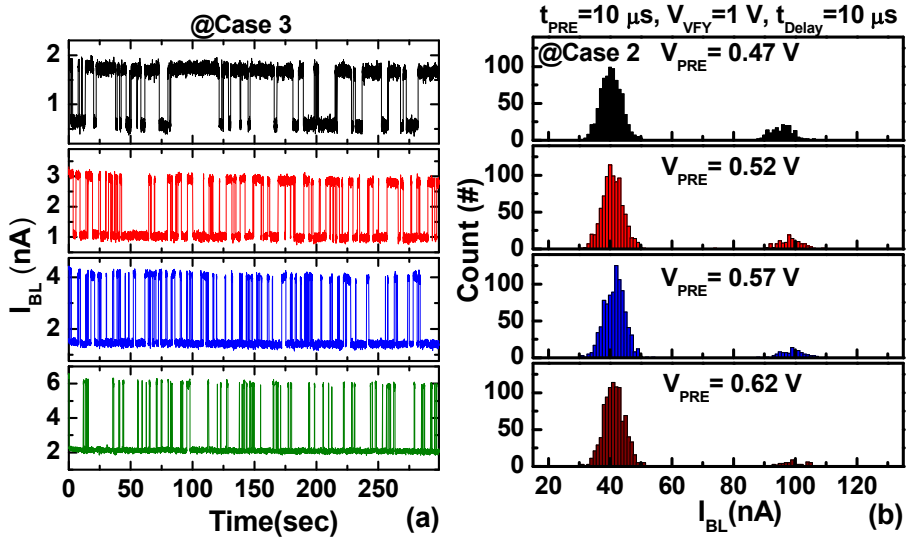


Fig. 4.11 (a) RTN waveforms of I_{BL} and (b) I_{BL} histogram of 1k sampled I_{BL} with V_{CG} (0.47, 0.52, 0.57 and 0.62 V) in case 3.

Fig. 4.12 (a), (b), and (c) compare τ_c/τ_e and frequency count ratio of high and low I_{BL} as a parameter of V_{PRE} in cases 1, 2, and 3, respectively. In case 1, τ_c/τ_e and the frequency count are similar. In case 2, the frequency count ratio is higher than τ_c/τ_e. In case 3, τ_c/τ_e is higher than frequency count ratio. This means that current fluctuation depends on not only V_{PRE} but also V_{VFY}.

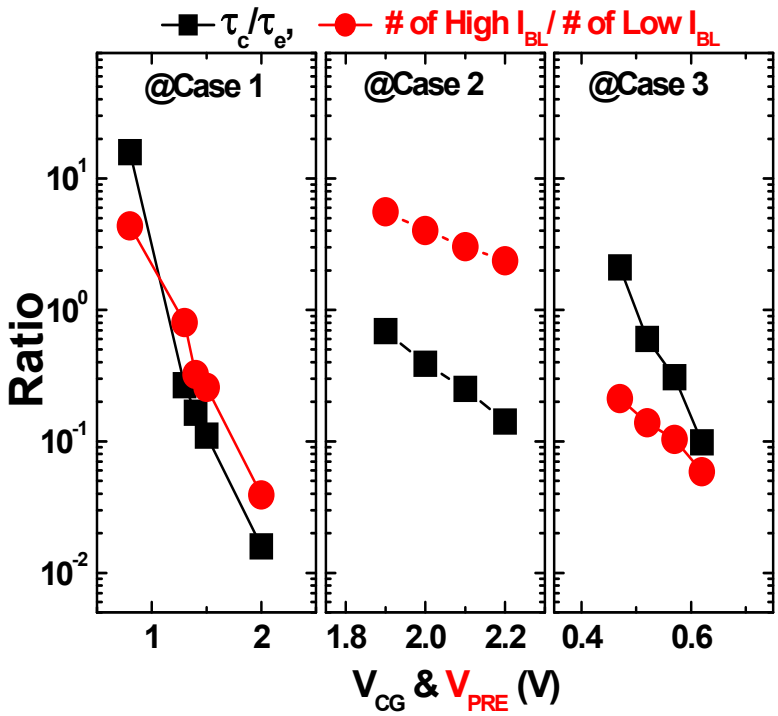
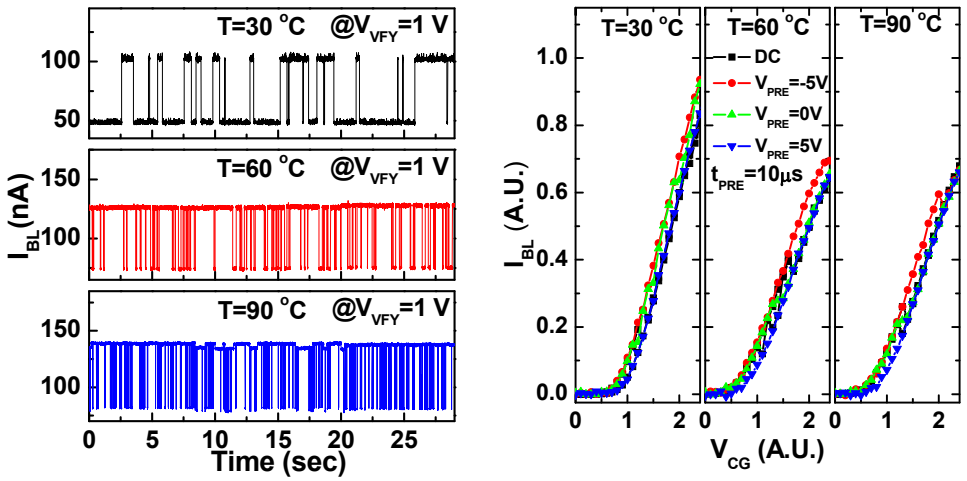


Fig. 4.12 τ_c/τ_e and frequency count ratio of high I_{BL} and low I_{BL} in cases (a) 1, (b) 2 and (c) 3.

With increasing T, τ_c and τ_e becomes short at a V_{VFY} as shown in Fig. 4.13 (a). Pulsed I-V curves plotted in Fig 4.13 (b) show different V_{th}s with the V_{PRE} at different Ts. Fig. 4.14 (a), (b), and (c) show histogram of 1k sampled I_{BL} as parameters of V_{PRE} and t_{delay} at 30, 60, and 90 °C, respectively. Although τ_c/τ_e becomes short as T increases, the characteristic of high or low I_{BL} distribution is not changed at the same V_{PRE} compared to that at 300 K. When I_{BL}s are sampled by 1k times after t_{delay} of 1 ms, frequency count suppressed I_{BL} level by a V_{PRE} increases as T increases. From these results, by controlling the pre-bias in ~μs range, it was confirmed that our method could suppress effectively the effect of RTN during read operation in NAND flash memory because I_{BL} are sampled before changing the state of trap occupancy.



(a) (b)

Fig. 4.13 (a) RTN waveforms of I_{BL} at different temperatures (T) of 30, 60, and 90 °C, (b) DC and pulsed I-V characteristics as a parameter of V_{PRE}.

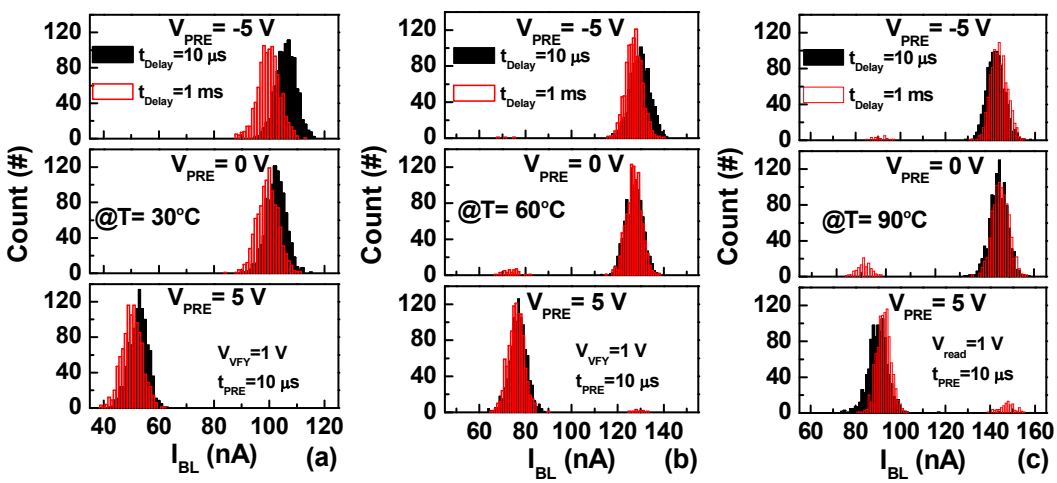


Fig. 4.14 Histogram of 1k sampled I_{BL} with V_{PRE} as a parameter of and t_{delay} at (a) 30, (b) 60, and (c) 90 °C.

Chapter 5

Hysteresis phenomena in floating-gate NAND flash memory

5.1 Introduction

The continuous market needs for larger capacity of portable devices forces the floating-gate (FG) NAND flash memory to severely scale down its feature size. Furthermore, the multi-level-cell (MLC) operation becomes more common due to a lower cost per bit without scaling down. The aggressive reduction of the feature size of FG NAND flash memory cells and MLC operation lead to various problems such as cell-to-cell interference, reduction of on-cell string current, random telegraph noise, and etc [3], [24], [25]. Especially, Inter-poly dielectric (IPD) becomes the limitation of scaling down and MLC operation [26], because the reduced space between adjacent bit-line cells can no longer accommodate both IPD and the wrapped control-gate (CG) around FG which can increase the coupling ratio and minimize the FG interference. In order to solve this problem

while maintaining the cell performance, the shape of FG is changed to secure the sufficient geometrical area ratio between CG and FG, and the thickness of IPD should be reduced [13], [27], [28]. However, the geometry change of FG leads to the increased process complexity and cost per bit. And reduction of IPD thickness will inevitably cause the reliability issue such as the leakage current and data retention [28]. Therefore, high-k dielectric material, which will be able to increase the capacitance of IPD with a thick physical thickness, has been regarded as one candidate for solving these problems [29], [30]. However, high-k materials have also a fatal problem due to the higher density of traps, which may increase the leakage current and degrade the retention characteristic due to trap-assisted tunneling. According to a previous paper, the threshold voltage shift (ΔV_{th}) due to a trapped electron at the bottom oxide of IPD can be about 10 mV in 25 nm technology node, and the effect of trap in the IPD becomes more severe as scaling down [4]. Therefore, the reliability of IPD in flash memory becomes the one of the critical issue and has been widely studied in many groups [31]-[33]. It has been reported that the low-field leakage current of $SiO_2/Al_xO_y/SiO_2$ (OAO) IPD at high temperature increases due to the abundant shallow traps of OAO IPD compared with those of the conventional $SiO_2/Si_xN_y/SiO_2$ (ONO) IPD [32]. Furthermore, the counterclockwise or clockwise hysteresis phenomena in the high-k material which lead to the shift of threshold voltage (V_{th}) were studied. The phenomena can be caused by the electron trapping or de-trapping from the

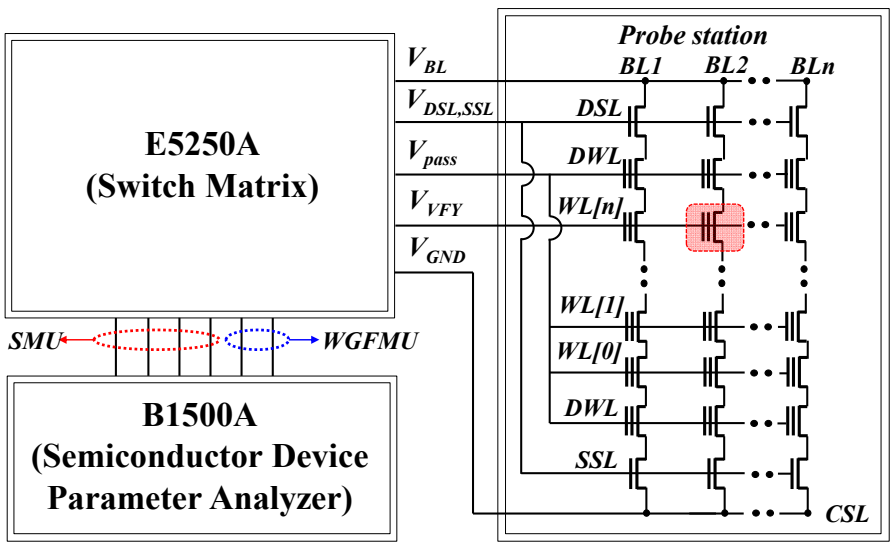
gate/substrate to the high-k stacks [34], or caused by the mobile charges in the high-k materials [35]. However, no paper has been systematically reported to investigate reliability problems and their cause in NAND flash memory having ONO stack as the IPD even if the ONO stack is still used as IPD in the industry.

In this paper, we observe the behavior of abnormal cell which has the counterclockwise hysteresis phenomena in floating-gate NAND flash memory strings having conventional ONO IPD. We also systematically identify the origin of the counterclockwise hysteresis phenomena by measuring the transient bit-line current (I_{BL}) characteristics. Furthermore, we investigate the transient I_{BL} characteristics due to the hysteresis phenomena under various conditions such as temperature, pre-bias voltage (V_{PRE}), verifying bias voltage (V_{VFY}), and program/erase cycling.

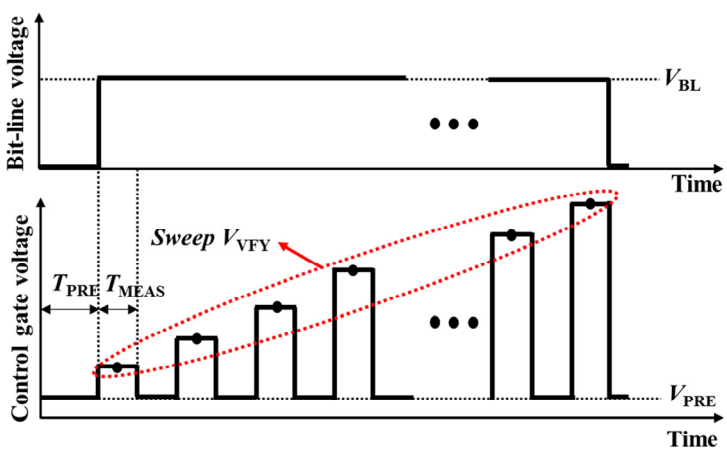
5.2 Device structure and measurement setup

The floating-gate NAND flash memory in this work was fabricated by applying 48 and 26 nm technologies. A 48 nm NAND cell string consists of thirty-two unit cells, a drain select line (DSL) transistor and a source select line (SSL) transistor. A 26 nm NAND cell string consists of sixty-four unit cells, two dummy cells, a DSL transistor and a SSL transistor. Since NAND flash memory strings actually are biased under dynamic signals during the short operation time (~μs), it is appropriate to measure the electrical properties of trap in a short time. In order to observe the behavior of trap in a short time, the I_{BL} is set to be measured in ~μs by using WGFMU modules that integrates arbitrary linear waveform generation capability with high-speed current and voltage measurement [36]. The block diagram of pulsed *I-V* and fast transient I_{BL} measurement system is represented in Fig. 5.1 (a). To observe the pulsed *I-V* and transient characteristics of I_{BL}, the biases are applied to the selected word-line (WL) and bit-line (BL) in the string by using the WGFMU modules. Fig. 5.1 (b) and (c) show the pulse waveform of V_{BL} and V_{CG} for pulsed *I-V* and fast transient I_{BL} measurements, respectively. In the pulsed *I-V* measurement, the V_{PRE} is applied to the CG for T_{PRE} before applying a verify voltage (V_{VFY}). Then, the V_{VFY} is incrementally applied and I_{BL} is sampled during the T_{MEAS}. In the fast

transient I_{BL} measurement, the V_{PRE} and 0 V were applied to the CG and bit-line (BL) of the selected cell for T_{PRE}, respectively, and then I_{BL} is set to be measured at a V_{VFY} and a V_{BL} for T_{MEAS}. I_{BL} is repeatedly measured by 10 times for statistics since the characteristic of transient I_{BL} is stochastic.



(a)



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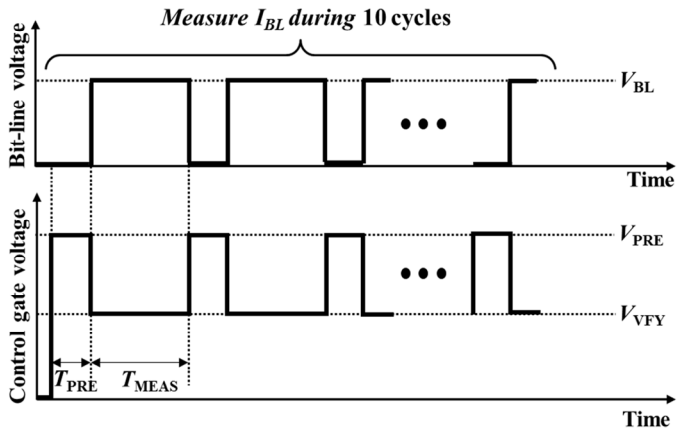


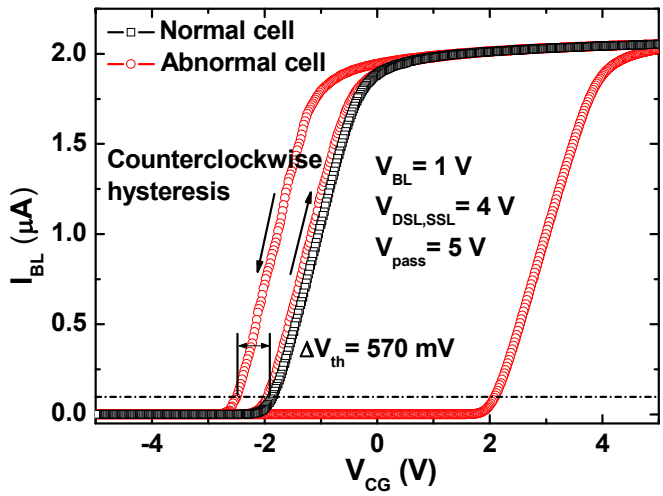
(c)

Fig. 5.1. (a) Block diagram of the measurement system. The selected cell is represented by a shaded box. The pulse waveform of V_{BL} and V_{CG} for (b) pulsed *I-V* and (c) fast transient I_{BL} measurement.

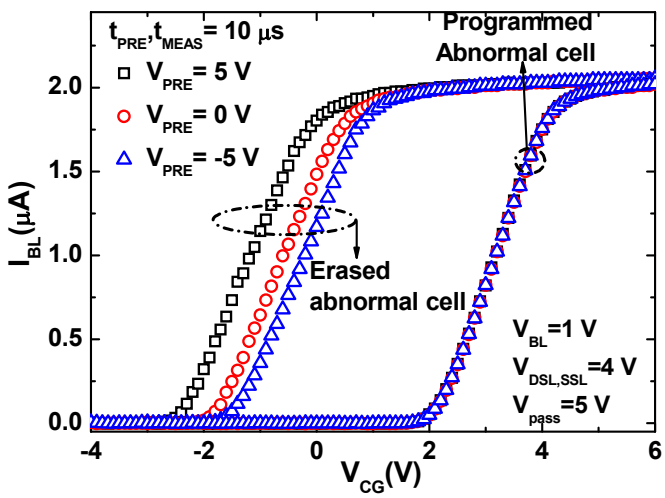
5.3 Hysteresis phenomena in abnormal cells

Fig.5.2 (a) shows the measured I_{BL}-V_{CG} characteristics of 48nm NAND flash memory cell by using the DC measurement when a selected cell is erased or programmed. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively, when unselected cells are erased. The I_{BL} of the selected cell is measured by using the up-scan reading where the V_{CG} of the selected cell is changed from a negative to a positive bias direction and down-scan reading where the V_{CG} of the selected cell is changed from a positive to a negative bias direction. As compared

with a normal cell in ease state, an abnormal cell in erase state has a counterclockwise hysteresis phenomenon that results in the large ΔV_{th} (~570 mV) as shown in Fig. 5.2 (a). Note we can observe a clockwise hysteresis if electrons are trapped into the tunneling oxide [37]. When the abnormal cell is programmed, the counterclockwise hysteresis phenomenon disappears. In order to observe this phenomenon more clearly, we compare the I_{BL}-V_{CG} characteristics of DC measurement with that of pulsed *I-V* measurement when the abnormal cell is erased or programmed. Here, the bias conditions for measurement are the same as those mentioned in Fig. 5.2(a), instead, the V_{CG} of the selected cell is switched by WGFMU module as mentioned in Fig. 5.1(b) during the pulsed *I-V* measurement. Here, t_{PRE} is 10 μs and V_{PRE} is changed to have -5 V, 0V, and 5 V. When the abnormal cell is measured by using DC measurement, I_{BL}-V_{CG} characteristics of the abnormal cell show the same results as that mentioned in Fig. 5.2(a). When the abnormal cell is measured by using pulsed *I-V* measurement, the V_{th} of the abnormal cell in erase state is changed by V_{PRE} as shown in Fig. 5.2(b). With increasing V_{PRE} from -5 V to 5 V, the V_{th} is decreased from -3.458 V to -4.359 V. On the contrary, the V_{th} of the abnormal cell in programmed state is constant with increasing V_{PRE}.



(a)



(b)

Fig. 5.2. (a) Measured I_{BL}-V_{CG} characteristics of a 48nm NAND flash memory cell by using DC measurement when a selected cell is erased or programmed. (b) Measured I_{BL}-V_{CG} characteristics of the 48nm NAND flash memory cell by using the pulsed *I-V* measurement when a selected cell is erased or programmed.

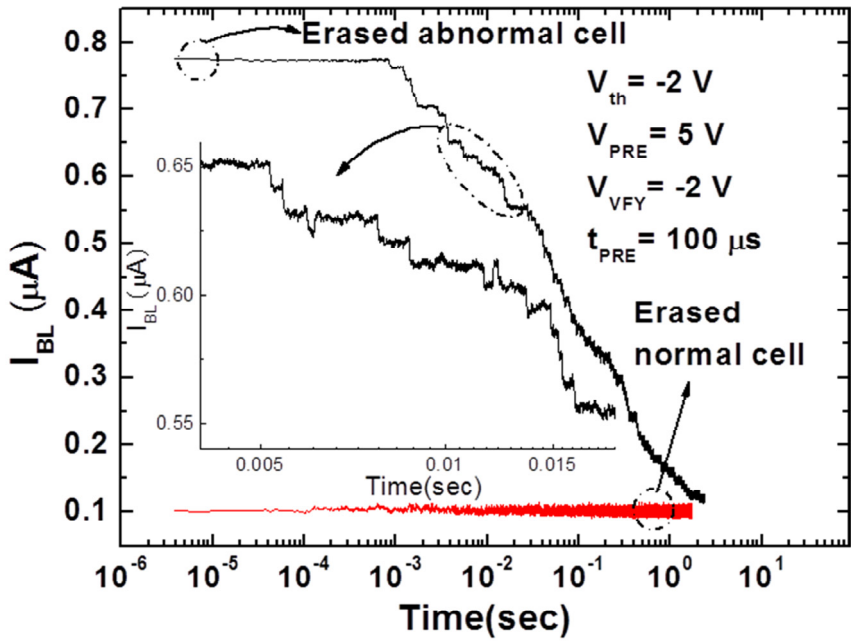


Fig. 5.3. Transient I_{BL} characteristics of normal and abnormal cells in erased state. The inset shows the magnified I_{BL} versus time.

Fig. 5.3 shows the transient I_{BL} characteristics of normal and abnormal cells in erase state. The inset of Fig. 5.3 shows the magnified I_{BL} versus time. Here, the selected and unselected cells are erased to have a V_{th} of -2 V. t_{PRE} and V_{PRE} are 100 μs and 5 V, respectively. $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. By comparing the transient I_{BL} characteristics of normal cell with that of abnormal cell, the I_{BL} of the abnormal cell discretely decreases such as the staircase during the t_{MEAS} as shown in Fig. 5.3.

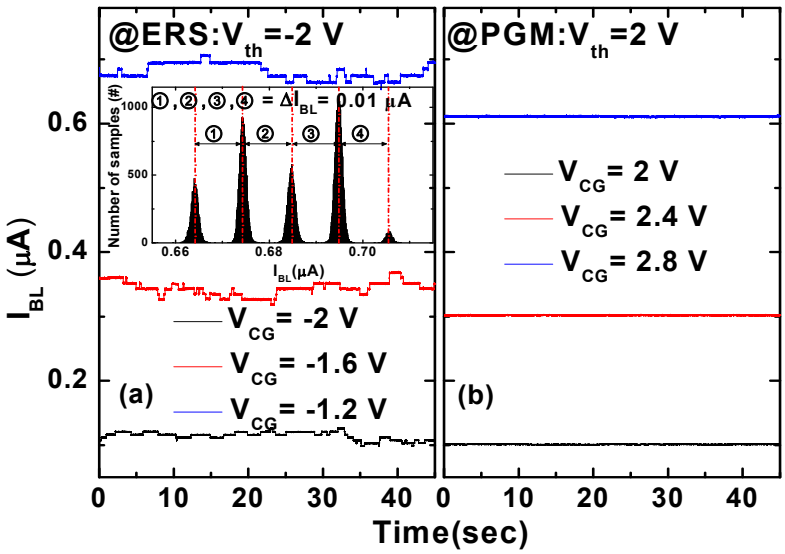


Fig. 5.4. Characteristics of I_{BL} versus time with increasing V_{CG} of abnormal cell when the abnormal cell is (a) erased or (b) programmed. The inset of Fig. 4 (a) shows the multi-level RTN amplitude distribution.

Fig. 5.4 shows the characteristics of I_{BL} versus time with increasing V_{CG} of abnormal cell when the abnormal cell is (a) erased or (b) programmed. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. The inset of Fig. 5.4(a) is the distribution of I_{BL} when I_{BL} is nearly 0.6 μA. As shown in Fig. 5.4, the multi-level random telegraph noise (RTN) is observed in the erased abnormal cell, but, disappeared in the programmed abnormal cell. Moreover, the fluctuation of I_{BL} (ΔI_{BL}) due to multi-level RTN is nearly constant as 0.01 μA as shown in the inset of Fig. 5.4(a).

Fig. 5.5 (a) shows the erased V_{th} as functions of erase voltage (V_{ERS}) and the erase time (t_{ERS}) when a selected cell is the normal cell or the abnormal cell. Fig. 5.5 (b) shows the erased V_{th} of the abnormal cell as a function of erase voltage (V_{ERS}) when the erase time (t_{ERS}) is 10 μs or 1 ms. Here, a selected cell is initially programmed to have a V_{th} of 4 V and then erased by the single pulse of amplitude V_{ERS} during t_{ERS}. According to previous report [38], the degradation of erase efficiency occurs by the depletion effects in the poly-silicon FG due to the increase of fringing fields at the rounded FG and the reduction of the active dopant concentration in the small poly-silicon volume. From the results of Fig. 5.5, we can notice that the degradation of erase efficiency increases as decreasing t_{ERS} when a selected cell is the abnormal cell, which implies that the deep depletion occurs in the poly-silicon FG.

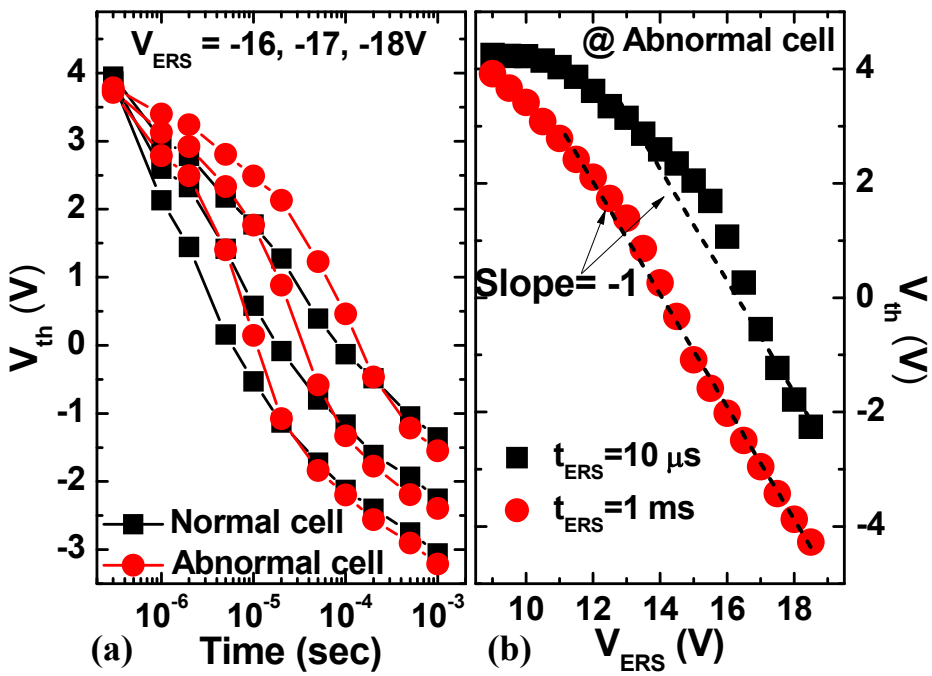


Fig. 5.5 (a) Characteristics of erased V_{th} as functions of erase voltage and erase time when a selected cell is the normal cell or the abnormal cell. (b) Erased V_{th} of the abnormal cell as a function of erase voltage when the erase time is 10 μs or 1 ms. Dashed lines show the ideal characteristics of erase speed.

5.4 Origin of hysteresis phenomenon in the abnormal cell

From the results as shown in above, we can assume that these phenomena are caused by the effect of trap in an abnormal cell. From now on, we discuss the origin of these hysteresis phenomena of the abnormal cell. From the results of Figs. 5.3 and 5.4, we can notice that a number of traps exist somewhere in the abnormal cell, which is responsible for the hysteresis phenomena. In order to define the position of traps in the abnormal cell, we consider the four different cases as shown in Fig. 5.6. Fig. 5.6 shows the simulation results of energy band diagram with V_{CG} of a selected cell when the selected cell is erased or programmed. For device simulation, the cell in the simulation has channel length and width of 48 nm, tunneling oxide thickness (t_{ox}) of 7.9 nm, uniform channel doping of 2×10^{17} cm^{-3}, and peak source/drain doping of 1×10^{19} cm^{-3}. From the results of Fig. 5.5, we can notice that doping concentration of FG in the abnormal cell is lower than that of CG because the depletion occurs at the interface between the FG and the bottom oxide of IPD. So, the cell in the simulation has constant FG doping of 1×10^{19} cm^{-3} and constant CG doping of 1×10^{20} cm^{-3}.

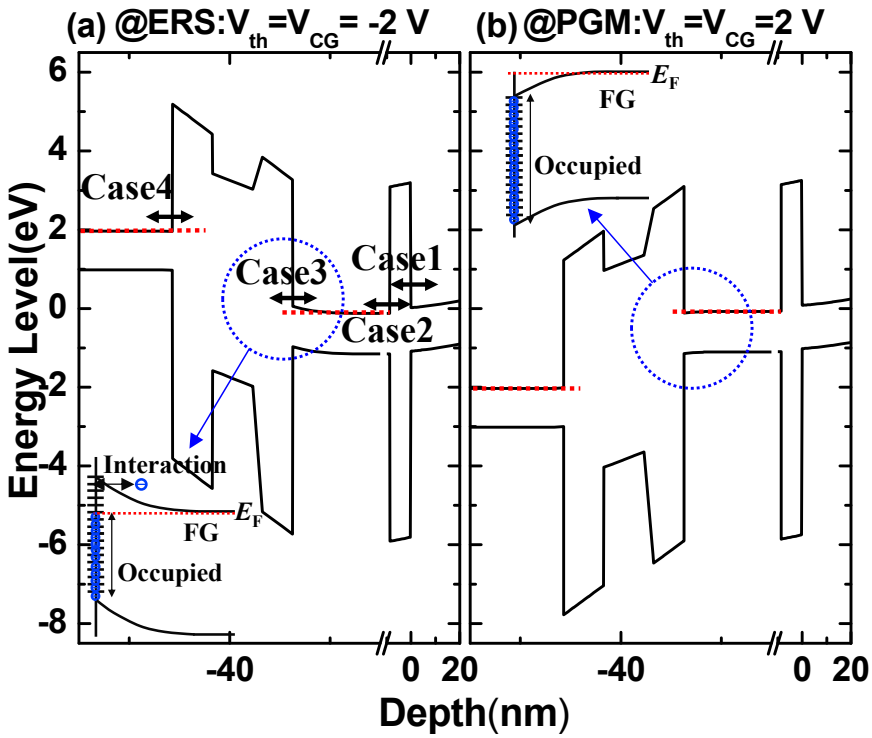


Fig. 5.6. Simulated energy band diagrams with V_{CG} of a selected cell when the selected cell is (a) erased or (b) programmed. Insets of Fig.5.6 represent the schematic views of energy band diagrams between FG and bottom oxide with showing the occupancy of interface traps. Each of the small horizontal lines represents the interface trap.

According to previous papers [7]-[10], a trap which leads to various problems such as RTN and hysteretic effect is located in the tunneling oxide. So, we consider first assume that the traps responsible for the hysteresis are located

in the tunneling oxide and interacted with electrons in the channel (case1) or in the FG (case2). If traps are located in the tunneling oxide as mentioned in cases1 and 2, multi-level RTN is should be observed in not only the erased abnormal cell but also the programmed abnormal cell under the condition that I_{BL} is adjusted to have the same level by controlling V_{CG}, because the energy band banding of the tunneling oxide is the same whenever the selected cell is erased or programmed as shown in Fig. 5.6. However, the multi-level RTN is only observed in the abnormal cell in erased state and disappeared in the abnormal cell in programmed state as shown in Fig. 5.4. Furthermore, ΔI_{BL} due to multi-level RTN of cases1 and 2 cannot be constant due to the effect of random dopant fluctuations (RDF), line edge roughness (LER), and BL interference which can generate the percolation path in the channel [20], [22], [39]. However, ΔI_{BL} due to the multi-level RTN is nearly constant as 0.01 μA as mentioned in the inset of Fig. 5.4. According to the argument mentioned above, cases1 and 2 can be ruled out.

Now, we assume that traps are located in the IPD and interact with electrons in the FG (case3) or in the CG (case4). In case3, traps, which interact with electrons in the FG, are located at the interface between the bottom oxide of IPD and FG. When the V_{CG} of a selected cell in erased state is the same as the V_{th} (=-2 V), the depletion occurs at the interface between the bottom oxide of IPD and FG due to low doping concentration. Electrons can interact with the interface

traps because there are traps unoccupied by electrons as shown in the inset of Fig. 5.6 (a). So, the multi-level RTN is observed in the erased cell. On the contrary, when the V_{CG} of a selected cell in programmed state is the same as the V_{th} (=2 V), the multi-level RTN is disappeared because all traps are occupied by electrons due to the accumulation of FG as shown in the inset of Fig. 5.6 (b). Moreover, the behavior of transient I_{BL} can be explained as follows. First of all, in case3, we assume that electrons are not injected from any electrode to FG or IPD during the t_{PRE} and t_{MEAS}. Fig. 5.7 represents schematically the energy band diagrams to explain the emission and capture process between the CG and the top oxide of the IPD, the FG and the bottom oxide of the IPD during the transient measurement. Looking at the results of Figs. 5.3 and 5.6, the I_{BL} of the abnormal cell in erased state decreases when the V_{CG} of the selected cell in erased state is changed from 5 V to V_{th}. When the V_{CG} of the selected cell is 5 V, electrons in the FG are captured into traps because the E_T is lower than the E_F of FG (E_T- E_F<0) as shown in Fig. 5.7 (a), which leads to the increase of I_{BL}. When the V_{CG} of the selected cell in erased state is V_{th}, trapped electrons are emitted to the FG because the E_T is higher than the E_F of FG (E_T- E_F>0) as shown in Fig. 5.7 (b) and (c), which leads to the decrease of I_{BL}.

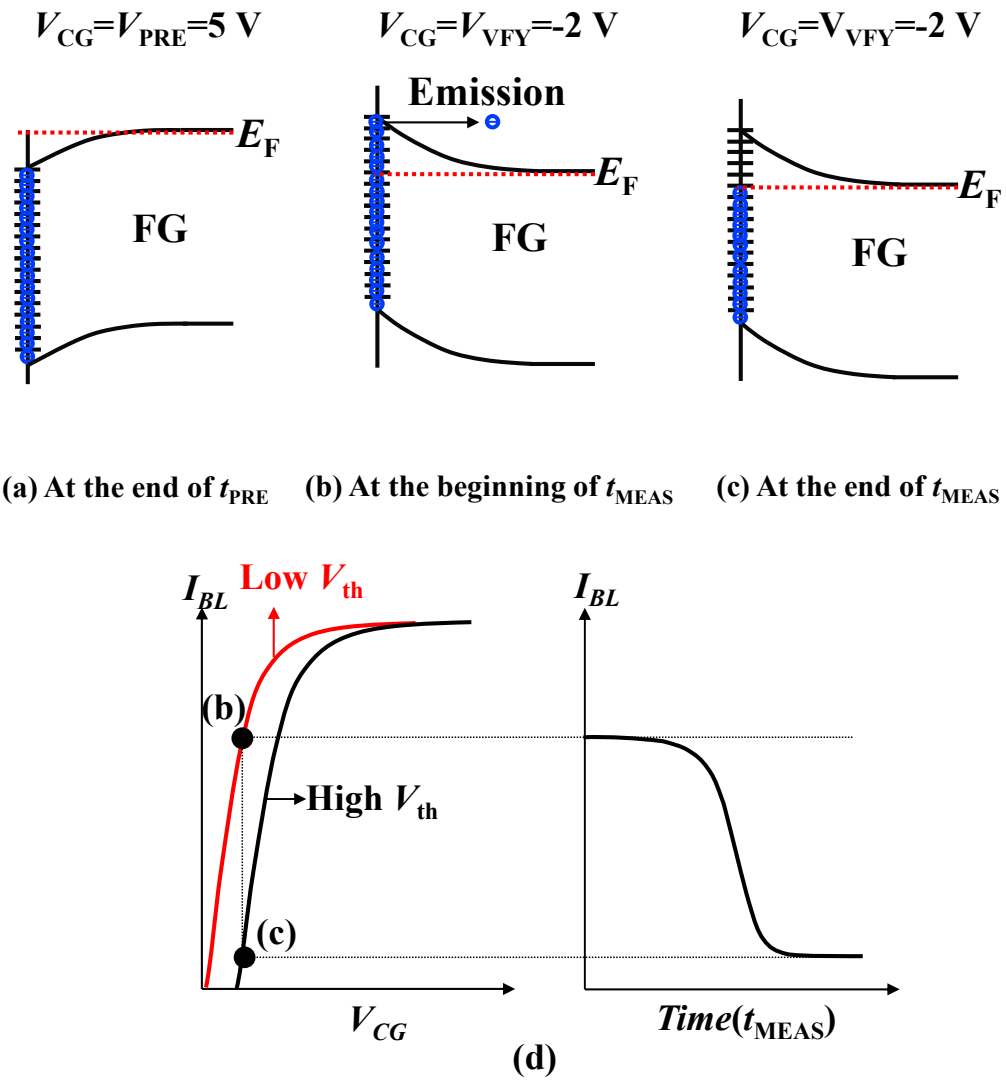


Fig. 5.7. Schematic views of energy band diagram when an abnormal cell is erased. (a) At the end of t_{PRE}, (b) at the beginning of t_{MEAS}, and (c) at the end of t_{MEAS}. (d) Schematic view of transient I_{BL} characteristic during t_{MEAS}. Here, the V_{CG} of a selected cell in erased state is 5 V during the t_{PRE}, and the V_{CG} of the selected cell is V_{th} (=-2 V) during the t_{MEAS}.

In case4, traps are located in the top oxide of IPD and interact with electrons in the CG. When the V_{CG} of a selected cell in erased state is the same as the V_{th} (=-2 V), the depletion cannot occur at the interface between the top oxide of IPD and CG due to high doping concentration of CG as shown in Fig. 5.6 (a). Because all traps are occupied by electrons, the hysteresis phenomenon and multi-level RTN cannot be observed. Therefore, case4 can be also ruled out.

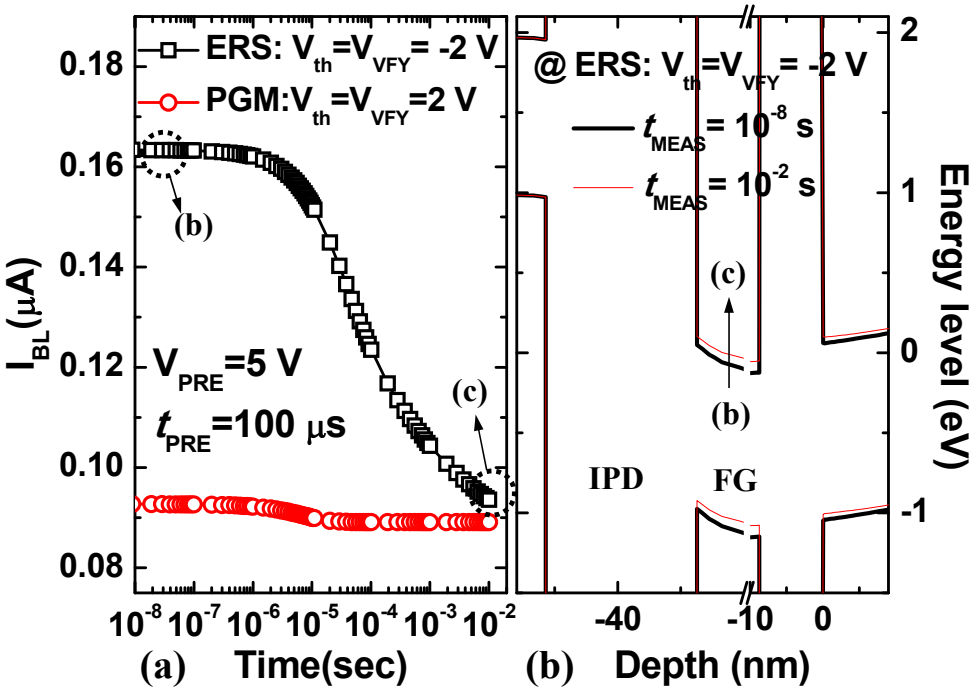


Fig. 5.8. (a) Simulated transient I_{BL} characteristics of a cell when the cell is erased or programmed. (b) Simulated energy band diagram of an erased cell when t_{MEAS} is 10 ns or 10 ms.

Fig. 5.8 (a) shows simulated transient I_{BL} characteristics of a cell when the cell is erased or programmed. Fig. 5.8 (b) shows the simulation result of energy band diagram in an erased cell when t_{MEAS} is 10 ns or 10 ms. Here, t_{PRE} and V_{PRE} are 100 μs and 5 V, respectively. When the cell is erased, V_{th} and V_{VFY} are same as -2 V. When the cell is programmed, V_{th} and V_{VFY} are same as 2 V. In the simulation results of Fig. 5.8, we used the profile of trap density (D_{it}) at the interface between the bottom oxide of IPD and FG which is extracted from fabricated 3-D NAND cells having tube-type poly-Si body [40]. From the results of Fig. 5.8 (a), the simulation result shows the same behavior of measured transient I_{BL} as shown in the Fig. 5.3. In addition, Fig. 5.8 (b) shows a good agreement with the explanation as mentioned above. When t_{MEAS} increases from 10 ns to 10 ms, the energy level of FG increases because trapped electrons are emitted to the FG, which leads to the decrease of I_{BL}.

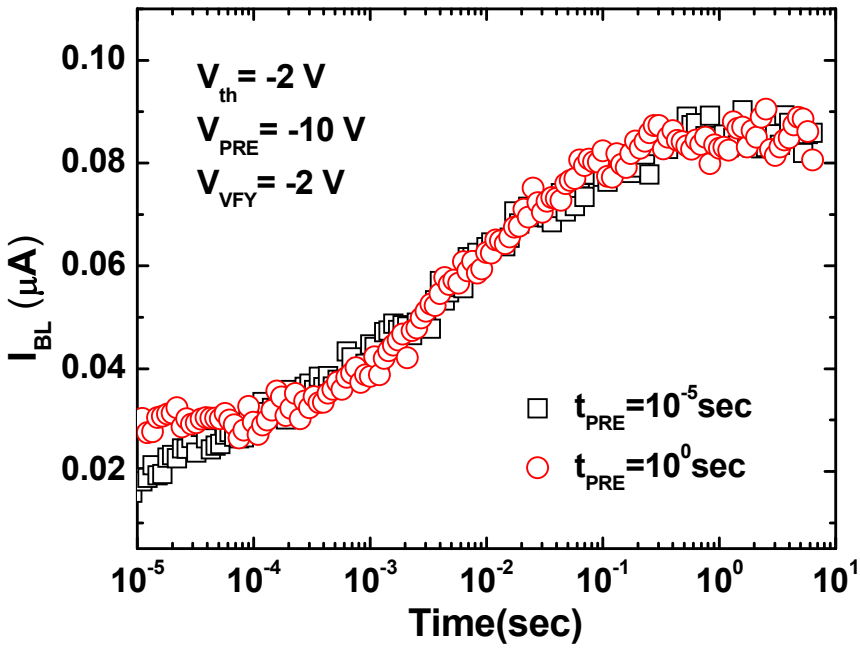


Fig. 5.9. Transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of t_{PRE}.

From the results of Fig. 5.5 and 5.6 (a), we assume that the behavior of transient I_{BL} will be changed due to the deep depletion effect in the poly-silicon FG when the negative V_{CG} of an abnormal cell in erased state is induced by changing the t_{PRE}. Fig. 5.9 shows the transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of t_{PRE}. Here, a selected cell is initially erased to have a V_{th} of -2 V. V_{VFY} and V_{PRE} are -2 V and -10 V, respectively. $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. To observe the effect

of deep depletion on transient I_{BL} characteristics, t_{PRE} is split into 10 μs and 1 s. As shown in Fig. 1(c), each curve in Fig. 5.9 is the average value of transient I_{BL} which is repeatedly measured by 10 times for statistics. Open rectangular symbols represent the transient I_{BL} when the t_{PRE} is 10 μs. Circular symbols represent the transient I_{BL} when the t_{PRE} is 1 s. As shown in Fig. 5.9, the I_{BL} during short t_{PRE} (=10 μs) is decreased more significantly than that during long t_{PRE} (=1 μs), which can be explained by the schematic views in Fig. 5.10.

Fig. 5.10 shows schematically the energy band diagrams of the FG NAND flash memory during t_{PRE}. Fig. 5.10 (a) shows the energy band diagram when the deep depletion occurs in the FG. In Fig. 5.10 (b), it is shown that the energy band diagram when the deep depletion is disappeared due to the hole generation at the interface between the FG and the bottom oxide of IPD. In case3, I_{BL} of an abnormal cell in erased state decreases during t_{PRE} because trapped electrons in the bottom oxide of IPD are emitted to the FG as mentioned above. As shown in Fig. 5.9 and 5.10, the I_{BL} during short t_{PRE} is decreased more significantly than that during long t_{PRE} because more electrons trapped in the bottom oxide are emitted to the FG in deep depletion mode (just after the a pulse of -10 V is applied to the CG) than in the steady state. As a result of Fig. 5.9, we confirm obviously that the traps responsible for the multi-level RTN and the hysteresis phenomenon are located in the bottom oxide of IPD

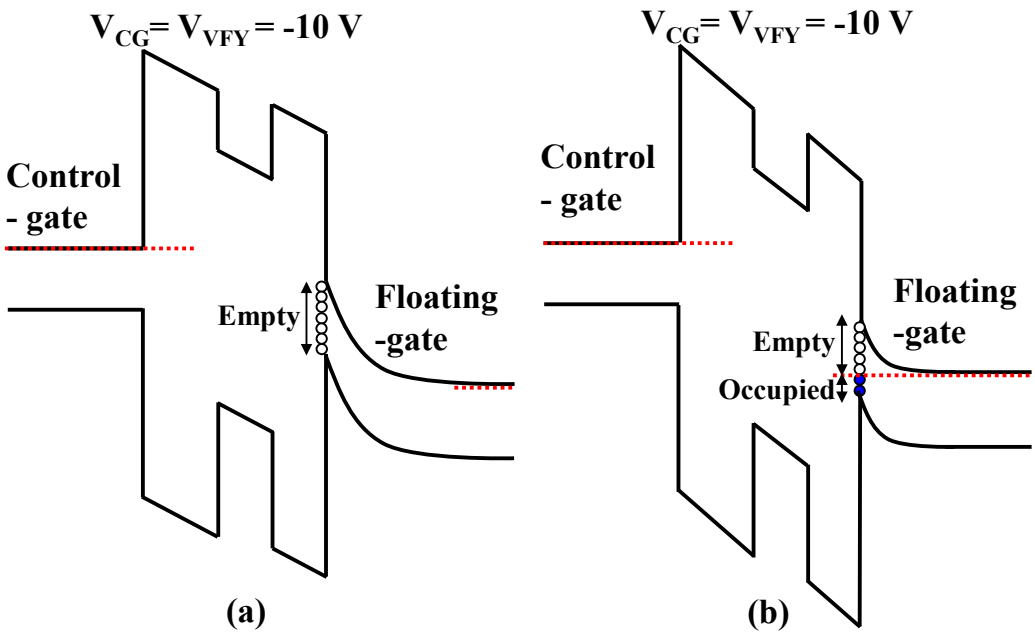


Fig. 5.10. Schematic views of energy band diagram of an abnormal cell in erased state (a) when the deep depletion occurs in the FG (deep depletion mode) and (b) the deep depletion is disappeared (steady state) during the t_{PRE}. Here, the V_{CG} of a selected cell in erased state is -10 V during the t_{PRE}.

In order to extract the activation energy (E_a) of the trap in the bottom oxide of IPD, we measure the transient I_{BL} characteristics of an abnormal cell in erased state with increasing temperature as shown in Fig. 5.11. We firstly applied a method to extract an activation energy of traps in our NAND flash memory cells. Here, a selected cell and unselected cells are erased to have a V_{th} of -2 V. t_{PRE} and

V_{PRE} are 100 μs and 5 V, respectively. $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. As mentioned in Fig. 5.1(c), each curve in Fig. 5.11 is the average value of transient I_{BL} which is repeatedly measured by 10 times for statistics. Open symbols and lines represent measured data and fitting results of measured data by using a stretched exponential function.

The behavior of transient I_{BL} due to traps can be characterized by using the stretched exponential model [41]. Trapping and de-trapping characteristics of electrons determine the transient response, which is explained by the stretched exponential model. The stretched exponential model can be modified to include weighted sum of exponentially decaying terms Eq. (5.1) [42].

$$I_{BL} = I_{BL0} \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] = \sum_i a_i \exp\left[-\left(\frac{t}{\tau_i}\right)\right] \qquad \text{Eq. (5.1)}$$

The amplitude (a_i) and characteristic time constant (τ) of each exponential term are response of a characteristic trap in a device. Moreover, a_i and τ contain the information about their activation energy and trapping or de-trapping mechanism at various temperatures.

From the results of Fig. 5.11, the decrease of transient I_{BL} becomes fast with increasing temperature. Each transient response is well fitted with exponentially decaying terms with characteristic time constants from 10^{-4} to 10^{1} s.

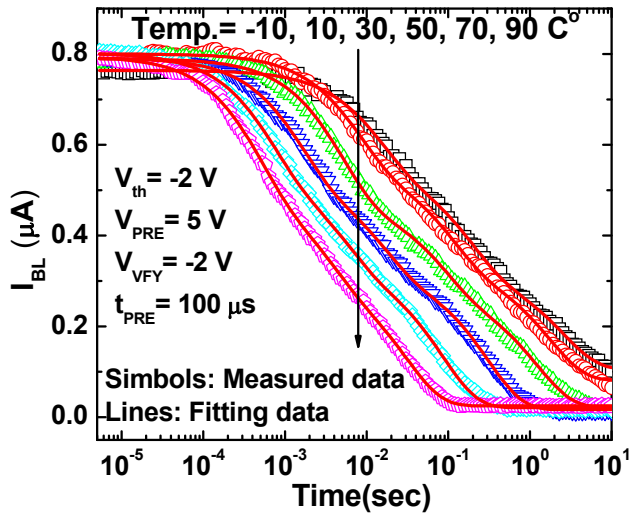


Fig. 5.11. Transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of temperature. Open symbols and lines represent the measured data and fitting data by using Eq. (5.1), respectively.

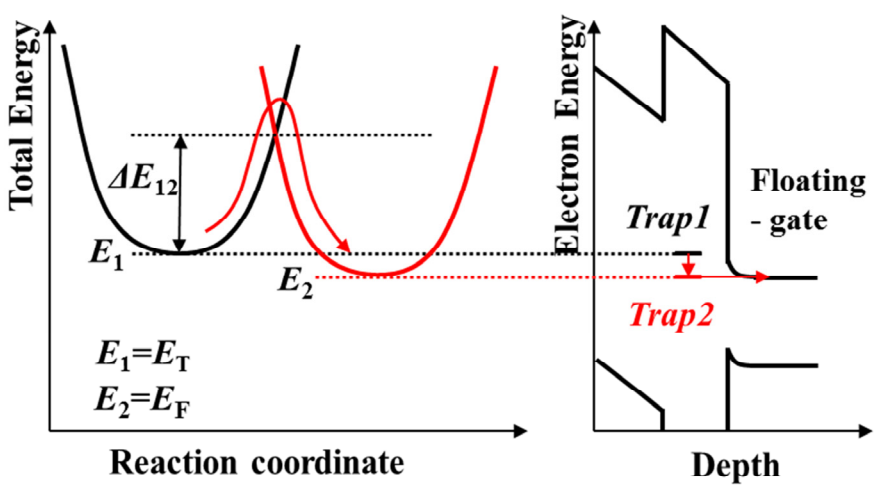


Fig. 5.12. Schematic views of energy diagram of traps in the bottom oxide of IPD when an electron transits from trap1 to trap2.

Fig. 5.12 shows the energy diagram of traps in the bottom oxide of IPD. E_1 is the energy level of trap1, and the trap is filled by an electron during the t_{PRE}. E_2 is the energy level of trap2 which is located near the E_F of FG. ΔE_{12} is E_a in order to transit from E_1 to E_2. From the previous study [43], the emission rate (e_n) can express as,

$$e_n = N_C V_{th} \delta_n \exp\left(-\frac{E_a}{kT}\right) \qquad \text{Eq. (5.2)}$$

where, N_c is the effective density of state at conduction band of FG, V_{th} is the thermal velocity, δ_n is the capture cross section, k is the Boltzmann constant, and T is the temperature. Since N_c V_{th} δ_n is proportional to T^2 and the emission time (τ_e) is inversely proportional to δ_n, the relationship between T and E_a is given by,

$$\ln\left(T^2\tau\right) \propto \frac{E_a}{kT} \qquad \text{Eq. (5.3)}$$

Fig. 5.13 (a) and (b) show the transient responses of an abnormal cell in erased state under various temperatures. Fig. 5.13 (a) shows the behavior of characteristics time constant (τ) obtained by fitted value of the transient I_{BL} curves as shown in Fig. 5.11. Extracted τs can be categorized into three groups depending on the temperature dependence as shown in Fig. 5.13 (a). All three

groups significantly decrease with increasing temperature. Using the extracted τs under various temperatures as shown in in Fig. 5.13 (a), Arrhenius plot can be obtained as shown in Fig. 5.13 (b). From the slopes of the Arrhenius plot in Fig. 5.13 (b), E_as are 0.249 eV ~ 0.319 eV extracted by using Eq. (5.3). We can notice that the behavior of transient I_{BL} occurs by not a trap but a lot of traps which have three different τs. Moreover, electrons need E_as in order to emit from the traps at the read bias condition (V_{VFY}=V_{th}=-2 V).

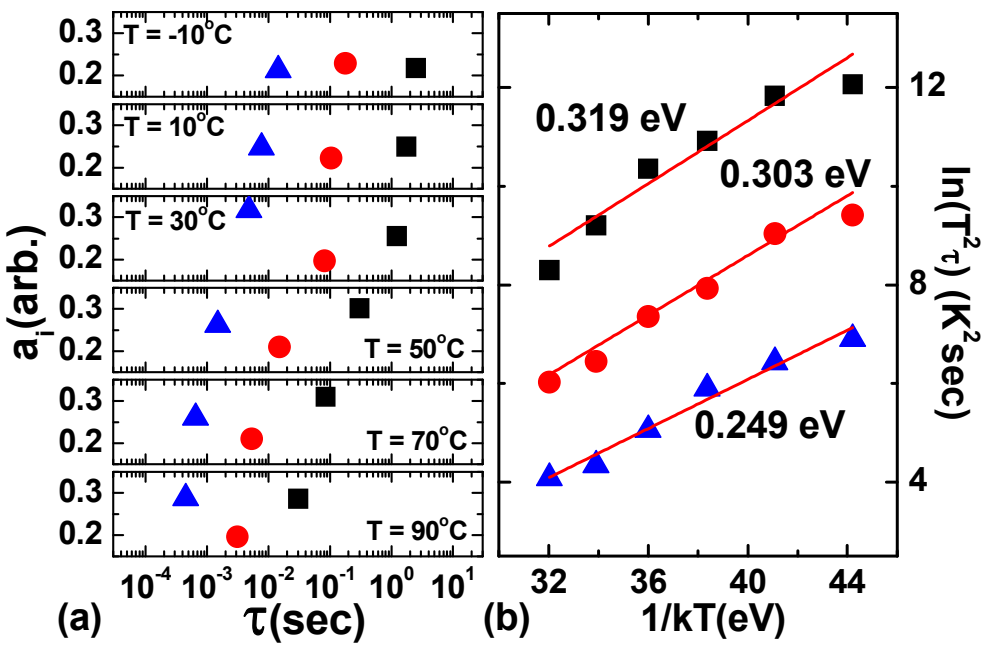


Fig. 5.13. (a) Behavior of characteristics time constants (τ) obtained from transient I_{BL} responses under various temperatures. Y-axis implies the a_i of each τ. (b) Arrhenius plot of the τs which are extracted from Fig. 5.13(a).

5.5 Hysteresis phenomena with bias and P/E cycling stress

Fig. 5.14 shows the transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of V_{PRE}. Here, a selected cell and unselected cells are erased to have a V_{th} of -2 V. t_{PRE} and V_{VFY} are 100 μs and -2 V, respectively. $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. With increasing V_{PRE} from -1 V to 5 V, transient I_{BL} increases because more electrons from FG are captured into traps in the bottom oxide of IPD during t_{PRE}.

Fig. 5.15 shows the transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of V_{VFY}. Here, a selected cell and unselected cells are erased to have a V_{th} of -2 V. t_{PRE} and V_{PRE} are 100 μs and 5 V, respectively. $V_{DSL,SSL}$,V_{pass}, and V_{BL} are the same as above. With decreasing V_{VFY} from -1 V to -3 V, the decrease of transient I_{BL} becomes fast. The behavior of transient I_{BL} can be explained as follows. With decreasing V_{VFY}, E_a decreases because E_T-E_F increases. Therefore, electrons, which are captured to the traps having high E_T during the t_{PRE}, emit rapidly to the FG during the T_{MEAS}.

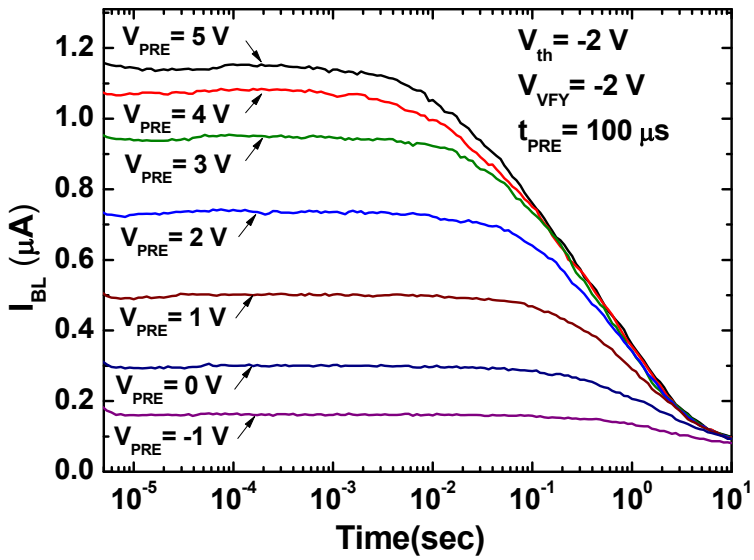


Fig. 5.14. Transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of V_{PRE}.

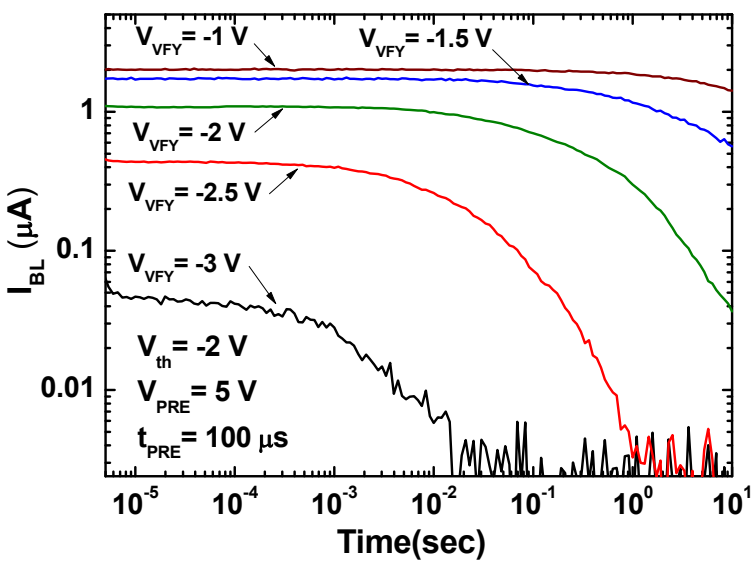


Fig. 5.15. Transient I_{BL} characteristics of an abnormal cell in erased state as a parameter of V_{VFY}.

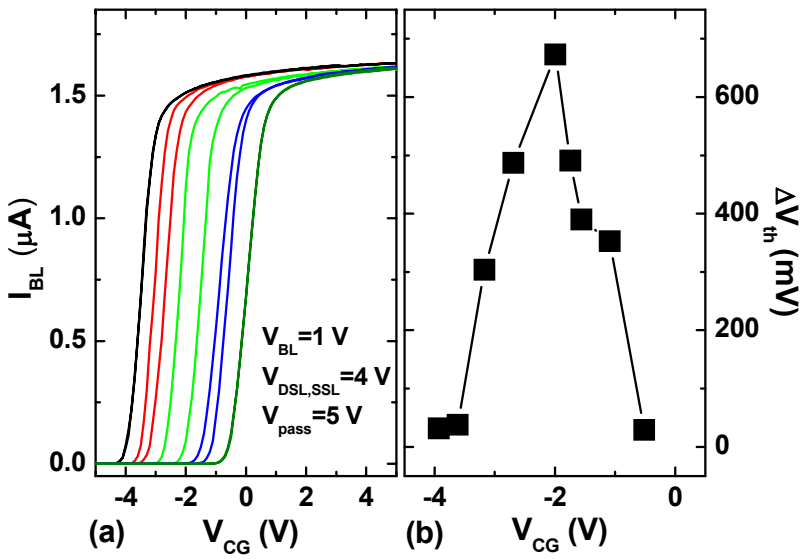


Fig. 5.16. (a) Measured I_{BL}-V_{CG} characteristics by using DC measurement, and (b) ΔV_{th} due to the counterclockwise hysteresis with various V_{th}s of an abnormal cell in a fresh state.

Fig. 5.16 shows (a) the measured I_{BL}-V_{CG} characteristics by using DC measurement and (b) ΔV_{th} due to the counterclockwise hysteresis with various V_{th}s of an abnormal cell in a fresh state. The bias condition is the same as mentioned above in Fig. 5.2(a). From the results of Fig. 5.16, the counterclockwise hysteresis due to traps in the bottom oxide of IPD is observed within the range from V_{th}=-4 V to 0 V. Therefore, we can notice that the traps in the bottom oxide of IPD are distributed within a certain E_T range.

Until now, we measured the multi-level RTN and transient I_{BL} in abnormal cells in erased state. However, these phenomena do not affect significantly on a

read operation of NAND flash memory strings because V_{th} of an erased cell does not commonly verify during the read operation. From now, we measure the same device in Fig. 16 after program (P)/erase (E) cycling stress.

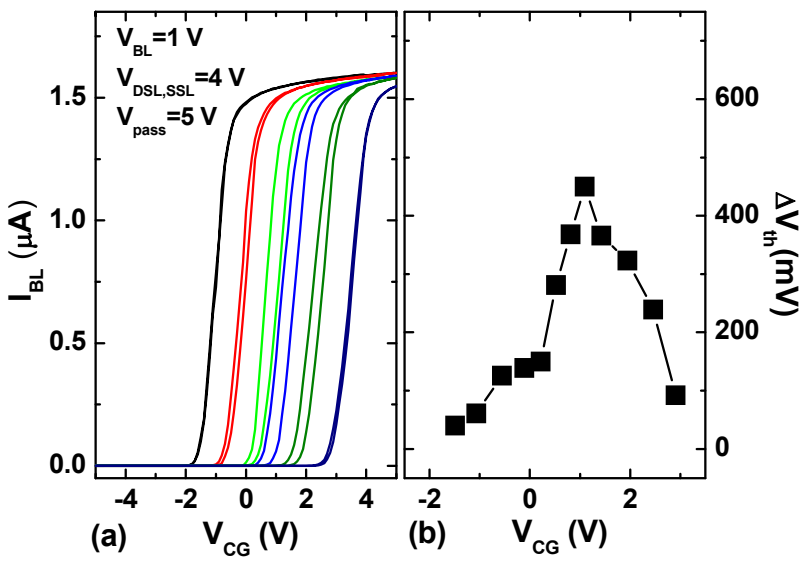


Fig. 5.17. (a) Measured I_{BL}-V_{CG} characteristics by using DC measurement, and (b) ΔV_{th} due to the counterclockwise hysteresis with various V_{th}s of the abnormal cell after P/E cycling stress.

Fig. 5.17 shows (a) the measured I_{BL}-V_{CG} characteristics by using DC measurement and (b) ΔV_{th} due to the counterclockwise hysteresis with various V_{th}s of the abnormal cell after P/E cycling stress. The bias condition is the same as that mentioned in Fig. 5.2(a). From the results of Fig. 5.17, the counterclockwise hysteresis due to traps in the bottom oxide of IPD is observed

within the range from V_{th}=-1.5 V to 3 V. Because electrons are trapped in the bottom oxide during the P/E cycling stress, the range of V_{th}, which we can observe the counterclockwise hysteresis, moves toward to a positive V_{th} direction as compared with the results of Fig. 5.17. This result means that the multi-level RTN and hysteresis phenomena can affect significantly on the reliability of the read operation. For example, ΔV_{th} due to the counterclockwise hysteresis is about 450 mV when the abnormal cell is programmed to have a V_{th} of 1 V after P/E cycling stress as shown in Fig. 5.17 (b).

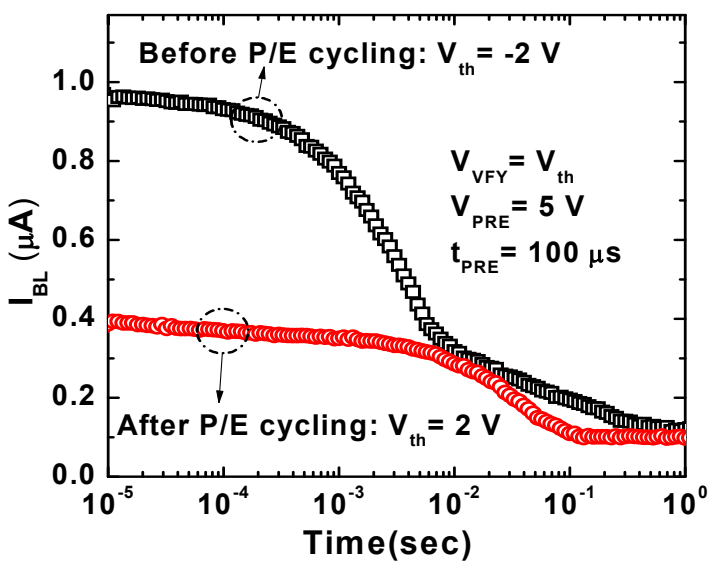


Fig. 5.18. Transient I_{BL} characteristics of the abnormal cell when (a) the abnormal cell is erased to have a V_{th} of -2 V before P/E cycling stress, and (b) programmed to have a V_{th} of 2 V after P/E cycling stress.

Fig. 5.18 shows the transient I_{BL} characteristics of the abnormal cell when (a) the abnormal cell is erased to have a V_{th} of -2 V before P/E cycling stress, and (b) programmed to have a V_{th} of 2 V after P/E cycling stress. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. t_{PRE}, V_{PRE} and V_{VFY} are 100 μs, 5 V, and V_{th} of a selected cell, respectively. Even if the initial value of transient I_{BL} decreases in an abnormal cell after P/E cycling stress as compared with that in the abnormal cell before P/E cycling stress, such transient I_{BL} still leads to a large ΔV_{th} (=319 mV) when the abnormal cell is programmed to have a V_{th} of 2 V.

Fig. 5.19 shows the characteristics of I_{BL} versus time when (a) the abnormal cell is erased to have a V_{th} of -2 V before P/E cycling stress, and (b) programmed to have a V_{th} of 2 V after P/E cycling stress. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. The V_{CG} of a selected cell is V_{th}. From the results of Fig. 5.19, the multi-level RTN is observed not only in the abnormal cell before P/E cycling stress, but also in abnormal cell after P/E cycling stress.

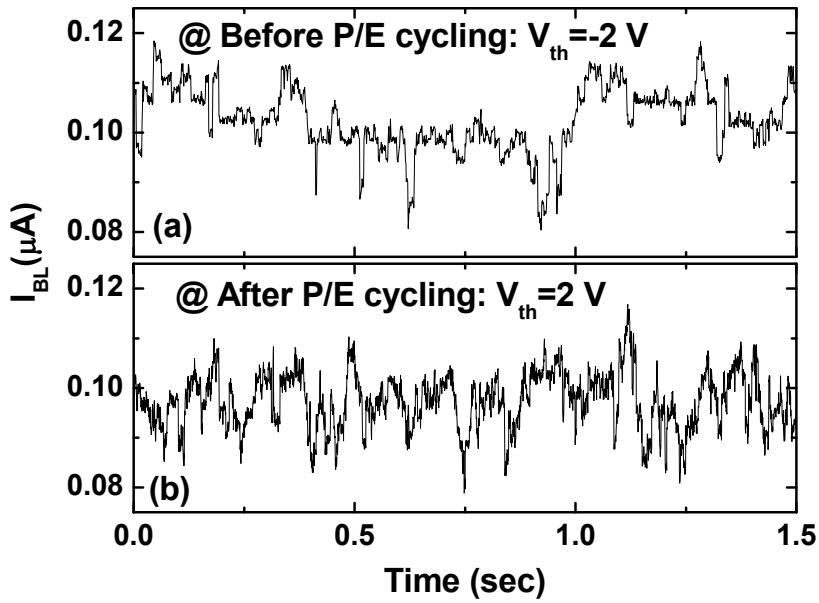
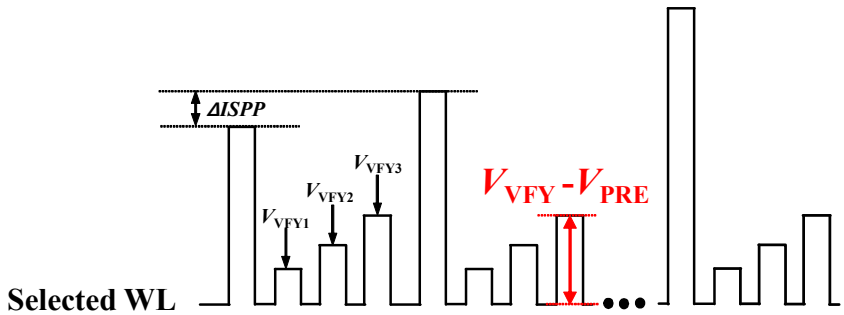


Fig. 5.19. Characteristics of I_{BL} versus time in abnormal cell when (a) the abnormal cell is erased to have a V_{th} of -2 V before P/E cycling stress, and (b) programmed to have a V_{th} of 2 V after P/E cycling stress. Here, the V_{CG} of a selected cell is V_{th}.

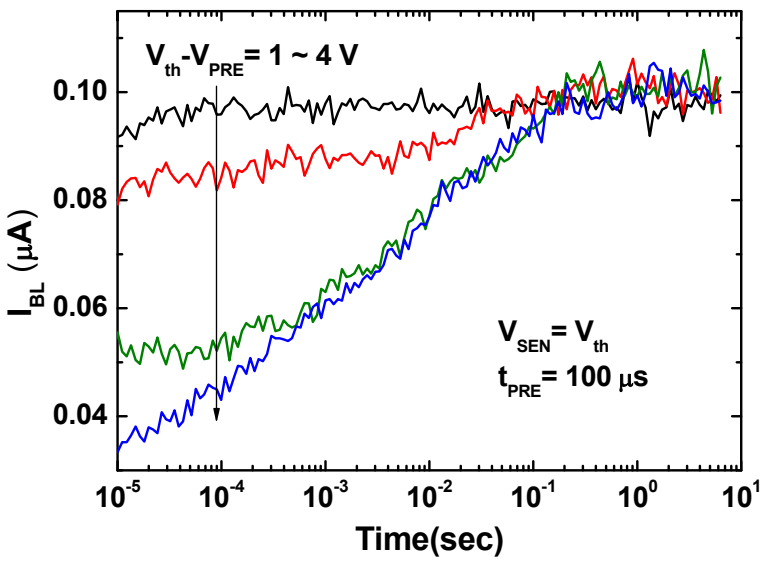
5.6 Effect of hysteresis phenomena on read operation

Fig. 5.20 (a) shows a signal waveform applied to a selected WL during the incremental step pulse programming (ISPP). The ISPP has been widely used in the MLC NAND flash memory in order to achieve the narrow V_{th} distribution of cells [44]. As shown in Fig. 5.20 (a), V_{VFY}s are induced to detect the V_{th} of a cell after the program pulse. Because the potential of the selected WL rises from 0 V to V_{VFY}s during the ISPP, the hysteresis phenomena can occur in an abnormal

cell as shown in Fig. 5.20 (b). Fig. 5.20 (b) shows the transient I_{BL} characteristics of an abnormal cell as a parameter of V_{VFY}-V_{PRE}. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. t_{PRE} and V_{VFY} are 100 μs and V_{th} of a selected cell, respectively. As increasing the V_{VFY}-V_{PRE} from 1 V to 5 V, the variation of transient I_{BL} increases. This result can be explained as follows. For example, when a selected cell is programmed to have a V_{th} of 4 V and the V_{CG} of the selected cell is 0 V, trapped electrons are emitted to the FG because the E_T is higher than the E_F of FG (E_T- E_F>0) , resulting in the decrease of I_{BL}. When the V_{CG} of the selected cell is V_{VFY} (=4 V), electrons in the FG are captured into traps because the E_T is lower than the E_F of FG (E_T- E_F<0), which leads to the increase of I_{BL} as shown in Fig. 5.20 (b).



(a)

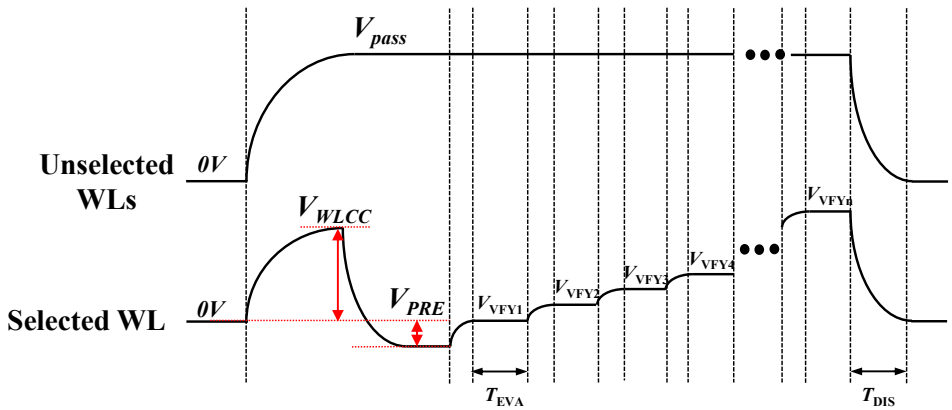


(b)

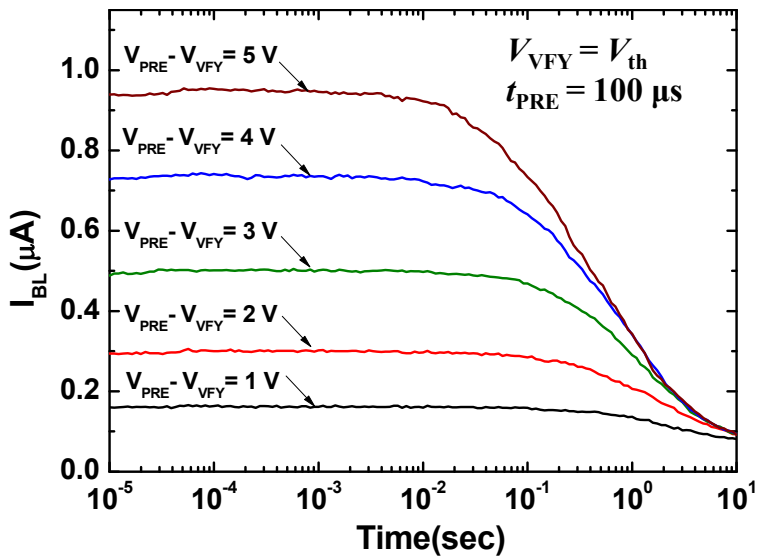
Fig. 5.20. (a) Signal waveform of a selected WL during the incremental step pulse programming (ISPP). (b) Transient I_{BL} characteristics of an abnormal cell as a parameter of V_{VFY}-V_{PRE}.

Fig. 5.21 (a) shows the signal waveforms applied to a selected WL and unselected WLs during the read operation. As a result of scaling down, the

capacitive coupling between the selected WL and unselected WLs increases [45], [46]. As shown in Fig. 5.21 (a), the potential of a selected WL bounces as V_{WLCC} when the potential of unselected WLs rise to V_{pass}. Because the potential of the selected WL rises to V_{WLCC} before biasing V_{VFY1}, the hysteresis phenomena can occur in an abnormal cell during the evaluation time (T_{EVA}) as shown in Fig. 5.21 (b). Fig. 5.21 (b) shows the transient I_{BL} characteristics of an abnormal cell as a parameter of V_{PRE}-V_{VFY}. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. t_{PRE} and V_{VFY} are 100 μs and V_{th} of a selected cell, respectively. With increasing the V_{PRE}-V_{VFY} from 1 V to 5 V, transient I_{BL} increases due to the same reason as that mentioned in Fig. 5.14. If a selected cell is an abnormal cell and programmed to have a V_{th} of V_{VFY1}, the read failure occurs during t_{EVA}. To remove the read failure due to the hysteresis phenomena, a suitable negative bias should be applied to the selected WL before biasing V_{VFY1} because electrons trapped in the bottom oxide of the IPD due to the V_{WLCC} are emitted to the FG so that we can eliminate the effect of hysteresis phenomena.



(a)



(b)

Fig. 5.21. (a) Signal waveforms of a selected WL and unselected WLs during the read operation. (b) Transient I_{BL} characteristics of an abnormal cell as a parameter of V_{PRE}-V_{VFY}.

Fig. 5.22 (a) shows the measured I_{BL}-V_{CG} characteristics of an erased abnormal cell in a 26 nm NAND flash memory string. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 6.5 V and 0.8 V, respectively, when unselected cells are erased to have a V_{th} of -1.5 V. The I_{BL} of a selected cell is measured by using the up-scan reading and down-scan reading. As compared with an abnormal cell in a 48 nm NAND flash memory string, an abnormal cell in a 26 nm NAND flash memory string has the larger ΔV_{th} (~ 1.395 V) as shown in Fig. 5.22 (a). From the results of Fig. 5.22 (a), the ΔV_{th} due to hysteresis phenomena will be more severe as the cell size scales down. Fig. 5.22 (b) shows the transient I_{BL} characteristics of the abnormal cell in the 26 nm NAND flash memory string when the abnormal cell is erased or programmed. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 6.5 V and 0.8 V, respectively. t_{PRE} and V_{VFY} are 1 s and V_{th} of the selected cell, respectively. As shown in Fig. 5.22 (b), the behavior of transient I_{BL} in the 26 nm NAND flash memory string is the same as that in the 48 nm NAND flash memory string. Therefore, the read failure which was mentioned above also occurs in 26 nm NAND flash memory strings during T_{EVA} due to the hysteresis phenomena.

Fig. 5.23 (a) shows the signal waveforms applied to a selected WL and unselected WLs with and without a negative pre-bias (V_{PRE2}) before inducing the verifying bias during the read operation. Fig. 5.23 (b) shows the transient I_{BL} characteristics of an abnormal cell as a parameter of V_{PRE2}. Here, $V_{DSL,SSL}$,V_{pass}, and V_{BL} are 4 V, 5 V and 1 V, respectively. t_{PRE1} and t_{PRE2} are 10 μs and 20 μs,

respectively. V_{th} of a selected cell and V_{VFY} are 0.5 V and 0 V, respectively. In Fig. 5.23(b), the variation of I_{BL} due to hysteresis phenomena decreases with increasing $|V_{PRE2}|$ because of pre-emission of electrons trapped in IPD. As shown in Fig. 5.23(b), a suitable negative bias (V_{PRE2}) should be applied to the selected WL before biasing V_{VFY} to remove the read failure due to the hysteresis phenomena.

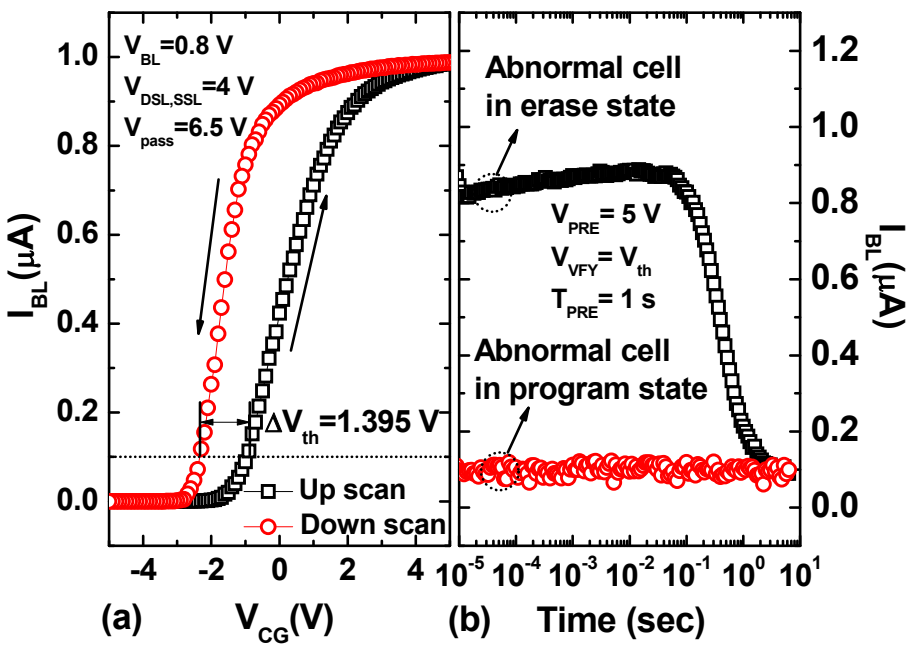
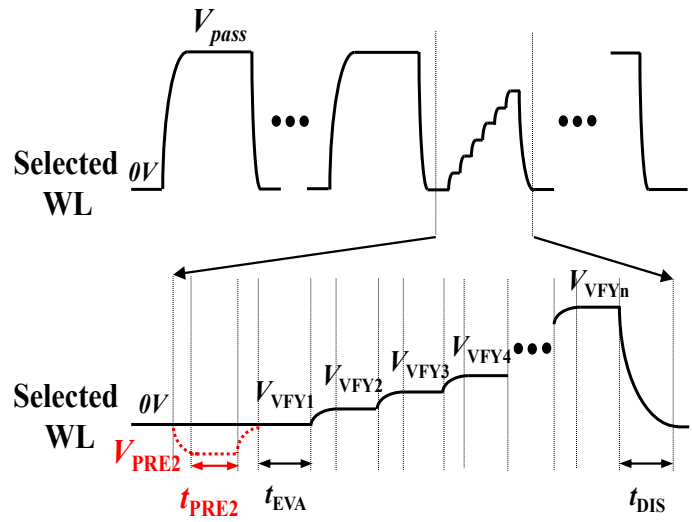
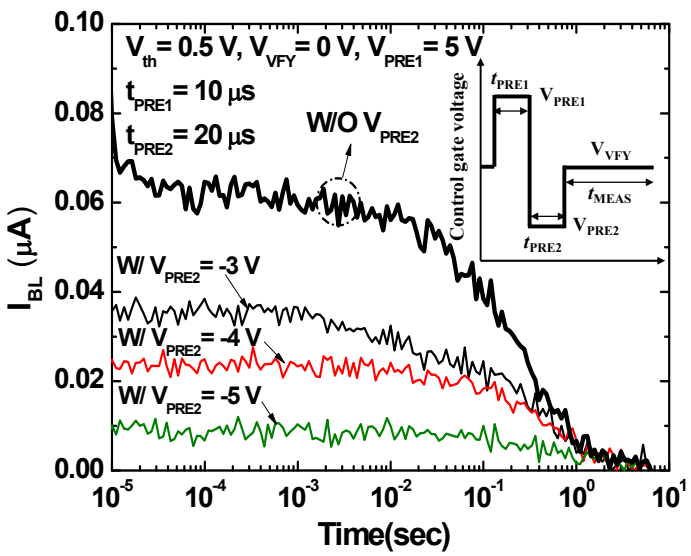


Fig. 5.22 (a) Measured I_{BL}-V_{CG} characteristics of an abnormal cell in erased state in a 26 nm NAND flash memory string by using DC measurement. (b) Transient I_{BL} characteristics of the abnormal cell in the 26 nm NAND flash memory string when the abnormal cell is erased or programmed.



(a)



(b)

Fig. 5.23 (a) Signal timing diagram of a selected word-line for read operation with and without V_{PRE2}. (b) Transient I_{BL} characteristics of an abnormal cell with and without V_{PRE2}. The inset shows the pulse waveform of V_{CG} for transient I_{BL}.

Conclusions

In this dissertation, we investigate reliability issues in floating-gate NAND flash memory through numerical device simulation and measuring the fabricated floating-gate NAND flash memory. For the first time, we extracted the exact position (x_T and y_T) and energy of a trap in tunnel oxide which induces RTN by considering the channel resistances of pass cells in floating gate NAND flash memory string. The effect of adjacent bit-line cell interference on RTN was investigated through 3-D device simulation and measurement in 32 nm NAND flash memory. It was shown that the state (program or erase) of adjacent bit-line cells affects appreciably the distribution of J_e along the channel width direction of a read cell, and ΔI_{BL} due to RTN is changed as a result. We have also shown that the interference from the adjacent bit-line cells changes $\ln(\tau_c/\tau_e)$ by changing trap energy. The change of ΔI_{BL} and $\ln(\tau_c/\tau_e)$ will be more severe due to the increasing interference from adjacent bit-line cells as the cell size scales down. Moreover, the trap position (z_T) along the channel width direction was also extracted by using interference between adjacent bit-lines. In order to suppress effect of RTN current fluctuation in NAND flash memory and reduce read error during read operation, we proposed new read method by using hysteretic

characteristics of RTN. By controlling the pre-bias in μs range, it was confirmed that our method could suppress effectively the effect of RTN during read operation in NAND flash memory. Finally, hysteresis phenomena have been investigated through the pulsed *I-V* and fast transient I_{BL} measurement in NAND flash memory strings. It was shown that the hysteresis phenomena are originated by traps in the bottom oxide of IPD, which can make an error in verifying a cell's state during read operation. We observed the transient bit-line current (I_{BL}) characteristics due to the hysteresis phenomena under various conditions such as temperature, pre-bias voltage (V_{PRE}), and program (P) /erase (E) cycling. In order to reduce the read failure in NAND flash memory, a new read method which suppresses the effect of hysteresis phenomena was proposed.

Appendix

Modeling of ΔI_{BL} due to RTN considering bit-line interference

A.1 Introduction

NAND flash memory has been growing rapidly in terms of popularity in recent years to meet the increasing demand for portable and embedded devices. According to a projection by the 2013 International Technology Roadmap for Semiconductors (ITRS), the physical gate length of NAND flash memory can be scaled down to 12 nm, with the maximum number of bits per cell becoming three bits due to the lower cost per bit projected for 2015 [1]. As a result of the scaling down and increasing number of bits per cell, various problems have arisen with NAND flash memory, such as cell-to-cell interference, a reduction of the on-cell string current, read disturbances and others [2], [25], [47]. Among these issues, random telegraph noise (RTN) caused by the capture/emission of an electron at a trap has become a critical issue, because multi-level-cell (MLC) NAND flash

memory requires a narrow threshold voltage (V_{th}) distribution for a stable read operation [3]. Recently, RTN in NAND flash memory has been examined closely by many groups. In scaled flash memory, RTN is influenced by the shape and doping profile of the channel. This is especially true for the random variations such as random dopant fluctuation (RDF), line edge roughness (LER), oxide thickness fluctuation (OTF) and others, which can lead to the creation of a percolation path in the channel [48]-[51]. We also demonstrated the effect of adjacent bit-line (BL) cell interference on BL current fluctuations (ΔI_{BL}) due to RTN and a methodology that allows the extraction of the 3-D trap position experimentally in NAND flash memory strings [9]. According to our results, ΔI_{BL} due to RTN ranges from ~48 nA to ~63 nA with the state of adjacent BL cells, as the interference between adjacent BLs significantly affects the current density distribution of a read cell in NAND flash memory strings [9], [52]. Therefore, it is very useful to model the RTN behavior due to the interference when analyzing the V_{th} distribution of NAND flash memory. A physical model of ΔI_{BL} will be very helpful for readers who are working on the problem of RTN in various devices. Such a model can also be expanded to analyses of RTN in other devices.

In this section, we proposed a characteristic function which takes into account the relationship between the distribution of the integrated electron current density (J_0) without a trapped electron and J_0 without a trapped electron in the tunneling oxide considering a physical model. We also model the ΔI_{BL} of

RTN by considering the state (program (P) or erase (E)) functions of adjacent BL cells and the trap positions along the direction of the channel width.

A.2 Device structure

The floating-gate NAND flash memory in this work was fabricated by applying 32 nm technology. A NAND cell string consists of sixty-four unit cells, two dummy cells, a drain select line (DSL) transistor and a source select line (SSL) transistor. For a three-dimensional (3-D) device simulation, a NAND flash memory cell array which consists of one word-line (WL) and three BLs was prepared with the same structure.The cells in the simulation have a channel length and width of 32 nm, a tunneling oxide thickness (t_{ox}) of 7.9 nm, uniform channel doping of 2×10^{17} cm^{-3}, and peak source/drain doping of 1×10^{19} cm^{-3}. The space length between adjacent BLs is 32 nm and the space between adjacent BLs is filled with the oxide. We obtained the simulation data by solving the Poisson and drift-diffusion equations in the read condition (BL bias (V_{BL})=0.5 V, control-gate bias for an I_{BL} of 100 nA).

A.3 Results and discussion

Fig. A.1 shows the measured ΔI_{BL} with the state of adjacent bit-line cells in a 32 nm NAND flash memory cell string. The inset of Fig. A.1 represents a part

of measured RTN waveform and low and high I_{BL}s correspond to the capture and emission of an electron at a trap, respectively. In this sample, ΔI_{BL} due to RTN ranges from ~34 nA to ~45 nA with 4 different states of adjacent bit-line cells owing to the effect of adjacent bit-line cell interference [9], [52]. As mentioned above, ΔI_{BL} due to RTN is influenced by the percolation path in the channel, and the path can be controlled by the cell state (program or erase) of adjacent bit-lines. So, the percolation path induced by the cell state was taken into account in modeling and verification of ΔI_{BL} due to RTN in this work.

Fig. A.2 shows the simulated distribution of J_0 along the channel width direction (z-direction) while changing the states of the adjacent BL cells. Because each adjacent BL cell has a program (P) or an erase (E) state, we can consider four different modes (E/E, E/P, P/E, and P/P). Here, the adjacent BL cells are programmed to have a V_{th} of 3 V or are erased to have a V_{th} of -3 V. The read cell is in a fresh state, meaning that it has a V_{th} of nearly 0 V to minimize the electric field from the recessed control gate [17], [52]. Each solid symbol represents the J_0 from the channel surface to a deep vertical position at each position along the z-direction when I_{BL} is 100 nA at a given V_{BL} of 0.5 V. The distribution of J_0 is fitted to the simulation data using a polynomial function (dashed lines). As the cell size scales down, NAND flash memory is influenced severely by cell-to-cell interference caused by the increased parasitic capacitance. Therefore, the distribution of J_0 along the z-direction in a read cell (BL_n cell)

changes significantly with the states of the adjacent BL cells (BL_{n-1} and BL_{n+1} cells), as shown in Fig. A.2. For example, the J_0 of a read cell is crowded toward the BL_{n-1} side (the position from the center to the left edge of the channel width) in the z-direction, as shown by the solid triangles in Fig. A.2, when the BL_{n-1} and BL_{n+1} cells are erased and programmed, respectively.

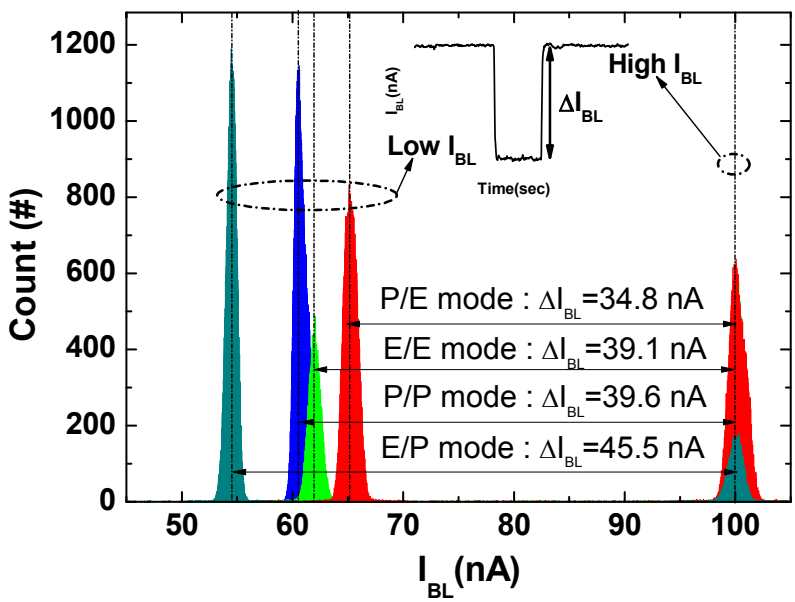


Fig. A.1. Distributions of measured ΔI_{BL}s of a read cell with four different modes in a 32 nm NAND flash memory cell string. Here, I_{BL} was fixed at 100 nA by controlling the control-gate bias of the read cell at a V_{BL} of 0.8V and a pass bias of 6.5 V. The adjacent BL cell is programmed to have a V_{th} of 3 V or erased to have a V_{th} of -3 V, and the read cell is set to have a V_{th} of 0 V.

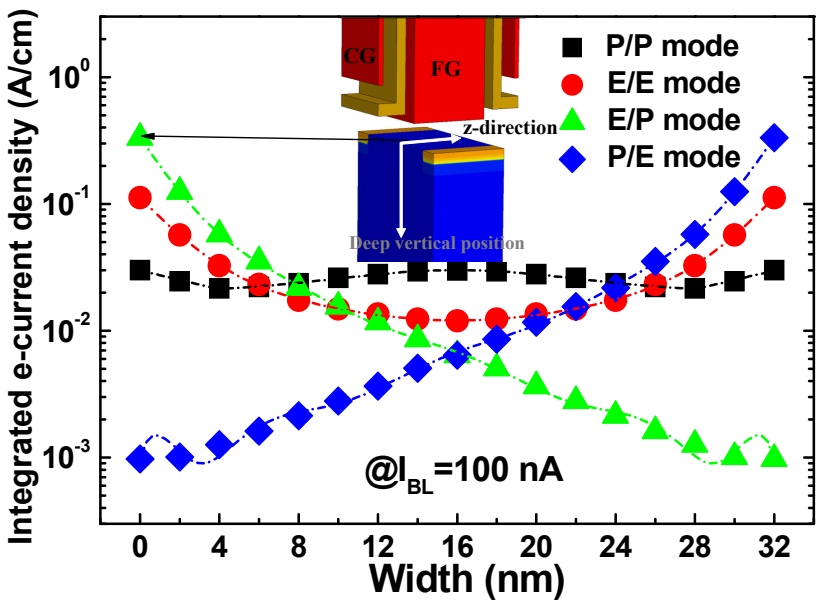


Fig. A.2. Simulated distribution of J_0 along the channel width direction (z-direction) with four different modes of the states of the adjacent cells. Each solid symbol represents J_0 from the surface to a deep vertical position at each position along the z-direction, as shown in the inset. Dashed lines represent the fitted curves of the J_0 distributions.

As mentioned above, the effect of interference caused by adjacent BL cells should be considered when modelling ΔI_{BL} because the distribution of the channel electron density in a read cell changes with the states of the adjacent BL cells [9], [52]. As a result, we need to calculate the electrical blockade length (L_t) with four different modes of the states of adjacent BL cells, as shown in Fig. A.3. Each solid symbol and dashed line represent the calculated value of L_t and the

fitting result of L_t, respectively, according to a polynomial function with the four different modes of the states of adjacent BL cells. The charges transported through the channel are blockaded over some width of L_t by the trapped charge, with L_t given by [8], [9],

$$L_t = \frac{L_s L_c}{L_s + L_c} \quad where, L_s = \sqrt{\frac{4\varepsilon_s kT}{q^2 n(z)}} \quad and \quad L_c = \frac{2q^2}{4\pi\varepsilon_s kT} \qquad \text{Eq. (A.1)}$$

where q is the electron charge, k is the Boltzmann's constant, T is the absolute temperature, and the $n(z)$ is the electron concentration in the channel along the z-direction. L_C is double the critical radius from the trapped electron, where the Coulomb potential energy is equal to the carrier-average kinetic energy kT in a two-dimensional electron gas (2DEG) [53], [54], and L_c is approximately 9.5 nm at 300 K. L_S is the screening length by the 2DEG [53], [54]. L_S is calculated by considering n, which changes according to the electric field from the adjacent BL cells when the adjacent BL cells are programmed or erased. Here, the values of n with four different modes of the states are extracted at a depth of 1 Å below the surface along the z-direction when I_{BL} is 100 nA at a given V_{BL} of 0.5 V. We assume that a trapped electron is located within the tunneling oxide near the surface of the channel. As shown in Fig. A.3, the distribution of L_t along the z-direction changes significantly with the state of the adjacent BL cells.

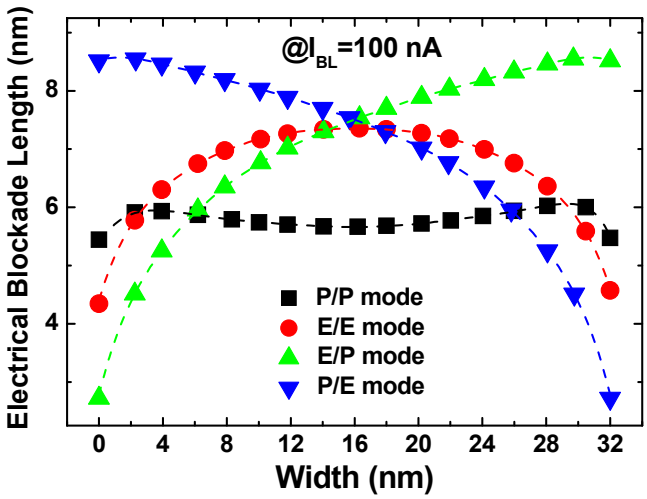


Fig. A.3. Distribution of the electrical blockade length ($L_t(z_T)$) in a read cell along the channel width direction with the states of the adjacent BL cells.

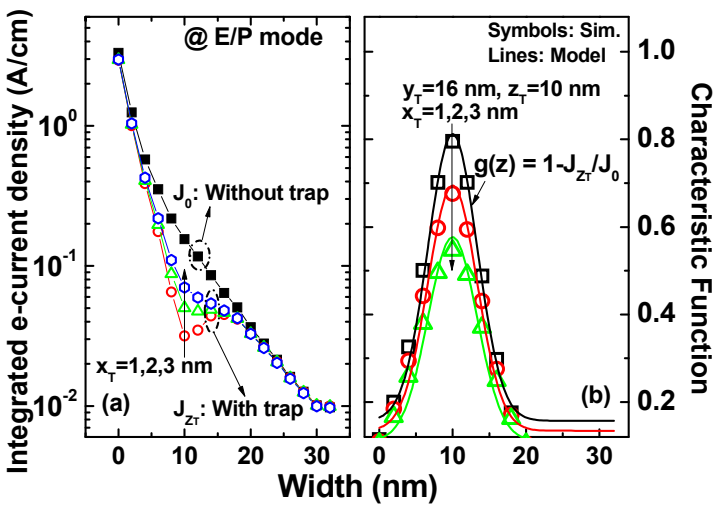


Fig. A.4. (a) Distribution of J_0 along the z-direction with and without a trapped electron in the E/P mode. (b) Simulated (open symbols) and calculated (lines) characteristic function in the E/P mode..

This section demonstrates the extraction of ΔI_{BL} versus z_T with four different modes of adjacent BL cells. Fig. A.4 (a) shows the simulated distribution of J_0 along the z-direction with and without a trapped electron in the E/P mode. Here, the distribution of J_0 along the z-direction is extracted 16 nm away from the source edge when I_{BL} is 100 nA at a given V_{BL} of 0.5 V. The trap position along the channel length direction (y_T) and z_T are 16 nm and 10 nm, respectively. The trap position within the tunneling oxide from the channel surface (x_T) changes from 1 nm to 3 nm. When an electron is captured in a trap in the tunneling oxide, J_0 under a trapped electron decreases dramatically, as shown in Fig. A.4 (a), which leads to a decrease of I_{BL}. Consequently, the ΔI_{BL} resulting from the trap is given by

$$Area = \Delta I_{BL} = \int_0^W J_0 - J_{z_T} dz = \int_0^W J_0 \cdot \left(1 - \frac{J_{z_T}}{J_0}\right) dz = \int_0^W J_0 \cdot g(z) dz \qquad \text{Eq. (A.2)}$$

where J_{ZT} and J_0 are respectively the integrated electron current densities from the surface to a deep vertical position at each position along the z-direction when a trap at z_T captures and emits an electron. In order to calculate ΔI_{BL} due to the trap, it is necessary to obtain $g(z)$, as shown in Eq. (A.2). In previous work [9],[52], J_{ZT}/J_0 could be fitted well to a Gaussian amplitude function ($h(z)$). The difference between J_0 and J_{ZT} is the integrated current density fluctuation; it can be expressed as $J_0 \cdot (1 - h(z))$. Here, $1 - h(z)$ is termed the characteristic function,

($g(z)$= 1- J_{ZT}/J_0), which has a Gaussian functional form. The g(z) is determined as follows:

$$g(z) = \left(y_0 + A \cdot \exp\left(\frac{-(z - z_T)^2}{2w(z_T)^2} \right) \right) \cdot \left(1 - \frac{x_T}{t_{ox}} \right) \quad \text{Eq. (A.3)}$$

In this equation, y_0 and A are the fitting parameters, (1-x_T/t_{ox}) is a physical term which reflects the x_T effect [55], [56], and $2w(z_T)^2$ is determined by $[0.5L_t(z_T)]^2 \cdot [\ln(A/(1-e^{-1}-y_0))]^{-1}$. Note that y_0 and A are constant in each mode of the adjacent BL cells; these corresponding values are fixed at 0.18 and 0.75 in this work. Fig. A.4 (b) shows the simulated and calculated $g(z)$ in E/P mode when a trapped electron is located at z_T=10 nm. Here, y_T is 16 nm and x_T is changed from 1 nm to 3 nm. Open symbols and lines represent the simulation data of $g(z)$ and the calculated data of $g(z)$ according to Eq. (A.3), respectively. From the results of Fig. A.4 (b), the calculated data of $g(z)$ is in good agreement with the simulation data of $g(z)$.

Fig. A.5 shows an example in which ΔI_{BL} is extracted with the trap position along the z-direction (z_T) in the E/P mode. Fig. A.5(a) again shows the distribution of J_0 along the z-direction and the fitted curve (dashed line) of J_0 in the E/P mode. Here, the distribution of J_0 along the z-direction is extracted 16 nm away from the source edge. Fig. A.5(b) shows $g(z)$ as obtained after taking L_t into account in the E/P mode when a trapped electron is located at z_T=2, 10, 20

and 30 nm. As L_t along the z-direction changes due to interference from adjacent BL cells, $g(z)$ at each z_T also changes while maintaining nearly the same peak, as shown in Fig. A.5(b). By multiplying the fitting result of J_0 (=$f(z)$) and $g(z)$, as shown in Fig. A.5(c), we can express the amount of J_0 fluctuation due to a trapped electron at each position along the z-direction. Finally, ΔI_{BL} with z_T can be obtained by integrating $f(z)\cdot g(z)$ from z=0 to z=32 nm. This is given by

$$\Delta I_{BL}(z) = \int_0^W f(z)\cdot g(z-\tau)d\tau \qquad \text{Eq. (A.4)}$$

Fig. A.6 shows the simulated ΔI_{BL} (symbols) and the calculated ΔI_{BL} (dashed lines) according to Eq. (A.4) with z_T and x_T as parameters of the states of the adjacent BL cells. Here, y_T is 16 nm. The x_T and z_T change from 1 nm to 3 nm and from 0 nm and 32 nm, respectively. The ΔI_{BL}s are obtained at an I_{BL} of 100 nA. Bias conditions are identical to those in Fig. A.2. The ΔI_{BL} calculation routine was coded with Matlab. From the results shown in Fig. A.5, the model of ΔI_{BL} expresses a similar trend with the 3-D simulation results, and the error between the model of ΔI_{BL} and the 3-D simulation data is within ~14%. The error is maximized when the trapped electron is located at z_T=0 nm in the E/P mode because the 'tip' effect [52] is maximized and excluded in the calculated $g(z)$. Nevertheless, we ruled out the 'tip' effect in the proposed ΔI_{BL} model, as the range of error increases by only ~4% due to the 'tip' effect and because the 'tip'

effect complicates the ΔI_{BL} model. The proposed ΔI_{BL} model can reflect the effect of a percolation path well because ΔI_{BL} is extracted from the electron current density, which automatically reflects the percolation path generated by the states (P or E) of the adjacent cells; the electrical blockade length (L_t) is calculated on the basis of $n(z)$, which can change according to the states of the adjacent cells. Here, it is important to note the percolation path is generated by the states of the adjacent cells. If there is a percolation path generated by random dopant fluctuation (RDF) in the channel, the electron current density and $n(z)$ obtained from only a single device simulation include the percolation effect when a trap is empty. In this work, only one device simulation has a significant meaning at a fixed state of the adjacent cells, as it solves complicated factors such as the cell geometry, the RDF (if any exists), and any interference. For example, when the adjacent BL states (P or E) are fixed, only one device simulation is enough, and allows the determination of the integrated current density (J_0) and $n(z)$. Based on $n(z)$, we can obtain L_t and $g(z)$, as shown in (3), using the value of L_t. Finally, ΔI_{BL} is calculated by integrating $f(z) \cdot g(z)$. Without any additional device simulations, we can calculate the ΔI_{BL}s with the changes in x_T and z_T using our compact model. If we calculate the ΔI_{BL}s with the trap position without using the model, it takes at least 10 times as long.

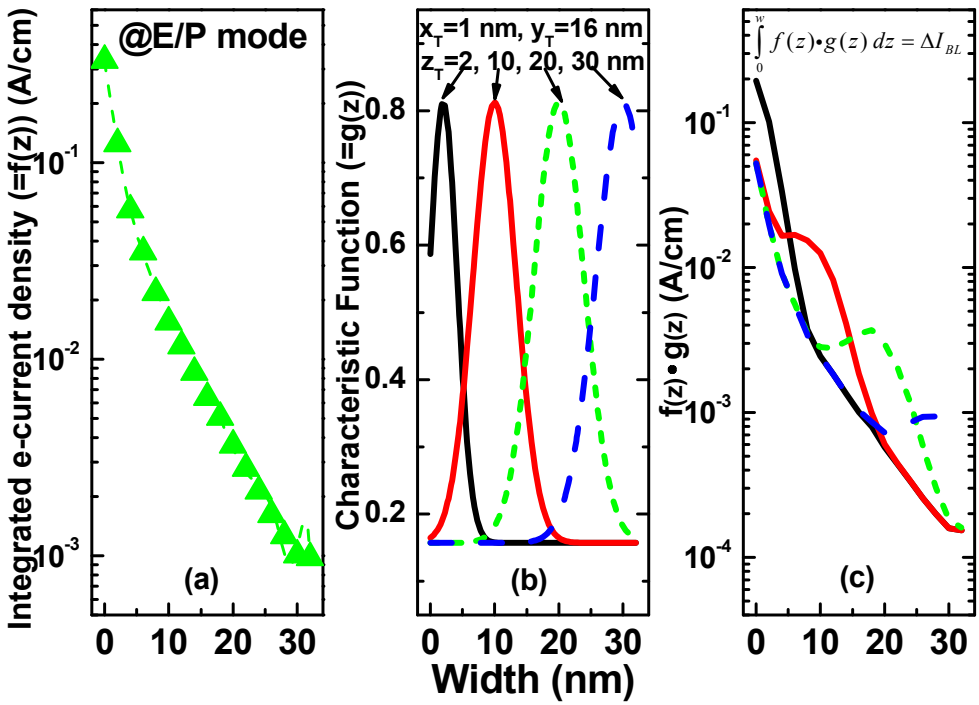


Fig. A.5. (a) Distribution of J_0 along the z-direction and the fitting result (dashed line) of J_0 in the E/P mode. (b) Characteristic function, which has a Gaussian functional form, is obtained while accounting for L_t in the E/P mode when a trapped electron is located at z_T=2, 10, 20 and 30 nm. (c) Multiplication of J_0 along the z-direction ($f(z)$) and the characteristic function ($g(z)$) at z_T=2, 10, 20 and 30 nm. Here, x_T and y_T are 1 nm and 16 nm, respectively.

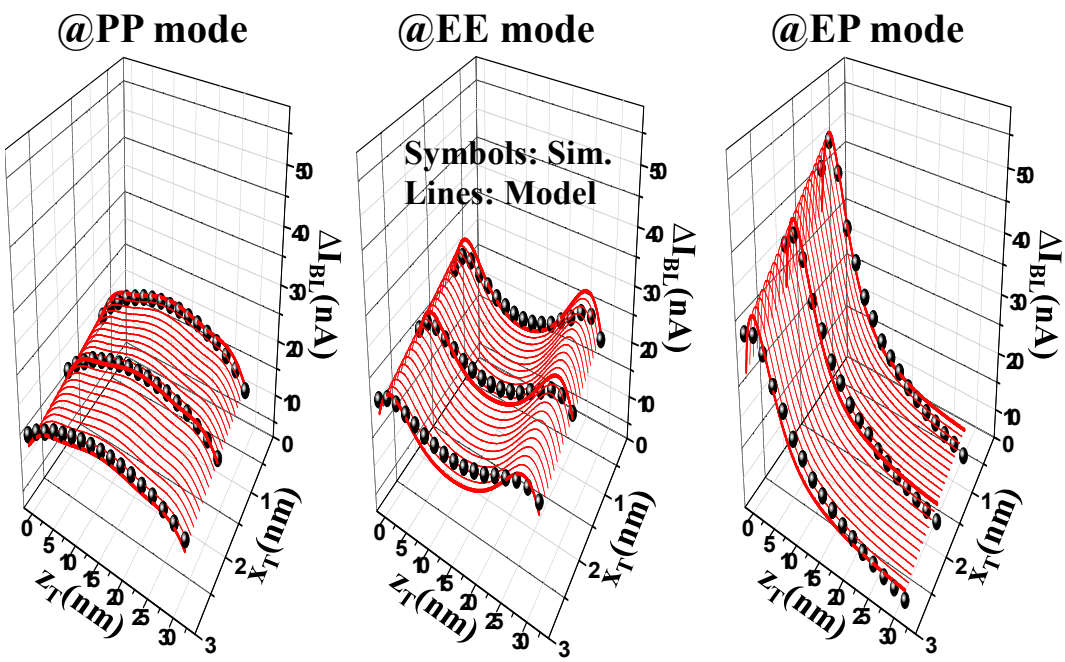


Fig. A6. ΔI_{BL} with z_T and x_T as a parameter of the state of the adjacent BL cells. Here, y_T is 16 nm. Values of x_T and z_T change from 1 nm to 3 nm and from 0 nm to 32 nm, respectively. Solid symbols and lines respectively represent the simulated ΔI_{BL} and the calculated ΔI_{BL} using Eq. (A.4).

Bibliography.

[1] *International Technology Roadmap for Semiconductors*, 2013. [Online]. Availabel: http://public.itrs.net

[2] K.-T. Park, M. Kang, D. Kim, S.-W. Hwang, B. Y. Choi, Y.-T. Lee, C. Kim, and K. Kim,"A zeroing cell-to-cell interference page architecture with temporary LSB storing and parallel MSB program scheme for MLC NAND Flash memories," *IEEE J. Solid-State Circuits,* vol. 43, pp. 919–928, Apr. 2008.

[3] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, "The impact of random telegraph signals on the scaling of multilevel flash memories," *in Proc. IEEE Symp. VLSI Circuit*, pp. 112–113, 2006.

[4] Kirk Prall, and Krishna Parat, "25nm 64Gb MLC NAND technology and scaling challenges," *in Proc. IEEE IEDM Tech. Dig.,* pp. 102-105, 2010.

[5] Gabriel Molas, Damien Deleruyelle, Barbara De Salvo, Gérard Ghibaudo, Marc Gély, Luca Perniola, Dominique Lafond, and Simon Deleonibus, "Degradation of

floating-gate memory reliability by few electron phenomena," *IEEE Trans. on Electron Devices*, vol. 53, no. 10, pp. 2610–2619, Oct. 2006.

[6] K. Fukuda, Yuui Shimizu, K. Amemiya, M. Kamoshida, and C. Hu et al., "Random telegraph noise in flash memories - model and technology scaling," *in Proc. IEEE IEDM Tech. Dig.*, pp.169–172, 2007.

[7] Sung-Ho Bae, Jeong-Hyun Lee, Hyuck-In Kwon, Jung-Ryul Ahn, Jae-Chul Om, Chan Hyeong Park, and Jong-Ho Lee, "The 1/f noise and random telegraph noise characteristics in floating-gate NAND flash memories," *IEEE Trans. on Electron Devices*, vol. 56, no. 8, pp. 1624-1630, Aug. 2009.

[8] Sung-Min Joe, Jeong-Hyong Yi, Sung-Kye Park, Hyungcheol Shin, Byung-Gook Park, Young June Park, and Jong-Ho Lee, "Threshold voltage fluctuation by random telegraph noise in floating gate NAND flash memory string," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 67-73, Jan. 2011.

[9] Sung-Min Joe, Min-Kyu Jeong, Ju-Wan Lee, Myoung-Sun Lee, Bong-Su Jo, Jong-Ho Bae, Sung-Kye Park, Kyoung-Rok Han, Jeong-Hyong Yi, Gyu-Seong Cho and Jong-Ho Lee, "Extraction of 3-D trap position in NAND flash memory considering channel resistance of pass cells and bit-line interference," *in Proc. IEEE Symp. VLSI Technology*, pp. 76–77, 2011.

[10] Sung-Min Joe, Jeong-Hyong Yi, Sung-Kye Park, Hyuck-In Kwon, and Jong-Ho Lee, "Position-dependent threshold-voltage variation by random telegraph noise in NAND flash memory strings," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 635–

637, Jul. 2010.

[11] L. Larcher, P. Padovani, P. Pavan, P. Fantini, A. Calderoni, A. Mauri, and A. Benvenuti, “Modeling NAND flash memories for IC design,” *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1152–1154, Oct. 2008.

[12] Heung-Jae Cho, Younghwan Son, Byoungchan Oh, Seunghyun Jang, Jong-Ho Lee, Byung-Gook Park, and Hyungcheol Shin, "Investigation of gate etch damage at metal/high-k gate dielectric stack through random telegraph noise in gate edge direct tunneling current," *IEEE Electron Device Letters*, Vol. 32, No. 4, pp. 569-571, Apr. 2011.

[13] Sang-Goo Jung, Keun-Woo Lee, Ki-Seog Kim, Seung-Woo Shin, Seaung-Suk Lee, Jae-Chul Om, Gi-Hyun Bae, and Jong-Ho Lee, “Modeling of V_{th} shift in NAND flash-memory cell device considering crosstalk and short-channel effects,” *IEEE Trans. on Electron Devices*, vol. 55, no. 4, pp. 1020–1026, Apr. 2008.

[14] Mincheol Park, Keonsoo Kim, Jong-Ho Park, and Jeong-Hyuck Choi, “Direct field effect of neighboring cell transistor on cell-to-cell interference of NAND flash cell arrays,” *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 174–177, Feb. 2009.

[15] Yi-Hsuan Hsiao, Hang-Ting Lue, Kuang-Yeu Hsieh, Rich Liu and Chih-Yuan Lu, “A study of stored charge interference and fringing field effects in sub-30nm charge-trapping NAND flash,” *in Proc. IEEE IMW*, pp. 1–2, 2009.

[16] Andrea Ghetti, Luca Bortesi, and Loris Vendrame, “3D Simulation study of gate coupling and gate cross-interference in advanced floating gate non-volatile memories,” *Solid-State Electronics*, vol. 49, no. 11, p. 1805-1812, Nov. 2005

[17] Mincheol Park, Eungjin Ahn, Eunsuk Cho, Keonsoo Kim, and Won-Seong Lee, “The effect of negative V_{TH} of NAND flash cells on data retention characteristics,” *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 155–157, Feb. 2009.

[18] A. Ghetti, C. Monzio Compagnoni, F. Biancardi, A. L. Lacaita, S. Beltrami, L. Chiavarone, A.S. Spinelli, and A. Visconti, “Scaling trends for random telegraph noise in deca-nanometer flash memories,” *in Proc. IEEE IEDM Tech. Dig.*, pp. 835-838, 2008.

[19] Ken’ichiro Sonoda, Kiyoshi Ishikawa, Takahisa Eimori, and Osamu Tsuchiya, “Discrete dopant effects on statistical variation of random telegraph signal magnitude,” *IEEE Trans. on Electron Devices*, vol. 54, no. 8, pp. 1918–1925, Aug. 2007.

[20] Asen Asenov, Ramesh Balasubramaniam, Andrew R. Brown, and John H. Davies, "RTS amplitudes in decananometer MOSFETs: 3-D simulation study," *IEEE Trans. on Electron Devices*, vol.50, no.3, pp. 839- 845, Mar. 2003.

[21] Nabil Ashraf, Dragica Vasileska, Gilson Wirth and P. Srinivasan, “Accurate Model for the Threshold Voltage Fluctuation Estimation in 45-nm Channel Length MOSFET Devices in the Presence of Random Traps and Random Dopants," *IEEE Electron Device Lett.*, vol.32, no.8, pp.1044-1046, Aug. 2011.

[22] Asen Asenov, Andrew R. Brown, John H. Davies, Savas Kaya, and Gabriela Slavcheva, "Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs," *IEEE Trans. on Electron Devices*, vol.50, no.9, pp. 1837- 1852, Sep. 2003.

[23] H. Miki, M. Yamaoka, D. J. Frank, K. Cheng, D.-G. Park, E. Leobandung, and K. Torii, "Voltage and temperature dependence of random telegraph noise in highly scaled HKMG ETSOI nFETs and its impact on logic delay uncertainty," *in Proc. IEEE Symp. VLSI Technology*, pp. 137–138, 2012.

[24] Jae-Duk Lee, Sung-Hoi Hur, and Jung-Dal Choi, "Effects of floating-gate interference on NAND flash memory cell operation," *IEEE Electron Device Lett.,* vol. 23, no. 5, pp. 264–266, May. 2002.

[25] Myounggon Kang, Ki-Tae Park, Youngsun Song, Youngho Lim, Kang-Deog Suh, and Hyungcheol Shin, "Improving Read Disturb Characteristics by Self-boosting Read Scheme for MLC NAND Flash Memories", *Jpn. J. appl. Phys*, vol. 48, no.4, pp.1-6, Apr. 2009.

[26] Kinam Kim, "Technology for sub-50nm DRAM and NAND flash manufacturing," *in Proc. IEEE IEDM Tech. Dig.,* pp. 323-326, 2005.

[27] Udayan Ganguly, Yoshitaka Yokota, Jing Tang, Shiyu Sun, Matt Rogers, Miao Jin , Kiran Thadani, Hiroshi Hamana, Garlen Leung, Balaji Chandrasekaran, Sunderraj Thirupapuliyur, Chris Olsen, Vicky Nguyen, and Swami Srinivasan, "Scalability

enhancement of FG NAND by FG shape modification," *in Proc. IEEE IMW*, pp. 1–4, 2010.

[28] M. Florian Beug, Nigel Chan, Timm Hoehr, Lars Mueller-Meskamp, and Michael Specht, "Investigation of program saturation in scaled interpoly dielectric floating-gate memory devices," *IEEE Trans. on Electron Devices,* vol. 56, no. 8, pp. 1698–1704, Aug. 2009.

[29] B. Govoreanu, D. P. Brunco, and J. Van Houdt, "Scaling down the interpoly dielectric for next generation Flash memory: Challenges and opportunities," *Solid-State Electronics*, vol. 49, no. 11, pp. 1841-1848, Nov. 2005.

[30] J. De Vos, et al., "A scalable Stacked Gate NOR/NAND Flash Technology compatible with high-k and metal gates for sub 45 nm generations," *Proc. ICICDT*, pp. 21-24, 2006.

[31] Bogdan Govoreanu, et al., "On the roll-off of the activation energy plot in high-temperature flash memory retention tests and its impact on the reliability assessment," *IEEE Electron Device Lett.,* vol. 29, no. 2, pp. 177–179, Feb. 2008.

[32] Se Hoon Lee, et al., "Investigation on the retention reliability of scaled SiO2/AlxOy/SiO2 inter-poly dielectrics for NAND flash cell arrays," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 266–268, Apr. 2010.

[33] Jong-Ho Lee, et al., "Investigation of reliability issue in tunneling and inter-poly dielectrics in floating gate NAND flash memory cell strings," *IEEE Int. Nanoelectronics Conf.*, pp. 1–2, 2011.

[34] Man Chang, et al., “Transient charge trapping and detrapping properties of a thick SiO2/Al2O3 stack studied by short single pulse Id-Vg,” *Appl. Phys .Lett.,* vol. 94, no. 26, p. 262107, Jul. 2009.

[35] Baojun Tang, et al., “Investigation of abnormal V_{TH}/V_{FB} shifts under operating conditions in flash memory cells with Al2O3 high-κ gate stacks,” *IEEE Trans. on Electron Devices,* vol. 59, no. 7, pp. 1870–1877, Jul. 2012.

[36] Agilent Technologies, inc., Agilent B1530A User's Guide, Aug. 2012

[37] Min-Kyu Jeong, et al., “A new read method suppressing effect of random telegraph noise in NAND flash memory by using hysteretic characteristic,” *in Proc. IEEE Symp. VLSI Circuit*, pp. 154–155, 2013.

[38] Alessio Spessot, et al., “Effect of floating-gate polysilicon depletion on the erase efficiency of NAND flash memories,” *IEEE Trans. Electron Devices*, vol. 31, no. 7, pp. 647-649, Jul. 2010.

[39] Xingsheng Wang, et al., “Statistical variability and reliability in nanoscale finFETs,” *in Proc. IEEE IEDM Tech. Dig.*, pp. 5.4.1-5.4.4, 2011.

[40] M.-K. Jeong, et al., “Characterization of traps in 3-D stacked NAND flash memory devices with tube-type poly-Si channel structure,” in *Proc. IEEE IEDM Tech. Dig.*, pp. 9.3.1-9.3.4, 2012.

[41] Man Chang, *et al*., “Bias stress induced stretched exponential time dependence of charge injection and trapping in amorphous thin film transistors,” *Appl. Phys .Lett.*, vol. 62, no. 11, pp. 1286-1288, Mar. 1993.

[42] K. C. Benny Lee, *et al*., "Application of the Stretched Exponential Function to Fluorescence Lifetime Imaging", *Biophysical Journal,* vol. 81, pp. 1265-1274, 2001.

[43] Tibor Garasser, et al., "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities", *Microelectronics Reliability,* vol. 52, no.1, pp. 39-70, Jan. 2012.

[44] K.D Suh, et al., "A 3.3 V 32Mb NAND flash memory with incremental step pulse programming Scheme," *IEEE Int. Solid-State Circuits Conf.* , pp. 128-129, 1995.

[45] C. Trinh, et al., "A 5.6MB/s 64Gb 4b/Cell NAND flash memory in 43nm CMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 246–247, Feb. 2009.

[46] K. Takeuchi, et al., "A 56nm CMOS 99mm2 8Gb multi-level NAND flash memory with 10MB/s Program Throughput," *IEEE Int. Solid-State Circuits Conf.*, pp. 507-508, Feb. 2006.

[47] Tae-Kyung Kim, et al., "Floating gate technology for high performance 8-level 3-bit NAND flash memory", *Solid-St. Electronics*, vol. 53, issue 7, pp. 792-797, July. 2009.

[48] Gareth Roy, et al., "Comparative simulation study of the different sources of statistical variability in contemporary floating-gate nonvolatile memory," *IEEE Trans. Electron Devices*, vol. 58, no.12, pp. 4155-4163, Dec. 2011.

[49] Andrea Ghetti, et al., "Impact of nonuniform doping on random telegraph noise in decananometer flash memories," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 309-315, Feb. 2012.

[50] Salvatore Maria Amoroso, et al., “Impact of cell shape on random telegraph noise in decananometer flash memories,” *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2774-2779, Oct. 2012.

[51] Fu-Hai Li, et al., “Impact of source/drain junction and cell shape on random telegraph noise in NAND flash memory,” *Jpn. J. Appl. Phys.*, vol. 52, no.7R, p. 074201, 2013.

[52] Sung-Min Joe, et al., “The effect of adjacent bit-line cell interference on random telegraph noise in NAND flash memory cell strings,” *IEEE Trans. Electron Devices,* vol. 59, no. 12, pp. 3568-3573, Dec. 2012

[53] Eddy Simoen, et al., “Explaining the amplitude of RTS noise in submicrometer MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 422-429, Feb. 1992

[54] Ming-Jer Chen, et al., “Probing a nonuniform two-dimensional electron gas with random telegraph signals,” *J. Appl. Phys.*, vol. 103, no. 3, pp. 034511, Feb. 2008.

[55] Nor Hisham Hamid, et al., “Time-Domain Modeling of Low-Frequency Noise in Deep-Submicrometer MOSFET,” *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 245-257, Feb. 2008

[56] K. Kandiah, et al., “A physical model for random telegraph signal currents in semiconductor devices,” *J. Appl. pPhys.,* vol. 66, no. 2, pp. 937-948, Jul. 1988.

초 록

최근 NAND 플래시 메모리가 점차 고집적, 소형화 되면서 트랩에 전자가 capture 또는 emission 되어 발생하는 Random Telegraph Noise (RTN)가 읽기 동작 및 소자의 불안정성 등 심각한 문제를 야기 시키고 있어 메모리 동작 시 중요한 사안으로 대두되고 있다. 또한, Interpoly dielectric (IPD)의 두께가 점점 감소함에 따라, IPD에 존재하는 트랩으로 인해 발생되는 신뢰성문제 또한 중요해지고 있다. 이에 본 논문에서는 Tunneling oxide및 IPD에 존재하는 트랩의 분석을 통해 Floating Gate NAND 플래시 메모리의 신뢰성에 대하여 논하고자 한다.

먼저, Read cell은 NAND string의 구조적인 특성으로 인해 pass cell들의 채널저항 영향을 받게 되며, 트랩의 위치와 에너지 준위를 추출함에 있어 pass cell들의 채널저항을 고려하여야 더욱 정확한 값을 추출할 수 있다는 것을 알 수 있었다. 또한, 최근 소자가 소형화 됨에 따라 인접 cell에 의한 간섭효과가 급속히 커지고 있기 때문에 인접 cell의 간섭효과에 따른 RTN 특성을 보고자 3-D TCAD 시뮬레이션 및 측정을 진행하였다. 인접 cell 상태에 따라, Read cell의 채널 Width 방향의 Electron current density 및 RTN에 의한 비트라인 전류변화, capture/emission time constant가 변화 됨을 3-D TCAD 시뮬레이션 및 측정을 통해 알 수 있었다. 또한, 앞서 pass cell들의 채널저항 효과 및 인접 cell 간섭효과를 이용하여 실제 32nm 및 26nm NAND 플래시 메모리string에서 RTN을 유발하는 트랩의 위치를 Vertical, Lateral, Width 방향으로 추출을 하여 3-D 그래프로 표현을 할 수 있었다. 더 나아가 NAND 플래시 메모리의 읽기 동작 시, RTN의 영향을 줄이기 위하여 ~μsec 범위의 pre-bias를 인가하는 새로운 읽기방법을 제안을 하였으며 측정을 통해 그 효과를 보여주었다.

다음으로는 NAND 플래시 메모리에서 발생하는 hysteresis 현상을 분석하기 위해 pulsed I-V 측정 및 비트라인 전류의 Transient 특성, 시뮬레이션을 진행하였으며, 이는 IPD의 bottom oxide에 존재하는 트랩에 의해 발생된다는 결론을 도출 할 수 있었다. 또한 이런 hysteresis 효과를 줄이기 위해 새로운 읽기방법을 제안을 하였으며 측정을 통해 그 효과를 보여주었다.

마지막 부록에서는 인접 cell 상태에 따라 영향을 받게 되는 간섭효과를 고려하여, 트랩 위치에 따른 비트라인 전류변화에 대한 모델링을 진행하였다. 모델링을 진행하

기 위해 electric blockade length 및 트랩 위치가 고려된 Gaussian 형태를 가진 특성 함수를 정의를 하였고 이를 이용하여 트랩에 의한 비트라인 전류변화를 추출할 수 있었다. 3-D TCAD 시뮬레이션 결과와의 비교를 통해 제안된 모델이 매우 정확하다는 것을 알 수 있었고, 제안된 모델을 이용하면 트랩에 의한 비트라인 전류 변화값을 손쉽게 예측할 수 있을 것으로 예상된다.

주요어: 신뢰성, NAND 플래시 메모리, Random telegraph noise, 비트라인 간섭, 비트라인 전류 변화, 플로팅 게이트, Inter-poly 유전막, Hysteresis

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