Ph.D. DISSERTATION

Tunnel Field-Effect Transistor with Si/SiGe Materials for High Current Drivability

높은 전류구동능력을 위한 Si/SiGe 물질을 가지는 터널링 전계효과 트랜지스터

BY

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DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
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SEOUL NATIONAL UNIVERSITY

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Abstract

For integrated circuits with highly-scaled complementary MOS (CMOS) technology, power dissipation problem has become an important issue since power per chip continues to increases and leakage power dominates in advanced technology nodes. In order to solve power issues, the supply voltage (V_{DD}) scaling is very essential and devices which have low leakage current are needed. Recently, many research groups have studied a tunnel field-effect transistors (tunnel FETs) which is suitable for low operating power device. Tunnel FETs have very low leakage current and small subthrehold swing (SS) at room temperature unlike CMOS because of carrier injection using tunneling.

In this thesis, a novel tunnel FET with SiGe body and elevated Si drain region have been proposed. The proposed tunnel FET has larger current drivability than conventional Si tunnel FETs because it uses a narrow bandgap material for low tunneling resistance. Also, it is expected that electrical characteristics can be improved by using SiGe channel and source for n-channel as well as p-channel operation. In addition, ambipolar current that is caused by band-to-band tunneling (BTBT) between channel and drain can be suppressed by using elevated Si drain region.

For obtaining fundamental electrical properties of tunnel FET with SiGe body, planar structures are firstly fabricated and analyzed with Si tunnel FET. From electrical

characteristics of fabricated devices, it is observed that both n-type and p-type SiGe tunnel FETs have better switching properties than Si devices. Current saturations become faster and drive current shows 10 times more than that of Si tunnel FETs. In addition, BTBT model parameters of Si and Ge materials in fabricated devices are extracted through TCAD simulation. Extracted A and B parameters of BTBT model in Si are 4×10^{14} $cm^{-1}s^{-1}$ and 9.9×10^{6} V/cm. Also, A and B parameters of Ge can be extracted as 3.1×10^{16} $cm^{-1}s^{-1}$ and 7.1×10^{5} V/cm, respectively.

Using calibrated model parameters, proposed tunnel FET is simulated and optimized in terms of switching properties with changing Ge contents, effect of the elevated Si drain region, short-channel effects, inverter operation, and device delay. Based on these optimized simulation results, the proposed tunnel FET is fabricated using spacer technique because it is possible to make self-aligned doping process. Key unit process is as follows: epitaxial growth for Si and SiGe materials, e-beam lithography for active-fin formation, and sidewall spacer gate formation.

For n-channel and p-channel operation, fabricated tunnel FET shows the better electrical characteristics than control groups. Extracted point SS is 51.1 mV/dec for p-type tunnel FET and 87 mV/dec for n-type tunnel FET. Ambipolar current of the proposed tunnel FET is suppressed to 1/100 of that of planar SiGe tunnel FET. Also, in order to analyze current flow mechanism of tunnel FET, the electrical characteristics are measured with temperature variation. As temperature goes up, Shockley-Read-Hall and field-dependent generation are increased resulting in degradation of switching property.

In current saturation region, BTBT which has low temperature sensitivity is dominant on current property.

From this study, it is demonstrated that the novel tunnel FET with SiGe body and the elevated Si drain shows improved electrical performance compared with Si tunnel FET. Also, both n-type and p-type devices can obtain high current drivability and small SS without structure changes. This means that the proposed device has strong advantage in terms of implementing IC with tunnel FET. Thus, it will be one of the promising candidates for next-generation devices.

Key Words: band-to-band tunneling, tunnel field-effect transistor, low operating power device, tunneling resistance, subthreshold swing, ambipolar current.

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Chapter 1

Introduction

1.1 Power issues on CMOS technologies

In semiconductor industries, metal-oxide-semiconductor field-effect transistor (MOSFET) has been scaled down based on Moore's Law. Moore's Law is a theory that the number of transistors in a dense integrated circuit (IC) doubles approximately every two years and it brings more features on chips and provides speed boosts. Thus, for decades, IC has been added to more transistors while reducing the size and cost of a chip. It helps make smartphones, tablet, and desktop computers faster and more power efficient. However, as chip sizes get shrunk, it is more difficult to maintain Moore's Law due to leakage issues [1-3]. Most leakages come from short-channel effects (SCEs) in MOSFETs such as threshold voltage (V_{TH}) roll-off, drain induced barrier lowering (DIBL), punch-through, etc. As a result, power dissipation problem in chips due to

leakage current has become more and more critical. From Fig. 1.1, as gate length scaling, the active power (CV_{DD}^2f) and passive power ($I_{OFF}V_{DD}$) density is increasing. The increase of the power dissipation also induces the slowing down of supply voltage (V_{DD}) scaling. For reducing the power dissipation, V_{DD} should be scaled down. However, in case of the scaling of V_{DD} in MOSFET, gate overdrive voltage (V_{ov}) is decreased and on-current (I_{ON}) becomes smaller. Otherwise, in case of the reduction of V_{TH} in MOSFET, off-current (I_{OFF}) is extremely increased although I_{ON} is increased (I_{OFF} is proportional to $\exp(-qV_{TH}/mk_BT)$) as shown in Fig. 1.2(a). Thus, in order to achieve high I_{ON}/I_{OFF} in a device with lower V_{DD}, it needs a new mechanism device unlike MOSFET that operates by thermal carrier injection over source-side potential barrier as shown in

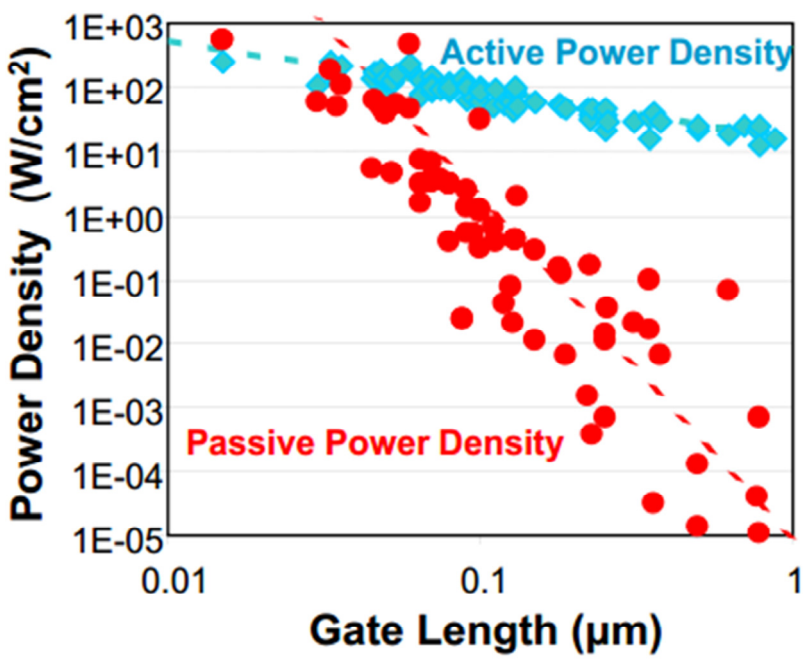


Fig. 1.1. Correlation between power density and gate length.

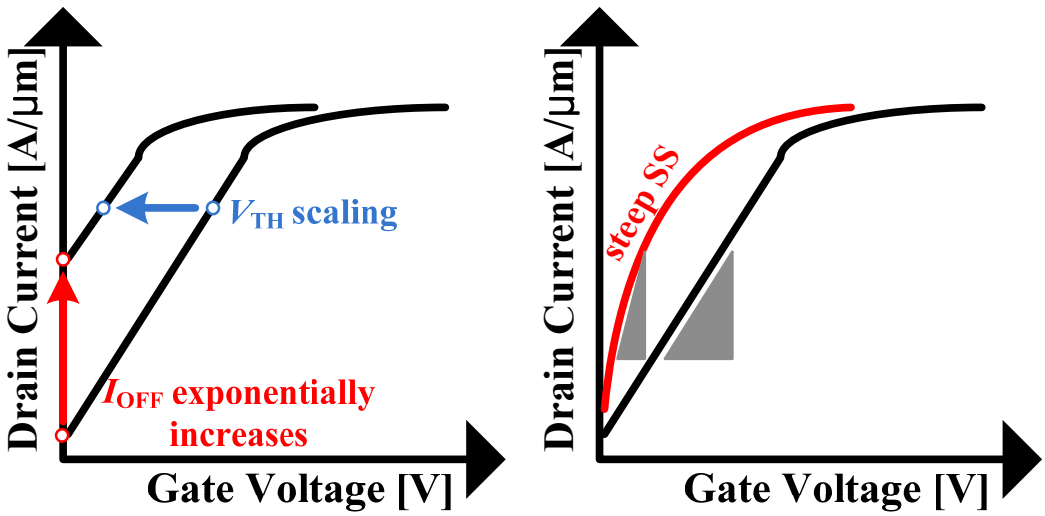


Fig. 1.2. (a) Current characteristics according to V_{TH} scaling in MOSFET and (b) necessity of steep SS for low V_{DD} operating.

Fig. 1.2(b). Recently, various devices have been proposed, one of which is the tunnel field-effect transistor (tunnel FET) as an alternative to low operating power devices [4-6].

1.2 Tunnel field-effect transistor (tunnel FET)

Tunnel FET is based on band-to-band tunneling (BTBT) mechanism where electrons in the valence band of the source region pass through the barrier to the conduction band of the channel region. Thus, it has very small leakage current due to

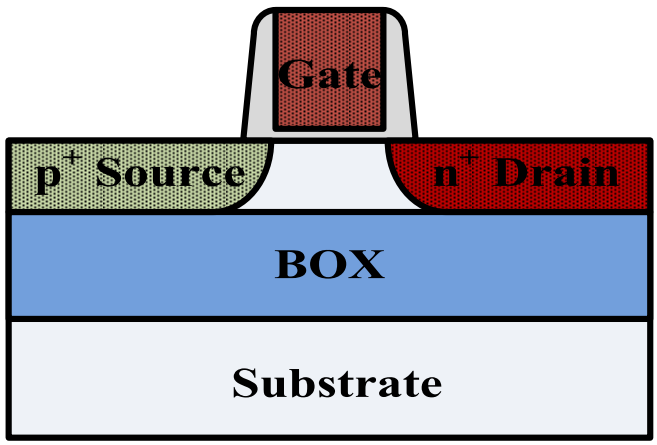
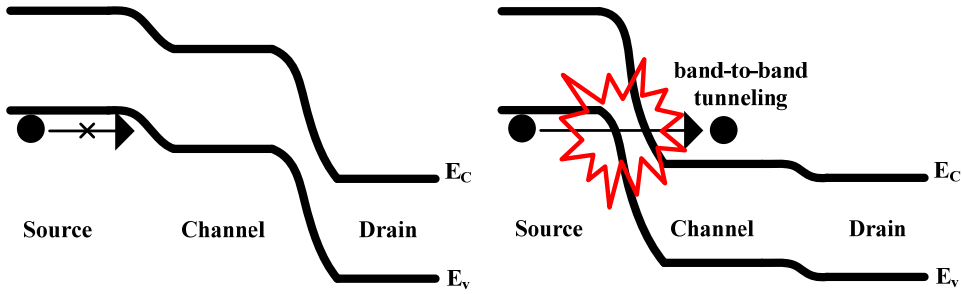


Fig. 1.3. Scheme of n-channel tunnel FET

potential barrier. The basic structure of tunnel FET consists of a gated p-i-n diode where the source and drain have asymmetric dopant type as shown in Fig. 1.3 (n-type tunnel FET). For principle operation, figure 1.4 shows the energy band diagrams in ON/OFF states of tunnel FET. When the device is in the OFF state, the electrons in the valence band of the source region can't be passed to empty states in the conduction band of the channel region by energy barrier. Thus, I_{OFF} is mostly determined by Shockley-Read-Hall (SRH) generation-recombination. As the positive gate voltage (V_{GS}) is applied, the conduction band of the channel region starts to go down. When the conduction band of the channel region is placed below the valence band of the source region, electrons can move to empty states in the channel region resulting in a sudden increase in the drain current (BTBT). Therefore, carriers in the tunnel FET are unaffected by thermal energy unlike MOSFET and subthreshold swing (SS) can be lower than 60 mV/dec at room



(a)ON state (b) OFF state

Fig. 1.4. Energy band diagrams of (a) OFF state (V_{GS} = 0 V, V_{DS} = V_{DD}) and (b) ON state (V_{GS} > V_{TH}, V_{DS} = V_{DD}) in n-type tunnel FET.

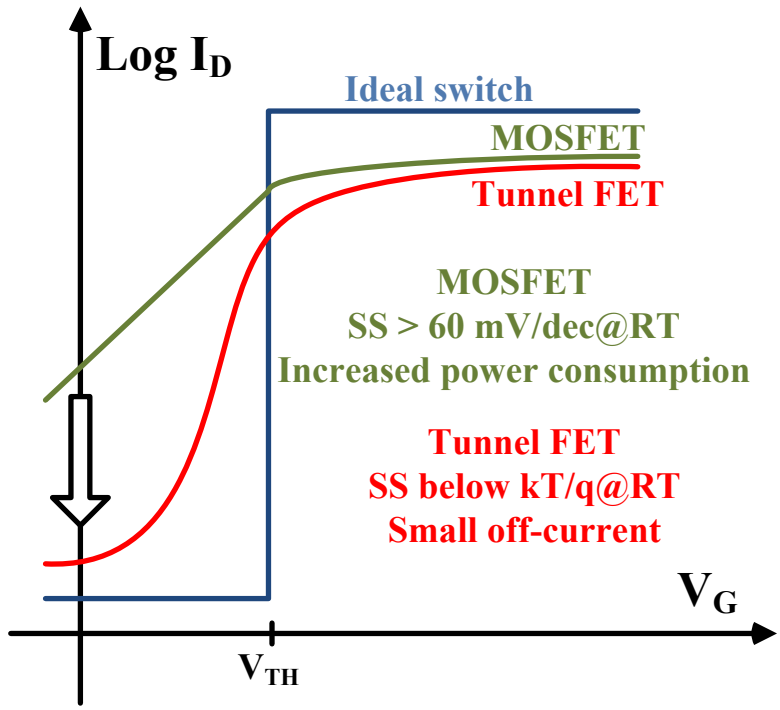


Fig. 1.5. Switching properties of MOSFET and tunnel FET.

temperature. Thus, it is well known that tunnel FET is closed to ideal switch compared with MOSFET and is suitable for low voltage operation as shown in Fig. 1.5.

1.3 Issues in tunnel FET

As mentioned before, tunnel FETs have strong advantages in terms of small SS and I_{OFF}. However, there remains the further question as to commercialization of tunnel FETs. The reason is that tunnel FET has poor current drivability, ambipolar behavior, and non-symmetric doping structure [7-10]. First, for drive current, most reported silicon tunnel FET's performances show very small I_{ON} (< 1 μA/ μm) and poor SS (> 60 mV/dec) properties because silicon material has 1.12 eV of bandgap. In tunnel FET based on BTBT mechanism, bandgap size absolutely affects tunneling current. Also, since it is difficult to make abrupt junction between source and channel in real fabrication process, tunneling resistance becomes larger than expected device design resulting in poor SS characteristics (Fig. 1.6). Therefore, in order to improve current drivability and SS characteristics, it needs to apply narrow bandgap materials and heterojunction technology such as silicon-germanium (SiGe), germanium (Ge), germanium-tin (GeSn), carbon nanotubes, and III-V compound materials [11-28]. Each technology has both merits and demerits. Narrow bandgap materials help to boost current of tunnel FET. However, SRH current is increased because bandgap is smaller than silicon. In case of heterojunction tunnel FET, although fabrication costs are high,

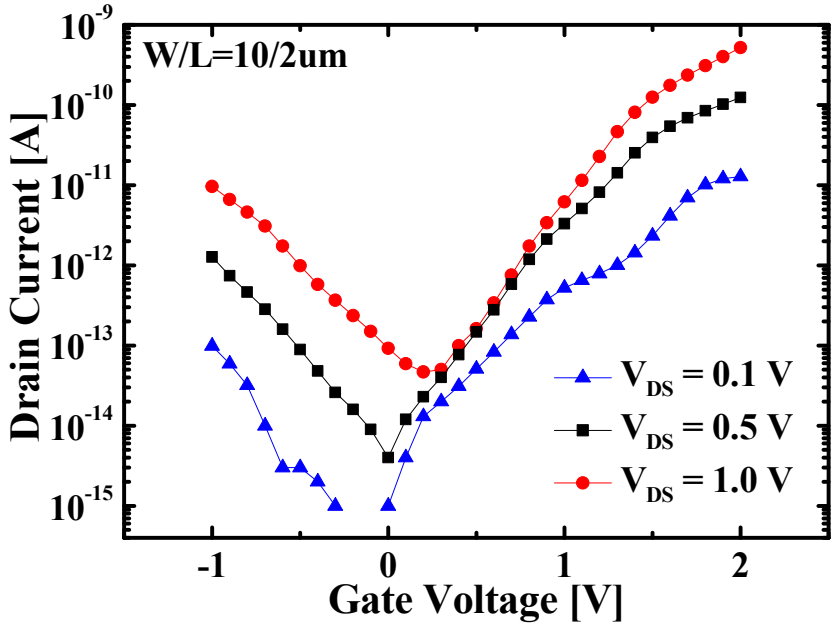
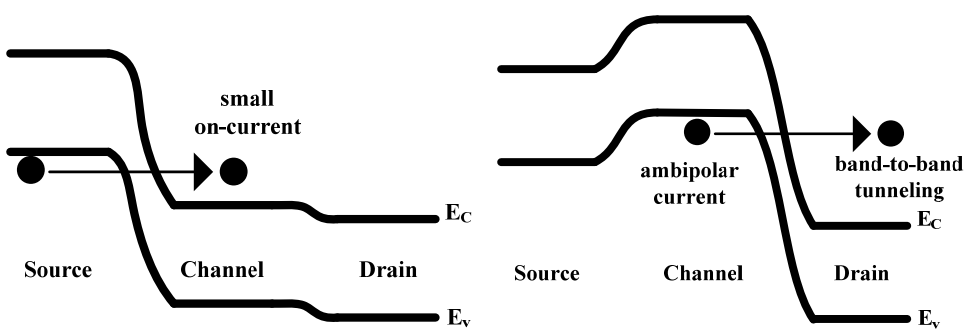


Fig. 1.6. Transfer characteritics with V_{DS} variation in fabricated silicon tunnel FET.



(a) ON state (b) OFF state

Fig. 1.7. (a) Small I_{ON} and (b) ambipolar behavior ($V_{GS} < 0$, $V_{DS} = V_{DD}$) energy band diagrams in n-type tunnel FET.

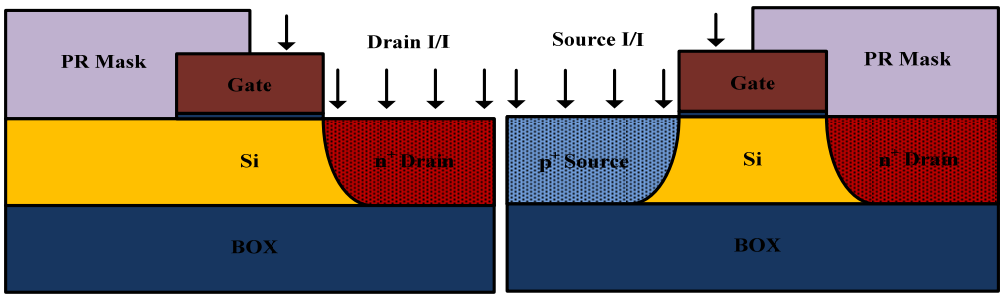


Fig. 1.8. Conventional tunnel FET process for making source and drain region.

large I_{ON} and smaller SS can be obtained than silicon tunnel FET. For making steep junction profiles, plasma doping and in situ doped epitaxial growth technologies are essential instead of implantation process [29-30]. Next, ambipolar behavior occurs when V_{GS} is negative in tunnel FET as shown in Fig. 1.7. As the conduction band of the channel region goes up, tunneling width between the channel and drain region get thinning leading to large tunneling current, namely ambipolar current (I_{AMB}). For better switching property, ambipolar behavior can be easily suppressed using fabrication skills such as low drain doping concentration and underlapped drain region [31-32]. Lastly, in tunnel FET fabrication, misalignment problem might happen during photolithography process as shown in Fig. 1.8. Because tunnel FET has asymmetric doping region unlike MOSFET, two photoresist masks must use to define source and drain. However, in case of the short-channel tunnel FET, photoresist mask is difficult to form on each of source and drain region during photolithography process resulting in misalignment problem. Thus, self-aligned doping process is needed to make short-channel tunnel FET [33].

1.4 Scope of Thesis

The main objective of this work is to propose and implement a novel SiGe tunnel FET. Especially, it is important to present improved electrical performances of the proposed tunnel FET that has high current drivability on both n-type and p-type tunnel FET operation. Before fabrication of the proposed tunnel FET, planar Si and SiGe tunnel FETs are firstly fabricated and investigated. Then, device simulation and fabrication of the proposed tunnel FET are conducted with planar Si and SiGe tunnel FETs. Finally, the proposed tunnel FETs are investigated with control groups.

In Chapter 2, planar Si and SiGe tunnel FETs are fabricated for confirming characteristics improved by narrow bandgap material. Then, electrical characteristics are analyzed in terms of n-channel and p-channel operation in tunnel FETs. In addition, temperature effects are investigated to understand current flow mechanism of tunnel FET through TCAD simulation. BTBT model parameters of Si and Ge are extracted by using TCAD simulation and measurement results. In Chapter 3, device simulations of the proposed tunnel FET are performed based on extracted BTBT model parameters. According to various process conditions, electrical performances are investigated in terms of DC characteristics. For logic applications, AC characteristics of the proposed tunnel FETs are examined by mixed-mode simulation. Chapter 4 will cover the fabrication flow and key process in details. Then, electrical characteristics of the fabricated devices are investigated. Compared with control groups, both n-type and p-type tunnel FETs are examined in terms of switching properties and ambipolar

behaviors. In chapter 5, the work will be concluded with summary and suggestions for future work.

Chapter 2

Planar Si and SiGe tunnel FETs

In this chapter, in order to investigate improved electrical characteristics of a SiGe tunnel FET, Si and SiGe tunnel FETs with planar structure are firstly fabricated and analyzed. For a SiGe tunnel FET fabrication, epitaxial growth test is performed for Si and SiGe materials. Also, MOSCAPs and MOSFETs which are made of SiGe materials are analyzed for gate dielectric estimation and current properties. After that, the fabricated devices are investigated and band-to-band tunneling parameters are extracted using Sentaurus Device TCAD simulator (version D-2012. 06).

2.1 Expitaxial growth for Si and SiGe layers

Figure 2.1 shows the epitaxial growth test structure (Si/SiGe/Si substrate = 60 Å/300 Å/Si substrate). The SiGe material which has Ge contents of 30 percent is set on bulk Si wafer because of critical thickness. A lattice constant of Si is 5.43 Å and Ge has 5.64 Å. Thus, when SiGe layer which has high Ge contents grow up on Si wafer, lattice

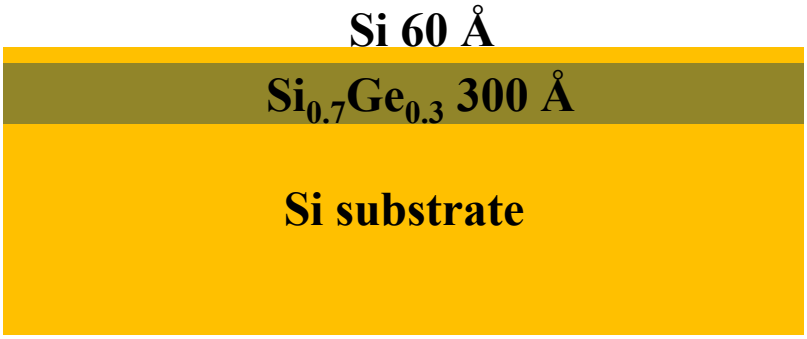


Fig. 2.1. SiGe epitaxial growth test structure (Si/SiGe/Substrate = 60 Å/300 Å/Substrate).

mismatch can occur between Si and SiGe resulting in threading dislocations (TDs) [34-36]. These TDs induce many defects and degrade switching property of tunnel FET because recombination components increase by traps. Therefore, 30 percent of Ge content in SiGe is set for minimizing TDs. For SiGe layer, epitaxial growth process is performed using Metal Organic Chemical Vapor Deposition (MOCVD). Process condition is that a gas mixture of H_2 at 20 sccm, SiH_4 at 20 sccm, and GeH_4 at 90 sccm is used at 670 °C during 61 second for SiGe epitaxial growth of 300 Å. For Si layer of 60 Å, a gas mixture of H_2 at 20 sccm and SiH_4 at 50 sccm is used at 720 °C during 18 second. Process pressure is progressed at 30 Torr. After epitaxial growth process, quality of layers is investigated by using transmission electron microscopy (TEM) and auger electron spectroscopy (AES). First of all, thickness of epitaxial growth layers is observed using TEM as shown in Fig. 2.2. Boundary between materials can distinguish by lattice constant mismatch between Si and SiGe. Also, epitaxial growth layers are

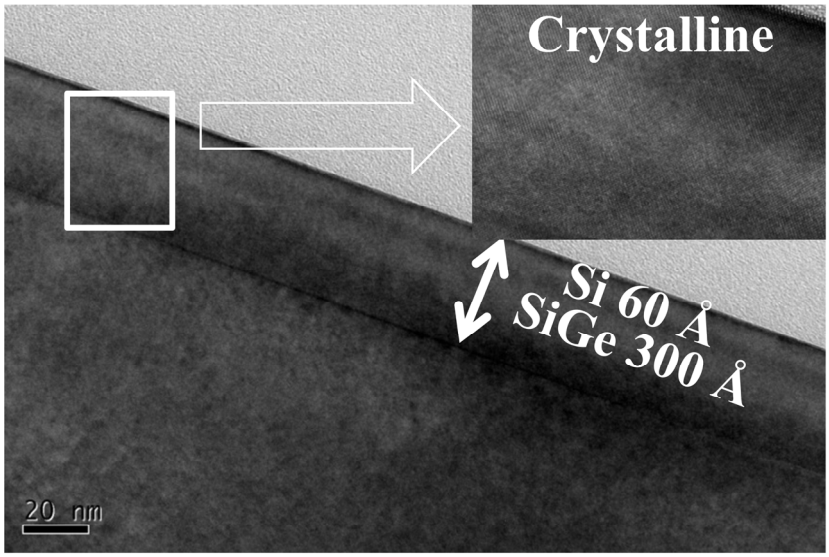


Fig. 2.2. TEM image of Si and SiGe layer for confirming crytalline structure.

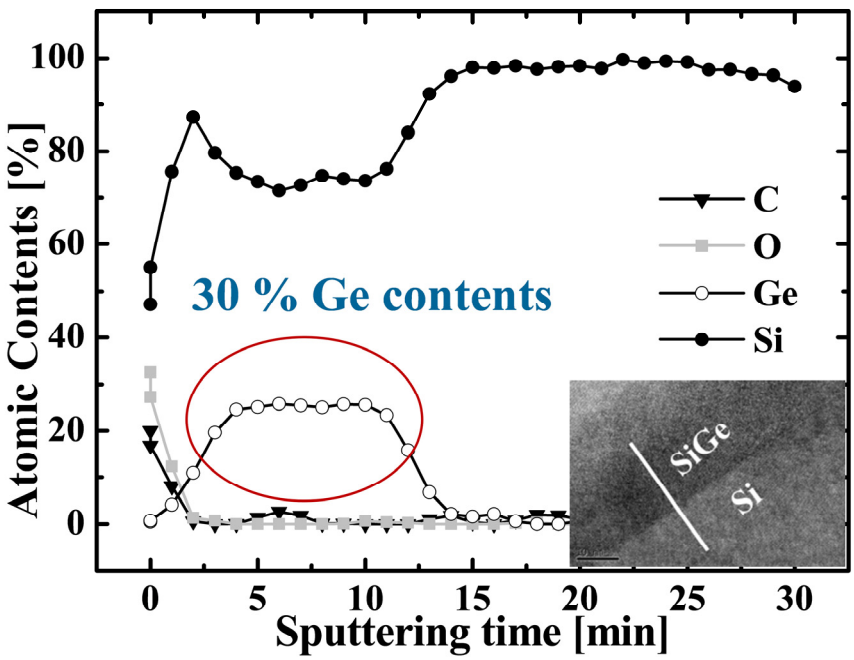


Fig. 2.3. Atomic contents of each element in the depth direction from surface using AES.

confirmed as crystalline states through high resolution TEM (HR-TEM). Then, atomic contents of each element in the depth direction from surface are analyzed using AES. Analysis condition is that beam uses 10 kV/10 nA and sputtering depth is 3.3 nm per 1 step at SiO_2. From AES data of Fig. 2.3, Ge content shows about 30 percent as expected.

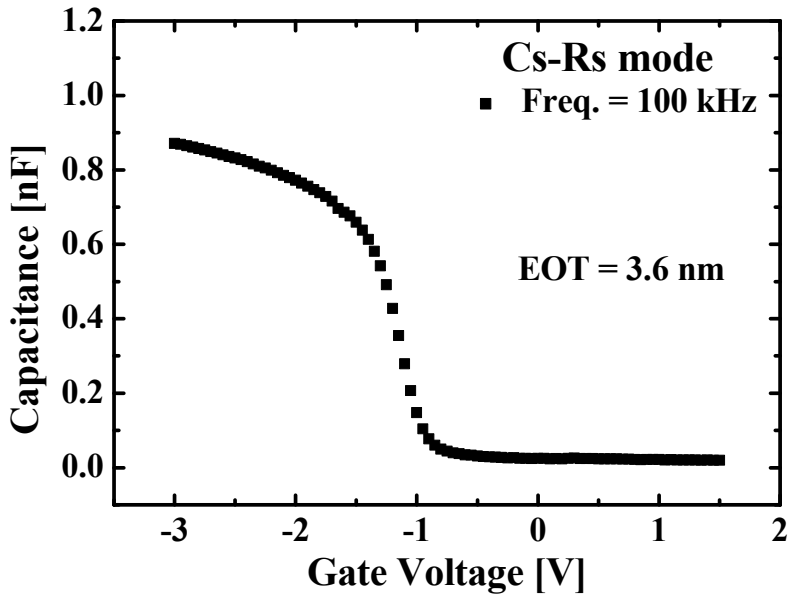
2.2 SiGe MOSCAP and MOSFET fabrication

After SiGe epitaxial growth test, analysis on interface properties between gate stacks and SiGe surface is needed to fabricate SiGe tunnel FET. Thus, MOS capacitors (MOSCAPs) with Si and SiGe channels are fabricated to obtain equivalent oxide thickness (EOT). In case of SiGe MOSCAP, SiGe layer with 30 nm thickness and 30 % Ge content is grown on p-type Si substrate. Also, Si capping of 1 nm is added to reduce defects induced between SiGe and gate dielectric. Then, thermal oxidation process is performed at 800 °C during 30 second. SiO_2 of 3.3 nm is formed from ellipsometer measurement and aluminum gate of 200 nm is used. For EOT extraction, capacitance-voltage (*C-V*) measurement is performed using HP 4284 LCR meter at frequency of 100 kHz. Capacitor area is 300 μm× 300 μm and C_S-R_S mode is selected. Figure 2.4 shows the *C-V* characteristics of Si and SiGe MOSCAP. From measurement results, SiGe MOSCAP shows the flatband voltage (V_{FB}) of -1.3 V because of aluminum gate which has workfunction of 4.1 eV. From *C-V* data, EOT can be extracted as 3.6 nm and 3.4 nm for Si and SiGe MOSCAP, respectively (EOT = ε_{ox}/T_{ox}). This result is approximately

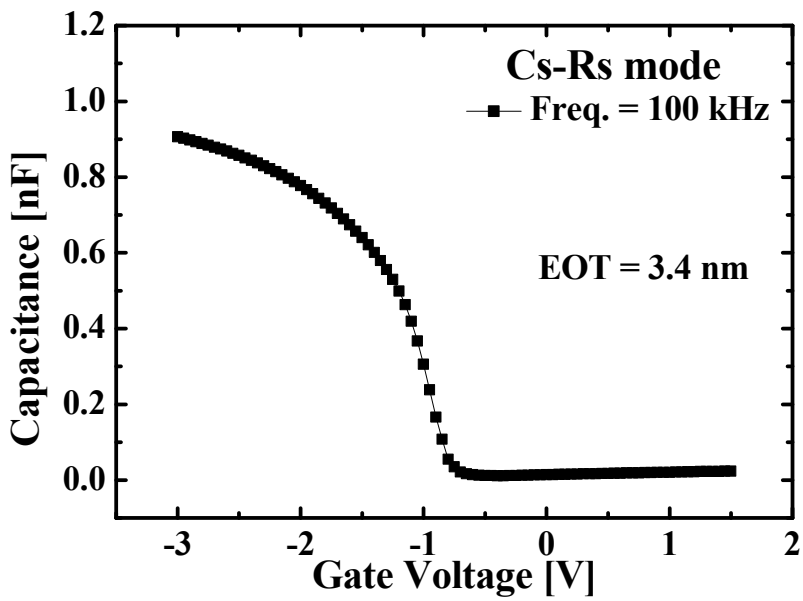
equal to ellipsometer measurement. Trap density extraction from *C-V* data isn't conducted because mobility degradation has not an influence on tunnel FET's property by large tunneling resistance. For confirming tunneling enhancement in device with SiGe material, MOSFET is simultaneously fabricated with MOSCAP. MOSFET has gate stacks with 150 nm n-doped poly-Si gate and 3.4 nm SiO_2 on 1 nm Si capping/30 nm SiGe/p-type Si substrate. Also, Si MOSFET as a control group is fabricated with same process condition. Figure 2.5 shows the transfer characteristics of fabricated MOSFETs with gate length and width of 0.55 μm and 20 μm. Compared to Si MOSFET, SS characteristics are nearly degraded in SiGe MOSFET. In terms of I_{ON} of devices, SiGe MOSFET has lower I_{ON} level than Si MOSFET because n-type dopants such as phosphorus and arsenic have low solubility in SiGe material [37]. In case of gate-induced drain current (GIDL) based on BTBT mechanism, SiGe MOSFET has larger than Si MOSFET due to small bandgap. From this result, high current drivability of SiGe tunnel FET can be expected than Si tunnel FET.

2.3 Planar Si and SiGe tunnel FET

Based on results in MOSCAP and MOSFET's characteristics, planar Si and SiGe tunnel FETs are fabricated for understanding of tunnel FET. The studied SiGe tunnel FET is fabricated on a (100) p-type SOI wafer with 60 nm thick Si on top of 375 nm buried oxide. Using Epsilon 2000, SiGe epitaxial growth process which has Ge content

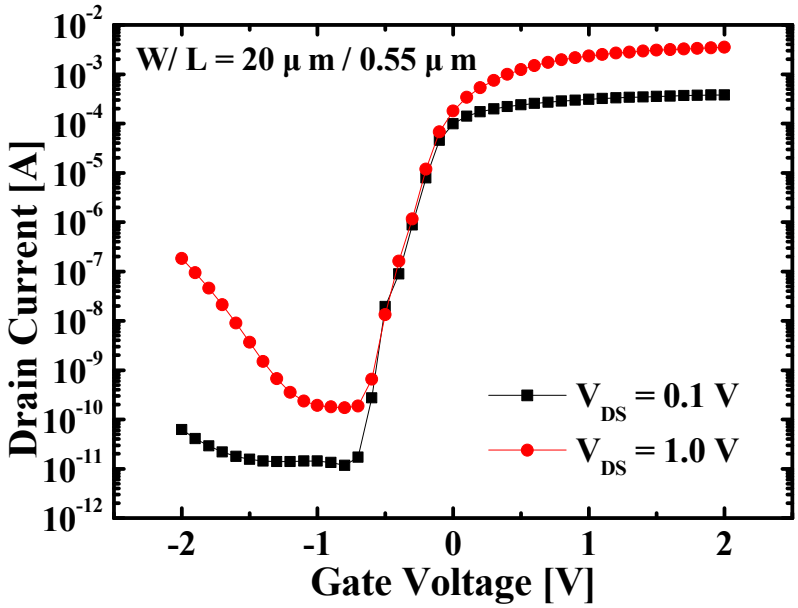


(a)

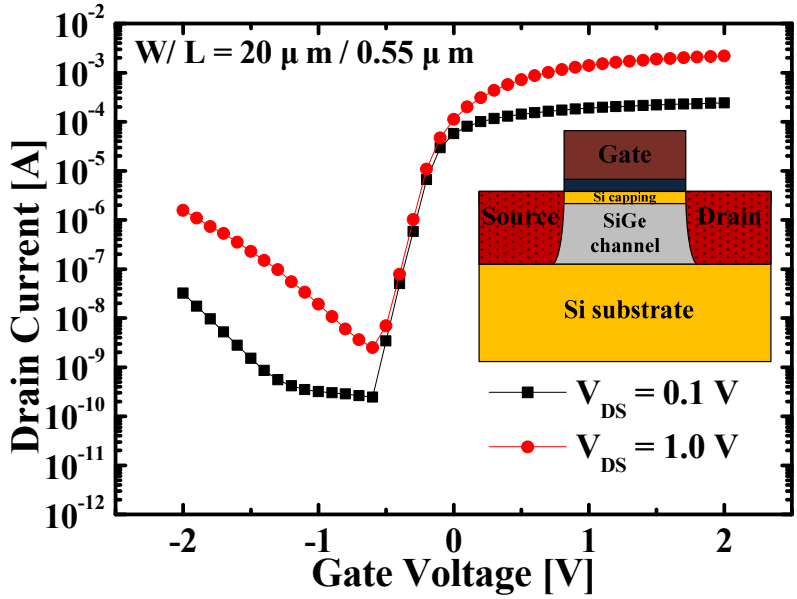


(b)

Fig. 2.4. *C-V* characteristics of (a) Si and (b) SiGe MOSCAP using Agilent 4284.

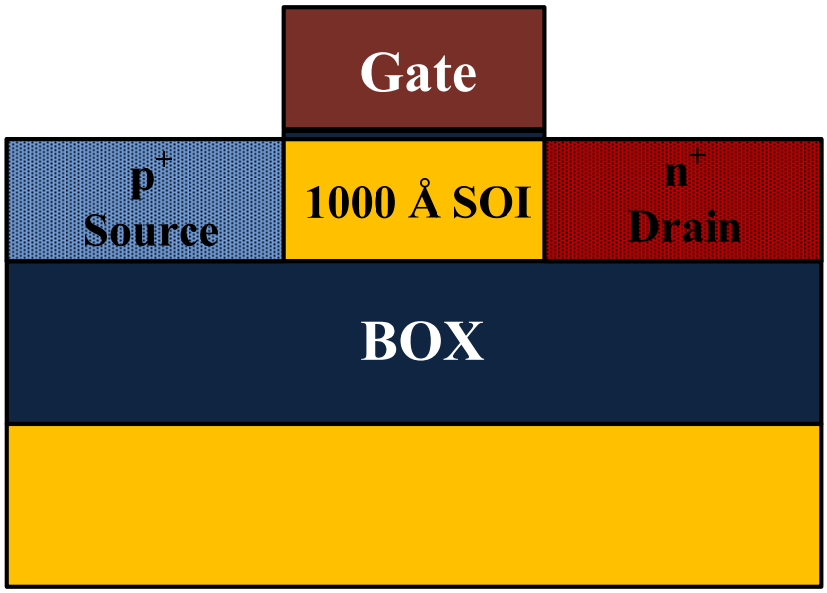


(a)

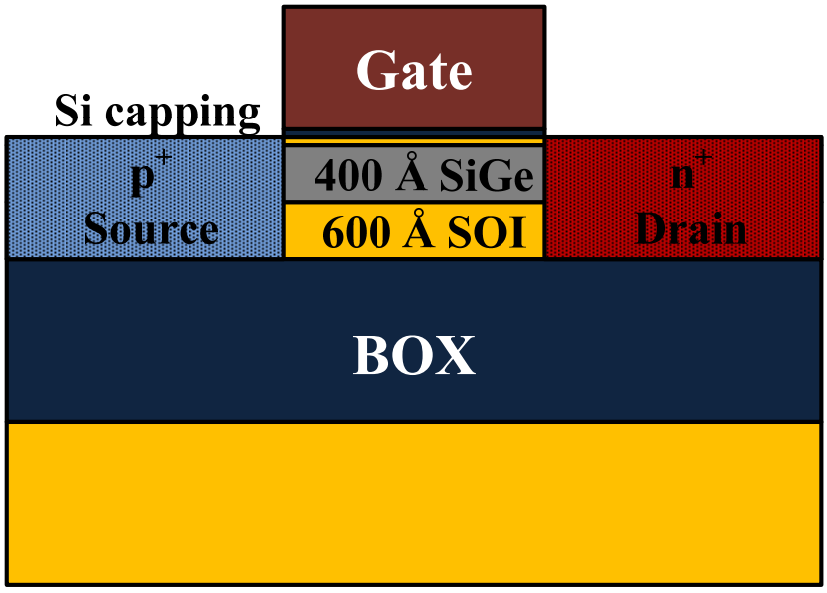


(b)

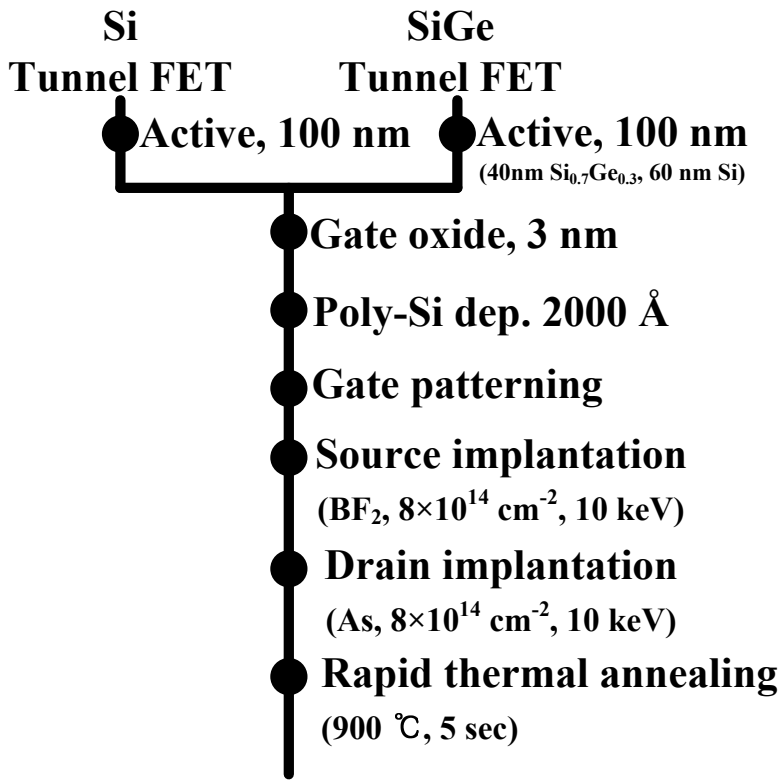
Fig. 2.5. Transfer characteristics of (a) Si and (b) SiGe MOSFET with gate length and width of 0.55 μm and 20 μm.



(a) Si tunnel FET



(b) SiGe tunnel FET

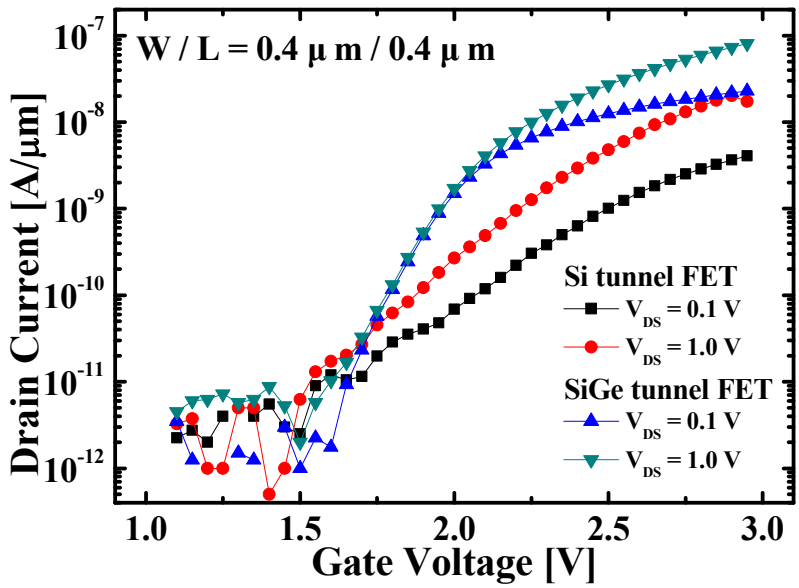


(c) Process flow of fabricated tunnel FET

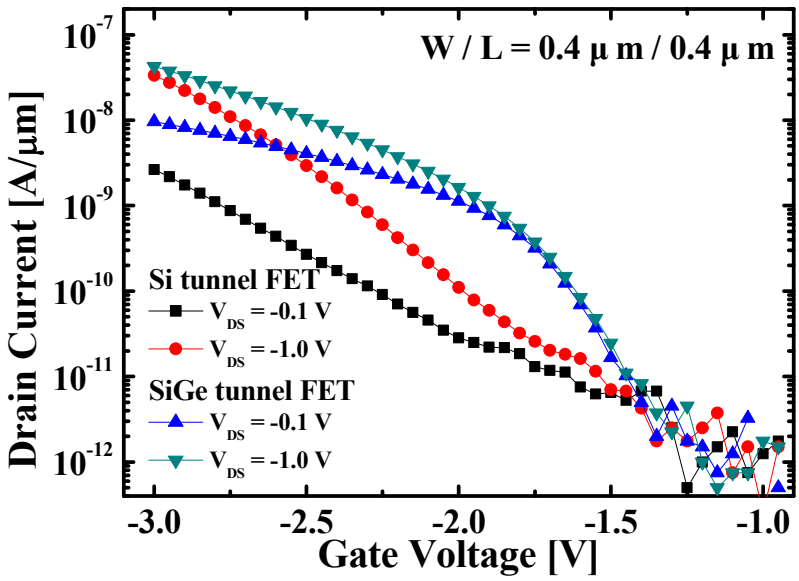
Fig. 2.6. Cross-sectional views of (a) Si tunnel FET and (b) SiGe tunnel FET, (c) process sequence in this work .

of 30 percent and thickness of 40 nm is performed on SOI wafer. Then, in order to reduce defects at interface between gate stack and SiGe channel, Si capping layer is grown on SiGe channel. The gate stack consists of 200 nm poly-Si layer and 3 nm SiO_2. After gate patterning, source and drain region are defined through photolithography and implantation process. BF_2 with dose of 8×10^{14} cm^{-2}, 7° tilt, and an energy of 10 keV is used for source implantation. Drain implantation is also performed using As with the

same condition. Finally, dopant activation is implemented by rapid thermal process (RTP) with 900 °C and 5 sec. For comparison, Si tunnel FET as a control group is fabricated on SOI wafer of a 100 nm. The rest of fabrication process is the same. The scheme of tunnel FETs and process condition in this work are shown in Fig. 2.6. Transfer characteristics of fabricated Si and SiGe tunnel FETs are investigated as shown in Fig. 2.7. Measured devices have gate length and width of 0.4 μm. Both n-type and p-type SiGe tunnel FETs have better switching characteristics than Si tunnel FETs. This can be attributed to the smaller bandgap of the SiGe material leading to improving performance. In n-type tunnel FET, SS of 69.1 mV/dec in SiGe tunnel FET is observed while Si tunnel FET shows SS of 157 mV/dec. Also, SS and on-current of p-type tunnel FET are improved by using SiGe channel. This shows that SiGe tunnel FETs have an advantage in terms of implementing tunnel FET circuits because it has compatibility with conventional Si process. Also, it doesn't need to change each n-type and p-type tunnel FET structure unlike heterojunction and III-V compound tunnel FETs. From Fig. 2.7, it is observed that both n-type and p-type tunnel FET have large V_{TH}. It is because a half of gate region is implanted by photoresist mask when source implantation is performed. Hence, the n-type devices have p^+ workfunction gate (5.1 eV) and p-type devices have n^+ workfunction gate (4.17 eV). Figure 2.8 shows the output characteristics of Si and SiGe tunnel FETs. Both SiGe tunnel FETs have a stronger current drivability than Si tunnel FETs. Drive current of n-type SiGe tunnel FET is increased more than 10 times for Si device. In low drain voltage (V_{DS}) region, Si tunnel

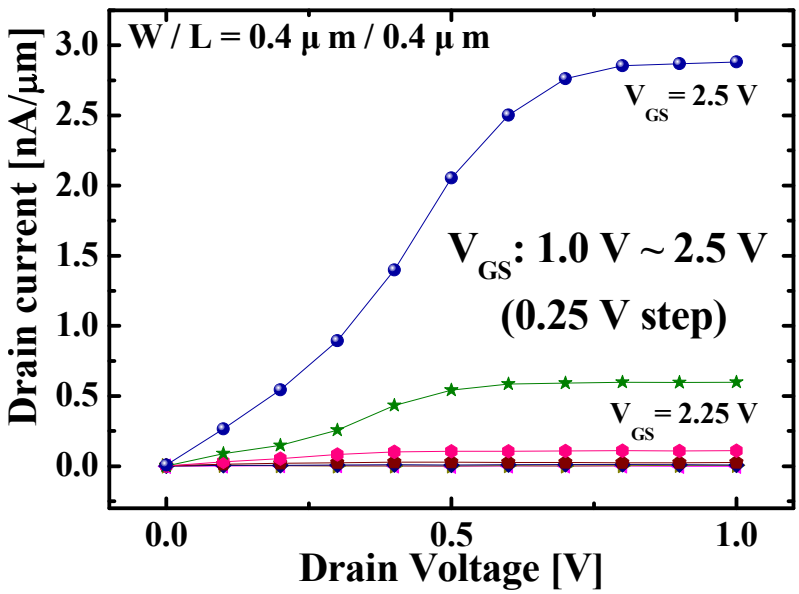


(a) n-type Si and SiGe tunnel FETs

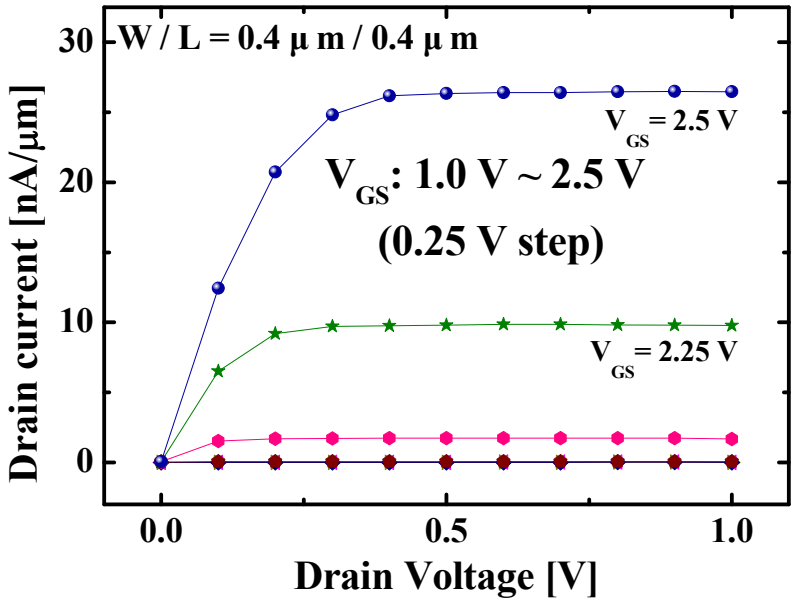


(b) p-type Si and SiGe tunnel FETs

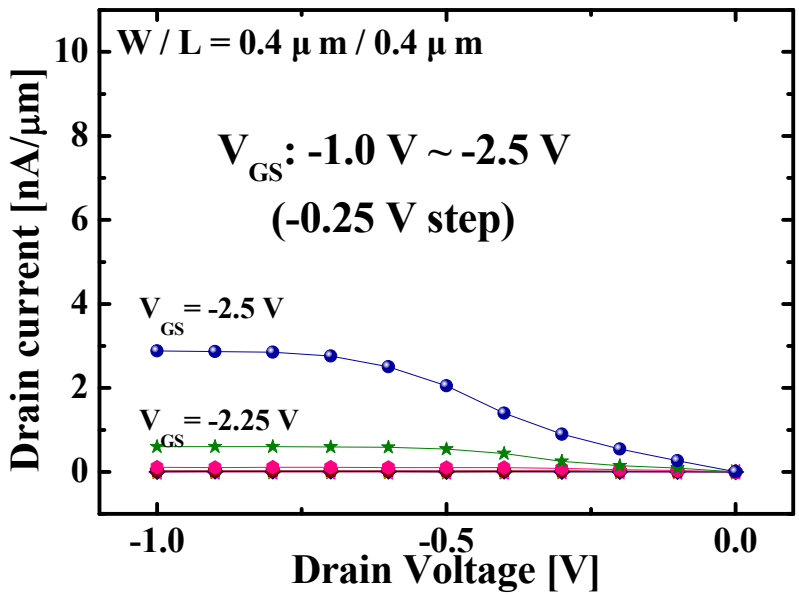
Fig. 2.7. Transfer characteristics of fabricated devices for (a) n-type and (b) p-type Si and SiGe tunnel FETs.



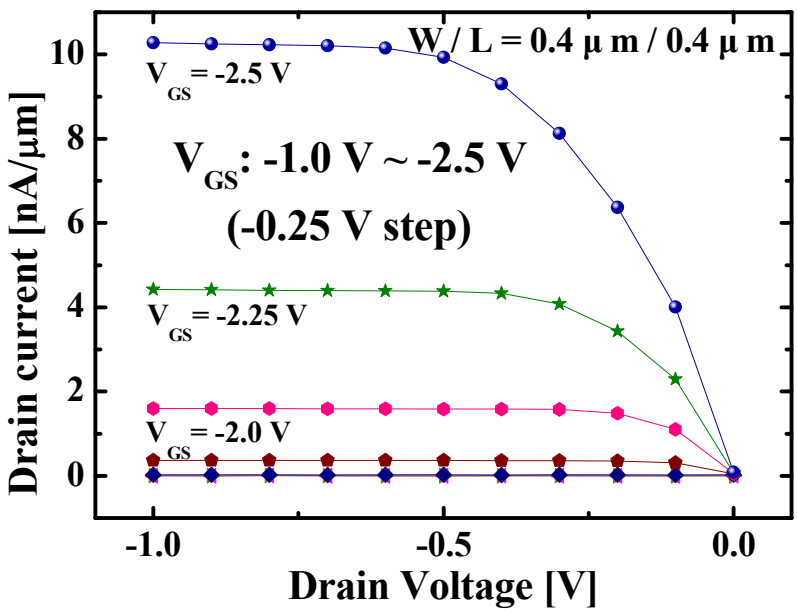
(a) n-type Si tunnel FET



(b) n-type SiGe tunnel FET



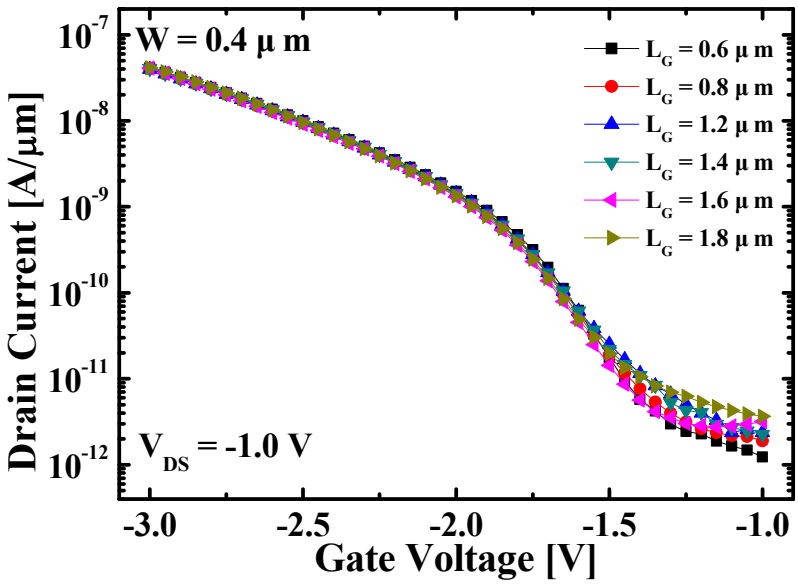
(c) p-type Si tunnel FET



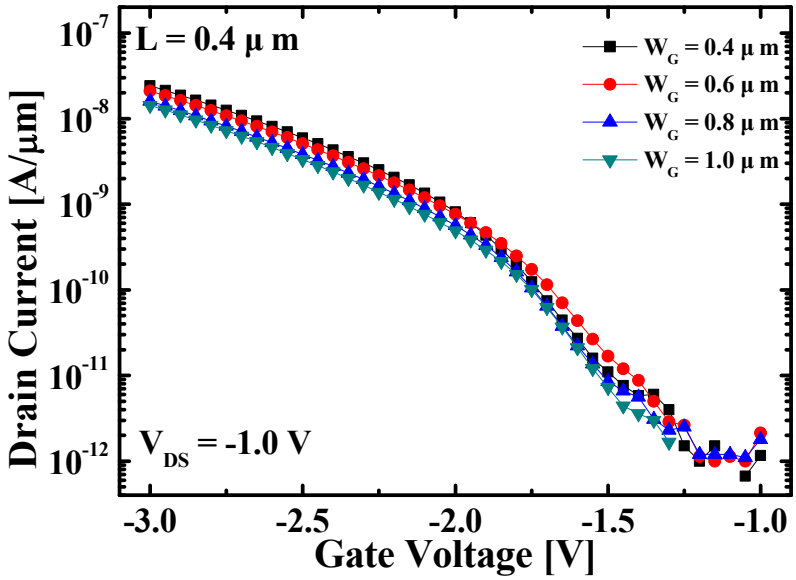
(d) p-type SiGe tunnel FET

Fig. 2.8. Output characteristics of (a) n-type Si, (b) SiGe tunnel FETs, (c) p-type Si, and (d) SiGe tunnel FETs, respectively.

FET shows weak current drivability due to large tunneling resistance. On the other hand current saturations of n-type and p-type SiGe tunnel FET become faster than that of Si tunnel FETs. In addition, the properties on gate length and width dependency of tunnel FET are investigated as shown in Fig. 2.9(a). In case of CMOS devices, as gate length is decreased, channel resistance is reduced resulting in boosting I_{ON} which is proportional to 1 of channel length. However, for tunnel FET, gate length variation can't have an influence on I_{ON} since its currents are determined by a region of a few nanometers around the source-channel tunneling junction at the edge of the gate as shown in Fig. 2.9(a). Thus, I_{ON} of tunnel FET is independent of gate length. In case of I_{OFF} of tunnel FET, it becomes larger as gate length increases. The reason is that SRH generation components in channel region increase. Then, gate width dependency is investigated as shown in Fig. 2.9(b). As gate width decreases, it is observed that current properties aren't almost changed because measured devices have large gate width (> 0.4 μm). In order to analyze these current flow mechanisms, the electrical characteristics of SiGe tunnel FET are measured with temperature variation. Current characteristics of tunnel FET have two components: SRH, and BTBT [38-40]. I_{OFF} in tunnel FET is dominated by SRH generation and BTBT between channel and drain. I_{ON} is determined by BTBT at source-channel tunneling junction. Figure 2.10(a) shows the transfer characteristics of n-type Si and SiGe tunnel FET with 0.4 μm gate length and width measured at V_{DS} of 0.1 V in temperature range from 298 K to 373 K. SS and I_{OFF} become larger as temperature increases. In current saturation region, current variation is hardly shown.

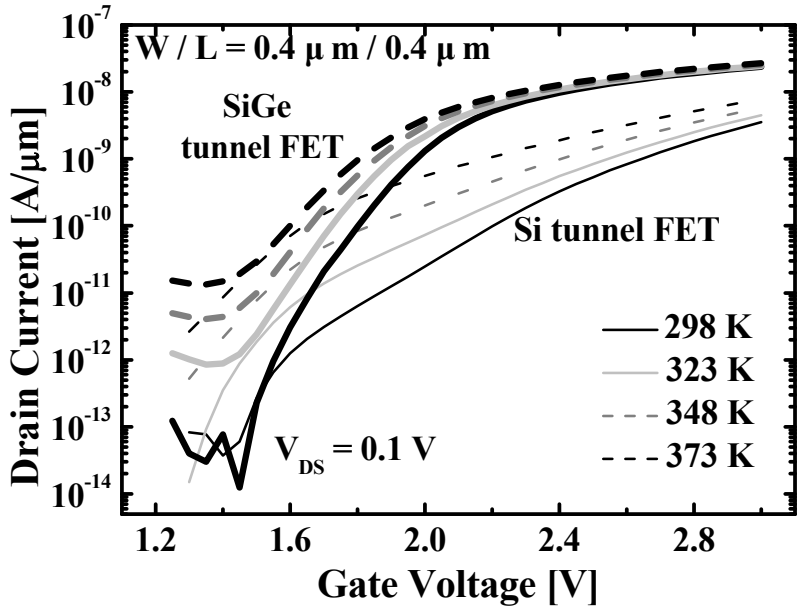


(a) Gate length dependency

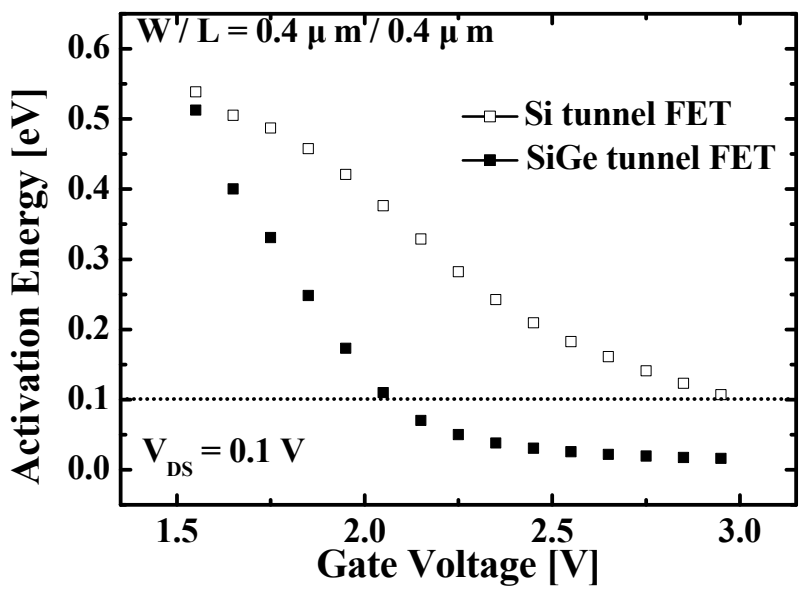


(b) Gate width dependency

Fig. 2.9. Transfer characteristics of fabricated devices for (a) gate length and (b) width dependency in p-type SiGe tunnel FETs.



(a)



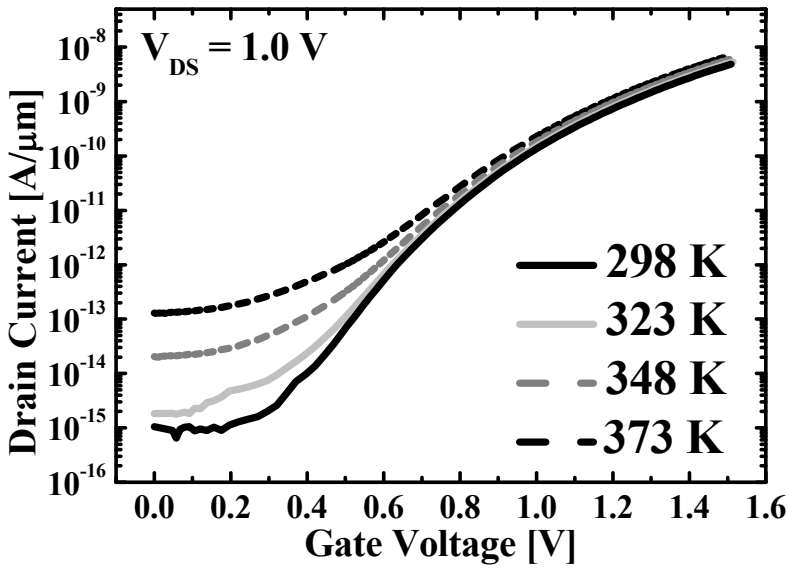
(b)

Fig. 2.10. (a) Transfer characteritics in temperautre range from 298 K to 373 K and (b) extracted activation energy according to each V_{GS} in Si and SiGe tunnel FETs.

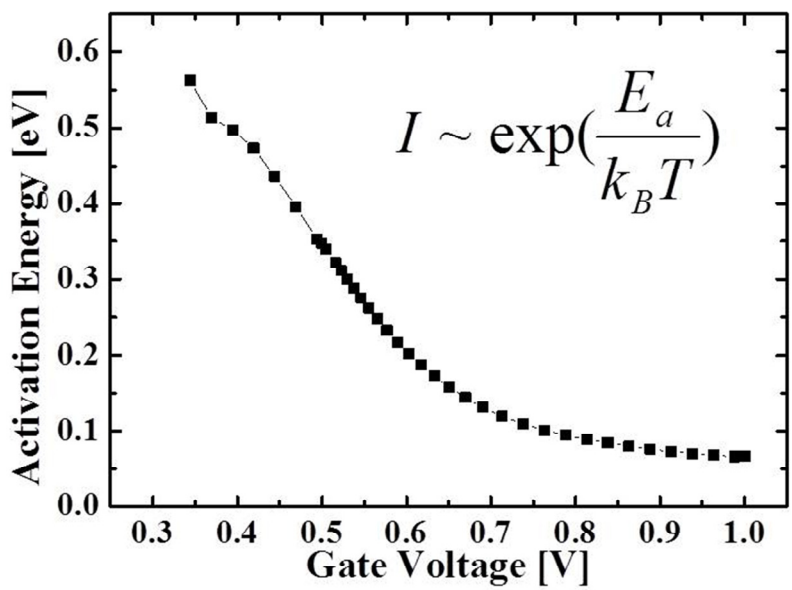
Also activation energy (E_a) for each V_{GS} can be extracted through Arrhenius plot as

$$I \sim \exp\left(\frac{E_a}{k_B T}\right)$$

shown in Fig. 2.10(b) [41]. V_{DS} is fixed at -0.1 V because effects of other current flow mechanisms by high V_{DS} can be excluded. In Si tunnel FET, extracted E_a shows bigger value than that of SiGe device due to large bandgap. In SiGe tunnel FET, it is observed that current rarely changes in V_{GS} region with E_a below 0.1 eV (V_{GS}> 2.0 V). In order to analyze these phenomena, TCAD simulations are performed according to temperature variation. Simulated Si device with same structure condition is used. Field- and temperature-dependent SRH model and nonlocal BTBT models are applied. Figure 2.11 shows the transfer characteristics and E_a extracted by temperature changes. As temperature increases, it is shown that SS degrades and SRH generation increases like measurement results. In saturation region, current level is nearly changed. Also, it is observed that E_a extracted by simulation results is similar to measured E_a. For confirming current components with increasing V_{GS}, transfer characteristics are plotted using SRH or BTBT model. Figure 2.12(a) shows SRH generation current in Si tunnel FET. For increasing temperature, SRH currents in all V_{GS} regions are generally increased due to thermal generation. In low V_{GS} region, SRH current is sustained as V_{GS} increases. And then, in high V_{GS} region, SRH current is gradually increased. Furthermore, the rates of increase in SRH current become larger for high temperature. Figure 2.12(b) shows BTBT current in Si tunnel FET. Since BTBT components have

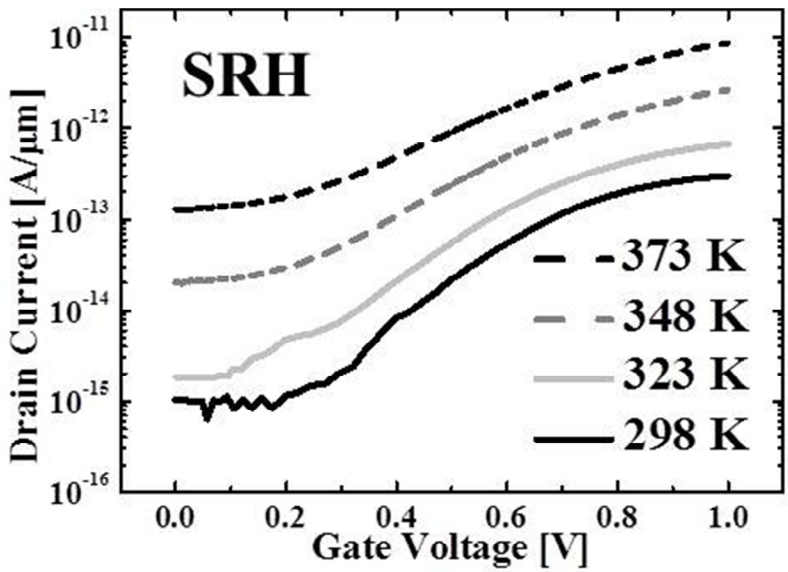


(a)

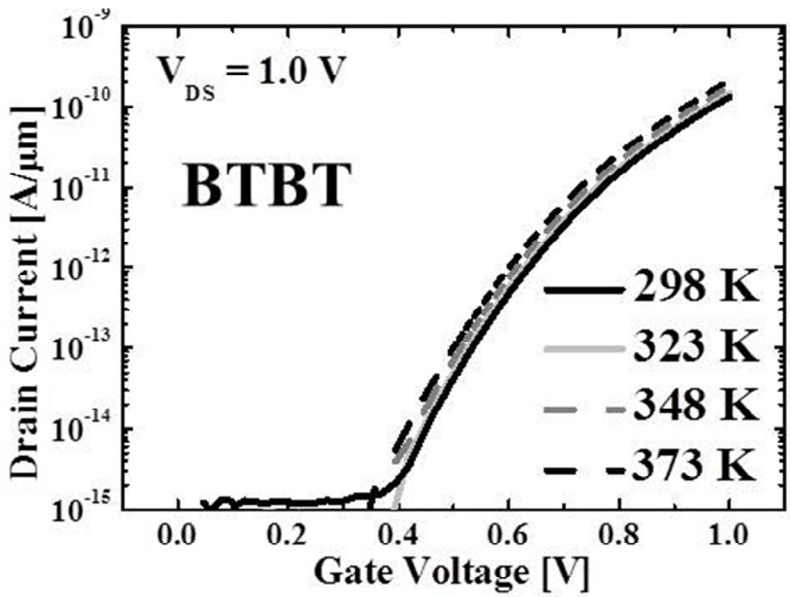


(b)

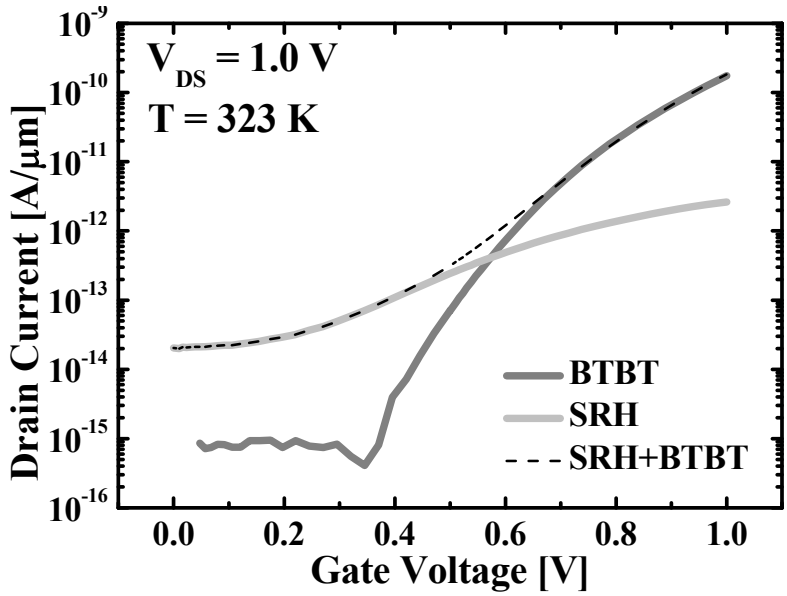
Fig. 2.11. (a) Transfer characteritics in temperautre range from 298 K to 373 K and (b) extracted activation energy according to each V_{GS} in Si tunnel FETs using TCAD simulation.


SRH
Drain Current [A/μm]
Gate Voltage [V]
373 K
348 K
323 K
298 K

(a)


V_DS = 1.0 V
BTBT
Drain Current [A/μm]
Gate Voltage [V]
298 K
323 K
348 K
373 K

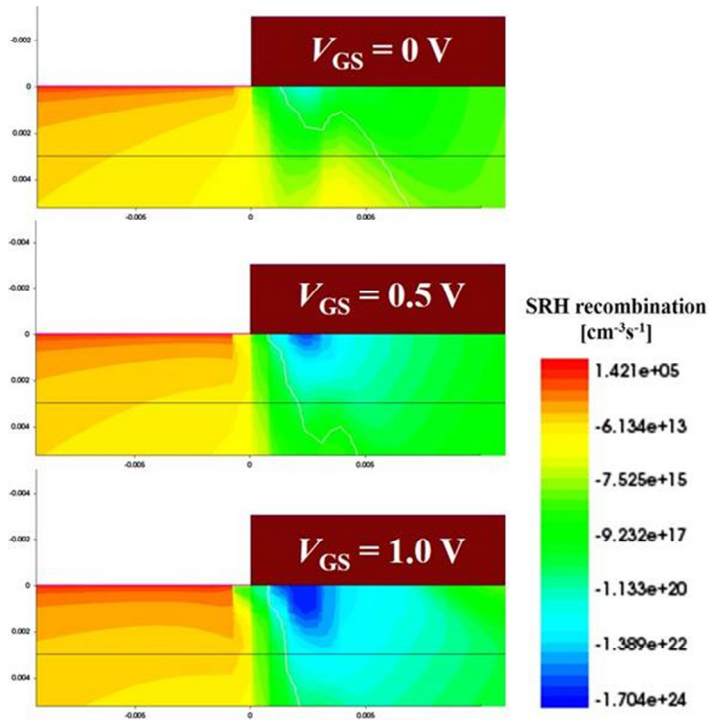
(b)



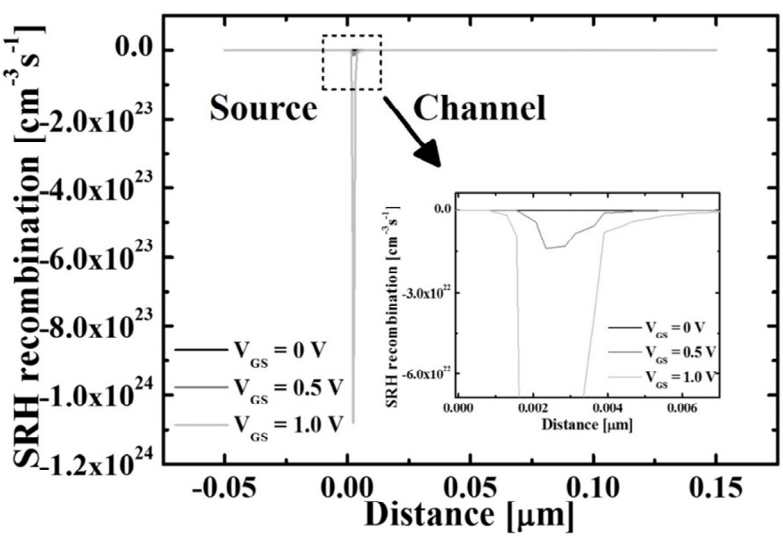
(c)

Fig. 2.12. (a) SRH generation, (b) BTBT current, and (c) total current of Si tunnel FET with temperature variation.

low sensitivity to temperature variation, BTBT currents slightly increases because bandgap is decreased by increase of temperature. Figure 2.12(c) shows transfer characteristics of Si tunnel FET using SRH and BTBT models. As a result, from simulation results, it is founded that degraded switching property comes from increased SRH generation as temperature increases. In order to origin of field-dependent SRH components, SRH generation contours and rates are investigated as shown in Fig. 2.13. SRH generation contours are plotted at V_{GS} of 0, 0.5, and 1.0 V. From Fig. 2.13(a), it is observed that SRH generation almost occurs in source-channel junctions and it continues to increase with V_{GS}. It is because depletion region becomes wider with



(a)



(b)

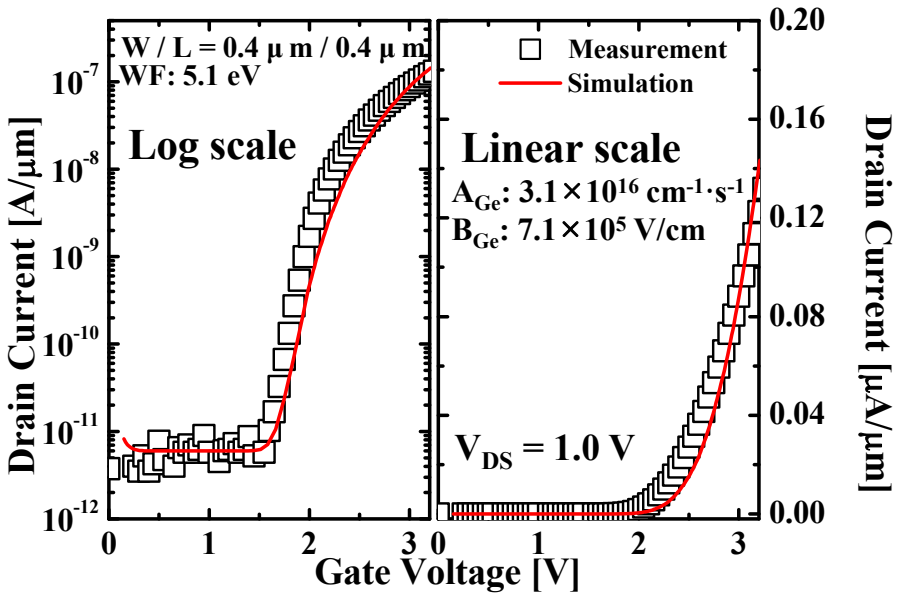
Fig. 2.13. (a) SRH generation contours and (b) rates in source-channel junctions as increasing V_{GS}.

increasing V_{GS}. These results shows that SRH generation has to be reduced while increasing BTBT is very essential for better switching characteristics.

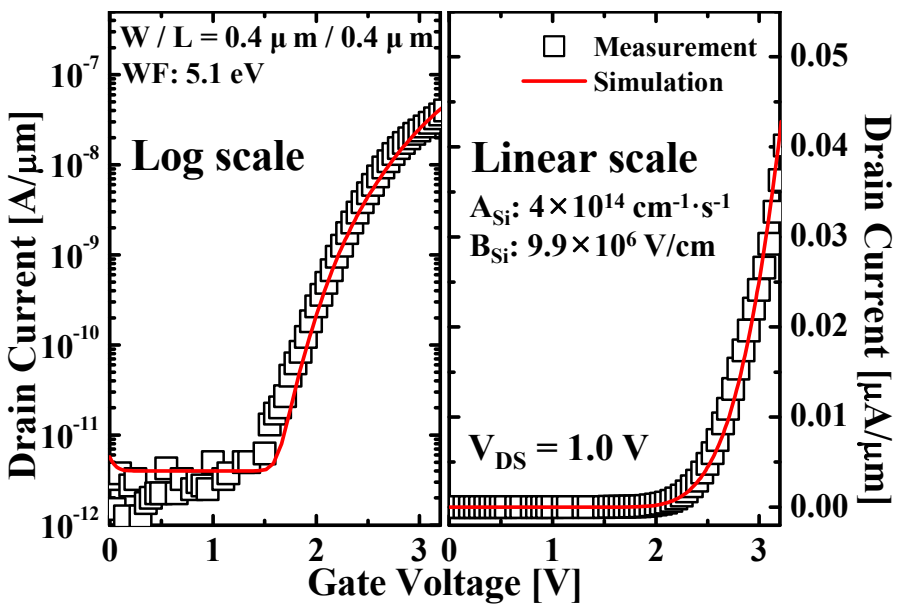
Last, BTBT parameters of Si and Ge in fabricated devices are extracted through TCAD simulation. Thus, Sentaurus tool (version D-2012.06) of Synopsys and non-local BTBT model are used [42]. Also bandgap narrowing model is applied since source and drain region are heavily doped. This tool is especially suitable for accurate tunneling current calculation because it automatically defines the tunneling path and the mesh on the basis of the valence band gradient. Also, it completely gets rid of uncertainty of the current calculations due to the inappropriate assumption of the tunneling direction. BTBT generation rates G per unit volume in this model are defined by

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right)$$

in the uniform electric field limit where F_0 = 1 V/m, P = 2.5 for indirect BTBT. A of prefactor and B of exponential factor are the Kane parameters and F is the electric field. For current fitting, simulation is performed based on experimental results of the fabricated tunnel FET. Figure 2.14 show the calibration of transfer characteristics at V_{DS} of 1.0 V in n-type Si and SiGe tunnel FETs. Both linear and log scale in the transfer characteristics are well matched using simulation and measurement results. From Fig. 2.14(a), extracted A and B parameters of BTBT model in Si are 4×10^{14} $cm^{-1}\cdot s^{-1}$ and



(a)



(b)

Fig. 2.14. Calibrated trasfer characteristics from simulation and measurement results for (a) Si and (b) SiGe tunnel FETs.

9.9×10^{6} V/cm. Also, from SiGe tunnel FET's transfer characteristics, A and B parameters of Ge can be extracted as 3.1×10^{16} $cm^{-1}\cdot s^{-1}$ and 7.1×10^{5} V/cm, respectively (Fig. 2.14(b)).

2.4 Summary

In this work, planar SiGe tunnel FETs are fabricated and analyzed before implementing the proposed tunnel FET. In SiGe tunnel FET, transfer and output characteristics are improved compared with Si tunnel FET due to narrow bandgap. Also, both n-type and p-type SiGe tunnel FET shows better properties without structure changes. This means that SiGe tunnel FET have strong advantage in terms of implementing tunnel FET circuits. For understanding of current flow mechanisms in tunnel FET, transfer characteristics are measured as temperature increases. In region of SRH generation, SS and off-current properties become worse. However, BTBT current which has low temperature sensitivity rarely changes. By using Arrhenius plot, E_a of each gate voltage in Si and SiGe tunnel FET is extracted. Also, A and B parameters of nonlocal BTBT model are extracted through simulation and measurement results.

Chapter 3

Device Simulation

In this chapter, in order to overcome disadvantages of conventional tunnel FETs, a novel tunnel FET structure is proposed [43, 44]. The proposed tunnel FET has strong current drivability and small I_{AMB} because of SiGe body and elevated Si drain region. For confirming improved electrical performances, the proposed tunnel FET is investigated by using TCAD simulation before fabrication process. For accurate calculation of tunneling current, nonlocal BTBT and bandgap narrowing models are applied using extracted model parameters.

3.1 Proposed tunnel FET

On the basis of discussions so far, the novel SiGe tunnel FET which has fin-channel

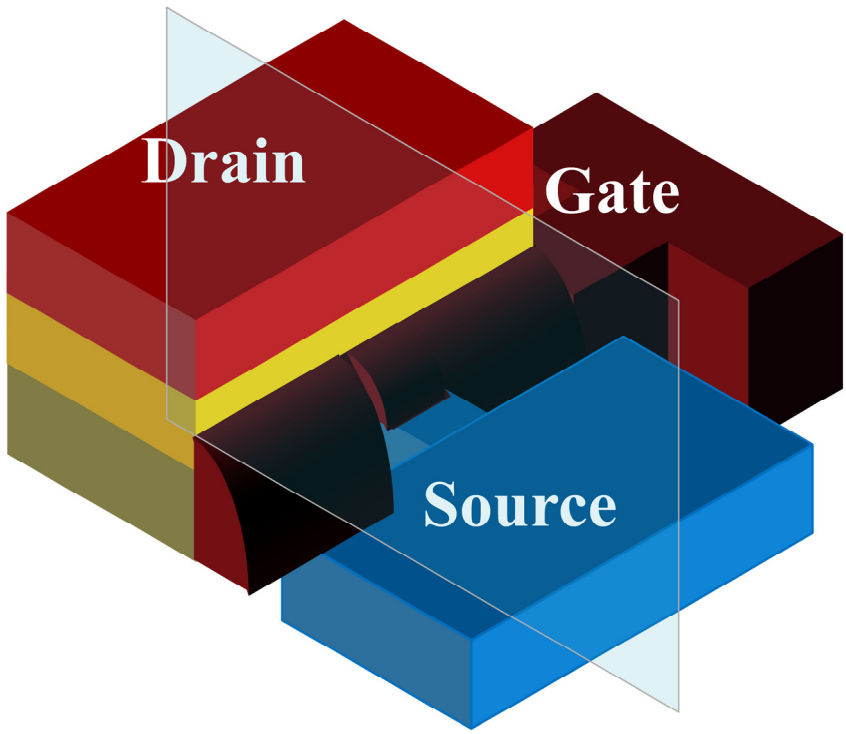


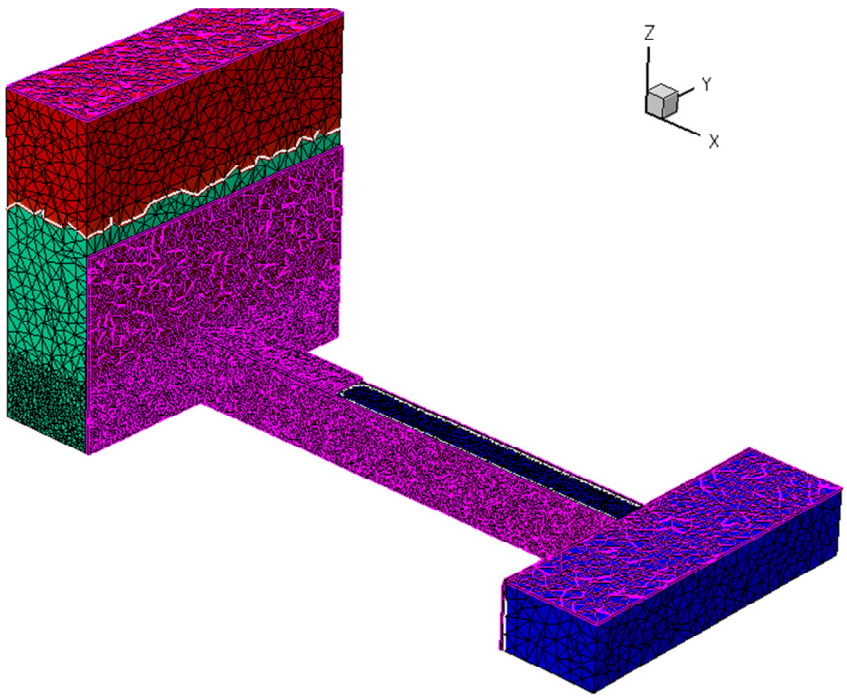
Fig. 3.1. Scheme of the proposed tunnel FET with SiGe source & channel and elevated Si drain regions.

and elevated Si drain region is proposed to improve switching characteristics as shown in Fig. 3.1. In order to obtain high current drivability in tunnel FET, SiGe material is applied to the source and channel regions. Also, fin-channel structure is used for better gate controllability. For reducing ambipolar behavior, the proposed device uses the elevated Si drain region. Thus, I_{AMB} can be suppressed through gate-drain underlap and Si bandgap. In terms of fabrication process, the proposed device is made by using spacer technique. Thus, it is possible to progress self-aligned doping process and short-

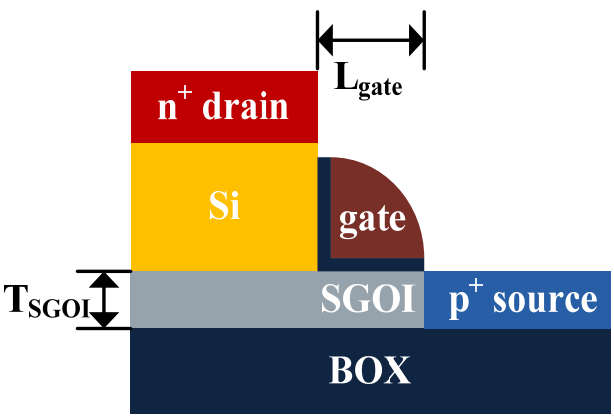
channel device implementation. Among the several advantages of the proposed tunnel FET, the biggest merit is that the proposed device can simultaneously implement n-type and p-type tunnel FET without structural changes. In tunnel FET researches, n-type and p-type channel tunnel FETs have been optimized separately with different materials system [45]. However, theses advanced tunnel FETs can cause the process complexity and increase of expense when ICs based on tunnel FETs are fabricated.

3.2 Simulation parameters and results

Sentaurus TCAD simulations are performed to verify the proposed tunnel FET. For accurate calculation of tunneling current, nonlocal BTBT model is applied using parameters extracted by planar SiGe tunnel FET's results. Also, since the source and drain region have heavy doping concentration, the bandgap narrowing model is used. The gate leakage current is ignored. In this simulation work, the gate length is fixed at 50 nm and the gate workfunction for n-type tunnel FET is set to be 4.17 eV as shown in Fig. 3.2. The EOT is 1 nm for gate dielectric layer. The doping concentration of source, channel and drain regions are 2×10^{20}, 1×10^{15}, and 1×10^{20} cm^{-3}, respectively. The dopant types of the source and channel region are boron while the drain dopant type is arsenic. The SiGe fin-channel consists of 10 nm F_{width} and 20 nm F_{height}. A turn-on voltage ($V_{turn-on}$) is defined as the V_{GS} when I_{ON} is equal to 10^{-10} A/μm. The average SS (SS_{avg}) is defined as the inverse of the slope between the zero-gate-bias point and the $V_{turn-on}$ point



(a)



(b)

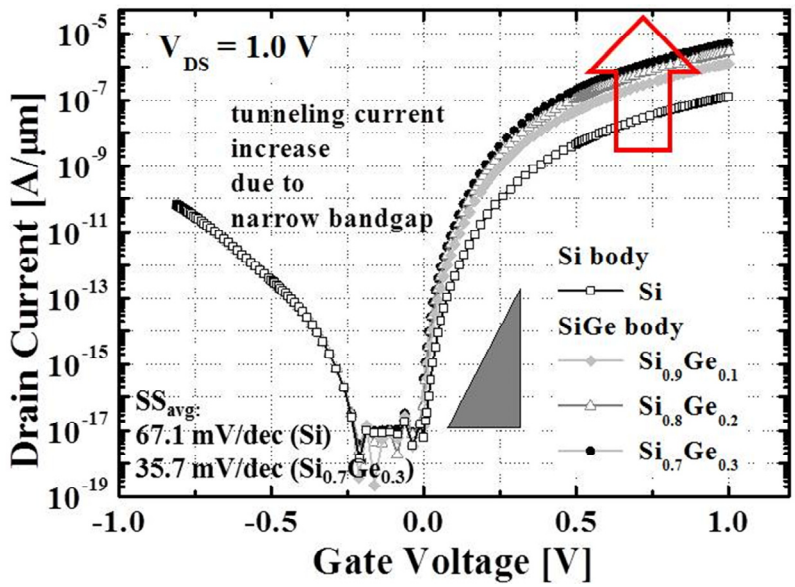
Device parameter	
Lgate	50 nm
EOT	1 nm
T_{SGOI}	20 nm
N_{body}	1×10^{15} cm^{-3}
N_{source}	2×10^{20} cm^{-3}
N_{drain}	1×10^{20} cm^{-3}
Gate W.F.	4.17 eV

(c)

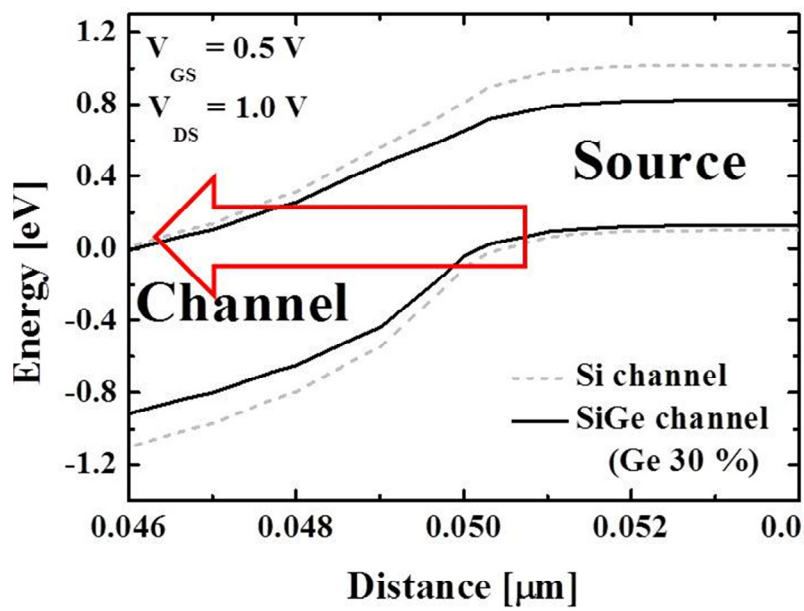
Fig. 3.2. (a) Simulated tunnel FET structure, (b) cross-sectinoal view, and (c) device parameters used in this work.

on the transfer characteristics. First, transfer characteristics of the proposed tunnel FET are investigated as Ge contents in the SiGe body are changed from 0 to 30 percent (Fig. 3.3(a)). The tunnel FET with pure Si fin-channel shows poor switching property as previously reported [46, 47]. The extracted SS_{avg} and $V_{turn\text{-}on}$ are 67.1 mV/dec and 0.47 V due to the large bandgap of Si. From these simulation results, it is observed that the use of narrow bandgap material is very essential to enhance tunneling current. As the Ge content increases in the SiGe body, the bandgap of the source and channel region decreases as shown in Fig. 3.3(b). Consequentially, BTBT generation rates increase and tunneling current increases. In case of the tunnel FET with SiGe body (Ge content of 30 percent), it shows better on/off current ratio compared to the Si tunnel FET. Because of small tunneling resistance, the point of device turn-on starts faster (0.25 V) and SS_{avg} shows a much lower value (35.7 mV/dec). Figure 3.3(c) shows the comparison of the BTBT generation rates in the tunnel FETs with Si and SiGe body at V_{GS} of 0.5 V and V_{DS} of 1.0 V. By using the SiGe body, it is found that BTBT generation rates can be enhanced drastically.

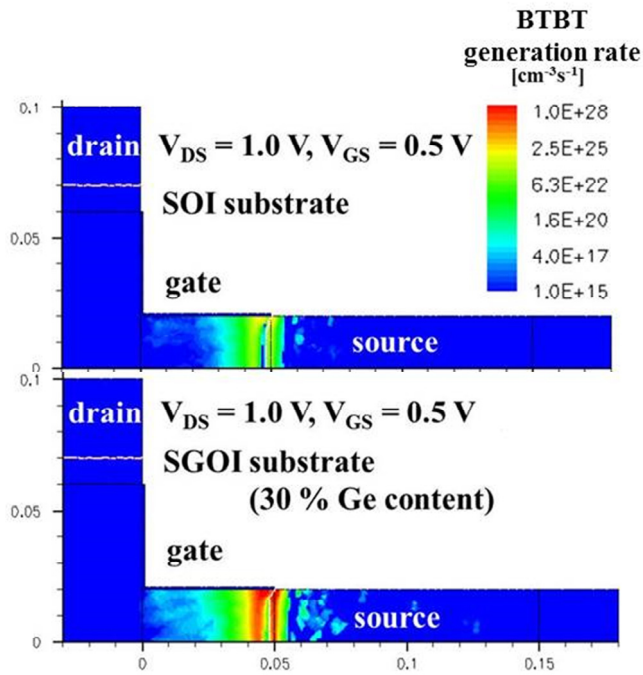
Next, for the elevated drain region, the difference between the Si and SiGe drain region is investigated as shown in Fig. 3.4(a). In case of I_{ON}, there is no difference between the Si and SiGe drain region. It is because I_{ON} is mostly determined by tunneling resistance between the source and channel region. However, in case of the leakage current, the tunnel FET with the elevated SiGe drain has much larger leakage current than that of the tunnel FET with the Si drain. Figure 3.4(b) shows the BTBT generation rates in the


V_{DS} = 1.0 V
tunneling current
increase
due to
narrow bandgap
Si body
Si
SiGe body
$Si_{0.9}Ge_{0.1}$
$Si_{0.8}Ge_{0.2}$
$Si_{0.7}Ge_{0.3}$
SS_{avg}:
67.1 mV/dec (Si)
35.7 mV/dec ($Si_{0.7}Ge_{0.3}$)
Drain Current [A/μm]
Gate Voltage [V]

(a)


V_{GS} = 0.5 V
V_{DS} = 1.0 V
Source
Channel
Si channel
SiGe channel
(Ge 30 %)
Energy [eV]
Distance [μm]

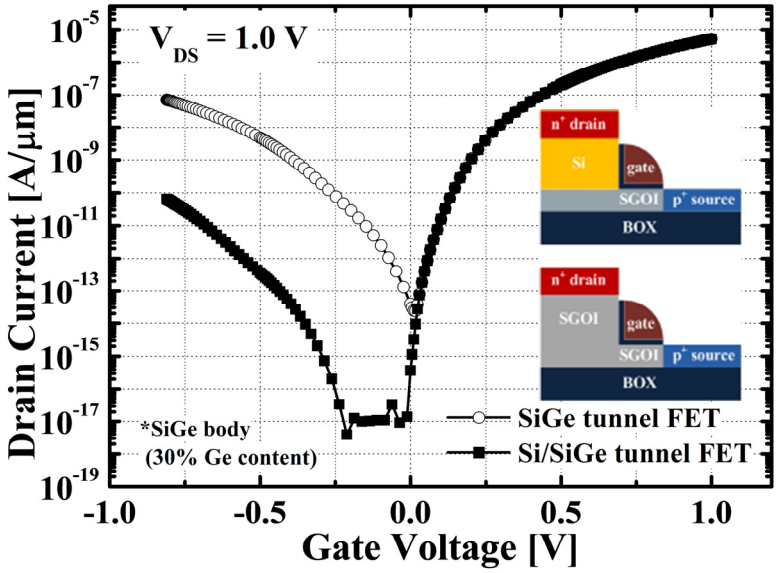
(b)



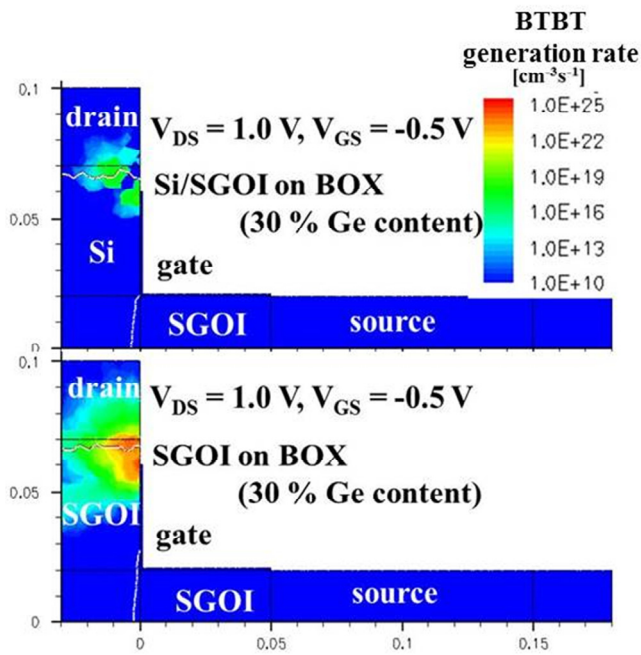
(c)

Fig. 3.3. (a) Transfer characteristics, (b) energy band diagram, and (c) BTBT generation rates with various Ge contents in the SiGe body for the proposed tunnel FET.

drain region at V_{GS} of -0.5 V and V_{DS} of 1.0 V. Thus, the use of the elevated Si drain is essential to suppress leakage current and ambipolar behavior. In terms of the short-channel behavior, the proposed tunnel FET has some advantages. In case of conventional tunnel FET, as the channel length of the tunnel FET is decreased, drain-induced current enhancement (DICE) becomes larger like DIBL of MOSFET. Figure 3.5(a) shows transfer characteristics of conventional tunnel FETs according to gate lengths. Conventional tunnel FET structure has SiGe body (Ge content of 30 percent)



(a)



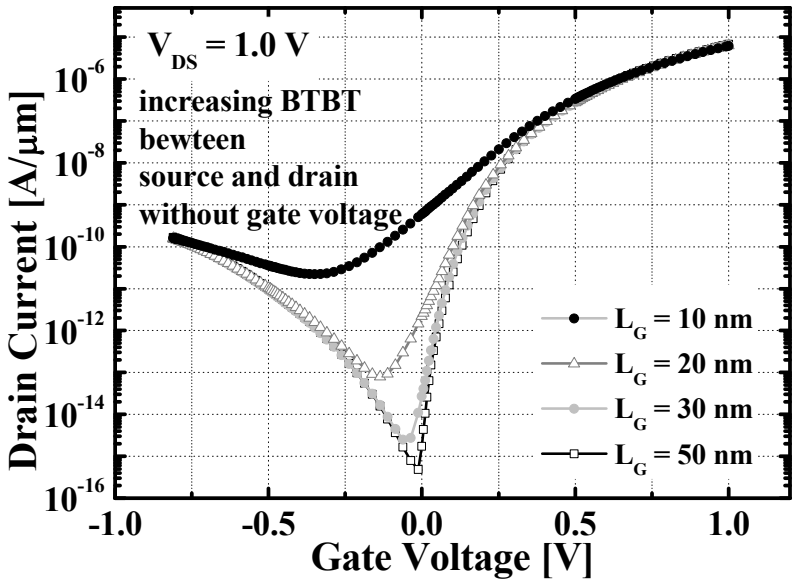
(b)

Fig. 3.4. (a) Transfer characteristics and (b) BTBT generation rates for tunnel FETs with elevated SiGe and Si drain region.

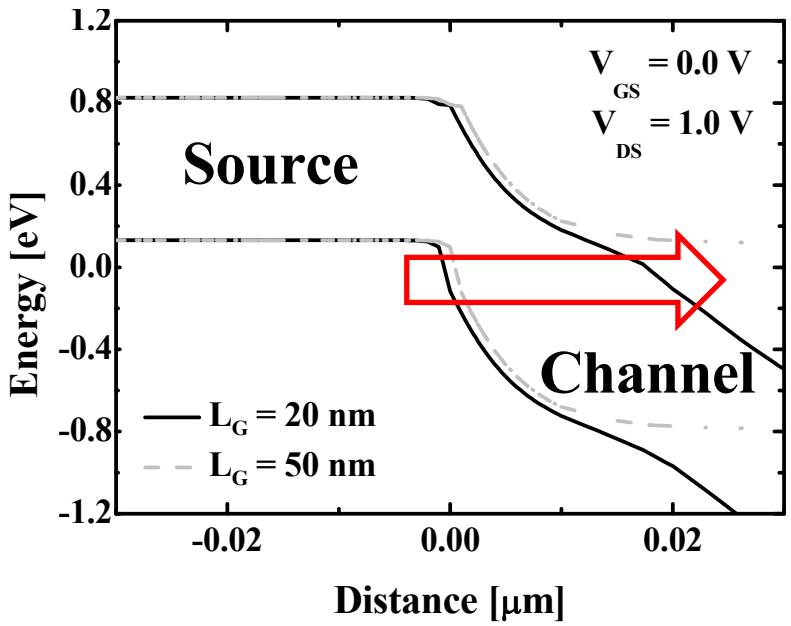
and fin-channel (10 nm F_{width} and 20 nm F_{height}) but no elevated Si drain. As gate length decreases below 20 nm, I_{OFF} and SS property become worse. It is because the tunneling barrier can be modulated by V_{DS} as shown in Fig. 3.5(b). Thus, in tunnel FET with 20 nm gate length, electrons of valence band in source can pass though tunneling barrier without V_{GS}. This phenomenon is called DICE like DIBL in MOSFET. For the proposed tunnel FET with short-channel, DICE characteristics are investigated. Figure 3.6 shows the transfer characteristics of the proposed tunnel FET with the 20 nm and 50 nm gate lengths. As the gate length is reduced, the DICE is not shown despite the very short-channel device. It is because the effective gate length of the proposed tunnel FET is longer than the physical gate length. So, I_{OFF} and SS are less vulnerable to the increase of V_{DS}. As a result, the proposed tunnel FET has strong immunity to SCEs.

3.3 Transient response characteristics

For low power application of tunnel FETs, the electrical characteristics of both n-type and p-type devices are needed to be improved. However, in tunnel FET researches, n- and p-type channel tunnel FET have been optimized separately with different materials system. These advanced tunnel FETs can cause the process complexity and increase of expense when integrated circuits based on tunnel FETs are fabricated. In order to investigate the n-type and p-type tunnel FET with the proposed structure, the transfer characteristics are plotted as shown in Fig. 3.7. The workfunction of p-type tunnel FET



(a)



(b)

Fig. 3.5. (a) Transfer characteristics and (b) energy band diagram of conventnional short-channel tunnel FET.

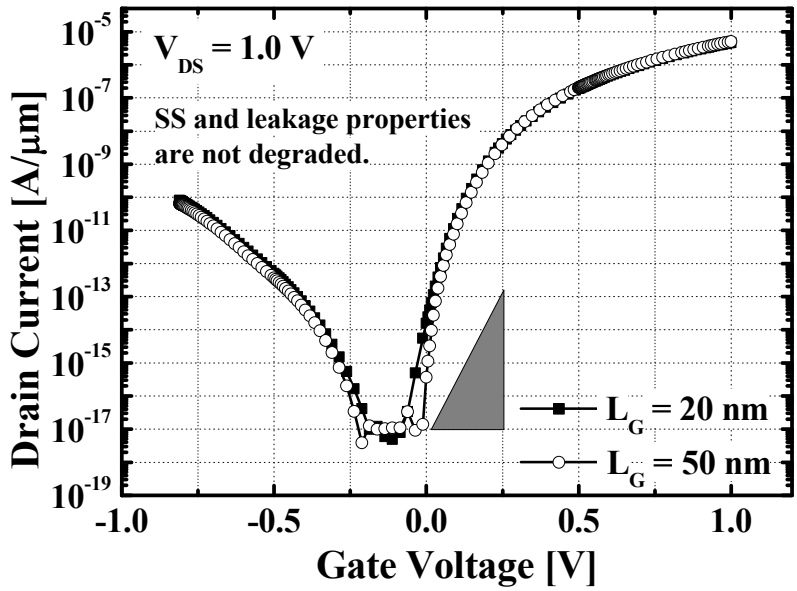


Fig. 3.6. Transfer characteristics of proposed tunnel FET with gate lengh of 20 & 50 nm.

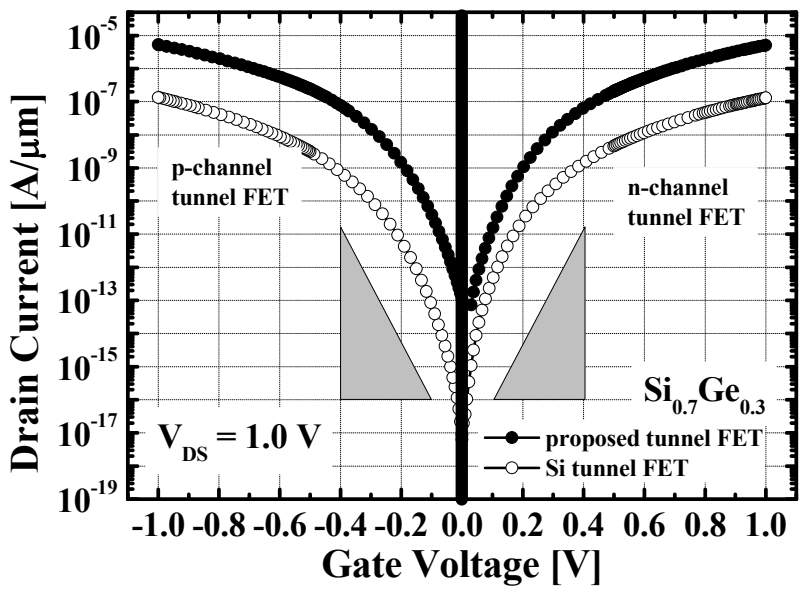


Fig. 3.7. Transfer characteristics of the n-type and p-type proposed tunnel FETs.

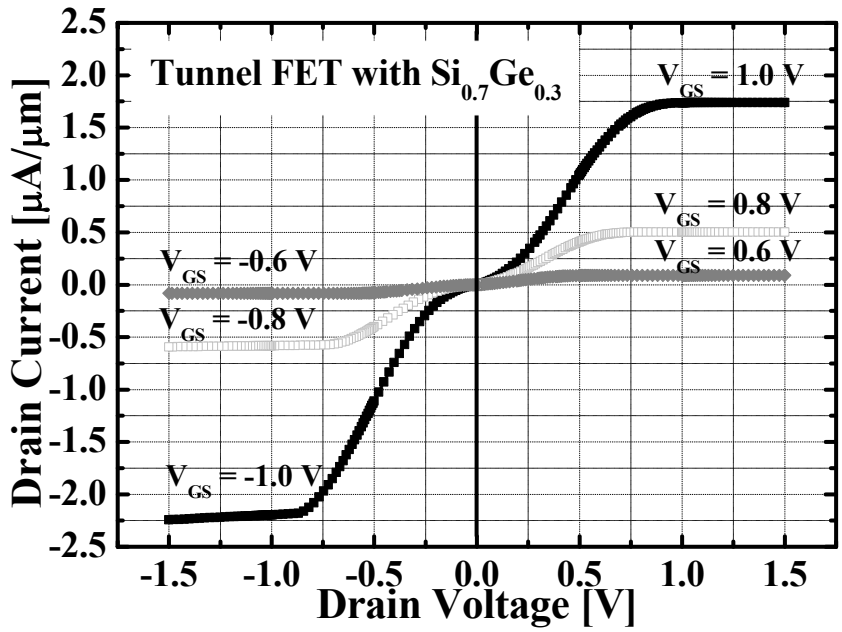


Fig. 3.8. Output characteristics of the n-type and p-type proposed tunnel FETs.

is set to be 4.9 eV to match the characteristics of the n-type tunnel FET. It is observed that both n-type and p-type tunnel FET characteristics are improved due to the increase of Ge contents in the SiGe body. From these results, it is very effective to improve the tunnel FET performance without structural changes in n-type and p-type tunnel FETs. Figure 3.8 shows the output characteristics of the proposed tunnel FET with the SiGe body (Ge content of 30 percent). Although the current drivability seems to weaken at a small V_{DS}, the proposed tunnel FET has a large I_{ON} compared with experimental data of the Si tunnel FET.

Based on these simulation results of n-type and p-type tunnel FETs, transient response characteristics of the proposed tunnel FET are investigated using mix-mode

inverter simulation. The Si and proposed tunnel FET-based inverters are used. Input ramp voltage is applied to peak voltage of 1.2 V and rise time of 1 ns. For considering fan-out, load capacitor (C_L) of 0.54 fF is used. It is well known that AC characteristics of tunnel FET are closely related with gate-to-drain capacitance (C_{GD}) [48-51]. Unlike MOSFET, C_{GD} of tunnel FET is larger than C_{GS} because of potential barrier between source and channel. Also, C_{GD} directly affects the output node of inverter resulting in delay increase of output voltage. From transient response characteristics of inverters with Si and proposed devices, it occurs overshoot/undershoot of output voltage as shown in Fig. 3.9. However, in case of the Si inverter, it is observed that pull-up/pull-down at output node does not continuously sustain during applying input voltage. The reason is that load capacitor can't be sufficiently charged and discharged due to low current level by large tunneling resistance. For inverter with proposed device, although a little delay property is shown in transient response characteristics, pull-up/pull-down can be occurred due to high current drivability.

In order to investigate delay property in the proposed device, the transient response characteristics of the proposed device are examined according to drain width as shown in Fig. 3.11(a). Figure 3.10 shows the C_{GD} of the proposed tunnel FET with drain width variation. As drain width increases, more electrons in drain region can move the conduction band in channel region leading to high C_{GD}. As a result, transient response becomes worse as shown in Fig. 3.11(b). From transient response characteristics, delay time is extracted in Fig. 3.11 (c). When drain width is 50 nm,

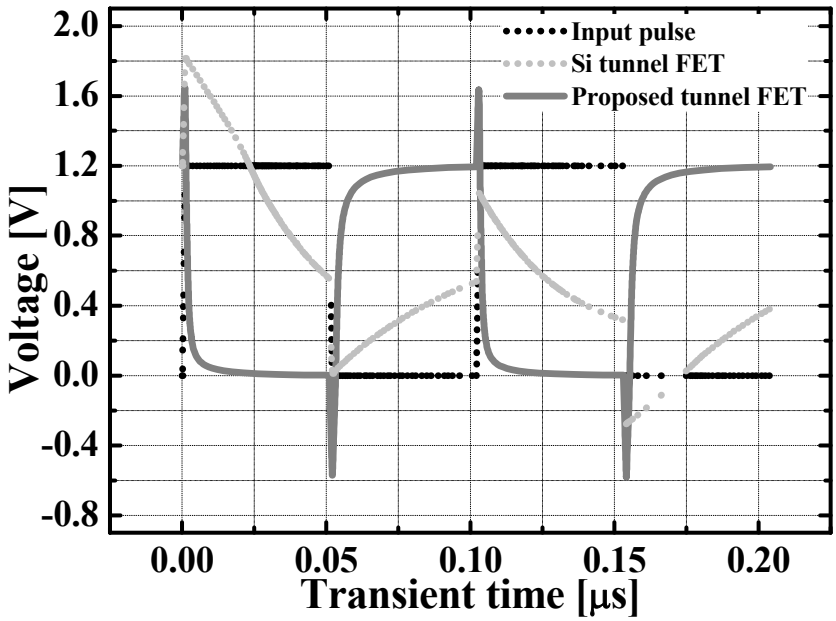


Fig. 3.9. Transient response of Si and proposed tunnel FET-based inverters

delay of 4.25 ns is observed. However, delay increases more than 1.5 times in case of 200 nm drain width. This means that narrow drain width is needed for better transient characteristics.

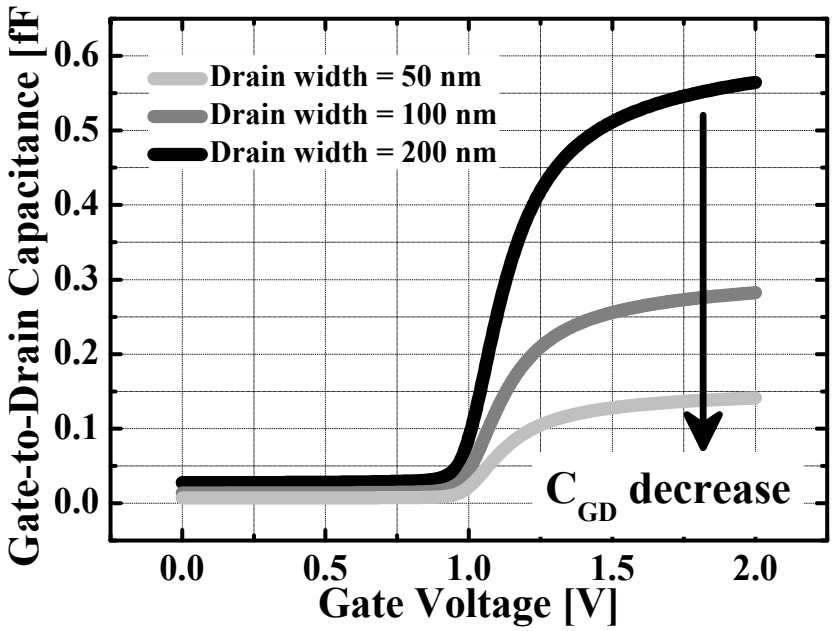
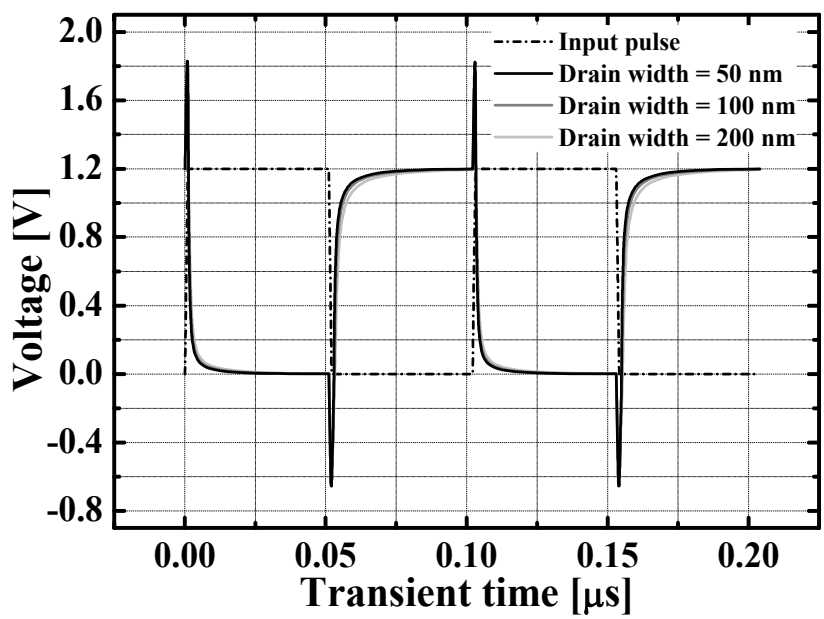
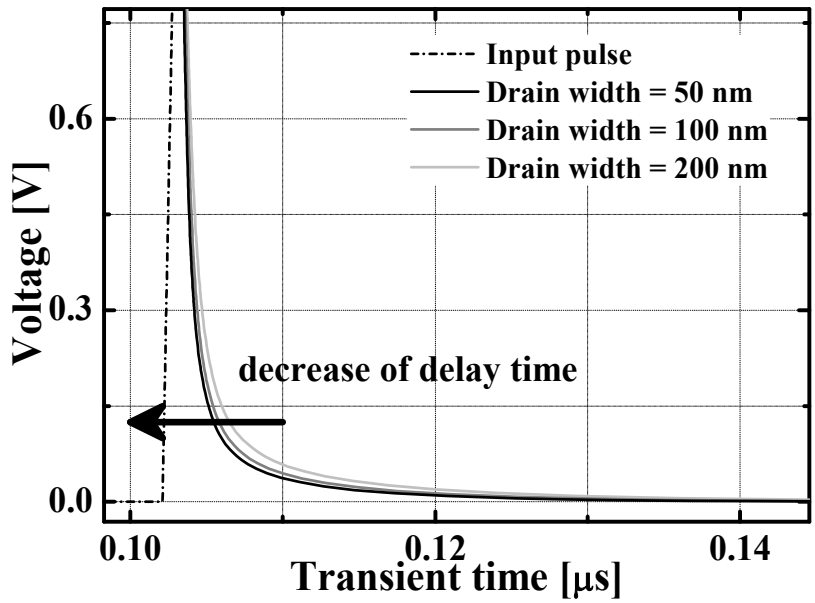


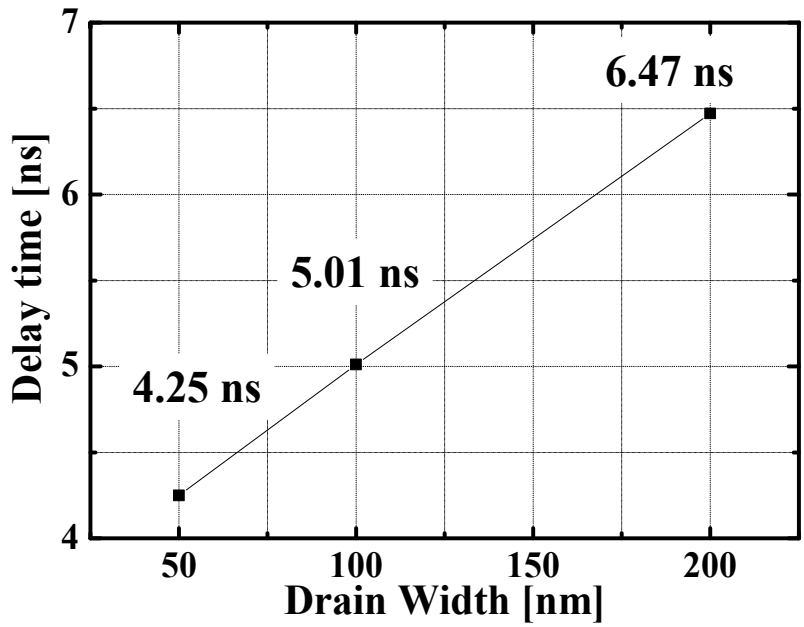
Fig. 3.10. Gate-to-drain capacitance with drain width variation



(a)



(b)



(c)

Fig. 3.11. (a) Transient response characteristics, (b) effect on drain widh variation, and (c) delay time for the proposed tunnel FET.

Chapter 4

Device Characteristics

In this chapter, process flows is firstly explained for device fabrication. For self-aligned doping process, gate spacer technique is applied. Thus, it is possible to make short-channel device without DICE. Also, the key unit process among process flows describes in detail. Next, the electrical characteristics of fabricated devices are investigated with control groups in terms of SS characteristics, I_{ON}, I_{AMB}, and temperature effects.

4.1 Process flow

As mentioned in Section 1.3, the proposed tunnel FET is designed with self-aligned doping process and short-channel. Fabrication sequence follows the process flow given below (Fig. 4.1). (a) First, silicon-on-insulator (SOI) thickness is reduced by

using dry and wet oxidation process and SiGe/Si epitaxial growth layers which is defined as channel and drain are conducted. (b) Ion implantation is performed after drain region and nitride are deposited using plasma-enhanced chemical vapor deposition (PECVD). The reason why PECVD nitride uses implanted dopants in drain region can rarely diffuse due to low temperature process. (c) Active region is defined using photolithography and reactive ion etching (RIE) process. (d) Using photoresist (PR) mask, drain region is formed by nitride and silicon RIE process. Then, narrow active fin patterning is conducted by using optimized mix-and-match process through negative-resist electron-beam (e-beam) lithography, PR mask, and RIE process. Additionally, in order to enhance gate controllability, fin trimming is performed by standard cleaning-1 (SC-1) solution. (e) Using selective epitaxial growth (SEC), 1 nm Si capping layer is conducted to prevent defects induced between Si and SiGe. After that, thin gate oxide (T_{OX} = 3 nm) is grown by dry oxidation. (f) Doped poly-Si gate is directly deposited using low pressure chemical vapor deposition (LPCVD). For gate patterning, sidewall spacer technique is applied to be possible to make short-channel tunnel FET. Gate length is defined by thickness of doped poly-Si deposition and RIE process. Then, source region is formed and (g) dopant activation is performed by RTP with 900 °C and 5 sec. For passivation, high-density plasma (HDP) oxide is deposited as inter-layer dielectric (ILD) and chemical mechanical (CMP) polishing process is conducted for oxide planarization. (h) Contact holes formation, metal (Ti/TiN/Al/TiN) deposition, and RIE are performed, sequentially. Next chapter shows that critical fabrication steps are

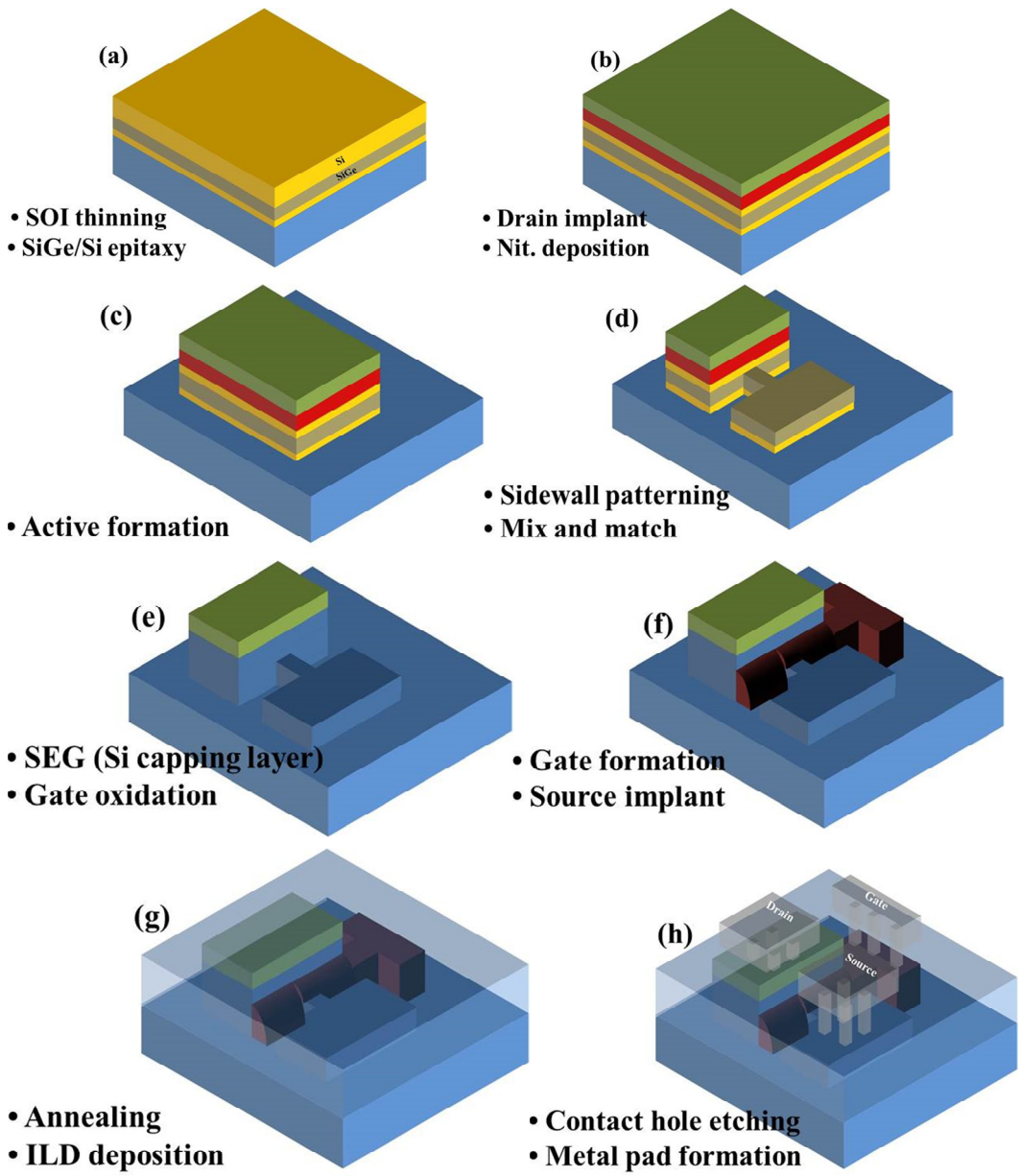
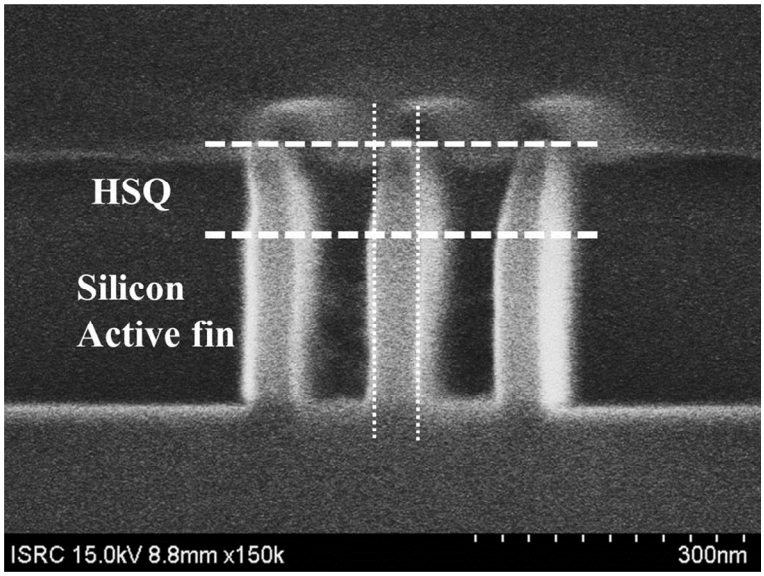


Fig. 4.1. Fabrication flow of the proposed tunnel FET.

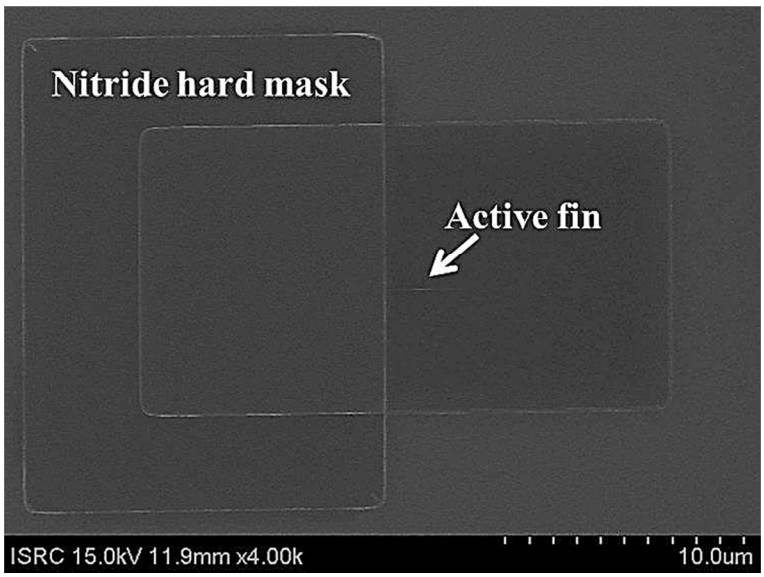
described in more details among these fabrication flows.

4.2 Active fin patterning using e-beam lithography

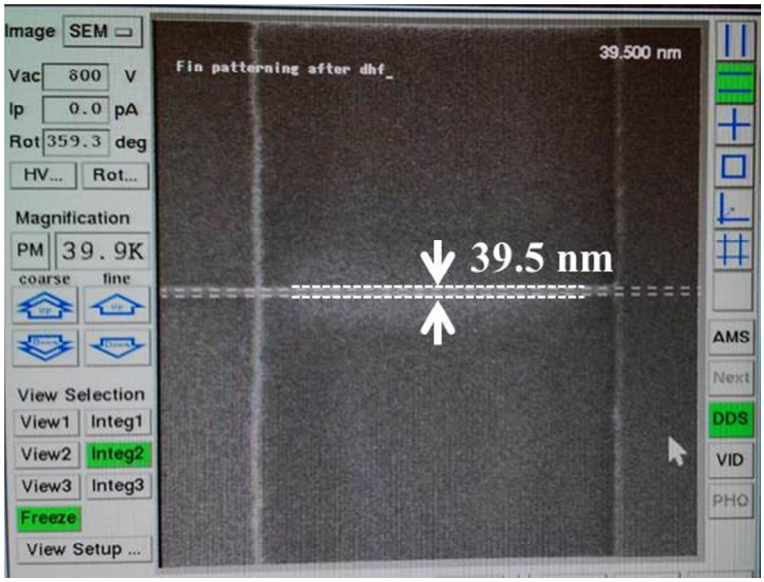
For making SOI wafer samples with the same process condition, thermal oxide of 375 nm is grown on p-type (100) Si wafers and poly-Si of 200 nm is deposited using LPCVD like SOI wafer. Then, nitride of 100 nm is formed using PECVD. Channel thickness is reduced through RIE process using nitride hard mask. After that, hydrogen silsesquioxane (HSQ) of 130 nm is coated and 1000 dose is exposed for e-beam lithography. When e-beam process is performed, dummy e-beam patterns are also made because pattern slopes of active fin as shown in Fig. 4.2(a) [52]. Finally, active fin patterning is performed using mix-and-match process as shown in Fig. 4.2(b). Formed active fin shows width of about 50 nm. However, active fin needs to be less than 50 nm for high electrical performance of tunnel FET. These active fins can be reduced using SC (standard cleaning) -1 solution. It is well known that Si and SiGe materials are slightly etched during SC-1 process [53, 54]. Its solution consists of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and de-ionized wafer (H_2O). The main purpose of H_2O_2 is to oxidize Si or SiGe, and oxide is then dissolved with help of NH_4OH. Thus, the loss of Si or SiGe occurs during this process. For reducing active fin using this chemical property, etch rates of SiGe materials are investigated in SC-1 solution. Composition ratios of SC-1 solution used are 1:1:5 (80 °C) and 1:8:64 (65 °C),


HSQ
Silicon
Active fin
ISRC 15.0kV 8.8mm x150k
300nm

(a)


Nitride hard mask
Active fin
ISRC 15.0kV 11.9mm x4.00k
10.0um

(b)



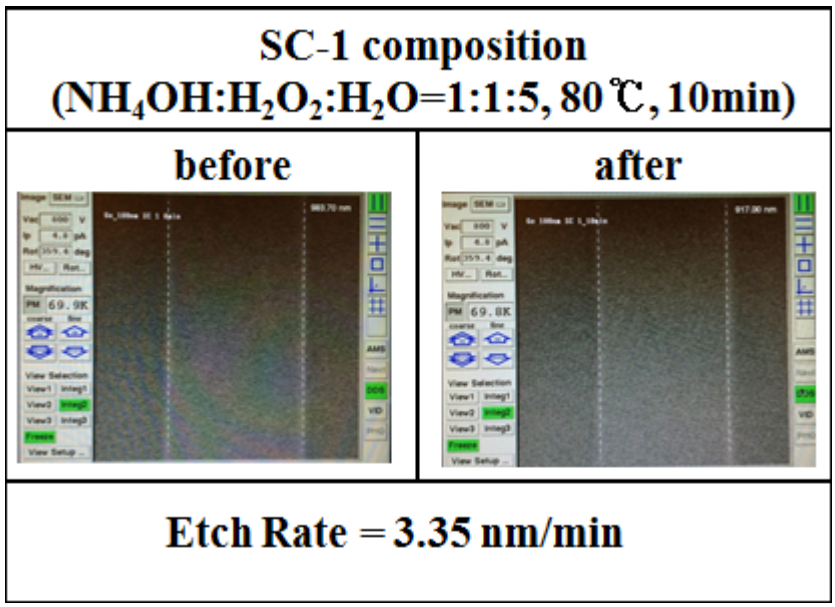
(c)

Fig. 4.2. (a) Cross-sectional, (b) top-view FE-SEM image of active fin formed after mix-and-matching process and (c) CD-SEM image of active fin formed by using SC-1

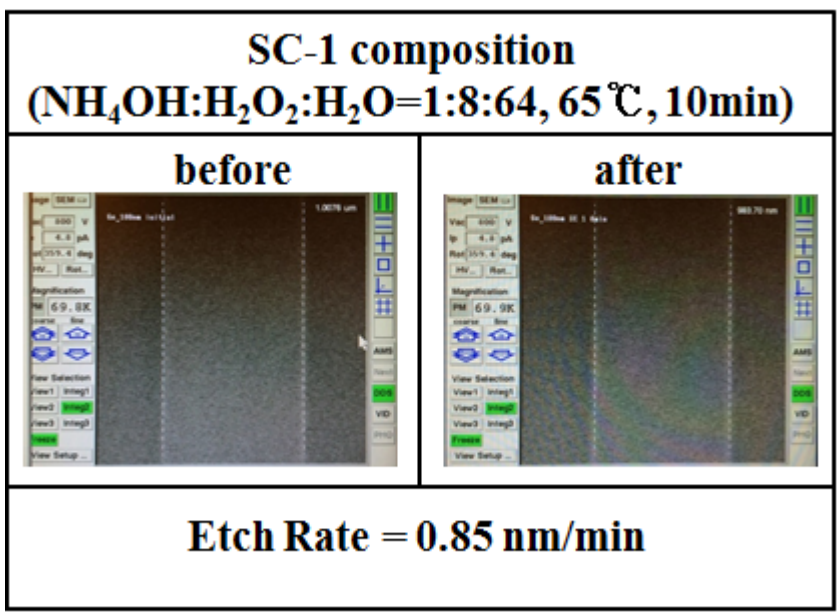
respectively. Process is conducted during 10 minutes. From Fig. 4.3, when composition ratio of 1:1:5 is used, etch rate of 3.35 nm/min is observed. Also, etch rate of SiGe is 0.85 nm/min by using SC-1 composition of 1:8:64. Based on these results, very narrow fin below 50 nm can be implemented by using SC-1 solution as shown in 4.2(c).

4.3 Drain and gate formation

In order to make drain region of the proposed tunnel FET, ion implantation process is performed after SiGe and Si epitaxial growths. Thus, it is important to inform predict junction depth of drain region by implantation process. When implanted dopants are



(a)

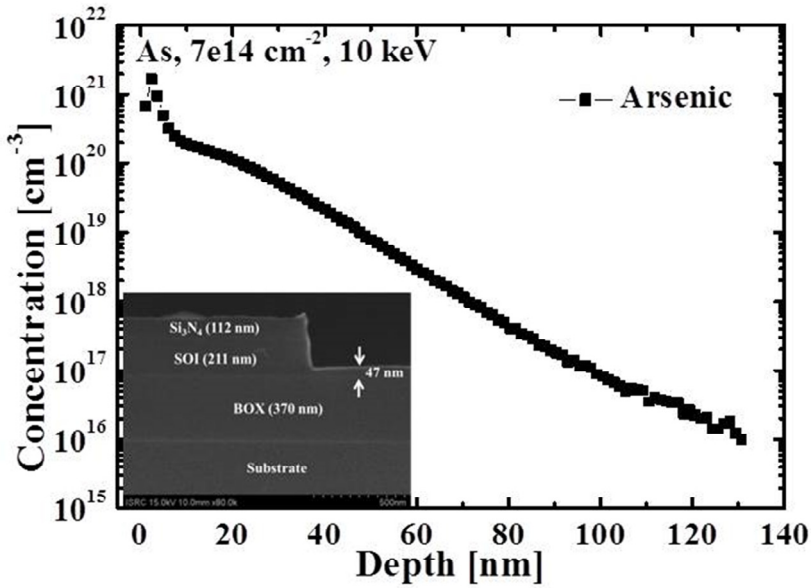


(b)

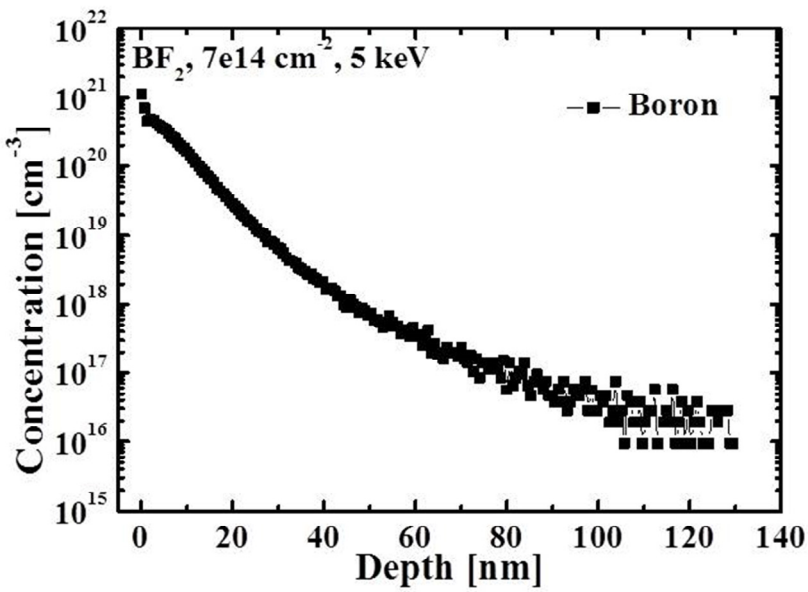
Fig. 4.3. SiGe etch rates using SC-1 solution with composition ratio of (a) 1:1:5 and (b) 1:8:64.

diffused in channel region, it can affect device characteristics. For obtaining accurate junction depths of As and BF_2 in p-type (100) wafers, samples are made for secondary ion mass spectrometry (SIMS) analysis. Implantation conditions of BF_2 are dose of 7×10^{14} cm^{-2} and energy of 5 keV for p-type tunnel FET. On the other hand, As implantation energy is 10 keV with 7×10^{14} cm^{-2} dose for n-type tunnel FET because of atomic mass difference. After that, RTP process (900 °C, 5 sec) is performed for dopant activation. From these samples, As and B concentration in the depth direction from surface are performed by using SIMS analysis as shown in Fig. 4.4. In case of As, junction depth of 90 nm is observed from surface. Also, junction depth of B is 80 nm. Thus, it is necessary that channel region have to be formed below 100 nm from surface for avoiding effects induced by drain region.

For gate formation of the proposed tunnel FET, sidewall spacer technology is applied. Samples are firstly fabricated as shown in Fig. 4.5(a). After that, SPM and SC-1 cleaning are performed due to surface cleaning. Then, gate oxidation of 3 nm and doped poly-Si deposition of 150 nm are conducted, sequentially. When poly-Si gate is etched, it is difficult to form perfectly gate region due to very thin gate oxide. Thus, RIE process is performed twice because micro-trenching may occur at gate edge region. Poly-Si of 120 nm is firstly etched using Cl_2 and HBr gas. Then, poly-Si residue is completely removed by using same gas. As a result, gate length of 76 nm can be obtained as shown in Fig. 4.5(b).

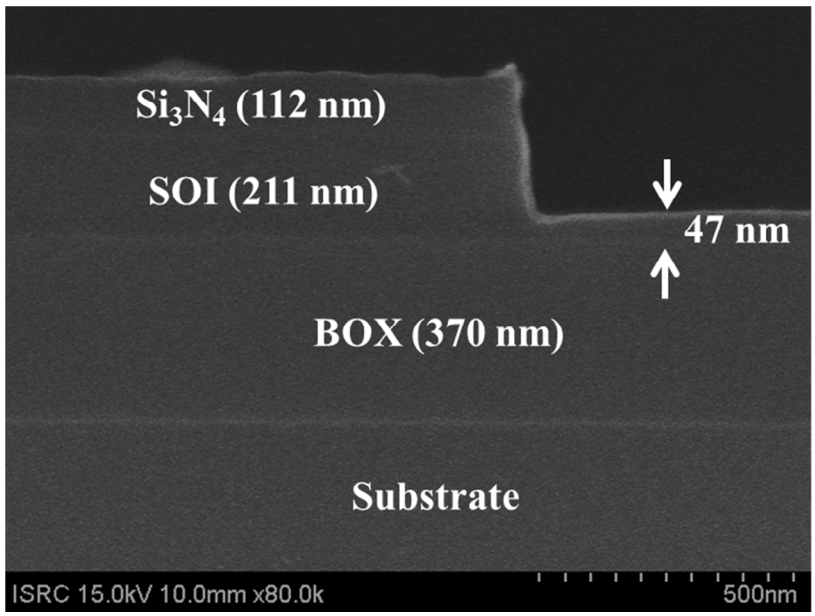


(a)

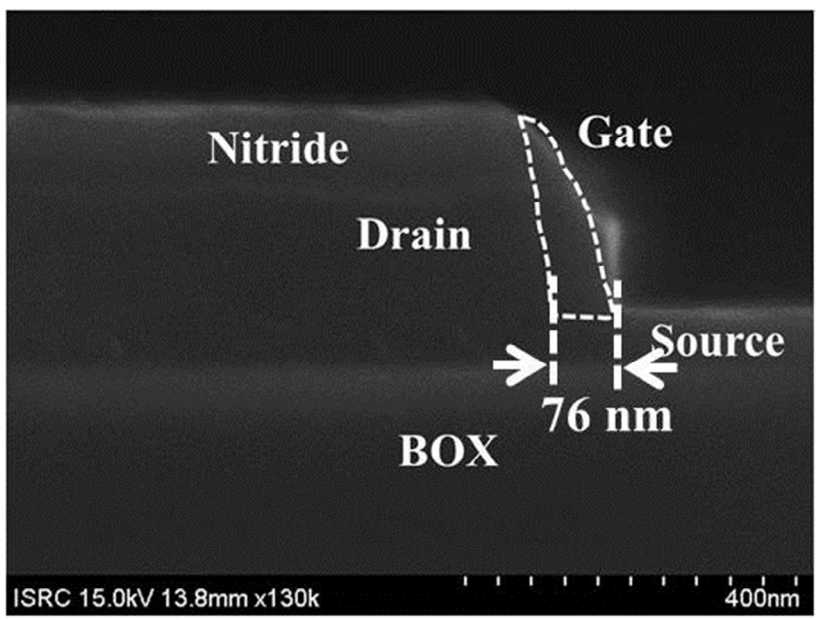


(b)

Fig. 4.4. (a) As and (b) B concentrations in the depth direction from surface using SIMS.



(a)



(b)

Fig. 4.5. (a) Before image and (b) after image for sidwall spacer gate formation.

4.4 Device Characteristics

Based on the unit process results, n-type and p-type proposed tunnel FETs are fabricated by using process conditions of Fig. 4.6. Also, planar Si and SiGe tunnel FETs are implemented as control groups. For confirming p-i-n junction in the proposed tunnel FET, diode characteristics are firstly examined. Thus, the proposed tunnel FET with gate length of 100 nm and width of 50 nm has been measured while gate is floated. As shown in Fig. 4.7, the p-i-n junction is well operated as V_{DS} changes.

The transfer characteristics of n-type and p-type proposed devices are investigated with increasing V_{DS}. From Fig. 4.8, $V_{turn\text{-}on}$ is a 0.75 V for n-type device and -2.15 V for p-type device. Since the gate material used in fabricated devices is n-type doped poly-Si, gate workfunction is 4.17 eV. Thus, it is observed that p-type tunnel FET has large $V_{turn\text{-}on}$. Minimum SS of 87 mV/dec is extracted for n-type device. Extracted SS_{avg} is 366 mV/dec. In case of p-type device, minimum SS is 51.1 mV/dec and SS_{avg} is 115 mV/dec. Also, the output characteristics of n-type and p-type devices are measured as shown in Fig. 4.9. In case of the p-type device, current saturation is faster than that of n-type device. This means that p-type device has larger current drivability because of small tunneling resistance. On the other hand, n-type tunnel FET shows poor switching compared with p-type tunnel FET as shown in Fig. 4.8. This result is caused by dopant diffusion difference. Boron dopants in the n-type device source region are easily diffused compared with heavy arsenic dopants in the p-type device source region during thermal annealing process for dopant activation. As a result, tunneling resistance

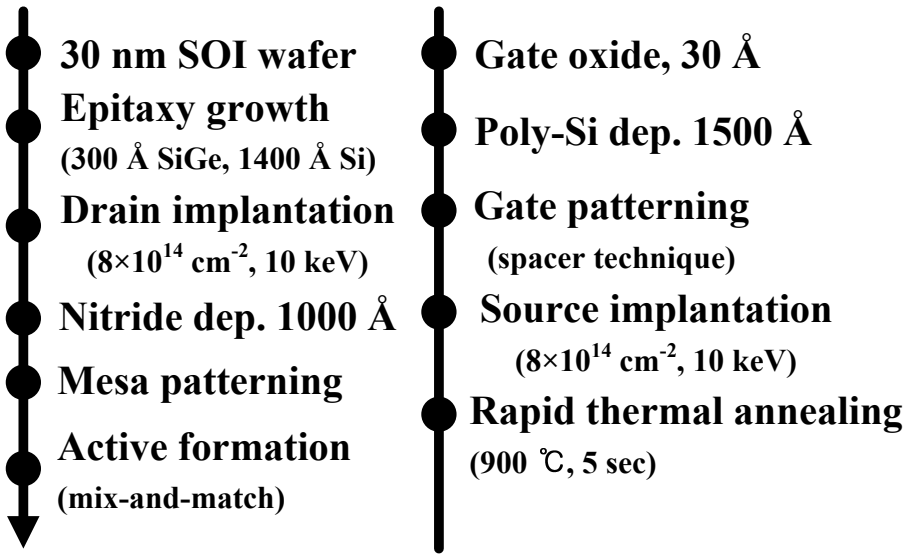


Fig. 4.6. Device process condition for proposed tunnel FET.

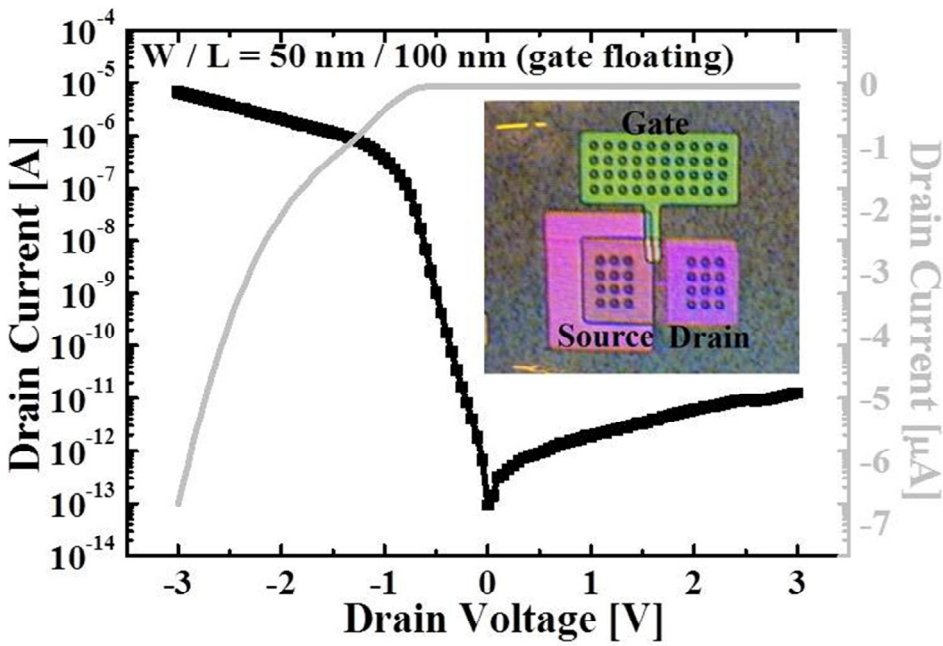
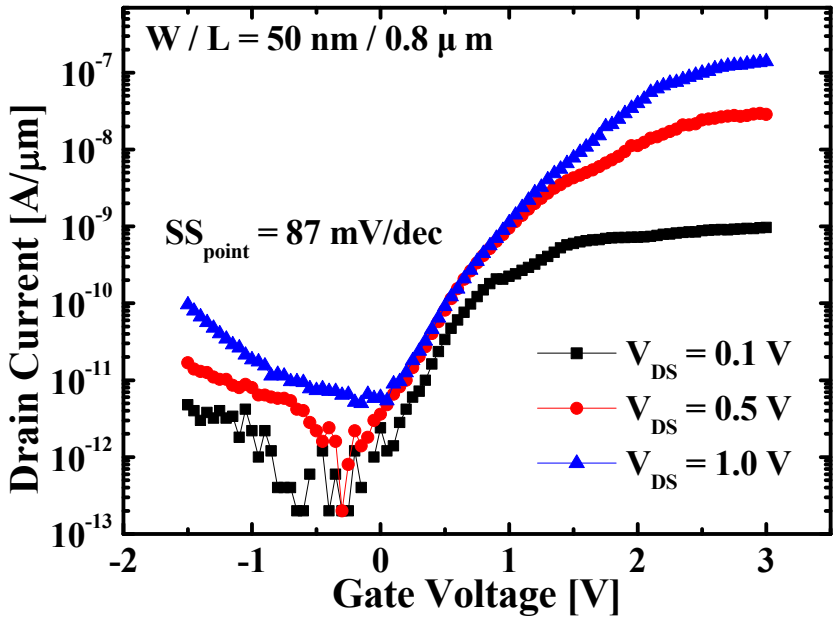
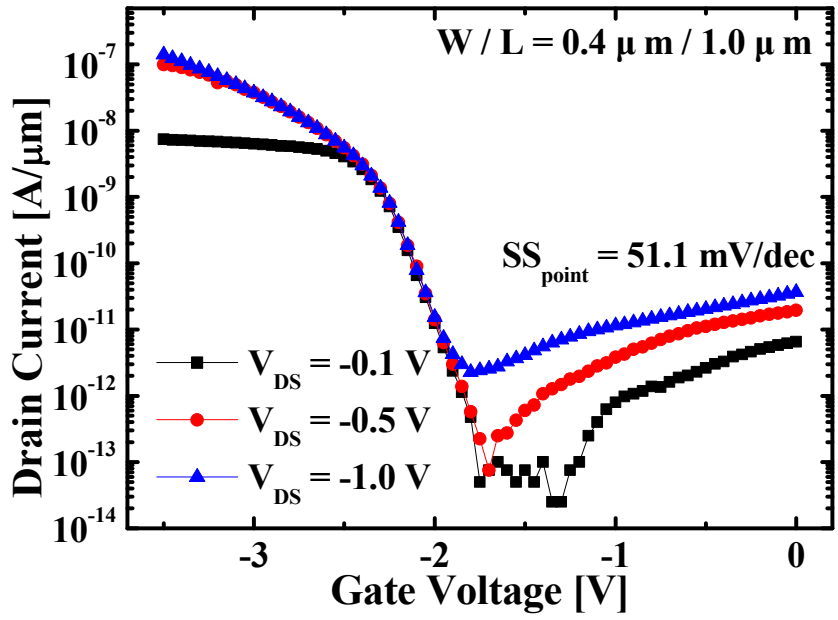


Fig. 4.7. Diode characteritics of proposed tunnel FET.

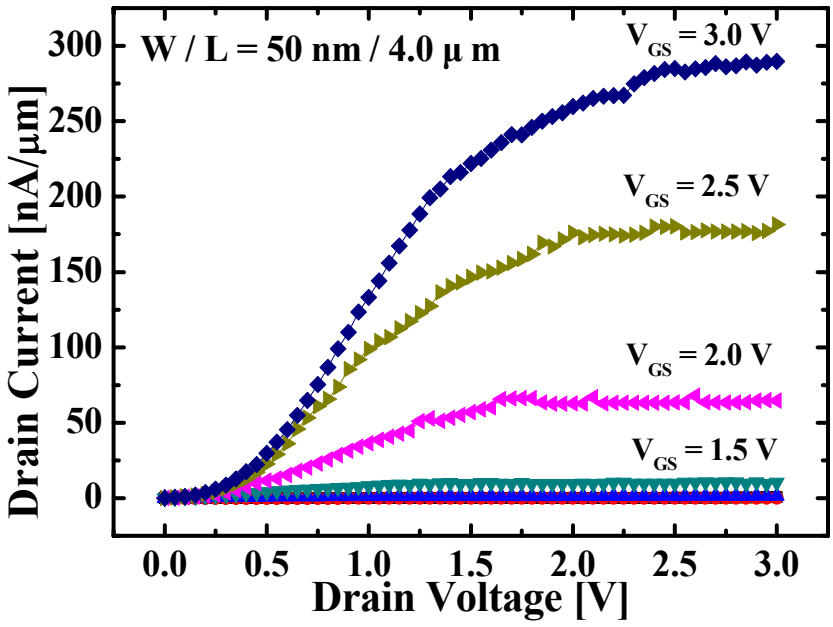


(a)

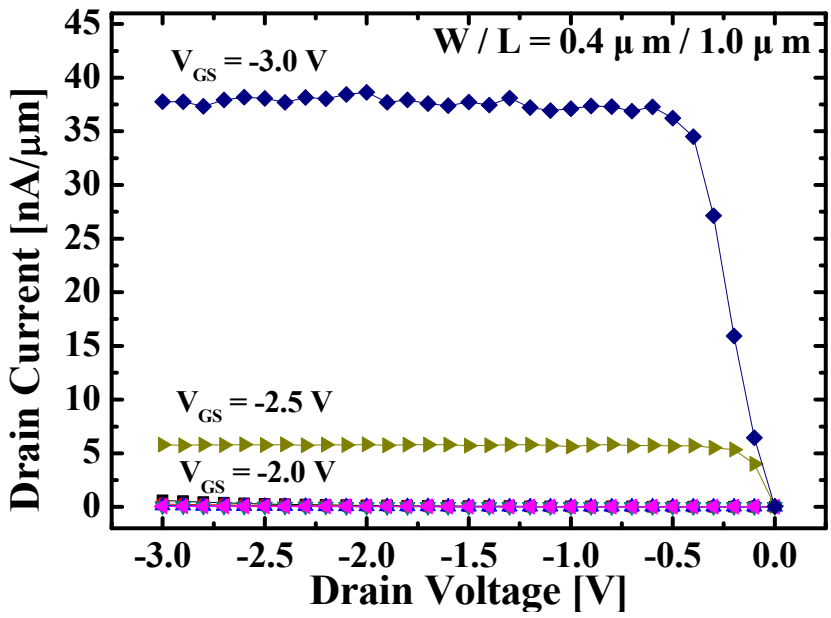


(b)

Fig. 4.8. Transfer characteristics of (a) n-type and (b) p-type proposed tunnel FET.



(a)

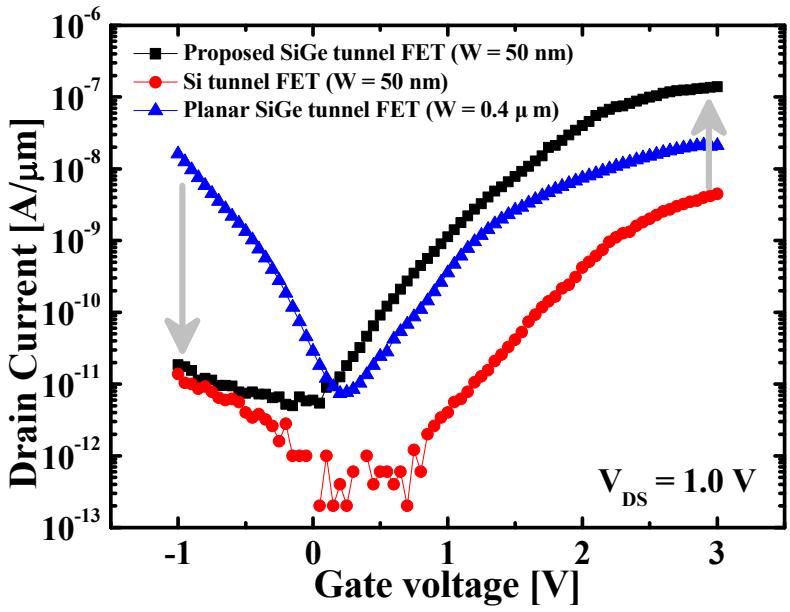


(b)

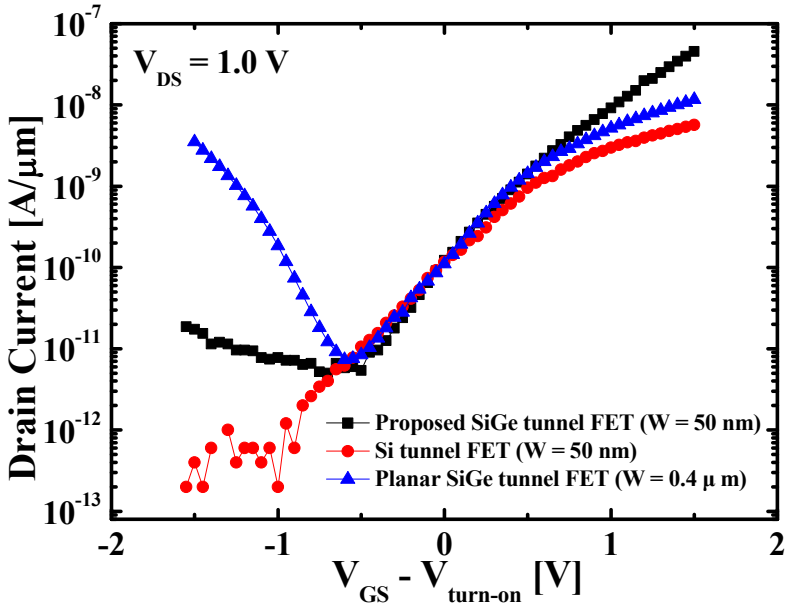
Fig. 4.9. Output characteristics of (a) n-type and (b) p-type proposed tunnel FET.

between the source and channel becomes larger resulting in poor SS and I_{ON} properties. For comparison between experimental and control groups, Figure 4.10(a) shows the transfer characteristics of n-type tunnel FETs at V_{DS} of 1.0 V. Control groups consist of proposed Si tunnel FET and planar SiGe tunnel FET. The SS property of the proposed device is improved due to narrow bandgap. However, each device has different $V_{turn\text{-}on}$. Thus, transfer characteristics are shifted as $V_{turn\text{-}on}$ for correct comparison. From 4.10(b), I_{ON} is 10 times more than that of Si control group. Compared with planar SiGe tunnel FET, I_{ON} of the proposed tunnel FET is increased by more than 4 times. I_{AMB} is suppressed to 1/100 of that of planar SiGe device. It is because the fin channel and elevated Si drain region are used for high gate controllability and tunneling current reduction between channel and drain. For p-type tunnel FETs, transfer characteristics are investigated as shown in Fig. 4. 11(a). Control groups is composed of planar Si and SiGe tunnel FETs. For p-type devices, transfer characteristics are moved as $V_{turn\text{-}on}$. From 4.11(b), I_{ON} of the proposed device is larger than 12 times that of the Si control group. Also, it is found that I_{AMB} is suppressed to 1/10 of that of the control group. From transfer characteristics, it is observed that leakage current level of the proposed tunnel FET is higher than those of Si control groups. The reason is for theraml-generation component induced by SiGe materials with narrow bandgap.

In order to analyze current flow mechanism of the proposed device, temperature effects are investigated as shown in Fig. 4.12(a). As temperature increases, thermal-generation current is increased for OFF state. In ON state, tunneling current is slitly

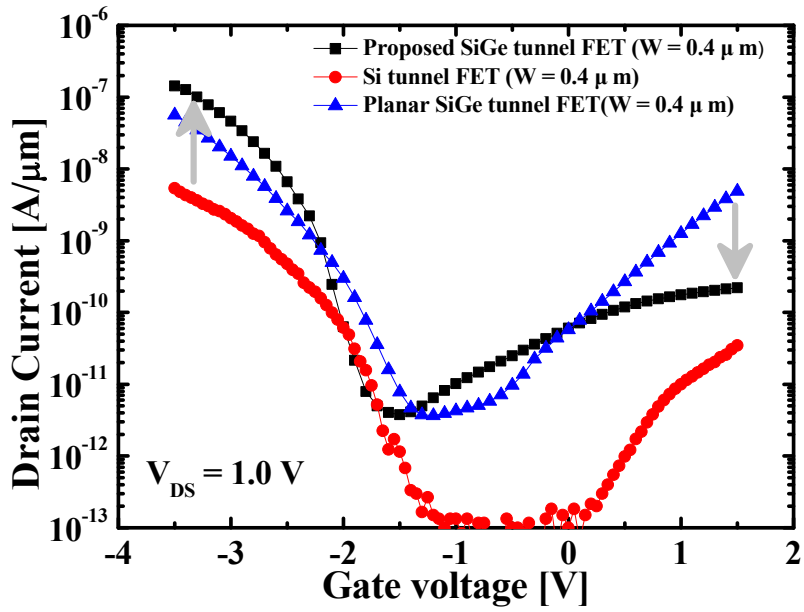


(a)

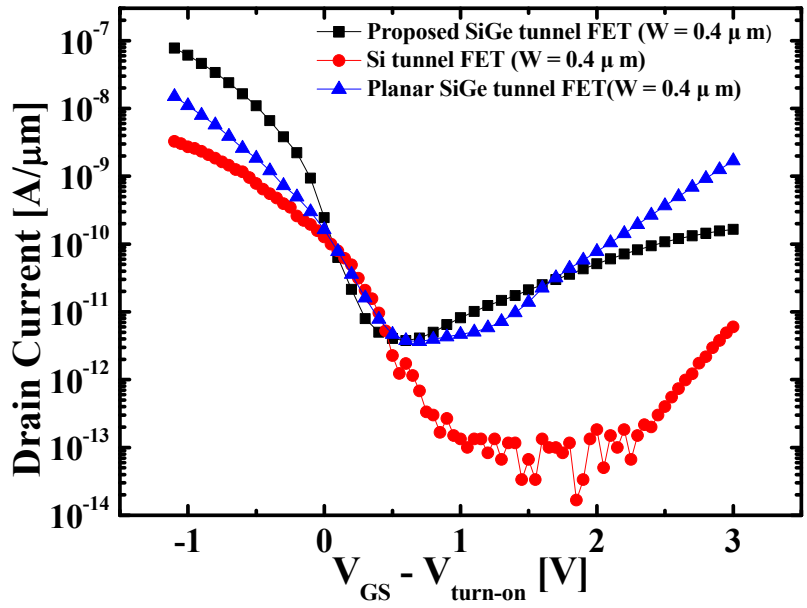


(b)

Fig. 4.10. Comparison of transfer characersitics for n-type devices.

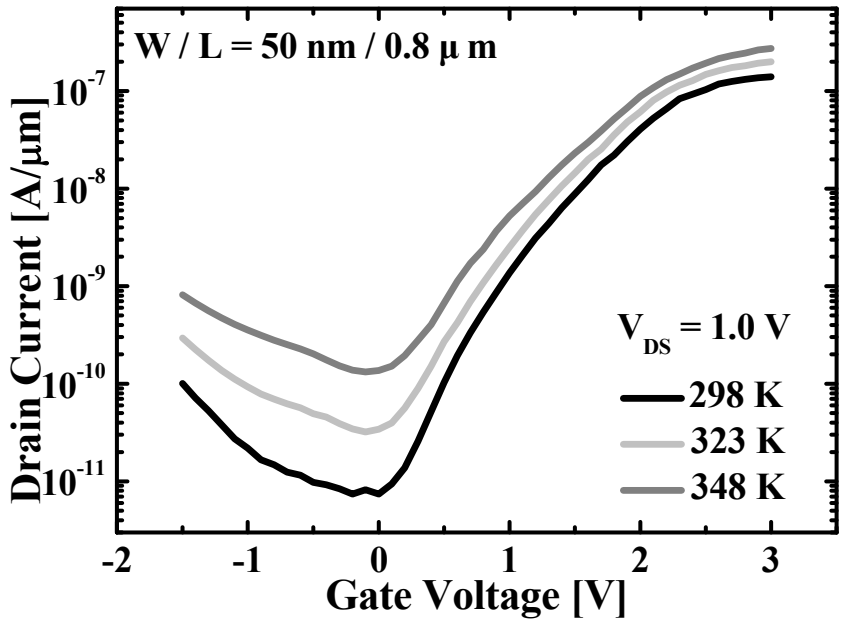


(a)

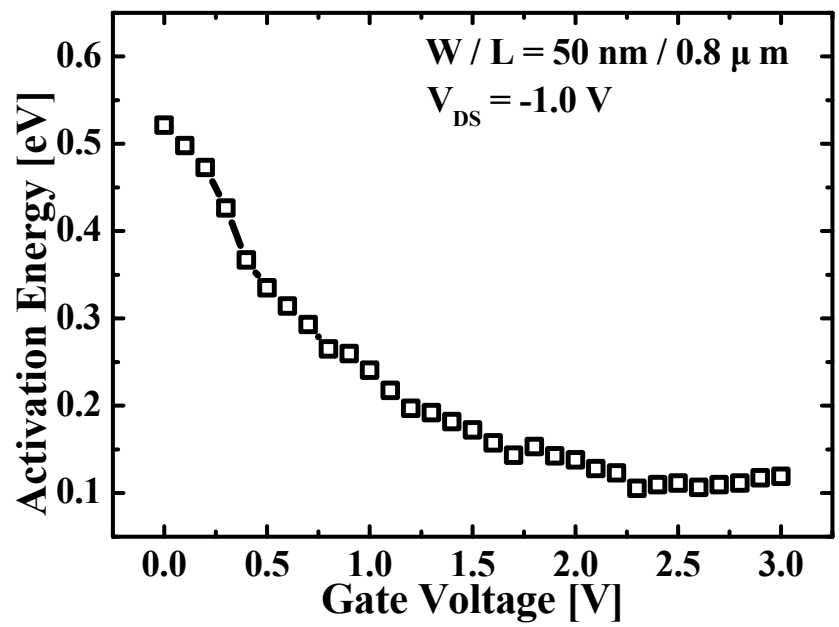


(b)

Fig. 4.11. . Comparison of transfer characersitics for p-type devices.

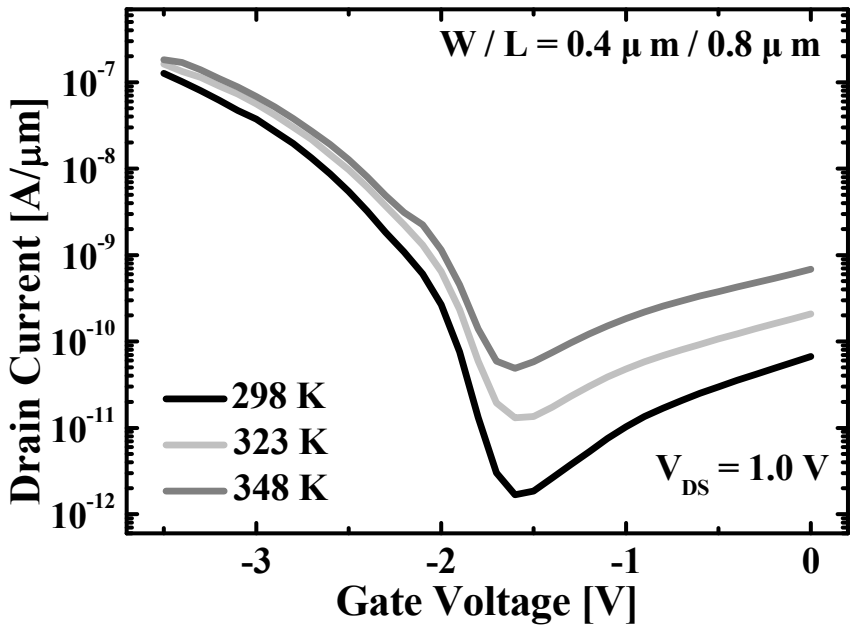


(a)

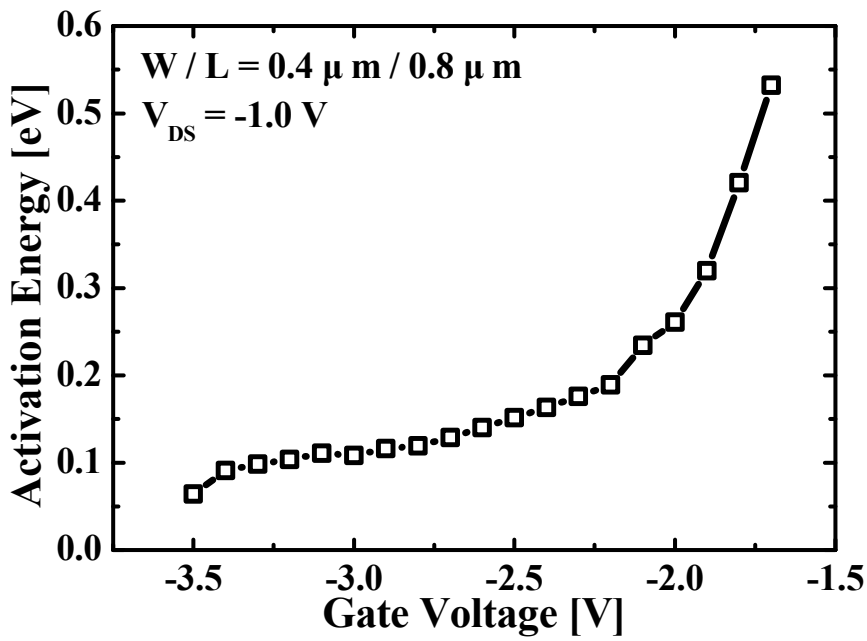


(b)

Fig. 4.12. (a) Temerature effects and (b) activation energy of n-type proposed tunnel FET.



(a)



(b)

Fig. 4.13. (a) Temerature effects and (b) activation energy of p-type proposed tunnel FET.

increased since channel bandgap is reduced in high temperature. To confirm sensitivity of temperature in tunnel FET, activation energy is extracted by using Arrhenius plot as shown in Fig. 4.12(b). In bias condition which tunnleing can't occur, thermal-generation component is dominant. Thus, activation energy extracted for this region shows a half of energy bandgap. Then, as V_{GS} increases, it is observed that SS characteristics are degraded and I_{OFF} is increased because field-dependent SRH generations are increased at junction between source and channel region. As tunneling current flows, BTBT is dominant and activatoin energy decreases. For p-type tunnel FET, it is observed that temperature characteristics are similar to those of n-type device as shown in Fig. 4. 13.

4.5 Reason of degraded characteristics in n-type device

For fabricated device, n-type tunnel FET shows worse characteristics than p-type device. As mentioned before, the reason is that boron profile shows gradual profile because of boron penetration and light atomic mass of boron. In order to investigate these effects, device simulations are performend with junction profile. a situation induced by boron penetration is considered. When boron penetration occurs, channel doping goes higher. Thus, the electrical characteristics with channel doping variation are investigated as shown in Fig. 4.14. It is observed that tunnel FET with high channel doping has poor switching characteristics than device with low channel doping. Additionally, Figure 4.15(a) shows the electrical characteristics with changing junction

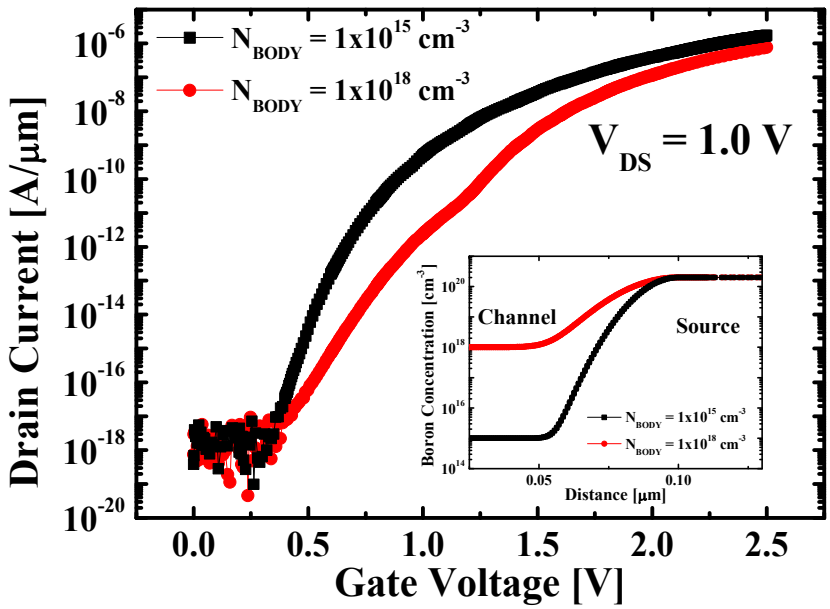
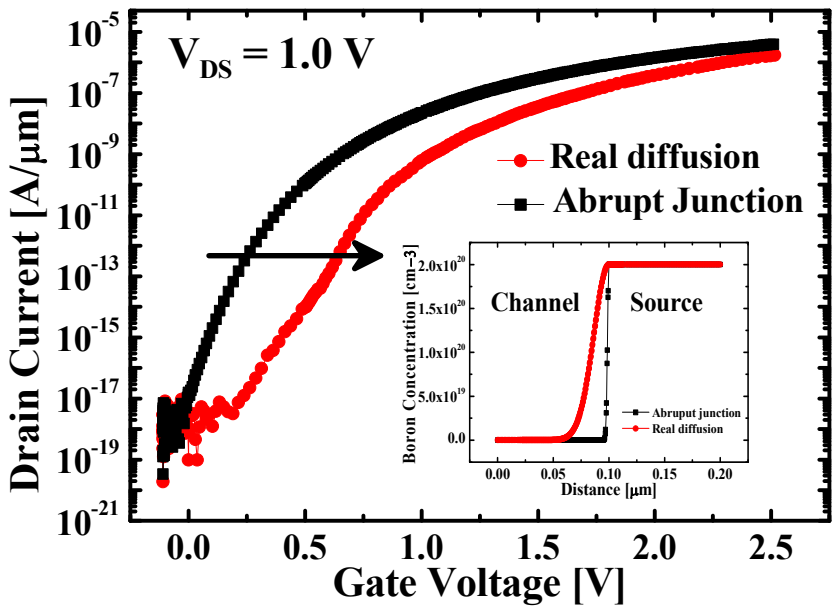
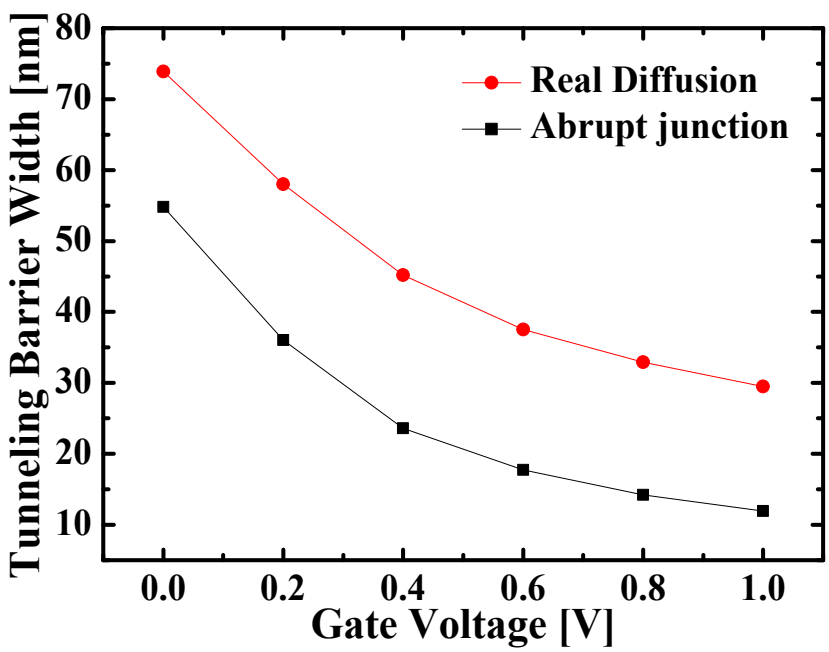


Fig. 4.14. Transfer characteristics with channel doping variation.

profile. For comparison, Figure 4.15(a) shows the electrical characteristics with changing junction profile. For comparison, abrupt junction and real process condition are considered at source doping of 2×10^{20} cm^{-3} and body doping of 1×10^{15} cm^{-3}. Real process condition is extracted by using process simultion results. As junction profile becomes gradually changed, tunneling resistance is increased. It leads to degradation of switching property such as SS and I_{ON}/I_{OFF} ratio. Figure 4.15(b) shows the tunneling barrier changes according to V_{GS}. As V_{GS} increases, tunneling barrier is generally reduced by channel band bending. However, it is observed that tunneling barriers with gradual doping profiles are much higher.



(a)



(b)

Fig. 4.15. (a)Switching property and (b) tunneling resistance as junction profile changes.

Chapter 5

Conclusions

In this dissertation, a new tunnel FET has been introduced with fin channel and elevated drain region. In order to increase the tunneling probabilities and reduce I_{AMB}, SiGe body and Si drain region are used. Also, by using SiGe channel and source, the proposed tunnel FET is expected to have excellent performance on both n- and p-channel operation.

For prediction of electrical characteristics, nonlocal BTBT model parameters though TCAD simulation are extracted with measurement results of fabricated planar Si and SiGe tunnel FET. Extracted A and B parameters of BTBT model in Si are 4×10^{14} $cm^{-1}\cdot s^{-1}$ and 9.9×10^{6} V/cm. Also, from SiGe tunnel FET's transfer characteristics, A and B parameters of Ge can be extracted as 3.1×10^{16} $cm^{-1}\cdot s^{-1}$ and 7.1×10^{5} V/cm, respectively. Then, it is found that the proposed tunnel FET has a smaller SS value and larger I_{ON} than that of the control group. Also, as channel length is decreased, the proposed tunnel FET has a strong immunity to SCEs due to the long effective gate length. For logic application, transient response characteristics are examined in terms of

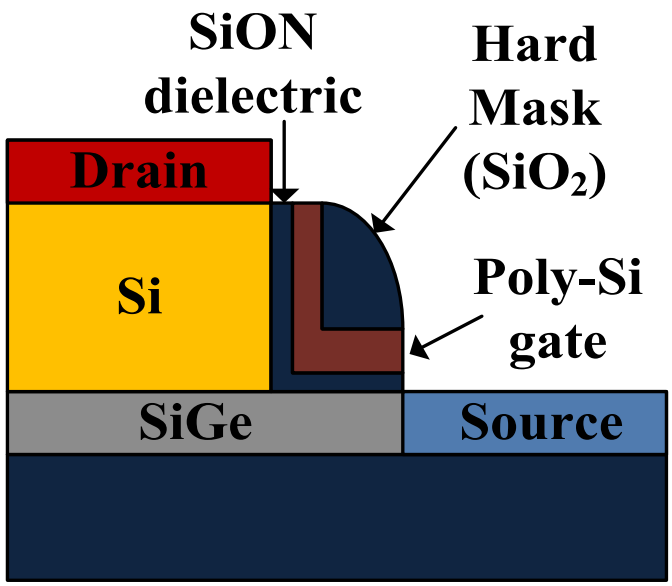
inverter switching. The proposed device shows pull-up/pull-down property. However, it is observed that control group can't show pull-up/pull-down due to low I_{ON}. For device delay, drain width of the proposed device affects gate-to-drain capacitance. Thus, small drain width is needed to obtain small delay time.

For device fabrication of the proposed tunnel FET, 30 nm SiGe and 150 nm Si are grown on SOI wafer using epitaxial growth process. Also, EOT of 3 nm and gate length of 76 nm are applied by using oxidation and spacer technique.

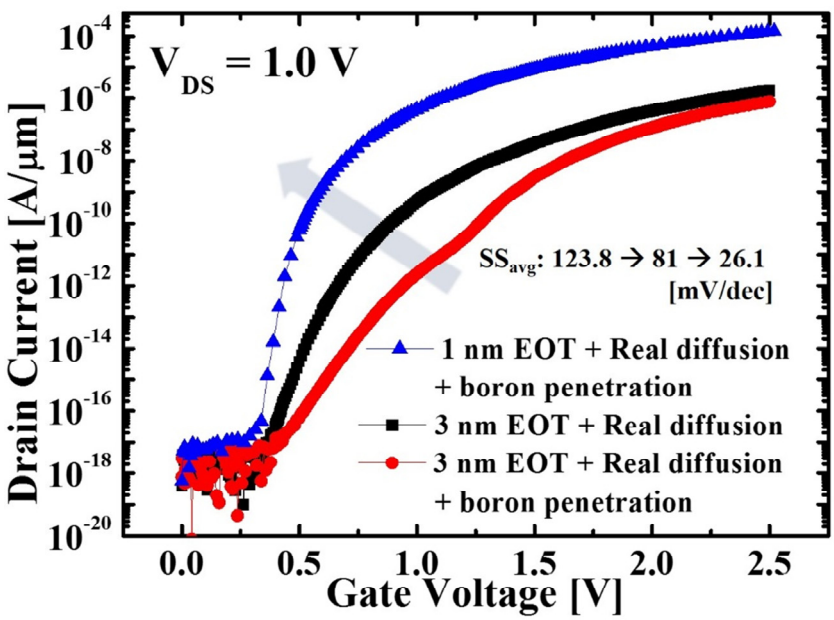
From electrical characteristics of fabricated proposed devices, minimum SS of 87 mV/dec is extracted for n-type device. In case of p-type device, minimum SS is 51.1 mV/dec. Current saturation of proposed p-type device is faster than that of n-type device because of dopant diffusion difference. In terms of comparison between experimental and control groups, I_{ON} of n-type proposed device is 10 times more than that of Si control group. Compared with planar SiGe device, it is increased by more than 4 times. In terms of I_{AMB}, it can reduce to more than 100 times. It is because the fin channel and elevated Si drain region are sued for high gate controllability and tunneling current reduction between channel and drain. For p-type tunnel FETs, I_{ON} of the proposed device is larger than 12 times that of the Si control group. Also, it is found that I_{AMB} is suppressed to 1/10 of that of the control group.

For further improved characteristics, EOT of sub-2nm is essential to enhance tunneling current. Thus, high-κ/metal gate stacks can apply to obtain lower SS and large drive current than fabricated tunnel FET as shown in Fig. 5.1(a). Figure 5.1(b) shows

the transfer characteristics of the proposed tunnel FET with EOT of 1 nm. Although the proposed device with EOT of 1 nm has high channel doping and gradual doping profile, SS and I_{ON} properties are extremely improved by high gate controllability.



(a)



(b)

Fig. 5.1. (a) Solution and (b) transfer characteristics for improved n-type proposed tunnel FET.

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초록

고집적 상보형 전계효과 트랜지스터 (CMOS) 기술로 만들어진 집적회로에서의 전력소비는 중대한 문제로 인식되고 있다. 왜냐하면 칩당 요구되는 전력과 누설전력들이 계속해서 증가하고 있기 때문이다. 이러한 전력문제를 해결하기 위해서는 공급전압을 줄이는 것이 필수적이고 누설전류가 작은 소자들이 사용되어야 한다. 최근, 많은 연구자들은 저전력 동작에 적합한 터널링 전계효과 트랜지스터 (tunnel field-effect transistor, tunnel FET)를 연구해 오고 있다. Tunnel FET은 터널링을 이용한 반송자 주입방식을 사용하여 누설전류가 매우 작고, 낮은 subthreshold swing (SS) 값을 가진다.

이 논문에서는 실리콘저머늄 바디와 들려진 (elevated) 실리콘 드레인 영역을 가지는 새로운 tunnel FET 구조를 제안하였다. 제안된 소자는 낮은 터널링 저항을 위해 실리콘저머늄 물질을 사용하여 기존의 실리콘 tunnel FET보다 훨씬 큰 전류 구동성을 가진다. 또한 실리콘저머늄 소스와 채널을 가지므로 n채널뿐만 아니라, p채널 동작에 대해서도 전기적인 특성이 향상될 것을 기대한다. 게다가 들려진 실리콘 드레인 영역으로 인해 채널과 드레인 사이의 터널링으로 인한 양방향 전류 (ambipolar current)도 줄어들 수 있다.

실리콘저머늄 채널을 지닌 tunnel FET의 기본적인 특성을 얻기 위해, 평면 구조의 tunnel FET 소자를 우선 제작하고 분석하였다. 제작된 소자의 전기적인 특성으로부터 n형과 p형 실리콘저머늄 tunnel FET은 대조군인

실리콘 tunnel FET보다 훨씬 좋은 특성을 보였으며, 구동전류는 10배 이상 증가하였다. 또한 전류포화도 대조군보다 훨씬 빨랐다. 그리고 만들어진 소자로부터 TCAD 시뮬레이션을 이용하여 밴드간 터널링 모델 파라미터들을 추출하였다. 실리콘 물질의 경우 추출된 A 파라메터는 4×10^{14} $cm^{-1}s^{-1}$이고, B는 9.9×10^{6} V/cm이다. 저머늄 물질은 A와 B가 각각 3.1×10^{16} $cm^{-1}s^{-1}$와 7.1×10^{5} V/cm로 얻어졌다.

보정된 모델 파라미터를 이용한 TCAD 시뮬레이션으로부터 제안된 소자의 전기적인 특성을 분석하였다. 실리콘저머늄 내의 저머늄 함량에 따른 영향, 들려진 실리콘 드레인 영역효과, 짧은 채널효과, 인버터 동작, 소자의 지연(delay)들에 대한 특성을 살펴보고 소자를 최적화하였다. 이를 바탕으로 제안된 소자는 자기정렬 도핑 공정이 가능한 스페이서 기술 (spacer technique)을 이용하여 제작하였다. 제작에 필요한 주요 공정은 실리콘과 실리콘저머늄을 위한 단결정 성장, 미세 액티브를 위한 사진공정, 그리고 스페이서 게이트 형성들이 있다.

제작된 제안소자는 n채널과 p채널에서 모두 대조군보다 뛰어난 전기적인 특성을 보였다. P형 소자의 경우, 최소 SS는 51.1 mV/V였으며, n형 소자는 87 mV/dec가 나왔다. 양방향 전류의 경우, 제안된 소자가 실리콘저머늄 평면구조의 소자보다 100 배 이상 낮게 나왔다. 또한 tunnel FET의 전류를 분석하기 위해 온도에 따른 전달특성곡선을 관측하였다. 온도가 증가할수록, Shockley-Read-Hall 과 field-dependent 결합이 증가하여 소자의 특성을 열화시켰다. 전류 포화영역에서는 낮은 온도민감성을 지니는

밴드간 터널링이 지배적이므로 온도에 따른 특성변화가 없었다.

이 연구로부터 실리콘저머늄 바디와 들려진 실리콘 드레인 영역을 가지는 새로운 tunnel FET 구조를 검증하였다. 제안된 소자는 구조의 변화없이 n형과 p형 동작에서 기존 소자와 비교하여 향상된 전기적 성능을 보였다. 이는 tunnel FET 소자들을 이용한 집적회로를 구현하는데 있어 엄청난 장점이며, 차세대 tunnel FET 소자들 가운데 유력한 소자가 될 것이다.

주요어:밴드간터널링, 터널링전계효과트랜지스터, 저전력소자, 터널링 저항, 문턱전압이하기울기, 양방향 전류.

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