Ph.D. DISSERTATION

A STUDY ON MULTIBAND RECONFIGURABLE LINEAR CMOS POWER AMPLIFIER FOR MOBILE APPLICATIONS

이동통신 기기에 적합한 재구성이 가능한 다중대역 선형 CMOS 전력증폭기에 관한 연구

BY

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COMPUTER SCIENCE COLLEGE OF ENGINEERING
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Abstract

In this Dissertation, a study on multiband reconfigurable linear CMOS power amplifier (PA) is performed. Since a larger number of frequency bands is allocated for 3G/4G mobile communication standards nowadays, handset PAs are required to support the ever-increasing number of frequency bands. With the advent of high-speed wireless data transmission, handset PAs are also demanded to perform linear power amplification under the wide-band signal condition. Even though the CMOS technology has cost and size benefits, however, designing a watt-level linear CMOS PA is a challenging issue due to low breakdown voltage and nonlinear nature of the CMOS device.

To resolve the issues above, this study presents two methods suitable for multiband (MB) linear CMOS PA: a reconfigurable MB matching structure and a linearization technique. The proposed MB structure shares a PA core to reduce the cost and size, and contains the power- and frequency-reconfigurable matching networks as well as the output path-selection function. Thus, it can perform the MB operation requiring multiple frequency bands and target output powers. The reconfiguration mechanism is quantitatively analyzed and experimentally demonstrated. The fabricated tri-band reconfigurable 3G UMTS PA using an InGaP/GaAs heterojunction bipolar transistor (HBT) process for practical handset application showed minimal efficiency degradation of less than 2% by multi-banding, compared with a single-band reference PA.

For linearization of a CMOS PA, a phase-based linearization technique is presented. Since the PA nonlinearity is determined by the dynamic AM-AM and AM-PM, the two distortions should simultaneously be considered in linearization. Contrary to the previous works which have focused on the correction of AM-AM distortion by providing an envelope-dependent gate-bias, this work proposes an

AM-PM linearizer using a varactor and an envelope-reshaping circuit. This linearizer helps the PA recover AM-AM distortion as well. To validate the usefulness of the proposed linearizer, 1.88 GHz and 0.9 GHz stacked-FET PAs using a 0.32-μm silicon-on-insulator (SOI) CMOS process were designed and fabricated. Measurement results showed that the fabricated 1.88 / 0.9 GHz linear CMOS PAs achieved linear efficiencies (meeting –39 dBc W-CDMA ACLR) of higher than 44 / 49%. Furthermore, a single-chain MB linear CMOS PA was implemented based on the proposed MB reconfiguration and linearization techniques. The fabricated MB PA, which has two outputs and covers five popular uplink UMTS/LTE bands (Band 1/2/4/5/8: 824 ~ 1980 MHz), showed minimal efficiency degradation (< 3.3%) compared to the single-band dedicated CMOS PA with W-CDMA efficiencies in excess of 40.7%.

Finally, the signal-bandwidth limiting effect of the envelope-based linear CMOS PA is discussed and a solution is proposed. Due to the time delay during envelope-detection and shaping, a timing mismatch between the incoming RF signal and envelope-reshaped signal occurs, thus resulting in no linearization effect under wide-band signal (LTE 20 MHz or more) conditions. To resolve the problem, a group delay circuit with a compact size is employed and thus the linearization effect of the proposed phase-based linearizer is maintained up to 40 MHz LTE bandwidth.

Keywords: CMOS, linearization, LTE, multiband, power amplifier (PA), reconfigurable, silicon-on-insulator (SOI), stacked-FET, W-CDMA.

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Chapter 1

Introduction

1.1 Motivation

Since the first-generation (1G) analog cellular telecommunication system (advanced mobile phone system: AMPS) was developed in early 1980s [1], the mobile communication standard has significantly been evolved. In initial evolution stages such as the 1G AMPS and second-generation (2G) code-division multiple access (CDMA) [2] / global system for mobile communication (GSM) [3] deployed before early 2000s, the technology and service provider had been focused on providing a reliable voice communication. As the semiconductor technology and the demand for wireless internet service have been evolved and increased, the mobile standards have pursued to achieve high-speed data-centric communication. For the purpose, the signal bandwidth and modulation scheme have been increased and more complex in the third-generation (3G) wideband code-division multiple access (W-CDMA) [4] and fourth-generation (4G) long term evolution (LTE) [5].

To achieve high transmit data-rate in mobile terminals, RF power amplifiers (PAs) play a key role, since the signal quality of a transmitter is determined by the

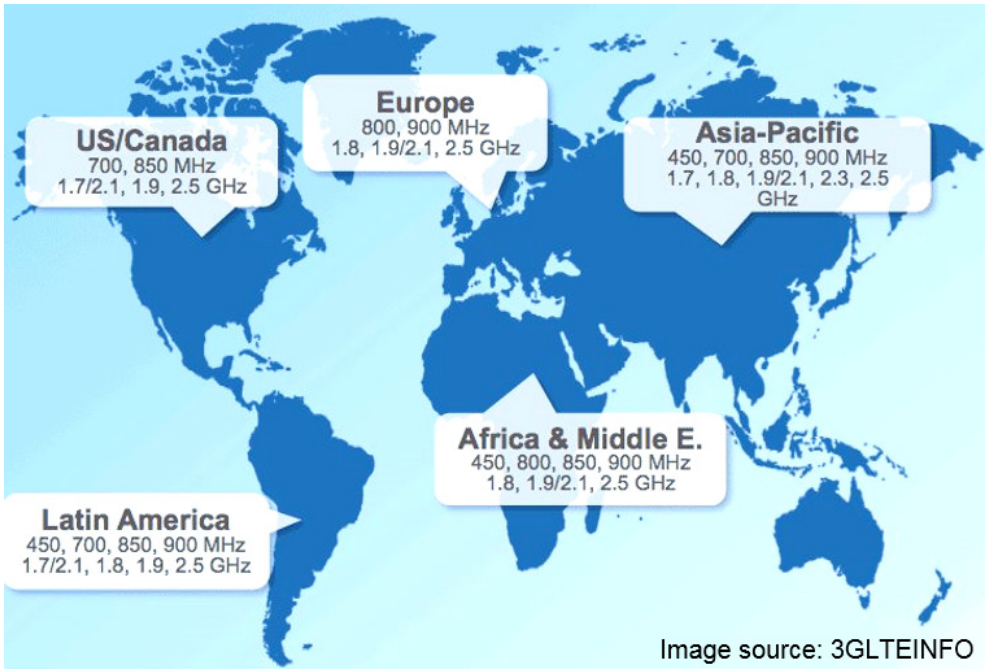

Figure 1.1: 3G/4G frequency band allocations by region.

PA characteristics. As a mobile communication standard is getting evolved from the 3G universal mobile telecommunications system (UMTS) to the 4G LTE, the modulation scheme and bandwidth of a signal become more complex and wider. For example, the uplink 4G LTE signal employs the 10 ~ 20 MHz bandwidth 16/64-quadrature-amplitude-modulation (16/64-QAM) scheme, whereas the 3G W-CDMA uses the 3.84 MHz bandwidth hybrid phase-shift-keying (HPSK) scheme which is rather similar to the quadrature PSK (QPSK) of 2G CDMA. As a result, the LTE signal has higher peak-to-average power ratio (PAPR) and requires higher linearity to reduce bit-error-rate (BER) during demodulation. Due to the reason, the operating output power level of a 4G LTE PA should be backed-off to maintain the stringent linearity requirement, which further reduces the efficiency [6].

The proliferation of worldwide 3G/4G frequency bands demands handset PAs to support multiple frequency bands for global roaming [7]. Fig. 1.1 shows the

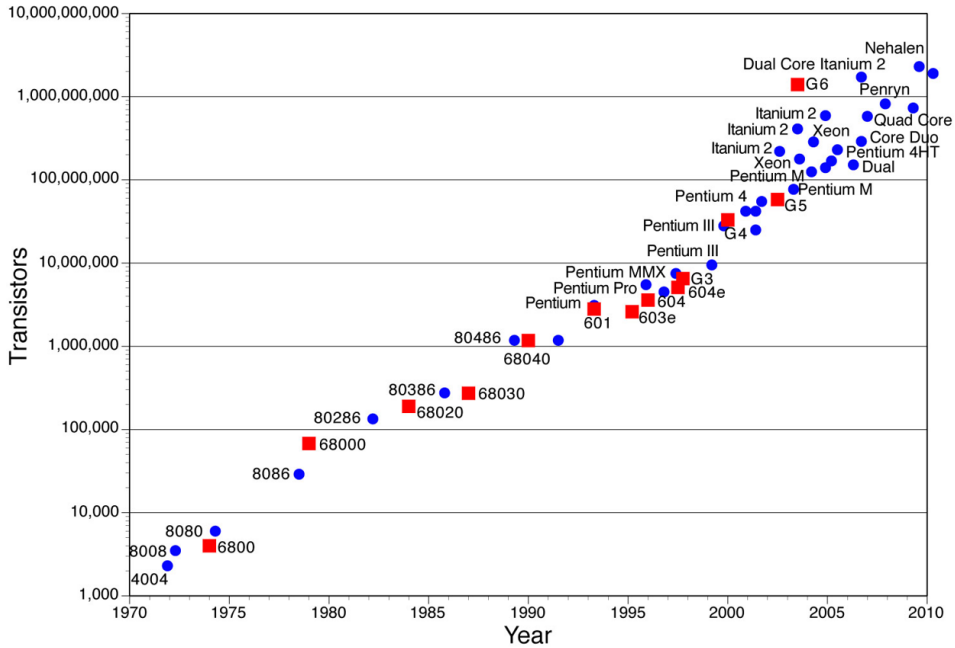

Figure 1.2: Moore's law.

3G/4G frequency band allocations by region. Even though the 3G UMTS standard initially aimed to unite the wide-spread frequency bands into a single-band (UMTS Band-1), in reality, it is impossible for each country to completely reallocate the occupied frequency bands (called as "frequency re-farming"), because the service providers must pay additional/excessive cost to replace the previous systems with new one. In terms of phone makers and users, the size of recent smartphones is getting smaller and thinner whereas more functions (such as internet, camera, video, navigation, fingerprint recognition, and so on) are included. Due to the reason, phone makers have demanded PA manufacturers to develop a multiband (MB) PA which fulfills multiband coverage while maintaining low cost and small size, which makes a challenge in designing MB PAs.

In terms of process technology, there have been remarkable improvement on transistor scaling and integration in CMOS coinciding Moore's law, as shown in Fig. 1.2 [8]. As the CMOS device is scaled down to nanometer, the operating speed

of a transistor gets further increased and it can thus be employed for the millimeter-wave circuit as well as the RF circuit. However, down-scaling of CMOS device gives rise to low voltage operation, thus limiting its application within small-signal circuits. Also, nonlinear nature of CMOS device makes the design of a watt-level linear PA very challenging, in particular, for applications using high-level modulation scheme. Due to the reason, there have been continuous studies to realize a highly linear and efficient watt-level PA using CMOS process to take advantage of its cost and size benefits. Even though many researchers have also tried to implement the single-chip integration of a radio transceiver in CMOS, it is almost impossible due to the fact that the signal leakage and noise from the PA directly affects the receive-band sensitivity. Thus, implementing CMOS PAs in a separate IC die is a desirable approach. Even though several linearization techniques of CMOS PA have been introduced, however, the overall linearity and efficiency cannot match those of GaAs heterojunction bipolar transistor (HBT) PAs.

Based on the motivations above, in this study, multi-banding and linearization of CMOS PA are performed to implement a MB reconfigurable linear CMOS PA for 3G/4G mobile applications.

1.2 Multiband PA Structure

To implement a MB PA, several multi-banding structures have been proposed as shown in Fig. 1.3. In initial development stage, multi-banding of a PA was achieved by simply consolidating single-band dedicated PAs into a single PA-module, as shown in Fig. 1.3(a). However, this approach cannot obtain the size and cost benefits. Thus, recent researches have focused on “converged-PA” design. The converged PA employs reduced number of PA-cores and MB matching networks such as the broadband and/or reconfigurable matching networks to reduce the size and cost [7], [9]. Contrary to the broadband matching method shown in Fig. 1.3(b),

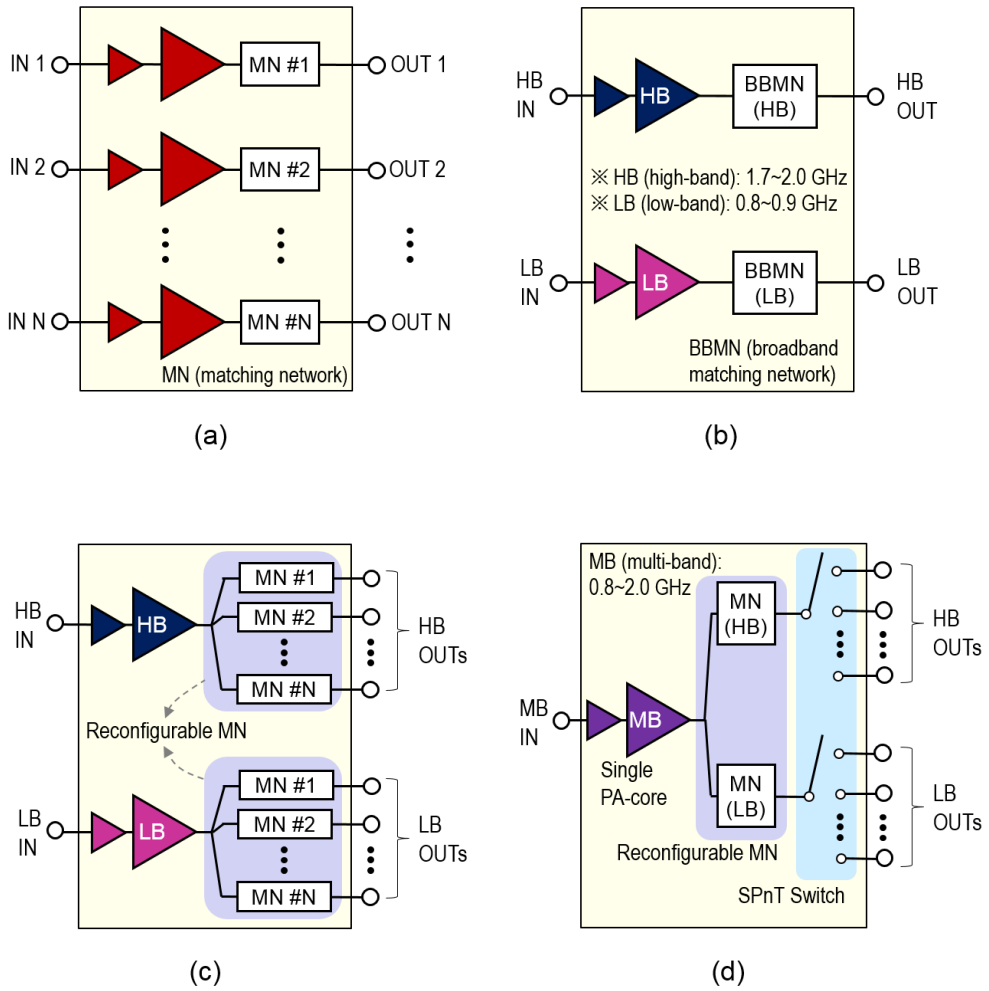

Figure 1.3: Multiband (MB) PA module topologies. (a) Classical MB PA module consisting of single-band dedicated PAs. (b) Converged PA using the broadband matching networks (MNs). (c) Converged PA using the reconfigurable MNs. (d) Converged PA using a single PA-core and reconfigurable MNs.

the reconfigurable matching technique shown in Fig. 1.3(c) can adaptively reconfigure the target output powers as well as the target frequencies by employing tunable passive elements such as the voltage-controlled capacitors (varactors) and RF switches, thus achieving higher performance at each target band. To avoid excessive complexity and power loss in covering too wide bandwidth, the two

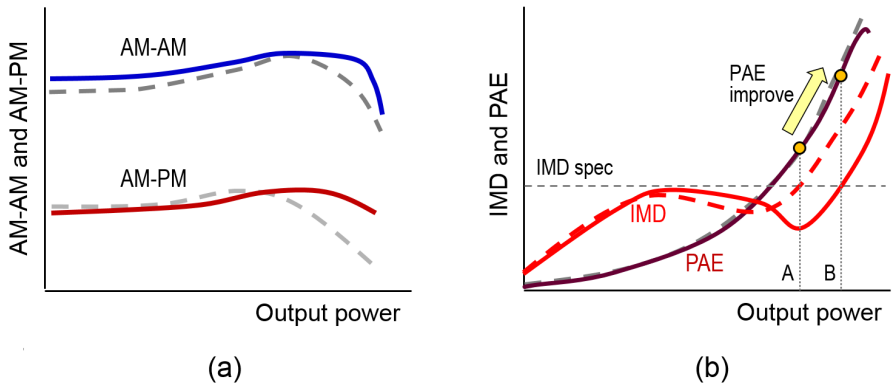

Figure 1.4: Linearization of CMOS PA (line/dash: with/without linearization). (a) AM-AM and AM-PM. (b) Linearity (IMD) and PAE.

structures in Fig. 1.3(b) and (c) employ two PA cores, each aiming for high-band (1.7 ~ 2.0 GHz) and low-band (0.8 ~ 0.9 GHz) UMTS/LTE frequency groups. To further reduce the IC die, a single PA-core approach can also be considered as shown in Fig. 1.3(d). However, the reconfigurations should also be applied to the interstage matching as well as the output matching. Also, high performance tunable elements are required to avoid excessive performance degradation.

1.3 Linearization of CMOS PA

To overcome the low breakdown voltage and nonlinear nature of CMOS device for handset PA applications, several power combining and linearization techniques have been researched. Since Aoki *et al* [10] and Pornpromlikit *et al* [11] successfully demonstrated the performances of transformer-based and stacked-FET-based PA structures, watt-level power amplification of a CMOS PA does not become a challenging issue. Even though several reported works on linearization showed some improvement on linearity [12], [13], however, their linear efficiency are still not comparable to that of the GaAs HBT PA [14]. Thus, linearization of CMOS PA is still an important research topic. Fig. 1.4 illustrates the linearization

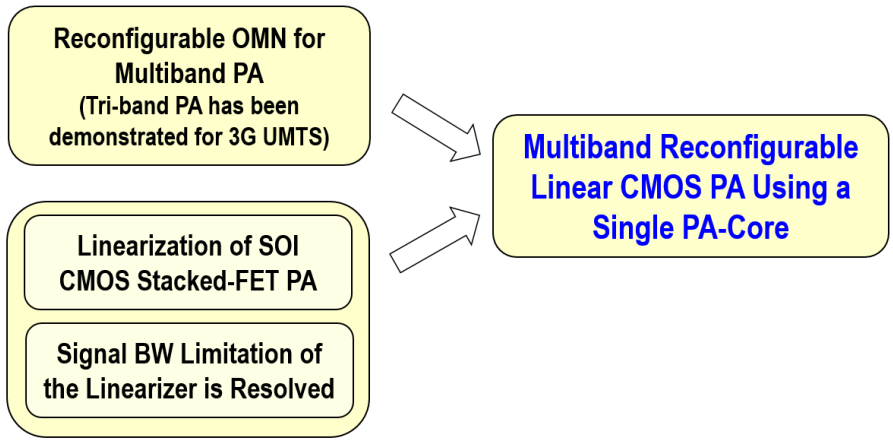

Figure 1.5: Scope of this study.

process of a CMOS PA. Since the AM-AM and AM-PM of a standalone CMOS PA show early compression behavior, the maximum linear output power meeting the intermodulation distortion (IMD) spec stays in "A" point in Fig. 1.4(b). If an effective linearization is applied to the PA, the AM-AM and AM-PM are flattened as shown in Fig. 1.4(a), and thus the linear output power is extended to "B" point. As a result, the maximum linear power-added efficiency (PAE) is improved compared to the result without linearization, as shown in Fig 1.4(b).

1.4 Dissertation Organization

In this dissertation, a methodology to realize a MB reconfigurable linear CMOS PA is presented for 3G/4G mobile applications. Fig. 1.5 illustrates the scope of this study. The contents of this study are sub-divided into three topics. In Chapter 2, a reconfigurable matching structure is presented to implement the MB function of a PA. The proposed reconfigurable matching networks are quantitatively analyzed and their usefulness is experimentally demonstrated.

In Chapter 3, a linearization technique to improve the linear efficiency of a

CMOS PA is presented. The proposed envelope-dependent phase-based linearizer corrects not only for the AM-PM but also for the AM-AM distortion. Thus, the fabricated silicon-on-insulator (SOI) CMOS stacked-FET linear PA shows very high linear efficiency. Moreover, the concept of the single-band linear CMOS PA is extended to a MB linear CMOS PA by employing the reconfigurable networks described in Chapter 2. Together with the high performance SOI technology and linearization method, the implemented MB CMOS PA covers five popular 3G/4G frequency bands (Band 1/2/4/5/8: 0.82 ~ 1.98 GHz) using a single-PA core.

In Chapter 4, the limiting effect of the linearizer under the wideband signal is discussed and a solution is presented. The limitation comes from the time delay of the linearizer during envelope-detection and injection. By employing a group delay circuit with compact size, the linearizer shows its usefulness under wideband signals (e.g. LTE 40 MHz bandwidth). Finally, Chapter 5 concludes this study.

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Chapter 2

A Multiband Reconfigurable Power Amplifier for 3G UMTS Handset Applications

2.1 Introduction

Since a larger number of frequency bands is allocated for third-generation (3G) universal mobile telecommunications system (UMTS) communication standards, wideband code-division multiple access (W-CDMA) handsets are required to support the ever increasing number of frequency bands. The conventional multiband power amplifier (PA) design approach, where a dedicated single-band PA is added for each additional frequency band, would result in excessive cost and board space for the mobile phones [1]. To solve this issue, researchers have recently started to develop reconfigurable PAs that cover several frequency bands using a single PA core [2]-[15]. Programmable matching networks using varactors as well as semiconductor and MEMS switches have been employed to reduce the number of PAs for multiband operation. However, attempts

to cover too wide a frequency range using a single PA core results in significant efficiency degradation and increased module size due to complicated matching networks. For example, the net additional loss of the reconfigurable matching network using MEMS switches in [4] can be as large as 0.96 dB at 1.6 GHz, which translates to approximately 6.5% power-added-efficiency (PAE) degradation. Excessive PAE degradation cannot be easily accepted for data-centric mobile terminals due to the thermal concerns and talk time metric. In addition, the large circuit size and high actuation voltage requirement using MEMS components makes their application to commercial handsets practically difficult.

Switches for the reconfigurable matching circuit can be avoided if multi-section matching networks are used to make the PA broadband [12]-[14]. However, the efficiency of the PA is degraded due to the sub-optimal impedance trajectory across the operating frequency band in addition to the increased loss of the matching network. Moreover, the approach of using a single RF input and output port for broadband amplifier design will lead to further PAE degradation due to the requirement of post-PA distribution switches, whose loss further degrades the overall efficiency [2], [3], [5]-[13].

A new approach for multiband UMTS reconfigurable PA for practical handset applications was introduced in our previous work [15], showing a small PAE degradation of 2 ~ 3% compared with the single-band designs. The UMTS transmit frequency bands were grouped into low-band (0.7 ~ 0.9 GHz) and high-band (1.4 ~ 2.5 GHz). The complication in covering too wide frequency range is mitigated in this approach by limiting the band reconfigurability within either low- or high-band group. The additional losses due to post-PA switches are also avoided by expanding the number of output ports in the PA design. Moreover, the proposed network does not only reconfigure frequency band, but also linear output power according to the selected band. This allows the PA to operate at optimum power

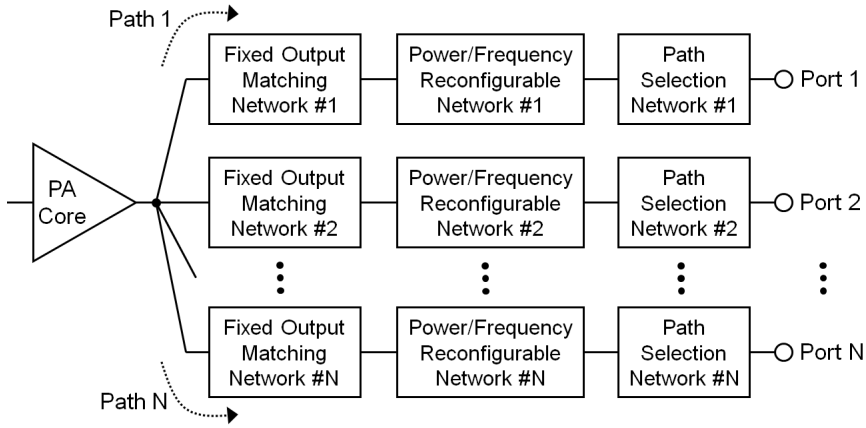


Figure 2.1: Block diagram of the proposed reconfigurable PA.

and efficiency in the system, by avoiding different power requirements due to different post-PA duplexer losses. In this work, the reconfigurable PA performance has been further optimized to limit PAE degradation to 2%. Also, included in this expanded study are the details of the systematic design methodology for power and frequency reconfigurable network together with closed-form design equations.

2.2 Operation Principle of the Reconfigurable Output Matching Network

The block diagram of the proposed reconfigurable PA is shown in Fig. 2.1. The PA has multiple outputs and each output has its "natural" frequency band with a corresponding target linear output power. The load impedance at natural frequency band and output power is generated by the fixed output matching network (FOMN). FOMN is followed by power/frequency reconfigurable network (PFRN), which can reconfigure operating frequency and/or target output power by the frequency reconfigurable network (FRN) and/or power reconfigurable network (PRN), respectively. This allows each path to support up to two different frequency bands with two different linear powers. Because only one output path should be

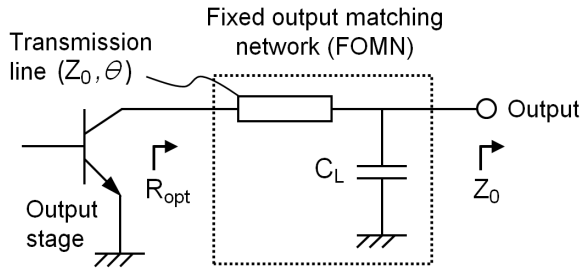


Figure 2.2: Schematic of the fixed output matching network (FOMN).

active at one time, the unused output paths are deactivated by the path-selection network (PSN). PFRN, PSN and FOMN are co-designed with each other to share the circuit components, which helps to reduce the overall circuit size and loss.

The FOMN of each path in Fig. 2.1 is designed to realize optimum load impedance at natural frequency band of its path, using a simple L-section matching network. It consists of a series transmission line (T/L) with an electrical length, θ, and a shunt capacitor, C_L, as shown in Fig. 2.2. If the optimum load impedance of the FOMN is assumed to be purely real ($Z_L = R_{opt}$) for simplification, which is a valid assumption for low-frequency handset PAs, the closed form formula for θ and C_L can easily be derived as

$$\theta = \tan^{-1}\left(\sqrt{\frac{R_{opt}}{Z_0}}\right) \tag{2.1}$$

$$C_L = \frac{Z_0 - R_{opt}}{\omega Z_0 \sqrt{Z_0 R_{opt}}} \tag{2.2}$$

where Z_0 is the characteristic impedance of the T/L and the output port impedance. The detailed design method of the PRN, FRN, and PSN is described in the subsequent sections.

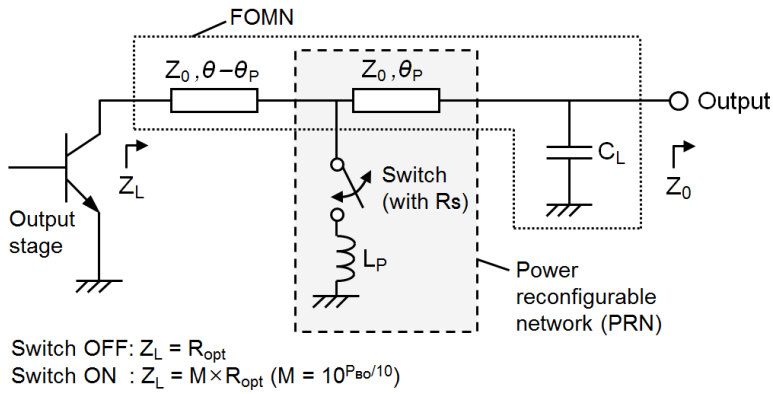


Figure 2.3: Schematic of the power reconfigurable network (PRN).

2.2.1 Power Reconfigurable Network (PRN)

Depending on the post-PA loss, the target linear output power of some bands is lower than the others. To maximize the efficiency at backed-off power level, the optimum load impedance should be increased [16]-[19]. This function is provided by the PRN. Fig. 2.3 shows a schematic of the proposed PRN along with FOMN. The power reconfiguration mechanism is carried out by placing a shunt arm of a switch and an inductor (L_P) in the middle of a T/L of the FOMN at an electrical length, θ_P. When the output network is not reconfigured with a shunt switch off ("as is" state), the FOMN provides the optimum load impedance ($Z_L = R_{opt}$) at the natural frequency band. If the output network is reconfigured ("switch on" state), the load impedance is increased according to the backed-off power. If a power back-off of P_{BO}-dB is required, the load impedance (Z_L) should be changed to $M \times R_{opt}$, where $M = 10^{P_{BO}/10}$. This is achieved by adding a compensation trajectory in the Smith chart, as shown in Fig. 2.4. As the compensation trajectory requires a constant g-circle and then a constant Γ-circle, it can be realized by a shunt inductor, L_P, and a T/L with an electrical length of $\theta - \theta_P$. Using T/L circuit theory, the two design parameters, θ_P and L_P, can be derived as

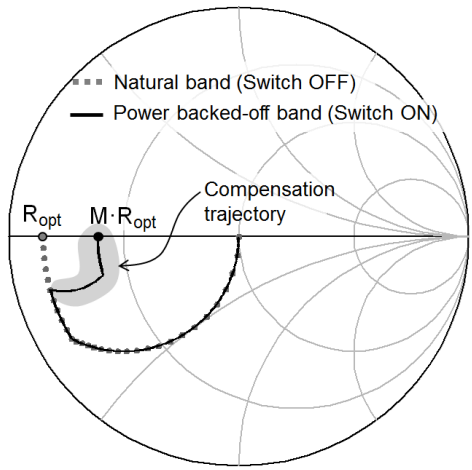


Figure 2.4: Load impedance (Z_L) trajectory of the PRN.

$$\theta_P = \tan^{-1}\left(\frac{\left(Z_0^2 + MR_{opt}^2\right) - \left(Z_0 + R_{opt}\right)\sqrt{MR_{opt}Z_0}}{\left(Z_0^3 - MR_{opt}^3\right)\Big/\sqrt{Z_0 R_{opt}}} \right) \tag{2.3}$$

$$L_P = \frac{1}{\omega(B_2 - B_1)} \tag{2.4}$$

where

$$B_1 = \frac{1}{Z_0}\frac{\left(Z_0^2 - M^2 R_{opt}^2\right)\tan(\theta - \theta_P)}{M^2 R_{opt}^2 + Z_0^2 \tan^2(\theta - \theta_P)} \tag{2.5}$$

$$B_2 = \frac{1}{Z_0}\frac{\left(Z_0 - R_{opt}\right)\left\{\sqrt{Z_0 R_{opt}} - \left(Z_0 - R_{opt}\right)\tan\theta_P - \sqrt{Z_0 R_{opt}}\tan^2\theta_P\right\}}{\left(\sqrt{Z_0 R_{opt}} - \left(Z_0 - R_{opt}\right)\tan\theta_P\right)^2 + Z_0 R_{opt}\tan^2\theta_P} \tag{2.6}$$

Fig. 2.5 shows the calculated electrical line length (θ_P) and inductive reactance (ωL_P) as a function of backed-off power level (P_{BO}) for various optimum load impedances of the FOMN.

The effect of series-resistance (R_S) of the switch at on-state is not considered in this calculation. When the switch is not completely lossless ($R_S \neq 0$), the effect of R_S on the PA performance can be represented as the reconfiguration loss. Fig.

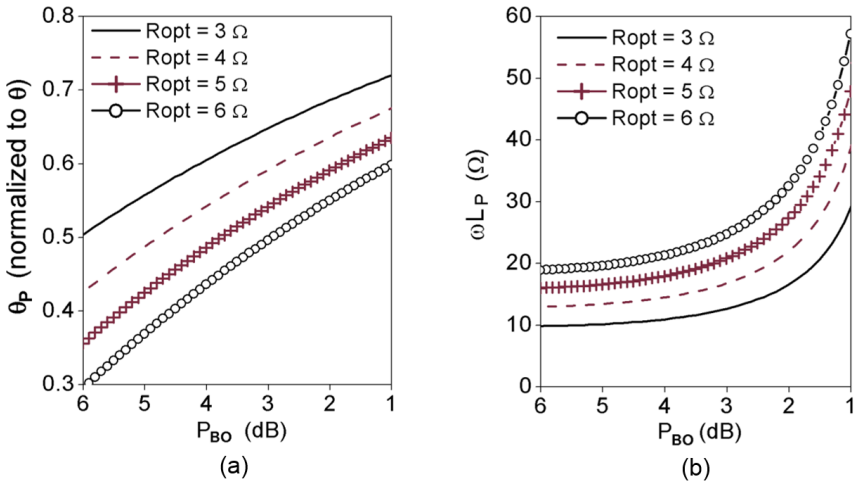


Figure 2.5: Required electrical line length and inductive reactance for power back-off operation. (a) θ_P (normalized to θ). (b) ωL_P.

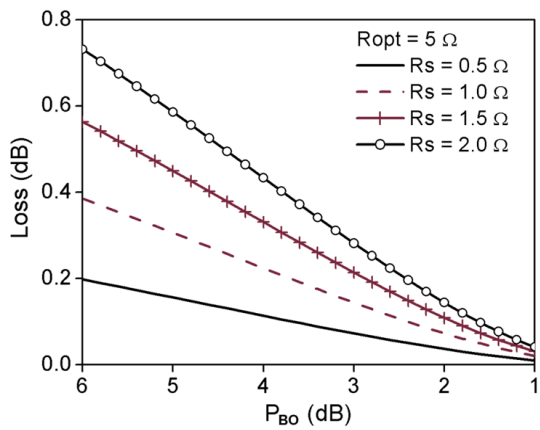


Figure 2.6: Reconfiguration loss of the PRN as a function of power back-off (P_{BO}) for various series-resistances (R_S) of the switch at on-state.

2.6 shows the calculated reconfiguration loss of the PRN as a function of P_{BO} for various R_S values. It is worthwhile to note from Fig. 2.6 that the reconfiguration loss is a strong function of R_S, especially when the power is backed-off. However, the R_S effect can be neglected when its value is far smaller than ωL_P.

On the other hand, the effect of parasitic capacitance of the switch in the off-state was ignored in this work due to the low frequency operation (< 2 GHz) and the small off-state capacitance (< 400 fF).

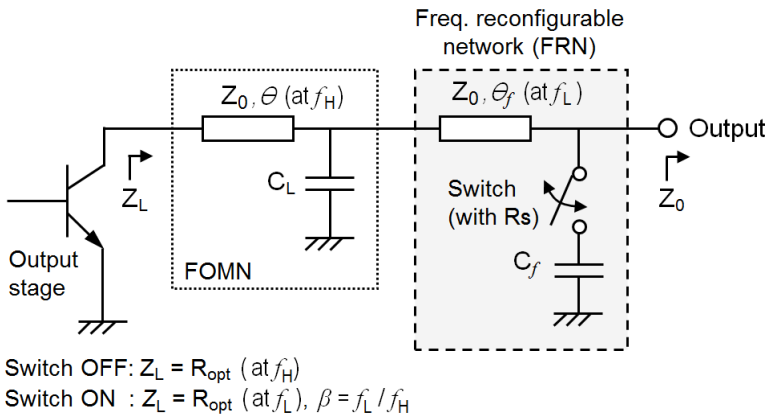


Figure 2.7: Schematic of the frequency reconfigurable network (FRN).

2.2.2 Frequency Reconfigurable Network (FRN)

If two frequency bands with the same target linear output power are required to share the output path, it can be realized by the FRN. This network consists of an additional T/L (θ_f) and a shunt arm consisting of a series combination of a switch and a capacitor (C_f). The FRN is placed at the end of the FOMN, as shown in Fig. 2.7. When the output network is not reconfigured ("as is" state), the impedance generated by the FOMN targets an optimum load impedance (R_{opt}) at a higher frequency (f_H). When reconfigured ("switch on" state), the FRN presents R_{opt} at a lower frequency (f_L) in conjunction with the FOMN. Fig. 2.8 shows the load-impedance trajectory describing how C_f and θ_f move load impedance (Z_L) toward R_{opt} at a lower frequency. Once the frequency scaling factor, $\beta = f_L / f_H$, is determined, the two design parameters, θ_f and C_f, can be derived as

$$\theta_f = \tan^{-1}\left(\frac{-b_3 + \sqrt{b_3^2 - \left(g_3^2 + b_3^2 - g_3\right)\left(1 - g_3\right)}}{g_3^2 + b_3^2 - g_3}\right) \tag{2.7}$$

$$C_f = \frac{1}{\omega_L Z_0}\frac{-b_3 \tan^2\theta_f + \left(g_3^2 + b_3^2 - 1\right)\tan\theta_f + b_3}{\left(1 + b_3 \tan\theta_f\right)^2 + \left(g_3 \tan\theta_f\right)^2} \tag{2.8}$$

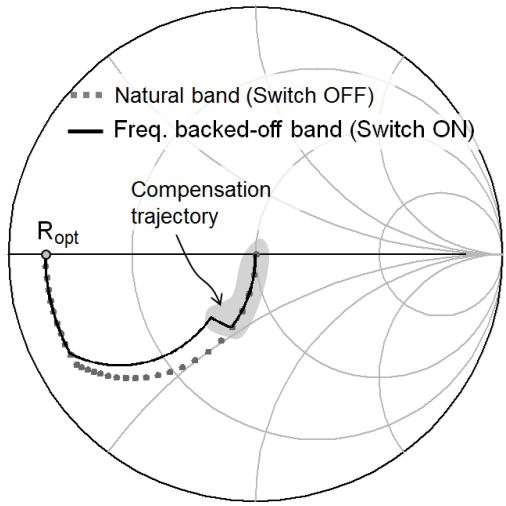


Figure 2.8: Load impedance (Z_L) trajectory of the FRN.

where

$$g_3 = \frac{Z_0 R_{opt}\left(1+\tan^2(\beta\theta)\right)}{R_{opt}^2 + Z_0^2\tan^2(\beta\theta)} \tag{2.9}$$

$$b_3 = \frac{\left(Z_0^2 - R_{opt}^2\right)\tan(\beta\theta)}{R_{opt}^2 + Z_0^2\tan^2(\beta\theta)} - \beta\frac{Z_0 - R_{opt}}{\sqrt{Z_0 R_{opt}}} \tag{2.10}$$

Fig. 2.9 shows the calculated electrical line length of the supplementary T/L (θ_f at f_L) and capacitive reactance ($1/\omega_L C_f$) as a function of frequency scaling factor (β) for various optimum impedances (R_{opt}).

For this calculation, the switch is also assumed to be lossless ($R_S = 0$). As in the case of the PRN, the on-state switch resistance (R_S) can affect the reconfiguration loss of the FRN. Fig. 2.10 shows the calculated reconfiguration loss of the FRN as a function of β for various R_S. It is clear from Fig. 2.10 that the loss becomes larger as the frequency difference ($1 - \beta$) is increased. When R_S is much smaller than $1/\omega_L C_f$, its effect can be neglected. As in the case of the PRN, the effect of parasitic capacitance of the switch in the off-state was ignored.

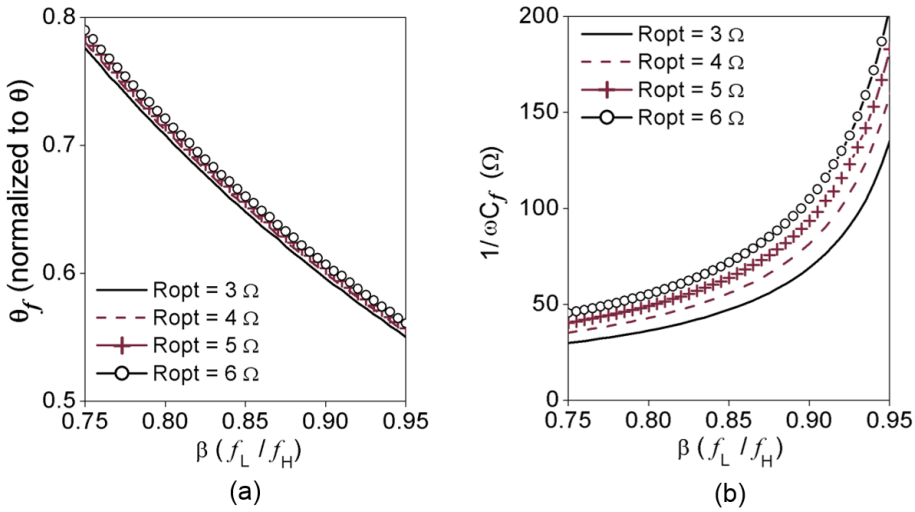


Figure 2.9: Required electrical line length and capacitive reactance for frequency back-off operation. (a) θ_f at f_L (normalized to θ at f_L). (b) $1/\omega_L C_f$.

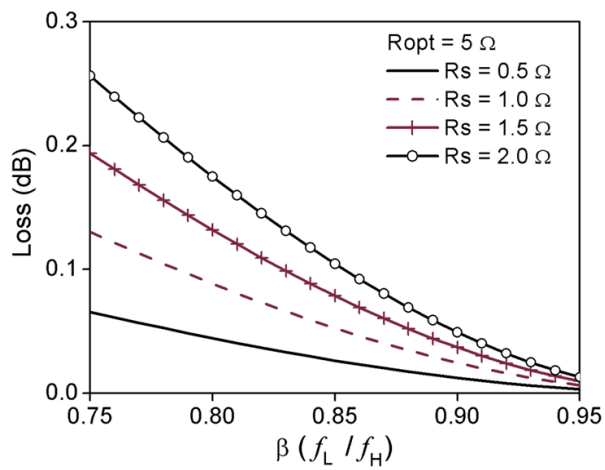


Figure 2.10: Reconfiguration loss of the FRN as a function of frequency scaling factor (β) for various series-resistances of the switch at on-state (R_S).

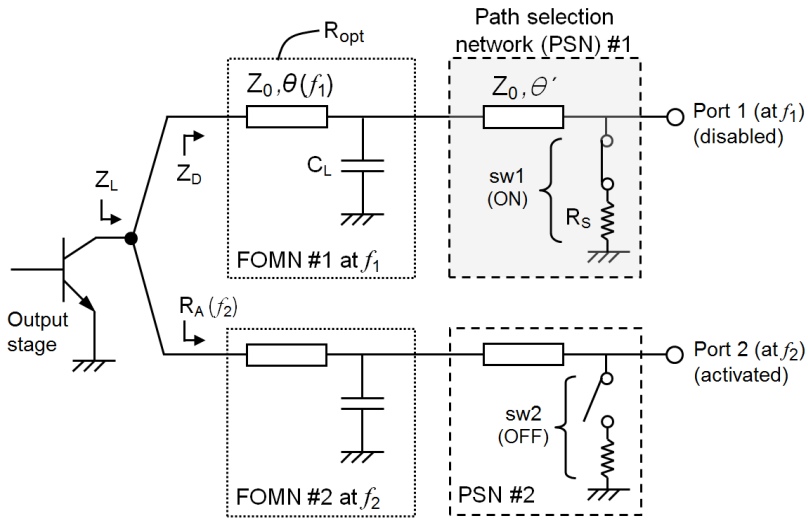


Figure 2.11: Schematic of the path-selection network (PSN) with two outputs.

2.2.3 Path Selection Network (PSN)

Since only one output path should be active at a time, the unused output paths should be deactivated. This is achieved by the PSN. The analysis of this network starts with the simple case of two output paths and is extended to multiple output paths later. Fig. 2.11 shows the schematic of the two-path output network, each consisting of a PSN and an FOMN with a unique frequency. The PSN consists of a T/L and a shunt switch. Compared to the series-type switch, the shunt-type switch can be co-designed with an FRN and a PRN, resulting in lower loss while meeting isolation requirements. The electrical length of the T/L (θ') is designed so that the unused path can represent a large impedance (Z_D) at the junction with the active path when the switch in the unused path is closed. By closing the shunt switch in path-1 (sw1) in Fig. 2.11, port-1 is disabled and thus port-2 becomes the active output path. To account for a general two-path case where both frequency and impedance can be different at each path, it is assumed that FOMN #1 presents R_{opt} at f_1, and FOMN #2 presents R_A at f_2. Also assumed is zero series-resistance of the switch at on-state ($R_S = 0$) for the initial design. Since the goal of the design is to minimize the impedance change in the active path by presenting a large reactive

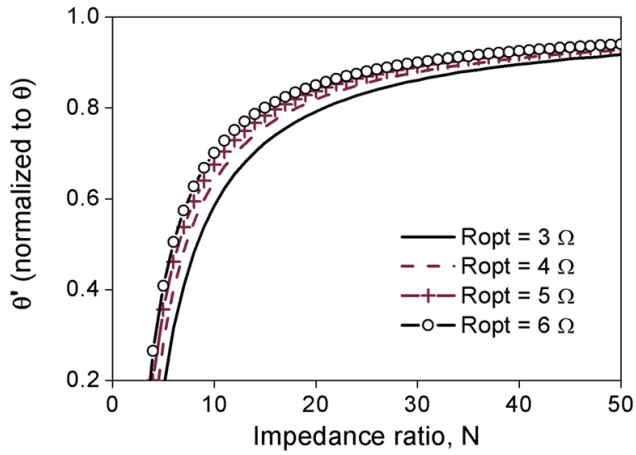


Figure 2.12: Required electrical line length (θ') of the PSN for the case of R_A = R_{opt} and $f_1 = f_2$.

impedance from the unused path (Z_D) at the junction, we have imposed the following condition:

$$Z_D\big|_{R_S=0} = jNR_A \tag{2.11}$$

where N is the impedance ratio ($N = |Z_D| / R_A$). Under this condition, the electrical length of the T/L (θ') is calculated as

$$\theta'\big|_{R_S=0} = \tan^{-1}\left(\left(\alpha\frac{Z_0 - R_{opt}}{\sqrt{Z_0 R_{opt}}} - \frac{Z_0 + NR_A\tan(\alpha\theta)}{Z_0\tan(\alpha\theta) - NR_A}\right)^{-1}\right) \tag{2.12}$$

where $\alpha = f_2 / f_1$. To simplify (2.12), if the two output paths are assumed to have the same operating frequency and load impedance (α = 1 and $R_A = R_{opt}$), θ' is derived as

$$\theta'\big|_{R_S=0,\alpha=1,R_A=R_{opt}} = \tan^{-1}\left(\frac{N\sqrt{R_{opt}} - \sqrt{Z_0}}{N\sqrt{Z_0} + \sqrt{R_{opt}}}\right). \tag{2.13}$$

Fig 2.12 shows the calculated θ' under various R_{opt} as a function of required impedance ratio (N). Not to affect the impedance of the active path ($Z_L = jNR_A \parallel R_A$

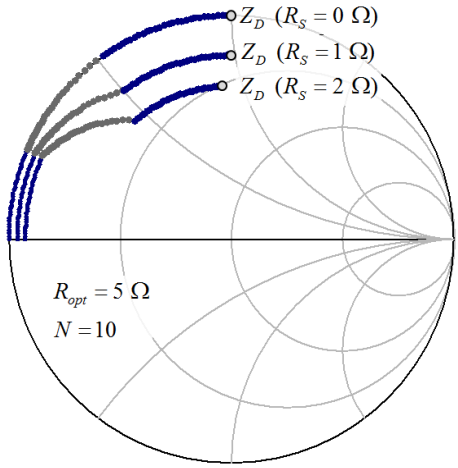


Figure 2.13: Off-impedance (Z_D) trajectory of the PSN.

≈ R_A), θ' should be chosen to provide N of at least 10 ~ 15. Also, N requirement should be larger as the number of output paths is increased. It is worthwhile to note that the capacitor-loaded lines help to reduce the physical line lengths ($\theta + \theta$') well below the quarter-wavelength as shown in (2.1) and (2.12).

When the switch is not completely lossless ($R_S \neq 0$), there is finite signal leakage into the unused path, which degrades the overall PAE and degrades the isolation between the paths, which may also affect the receive (Rx) band sensitivity in some cases [20]. We have repeated the analysis considering the effect of the finite series-resistance of the switches (R_S). Z_D in (2.11) is then calculated to be

$$Z_D\big|_{\alpha=1, R_A=R_{opt}} = R_{opt}\frac{R_{S1} + jNZ_0}{Z_0 + jNR_{S1}} \tag{2.14}$$

where $R_{S1} = R_S \,||\, Z_0$. Fig. 2.13 shows Z_D trajectories in the Smith chart under various R_S. As the value of R_S is increased, Z_D becomes lossy, resulting in power leakage into the unused path. If the number of outputs is k and the conditions of α = 1 and $R_A = R_{opt}$ are assumed, the output power at each path can be illustrated as shown in Fig. 2.14. The power loss (PL) and the port-port isolation (ISO) are calculated as

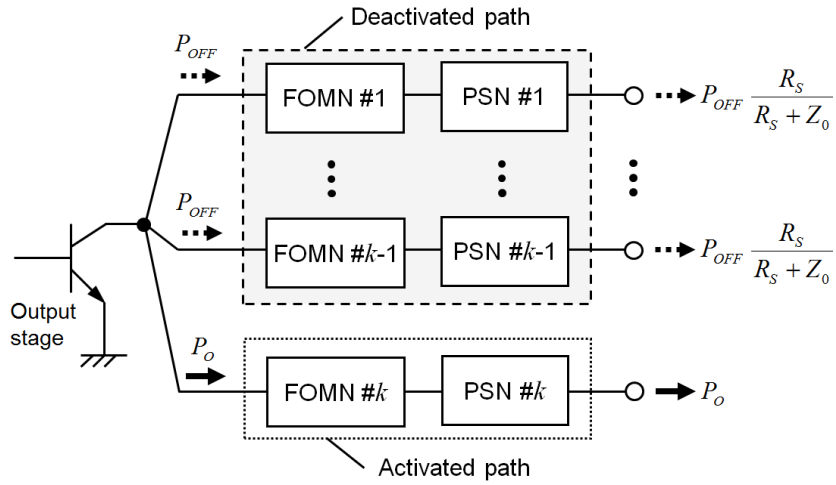


Figure 2.14: Power flow of the reconfigurable output network with k-outputs.

$$PL\big|_{\alpha=1,R_A=R_{opt}} \equiv \frac{P_O+(k-1)P_{OFF}}{P_O} = 1+\frac{(k-1)(R_{S1}Z_0)(1+N^2)}{R_{S1}{}^2+\left(NZ_0\right)^2} \approx 1+(k-1)\frac{R_S}{Z_0} \tag{2.15}$$

$$ISO\big|_{\alpha=1,R_A=R_{opt}} \equiv \frac{P_O}{P_{OFF}\dfrac{R_S}{Z_0+R_S}} = \frac{R_{S1}^2+\left(NZ_0\right)^2}{1+N^2}\frac{Z_0+R_S}{R_{S1}R_SZ_0} \approx \left(\frac{Z_0}{R_S}\right)^2. \tag{2.16}$$

N is assumed to be much greater than unity in the approximated results in (2.15) and (2.16). The PL and ISO are plotted in Fig. 2.15. It can easily be seen from Fig. 2.15 that R_S of the switch is a key factor in determining the PL and ISO.

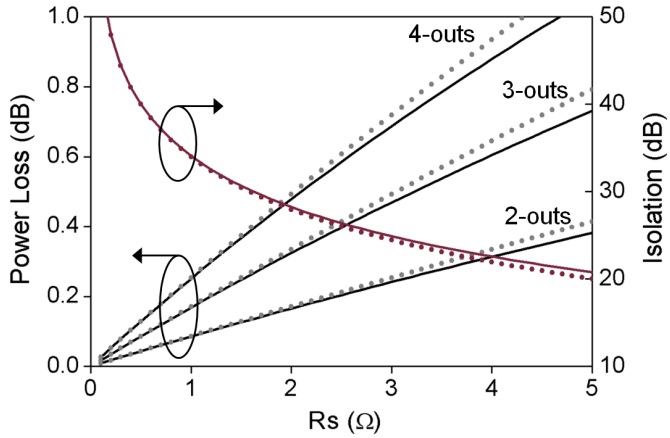


Figure 2.15: PL and port-port ISO of the PSN as a function of series-resistance of the switch at on-state (R_S) (solid lines: calculation, dotted lines: approximation).

2.2.4 Experimental Validation of PRN and FRN

To validate the power- and frequency-reconfiguration capabilities of the proposed networks under various power back-off ratios and frequency scaling factors, a one-stage PA with PRN and FRN, shown in Figs. 2.3 and 2.7, was fabricated and characterized. The fabricated InGaP/GaAs heterojunction bipolar transistor (HBT) PA has an emitter area of 4800 μm^2 and was implemented on a 400-μm thick FR4 (ε_r ~ 4.6, tanδ = 0.025) substrate. For this concept-proof experiment, the switch was assumed to be lossless and wire-bonding connection was used to represent a "switch on" state. The target output power and operating frequency of the PA for natural band are chosen to be 28.2 dBm and 1950 MHz, respectively. 3GPP uplink W-CDMA (Rel'99) signal and the supply voltage of 3.5 V with the quiescent current of 50 mA were used for the measurement. Fig. 2.16 shows the measured gain, adjacent channel leakage ratio (ACLR) at 5 MHz offset, and collector efficiency (CE) of the power reconfigured PA at seven backed-off power (P_{BO}) points from 0 to 6 dB (rated linear P_{out} = 28.2 ~ 22.2 dBm). The quiescent current of the power reconfigured PA was adjusted to further enhance the

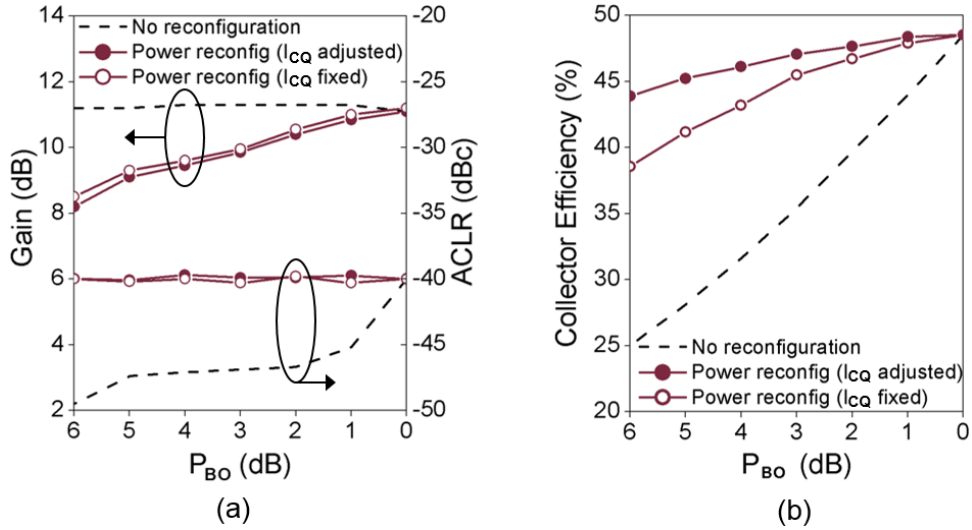


Figure 2.16: Measured performance of the power reconfigured PA: (a) Gain and ACLR. (b) Collector efficiency.

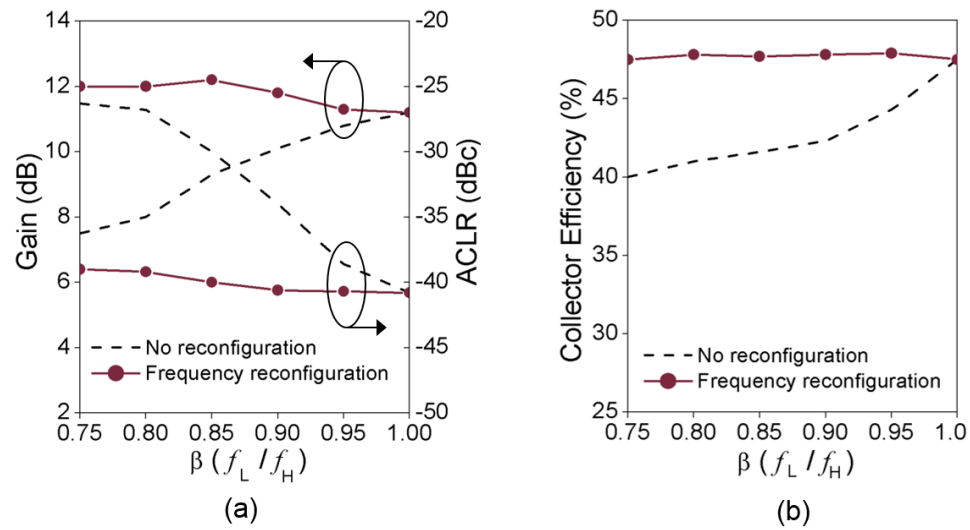


Figure 2.17: Measured performance of the frequency reconfigured PA: (a) Gain and ACLR. (b) Collector efficiency.

efficiency at the P_{BO} levels. As expected, the PRN allowed CEs to be maintained at P_{BO} levels. CE was maintained to be 43% with ACLR of –40 dBc at 6 dB backed-off power level whereas the CE dropped to 25% without a PRN.

Fig. 2.17 shows the measured results of the PA with a FRN at six scaled

frequency points (β = 0.75 ~ 1.0 or 1460 ~ 1950 MHz), which corresponds to a wide fractional bandwidth of 29%. The frequency reconfigured PA maintained ACLR of –39 dBc and CE of 46% while the PA without reconfiguration showed large efficiency and linearity degradation (40% CE and –26 dBc ACLR at β = 0.75). This experiment validates the concept and analysis of the proposed PRNs and FRNs. The verification of the PSN is included in the subsequent chapter, where the measured results of a fully integrated multiband reconfigurable PA module are presented.

2.3 Fabrication and Measurement of a Multiband UMTS Reconfigurable Power Amplifier

2.3.1 Design

To verify the performance of the proposed reconfigurable network for practical UMTS PA application, a fully integrated 5 mm × 6 mm multiband reconfigurable PA module was designed and fabricated [21]. Fig. 2.18 shows the schematic of the reconfigurable PA module. The PA has two inputs and three reconfigurable outputs for most popular tri-band UMTS applications. The complete PA module contains two reconfigurable output matching networks (OMNs) and two integrated three-stage PA monolithic microwave integrated circuits (MMICs) one each for high and low UMTS bands. The prototype PA can cover five popular UMTS frequency bands and works with two frequency-band combinations as follows:

- Combination 1: band-1, band-2, and band-5;
- Combination 2: band-1, band-4, and band-8.

Combination 1 is the North America-centric band combination with band-1 for roaming and Combination 2 is the Europe-centric band combo with band-4 for roaming. Both FRN and PRN can be demonstrated together with PSN in this band

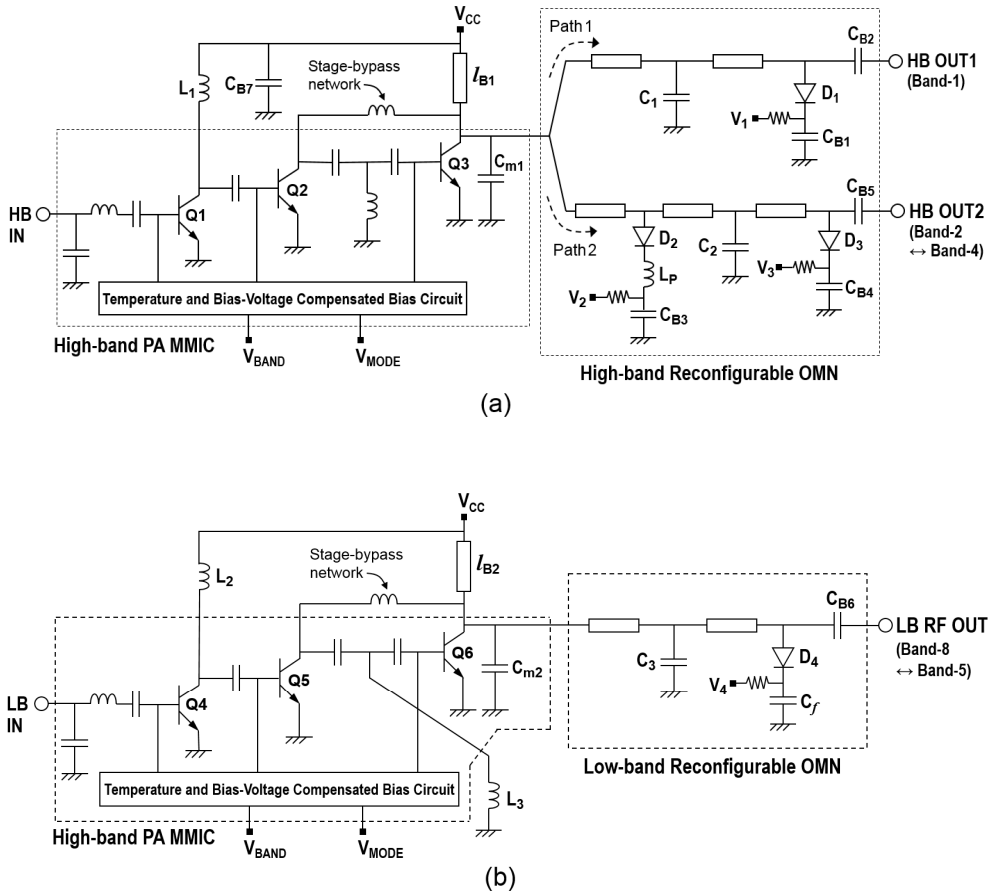


Figure 2.18: Schematic of the multiband reconfigurable PA module: (a) High-band PA. (b) Low-band PA.

combination. Details of the frequency and the targeted maximum linear output power are summarized in Table 2.1. The high-band output path-1 has a natural band (band-1) and has no reconfigurable band. In the case of high-band output path-2, band-2 is the natural band and band-4 is the reconfigured band. In the case of band-2 and band-4, besides the frequency difference (11%), the difference in the linear output power should be accounted for in the PA design. Band-2 requires at least 1 dB higher output power than band-4 due to the higher post-PA loss; band-2 has smaller Tx-Rx separation, which makes Tx insertion loss of the subsequent duplexer higher than that for band-4, as shown in Fig. 2.19 [22], [23]. Thus, the

TABLE 2.1

UMTS FREQUENCIES AND TARGET LINEAR OUTPUT POWERS

Band	Tx Frequency (MHz)	Rx Frequency (MHz)	Target P_{out} (dBm)
Band-1	1920 – 1980	2110 – 2170	28.0
Band-2	1850 – 1910	1930 – 1990	28.5
Band-4	1710 – 1755	2110 – 2155	27.5
Band-5	824 – 849	869 – 894	28.2
Band-8	880 – 915	925 – 960	28.2

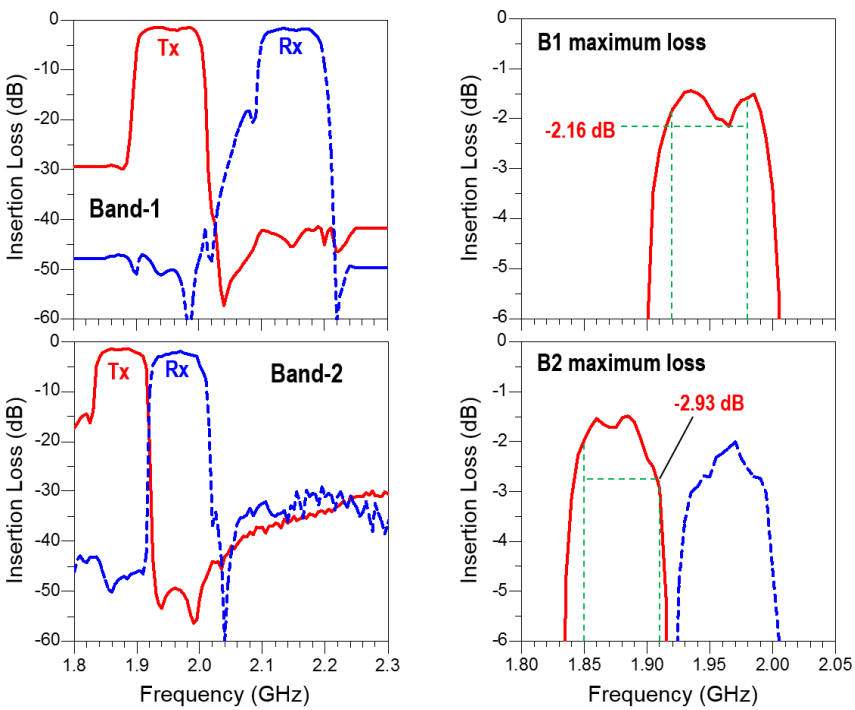


Figure 2.19: Tx/Rx insertion losses of the band-1 and band-2 duplexers (losses were not de-embedded) [22], [23].

PRN has been added in path-2 to reconfigure the output power for band-4. Finally, in the case of low-band output, the FRN is inserted to support both band-5 and band-8; band-8 is the natural band and band-5 is the frequency reconfigured band.

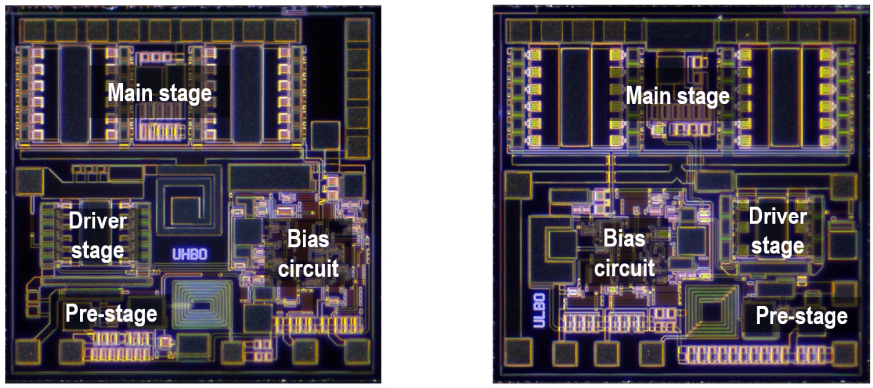
TABLE 2.2

LOGIC TABLE AND OPERATION DESCRIPTION OF PIN DIODES

V_{BAND}	PIN diode control voltage				Operation	
	V_1	V_2	V_3	V_4		
High	Off	Off	On	Off	HB Out 1	Band-1
High	On	Off	Off	Off	HB Out 2	Band-2
High	On	On	Off	Off	HB Out 2	Band-4
Low	Off	Off	Off	Off	LB Out	Band-8
Low	Off	Off	Off	On	LB Out	Band-5

The reconfigurable OMNs are implemented using the lumped elements and T/Ls on a 370-μm thick seven-layer substrate ($\varepsilon_r \sim 4.7$, $\tan\delta = 0.02$). In Fig. 2.18, C_1, C_2, and C_3 are lumped-element capacitors of FOMNs optimized for the natural bands, whereas L_P and C_f are the lumped-elements for PRN and FRN, respectively, as explained in Chapter 2.2. Six capacitors, $C_{B1} \sim C_{B6}$, were used for dc blocking and C_{B7} as bypass capacitor. Two bias-lines, l_{B1} and l_{B2}, are implemented on inner layers of the substrate. Switches are realized with PIN diodes, which have a series resistance of 1.0 Ω with forward on-current of 1.2 mA and a junction capacitance of 400 fF in the "off" state. They are controlled by control voltages, $V_1 \sim V_4$, according to the required UMTS band combinations. The mapping between control voltages and the selected frequency bands are summarized in Table 2.2, where the actual dc bias condition is 0 V for the "on" state and floating for the "off" state. Even if the PIN diodes at the output (D_1, D_3, and D_4) experience high RF voltage swing under high output power, they still remain "off" under the off-state bias condition. The large RF voltage swing does not cause any issues to PIN diodes since they have a very large reverse breakdown voltage of 50 V.

The PA MMICs were designed and fabricated using a 2-μm InGaP/GaAs HBT process. They are based on a three-stage amplifier design, and the emitter area of the pre-stage (Q1 and Q4), driver stage (Q2 and Q5), main stage for high-



(a) (b)

Figure 2.20: MMIC die photographs. (a) High-band PA MMIC. (b) Low-band PA MMIC.

band (Q3), and main stage for low-band (Q6) were designed to be 240 μm^2, 1440 μm^2, 5760 μm^2, and 6768 μm^2, respectively. The low-pass-type input matching networks and high-pass-type interstage matching networks were integrated in the MMICs. Two shunt capacitors, C_{m1} and C_{m2}, were added at the collectors of Q3 and Q6, respectively for harmonic termination. The bias circuit was designed following our previous work, which is insensitive to temperature and bias voltage variations [24], [25]. To enhance the efficiency in the low output power region where UMTS PAs are operated most of the time, the PAs were designed to bypass main stages below 16 dBm using the patented CoolPAM topology [26]. The die size of each PA MMIC is 1.1 mm × 1.08 mm and the photographs of the fabricated MMICs are shown in Fig. 2.20.

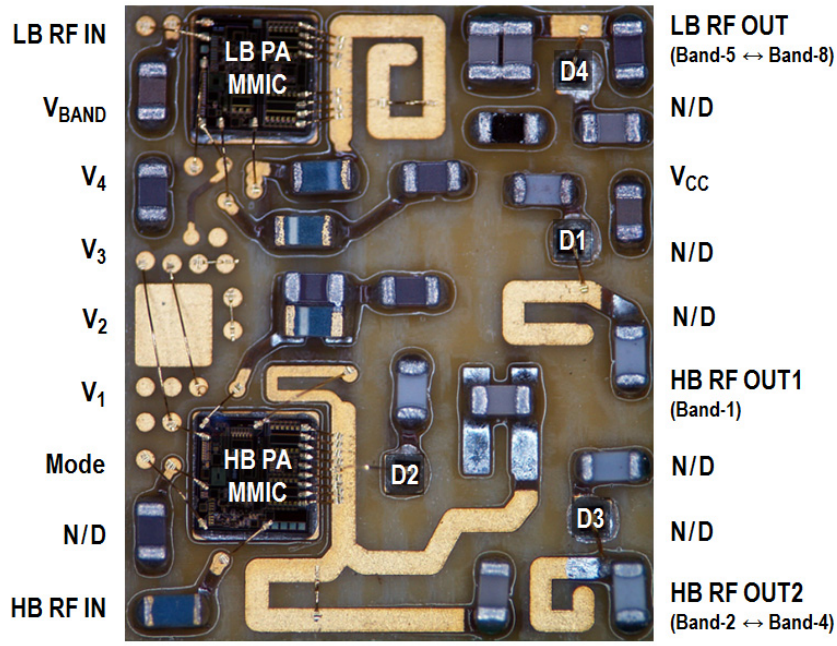


Figure 2.21: Photograph of the fabricated 5 mm × 6 mm PA module.

2.3.2 Measurement

The fabricated 5 mm × 6 mm PA module is shown in Fig. 2.21. The PA module works with 3.5-V supply voltage, and the 3GPP uplink W-CDMA signal (Rel'99) was used for the measurement. The high- and low-band PA have the same bias conditions in which the quiescent currents are 21 mA and 100 mA for low- and high-power modes, respectively. Fig. 2.22 shows the measured small-signal S-parameters of the fabricated PA module. The fabricated PA shows the input return loss higher than 10 dB for all the operating Tx frequency bands. Fig. 2.23 shows the measured output power vs input power using a continuous wave (CW) signal, showing the power linearity.

The measurement results of power gain, power-added efficiency (PAE), ACLR, and error vector magnitude (EVM) are shown in Fig. 2.24 and 2.25 for band combination 1 and 2, respectively. In the case of combination 1 (band-1, -2,

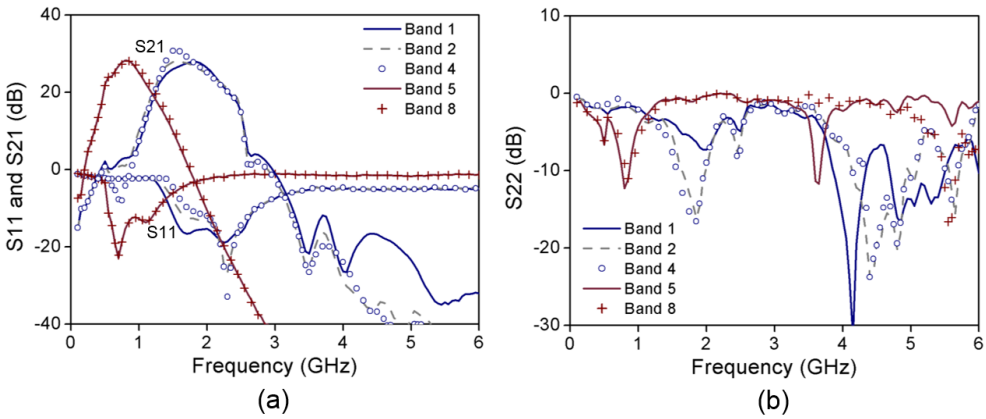


Figure 2.22: Measured S-parameters: (a) S11 and S21. (b) S22.

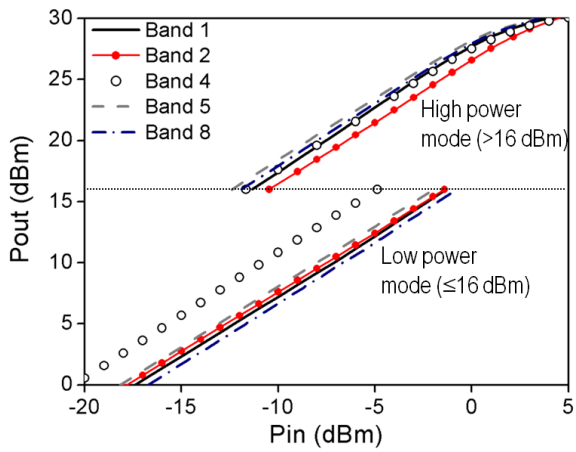


Figure 2.23: Measured CW output power as a function of input power.

and -5) shown in Fig. 2.24, the PA showed gains of higher than 26.6 dB and ACLRs of better than –39 dBc up to the rated maximum output powers (28.0 dBm at band-1, 28.5 dBm at band-2, and 28.2 dBm at band-5). PAE at maximum linear power meeting –39 dBc ACLR was higher than 39% for all the three bands (39% at 28 dBm for band-1, 40.7% at 28.5 dBm for band-2, and 43% at 28.2 dBm for band-5). It should be noted in Fig. 2.24 that the band-5 results with frequency reconfiguration (V_4 is on) show better PAE (2.6% improvement) than that without reconfiguration (V_4 is off), while maintaining the similar level of linearity.

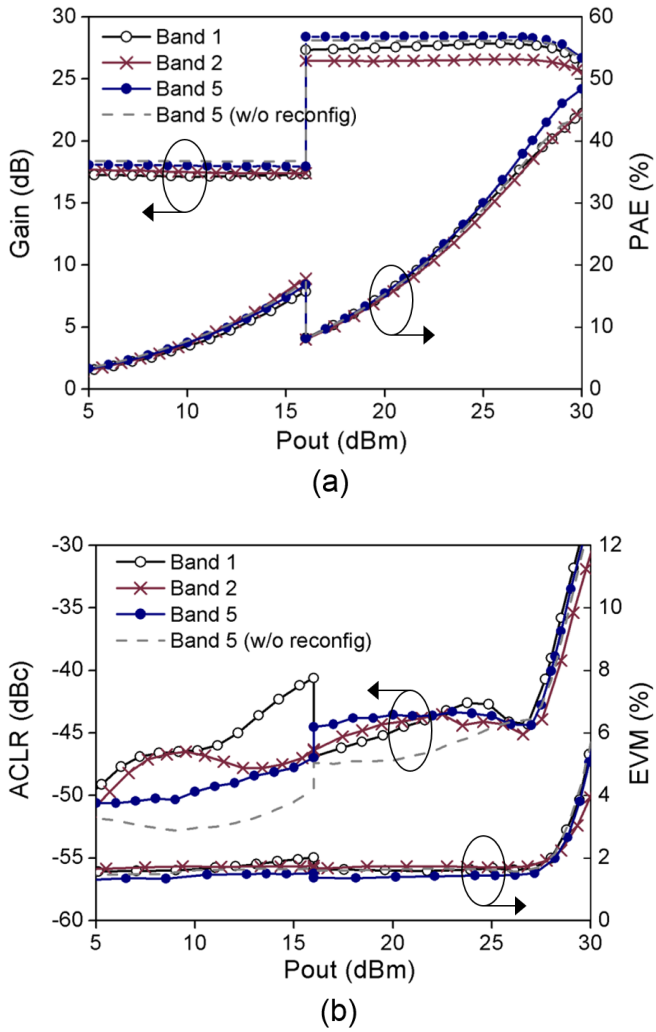


Figure 2.24: Measured W-CDMA results for combination 1: (a) Gain and PAE. (b) ACLR and EVM.

For combination 2 (band-1, -4, and -8) shown in Fig. 2.25, the PA also showed linear power gains of higher than 27.8 dB and ACLRs of better than –39.2 dBc up to the rated linear output powers (28 dBm at band-1, 27.5 dBm at band-4, and 28.2 dBm at band-8). PAE at maximum linear power meeting –39 dBc ACLR was higher than 38.5% for all the three bands (39% at 28.0 dBm for band-1, 38.5% at 27.5 dBm for band-4, and 43.2% at 28.2 dBm for band-8). It should be noted from Fig. 2.25 that the band-4 results with power reconfiguration (V_2 is on) show

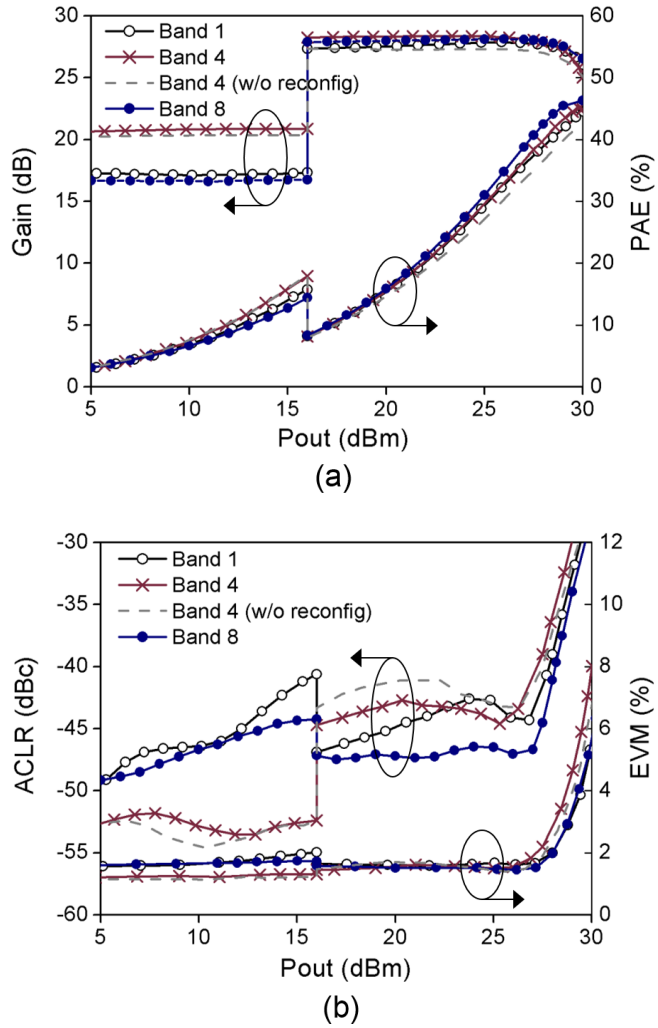


Figure 2.25: Measured W-CDMA results for combination 2: (a) Gain and PAE. (b) ACLR and EVM.

better PAE (3.3% improvement) than that without reconfiguration (V_2 is off), while maintaining the similar ACLRs. Band-4 showed the lowest PAE since the inductance used in PRN was only 2.0 nH and could not satisfy the condition of $R_S << \omega L_P$ to avoid the impact of switch loss. The measured EVMs were less than 2.3% up to the rated maximum output powers of all the frequency bands. Also, the measured port-port isolation was better than 29 dB for high bands. This is attributed to the PIN diodes with a small R_S of 1.0 Ω.

The idle current, which has significant impact on the overall talk time, was reduced to 21 mA using the stage-bypass approach. Also, high PAE in the low power region (< 16 dBm) helps reduce the average current consumption of the handset PA under the actual phone operating conditions [27]. PAE of higher than 14.5% was measured at P_{out} = 16 dBm. In order to compare the performance of the multiband reconfigurable PA with a single-band PA, a reference PA was also fabricated using the same PA die with an FOMN. The reference PA for each band showed PAE of 40.5% ~ 43.6% at the rated linear P_{out} with an ACLR of –39 dBc. Thus, the multiband reconfigurable PA showed PAE degradation of less than 2%. PAE degradation is attributed due to losses from the switches as well as the bias current of PIN diodes. The measured results are summarized in Table 2.3. The total estimated losses of the reconfigurable OMN are less than 0.6 dB, out of which 0.2 dB arises from the reconfiguration, while the loss of the FOMN and bias circuit accounts for 0.4 dB.

The performance of recently reported multiband reconfigurable PAs is summarized in Table 2.4 for comparison. The reconfiguration loss (0.2 dB) of this work compares favorably with the estimated losses of other reconfigurable PAs reported to date (higher than 0.45 dB) [2]-[8], [28]. PAE degradation can further be reduced by using lower loss switches such as pseudomorphic HEMTs (pHEMTs) and MEMS switches. To the best of our knowledge, this is the first demonstration of UMTS reconfigurable PAs meeting the system linearity requirements with minimal PAE degradation.

TABLE 2.3

SUMMARIZED MEASUREMENT RESULTS OF THE FABRICATED RECONFIGURABLE PA

Band	P_{out} (dBm)	Gain (dB)	PAE (%)	Ref PA PAE*(%)	ACLR (dBc)
Band-1	28.0	27.8	39	41	–39.2
Band-2	28.5	26.6	40.7	41.9	–39.1
Band-4	27.5	28.2	38.5	40.5	–39.5
Band-5	28.2	28.4	43	43.5	–39
Band-8	28.2	28.1	43.2	43.6	–39.3

*PAE of the single-band reference PA

TABLE 2.4

PERFORMANCE COMPARISON OF RECENTLY REPORTED MULTIBAND RECONFIGURABLE PAS

Ref.	PA core (switch) technology	Band coverage (GHz)	Num of outs[1]	PA operation	P_{out} and PAE	Rec. loss[2] (dB)
Fukuda 06 [3]	GaAs FET (MEMS)	0.9, 1.5 2.0, 5.0	1	Linear (CW)	P_{out} = 30.5~31 dBm PAE = 45~64%	0.45*
Zhang 09 [4]	GaAs HBT (MEMS)	0.9, 1.6	2	Linear (CW)	P_{out} >30 dBm PAE > 27%	0.96
Zhang 05 [6]	GaAs HBT (PIN diode)	0.85~0.95 1.71~1.95	1	Linear (CW)	P_{out} = 31 dBm PAE = 39~42%	0.45*
Kim 11 [9]	0.18 μm CMOS (w/o switch)	1.9, 2.3 2.6, 3.5	1	Non-linear (Class-E)	P_{out} = 20.5~24.2 dBm Drain Eff = 36~48%	0.8*
Neo 06 [10]	SiGe HBT (varactor)	0.9, 1.8 1.9, 2.1	1	Linear (CW)	P_{out} = 28 dBm Drain Eff = 30~55%	1.3*
Fukuda 10 [5]	GaAs HBT (GaAs FET)	0.7~2.5 (9-bands)	1	Linear (UMTS)	P_{out} = 29 dBm PAE = 23~33%	0.95*
This work [21]	GaAs HBT (PIN diode)	0.84, 0.9 1.73, 1.88 1.95	2	Linear (UMTS)	P_{out} = 27.5~28.5 dBm PAE = 38.5~40.7%	0.2

[1]Number of reconfigurable outputs

[2]Estimated reconfiguration loss

*Post-PA switch loss of 0.35 dB [28] was used to estimate the reconfiguration loss.

2.4 Summary

A design methodology to realize reconfigurable OMN for a multiband UMTS PA is presented together with details of closed-form design equations. The analysis shows how a PRN and an FRN can be co-designed with a fixed OMN to reduce the overall size and loss of the reconfigurable OMN. Proof-of-concept experiment using ideal switches demonstrated that the proposed PRN and FRN allows the PA efficiencies to be maintained at the reconfigured power levels and frequencies.

To prove the practicality of the proposed approach, we have designed and fabricated a tri-band UMTS reconfigurable PA module in a small form factor of 5 mm × 6 mm using InGaP heterostructure bipolar transistors and PIN diodes. This PA can switch between two band combinations, UMTS bands 1/2/5 and 1/4/8. The PA features stage-bypass topology to enhance the low-power efficiency below 16 dBm and meets all the UMTS linearity requirements with margin (<–39 dBc versus system spec of –33 dBc) at the rated linear output power level. The measured PAE from the module was better than 38.5% for all the UMTS bands while meeting –39 dBc ACLR. Compared with a single-band PA with an FOMN, the maximum power efficiency was degraded by less than 2%. The efficiency degradation can further be reduced by using low-loss switch elements such as pHEMTs and MEMS switches.

With the strong demand for multiband coverage for global roaming, the proposed reconfigurable PA can be a practical solution for UMTS multiband Tx applications. Moreover, the proposed PA architecture can be extended to include second-generation (2G GSM) and fourth-generation (4G LTE) bands in a single reconfigurable PA module.

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Chapter 3

Linearization of CMOS Power Amplifier and Its Multiband Application

3.1 Introduction

CMOS power amplifier (PA) can play an important role not only for WiFi but also for 3G/4G mobile terminals due to the cost and size benefits. However, low breakdown voltage and highly nonlinear nature of the CMOS devices make the design of a watt-level linear PA very challenging, in particular, for applications using high-level modulation schemes. To achieve the required output power level for 3G UMTS and 4G LTE handsets, several power combining techniques such as the distributed active transformer (DAT), differential cascode using a transmission line transformer (TLT), and stacked-FET have been researched and some of them have successfully been demonstrated [1]-[7]. To improve the linearity of CMOS PAs, various linearization techniques have been proposed such as the capacitance compensation, diode-linearizer, multi-gate transistor (MGTR), PA-closed loop feedback, adaptive bias, and so on [8]-[19]. However, the overall linearity and

efficiency of these works cannot match those of GaAs HBT PAs [20].

For modulated signals, PA nonlinearity is determined by the dynamic AM-AM and AM-PM characteristics. Thus, dynamic-based linearization techniques have also been researched to selectively correct for the compressed envelope region only of a modulation signal [21], [22]. Since these works have mostly focused on the correction of AM-AM distortion at high output power (P_{out}) using the envelope-reshaped bias, they do not correct for AM-PM distortion and, in some cases, degrade the linearity at backed-off power levels [23]. Even though the idea of using a varactor for AM-PM correction has been introduced in [24], however, the method is limited to the quasi-linear region with negligible AM-AM distortion. Also, it requires a separate digital signal processor (DSP) chip and digital to analog (D/A) converter, which makes the application to the self-contained mobile phone PA practically difficult.

In terms of multiband (MB) PAs for global roaming, multi-banding of CMOS PAs should be considered. To achieve this goal, several converged PA structures have been proposed [25]-[30]. Due to the practical bandwidth limit, however, most of the reported MB converged PAs for handsets employ two PA-cores to cover the 3G/4G bands from 800 MHz to 2000 MHz [27]-[30]. Even though a single-chain MB PA was tried in [26], however, its power-added efficiencies (PAEs) were compromised too much (25 ~ 31%) to be used for the power-hungry handset applications. Recently, a broad-banding method by employing the reconfigurable interstage network as well as the broadband output matching have been introduced to minimize the efficiency degradation [31]. However, its operating bandwidth has been limited to 0.65 to 1 GHz.

In this study, a highly linear and efficient MB PA is implemented using a silicon-on-insulator (SOI) CMOS technology. For linearization of CMOS PAs, a new linearizer based on AM-PM correction is proposed using an envelope-

reshaped phase (capacitance) injection circuit [32]. The AM-PM linearizer of this work also helps recover AM-AM distortion. Combined with the auxiliary amplitude injection [21] and hybrid biasing techniques, the 0.9 GHz and 1.88 GHz SOI CMOS stacked-FET PAs of this work achieve very high linear PAEs (almost state-of-the-art results while maintaining W-CDMA ACLR of –39 dBc). Then, a single-core single-chain MB linear CMOS PA is developed using the proposed linearizer and reconfigurable networks described in Chapter 2. The single-chain MB reconfigurable CMOS PA supports any combination of two bands, one from the high-band (HB: 1.7 ~ 2.0 GHz) group and the other from the low-band (LB: 0.8 ~ 0.9 GHz) group. The fabricated PA shows minimal PAE degradation compared with the single-band dedicated PA with W-CDMA PAEs in excess of 46% for LB and 40.7% for HB [33].

This study is organized as follows: In Chapter 3.2, prior arts are discussed. Chapter 3.3 and 3.4 deal with the harmonic termination and gate bias modulation effect of a stacked-FET amplifier for optimum design of a standalone PA. The detailed operation principle, design, and measurement of the proposed linearizer are described in Chapter 3.5 ~ 3.8. Finally, the design and measurement result of the single-chain MB reconfigurable linear CMOS PA is presented in Chapter 3.9.

3.2 Linearization of CMOS PAs: Prior Arts

CMOS PA linearization techniques reported so far can be subdivided into a static-level method and a dynamic-level method. The static linearizer has simple structure while compromising linearity improvement, and its performance is usually characterized using a constant-envelope signal (e.g. single-tone static AM-AM and AM-PM). On the other hand, the dynamic linearizer strongly corrects for the nonlinearity while increasing the circuit complexity, and its performance is usually evaluated by non-constant envelope signals (e.g. two-tone dynamic AM-

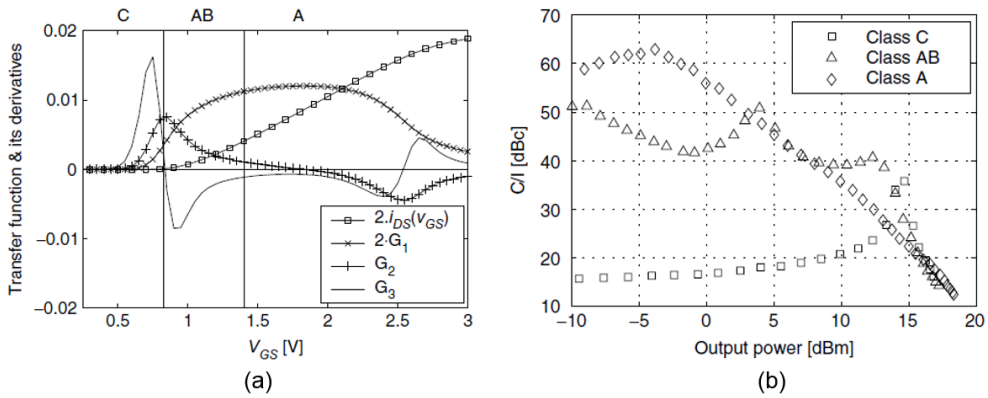


Figure 3.1: Typical characteristics of a common-source CMOS amplifier [23]. (a) PA input-voltage/output-current transfer function and its derivatives for IMD estimation. (b) Measured IMD3 for various PA-classes.

AM and AM-PM).

In the case of static-level linearization, various linearizers have been proposed. In [8], the nonlinear gate-source capacitance (C_{gs}) of a common-source (CS) NMOS amplifier was compensated using a PMOS counterpart. However, this method causes the excessive gate-source parasitic capacitance ($C_{gs.n}$+$C_{gs.p}$), thus resulting in power loss and bandwidth limitation. The diode linearizer in [9]-[12] boosts the dc gate bias of a CS amplifier and thus it enhances 1-dB compression output power (P_{1dB}). However, this method is effective for the PA of which the dc gate bias as a function of input power shows compression behavior [9], [10]. Even though the AM-PM compensator in [18] and cascode feedback bias [19] showed a certain amount of linearity improvement, the resultant performance is still not comparable as the GaAs HBT PA [20].

As Fager *et al* [23] analyzed and experimentally demonstrated, the linearity of a CMOS PA at high power level can be improved by applying low bias condition, which is due to the large-signal transfer function behavior of the transconductance (G_m). However, the linearity gets worse at mid power level, as shown in Fig. 3.1.

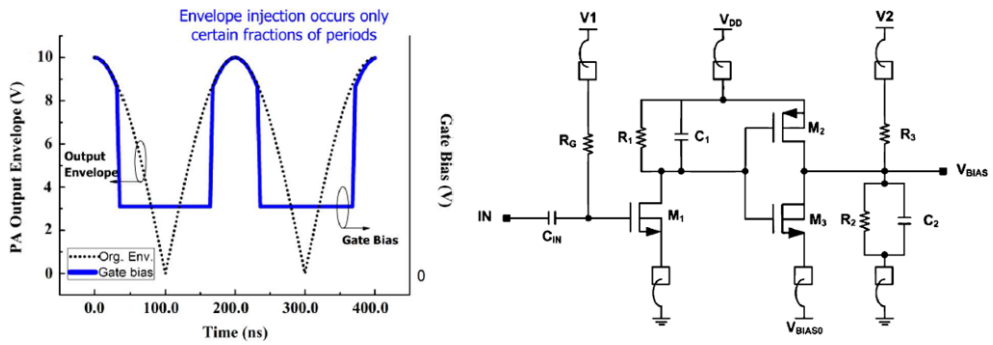


Figure 3.2: Envelope-reshaped gate biasing [21]. (a) Gate-biasing concept. (b) Schematic of the common-source (CS) bias circuit.

To achieve good linearity over a wide power range, a multi-gate transistor (MGTR) technique has been proposed [13], [14]. However, it excessively reduces the power gain. Therefore, the static bias profile having low bias at high power level (and high bias at low power level) can contribute for the PA linearity.

Contrary to the static linearizer, the dynamic linearizer utilizes the time-varying envelope signal to provide envelope-dependent voltages to the voltage-controlled elements to correct for dynamic AM-AM and/or AM-PM distortions. Thus, its linearization effect is stronger than the static case. Several researchers have revealed the usefulness of the envelope-injection technique for linearity improvement [34]-[36]. Koo *et al* [21] proposed an integrated CS bias circuit shown in Fig. 3.2, which showed almost state-of-the-art performance in terms of linear efficiency. Even though the method [21] clearly improves the dynamic AM-AM by providing high gate bias during the envelope-compressed time region only as shown in Fig. 3.2(a), however, it may not corrects (or even worse) for the AM-PM compression. Also, it may cause PAE degradation when the gate bias is over-driven. Jin *et al* [22] employed the enveloped-dependent gate bias circuits for a common-gate (CG) stage as well as a CS stage of a differential cascode PA.

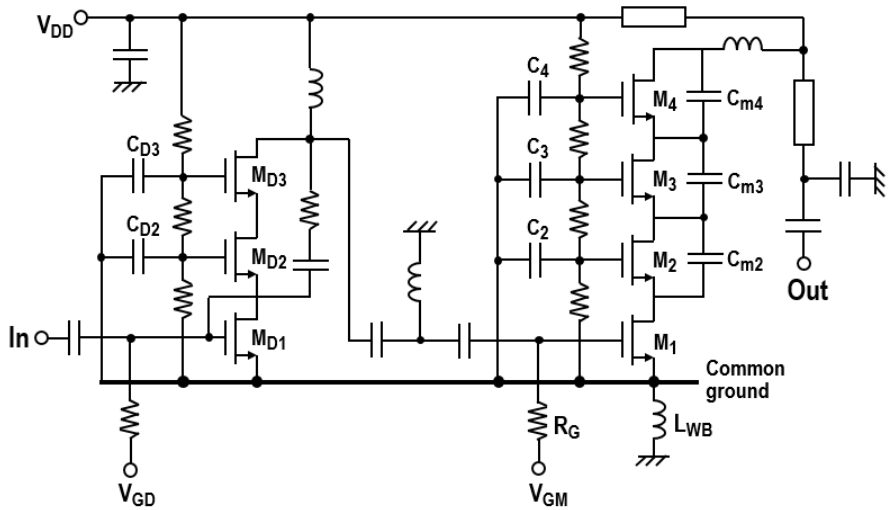


Figure 3.3: Schematic of the standalone CMOS PA used in this study.

However, the method is not suitable for the single-ended stacked-FET structure.

There is a previous work on the phase-based dynamic linearizer using a varactor for wireless local-area-network (WLAN) PA by Palaskas *et al* [24]. However, in [24], the power range of interest was quasi-linear region (4.5 dB power-backed-off from P_{1dB}), where the AM-AM distortion was negligible, leaving AM-PM as the only source of distortion to degrade the error vector magnitude (EVM) for WLAN application. This method cannot be directly applied to 3G/4G handset PAs, which often operate into the gain compressed region, where AM-AM and AM-PM distortions are coupled with each other and both affect the PA nonlinearity.

3.3 Harmonic Termination

To implement a highly linear and efficient CMOS PA, an optimum standalone PA design is prerequisite. The standalone PA design of this work is aimed to achieve high efficiency while maintaining moderate linearity; thus the proposed linearizers (in Chapter 3.5 and 3.6) make the PA further enhance the linear

efficiency. Fig. 3.3 shows a schematic of the proposed standalone CMOS PA. It is based on a two-stage stacked-FET amplifier, where the driver-stage and main-stage have triple stack with a 2-mm gate-width and quadruple stack with a 20-mm gate-width, respectively [6], [17]. The output matching network (OMN) is realized with off-chip components; a transmission line (T/L) and a lumped capacitor. To improve the efficiency and linearity of a standalone PA, the harmonic termination and control of the gate bias modulation effect are performed in Chapter 3.3 and 3.4, respectively.

3.3.1 Operation Analysis

To enhance the efficiency of a stacked-FET PA, load impedances of the stacks at the harmonic frequencies ($2f_0$, $3f_0$, $\cdots$) as well as the fundamental frequency (f_0) should be optimized. Since the CMOS FETs have parasitic capacitances (e.g. C_{gs}, C_{gd}, C_{ds}, and C_{dsub}), they make the fundamental load impedances locate sub-optimal region. To avoid the effect, several techniques such as the shunt-inductive elements and the external drain-source Miller capacitors have been adopted [37]. In this study, three Miller capacitors (C_{m2} ~ C_{m4} in Fig. 3.3) are employed to align the drain voltage of each stack in-phase. To further enhance the efficiency, the harmonic termination is essential since the load impedances at harmonic frequencies (especially at $2f_0$ and $3f_0$) can provide a condition in the manner that the drain voltage and current are not overlapped each other [38]. Thus, the Class-F/F^{-1}/J PA designs can improve the efficiency [39], [40]. Contrary to the PAs based on a CS stage, the stacked-FET PA is required to have optimum harmonic impedances at the internal FETs as well as the top FET, because each FET equally contributes to adding drain voltage while sharing drain current. To achieve this, the harmonic termination should not cause excessive loss and should not disturb the fundamental load impedance. Also, the dc supply voltage must be taken into account for choosing operation mode due to the limited battery voltage (V_{DD} < 4 V)

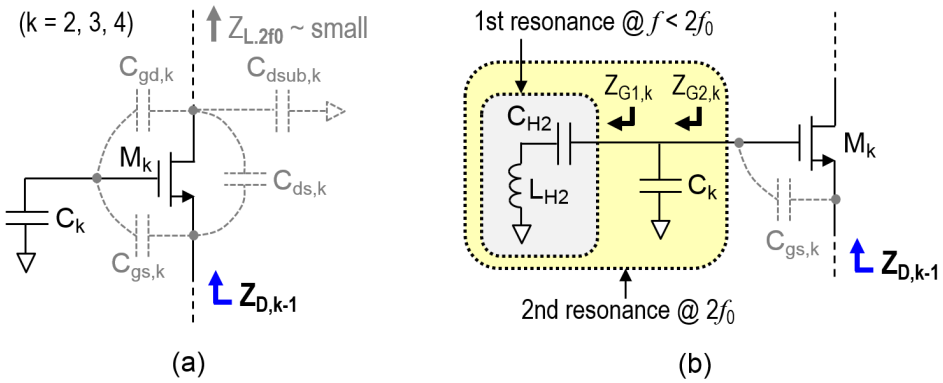


Figure 3.4: (a) Parasitic capacitances of the *k*-th FET in a stacked-FET PA. (b) Double resonance method to obtain an optimum impedance ($Z_{D,k-1}$) at $2f_0$.

of mobile devices.

In designing a watt-level stacked PA, several design parameters (such as the size of FET, number of stack, and supply voltage) should carefully be determined. Even if Pornpromlikit *et al* [6] achieved the output power (P_{out}) of more than a watt under high V_{DD} (= 6.5 V) and large load impedance (Z_L = 11.5 Ω) conditions, however, the supply voltage needs to be limited below 4 V for mobile handset applications. This means that the FET size should be larger to handle more drain current and avoid high knee voltage, which further lowers Z_L. In this work, the FET gate-width of 20 mm and V_{DD} = 4 V are chosen, which corresponds to the parasitic gate-source capacitance (C_{gs}) of ~22 pF and Z_L = 5~6 Ω. Due to the large parasitic capacitance of the *k*-th FET and the distribution capacitor (C_k) as shown in Fig. 3.4(a), the load impedances of the (*k*–1)-th FET at $2f_0$ and $3f_0$, $Z_{D,k-1(2)}$ and $Z_{D,k-1(3)}$, become lower. For high efficiency operation, one of them should not be small but be located in the high efficiency region [31], [39], [40]. Since $Z_{D,k-1(2)}$ is easier to move toward the high-efficiency region than $Z_{D,k-1(3)}$ case, the Class-F^{-1} mode is employed in this work.

Fig. 3.4(b) shows a schematic of the *k*-th FET in the proposed stacked-FET PA. To provide an optimum harmonic impedance at $2f_0$, a capacitor (C_{H2}) and an

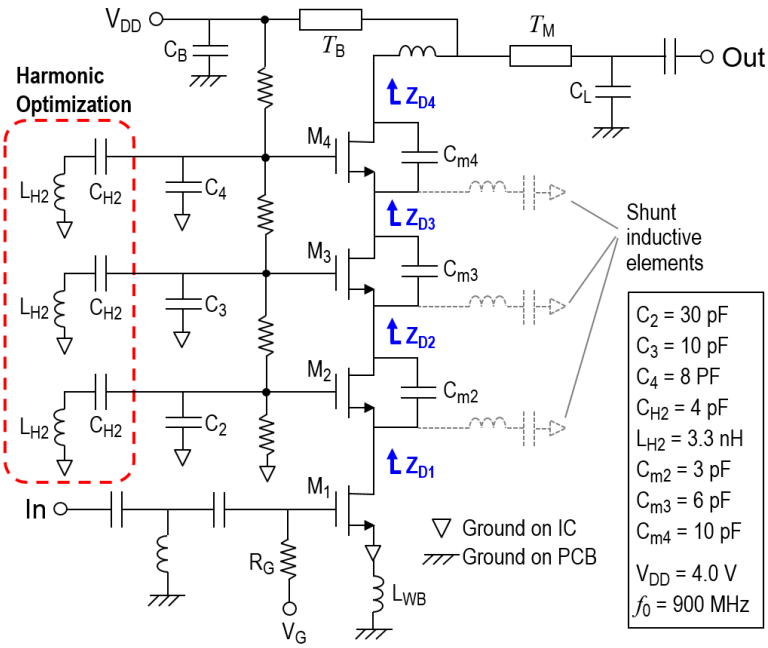


Figure 3.5: Schematic of the proposed harmonic-optimized PA.

inductor (L_{H2}) connected in series are added at the gate of a common-gate (CG) FET. C_{H2} and L_{H2} resonate below the second harmonic frequency ($f < 2f_0$) and thus their composite impedance at $2f_0$, $Z_{G1,k(2)}$ in Fig. 3.4(b), becomes inductive. $Z_{G1,k(2)}$ should be slightly inductive for parallel resonance with the following shunt element, C_k in Fig. 3.4(b). The second resonance is performed near $f \approx 2f_0$ by C_k along with $Z_{G1,k(2)}$ and thus the resultant impedance, $Z_{G2,k(2)}$ in Fig. 3.4(b), is obtained. Since $C_{gs,k}$ provides low impedance at $2f_0$ due to large gate-width of M_k, the target impedance, $Z_{D,k\text{-}1(2)}$ in Fig. 3.4(b), can thus have an optimum harmonic load at $2f_0$. To maintain the optimum load impedance at f_0 ($Z_{D,k\text{-}1(1)}$), C_k value in conjunction with C_{H2} and L_{H2} should be re-optimized.

Based on the double resonance technique described above, a 0.9 GHz stacked-FET PA was designed using an SOI CMOS process. Fig. 3.5 shows a schematic of the designed PA, where 0.32-μm gate-length 2.5-V NFETs were used. $C_2 \sim C_4$ are the gate distribution capacitors for stacked-FET PA design and $C_{m2} \sim C_{m4}$ are the

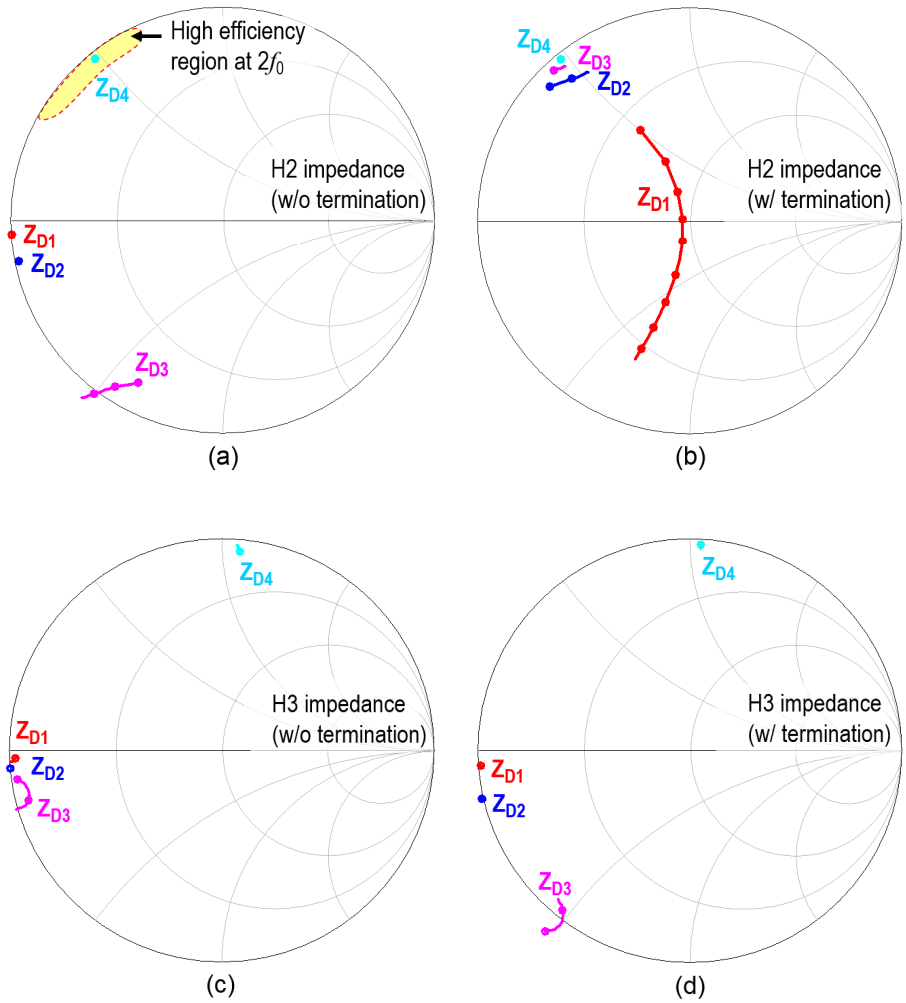


Figure 3.6: Simulated second-harmonic (H2) and third-harmonic (H3) impedances as a function of input power. (a) H2 without termination. (b) H2 with termination. (c) H3 without termination. (d) H3 with termination.

Miller capacitors [6], [37]. To completely reject the parasitic effect at f_0, the shunt inductive elements (dotted series inductors and capacitors in Fig. 3.5) are employed in the initial design. Fig. 3.6 shows the simulated harmonic load impedances of the PA. By applying the harmonic termination technique, the second-harmonic impedances of the intermediate FETs ($Z_{D,1(2)}$, $Z_{D,2(2)}$, and $Z_{D,3(2)}$) are moved to the inductive region where high efficiency is achieved, as shown in Fig. 3.6(b). Since C_2 is quite larger than C_3 and C_4, $Z_{D1(2)}$ is less optimized than expected. On the

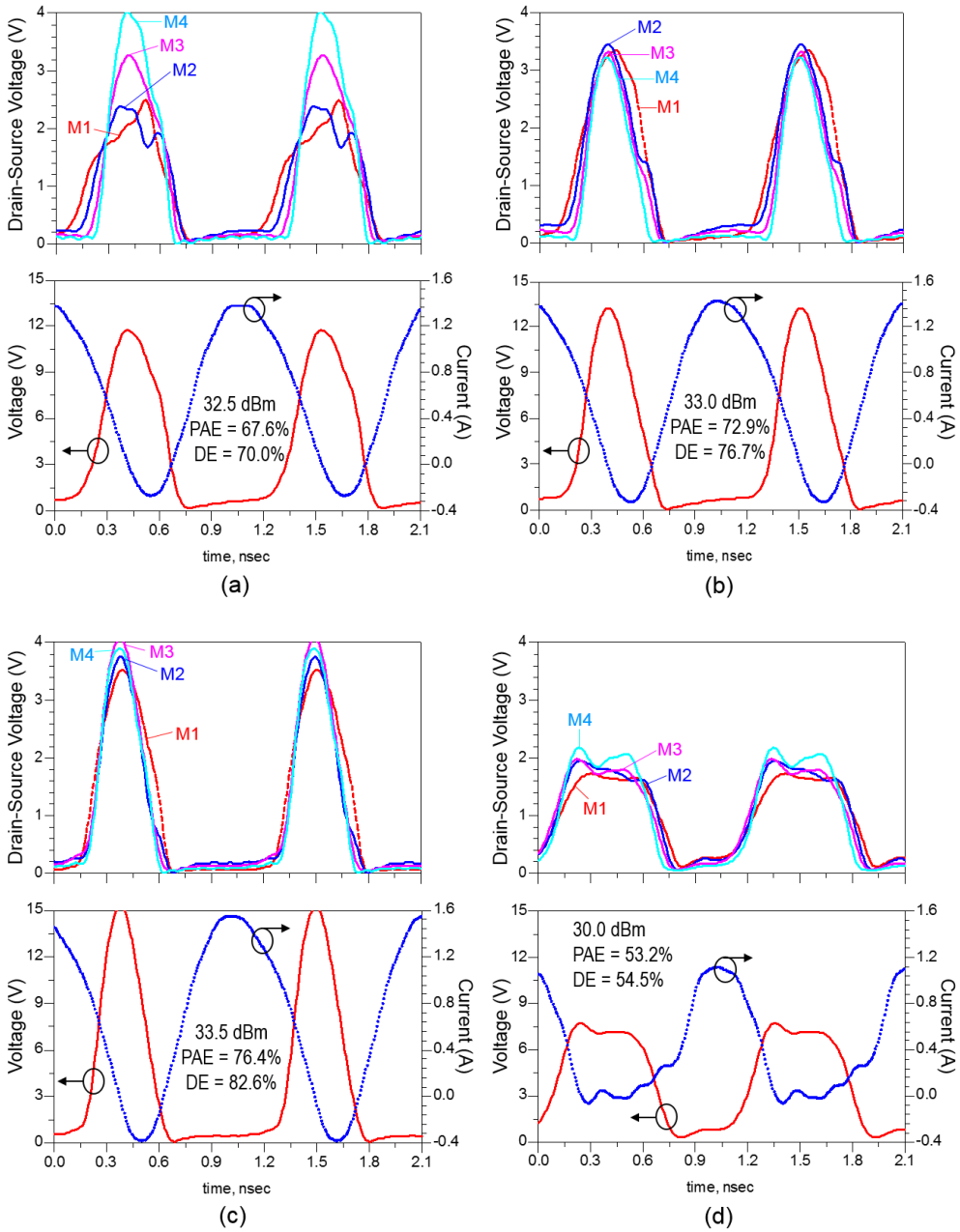


Figure 3.7: Simulated drain voltage and current waveforms. (a) Reference PA without ① shunt-inductive elements and ② harmonic tuning. (b) Reference PA with ①. (c) Proposed PA with ① and ②. (d) Class-F mode PA.

other hand, there is no considerable change in the third harmonic impedances, as shown in Fig. 3.6(c) and 3.6(d).

Fig. 3.7 shows the simulated drain-source voltage (V_{ds}) of each stack and the drain voltage/current waveforms of the top FET. To compare the performance of the proposed structure with other operation modes, two reference PAs and a Class-F PA were also simulated. The reference PA without shunt-inductive elements and harmonic termination (PA1) showed non-uniform V_{ds} profile among the FETs, moderate PAE (67.6%), and drain-efficiency (DE) of 70% at P_{out} = 32.5 dBm, as shown in Fig. 3.7(a). This is due to the fact that the parasitic cancellation by the Miller capacitors ($C_{m2} \sim C_{m4}$) was not completely fulfilled. As described in [37], too excessive Miller capacitances for complete parasitic rejection may cause stability issue and thus smaller values were employed. In the case of the reference PA with shunt-inductive elements (PA2) shown in Fig. 3.7(b), uniform V_{ds}'s and improved PAE of 72.9% were achieved at P_{out} = 33 dBm, which is the maximum achievable PAE when the harmonic termination is not considered. However, the harmonic-tuned PA (PA3) achieved better PAE/DE (76.4/82.6%) and V_{ds} peaking by the optimized harmonic voltages, as shown in Fig. 3.7(c). On the other hand, the Class-F PA by shorting $Z_{D,k(2)}$'s and opening $Z_{D,k(3)}$'s exhibited poor performance in terms of PAE (53.2%) and P_{out} (30 dBm), as shown in Fig. 3.7(d). Since the quadruple-stacked PA works with V_{DD} = 4 V, each FET occupies V_{DC} = 1 V and thus the maximum V_{ds} of each FET reaches to 2 V only, resulting in reduced V_{ds} swing and P_{out} [38]. Thus, it is validated that the Class-F^{-1} is a proper operation mode for low-V_{DD} watt-level stacked-FET PA compared to the Class-F mode.

Fig. 3.8 shows the simulated load-line, gain, and PAE of the designed PA. The harmonic-tuned PA exhibits the best performance in terms of voltage swing (P_{out}) and PAE. The impact of the harmonic termination gets larger when designing a PA operating at higher frequency (f_0 > 1.7 GHz).

3.3.2 Experimental Validation

To verify the usefulness of the proposed harmonic termination, a 0.9 GHz

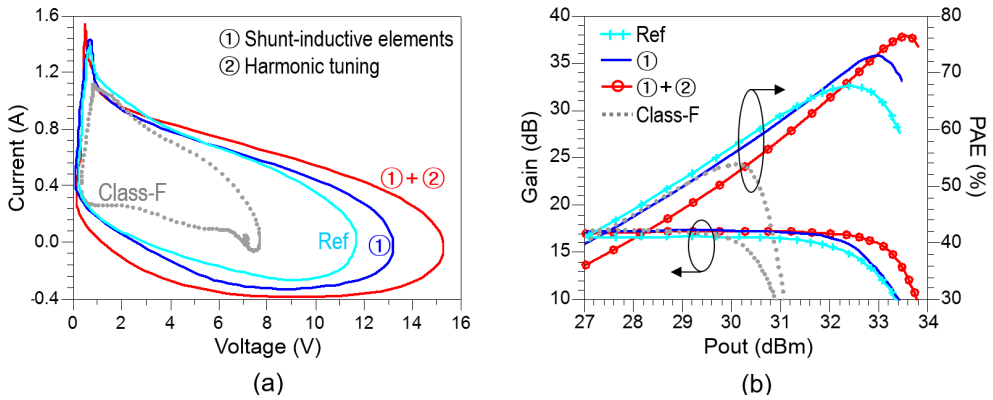


Figure 3.8: Harmonic-balance simulation results of the harmonic-tuned PA. (a) Load-line. (b) Gain and PAE.

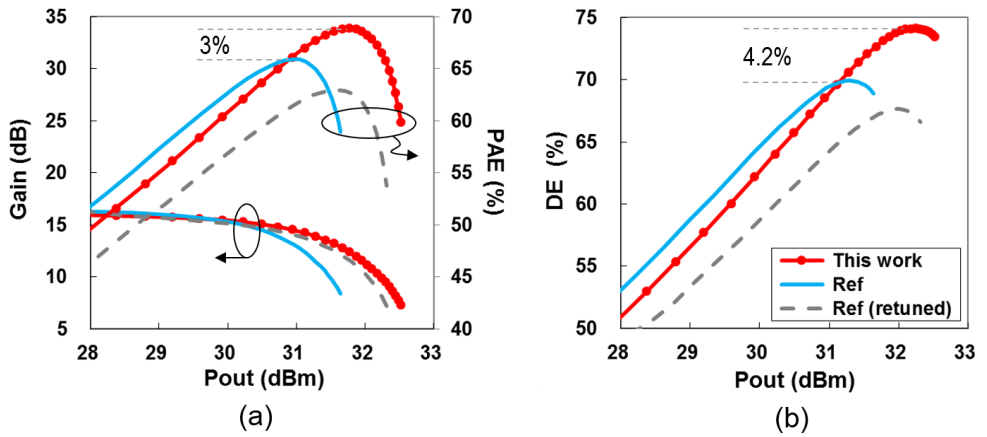


Figure 3.9: Measured CW results of the 0.9 GHz harmonic-tuned PA. (a) Gain and PAE. (b) Drain efficiency (DE).

stacked-FET PA was implemented and measured. The fabricated SOI CMOS PA IC was mounted on a 400-μm thick FR4 PCB ($\varepsilon_r \approx 4.6$, $\tan\delta = 0.025$) and bond-wires were used for harmonic termination (L_{H2}'s in Fig. 3.5). The shunt inductive elements (in Fig. 3.5) were not used in the implementation. Measurement results using CW signal are plotted in Fig. 3.9. The proposed harmonic-tuned PA showed maximum PAE of 69% and DE of 74.2% at P_{out} = 32 dBm. Compared to the reference PA without harmonic termination, P_{out} and PAE / DE were improved by

1 dB and 3 / 4.2%, respectively. In addition, compared to the re-tuned reference PA to obtain identical P_{out} to the proposed PA, PAE / DE improvements of +6 / 6.6% were achieved, thus validating the usefulness of the harmonic termination.

3.4 Control of the Gate Bias Modulation Effect

This chapter discusses the gate bias modulation (fluctuation) effect of a stacked-FET PA. Since most CMOS PAs employ a common-source (CS) amplifier as a first amplification stage, PA linearity and efficiency are strong functions of the gate bias of a CS amplifier. When a non-constant envelope signal (e.g. two-tone) is used, the nonlinearity of NFET induces baseband-level nonlinear current/voltage and thus they work as an effective gate bias combined with the external dc bias. Analysis and measurement show that the gate bias modulation should be rejected or can be utilized for better linearity under a certain condition.

3.4.1 Analysis

PA nonlinearity is characterized as the intermodulation distortion (IMD), and it comes from the AM-AM and AM-PM distortions [41]-[44]. Since most of the modern handset PAs are operated with non-constant envelope signals, the dynamic AM-AM and AM-PM can exhibit different behavior (including dispersions) to the static AM-AM and AM-PM. Therefore, it is worthwhile to analyze the difference between the static and dynamic behaviors for linear PA design. As described in [45]-[49], the IMD asymmetry (memory effect) comes from the second-order nonlinearity regarding the impedance termination at baseband / second-harmonic frequencies, of which the baseband impedance has more dominant effect. Since the gate of a CS amplifier is not frequently terminated at baseband whereas its drain node is mostly terminated with a bias-line and a micro-farad-level bypass capacitor [50], we have focused on the second-order nonlinearity by the gate-source

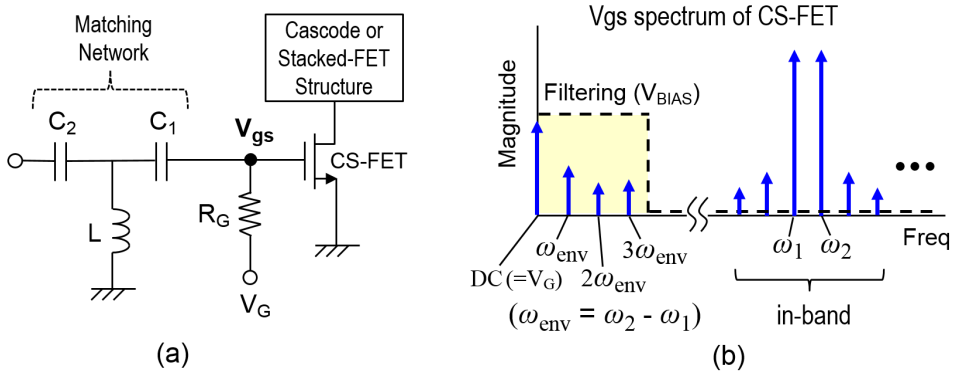


Figure 3.10: (a) Input schematic of the output-stage of a stacked-FET CMOS PA. (b) Typical gate voltage (V_{gs}) spectrum profile of the CS amplifier under the two-tone input condition, where V_{BIAS} means the effective gate-bias voltage.

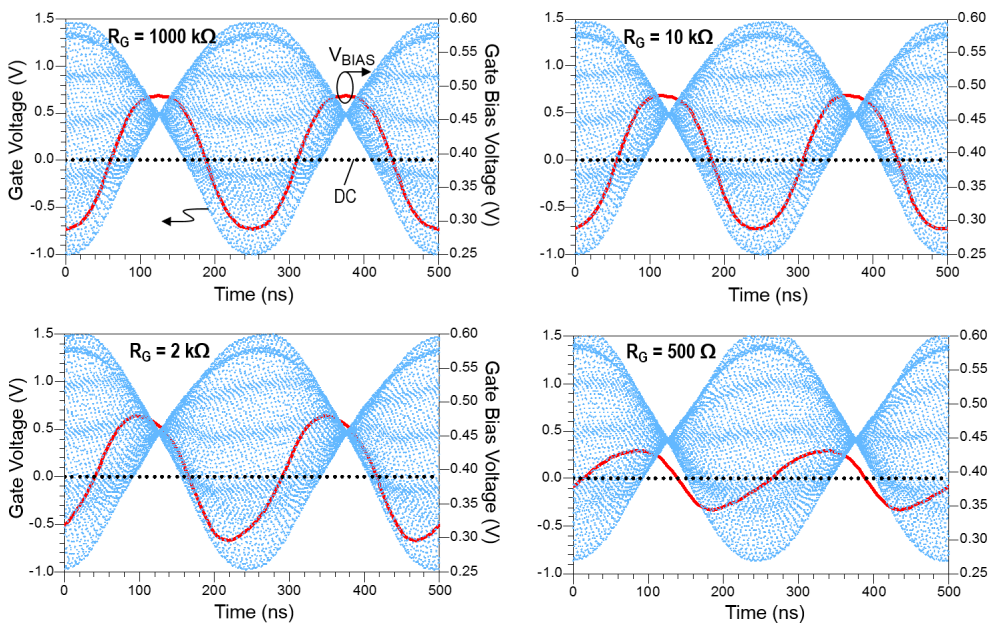


Figure 3.11: Simulated V_{gs} and V_{BIAS} waveforms for different R_G's at P_{out} = 28.2 dBm ($\approx P_{0.5dB}$).

capacitance (C_{gs}).

To analyze the gate impedance termination effect, a quadruple stacked-FET PA in Fig. 3.3 was simulated at 1.88 GHz using the two-tone harmonic balance

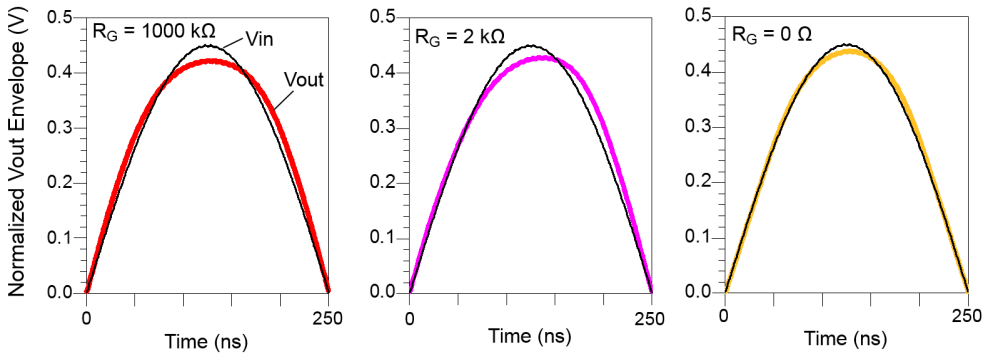


Figure 3.12: Simulated output two-tone envelope for different R_G's at $P_{0.5dB}$. An inductor of 30-nH was used for R_G = 0 Ω.

(tone spacing = 4 MHz). Fig. 3.10(a) shows a simplified input schematic of the output-stage, where the gate of a CS amplifier is biased to V_G through a resistor, R_G. When the PA is operated near soft compression region (~P_{1dB}), the gate voltage (V_{gs}) contains many harmonic and intermodulation components as well as the fundamental signal components, as shown in Fig. 3.10(b). Once the RF components (including in-band signals) of V_{gs} are completely filtered out, the remaining baseband-frequency components, which play a role of "effective" gate bias, V_{BIAS}, is extracted. The simulated V_{gs} and V_{BIAS} waveforms at $P_{0.5dB}$ of the PA for the case of R_G = 1000, 10, 2, and 0.5 kΩ are plotted in Fig. 3.11. As one can see from the result in Fig. 3.11, V_{BIAS}'s of the four cases are not constant to V_G but fluctuated. Also, the phase of V_{BIAS} for R_G = 1000 kΩ case is approximately –180˚ with respect to the input two-tone envelope. Due to the V_{BIAS} with opposite phase to the input envelope, the transconductance (G_m) of the CS amplifier becomes lower at high envelope and higher at low envelope. This bias modulation causes a compression of the output envelope and thus it deteriorates IMD.

Since most handset PAs are operated at RF frequencies, R_G of greater than 1 kΩ is usually considered to be a proper choice to block RF signal. As R_G value is decreased, however, V_{BIAS} profile is changed; the phase of V_{BIAS} strongly deviated

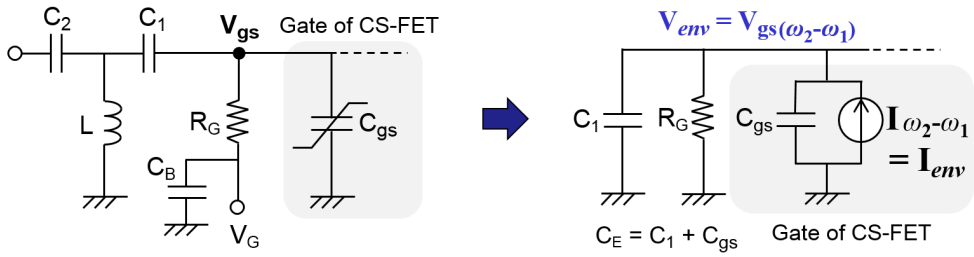


Figure 3.13: Simplified input equivalent circuit of the output stage to analyze V_{BIAS} modulation effect at the envelope frequency ($\omega_{env} = \omega_2 - \omega_1$).

from –180˚ while its fluctuation amplitude is decreased, as shown in Fig. 3.11. This phase deviation causes a significant IMD asymmetry, since the upward input envelope (↗) is amplified at low V_{BIAS} whereas the downward (↘) input envelope is amplified at high V_{BIAS}. To remove V_{BIAS} fluctuation, an RF choke inductor can be employed instead of R_G. The normalized input and output envelopes of the PA as a function of R_G are plotted in Fig. 3.12. It should be noted that R_G = 2 kΩ shows a significant envelope asymmetry between the upward and downward envelopes. In the case of R_G = 0 Ω, it does not cause the asymmetry and compression, compared to the other two cases.

The effect of R_G on V_{BIAS} modulation described above is originated from the C_{gs} nonlinearity of a CS-FET, which is known as one of the major nonlinear sources in CMOS PA [8]. The effect can be modeled as an RC network with nonlinear current source (I_{env}) at envelope (two-tone difference) frequency, as shown in Fig. 3.13. The nonlinear current (I_{env}) is induced by the second-order intermodulation (IM2) of C_{gs}, which is related to the second-order derivative term of C_{gs}. Thus, the non-constant V_{BIAS} can be represented as

$$V_{BIAS} = V_{G(DC)} + V_{env(1\omega.env)} + V_{env(2\omega.env)} + V_{env(3\omega.env)} + \cdots \qquad (3.1)$$

where $V_{G(DC)}$ is the dc gate bias voltage, and V_{env}'s are the envelope frequency and its harmonic voltage components. The magnitude and phase of the fundamental

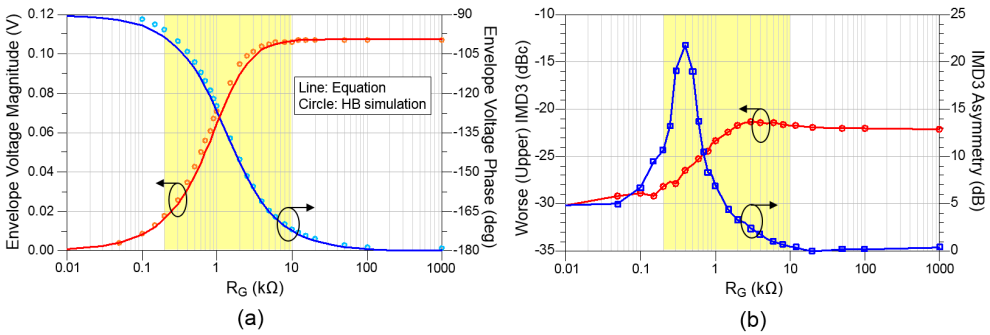


Figure 3.14: (a) Calculated/simulated magnitude and phase of V_{BIAS} as a function of R_{G} at $P_{0.5\mathrm{dB}}$. (b) Simulated worst IMD3 and IMD asymmetry.

envelope voltage ($V_{\mathrm{env}(1\omega.\mathrm{env})}$) is calculated as

$$|V_{env}| = \left| \frac{I_{env}}{1/R_G + j\omega_{env} C_E} \right| \tag{3.2}$$

$$\angle V_{env} = \tan^{-1}(I_{env}) - \tan^{-1}(\omega_{env} C_E R_G) \tag{3.3}$$

where $C_{\mathrm{E}} = C_1 + C_{\mathrm{gs}}$ and $\tan^{-1}(I_{env}) = -90^{\circ}$. It should be noted in (3.2) and (3.3) that as R_{G} is decreased, the magnitude of V_{env} is reduced toward zero whereas its phase moves toward –90˚, as shown in Fig. 3.11. The calculated magnitude/phase of V_{env} and simulated third-order IMD (IMD3) as a function of R_{G} at $P_{0.5\mathrm{dB}}$ are plotted in Fig. 3.14. The CS-FET device of this design has a gate-width of 20 mm (which corresponds to $C_{\mathrm{gs}} \approx 22$ pF) and the matching capacitance of C_1 is 9 pF, thus resulting in the effective capacitance (C_{E}) of 31 pF. Also, $I_{env} = -j81\ \mu$A was used in the calculation. The calculated $|V_{env}|$ and $\angle V_{env}$ in Fig. 3.14(a) are almost identical to the simulated results. As R_{G} gets smaller, IMD3 in Fig. 3.14(b) is getting improved due to smaller $|V_{env}|$. On the other hand, in the range of $R_{\mathrm{G}} = 0.2 \sim 10$ kΩ where the phase is deviated from –180˚ to –90˚, IMD3 asymmetry is significantly increased. Since the memory effect is very difficult to be rejected by predistortion, R_{G} value of 0.2 ~ 10 kΩ must not be used.

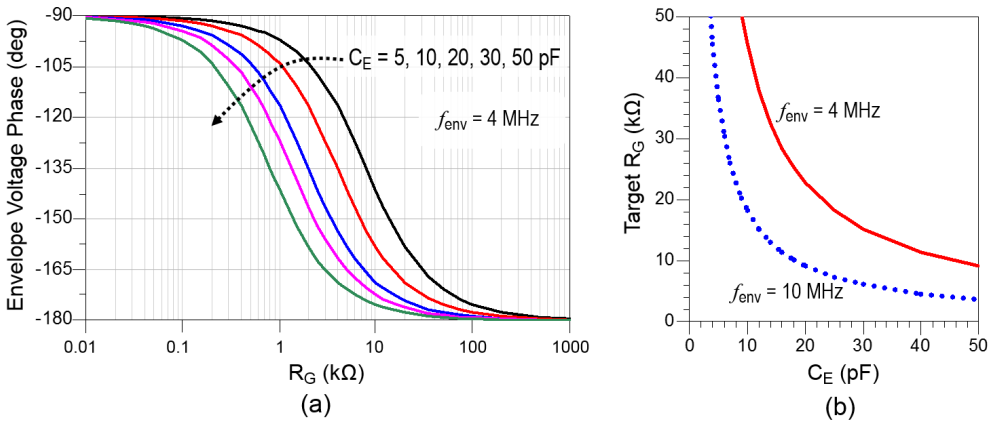


Figure 3.15: (a) Calculated V_{BIAS} phase as a function of R_G for various C_E's. (b) Target R_G to achieve V_{BIAS} phase of –175˚ to avoid IMD asymmetry.

Based on the analysis above, it seems that providing short-circuited gate impedance at baseband frequency is the only solution to avoid the bias modulation effect and improve the linearity. However, in some cases, the gate bias modulation effect can be utilized to suppress the excessive AM-AM expansion near high envelope, thus achieving linearity improvement. This is valid only if $|V_{env}|$ is not excessive and $\angle V_{env}$ does not cause a memory effect. Since IMD asymmetry is dependent on R_G, there is a reference guide in determining R_G value. Fig. 3.15(a) shows the phase of V_{env} as a function of R_G for various C_E's. If the phase is –180˚, the induced envelope voltage is inversely symmetric to the input two-tone envelope, and thus the memory effect arisen from R_G is avoided. Assuming that the target phase, $\angle V_{env.T}$, is lower than –175˚, the target gate resistance (R_{GT}) is calculated from (3.3) as

$$R_{GT} \geq \frac{-\tan(\angle V_{env.T} + 90°)}{\omega_{env} C_E} = \frac{\tan(85°)}{\omega_{env} C_E}. \tag{3.4}$$

The calculated R_{GT} value of this design is ~15 kΩ (C_E = 31 pF, f_{env} = 4 MHz), whose criterion is consistent with the result in Fig. 3.15(b).

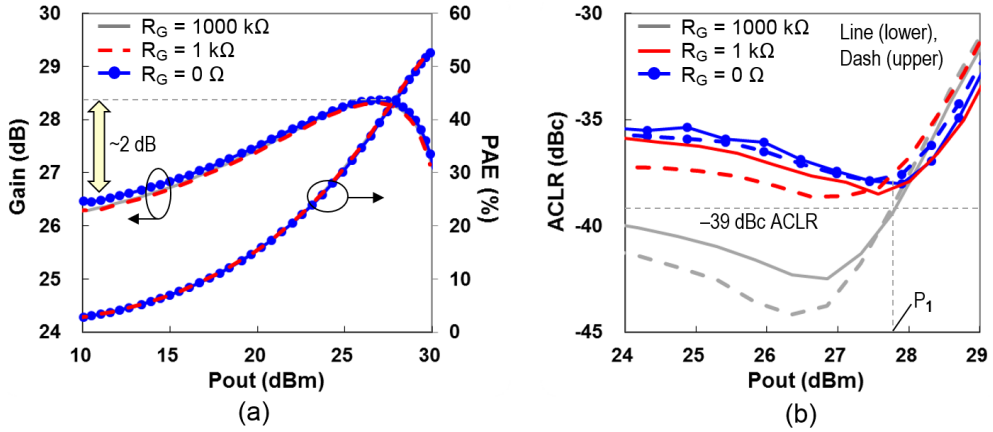


Figure 3.16: Measured W-CDMA results of the low-band (0.9 GHz) stacked-FET CMOS PA for different R_G's at I_Q = 77 mA. (a) Gain and PAE. (b) ACLR.

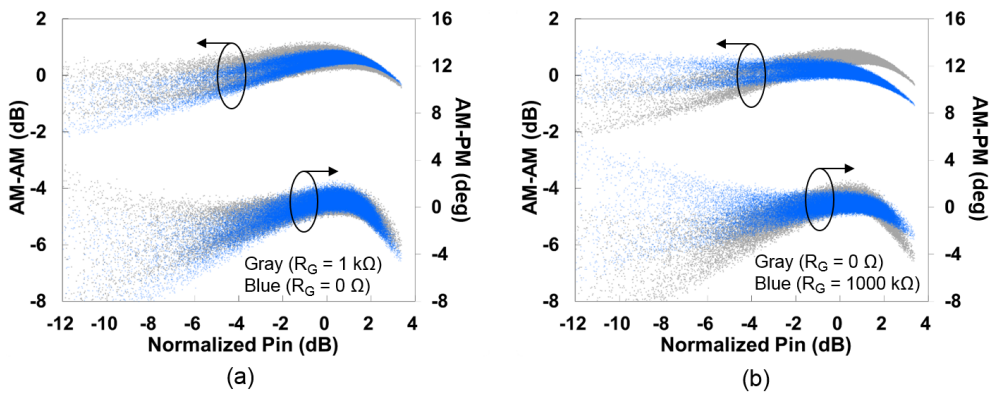


Figure 3.17: Measured dynamic AM-AM and AM-PM of the 0.9 GHz PA for different R_G's at I_Q = 77 mA and P_{out} = 27.8 dBm (=P_1 in Fig. 3.16(b)). (a) R_G = 1 kΩ vs. 0 Ω. (b) R_G = 0 Ω vs. 1000 kΩ.

3.4.2 Experimental Validation

To investigate the gate bias modulation effect in experimental level, two stacked-FET CMOS PAs, each for low-band (LB: 0.9 GHz) and high-band (HB: 1.88 GHz), were fabricated and measured using the 3GPP uplink W-CDMA (Rel'99) signal. The purpose of the LB PA is to demonstrate that the gate bias

modulation effect can be utilized for linearity improvement, whereas it cannot be utilized but be rejected for the HB PA.

A. Bias Modulation of a CS-FET for a Low-Band (0.9 GHz) PA

First, a 0.9 GHz PA with different R_G's (=1000, 1, 0 kΩ) was measured. Fig. 3.16 shows the measured gain, PAE, and ACLR of the PA at quiescent current (I_Q) of 77 mA. In the case of gain and PAE, the three results are almost identical. However, the PA showed different ACLR behaviors; the PA with R_G = 1000 kΩ showed better linearity (<–39 dBc) whereas the other two cases showed worse linearity near mid ~ high P_{out} region, as shown in Fig. 3.16(b). In reality, the gain expansion of greater than 2 dB shown in Fig. 3.16(a) is not acceptable, since such a large gain deviation cannot achieve high linearity (W-CDMA ACLR < –39 dBc) in the mid ~ high P_{out} region. Nevertheless, the PA with R_G = 1000 kΩ achieved good linearity in aid of the induced gate envelope voltage (V_{env}). This explanation is validated from the measured dynamic AM-AM and AM-PM. As shown in Fig. 3.17(a), the PAs with R_G = 1 kΩ and 0 Ω show gain and phase expansions, of which the gain slope is quite similar to that one in Fig. 3.16(a). It should also be noted in Fig. 3.17(a) that the PA with R_G = 1 kΩ exhibits more dispersive AM-AM behavior than the PA with R_G = 0 Ω, thus causing more ACLR (IMD) asymmetry, as shown in Fig. 3.11, 3.12 and 3.16(b). On the other hand, the PA with R_G = 1000 kΩ in Fig. 3.17(b) shows quite flat AM-AM and AM-PM than the other cases, even with the 2-dB gain expansion shown in Fig. 3.16(a).

Since the PA with R_G = 0 and 1 kΩ shows gain and phase expansions, the expansion can be mitigated by providing higher I_Q. Measurement showed that the PA with R_G = 0 Ω requires I_Q = 103 mA to achieve ACLR < –39 dBc over the entire linear P_{out} region. The ACLR characteristics as a function of R_G's for different I_Q are plotted in Fig. 3.18.

To investigate the memory effect of the PA, maximum linear P_{out} (meeting

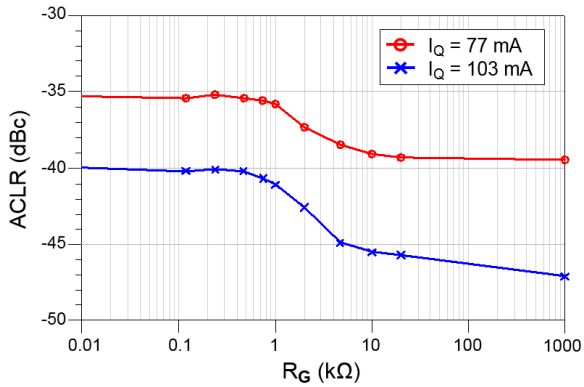


Figure 3.18: Measured W-CDMA ACLR of the 0.9 GHz PA at P_{out} = 27.8 dBm.

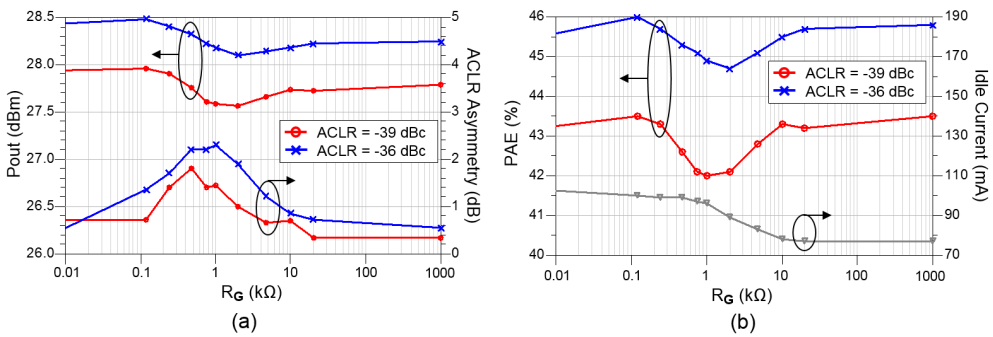


Figure 3.19: Measured W-CDMA characteristics of the 0.9 GHz PA meeting ACLR = –39 / –36 dBc at high P_{out}. The idle current (I_Q) of each R_G condition is adjusted to obtain ACLR < –39 dBc over the entire P_{out} region. (a) Maximum P_{out} and ACLR asymmetry. (b) Maximum PAE and I_Q condition.

ACLR = –39 dBc), ACLR asymmetry, PAE, and idle current (I_Q) of the PA are plotted in Fig. 3.19. In this measurement, I_Q is adjusted for each R_G to obtain ACLR (worst case between the lower/upper-side ACLRs) < –39 dBc over the entire linear P_{out} region. From the results, three analyses are inferred as follows:

① To avoid ACLR asymmetry and linear PAE degradation, R_G of 0.2 ~ 10 kΩ must not be used. This is consistent with the simulated result in Fig. 3.14(b).

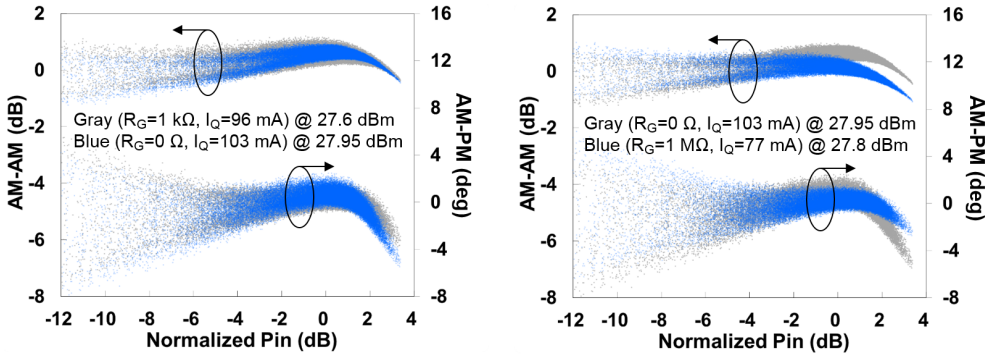


Figure 3.20: Measured dynamic AM-AM and AM-PM of the 0.9 GHz PA for different R_G's at I_Q / P_{out} meeting ACLR = –39 dBc. (a) R_G = 1 kΩ versus 0 Ω. (b) R_G = 0 Ω versus 1000 kΩ.

② The PA with R_G = 0 Ω shows more linear P_{out} and thus similar level of linear PAE is achieved even with higher I_Q (=103 mA), compared to the case with R_G = 1000 kΩ and I_Q = 77 mA.

③ R_G of greater than 20 kΩ shows almost no IMD asymmetry and good performance while maintaining low I_Q. This resistance is quite similar to the criterion $R_{GT} \geq$13 kΩ from Equation (3.4), where $C_E = (C_1 + C_{gs})$ = (15 + 22) = 37 pF and f_{env} = 3.84 MHz for 0.9 GHz W-CDMA PA.

Fig. 3.20 shows the dynamic AM-AM and AM-PM of the PA for different R_G and I_Q (meeting ACLR = –39 dBc). By providing higher I_Q to the PA with R_G = 0 Ω, its dynamic characteristics is flattened, compared to the result in Fig. 3.17(a).

B. Bias Modulation of CG-FETs for a Low-Band (0.9 GHz) PA

In the stacked-FET PA, the CS (bottom) FET performs as a current amplifier while the upper (CG) FETs work as current buffers. Even if the gate bias modulation of the CS amplifier is dominant, it is worthwhile to investigate the modulation effect by the CG-FETs. For this purpose, the gates of CG-FETs are terminated at envelope frequency using the small resistors (100 ~ 200 Ω) and large

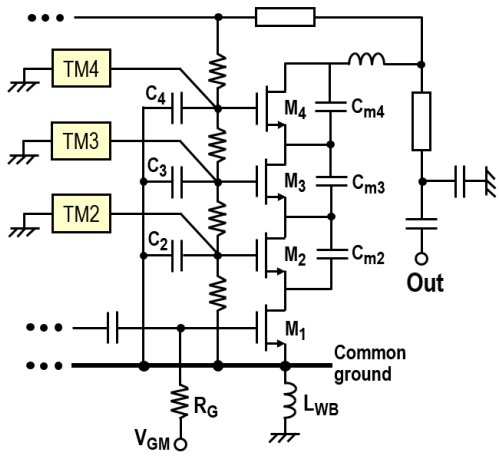


Figure 3.21: Gate envelope impedance termination of common-gate (CG) FETs. To avoid the gate capacitance mismatch of C_2 ~ C_4 at RF frequency, a resistor with low value (100 ~ 200 Ω) and a large capacitor (1 uF) connected in series are used for TM2 ~ TM4.

TABLE 3.1
MEASUREMENT SUMMARY OF THE 0.9 GHZ PA ACCORDING TO GATE ENVELOPE IMPEDANCE TERMINATION OF CG-FETS

	ACLR (dBc)	I_Q (mA)	P_{out} (dBm)	PAE (%)	P_{out} / PAE ↑
CS.R_G=1M (no CG term)	–39	77	27.78	43.5	Reference
CG2 term	–39	83	27.91	43.9	0.13 dB / 0.4%
CG3 term	–39	79	27.85	43.8	0.07 dB / 0.3%
CG23 term	–39	86	27.93	44.0	0.15 dB / 0.5%

capacitors (1 uF), as shown in Fig. 3.21. Since C_4 is smaller than C_2 and C_3, the envelope terminations of CG-FETs are performed for M_2 and M_3 only.

The measured results are summarized in Table 3.1. As shown in the table, gate termination of CG-FETs at envelope frequency requires higher I_Q than the case without CG termination, and maximum linear P_{out} and PAE are slightly increased. This means that the CG-FETs also experience the gate bias modulation by the C_{gs}

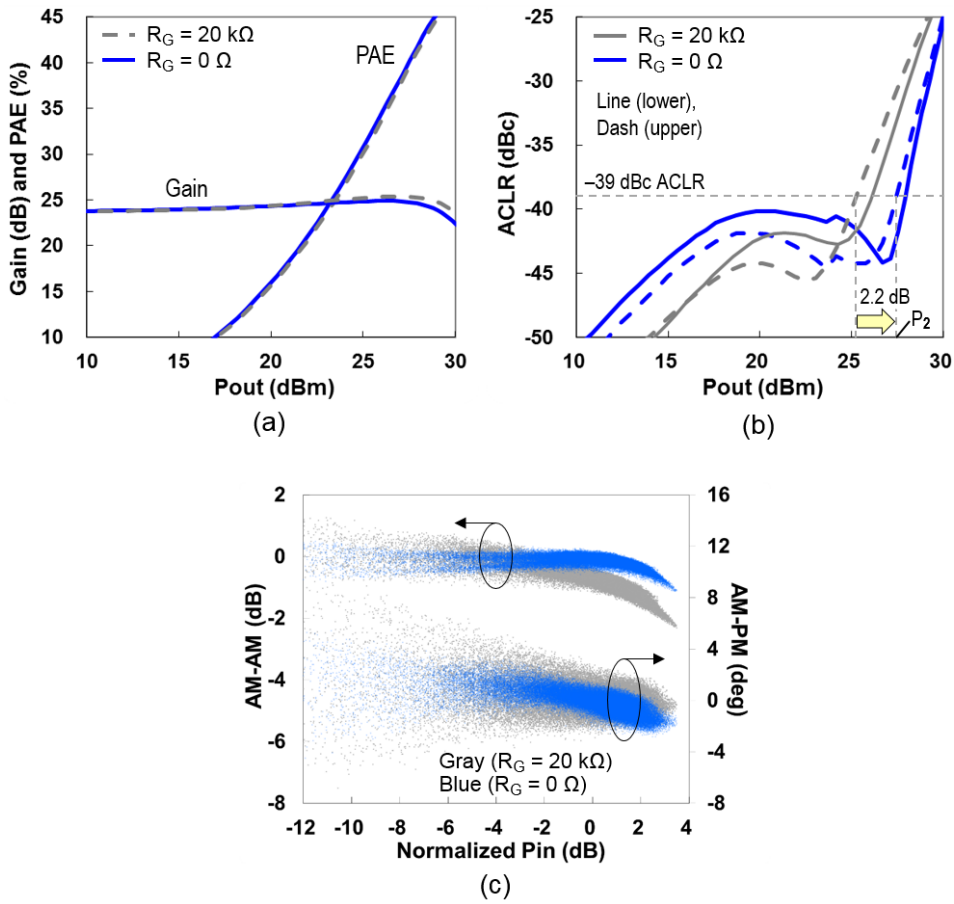


Figure 3.22: Measured W-CDMA results of the high-band (1.88 GHz) stacked-FET CMOS PA for different R_G's at I_Q = 91 mA. (a) Gain and PAE. (b) ACLR. (c) Dynamic AM-AM and AM-PM at P_{out} = 27.5 dBm (= P_2).

nonlinearity. The final result with CG-2 and CG-3 termination showed linear P_{out} / PAE improvements of 0.15 dB / 0.5%, compared to the case without CG termination. Since the amount of linear PAE improvement is relatively small and a large capacitor (micro-farad level) is required, the LB linearized PA presented in Chapter 3.7 does not use the CG-termination.

C. Bias Modulation of a CS-FET for a High-Band (1.88 GHz) PA

Contrary to the LB (0.9 GHz) PA described above, the HB (1.88 GHz) PA showed a significant difference between the cases of low R_G and high R_G. Fig. 3.22

shows the measured W-CDMA results of the HB PA. The PA with R_G = 0 Ω showed ACLR = –39 dBc at P_{out} = 27.5 dBm, whereas the PA with R_G = 20 kΩ exhibited poor linearity (–31.5 dBc) at the same P_{out}, which means the maximum linear P_{out} is increased by 2.2 dB by the termination. Maximum linear PAEs at output powers meeting –39 dBc ACLR of the two cases are 40.3% and 31.6%, respectively. This results obviously show that the gate bias modulation effect of the 1.88 GHz PA is too excessive to be utilized for linearity improvement, contrary to the 0.9 GHz PA. As one can see from the dynamic AM-AM and AM-PM results in Fig. 3.22(c), this phenomenon can be inferred as follows: Since the HB PA has 3 ~ 4-dB smaller power gain than the LB PA, the RF input power drive becomes higher, resulting in increase of the nonlinear IM2 current (I_{env} in Fig. 3.13). Also, C_E of the HB PA is smaller than that of the LB PA (31 versus 37 pF), which makes V_{env} increase by a factor of 1.2 from Equation (3.2). Thus, the resultant $|V_{env}|$ becomes larger that the signal envelope is excessively compressed. Without gate envelope impedance termination of the 1.88 GHz PA, any linearization technique could not improve the RF performance of the PA.

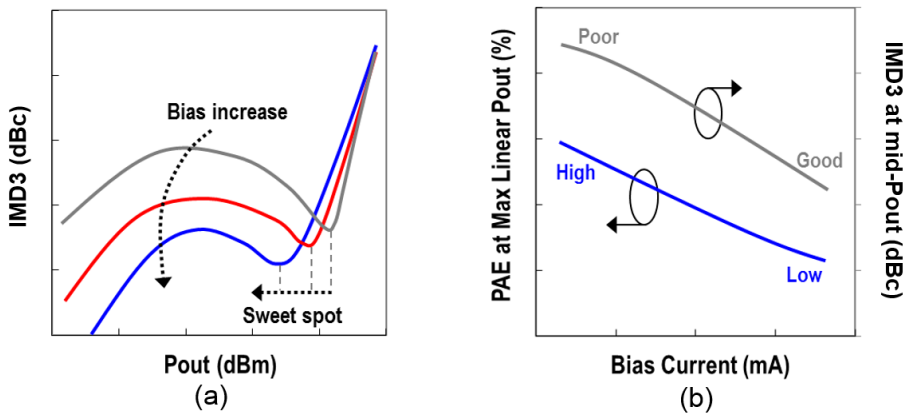


Figure 3.23: Typical characteristics of the CMOS PA according to bias current (I_Q). (a) IMD3. (b) PAE at maximum linear P_{out} and ACLR at mid-P_{out}.

3.5 Proposed Linearization #1: Hybrid Bias

Due to the large-signal nonlinear transconductance (G_m) behavior of a CMOS device, the IMD sweet spot of a CS amplifier moves to higher P_{out} level when the bias current (I_Q) gets lower, as described in [22], [23]. Thus, the bias point should be selected close to deep Class-AB region to maximize linear PAE. However, low I_Q gives rise to poor linearity in the mid P_{out} region where AM-AM and AM-PM are excessively expanded, as illustrated in Fig. 3.23. This is a dilemma in designing a linear CMOS PA. Since the linearity and efficiency of 3G/4G handset PAs cannot be compromised, a proper biasing approach, which provides high I_Q at mid P_{out} level and low I_Q at high-P_{out} level, is required to obtain good linearity over the entire output power regions while maximizing linear PAE. Even if Kousai *et al* [15] implemented a desirable dc bias profile, however, it requires complex PA-closed loop circuit.

To resolve the problem, a simple dc bias circuit is proposed. The circuit employs two bias circuits having different dc bias profiles, a diode bias and a resistor bias, and thus it is called as the "hybrid bias" circuit. Fig. 3.24 shows the

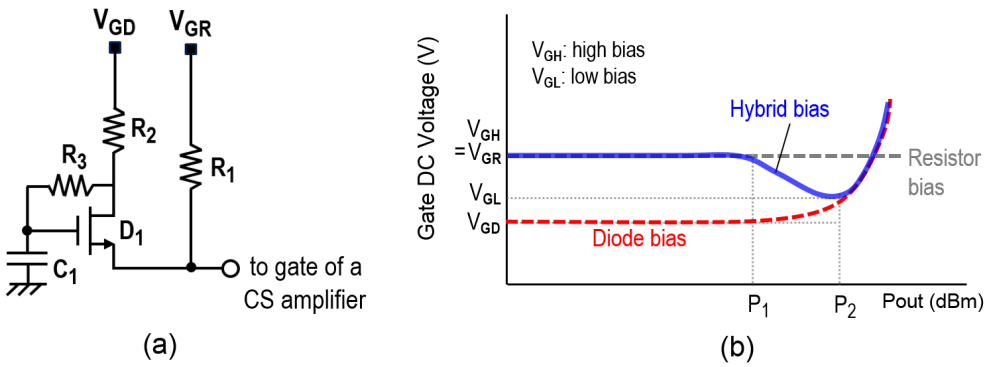


Figure 3.24: (a) Schematic of the proposed hybrid bias circuit. (b) Gate dc voltage profile by the hybrid bias.

schematic and dc gate voltage profile of the hybrid bias circuit. As described in [9]-[11], the diode bias is capable of boosting dc gate bias as the incident RF power is increased above the turn-on level of the diode. On the other hand, the resistor bias provides a constant dc gate bias irrespective of RF power level. The hybrid bias combines the power-dependent bias characteristics of both diode and resistor biases to achieve the bias profile as a function of P_{out}, as shown in Fig. 3.24(b). It should be noted that V_{GR} (resistor bias) should be set higher than V_{GD} (diode bias). Even if the circuit topology is similar to [51], however, the work [51] cannot achieve the negative slope due to the applied bias condition of $V_{GR} < V_{GD}$.

During $P_{out} < P_1$ (in Fig. 3.24(b)) where the RF voltage swing does not exceed the threshold voltage of the diode, the diode is in off-state and the gate dc bias voltage is identical to V_{GR}. When P_{out} is between P_1 and P_2, the diode is partially turned on, and the resultant gate dc bias voltage becomes a combination of V_{GR} and V_{GD}. Thus, the gate dc bias voltage is decreased and finally reaches the targeted level, V_{GL}, at $P_{out} = P_2$, where the two bias voltages (by the hybrid bias and standalone diode bias) coincide. It is worthwhile to note that V_{GL} is not the same as V_{GD}. Finally, when P_{out} exceeds P_2, the incident RF swing further boosts the gate bias through the diode action, resulting in the bias voltages higher than V_{GR}. The

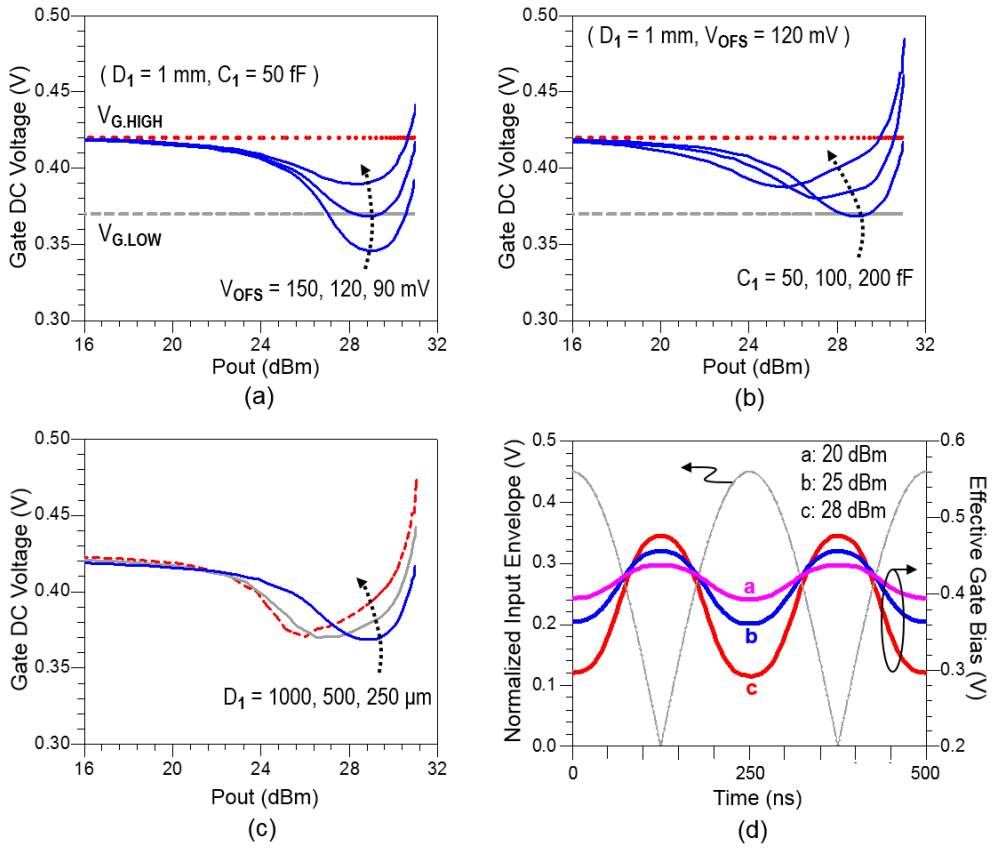


Figure 3.25: Two-tone simulation results of the CMOS PA using the hybrid bias circuit. (a) Offset voltage (V_{OFS}) dependency. (b) Capacitance (C_1) dependency. (c) Diode size (D_1) dependency. (d) Effective gate bias (V_{BIAS}) at time-domain when the gate envelope impedance is not terminated.

target rated linear P_{out} of a PA can be chosen to be P_2. The required gate dc voltage difference of CS CMOS amplifiers, $V_{GH} - V_{GL}$ in Fig. 3.24(b), is usually less than 50 mV.

The target values, $V_{GH} - V_{GL}$ and P_2, are mostly determined by the three design parameters: V_{OFS} (=$V_{GR} - V_{GD}$), C_1, and D_1. To investigate the effects of the parameters, a 0.9 GHz two-stage stacked-FET PA, in which the hybrid bias is employed for the output-stage, was simulated and the result is plotted in Fig. 3.25. As one can see from Figs. 3.25(a) ~ 3.25(c), the target voltage difference (=V_{GH} –

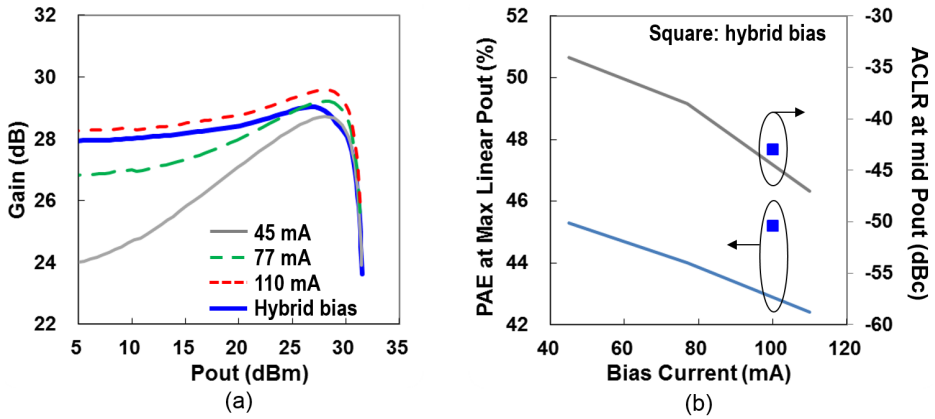


Figure 3.26: Measured characteristics of the CMOS PA using the hybrid bias circuit. (a) Gain. (b) PAE at maximum linear P_{out} meeting –39 dBc ACLR and ACLR at mid P_{out}.

V_{GL}) is a strong function of V_{OFS}, and the target P_{out} (=P_2 in Fig. 3.24(b)) can be adjusted by resizing D_1. The capacitor, C_1, can be placed at the drain of D_1 to reduce the sensitivity from the small capacitance (50 ~ 200 fF) and plays a role of adjusting $V_{GH} - V_{GL}$ and P_2. The effective gate bias (V_{BIAS}) of the PA without gate envelope impedance termination is plotted in Fig. 3.25(d), where the dc component of V_{BIAS} is reduced as P_{out} is increased (note that dc component of "c"-curve in Fig. 3.25(d) is lower than "a"-curve). Due to the nonlinear C_{gs}, envelope components of V_{BIAS} are nonzero, thus fluctuating V_{BIAS}. Since the diode (D_1) is operated at off-state, the impedance seen to the hybrid bias circuit at envelope frequency is very large and thus the circuit causes no IMD asymmetry.

To demonstrate the usefulness of the hybrid bias, the circuit was employed for the main-stage of a 0.9 GHz SOI CMOS stacked-FET PA. D_1 and C_1 in Fig. 3.24 were chosen to have a gate-width of 250-μm and capacitance of 100 fF, respectively. To mitigate the sensitivity, C_1 was connected at the drain of D_1 instead of the gate node. Two bias voltages for the resistor and diode, V_{GR} and V_{GD}, were 0.34 V and 0 V (V_{OFS} = 0.34 V), respectively. To compare the result with the

PA without hybrid bias, a standalone PA, which has a resistor bias with low ~ high I_Q's (45 ~ 110 mA), was also measured. Fig. 3.26 shows the measured W-CDMA results. The PA with hybrid bias (I_Q = 100 mA) showed a gain deviation of less than 1 dB, which is smaller than that of the PA with a resistor bias of I_Q = 110 mA (1.4 dB). Also, PAE at maximum linear P_{out} (meeting –39 dBc ACLR) was as high as 45.2% while maintaining good ACLR (–43 dBc) at mid P_{out}. As shown in Fig. 3.26(b), PAE of the hybrid-biased PA (45.2%) is 2.8% higher than a standalone PA with high I_Q (42.4%) and comparable to that of the standalone PA with low I_Q (45.3%).

The proposed hybrid bias is effective to provide an optimum dc (static) gate bias profile according to power level. In subsequent chapter, another effective linearization method which is based on dynamic-level correction is presented.

3.6 Proposed Linearization #2: Phase Injection

3.6.1 Motivation

Since the linearization effect of the static-level linearizers (e.g. hybrid bias) is not enough for compensating the compressed signal envelope near saturated power region, several techniques based on envelope-level correction (e.g. adaptive bias) have been proposed for stronger linearity improvement [21], [22]. In [21], the compressed peak envelope near gain compression region was successfully corrected by providing an envelope-reshaped gate-bias voltage (V_{BIAS}) to a CS amplifier, thus improving AM-AM and IMD linearity. However, the amplitude injection (AI) technique may not correct (or even worse) for the AM-PM. Thus, it is worthwhile to provide further analysis why the AI gives rise to AM-PM compression for a stacked-FET PA of this work.

The capacitance and phase variations of a stacked-FET amplifier by the AI are plotted in Fig. 3.27. As shown in Fig. 3.27(a), the average C_{gs} of a CS amplifier

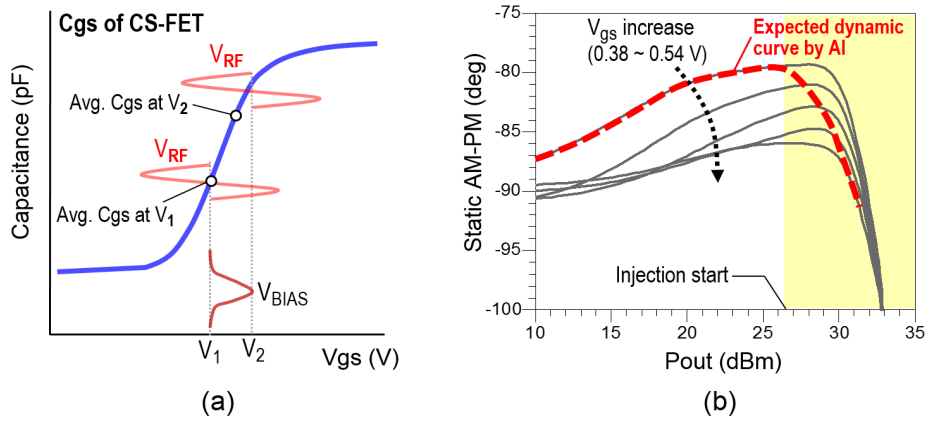


Figure 3.27: (a) C_{gs} of a CMOS CS amplifier as a function of gate bias. (b) Simulated static AM-PM for different gate biases and the expected dynamic AM-PM by the amplitude injection (AI).

biased at V_2 is larger than that biased at V_1 under the same RF voltage swing condition. This means that higher V_{BIAS} under large envelope swing results in larger C_{gs} and the phase is further compressed. This can be observed from the single-tone harmonic balance simulation result in Fig. 3.27(b), where the static AM-PM curves are plotted as the gate bias (V_{gs}) increases from 0.38 to 0.54 V. Considering that AI provides initial V_{BIAS} of 0.38 V (during low ~ mid P_{out}) and peak V_{BIAS} of 0.54 V (at compressed P_{out}), the expected dynamic AM-PM (dashed curve in red) shows early compression compared with the AM-PM with a fixed V_{gs} of 0.38 V. Moreover, even though the AI is provided during the small time-duration of the envelope signal, excessive V_{BIAS} causes higher dc current consumption at target P_{out}, thus resulting in PAE degradation. Due to the reason above, a phase-based linearization is required to correct for the dynamic AM-PM as well.

3.6.2 Phase (Capacitance) Injection

To recover the compressed dynamic AM-PM, a phase injection (PI) method is proposed in this work [32]. Fig. 3.28 shows the phase and capacitance variations of a shunt varactor to explain the PI mechanism. Since the typical AM-PM of the

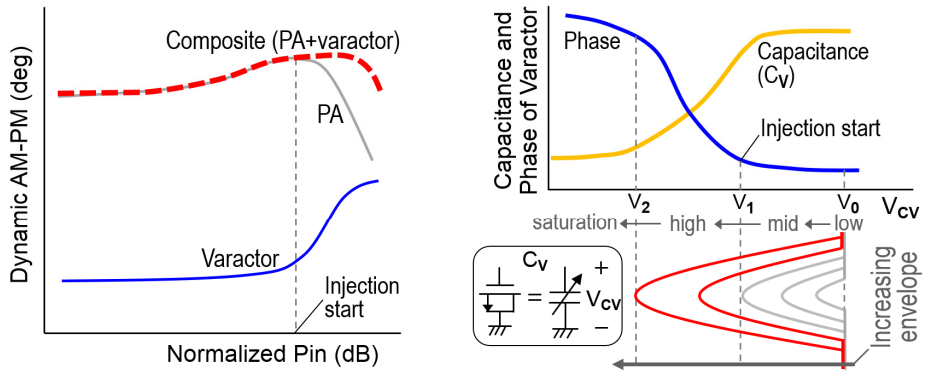


Figure 3.28: Operation of the phase injector. (a) Dynamic AM-PM curves with phase injection. (b) C_V and phase ($\angle S_{21}$) of the varactor as a function of V_{CV}.

CMOS PA shows compressive characteristics as shown in Fig. 3.28(a), the phase injector is required to provide positive slope versus the envelope, which requires negative capacitance slope. Thus, the voltage across the varactor (V_{CV}) is required to track the envelope signal in the opposite direction. The varactor is realized using MOS capacitor (n^+-implanted source/drain on n-well). During low ~ mid P_{out} region, V_{CV} stays between V_0 and V_1 in Fig. 3.28(b), where C_V is almost constant, resulting in little phase injection. When P_{out} is further increased, V_{CV} decreases below V_1, reaching V_2 at the maximum swing. Due to the reduced capacitance of the varactor, positive PI occurs in this region. Thus, the resultant dynamic AM-PM of the composite PA is flattened as shown in Fig. 3.28(a). Finally, when the PA enters strongly saturation, a limiting circuit prevents V_{CV} from decreasing below V_2.

The schematic of the proposed linear PA with PI is shown in Fig. 3.29. The envelope is detected at the power-stage input, and the envelope-reshaped capacitance (C_V) is generated by the PI circuit. C_V is injected to the gate of the driver-stage CS transistor. Since the gate-source capacitance of the output-stage CS-FET, $C_{gs.M0}$, is very large (~22 pF), C_V is injected to the driver-stage to avoid excessive capacitance loading (=$C_{gs.M0}$+C_V) of the power-stage. Envelope detection

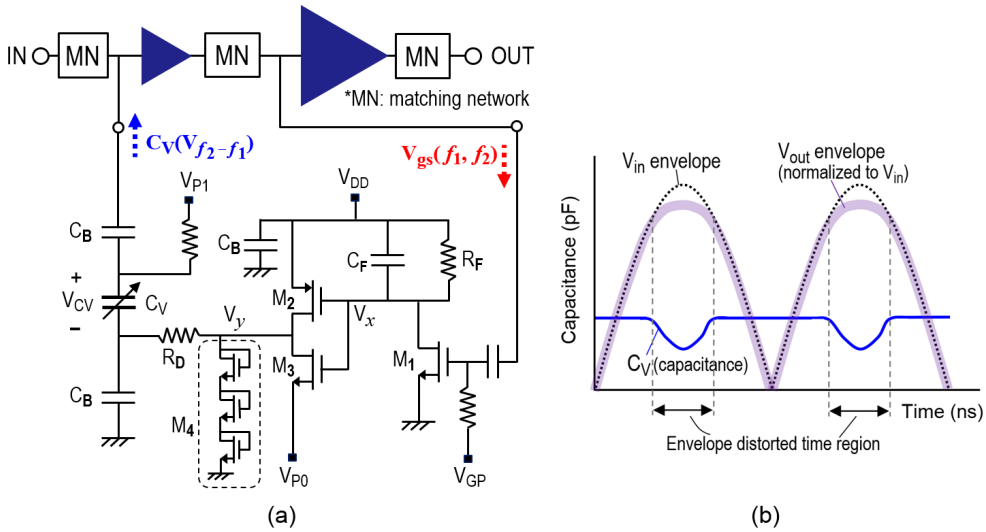


Figure 3.29: (a) Schematic of the phase injection (PI) circuit. (b) Capacitance (C_V) profile by the PI circuit (assumed two-tone input signal).

is performed using the common-source (CS) envelope detector (M_1, C_F, and R_F in Fig. 3.29(a)). Because the CS detector generates the output envelopes (V_x) in opposite phase to the input envelope, V_x is flipped again by the inverter-like envelope shaper (M_2 and M_3). The varactor is initially biased at V_{CV} (= $V_{P1} - V_{P0} >$ 0), and V_{CV} is dynamically decreased according to the amplitude of the input envelope, as shown in Fig. 3.29(b). This is achieved by applying the envelope-reshaped signal (V_y) to the cathode of the varactor. To avoid excessive voltage injection near saturation, a diode-connected limiter (M_4) is used.

It is worthwhile to note that the PI also improves AM-AM linearity since the dynamic C_V correction by the phase injector improves input matching at high power levels where AM-AM is compressed. Simulation shows that gain compression is reduced from 1.8 dB to 1 dB when the PI is applied. Thus, the AI circuit can be employed to work as an auxiliary correction to provide fine adjustment to AM-AM distortion. The required V_{BIAS} injection range becomes much smaller than that without PI [21], resulting in minimal efficiency degradation. The linearization effect of the circuit can be limited for wide bandwidth signal if the time delay

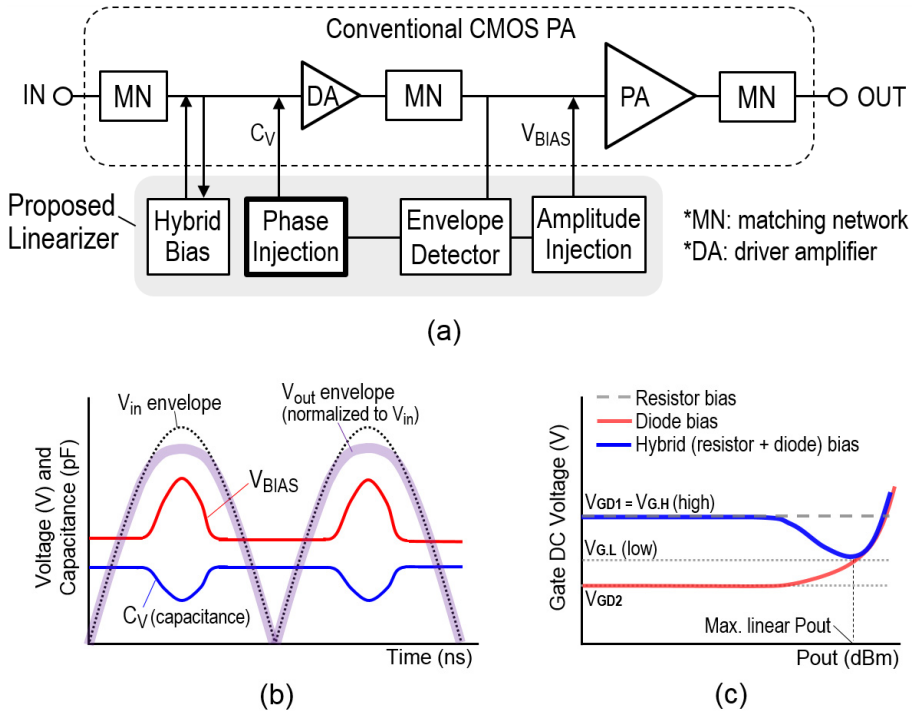


Figure 3.30: (a) Block diagram of the proposed linear CMOS PA. (b) Capacitance (C_V) and gate bias voltage (V_{BIAS}) profiles by the phase and amplitude injection circuits. (c) Gate DC voltage profile by the hybrid bias circuit.

between the incoming RF signal and PI/AI signals (C_V and V_{BIAS}) cannot be adjusted properly.

3.7 Linear CMOS PA Design

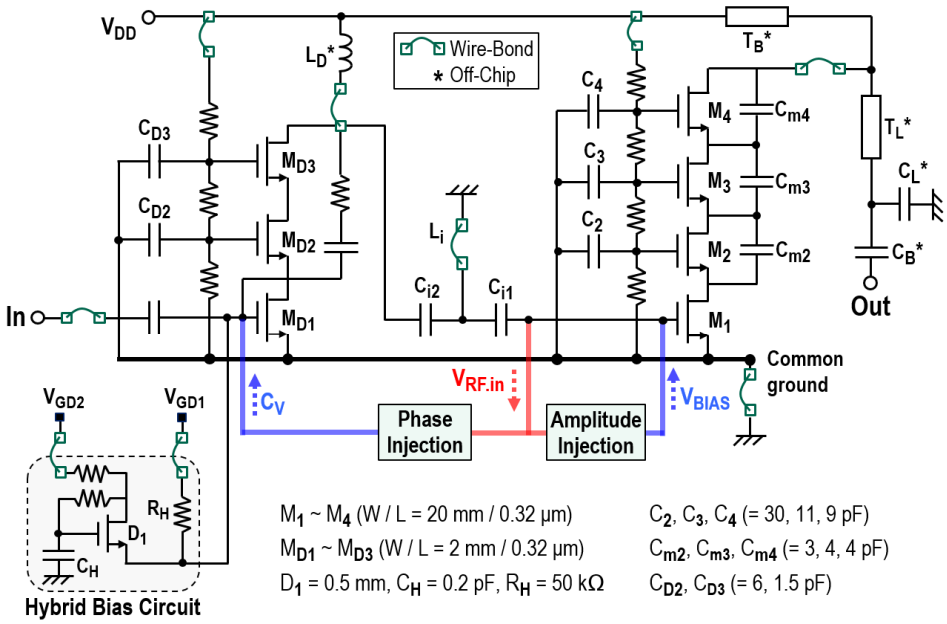
To demonstrate the performance of the proposed linearization techniques, two prototype 1.88 GHz and 0.9 GHz linear CMOS PAs are designed. Fig. 3.30(a) shows an overall block diagram of the proposed 1.88 GHz linear CMOS PA. The linearizer consists of an envelope-dependent PI circuit and an AI circuit as well as a hybrid bias circuit. As described in [21], the AI provides the envelope-reshaped gate bias (V_{BIAS}) to the main-stage amplifier to recover the compressed envelope magnitude. In this work, the PI circuit and AI circuit are employed to work as main

and auxiliary linearizers, respectively. The capacitance (C_V) and V_{BIAS} profiles by the PI and AI circuits are illustrated in Fig. 3.30(b). In addition, this PA contains a hybrid bias circuit to set the power-dependent static bias to the driver-stage, as shown in Fig. 3.30(c). The design details of the linear PA are explained below.

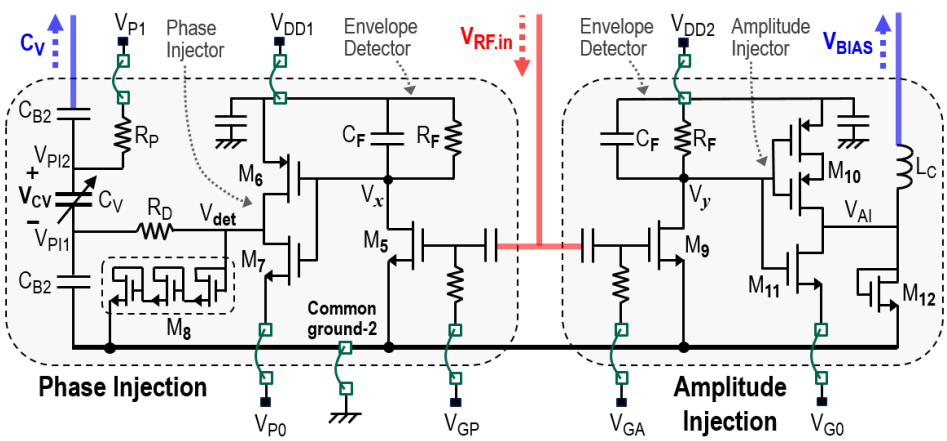
3.7.1 Baseline PA Design

Fig. 3.31 shows a schematic of the proposed linear CMOS PA. The baseline PA design is targeted to achieve watt-level P_{out} together with high PAE. Special care was taken to design the power cell and the output matching circuit to achieve this goal. The power cell is a quadruple-stacked FET with a gate-width of 20 mm so that it can sustain the voltage swing without breakdown when a V_{DD} supply of 4 V is applied. The optimum load impedance of the quadruple stack is 5 ~ 6 Ω, which is realized using the LC-based off-chip output matching network (T_L and C_L in Fig. 3.31(a)). The load impedances presented to the internal FET stacks (M_1 ~ M_3) are determined by the gate distribution capacitors (C_2 ~ C_4), whose capacitance values are determined based on the stacked-FET PA theory [5], [6]. The design values are summarized in Fig. 3.31(a). In addition, the harmonic impedance termination is important to achieve high PAE. Considering the small DC voltage and swing across each FET stack in the quadruple design (V_{DC} = 1 V for each stack), we have employed Class-F^{-1}-type harmonic load termination; the even-order voltage swing is induced while minimizing even-order current components. In the 1.88 GHz PA, the second-order harmonic termination described in Chapter 3.3.1 is applied to the gates of third and fourth FETs (M_3 and M_4), even with not shown in Fig. 3.31(a). In the case of the 0.9 GHz PA, the gate harmonic termination of CG-FETs is not performed, because the harmonic impedances of the internal FETs (under no harmonic termination) are already located near the high-efficiency region.

Since the range of the linearity correction using analog methods is limited compared with that using digital predistortion (DPD), the bias condition and power



(a)



(b)

Figure 3.31: (a) Schematic of the proposed linear PA for 1.88 GHz operation. (b) Detailed schematic of the phase and amplitude injection circuits.

drive level of the PA are set to avoid deep saturation and excessive gain compression. The target linear gain of the output stage was set to be higher than 12 dB. The transistor size ratio between the driver and main stages was selected to be

1:10 (2 mm vs. 20 mm). The idle current (I_Q) of the driver-stage was set at a higher level (14 mA for 2 mm FET) than the main-stage (80 mA for 20 mm FET). This bias condition allows higher efficiencies by reducing the quiescent current of the large transistor while avoiding excessive amplitude and phase distortion, which can be recovered by the proposed linearizer. The output-stage shows slight AM-AM expansion while the driver stage shows almost linear AM-AM characteristics. The measured dynamic AM-AM and AM-PM of the baseline PA (before linearization), which is presented in Chapter 3.8, shows soft compression characteristics. The phase-based linearizer is designed based on the amount of the dynamic AM and PM distortions.

3.7.2 Linearizer Design

Fig. 3.31(b) shows the detailed schematic of the proposed PI and AI circuits. Each injection circuit is composed of a CS envelope detector and an inverter-like envelope shaper. The input signal of the detectors is obtained from the gate of the main-stage. Two CS transistors, M_5 and M_9, are biased in deep Class-AB region to make V_x and V_y close to V_{DD1} and V_{DD2}, respectively, during low power region. R_F and C_F are used for filtering RF signal. To block RF signal at the output of the AI circuit, an on-chip inductor (L_C) is employed.

Two inverter-like injectors, M_6/M_7 for PI and M_{10}/M_{11} for AI, are different in terms of FET size and number-of-stack of PFET. Since the varactor and the gate of M_1 contain capacitances (C_V and $C_{gs.M1}$), the capacitances should be charged and discharged to generate the desirable V_{CV} and V_{BIAS} waveforms. As the gate capacitance of M_1 ($C_{gs.M1}$) is larger than the capacitance of the varactor (C_V), the FETs in the amplitude injector are designed to have larger gate width for larger current capability than those in the phase injector. M_{10} is a double-stacked PFET while M_6 is a single. Since the AI circuit is an auxiliary linearizer in this work, the required voltage swing of V_{BIAS} is much smaller than that of V_{CV}. A double-stacked

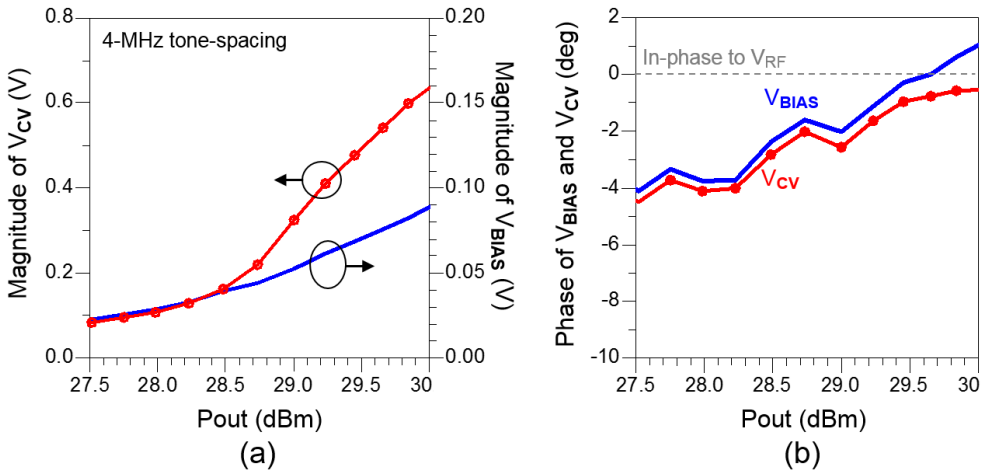


Figure 3.32: Two-tone simulation results of V_{CV} (PI circuit) and V_{BIAS} (AI circuit). Fundamental term of envelope frequency components is only considered. (a) Magnitude. (b) Phase mismatch with respect to the incoming RF voltage.

PFET provides lower voltage swing.

To maximize the linear P_{out} by the linearizer, the variation of V_{CV} and V_{BIAS} as a function of P_{out} should be controlled properly on-chip level, which means that excessive increase of V_{CV} and V_{BIAS} should be avoided for stable linearization. To this end, the design of limiters (M_8 and M_{12} in Fig. 3.31(b)) is important. The diode-connected limiter limits the maximum swing of the envelope-reshaped signal within the turn-on voltage of the diode. Simulation result showed that triple-stacked / single-stacked diode limiters are proper choice for phase / amplitude injectors, respectively. The simulated magnitude and phase mismatch of V_{CV} and V_{BIAS} are plotted in Fig. 3.32. Under the 4-MHz two-tone spacing condition, the phase of V_{CV}/V_{BIAS} is almost in-phase to that of the incoming RF signal.

The goal of the PI and AI circuits is to provide envelope-reshaped voltages (V_{CV} and V_{BIAS}) to the varactor (C_V) and common-source FET (M_1), respectively. However, in reality, the voltages may contain RF components as well as the envelope signals due to non-ideal RF-filtering by RC (R_F and C_F in Fig. 3.31(b))

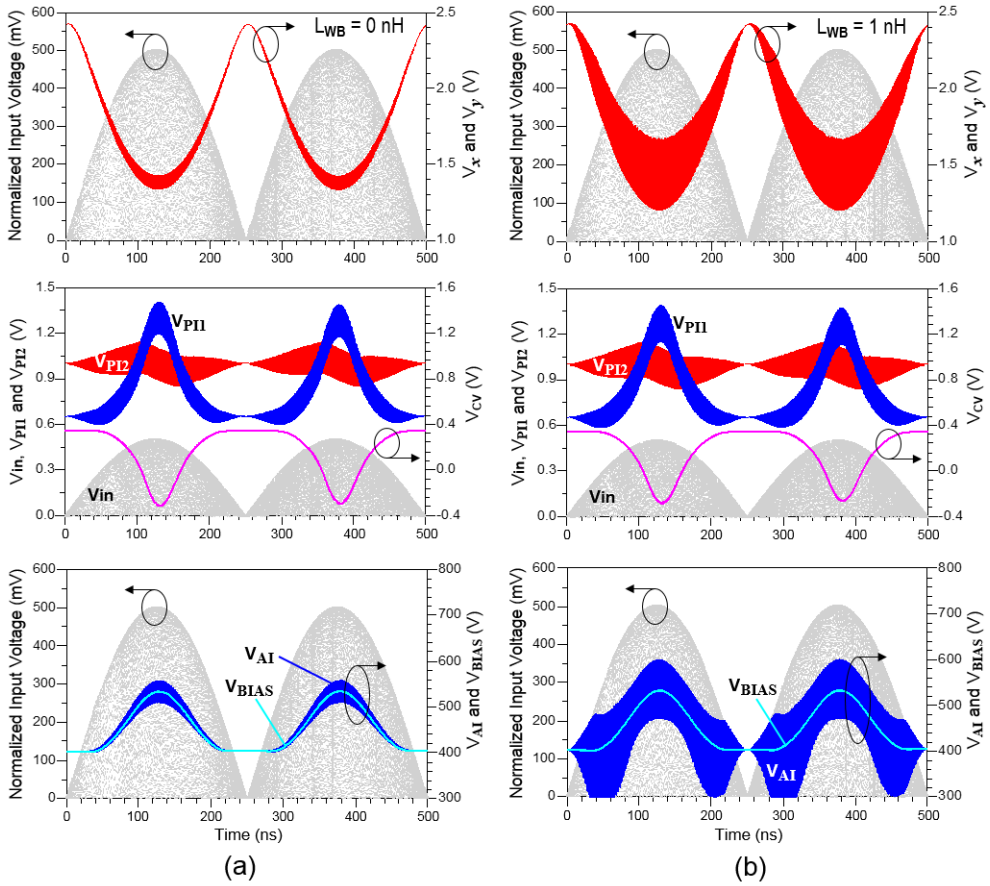


Figure 3.33: Envelope-reshaped voltages of the PI and AI circuits for the case of (a) L_{WB} = 0 nH and (b) L_{WB} = 1 nH.

and imperfect RF grounding at $V_{DD1/2}$ nodes by the bonding wires. Thus, it is worthwhile to check the RF components of V_{CV} and V_{BIAS} when the PI/AI circuits and $V_{DD1/2}$ are connected through bonding-wires with an inductance of 1 nH (worst case). Time-domain simulation shown in Fig. 3.33 reveals that the RF components of V_{CV} and V_{BIAS} are effectively rejected due to C_{B2}'s connected in series to C_V (and L_C and $C_{gs.M1}$ in Fig. 3.31), which effectively works as a low-pass filter for V_{CV} (and V_{BIAS}). To provide the evidence of AM-AM correction by the PI circuit as stated in Chapter 3.6, an envelope simulation was performed using a W-CDMA signal and the results are plotted in Fig. 3.34. The PI circuit shows AM-AM and AM-PM expansions of 0.7 dB and 9˚, respectively, at the bias conditions of V_{P1} =

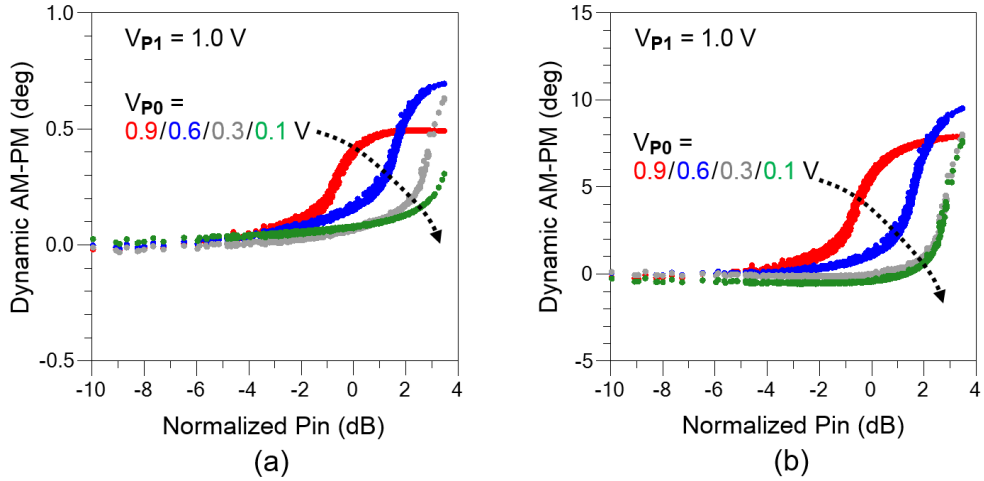


Figure 3.34: Simulated dynamic characteristics of the PI circuit using a W-CDMA signal. (a) Dynamic AM-AM. (b) Dynamic AM-PM.

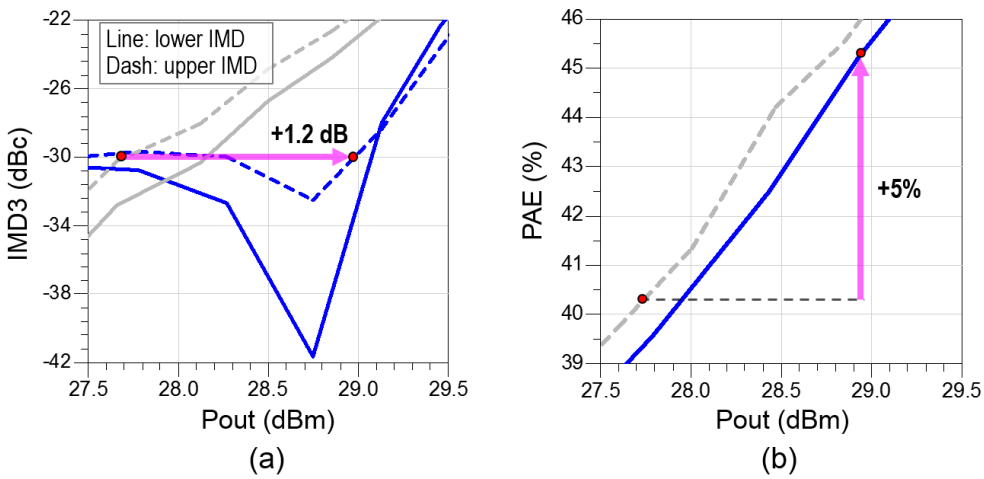


Figure 3.35: Two-tone simulation results of the designed 1.88 GHz linear PA with and without linearizer (curved in blue vs. gray). (a) IMD3. (b) PAE.

1.0 V and V_{P0} = 0.6 V.

As demonstrated in Chapter 3.4, the gate envelope impedance termination of a CS amplifier is essential for the 1.88 GHz PA to reject the gate bias modulation effect. This termination is fulfilled by M_{11} and L_C, since they provide a short-circuited envelope impedance (from V_{G0} node) to the gate of a main-stage. Due to

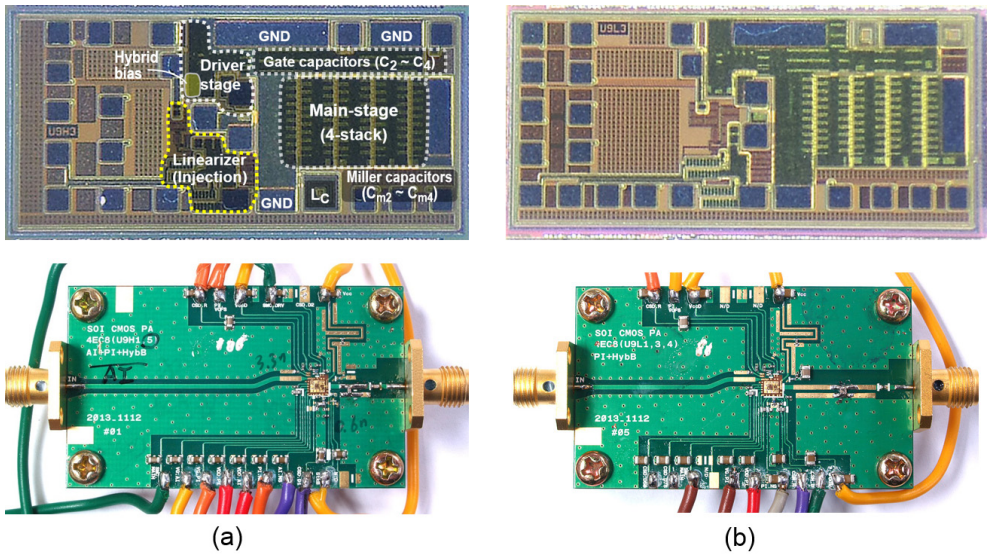


Figure 3.36: Photographs of the fabricated SOI CMOS PA ICs and evaluation modules. (a) 1.88 GHz PA. (b) 0.9 GHz PA.

the direct dc path between V_{G0} and the gate nodes, the hybrid bias circuit is employed for the driver-stage instead of the main-stage.

The two-tone simulation results (tone spacing = 4 MHz) of the designed 1.88 GHz linear CMOS PA is plotted in Fig. 3.35. Thanks to the proposed linearizer, the maximum linear P_{out} meeting IMD3 of –30 dBc is improved by 1.2 dB and thus the linear PAE is enhanced by 5%.

3.7.3 Fabrication

The designed PAs were fabricated using an SOI CMOS process (IBM CSOI7RF). All the MOSFETs have 0.32-μm gate length with an oxide thickness of 5.2 nm. Fig. 3.36 shows photographs of the fabricated SOI CMOS PA ICs and test modules for 1.88 GHz and 0.9 GHz operations (die size: 1.46 mm × 0.68 mm for 1.88 GHz PA and 1.54 mm × 0.68 mm for 1.88 GHz PA). The ICs with a thickness of 150-μm were mounted on a 400-μm-thick FR4 PCB ($\varepsilon_r \approx 4.6$, $\tan\delta = 0.025$), where LC-based off-chip output matching networks with a loss of 0.33 dB were

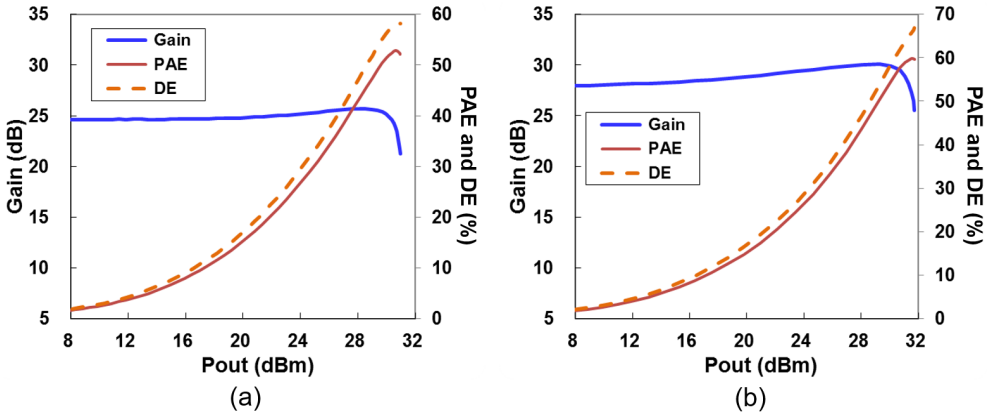


Figure 3.37: Measured CW results of the standalone PAs: (a) 1.88 GHz PA. (b) 0.9 GHz PA.

implemented. To minimize the source degeneration effect, multiple bond-wires were down-bonded to PCB ground.

3.8 Measurement Results

The implemented PAs work at V_{DD} = 4 V, and the quiescent currents of the driver and main stages were 14 and 80 mA for 1.88 GHz PA, respectively. V_{DD1} and V_{DD2} of the PI / AI circuits were biased near 2.0 V. In the case of 0.9 GHz PA, no measurable improvement was achieved using the AI and thus the hybrid bias circuit was employed for the main-stage. Quiescent currents of the driver and main stages of 0.9 GHz PA were 12 mA and 70 mA, respectively. The PAs were tested using the continuous wave (CW) signal, W-CDMA signal, and LTE signal.

3.8.1 CW Measurement

Since the fabricated PAs exhibited slight efficiency degradation near the saturated P_{out} due to dc power consumption of the linearizer, the standalone PAs (linearizer off) were first measured to characterize the performance of the PA core. Fig. 3.37 shows the measured gain, PAE, and DE of the 1.88 / 0.9 GHz PAs using

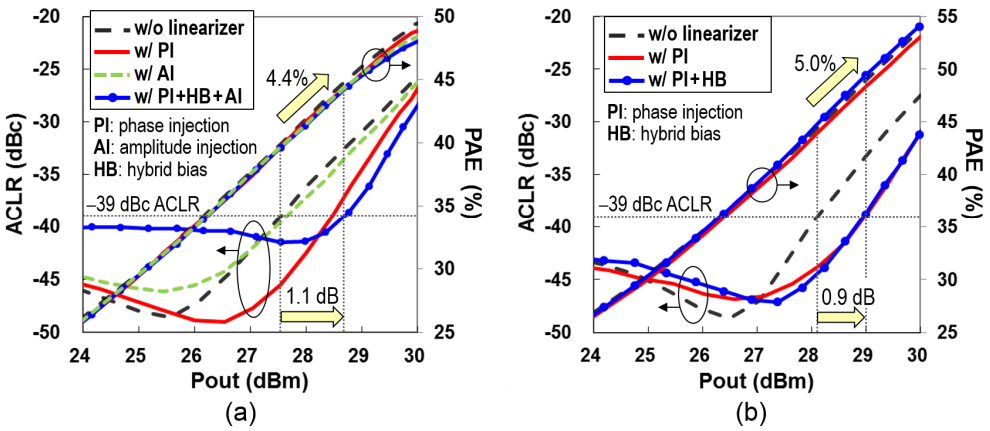


Figure 3.38: Measured 3G W-CDMA results: (a) 1.88 GHz PA. (b) 0.9 GHz PA.

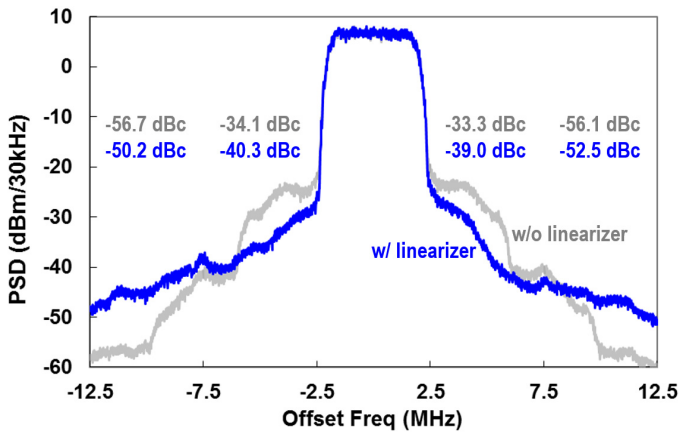


Figure 3.39: Measured power spectra of the 0.9 GHz PA at P_{out} = 29 dBm.

CW signal. In the case of 1.88 GHz PA shown in Fig. 3.37(a), saturated P_{out} of 31 dBm, gain of 24.5 dB, and peak PAE of 53% were achieved. Maximum DE (main-stage only) was 58.2%. The 0.9 GHz PA showed saturated P_{out} of 32 dBm, gain of 28 dB, peak PAE of 59.8%, and maximum DE was 67%, as shown in Fig. 3.37(b).

3.8.2 W-CDMA Measurement

The linear PAs were measured using a 3GPP uplink W-CDMA (Rel'99) signal with a channel bandwidth of 3.84 MHz and peak-to-average power ratio (PAPR) of 3.4 dB. The measured results are plotted in Fig. 3.38, where the

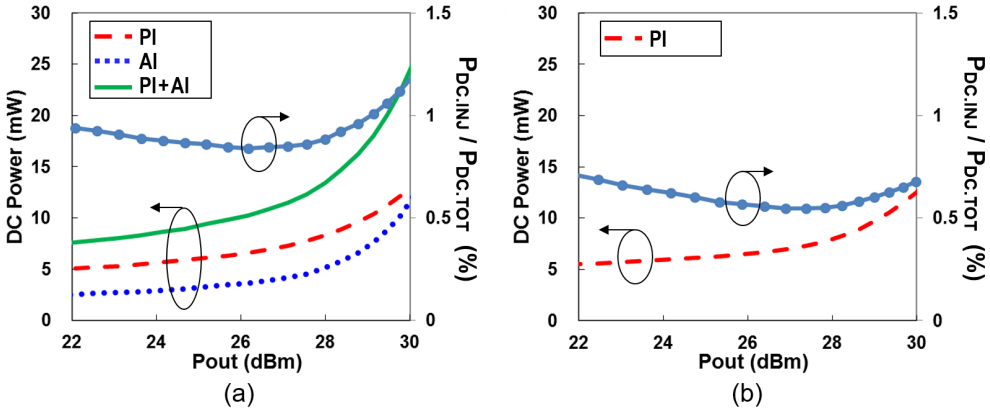


Figure 3.40: Measured dc power consumption of the linearizer using W-CDMA signal: (a) 1.88 GHz PA. (b) 0.9 GHz PA.

linearity data is the worst-case ACLRs. In the case of high-band PA shown in Fig. 3.38(a), four different cases are compared; PI only, AI only, both PI/AI with hybrid biasing and no linearization (reference). With both (PI/AI) linearizers, the PA shows a gain of 24.5 dB, an ACLR of –39 dBc, and a PAE of 44.3% at P_{out} = 28.7 dBm. Compared with the case of no linearization (and AI only), the maximum linear P_{out}, defined by the power meeting –39 dBc ACLR, is increased by 1.1 dB (and 1.0 dB) and PAE by 4.4% (and 4.1%). As one can see from Fig. 3.38(a), most of the linearization effect comes from the PI, as expected. The addition of hybrid bias helps improve ACLR in the max power region while trading off ACLR in the mid-power region. More linearization effect of the AI and hybrid biasing is shown near the output power meeting –36 dBc ACLR.

W-CDMA test results of the 0.9 GHz PA are plotted in Fig. 3.38(b), showing a gain of 28 dB, an ACLR of –39 dBc, and a PAE of 49.2% at P_{out} = 29 dBm. The maximum linear P_{out} and PAE are improved by 0.9 dB and 5%, compared to the reference PA. In the case of the low-band PA, no measurable improvement was achieved using the AI. The hybrid bias contributed to a PAE improvement by ~1% while meeting similar ACLR compared to the PA with PI only. Fig. 3.39 shows the

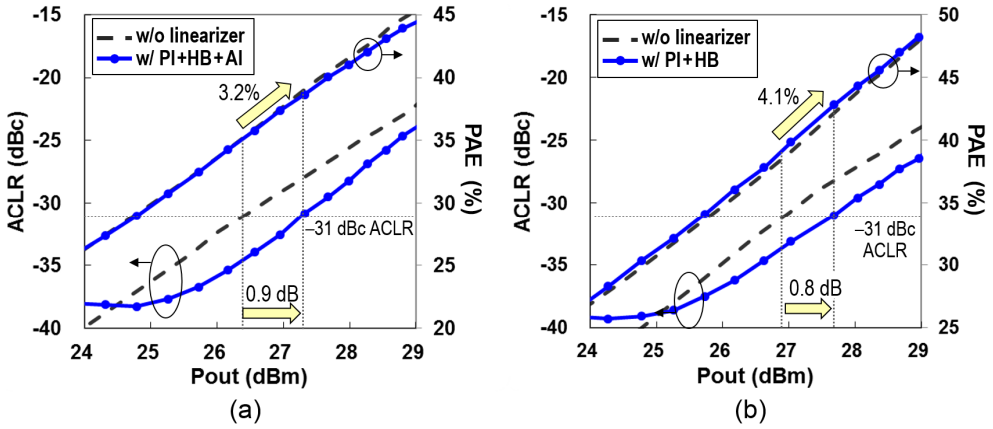


Figure 3.41: Measured 4G LTE results: (a) 1.88 GHz PA. (b) 0.9 GHz PA.

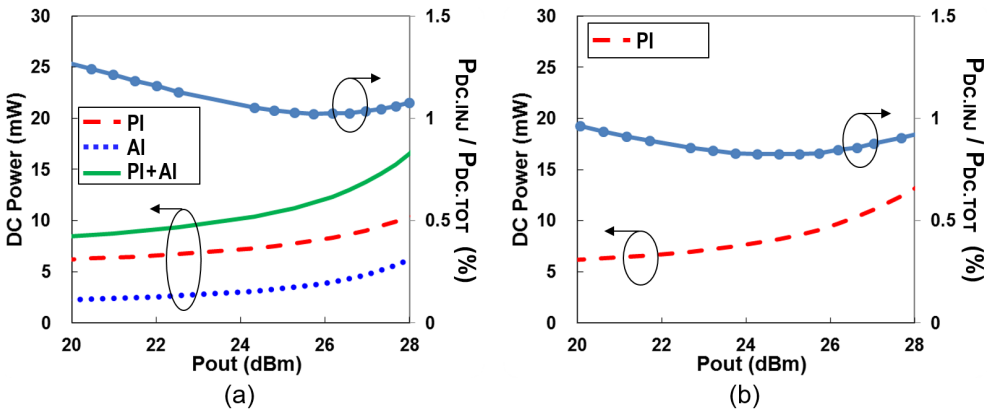


Figure 3.42: Measured dc power consumption of the linearizer using LTE signal: (a) 1.88 GHz PA. (b) 0.9 GHz PA.

measured W-CDMA power spectra of the 0.9 GHz PA with and without linearizer at P_{out} = 29 dBm.

Even though the linear PAE improvement is remarkable, the PI/AI circuits consume very low dc power. As shown in Fig. 3.40, the linearizer of 1.88 GHz PA (and 0.9 GHz PA) consumed 1% (and 0.6%) of the total dc power. Thus, the PAE degradation by the linearizer is less than 0.5% and 0.3% for 1.88 / 0.9 GHz PAs.

3.8.3 LTE Measurement

LTE performance was measured with a 10 MHz bandwidth 16-QAM signal (PAPR = 7.5 dB). The signal was obtained from the Agilent Signal Studio (option: N7624B) and E4438C signal generator. The results of 1.88 GHz PA is plotted in Fig. 3.41(a). The PA showed a PAE of 38.5% at P_{out} = 27.3 dBm while meeting $ACLR_{E\text{-}UTRA}$ = –31 dBc. The PAE of the main-stage alone is estimated to be 40.5% for 1.88 GHz PA. Since the PAPR of the LTE signal is quite higher than W-CDMA signal (7.5 dB versus 3.4 dB), the linear P_{out} is further backed-off and thus the PAE improvement is slightly reduced to 3.2%. In the case of 0.9 GHz PA shown in Fig. 3.41(b), a linear PAE of 42.9% (meeting –31 dBc ACLR) was achieved at P_{out} = 27.7 dBm, which is 4.1% improvement compared with the case without linearizer. The linearizer consumed ~1% of the total dc power, as shown in Fig. 3.42, thus resulting in ~0.4% PAE degradation by the linearizer.

To validate the linearization effect of the proposed linearizer, the dynamic AM-AM and AM-PM of 1.88 GHz PA were measured with AI and PI circuits separately using the test setup in Fig. 3.43 and the results are plotted in Fig. 3.44. It is worthwhile to note that the AI degrades AM-PM linearity and shows limited ACLR improvement (~0.9 dB). On the other hand, the proposed PI recovers both AM-AM and AM-PM distortion and improves ACLR by 4.2 dB. By employing PI/AI/hybrid bias, the ACLR of the PA is improved by 6.4 dB compared with the case without linearizer, thus meeting –39 dBc W-CDMA ACLR.

Table 3.2 summarizes the measured results of the 1.88 / 0.9 GHz PAs, where LTE 10 MHz QPSK (PAPR = 6.7 dB) data is also included. The performance of recently reported linear CMOS PAs is summarized in Table 3.3. The measured efficiency and ACLR are among the best reported from CMOS PAs.

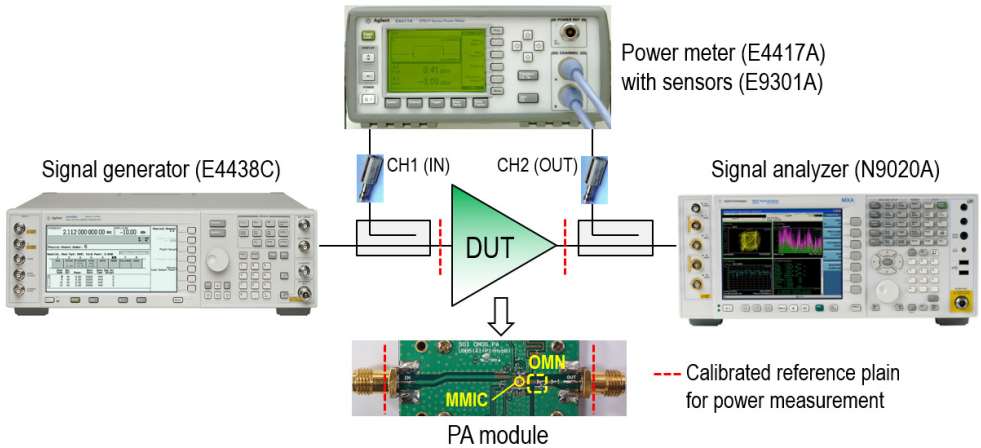


Figure 3.43: Test setup for power and dynamic AM-AM/PM measurements.

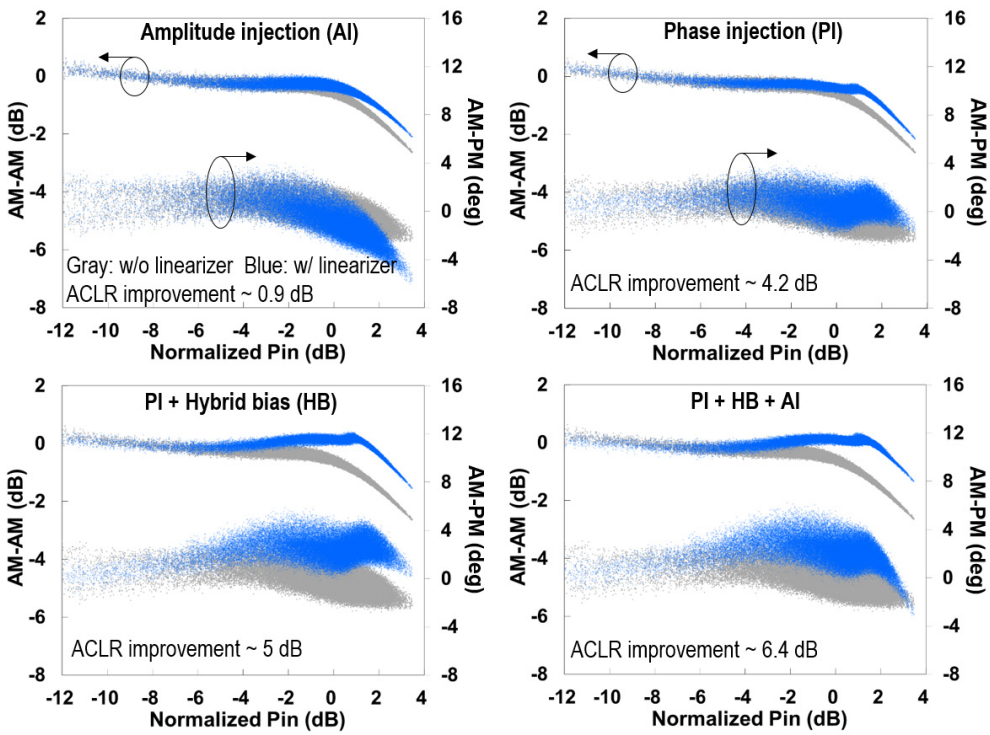


Figure 3.44: Measured dynamic AM-AM and AM-PM of 1.88 GHz PA at P_{out} = 28.7 dBm using a W-CDMA signal.

TABLE 3.2

MEASUREMENT SUMMARY OF THE LINEAR CMOS PAS

Signal	1.88 GHz PA				0.9 GHz PA			
	P_{out} (dBm)	ACLR (dBc)	PAE (%)	P_{out} / PAE ↑ (dB / %)	P_{out} (dBm)	ACLR (dBc)	PAE (%)	P_{out} / PAE ↑ (dB, %)
W-CDMA	28.7	–39	44.3	1.1 / 4.4	29.0	–39	49.2	0.9 / 5.0
LTE QPSK	28.0	–31	41.2	1.0 / 3.7	28.3	–31	45.4	0.7 / 4.0
LTE 16-QAM	27.3	–31	38.5	0.9 / 3.2	27.7	–31	42.9	0.8 / 4.1

"↑" means increments on linear P_{out} and PAE compared with the case without linearizer.

TABLE 3.3

PERFORMANCE COMPARISON OF THE STATE-OF-THE-ART LINEAR CMOS PAS

Ref	CMOS Technology	Signal	Freq (GHz)	P_{out} (dBm)	Gain (dB)	PAE (%)	ACLR (dBc)	V_{DD} (V)
[20]	GaAs HBT	W-CDMA	1.95	28	N/A	44.5	–38	3.4
[6]*	0.13 μm (SOI)	W-CDMA	1.9	28.5	14.6	38.7	–38	6.5
[8]	0.5 μm	W-CDMA	1.75	24	23.9	29	–35	3.3
[15]†	0.13 μm	W-CDMA	1.88	27.1	28.3	28	–40	3.0
[17]	0.32 μm (SOI)	W-CDMA	0.84	27.1	N/A	47.5	–36	4.0
[19]†	0.18 μm	W-CDMA	1.95	23.5	26	40	–33	3.4
[21]*	0.18 μm & IPD	W-CDMA	1.85	26.8	15.8	43.3	–37	3.5
[22]*	0.18 μm	LTE‡	1.85	27.8	14.2	41	–31	3.5
This work [32]	0.32 μm (SOI)	W-CDMA	0.9	29	28	49.2	–39	4.0
			1.88	28.7	24.5	44.3	–39	4.0
		LTE‡	0.9	27.7	28	42.9	–31	4.0
			1.88	27.3	24.5	38.5§	–31	4.0

*Single-stage PAs. †On-chip output matching.

‡Uplink LTE 10 MHz-bandwidth 16-QAM (PAPR = 7.5 dB)

§Estimated PAE of the main-stage amplifier only is 40.5%.

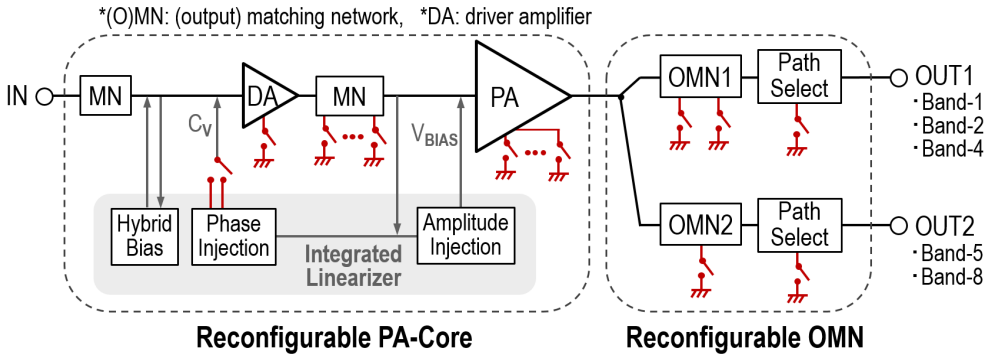


Figure 3.45: Block diagram of the proposed multiband (MB) linear CMOS PA.

3.9 A Single-Chain Multiband (MB) Reconfigurable Linear Power Amplifier in SOI CMOS

Based on the MB reconfigurable matching structure and linearization technique described above, a single-chain MB linear CMOS PA is implemented. The details of the design, fabrication, and measurement results are presented below.

3.9.1 MB Linear CMOS PA: Design

Fig. 3.45 shows a block diagram of the proposed MB linear CMOS PA [33]. It consists of a reconfigurable single-chain PA core and a reconfigurable output matching network (OMN). The PA has two outputs and is designed to support any combinations of one low-band and one high-band out of five popular 3G/4G bands (Band 1/2/4/5/8), covering uplink UMTS/LTE frequency range of 824 ~ 1980 MHz [25]. Circuit reconfiguration is achieved by using the SOI CMOS switches made out of the same process as the PA core. Also, to improve the linear P_{out} and PAE, a phase-based linearizer described in Chapter 3.8 is employed and reconfigured according to the operating frequencies [32].

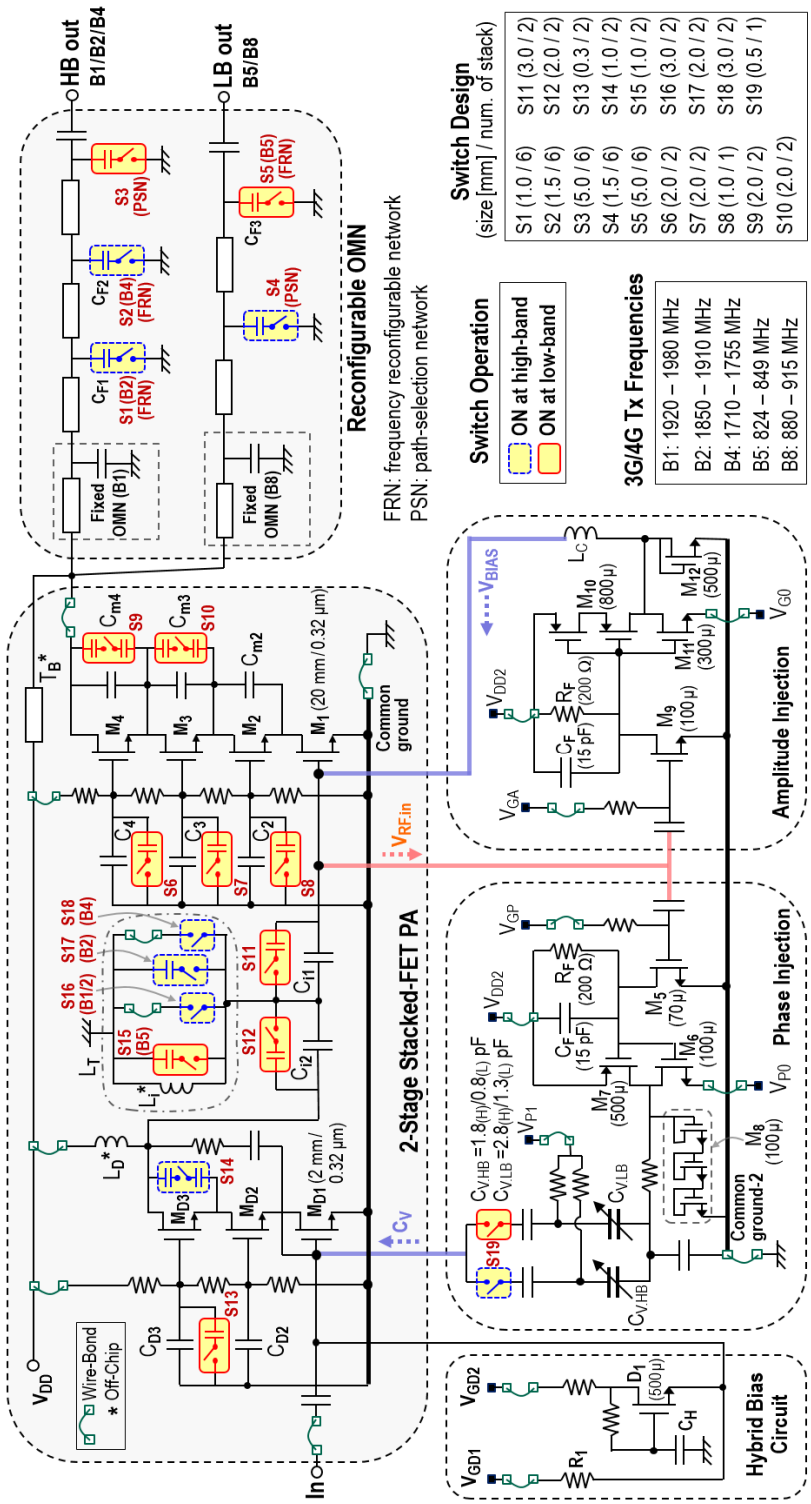


Figure 3.46: Schematic of the proposed MB reconfigurable linear CMOS PA.

The detailed schematic of the proposed PA is shown in Fig. 3.46. The PA core is based on a two-stage stacked-FET amplifier [6]. The high-band (HB) output path supports Band-1 as a natural band and can be reconfigured to support Band-2 and Band-4. The low-band (LB) output path supports Band-8 as a natural band and Band-5 as a reconfigured band. The transmit (Tx) frequencies of the five bands are also summarized in Fig. 3.46. Since only one output port is used at a time, the unused output is deactivated in the OMN using the path-selection networks and frequency reconfigurable networks [28], which was described in Chapter 2.

RF switches are implemented using 0.32-μm 2.5-V NFETs, which show an on-state resistance (R_S) of 0.8 Ω•mm and an off-state capacitance (C_{off}) of 310 fF/mm, as summarized in Table 3.4. The switch design is aimed to minimize the loss due to the reconfiguration. As shown in [28], the loss of the path-selection network is a strong function of R_S and thus large switches (6-stacked NFETs with a 5 mm gate-width; $R_S \approx 1$ Ω) are used for S3 and S4 in Fig. 3.46. On the other hand, the frequency reconfiguration switches (S1, S2 and S5 in Fig. 3.46) have smaller size (6-stacked NFETs with 1~1.5 mm; $R_S \approx 3.2$~4.8 Ω) since the reactances for frequency reconfigurations (C_{F1}, C_{F2}, and C_{F3} in Fig. 3.46) are far greater (>90 Ω) than R_S. A single-stack FET can handle a maximum RF voltage swing of 3.3 V and thus a switch cell composed of 6 FET-stacks shows $P_{0.1dB}$ more than 35 dBm, which is sufficient for 3G/4G handset applications. The measured power endurance of the SOI switch is plotted in Fig. 3.47.

In the PA-core, circuit reconfiguration is applied to the interstage network as well as the internal FETs in the stack. The interstage matching is based on a high-pass network consisting of two series capacitors and a shunt inductor. The values of the two series capacitors, C_{i1} and C_{i2} in Fig. 3.46, are designed for HB operation, and the capacitances are reconfigured by closing S11 and S12 during LB operation. The composite inductance of the shunt inductor, L_T, is reconfigured according to

TABLE 3.4

TYPICAL RF SWITCH CHARACTERISTICS

Characteristics	SOI CMOS (this work)	PIN diode [28]	pHEMT [52]
R_S (Ω)	0.8 Ω·mm	1.0	1.9
C_{off} (fF)	310 fF/mm	400	147
FOM (=$R_S \cdot C_{off}$) (fsec)	250	400	280
Power handling (dBm)	20log($N \cdot V_m$)+10	>38	>35

※ FOM: figure-of-merit.

N: number of stacks.

V_m: rated drain-source voltage of single NFET (approximately 3.3 V).

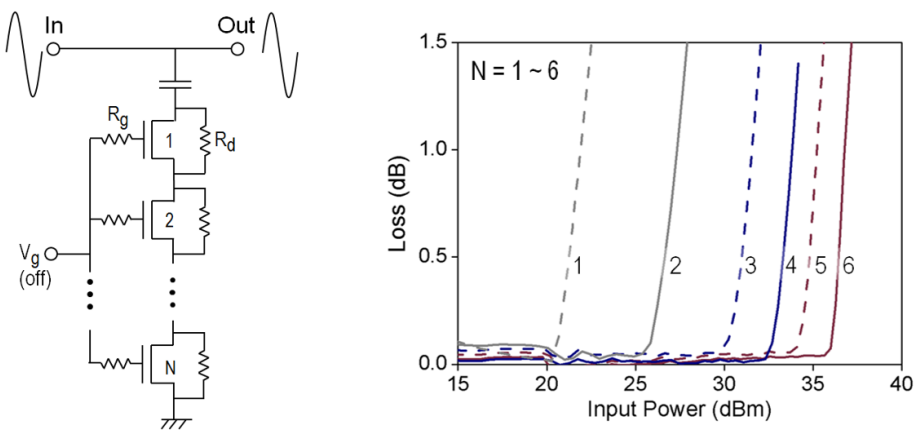


Figure 3.47: Measured power handling of the SOI switch (at off-state) for various number of stacks (N).

the frequency band of operation. For example, L_T becomes L_i at Band-8 (f_0 = 897.5 MHz) and is reconfigured for Band-5 (836.5 MHz) by turning S15 on. Likewise, S16 is closed during Band-1/2 operation and S17 and S18 are turned on for Band-2 (1880 MHz) and Band-4 (1732.5 MHz) operation, respectively.

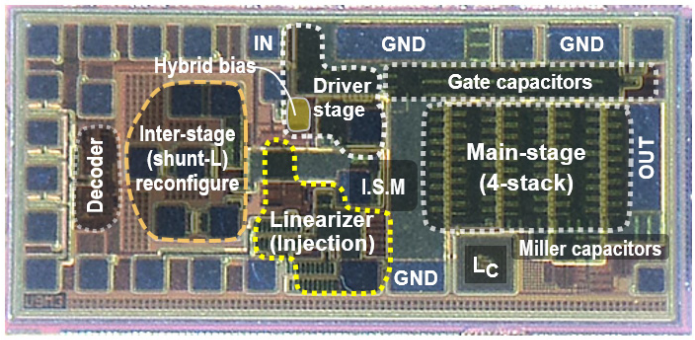
To operate the stacked-FET cells at optimum PAE and power points, the individual FETs in the stack need to present the optimum load to the preceding FETs. For this purpose, the external drain-source Miller capacitors (C_{m3} and C_{m4} in

Fig. 3.46) and the gate capacitors (C_2, C_3, and C_4) have been reconfigured according to the frequency. Simple stacked-FET theory assumes that constant gate capacitances ($C_2 \sim C_4$) can be used irrespective of the frequency [5], [6]. However, this assumption is no longer valid if the parasitic capacitances cannot be neglected [37]. Since the output-stage FETs ($M_1 \sim M_4$) with a 20 mm gate-width have large parasitic capacitances and the common node of $C_2 \sim C_4$ is RF grounded through a wire-bond, the optimum load impedances of internal FETs change as a function of frequency. To compensate for this, the capacitances in the power-stage stacked-FET cells are increased during LB operation by closing the switches, S6 ~ S10. Similar reconfiguration is also applied to the driver-stage using S13 and S14.

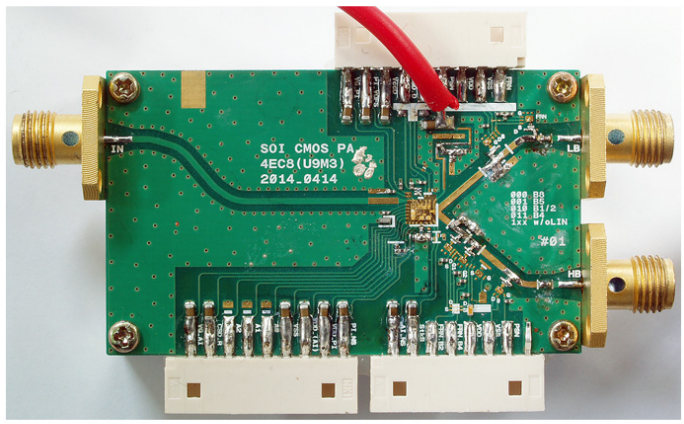
As experimentally demonstrated in Chapter 3.8, the linearizer circuits are instrumental in achieving the required W-CDMA/LTE linearity while not compromising the PAE for CMOS PAs. The detailed circuit schematic of the linearizers is also shown in Fig. 3.46. The phase injection circuit provides the envelope-reshaped capacitance (C_V) to the stacked-FET cells to recover the dynamic AM-PM distortion. Since the amount of the required capacitance injection for phase correction is different between HB and LB modes, the switches, S19, select one of the two varactors according to the operating frequency band groups ($C_{V.HB}$: HB, $C_{V.LB}$: LB). On top of the phase injection, the amplitude injection and hybrid bias are also activated during HB operation to further enhance the PA linearity.

3.9.2 MB Linear CMOS PA: Measurement

The PA was fabricated using an SOI CMOS process and all the MOSFETs have 0.32-μm gate length. Fig. 3.48 shows photographs of the SOI CMOS PA IC and test module. The IC was mounted on a 400-μm-thick FR4 substrate, where the reconfigurable OMN was realized using the off-chip capacitors and discrete SOI switches for the proof-of-concept experiment. The switches in the PA-core (S6 ~



(a)



(b)

Figure 3.48: Photographs of the fabricated (a) SOI CMOS IC (size = 1.54 mm × 0.68 mm) and (b) test module.

S19 in Fig. 3.46) are controlled by the integrated 3-bit logic decoder.

The PA works with V_{DD} = 4 V and idle current of 92 / 106 mA for HB / LB modes, and 3GPP uplink W-CDMA (Rel'99) signal was used for the initial testing. The measured results are plotted in Fig. 3.49. In the case of HB (Band 1/2/4) operation shown in Fig. 3.49(a), the PA showed gains higher than 23 dB and ACLRs better than –39 dBc up to the rated linear P_{out}'s (~28.5 dBm). The measured PAEs at the maximum linear P_{out}'s (meeting –39 dBc ACLR) were higher than 40.7% for all high bands. In the case of LB (Band 5/8) shown in Fig. 3.49(b), the PA showed gains higher than 28 dB and ACLRs of better than –39 dBc

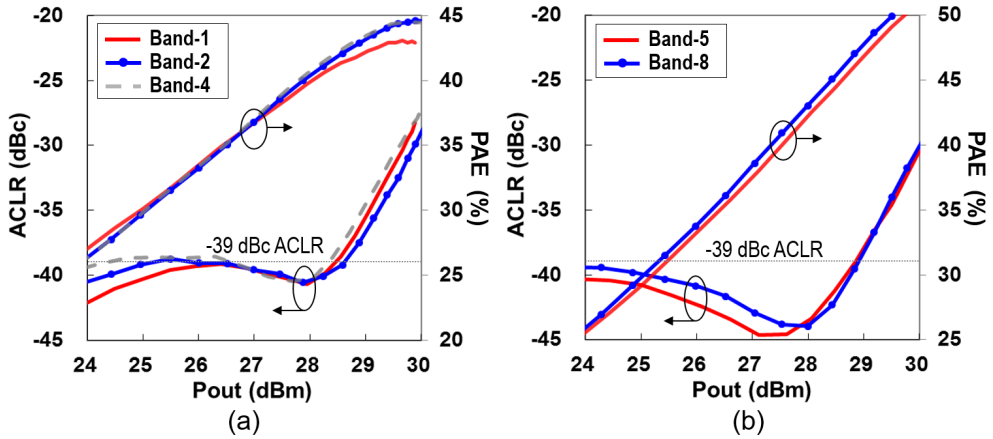


Figure 3.49: Measured W-CDMA results of the MB linear CMOS PA: (a) High-band. (b) Low-band.

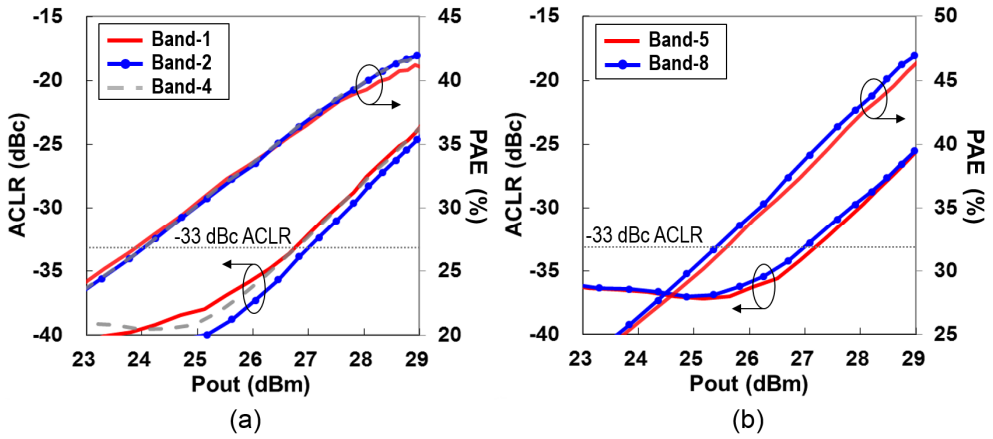


Figure 3.50: Measured LTE results of the MB linear CMOS PA: (a) High-band. (b) Low-band.

up to the rated linear P_{out}'s (~28.8 dBm). PAEs higher than 46% were measured for all the low bands while meeting –39 dBc ACLR. A separate test turning on and off the linearizer showed that the linear P_{out}'s and PAEs were improved by more than 0.8 dB and 3.5%, respectively, through the use of the linearizer.

LTE performance test was also performed using 10 MHz-bandwidth 16-QAM (PAPR = 7.5 dB) signal, and the results are shown in Fig. 3.50. The measured

TABLE 3.5

PAE SUMMARY FOR EACH BAND COMBINATION

Band	PAE (%) at W-CDMA –39 dBc	PAE (%) at LTE –33 dBc
B1/ B5	40.7 / 46.0	35.7 / 38.7
B1 / B8	40.7 / 46.9	35.7 / 38.9
B2 / B5	41.7 / 46.0	36.8 / 38.7
B2 / B8	41.7 / 46.9	36.8 / 38.9
B4 / B5	41.2 / 46.0	36.2 / 38.7
B4 / B8	41.2 / 46.9	36.2 / 38.9

TABLE 3.6

PERFORMANCE COMPARISON OF THE REPORTED MULTIBAND W-CDMA PAS

Ref	PA (switch) technology	N.out / core[1]	PAE (%)					ACLR (dBc)	Output Matching
			B1	B2	B4	B5	B8		
[26]	GaAs HBT (FET)	1 / 1	31	26	28	26.5	24.5	–37	Reconfiguration
[27][2]	pHEMT	5 / 2	40	40.5	40	44	42	–38	Broadband
[28]	GaAs HBT (PIN diode)	2 / 2	39.1	40.7	38.7	43	43.3	–39	Reconfiguration
[29]	GaAs HBT (0.32 μm SOI)	5 / 2	38.0	39	37.5	41	41.1	–39	Reconfiguration
[30]	GaAs HBT (PIN diode)	5 / 2	41.0	41.1	40.5	40.1	40.4	–39	Reconfiguration
This work [33]	0.32 μm SOI [W-CDMA]	2 / 1	40.7	41.7	41.2	46.1	47.0	–39	Reconfiguration
	0.32 μm SOI [LTE[3]]	2 / 1	35.7	36.8	36.2	38.8	38.9	–33	Reconfiguration

[1] Number of the reconfigurable outputs / PA-cores.

[2] It is based on triple stacked-FET structure with separated V_{DD} of each FET, resulting in very large optimum load impedance (R_{opt} = 25 ~ 30 Ω).

[3] LTE 10-MHz bandwidth 16-QAM signal with PAPR = 7.5 dB.

PAEs at the rated linear P_{out}'s (~27 dBm) meeting $ACLR_{E\text{-}UTRA}$ = –33 dBc were higher than 35.7% for all the high bands and 38.7% for the low bands. The measured PAEs for each band combination are summarized in Table 3.5.

To estimate the reconfiguration loss of the PA, a single-band reference PA was also fabricated on the same chip using the fixed OMN. The reference PAs for HB / LB showed PAEs of 44 / 48.4% at the rated linear P_{out}'s (meeting W-CDMA ACLRs of –39 dBc). Thus, the PAE degradation due to multi-banding in our work are estimated to be of 1.5 ~ 3.3%, which is attributed to the losses of the switches and output matching. The PAE degradation is much smaller than that from the previous single-chain PA [26]. The performance of recently reported MB linear PAs is compared in Table 3.6. To the best of our knowledge, this is the first demonstration of 3G/4G MB reconfigurable CMOS PA using a single PA-core showing above 40% W-CDMA efficiency while meeting 3GPP linearity requirements with margin. The performance is comparable or better than GaAs-based counterparts.

3.10 Summary

In this study, a PA linearization technique based on the envelope-dependent phase injection (PI) has been proposed for highly linear and efficient CMOS PA. To achieve better efficiency and linearity of a standalone CMOS stacked-FET PA, the second-order harmonic termination and control of gate bias modulation are discussed. Together with the auxiliary amplitude injection and hybrid bias circuit, the fabricated 1.88 / 0.9 GHz W-CDMA SOI CMOS PAs meet the stringent linearity (ACLR < –39 dBc) across the entire output power range and show PAEs higher than 44 / 49% at 28.7 / 29.0 dBm, respectively, which are comparable to those of GaAs-based PAs.

In addition, a single-chain multiband (MB) PA has been developed using an SOI CMOS process to cover multiple UMTS/LTE bands from 824 MHz to 1980 MHz. To avoid the performance degradation by covering too wide bandwidth using a single PA-core, SOI CMOS switch-based reconfiguration is applied to the stacked transistor cells and interstage matching as well as the output matching. Combined with the reconfigurable structure and linearization technique, the fabricated PA showed PAE degradation of less than 1.5 ~ 3.3% compared with the single-band dedicated PA. The proposed PA design can offer significant advantages in terms of the PA module size and cost for 3G/4G mobile applications requiring global roaming.

3.11 References

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Chapter 4

Linearization of CMOS Power Amplifier Covering Wideband Signal

4.1 Introduction

As a mobile communication standard is evolved from 3G UMTS to 4G LTE, the importance of high-speed data transmission is significantly increased. Contrary to the voice-centric 3G W-CDMA, the data-centric 4G LTE employs wideband signal as well as higher-level modulation scheme to maximize data transmission capacity. As a result, the peak-to-average power ratio (PAPR) of the LTE signal is far higher than that of the W-CDMA signal (7.5 dB for LTE 16-QAM versus 3.4 dB for W-CDMA Rel'99 hybrid PSK) and thus the operating power range of LTE PAs should further be backed-off to maintain acceptable linearity. Moreover, the use of wideband signal (10/20 MHz for 4G versus 3.84 MHz for 3G) may give rise to performance degradation due to the non-quasi-static operation of a PA, thus causing nonlinearity including memory effect [1]-[3].

With the advent of the carrier aggregation technology for wide-banding

recently, the LTE signal with a bandwidth (BW) of wider than 40 MHz will be deployed not only for downlink but also for uplink [4]-[6]. Since a wideband signal contains high-speed envelopes, PA linearization should also work on the envelopes. Even though the envelope-based analog linearizers ([7], [8]) demonstrated the usefulness in terms of linear efficiency under 10-MHz BW LTE signal, however, their practical limitations under wider BW signals have not been investigated yet. Therefore, it is worthwhile to analyze the BW limiting factor of the envelope-based linearizer and propose a new solution for wideband application.

This chapter deals with a linearization technique suitable for a wideband signal. Analysis shows that the envelope-based linearizer introduced in Chapter 3 is vulnerable to wideband signals. To overcome the limitation, the phase injection (PI) circuit structure is modified for feed-forward detection and a group delay circuit (GDC) is employed. Together with the GDC and PI circuits, the fabricated 0.9 GHz linear SOI CMOS PA achieves high linear efficiency under 10/20/40 MHz-BW LTE signals. This study is organized as follows: In Chapter 4.2, the BW limiting effect of envelope-based linearizers is analyzed and a simple solution is proposed. Chapter 4.3 presents a practical solution for covering wideband signal and miniaturizing circuit size by employing a compact GDC. The fabrication and measurement results of the proposed linear PA is presented in Chapter 4.4.

4.2 Bandwidth Limitation of Envelope-Based Linearizers

4.2.1 Analysis

To investigate the BW limiting effect of the phase-based linearizer described in Chapter 3, the linear CMOS PA using PI was measured with 10/20-MHz BW LTE signals (16-QAM with PAPR = 7.5 dB). Fig. 4.1 shows the measured $ACLR_{E\text{-}UTRA}$ of the PA with and without linearizer. This result shows that the linearization effect is limited below 10-MHz BW; linear P_{out} improvement is limited from 0.75

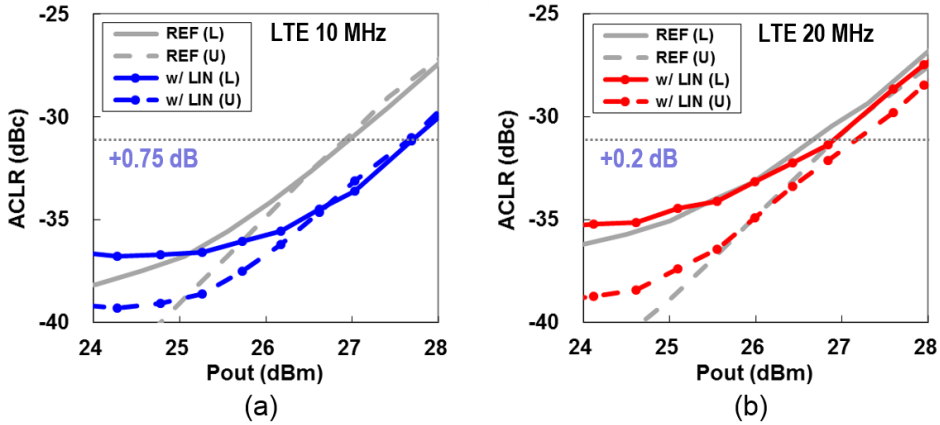


Figure 4.1: Measured bandwidth (BW) limiting effect of the linear CMOS PA with phase injection (PI). (a) $ACLR_{E\text{-}UTRA}$ using 10-MHz BW LTE signal. (b) $ACLR_{E\text{-}UTRA}$ using 20-MHz BW LTE signal.

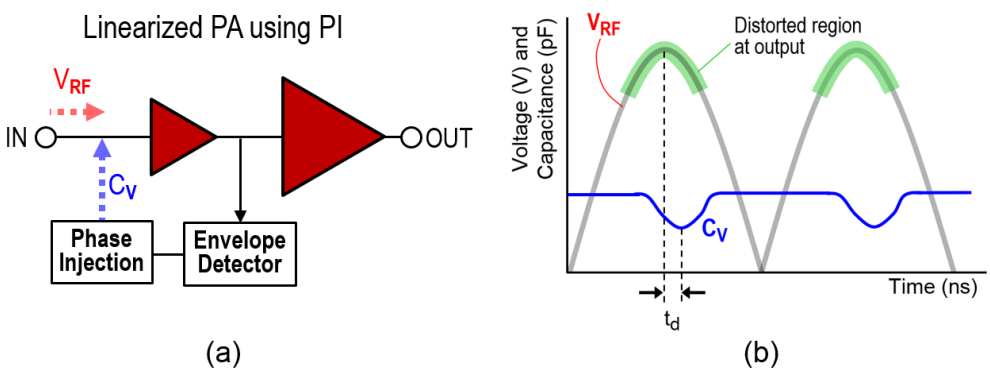


Figure 4.2: (a) Block diagram of the linear PA with PI. (b) Time-domain input RF signal (V_{RF}) and injected capacitance (C_V) waveforms.

dB (at 10 MHz) to 0.2 dB (at 20 MHz). Since the PAPRs of the two signals are almost identical (~7.5 dB), one can see that one of the most limiting factors comes from the timing issue between the incoming input RF signal (V_{RF}) and envelope-reshaped signal (C_V) of the phase injector. The BW limiting mechanism is illustrated in Fig. 4.2. Since C_V experiences a time-delay during the envelope-detection and shaping by the PI circuit, the time difference between V_{RF} and C_V

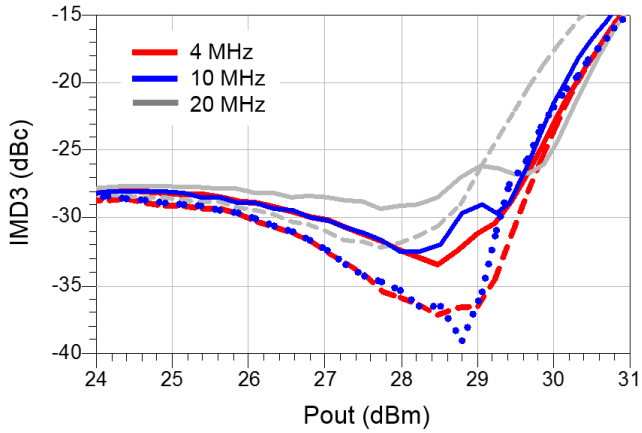


Figure 4.3: Simulated two-tone IMD3 of the linear PA with PI/AI for various tone-spacings (solid lines: lower IMDs, dotted/dashed lines: upper IMDs).

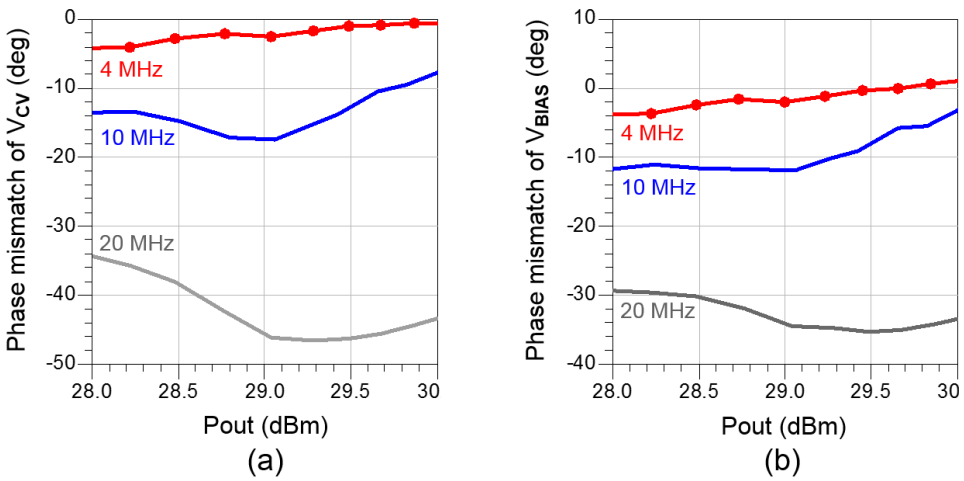


Figure 4.4: Simulated phase mismatch of the envelope-reshaped voltages with respect to the incoming RF signal (V_{RF}). (a) V_{CV}. (b) V_{BIAS}.

(V_{CV}) waveforms, t_d in Fig. 4.2(b), makes the phase injector perform non-ideal linearization, thus resulting in limited linearity improvement.

The BW-limitation of the PA is also observed in simulation level. Fig. 4.3 shows the simulated IMD3 of the linear CMOS PA with PI/AI under two-tone input condition (tone spacing of 4/10/20 MHz). Contrary to the 4-MHz and 10-

TABLE 4.1

SIGNAL BANDWIDTH (BW = TONE-SPACING) VERSUS ANGULAR DELAY

BW (MHz)	Period (ns)	Angular delay / ns (deg)	Application
1	1000	0.36	2G CDMA
4	250	1.44	3G W-CDMA
10	100	3.6	4G LTE (10 MHz)
20	50	7.2	4G LTE (20 MHz)
40	25	14.4	4G LTE 20+20 MHz (CA*)

*Carrier aggregation.

MHz BW cases, the PA under the 20-MHz BW signal exhibits a significant IMD asymmetry. As described in [9], the IMD asymmetry comes from the envelope asymmetry: especially when the upward (↗) and downward (↘) output envelopes show different behavior even with the same input signal amplitude, as shown in Fig. 3.12. If the time delay (t_d) in Fig. 4.2 is translated to a phase-domain, the phase mismatches of V_{CV} and V_{BIAS} with respect to V_{RF} can be obtained, as shown in the simulation results of Fig. 4.4. From the results, one can see that the phase mismatches are slightly reduced when P_{out} gets further increased. Also, the amount of phase mismatch is not proportional to the tone-spacing (signal BW). As a result, the 20-MHz BW result shows a significant linearity degradation due to the phase mismatch of larger than 30˚, compared to the 4-MHz and 10-MHz BW results.

Since the envelope of a two-tone signal is time-periodic, the phase mismatch between V_{RF} and C_V (by t_d) can be derived. Once the two-tone spacing (BW) and t_d are determined, the phase mismatch at envelope frequency, θ_d, is calculated as

$$\theta_d = 360 \cdot BW \cdot t_d \tag{4.1}$$

where the unit of θ_d is degree. The relation between the signal BW and angular delay is summarized in Table 4.1. In the case of the signals with 1 ~ 4 MHz BWs

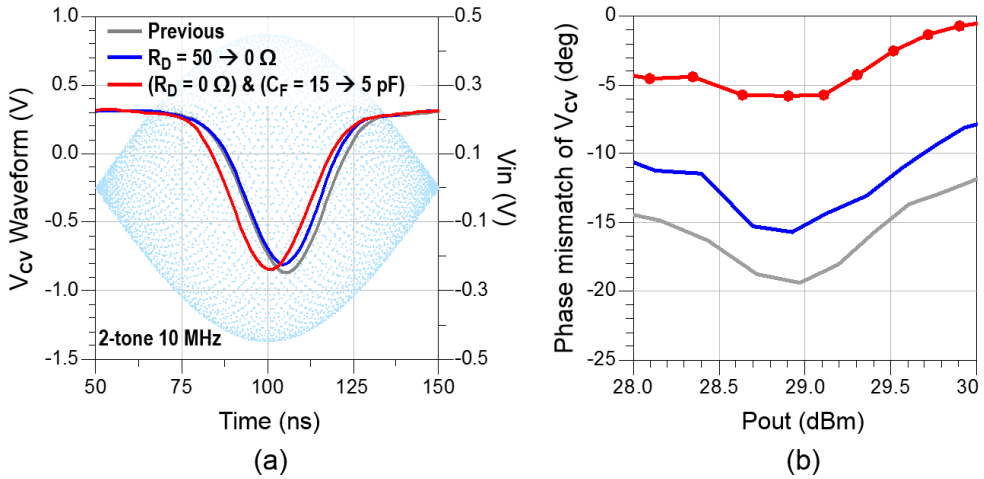


Figure 4.5: Delay correction by reducing R_D and C_F. (a) V_{CV} and incoming RF voltage (V_{in}) waveforms. (b) Phase mismatch of V_{CV}.

(for 2G CDMA and 3G W-CDMA applications), a time delay of several nano-seconds does not affect the linearizer performance. In the case of the signal with 40 MHz BW (for 4G LTE, two-carrier aggregation application), however, a time delay of a few nanoseconds significantly limits the linearization effect. To maintain the linearization effect under wideband signal condition, the amount of phase mismatch must be reduced below 5˚.

4.2.2 Delay Correction

To reduce the time delay (t_d), sub-circuits of the linearizer, which may have excessive RC time-constants, should be redesigned. In the case of PI circuit, the resultant envelope-reshaped signal (V_{CV}) experiences two RC time-constants, one from C_F || R_F (envelope detector) and the other from R_D || C_{B2} (envelope injector) in Fig. 3.31(b). Thus, we have reduced R_D and C_F values to 0 Ω and 5 pF, respectively. Two-tone simulation result of the linear PA with reduced R_D and C_F is plotted in Fig. 4.5. Compared to the previous design with R_D = 50 Ω and C_F = 15 pF (in Chapter 3), the modified design shows better performance in terms of phase

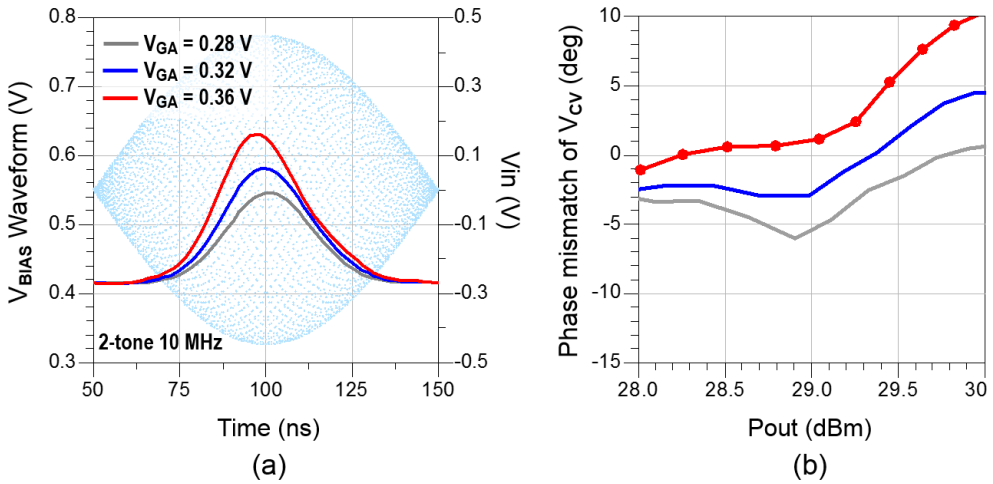


Figure 4.6: Delay correction by increasing V_{GA}. (a) V_{BIAS} and incoming RF voltage (V_{in}) waveforms. (b) Phase mismatch of V_{CV}.

mismatch (less than 6˚ at 10-MHz BW). Since the inverter-like envelope shaper (M_6 and M_7 in Fig. 3.31(b)) contains a parasitic gate capacitance ($C_{g.M6.M7}$), the composite capacitance for low-pass filter in the envelope detector, $C_F + C_{g.M6.M7}$, becomes larger than C_F. Thus, C_F value can further be reduced unless the non-ideal RF filtering significantly limits the linearization effect. Even if R_D was used in initial design to avoid the parallel resonance by C_{B2} and a bond-wire connecting M_7 and V_{P0} in Fig. 3.31(b), the absence of R_D does not cause any stability issue.

Furthermore, additional delay reduction is achieved by increasing the gate-bias of the AI circuit (V_{GA} in Fig. 3.31(b)). Fig. 4.6 shows the V_{BIAS} waveform and phase mismatch of V_{CV} by adjusting V_{GA}. As the V_{GA} value is increased, the phase mismatch of V_{CV} (as well as V_{BIAS}) is compensated, which means that the envelopes of V_{RF} and V_{CV} are getting aligned in-phase. Since a higher V_{BIAS} of a CS amplifier (M_1 in Fig. 3.31(a)) gives rise to larger gate-source capacitance ($C_{gs.M1}$), we can guess that this capacitance according to V_{BIAS} provides a time-delay to match V_{CV} (and V_{BIAS}) and V_{RF} in phase, even if the exact mechanism cannot be explained due

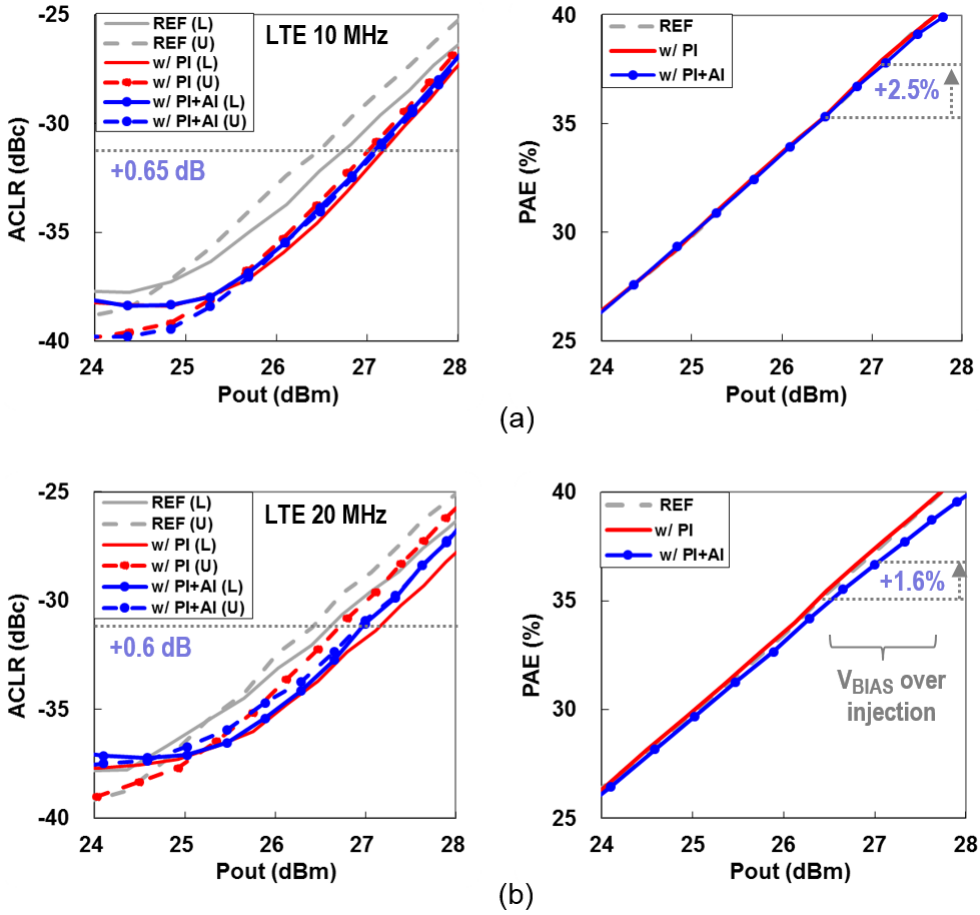


Figure 4.7: Measured LTE results of the 1.88 GHz linear CMOS PA after adjusting $R_D/C_F/V_{GA}$. (a) 10-MHz BW result. (b) 20-MHz BW result.

to the recursively connected structure between the envelope-detection path and V_{BIAS} injection path of the AI circuit.

To demonstrate the linearization effect of the modified linearizer under wideband signal condition, a 1.9 GHz linear PA was fabricated using a 0.28-μm SOI CMOS process (TowerJazz CS18QT1). The baseline design of the PA is almost identical to the PA described in Chapter 3 except for R_D / C_F / V_{GA} values. Three different cases (PI only, PI+AI, and no linearization) are compared; and the measured results are plotted in Fig. 4.7. In the case of 10-MHz LTE operation shown in Fig. 4.7(a), the linear PA exhibited an $ACLR_{E\text{-}UTRA}$ of –31 dBc and a PAE

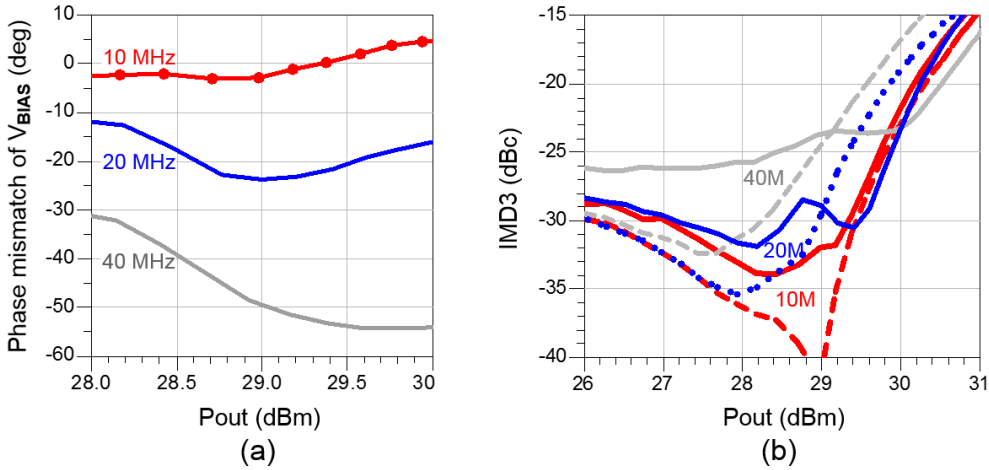


Figure 4.8: Two-tone simulation results of the linear CMOS PA with $R_D/C_F/V_{GA}$ adjustments under 10/20/40 MHz BWs. (a) Phase mismatch of V_{BIAS}. (b) IMD3.

of 37.8% at P_{out} = 27.2 dBm. Compared to the case of no linearization (reference PA), the maximum linear P_{out} and PAE, which are defined by the P_{out} and PAE meeting –31 dBc $ACLR_{E\text{-}UTRA}$, are increased by 0.65 dB and 2.5%, respectively. In the case of 20-MHz operation shown in Fig. 4.7(b), the linearizer also helped the PA achieve linear P_{out} of 0.6-dB higher than that of a reference PA, which improvement is in contrast to the result of Fig. 4.1(b). It should also be noted in Fig. 4.7(b) that the PA with PI+AI showed almost no ACLR asymmetry, compared to the result with PI only. Thus, it is validated that the AI has an effect of delay (t_d) correction, since the ACLR asymmetry (memory effect) is typically caused by the timing mismatch between V_{RF} and V_{CV} (and V_{BIAS}).

Even though the PA maintained the linearization effect at 20-MHz LTE BW, however, the improvement is achieved at the expense of AI (V_{BIAS}) over-injection, thus resulting in limited PAE improvement (1.6%) compared to the 10-MHz BW case (2.5%). Also, the linearizer still showed no measurable linearity improvement under the 40-MHz BW LTE signal (even with not shown here). As one can see from the simulated phase mismatch and IMD results in Fig. 4.8, this linearizer

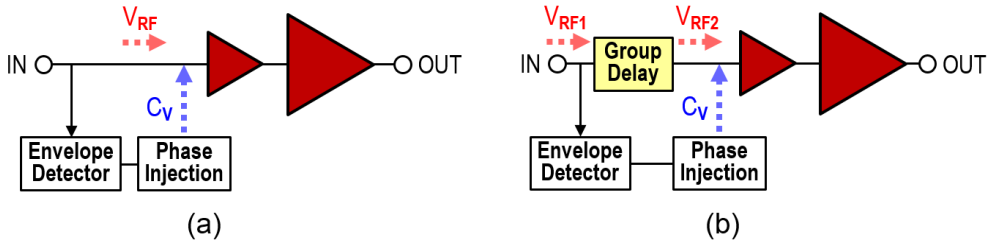


Figure 4.9: Envelope-detection structures. (a) Feedforward (FF) detection. (b) Feedforward/group-delay (FF/GD) detection.

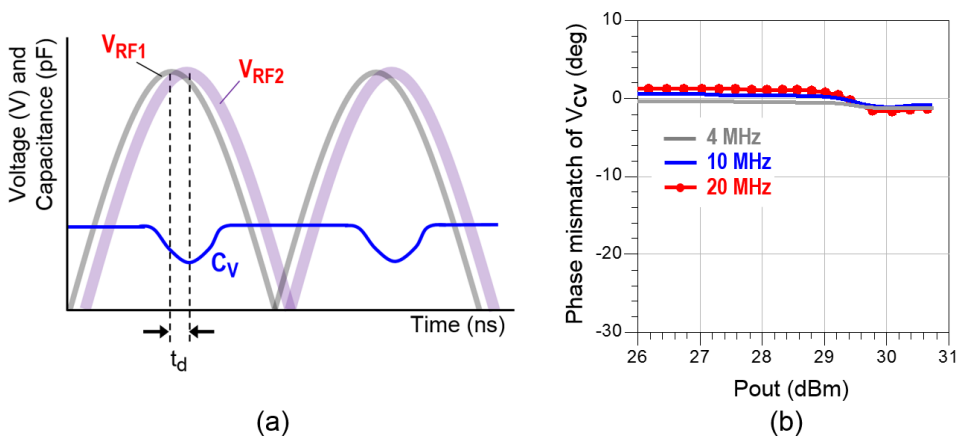


Figure 4.10: (a) Time-adjusted input RF signal (V_{RF2}) by the delay circuit. (b) Simulated phase mismatch of V_{CV} for various tone-spacings.

topology practically corrects for the nonlinearity only if the signal BW is less than 10 ~ 15-MHz. Thus, more effective linearization technique is required to overcome the limiting effect while maintaining linear PAE improvement.

4.2.3 Feedforward Envelope-Detection Structure with a Delay T/L

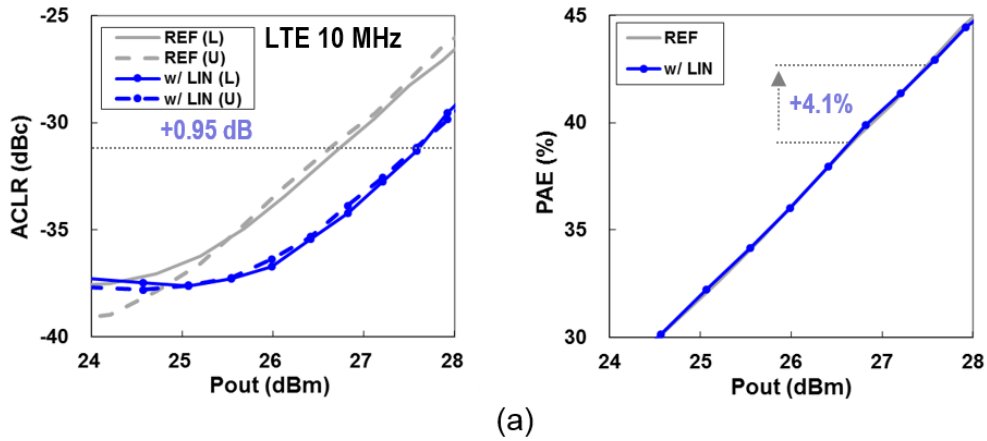
Since the BW limiting effect comes from the time-delay of the envelope-reshaped signal (V_{CV}) during envelope-detection and injection, the timing mismatch can be completely compensated by employing a delay line in the RF path. For this purpose, the envelope-detection structure in Fig. 4.2(a) should be modified to the feedforward (FF) types, as shown in Fig. 4.9. Even if the FF-detection structure in

Fig. 4.9(a) seems to perform better linearization than the feedback-detection structure in Fig. 4.2(a), in reality, both show similar performance. This is due to the fact that the driver-stage consumes far smaller time-delay (< 0.5 ns) than that of the linearizer (2 ~ 3 ns). Thus, the feedforward/group-delay (FF/GD) detection structure shown in Fig. 4.9(b) is proposed in this work. Conceptual time-domain waveforms of the original input signal (V_{RF1}), time-delayed input signal (V_{RF2}), and envelope-reshaped C_V are illustrated in Fig. 4.10(a), where V_{RF2} and C_V are aligned in-phase. The delay correction topology of this work is quite similar to a feedforward PA [1]. If the transmission line (T/L) has a time delay of t_d, its electrical length (phase) at a carrier frequency (f_c), θ_c, is calculated as

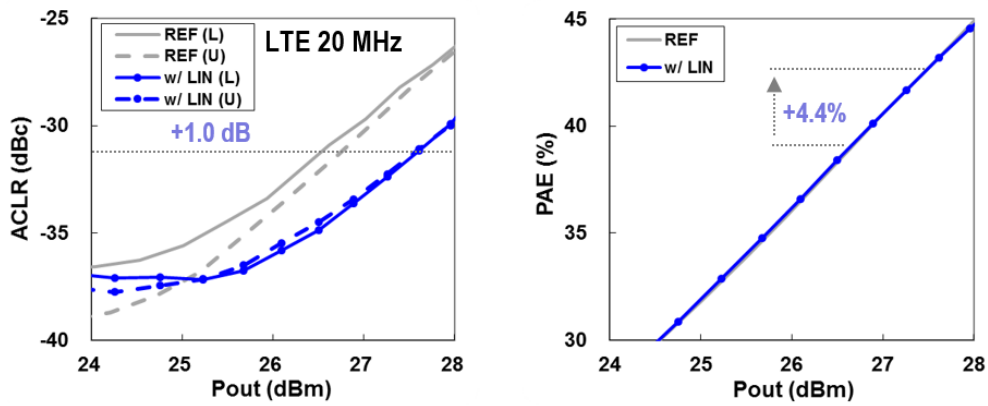
$$\theta_c = 360 \cdot f_c \cdot t_d \tag{4.2}$$

where the unit of θ_c is degree. Two-tone simulation result in Fig. 4.10(b) shows that the designed FF/GD-based linear PA, in which a T/L with a delay of 2.5-ns was employed, exhibits no phase mismatch under 20-MHz (and higher) BW. It should also be noted in Fig. 4.10(b) that the phase mismatch curve is not a function of P_{out} due to the FF-detection structure without AI, which result is in contrast to that of the feedback-detection structure shown in Fig. 4.6(b).

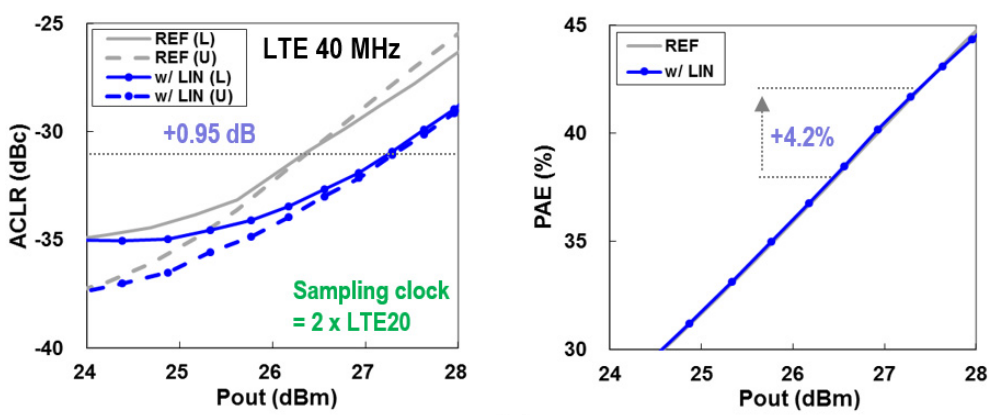
To validate the usefulness of the FF/GD-type phase linearizer, a 0.9 GHz SOI CMOS linear PA with a delay T/L was fabricated and tested. The delay line with a delay of 3 ns, which corresponds to an equivalent electrical length of 972˚ at 0.9 GHz, was implemented on a 25-mil-thick Rogers RT6010 substrate ($\varepsilon_r \approx 10.2$, $\tan\delta = 0.002$) for proof-of-concept. The PA was measured using the 10/20/40-MHz LTE signals, where the 40-MHz BW LTE signal was obtained by doubling the sampling clock of the 20-MHz BW signal in the Agilent E4438C signal generator. The measured $ACLR_{E\text{-}UTRA}$ and PAE of the linear PA are plotted in Fig. 4.11. The PA with FF/GD-type linearizer showed linear P_{out} / PAE improvements of higher than



(a)



(b)



(c)

Figure 4.11: Measured LTE $ACLR_{E\text{-}UTRA}$ of the linear CMOS PA with FF/GD structure for various LTE BWs. Delay was realized with a T/L on a PCB. (a) 10-MHz BW. (b) 20-MHz BW. (c) 40-MHz BW.

TABLE 4.2

MEASUREMENT SUMMARY OF THE LINEAR PA USING A T/L DELAY CIRCUIT

BW (MHz)	$ACLR_{E\text{-}UTRA}$ (dBc)	P_{out} (dBm)	PAE (%)	P_{out} / PAE improvement
10	–31	27.6	43.0	0.95 dB / 4.1%
20	–31	27.6	43.2	1.0 dB / 4.4%
40	–31	27.3	41.7	0.95 dB / 4.2%

0.95 dB / 4.1% over the entire signal BW cases. It should be noted that the measured improvements at 40-MHz BW case is almost identical to the 10/20-MHz BW results, thus validating the usefulness of the proposed FF/GD-type linearizer. The measurement summary of the PA is presented in Table 4.2.

4.3 Group Delay Circuit

The measured result of the PA using a delay T/L above is impressive since no BW limiting effect is observed up to 40-MHz (or higher) LTE BW. However, the electrical length of the T/L is too bulky to be adopted for practical handset PA applications when a delay of several nanoseconds is required, as calculated in (4.2). To reduce the size of delay circuit while obtaining a large group delay, a group delay circuit (GDC) is designed and fabricated in this chapter.

4.3.1 Positive GDC versus Negative GDC

Fig. 4.12 shows block diagrams of the linear PAs with PI circuits and GDCs. Since GDCs reported so far are sub-divided into a positive GDC and a negative GDC [10]-[20], the two types of delay circuits can be adopted in the different paths; a positive GDC is inserted in the RF path as shown in Fig. 4.12(a) whereas a negative GDC is inserted in the envelope-detector path as shown in Fig. 4.12(b). The group delay (GD), which is also called as the “true-time delay”, is defined as

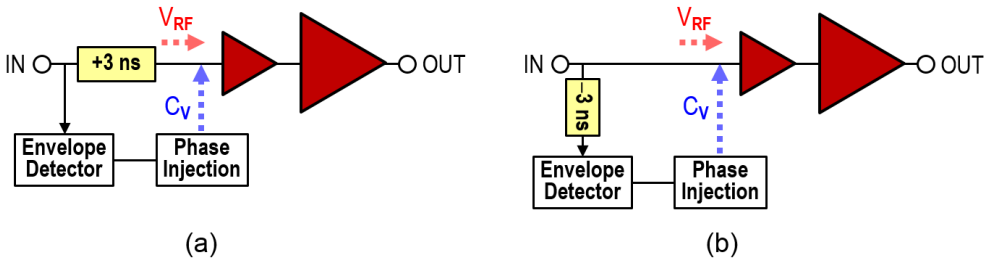


Figure 4.12: Block diagram of the FF/GD-detection type linear CMOS PA using (a) a positive GDC and (b) a negative GDC.

$$GD \equiv \frac{\partial \angle S_{21}}{\partial \omega} \tag{4.3}$$

where ω is the carrier angular frequency ($\omega = 2\pi f_c$), and the units of $\angle S_{21}$ and ω are radian and radian/second, respectively. It is worthwhile to note that the GD of a T/L can directly be calculated from the electrical phase at carrier frequency, as shown in (4.2). However, this relation becomes invalid when the GDC is realized with lumped-elements and transistors, because most RF circuits except T/Ls do not have linear phase characteristics and thus they show dispersive GDs.

Contrary to the positive GD, the negative GD concept is somewhat confusing because the signal which has traveled through a normal material cannot show time-leading property than the incident signal under normal condition (time-causality). As described in [19], the negative GD can only be obtained through the signal attenuation condition, and thus it causes a large power loss. Its usefulness was validated in the feedforward PA [19], since the negative GDC can remove the bulky and lossy output delay line which has a significant impact on power loss and PAE degradation. Even though the loss at the input stage can be compensated by employing a small-signal amplifier for our application, however, it requires / consumes additional biases / dc power. Moreover, negative GDCs typically have narrowband characteristics and thus multi-stage GDCs are required, which further

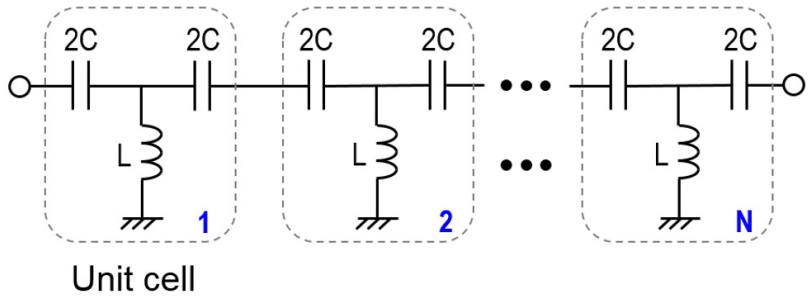


Figure 4.13: Schematic of the left-hand (LH) T/L-based positive GDC.

increase the input power loss (more than 20 dB) [15]-[20]. Due to the practical limit, we have employed a positive GDC. To achieve a large GD while maintaining compact size, a left-handed (high-pass type) T/L-based GDC, whose concept was introduced in [13] and [14], is employed.

4.3.2 Left-Handed T/L-Based GDC

Fig. 4.13 shows a schematic of the left-handed T/L-based GDC with N unit cells. Each unit cell consists of two series capacitors and a shunt inductor. To obtain a delay of several nanoseconds, multiple unit cells are connected in cascade. Since this circuit is a high-pass network, a cut-off frequency (also called as Bragg frequency), f_B, exists [13], [14]. The cut-off frequency (f_B) and GD are derived as

$$f_B = \frac{1}{4\pi\sqrt{LC}} \tag{4.4}$$

$$GD = \frac{2N}{\omega\sqrt{4\omega^2 LC - 1}}. \tag{4.5}$$

The characteristics impedance of the GDC, Z_T, is calculated as

$$Z_T = \sqrt{\frac{L}{C}}. \tag{4.6}$$

To maximize the return loss, Z_T should be close to the system impedance (Z_0).

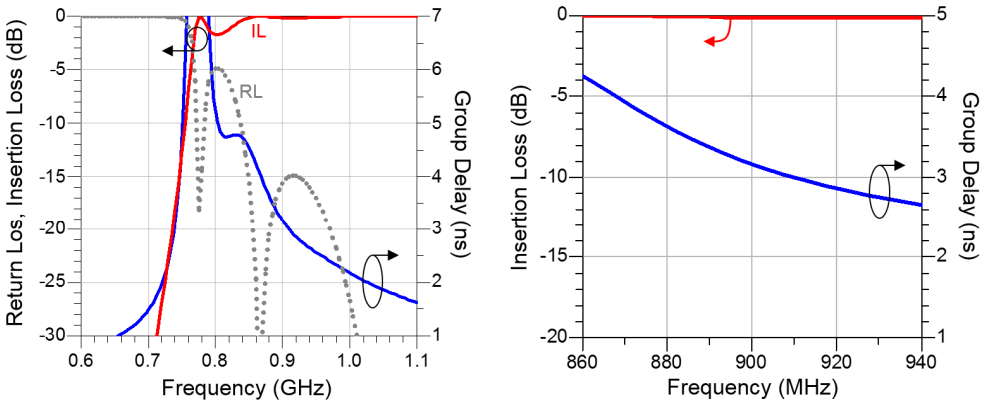


Figure 4.14: Simulated results of the designed 0.9 GHz GDC with 6 unit cells. (a) Return loss, insertion loss, and group delay. (b) Its magnified plot.

Based on the design equations above, a 3.2-ns GDC was designed at 0.9 GHz. The designed circuit has six unit cells, where each cell is composed of $2C$ = 3.0 pF and L = 7.5 nH. Calculation results using (4.4) ~ (4.6) show that each unit cell has a delay of 0.53-ns, and the return loss and cut-off frequency are 15.3 dB and 0.75 GHz, respectively. The simulated return loss, insertion loss, and GD are plotted in Fig. 4.14. It should be noted in Fig. 4.14(a) that the target frequency of the GDC should be at least 100-MHz higher than the Bragg frequency. Since the GDC has a dispersive characteristics in terms of GD, it cannot be adopted for ultra-wideband applications. At 0.9 GHz, the GDC has a delay of 3.2-ns and its ±10% delay bandwidth is 38 MHz (4.2%) while maintaining return loss of better than 15 dB.

To check the feasibility of the GDC in terms of delay dispersion, a circuit envelope simulation was performed using the Agilent ADS. Fig. 4.15 shows the simulated dynamic AM-AM, dynamic AM-PM, and power spectral density of the GDC under 40-MHz BW LTE signal (two-carriers) condition. Even though the dynamic AM-AM and AM-PM show a little bit dispersive characteristics as shown in Fig. 4.15(a) and 4.15(b), however, it does not affect any significant linearity

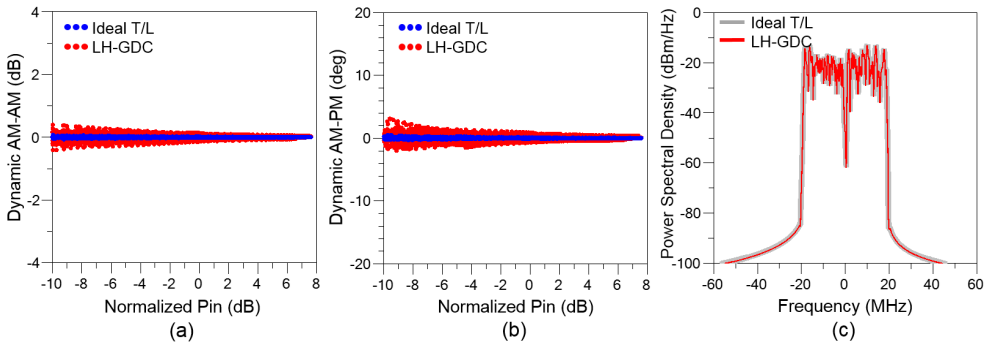


Figure 4.15: Simulated envelope-dispersion characteristics of the designed GDC under the 40-MHz BW (20 MHz, 2-channel) LTE signal. (a) Dynamic AM-AM. (b) Dynamic AM-PM. (c) Power spectra density.

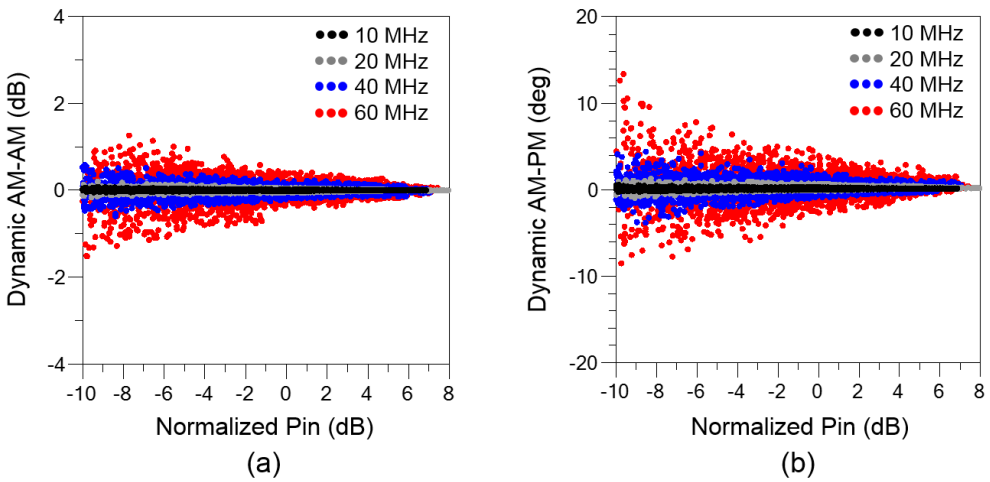
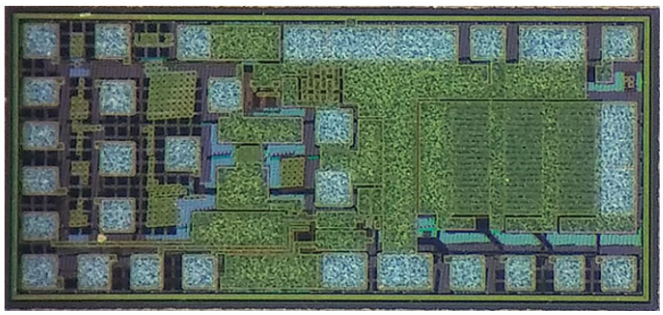
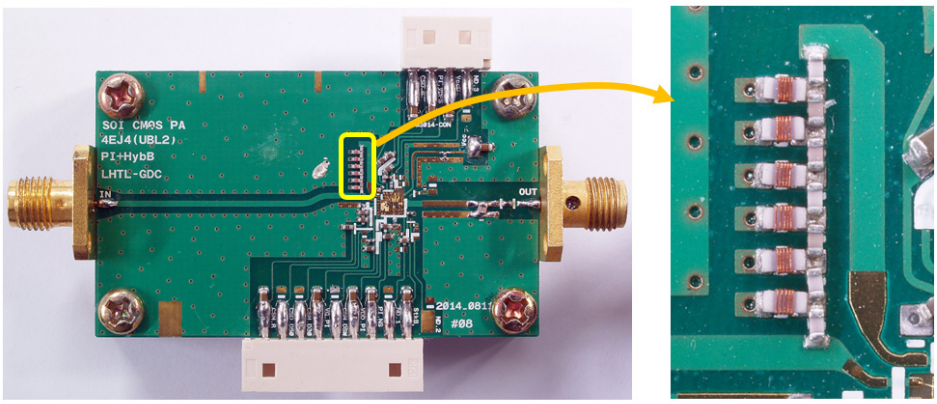


Figure 4.16: Simulated envelope-dispersions of the designed GDC for various BW (10/20/40/60 MHz) signals. (a) Dynamic AM-AM. (b) Dynamic AM-PM.

problem, which is validated through the power spectra plot in Fig. 4.15(c): its adjacent channel power is almost identical to that of an ideal T/L case. The simulated AM-AM/PM dispersion characteristics of the GDC for various LTE signal BWs (10/20/40/60 MHz) are also plotted in Fig. 4.16. In the case of 60-MHz BW LTE signal (three-carriers), the delay difference of the GDC at lower frequency (870 MHz) and upper frequency (930 MHz) is almost 1-ns, as shown in



(a)



(b)

Figure 4.17: Photographs of the fabricated (a) linear PA IC and (b) PA module with an external LH T/L-based GDC.

Fig. 4.14(b). This means that the delay dispersion makes the phase mismatch by 21.6˚ when two-tone input signal is used, as shown in Table 4.1. Thus, the AM-PM dispersion of the GDC becomes larger when higher signal BW is used.

4.4 Fabrication and Measurement

For the proof-of-concept experiment, a 0.9 GHz linear PA was implemented using a 0.28-μm SOI CMOS process (TowerJazz CS18QT1). The IC contains a two-stage PA core and a PI circuit, whose design is almost identical to that of Fig. 3.31 except for the feed-forward detection structure and reduced C_F and R_D values.

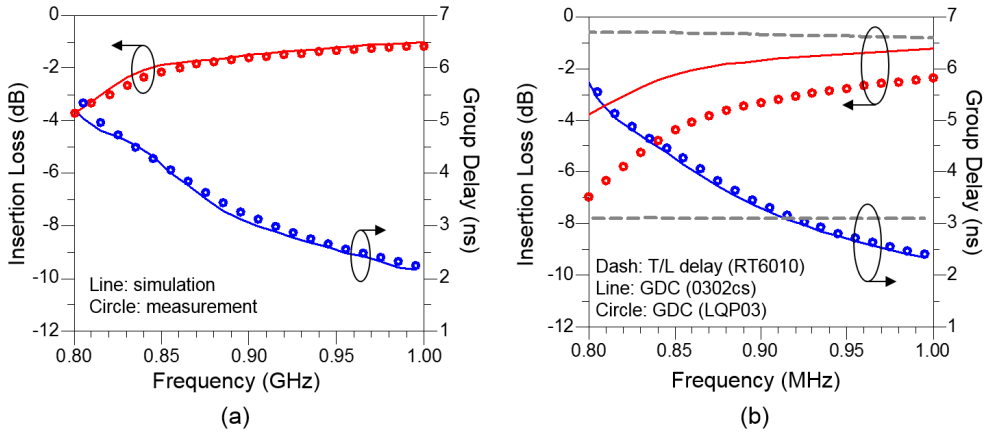
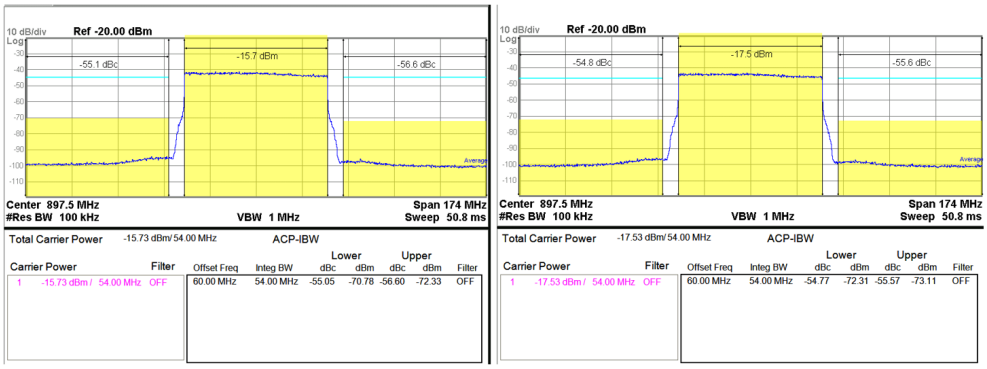


Figure 4.18: (a) Measured insertion loss and group delay of the 0.9 GHz 3.2-ns LH T/L-based GDC. (b) Measured results of a T/L delay (Rogers RT6010), a GDC using the Coilcraft 0302CS inductors, and a GDC using Murata LQP03 inductors.

The series capacitors and shunt inductors of the GDC (in Fig. 4.13) are realized with the lumped capacitors (Murata GJM03) and inductors (Coilcraft 0302CS). Fig. 4.17 shows photographs of the fabricated SOI CMOS IC (size = 1.39 mm × 0.61 mm) PA module. Even if the lumped capacitors are not integrated, they can easily be integrated in an SOI PA IC and thus the size can further be reduced.

4.4.1 GDC Measurement

Prior to the LTE measurement of the overall PA, small-signal characteristics of the GDC were measured using the vector network analyzer. Fig. 4.18(a) shows the measured insertion loss and GD of the GDC. The GDC showed an insertion loss of 1.7 dB and a GD of 3.2-ns at 0.9 GHz, which are almost identical to the simulation results. The GD bandwidth (meeting ±10%) is 45 MHz, which corresponds to the fractional bandwidth of 5%. For more comparison, two GDCs using two different inductor models (Coilcraft 0302CS and Murata LQP03), and a T/L delay circuit on a Rogers RT6010 substrate were also measured and the results are plotted in Fig. 4.18(b). Compared to the T/L delay circuit with a loss of 0.7 dB



(a) (b)

Figure 4.19: Measured $ACLR_{E\text{-}UTRA}$ characteristics using a 60-MHz BW LTE signal. (a) Source signal. (b) GDC.

and GD of 3.1 ns, the two GDCs have a little bit dispersive characteristics in terms of insertion loss and GD near 0.9 GHz. Even though the GDC using the LQP03 inductors showed loss of 1.5-dB higher than the GDC using the 0302CS inductors, almost identical GDs are achieved between the two GDCs.

Fig. 4.19 shows the measured ACLR characteristics of the source signal and GDC under 60-MHz BW LTE signal. As one can see from Fig. 4.19, the GDC does not cause any ACLR degradation (less than –55 dBc for both case), even though large GD dispersion is observed at 60-MHz BW as shown in Fig. 4.16.

4.4.2 LTE Measurement

The measured LTE performance of the linear PA is plotted in Fig. 4.20. In the case of 10-MHz and 20-MHz BW LTE operations, the PA showed $ACLR_{E\text{-}UTRA}$ of –31 dBc and PAE of 44.1% at P_{out} = 28.0 dBm. Thus, the proposed linearizer helps the PA improve the linear P_{out} and PAE by 1.1 dB and 4.5%, respectively, compared to the results without linearizer (standalone PA). In the case of 40-MHz BW LTE operations, the PA showed $ACLR_{E\text{-}UTRA}$ of –31 dBc and PAE of 42.9% at P_{out} = 27.7 dBm, which means that the maximum linear P_{out} / PAE are improved by

TABLE 4.3

MEASUREMENT SUMMARY OF THE LINEAR PA USING THE LH T/L-BASED GDC

BW (MHz)	$ACLR_{E\text{-}UTRA}$ (dBc)	P_{out} (dBm)	PAE (%)	P_{out} / PAE improvement
10	–31	28.0	44.2	1.1 dB / 4.5%
20	–31	28.0	44.1	1.1 dB / 4.5%
40	–31	27.7	42.9	0.85 dB / 3.4%

0.85 dB / 3.4%. Even if the maximum linear P_{out} (meeting –31 dBc ACLR) of the 40-MHz BW case is slightly reduced compared to the 10/20-MHz BW cases, it still validates that the amount of P_{out} improvement is well maintained. Since the standalone PA shows slightly dispersive ACLR characteristics, the PA performance at 40-MHz BW can further be improved when the standalone PA and delay of the GDC are fine optimized. Table 4.3 summarizes the measured LTE results of the PA.

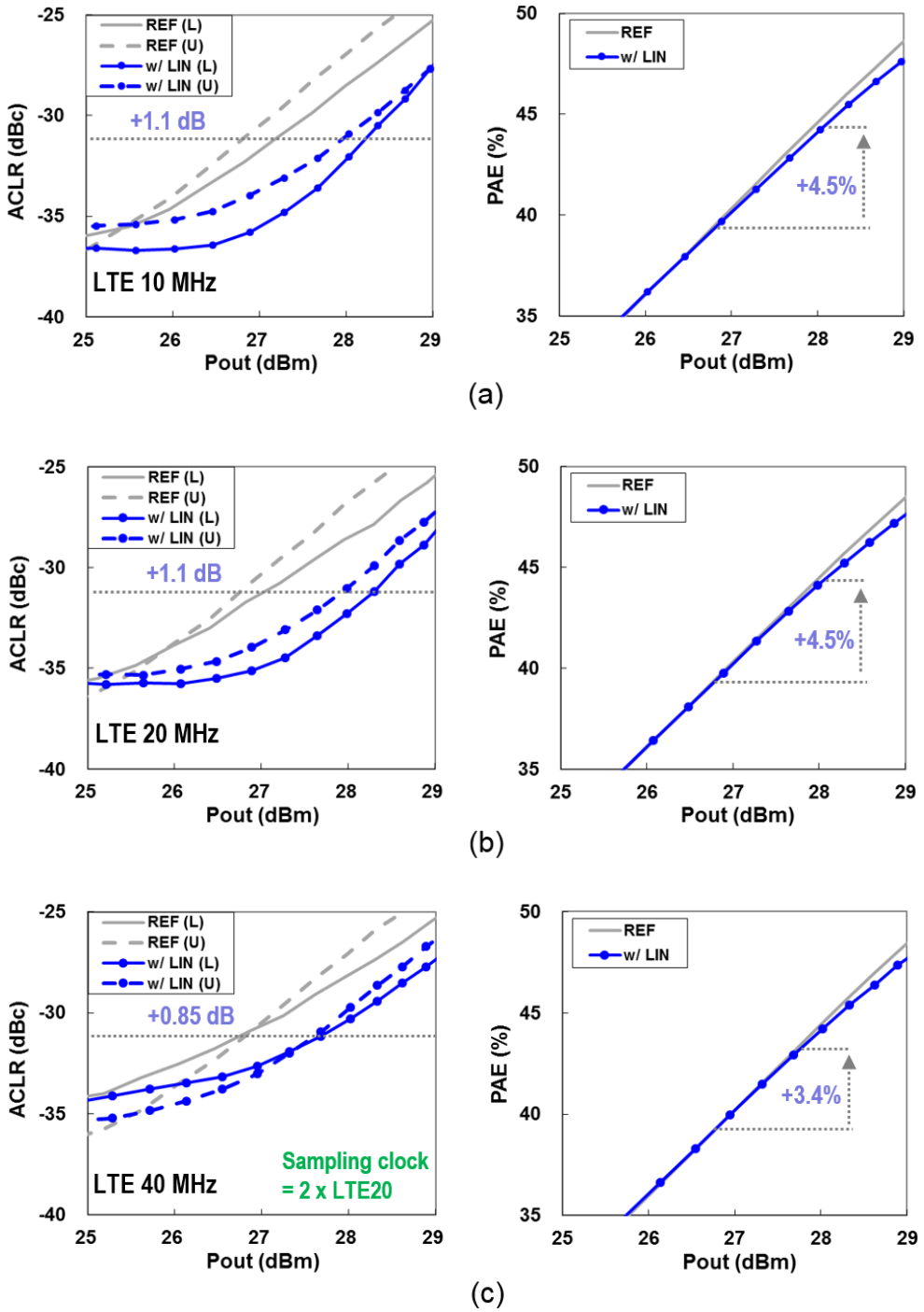


Figure 4.20: Measured LTE results of the fabricated PA with a GDC for various signal BWs. (a) 10-MHz BW. (b) 20-MHz BW. (c) 40-MHz BW.

4.5 Summary

In this work, the BW limiting factor of the envelope-based linearizer has been analyzed and investigated. Analysis showed that the timing mismatch between the incoming RF signal and envelope-reshaped capacitance causes a phase mismatch of the envelope signal, thus significantly degrading the linearization effect under the signal BW of higher than 20 MHz. To resolve the problem, the phase injection (PI) circuit has been modified to the feed-forward-type envelope-detector, and a compact left-handed T/L-based group delay circuit (GDC) have been proposed.

To demonstrate the usefulness of the proposed linearizer, a 0.9 GHz linear CMOS PA was fabricated using an SOI CMOS process. The implemented PA with PI circuit and off-chip GDC achieved linear efficiency (–31 dBc ACLR) of higher than 44% under the 10-MHz and 20-MHz BW LTE signals (16-QAM with PAPR = 7.5 dB). The linearizer also helped the PA to maintain the linearization effect at 40-MHz BW condition: linear PAE of 42.9% and ACLR of –31 dBc.

With the strong demand for wideband signal operation for higher data-rate uplink transmission, the proposed linear CMOS PA can be a practical solution for 4G LTE handset covering wide signal BW of higher than 40-MHz.

4.6 References

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Chapter 5

Conclusions

5.1 Research Summary

In this Dissertation, studies on multiband (MB) reconfigurable structure and linearization of a CMOS handset power amplifier (PA) have been presented. To implement the reconfigurable output matching network (OMN) for 3G/4G multiband PAs, a design methodology has been presented together with details of closed-form design equations. The analysis shows how the power, frequency, and output-path reconfigurable networks can be co-designed with a fixed OMN to reduce the overall size and loss. To demonstrate the usefulness of the proposed reconfigurable networks, a 5 mm × 6 mm tri-band PA module, which covers either band 1/2/5 or band 1/4/8, has been fabricated for 3G handset applications using GaAs HBT process and multi-layer substrate. Measured W-CDMA results of the PA meets the UMTS linearity requirement with margin (–39 dBc ACLR) at all the target frequency bands while maintaining minimal efficiency degradation (less than 2% compared to a single-band dedicated PA), thus validating the usefulness of the proposed reconfigurable OMN.

To achieve high linear efficiency of a CMOS PA, a phase-based linearization has been proposed. The proposed phase (capacitance) injection circuit is composed of an envelope-detector and an envelope-shaper with a varactor. The envelope-reshaped capacitance by the linearizer effectively corrects for the dynamic AM-PM distortion and helps the PA recover the dynamic AM-AM as well. In addition, a hybrid bias is employed to set the power-dependent static bias to help recover the linearity at backed-off power levels. Together with the standalone stacked-FET PA design and the auxiliary amplitude injection/hybrid bias, the fabricated AM-PM linearizer helps the 1.88 GHz and 0.9 GHz SOI CMOS linear PAs achieve best linear efficiencies among the reported CMOS PAs. Then, the MB reconfigurable structure and linearization technique have been combined together to implement a single-chain MB reconfigurable linear CMOS PA for practical 3G/4G handset PA applications. The single-chain PA supports any combination of two bands, one from the low-band (0.8 ~ 0.9 GHz) group and the other from the high-band (1.7 ~ 2.0 GHz). The fabricated MB CMOS PA showed minimal efficiency degradation (less than 3.3%) compared with the single-band dedicated PA with W-CDMA PAEs in excess of 46% for low-band and 40.7% for high-band.

Finally, the signal-bandwidth limiting effect of the above linearizer has been analyzed and a solution has been proposed. The analysis reveals that the timing mismatch between the incoming RF signal and envelope-reshaped signal, which comes from the envelope detector and shaper, makes the linearizer limit the linearization effect of the overall PA below 10 ~ 15 MHz LTE bandwidths. This problem has been resolved by employing a delay transmission line (T/L) with a delay of 2 ~ 3 ns. To remove the bulky T/L while maintaining the linearization effect under 40 MHz and higher LTE bandwidths, a compact left-handed T/L-based group delay circuit has been adopted for practical application. The fabricated feedforward-detection-type SOI CMOS linear PA with the delay circuit showed its

linearization effect under the 40 MHz uplink LTE signal condition.

With the strong demands for MB coverage and wideband signal operation of the 3G/4G mobile communication standards, the proposed reconfigurable linear CMOS PA can be a practical solution for UMTS/LTE multiband Tx applications.

5.2 Future Works

The study discussed in Chapter 4 has two future works for size miniaturization and further linearity improvement. Even though the linear CMOS PA with phase-injector and group delay circuit (GDC) showed its usefulness under the 40-MHz bandwidth LTE signal, the number of unit cells in the GDC is relatively excessive and thus the use of six external SMT inductors cannot be acceptable for practical handset PA requiring compact size and low cost. Thus, an additional effort is demanded to further reduce the time delay. Since the envelope shaper also contributes for the time delay, it can be removed to obtain smaller delay while compromising the linearizer performance. As a result, a small form-factor of the PA module can thus be achieved.

For stronger linearity improvement, a multi-section configuration of the phase injector can be proposed. Since the phase injector may cause the problems on the return/insertion losses and RF bandwidth when a single phase injector employs an excessive varactor capacitance, the multi-section phase injector (e.g. low-pass pi-network) is able to reduce the burdens of losses and RF bandwidth while achieving stronger dynamic AM and PM corrections. If the two solutions proposed above are combined together, the CMOS linear PA can achieve further linearity improvement with a small form-factor, even with wider signal bandwidths.

초 록

본 논문에서는 재구성이 가능한 다중대역 선형 CMOS 전력증폭기에 관한 연구를 수행하였다. 오늘날 3세대 UMTS 및 4세대 LTE 이동통신 주파수 대역은 나라와 지역별로 다양하게 분포되어 있기 때문에, 단말기용 전력증폭기는 이러한 많은 주파수 대역을 지원해야 한다. 또한, 고속 데이터 송수신의 시대가 도래함에 따라, 전력증폭기는 넓은 대역폭을 가진 신호에 대해서도 선형 증폭을 해야 한다. CMOS 공정을 이용한 전력증폭기 회로 제작이 가격과 크기 측면에서 이점이 있으나, CMOS 소자의 낮은 항복전압 및 비선형 특성으로 인해 와트(Watt) 단위의 선형 CMOS 전력증폭기를 설계하는 것은 매우 어렵다.

위와 같은 요구와 문제를 해결하기 위해, 본 논문에서는 다중대역 선형 CMOS 전력증폭기에 적합한 두 가지 방법(재구성이 가능한 다중대역 정합 구조와 선형화 기법)을 제안한다. 제안된 재구성이 가능한 다중대역 정합 구조는 비슷한 주파수 대역 그룹 내에서는 크기를 줄이기 위해 증폭기 코어를 공유하며, 전력/주파수/출력포트를 재구성할 수 있는 회로망을 포함한다. 따라서, 이 구조는 복수의 주파수와 전력을 가진 주파수 대역 그룹을 지원할 수 있다. 이와 같은 재구성 방법을 본 논문에서는 정량적으로 분석하였고, 실험적으로 검증하였다. InGaP/GaAs HBT 공정으로 제작한 재구성이 가능한 삼중대역 (tri-band) UMTS 전력증폭기는 각각의 단일밴드 전력증폭기의 최대 선형 효율 대비 2% 이하의 낮은 효율 감소를 보여주었다.

CMOS 전력증폭기의 선형화를 위해서는 위상 기반의 선형화 기법이 제안되었다. 전력증폭기의 비선형성은 변조신호의 dynamic AM-AM 및 AM-PM에 의해 결정되므로, 선형화를 위해 이 두 가지가 동시에 고려되어야 한다. 이전에 제시된 선형화는 주로 신호 포락선(envelope) 기반의 바이어스를 공통-소스 FET의 gate에 공급하는

방법임에 반해, 제안된 AM-PM 선형화 기법은 전압-제어 캐패시터(varactor)와 포락선-재형성 (envelope-reshaping) 회로를 사용한다. 또한, 이 방법은 AM-AM 선형성 역시 개선할 수 있다. 제안된 선형화 기법의 성능을 검증하기 위해 1.88 GHz / 0.9 GHz stacked-FET 전력증폭기가 SOI CMOS 공정을 통해 제작되었다. 측정 결과, 이 회로는 1.88 GHz / 0.9 GHz 에서 (-39 dBc의 W-CDMA ACLR을 만족하면서) 각각 44% / 49% 의 선형 효율을 보여주었다. 더 나아가, 단일-체인의 다중대역 선형 CMOS 전력증폭기도 위에서 설명한 두 가지 기법을 적용하여 SOI 공정으로 구현하였다. 제작된 다중대역 전력증폭기는 두 개의 출력과 다섯 개의 UMTS/LTE 주파수 대역을 지원하며 (824-1980 MHz), W-CDMA 선형 효율을 40.7% 이상 유지하면서도, 단일대역 전용 CMOS 전력증폭기 대비 3.3% 이하의 낮은 효율 감소를 보였다.

마지막으로, 앞서 설명한 CMOS 전력증폭기의 선형화 방법이 신호 대역폭의 증가에 따라 선형화의 크기가 감소하는 문제에 관해 논의하였고, 해결책을 제안하였다. 들어오는 RF 입력신호와 포락선-재생성을 통해 생성된 선형화 신호 간의 시간적인 지연 차이로 인해, 앞서 제시했던 선형화기의 선형화 효과는 신호 대역폭이 증가할수록 (LTE 20 MHz 또는 그 이상의 대역폭에서) 크게 감소한다. 이 문제를 해결하기 위해 작은 크기를 가진 군 지연 회로(group delay circuit)를 본 전력증폭기에 적용하였고, 측정 결과, 선형화 효과는 40 MHz 이상의 넓은 대역폭을 가진 LTE 신호에 대해서도 유지가 됨을 확인하였다.

주요어: CMOS, 선형화, LTE, 다중대역, 전력증폭기, 재구성이 가능한, SOI, stacked-FET, W-CDMA

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