공학박사학위논문

A Study on Ditherless CDR with Optimal Phase Detection

최적 위상 검출 회로를 이용한 클럭 및 데이터 복원 회로에 관한 연구

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이 논문을 공학박사 학위논문으로 제출함
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박명재의 공학박사 학위논문을 인준함
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Abstract

Bang-bang phase detectors are widely used for today's high-speed communication circuits such as phase-locked loops (PLLs), delay-locked loops (DLLs) and clock-and-data recovery loops (CDRs) because it is simple, fast, accurate and amenable to digital implementations. However, its hard nonlinearity poses difficulties in design and analyses of the bang-bang controlled timing loops. Especially, dithering in bang-bang controlled CDRs sets conflicting requirements on the phase adjustment resolution as one tries to maximize the tracking bandwidth and minimize jitter. A fine phase step is helpful to minimize the dithering, but it requires circuits with finer resolution that consumes large power and area. In this background, this dissertation introduces an optimal phase detection technique that can minimize the effect of dithering without requiring fine phase resolution. A novel phase interval detector that looks for a phase interval enclosing the desired lock point is shown to find the optimal phase that minimizes the timing error without dithering. A digitally-controlled, phase-interpolating DLL-based CDR fabricated in 65nm CMOS demonstrates that it can achieve small area of $0.026mm^2$ and low jitter of 41mUIp-p with a coarse phase adjustment step of 0.11UI, while dissipating only 8.4mW at 5Gbps. For the theoretic basis, various analysis techniques to understand bang-bang controlled timing loops are also presented. The proposed techniques are explained for both linearized loop and non-linear one, and applied to the evaluation of the proposed phase detection technique.

Keywords: Bang-bang control, dither, ditherless, clock-and-data recovery

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Chapter 1
Introduction

1.1 Motivations

Many timing loops in today's high-speed communication circuits, such as phase/delay-locked loops (PLL/DLLs) and clock-and-data recovery loops (CDRs), use binary, also known as bang-bang phase detection since their circuit implementations are simple, fast, accurate and amenable to digital implementations. The BBPD compares the phases between the reference input and the feedback clock and tells only about the polarity of the phase error. As it does not measure the magnitude of the phase error, it is suitable for simple implementation and high-speed operation. In addition, it is accurate because most of them measures the phase error based upon the sampled inputs. This characteristic is important for the CDRs, as their purpose is to find the optimal sampling phase for the sampling receivers.

However, its hard nonlinearity poses some difficulties in design and analyses of the BBPD. First, traditional linear analysis including the concepts of loop bandwidth and phase margin cannot be applied directly. Secondly, the quantization noise generated from the BBPD affects the output clock jitter. Thirdly, its loop characteristic changes according to the amount of noise in the input stream. For example, it will be shown that the noise filtering bandwidth gets narrower when the input stream includes larger random noise. Lastly, the bang-bang controlled system does not converge to one stable point but wanders around there, which is called

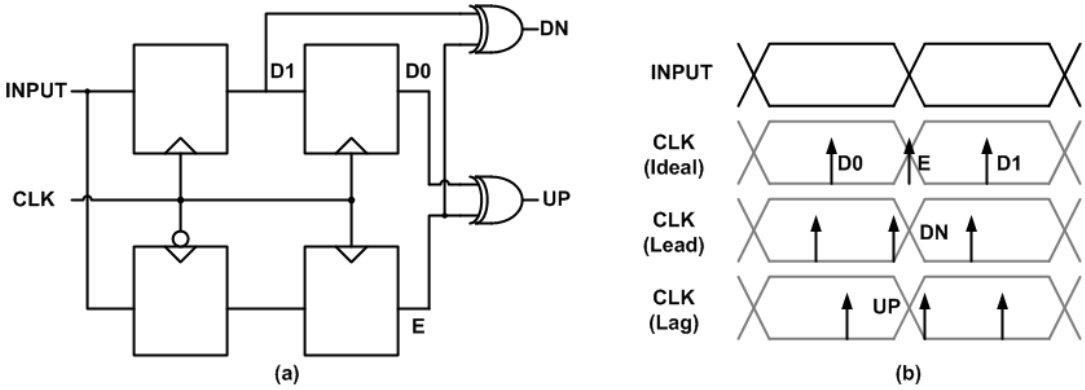


Figure 1.1: (a) Circuit diagram of Alexander phase detector and (b) its timing diagram for ideal/lead/lag cases.

dithering.

As an example, the Alexander PD [1], the most well known implementation of BBPD is shown in Fig. 1.1. It is basically a 2x oversampling phase detector where two samples - data sample and edge sample - are made per one bit to measure the phase difference between the sampling clock and the center of the bit duration. The outputs of upper two flip-flops (D0 and D1) are data samples, whereas the final output of the lower branch (E) is the edge sample that contains the phase information. Assuming that the ideal data sampling point is the center of the bit duration, it detects the relative position of the bit boundary from the edge sampling clock. When the bit boundary is prior to the edge sampling clock, it means that the sampling clock is lagging and vice versa. For example, if D0 and E have different values, it means that the sampling phase leads, and UP signal is asserted. Likewise, when E and D1 have different values DN signal is asserted.

In response to the polarity of the phase error measured by BBPD, the bang-bang controlled loop can only make a fixed amount of adjustment, no matter how large or small the phase error is. A typical BB controlled loop consists of a BBPD, a

loop filter and a clock generator as shown in Fig. 1.2. If the transfer function of the loop filter is $G_{LF}(s) = A_{prop} + A_{integral}/s$ and the gain of the clock generator is K_{clkgen}, the phase change of the sampling clock per each decision cannot be less than $A_{integral}K_{clkgen}T_{ref}$ where T_{ref} is the interval between consecutive phase detections.

This gives rise to a range of phenomena that are unique to bang-bang controlled loops. For instance, even when the CDR clock phase is far from the desired position, the bang-bang CDR can advance its phase only in fixed steps and the phase transient exhibits a linear slewing behavior rather than an exponentially converging one. Simply put, bang-bang controlled loops can have a vastly different response to the input depending on its magnitude, which is not a phenomenon found in linear controlled loops.

One of the most important characteristic of bang-bang controlled loop is its dithering behavior. When the feedback phase is in proximity to the lock position, the loop keeps moving its phase by the same fixed amount every cycle and the phase displays an alternating phase which is called dithering. Assuming there is no frequency offset between the input bit stream and the sampling clock, the output phase alternates between two phases as shown in Fig. 1.3 (a). Dual-loop DLLs [2] or blind oversampling architectures [3] operating in synchronous or meso-chronous configuration fall in this category. In the aforementioned example, the dithering amount will be $(A_{prop} + A_{integral})K_{clkgen}T_{ref}$ assuming less than one T_{ref} of loop delay. On the other hand, in a system that has small frequency difference between the transmitter and the receiver, the relative position of the reference phase drifts over time, and the loop must track the phase drift. For example, the average output phase of conventional charge-pump PLL-based CDRs [4] gradually decreases while

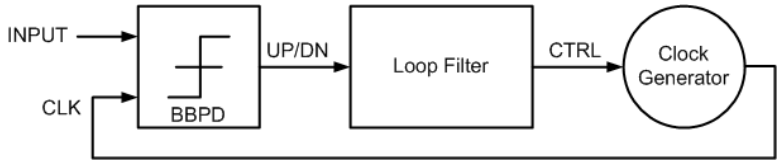


Figure 1.2: Bang-bang controlled timing loop.

alternating up and down as shown in Fig. 1.3 (b). Assuming that the control voltage of the VCO due to the integral path and proportional path are V_0 and V_{prop}, respectively, the control voltage is $V_0 + V_{prop}$ when the BBPD decides UP, while it is V_0 when the BBPD decides DN. Therefore, the output phase decreases by

$$\Delta\phi = \frac{1}{K_{VCO}V_O} - \frac{1}{K_{VCO}(V_0 + V_{prop})} \tag{1.1}$$

per each alternation cycle of UP and DOWN where K_{VCO} is the gain of the VCO. The otput phase keeps decreasing until it crosses $\phi_{REF} - \phi_{BB}$ and generates two consecutive UPs.

The effect of dithering increases when the system has a long loop delay between phase detection and output phase adjustment [5]. If the loop delay is N_d update cycles, it takes N_d cycles for the decision to be reflected to the output, which results in dithering with the magnitude of $2(N_d + 1)$ cycles, and duration of $4(N_d + 1)T_{ref}$.

As the dithering is the dominant factor of deterministic jitter in most of bang-bang controlled systems, careful analyses and design efforts are necessary to minimize its effect. For the CDRs, the increased deterministic jitter can cause the reduction of sampling timing margin, and hence the increased bit-error rate (BER). Considering that the bit error rate under gaussian random noise increases exponentially as the sampling margin decreases, securing the sampling timing margin is important for the CDRs, especially for the ones adopted in high-speed I/Os.

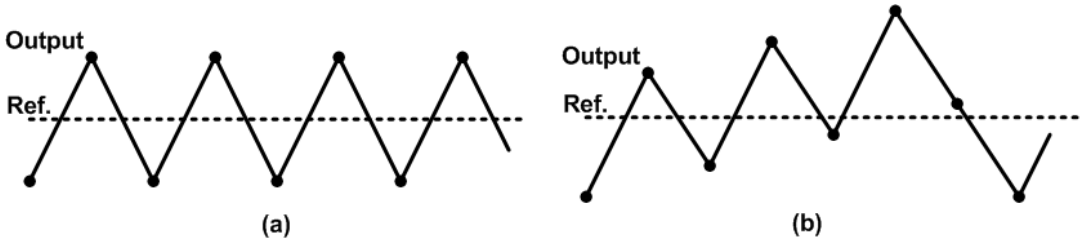


Figure 1.3: Dithering behavior of (a) the systems with quantized selectable phases and (b) the systems with infinite resolution of phases.

A fine phase step is helpful to minimize the dithering, but it requires circuits with finer resolution that consumes large power and area. Fig. 1.4 shows inverter-based phase interpolators with interpolating ratios of 1/2, 1/3 and 1/4. As the minimum achievable inverter size is limited, the area of the interpolator increases quadratically with the phase resolution. At the same time, the power consumption increases linearly assuming that only the inverters contributing the selected output are turned on, but it usually increases faster than linear because the parasitic capacitances of unused inverters contribute to the loading of the buffers. For example, the gate capacitances on ϕ_i node increases from $3C_{inv}$ to $10C_{inv}$ while the interpolating ratio changes from 1/2 to 1/4. The tradeoff between the CDR's tracking bandwidth and dithering magnitude also hinders the use of fine phase resolution. As the bang-bang controlled loops tracks the input phase with a fixed amount per each update cycle, a fine phase resolution can cause slower tracking bandwidth.

With this background, this dissertation proposes a novel phase detection technique that can eliminate the dithering. The increased sampling timing margin attained from the proposed technique enables the system to adopt coarse phase resolution, and achieves small area and low-power operation. Moreover, various analysis techniques to predict the performance of the bang-bang controlled systems are pro-

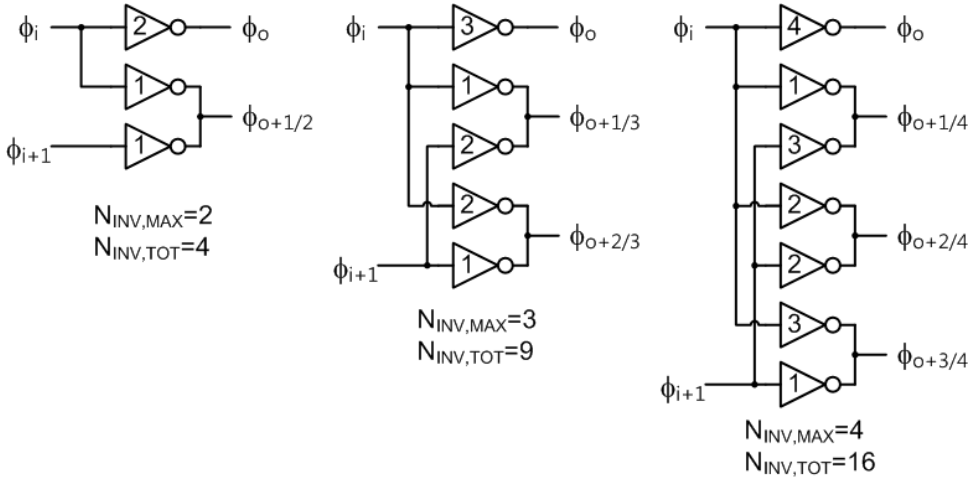


Figure 1.4: Implementation of inverter-based phase interpolators with interpolating ratios of 1/2, 1/3 and 1/4.

posed and applied to the evaluation of the suggested phase detection technique.

1.2 Thesis Contribution and Organization

This dissertation proposes a ditherless CDR and its analysis techniques that can be applied to wide range of bang-bang controlled timing circuits.

Previous efforts to analyze the behavior of bang-bang controlled loops can be largely classified into two categories: the ones that analyze the loop directly as a nonlinear system and the ones that model the system as an equivalent linear system. Without the presence of random noise, nonlinear behaviors such as the aforementioned dithering and slewing determine the majority of the loop's steady-state characteristics, including the clock jitter and loop's tracking bandwidth. Hence, in this case, the system is best modeled as a nonlinear one. On the other hand, with sufficient noise present in the system, a bang-bang controlled system can be modeled effectively as a linear one in a stochastic sense.

This dissertation presents analysis techniques applicable to bang-bang controlled CDRs for both linearized loop and non-linear one. Recently, various techniques were reported to analyze bang-bang controlled PLLs, but there was still no solution to predict the detailed shape of the JTOL curve of CDRs including the effect of additional random or deterministic jitter. On the contrary, the analysis techniques proposed in this dissertation can accurately predict the behavior of CDRs including various design parameters such as transition density, random noise, decimation and dead-zone width.

Chapter 2 describes an accurate, yet analytical method to predict the key characteristics of a bang-bang controlled timing loop: namely, the jitter transfer (JTRAN), jitter generation (JG), and jitter tolerance (JTOL). The analysis basically derives a linearized model of the system, where the bang-bang phase detector is modeled as a set of two linearized gain elements and an additive white noise source. This phase detector (PD) model is by far the most extensive one in literature, which can correctly estimate the effects of random jitter, transition density, and finite loop latency on the loop characteristics. The described pseudo-linear analysis assumes the presence of random jitter at the PD input and the minimum jitter necessary to keep the linear model valid is derived, based on a describing function analysis and Nyquist stability analysis. The presented analysis re-confirms the findings of prior theories and provides theoretical basis to the prior empirically-drawn equations, such as those for the quantization noise power and the gain reduction in presence of a finite loop delay.

Chapter 3 explains various analysis techniques to analyze the bang-bang controlled loop when it is not linearized. Especially, Markov-chain model analysis pre-

viously applied to the analysis of all-digital PLLs [6] are extended to include various design factors of CDRs such as loop delay, transition density, deadzone width and decimation. While explanation, it shows that the optimal deadzone width is a half of minimum phase resolution in the respect of low BER and high bandwidth, which gives the theoretic basis of the proposed phase interval detector.

Based upon the aforementioned analyses, Chapter 4 introduces a novel phase interval detector that looks for a phase interval enclosing the desired lock point to find the optimal phase that minimizing the timing error without dithering. A digitally-controlled, phase-interpolating DLL-based CDR fabricated in 65nm CMOS demonstrates that it can achieve low jitter of 41-mUI_{pp} with a coarse phase adjustment step of 0.11-UI, while dissipating only 8.4mW at 5Gbps. Measurement results verifies that the loop does not dither unless there are two sampling phases that give similar results. In addition, an on-chip measurement technique for characterizing the jitter tolerance (JTOL) of high-speed receivers is presented. The proposed technique emulates the SJ in the off-chip input data stream with a SJ in the on-chip recovered clock of the clock-and-data recovery loop (CDR), allowing an ordinary transmitter to be used as the input source.

Chapter 2
Pseudo-Linear Analysis of Bang-Bang Controlled Loops

BBPD's strongly nonlinear transfer characteristic hinders the use of long-established design insights and practices of linear PLL/DLLs. This chapter presents an analysis technique that derives the equivalent linear model of a bang-bang controlled timing loop so that its key characteristics, such as jitter generation (JG), jitter transfer (JTRAN) and jitter tolerance (JTOL), can be accurately predicted and the design trade-offs among those characteristics can be reasoned based on the familiar linear system theories.

2.1 Model of a Second-Order, Bang-Bang Controlled Timing Loop

Before delving into the proposed analyses, this section defines the analytical model of a second-order, bang-bang controlled loop and its associated design parameters.

Fig. 2.1 shows the discrete-time model of the second-order, bang-bang controlled PLL whose loop filter is made of two control paths: a proportional control path that updates the VCO phase by ϕ_{bb} (rad) and an integral control path that updates the VCO frequency by $\phi_{bb}/(\tau_N T_{ref})$ (rad/s) upon the detection of the phase error polarity at each update cycle (T_{ref}). The loop filter can be implemented either as analog circuits (e.g., a charge pump followed by a series-RC filter) or as digital

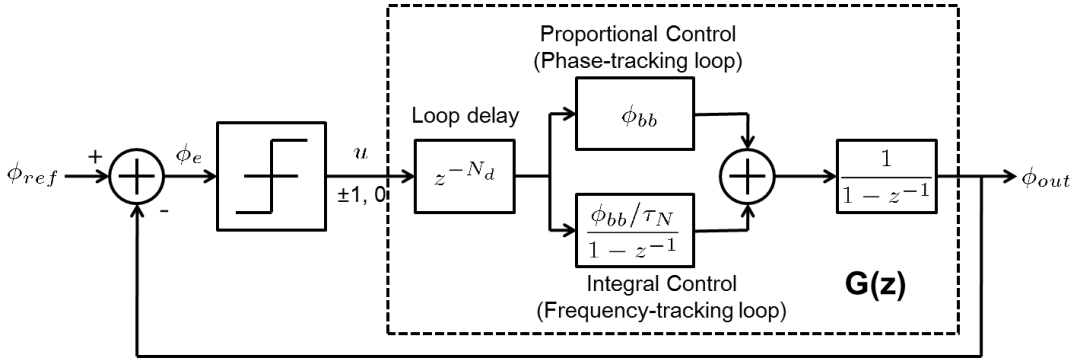


Figure 2.1: A discrete-time model of a second-order, bang-bang controlled PLL with normalized loop parameters.

logic (e.g., a scaler, an accumulator and a summer). Higher-order control terms in the loop filter can be ignored for simplicity, unless the intra-cycle behavior is concerned [7].

We model the bang-bang phase detector (BBPD) as a slicer that provides the discrete output levels of +1, -1, and 0 each indicating that the output phase is 'late', 'early' or 'neutral (in case of no transition)', respectively according to the following equation:

$$u(t) = \begin{cases} sgn\left(\phi_e\left(t\right)\right) & \text{if there is transition} \\ 0 & \text{otherwise} \end{cases}$$

The VCO is basically modeled as a phase accumulator that accrues all the phase shifts requested by the loop filter in the past. The phase shift includes both the proportional phase shift ϕ_{bb} and the phase shift resulting from the error in the integral control's frequency.

Note that we added a delay element $z^{-(N_d+1)}$ in the loop filter, modeling the raw latency of N_d update cycles around the loop. The additional one cycle delay reflects the inherent delay of a discrete-time, sampled-data system. In other words, a

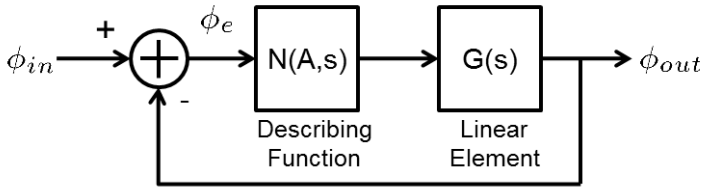


Figure 2.2: General model of non-linear feedback system.

discrete-time system cannot detect a change in a signal until it samples that change at the next cycle. It should be noted that including the loop delay in the PLL model is essential in describing the unique behavior of a bang-bang controlled PLL, such as dithering [5], slewing (i.e. slope overloading) [8] and pull-in force inversion [9].

Apart from the BBPD, which is modeled as the slicer, the rest of the system is linear. The discrete-time transfer function $G(z)$, from the slicer output u to the output clock phase ϕ_{out}, can be expressed as:

$$G(z) = \frac{\phi_{bb}}{\tau_N} \cdot \frac{1 + \tau_N(1 - z^{-1})}{(1 - z^{-1})^2} z^{-(N_d+1)} \tag{2.1}$$

Often, it is more convenient to use a continuous-time version of $G(z)$. An approximate continuous-time transfer function can be obtained by substituting $e^{-sT_{ref}} \approx 1 - sT_{ref}$ for z^{-1}, assuming that the frequency of interest is much lower than the Nyquist frequency (i.e., one half of the BBPD update frequency),

$$G(s) = \frac{\phi_{bb}}{\tau_N T_{ref}^2} \frac{1 + \tau_N T_{ref} s}{s^2} e^{-sT_{ref}(N_d+1)} \tag{2.2}$$

where T_{ref} is the update period of the loop.

The model presented here can be applied to a wide class of bang-bang controlled timing circuits other than the second-order PLL-based CDRs, including semi-digital

dual-loop DLLs [2], blind oversampling CDRs [3] and phase-rotating PLLs [10]. Some timing circuits are first-order loops in nature without the integral control paths, in which case the integral time constant τ_N in our model can be set to an infinite value.

2.2 Necessary Condition for the Pseudo-Linear Analysis

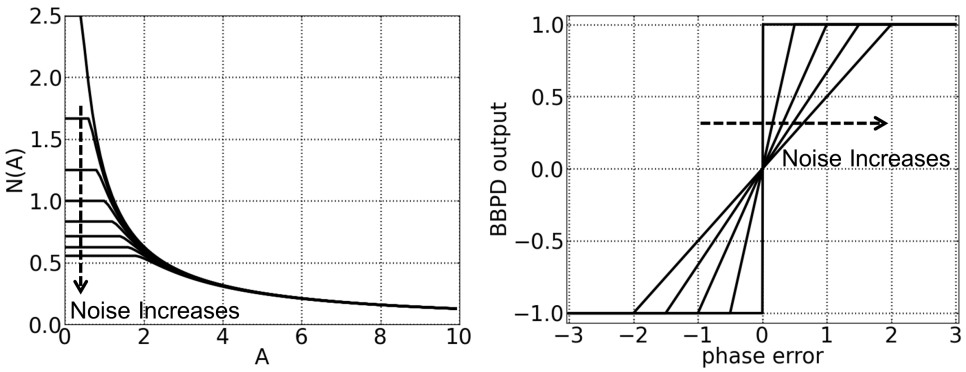
A bang-bang controlled system can be modeled as an equivalent linear system when sufficient noise is present in the system. This section derives the minimum noise necessary for our pseudo-linear analysis to be valid.

In a strict sense, dithering implies that the system is unstable and occurs when the feedback loop satisfies the following conditions: (1) large enough gain and (2) long enough delay. For instance, if we model the bang-bang controlled loop in Fig. 2.1(b) as a feedback loop as shown in Fig. 2.2, consisting of a linearized gain $N(A)$ that corresponds to the nonlinear BBPD and $G(s)$ that models the rest of the system, the closed-loop transfer function $H(s)$ of the system from input to output can be written as:

$$H(s) = \frac{N(A) \cdot G(s)}{1 + N(A) \cdot G(s)}. \tag{2.3}$$

With $G(s)$ including the loop delay component $e^{-sT_{ref}(N_d+1)}$, as in Eq. (2.2), this system may become unstable and exhibit limit-cycle behavior when the denominator $1 + N(A) \cdot G(s)$ is equal to zero [11]. In other words, dithering can occur when there exist an amplitude A and a frequency $s = j\omega$ that satisfy

$$G(s) = -\frac{1}{N(A)} \tag{2.4}$$



(a) (b)

Figure 2.3: (a) Describing function $N(A)$ vs. A as a function of the input noise, and (b) effective input-to-output transfer of a BBPD as a function of noise.

We denoted the linearized gain of the BBPD $N(A)$ as a function of the input amplitude A. One way to derive the approximate linear gain of a nonlinear element as a function of the input signal amplitude A is the describing function analysis [11]. Assuming that the nonlinear BBPD receives a sinusoidal input with amplitude A and the frequency ω, the linearized gain is derived as the ratio between this input amplitude A and the amplitude of the corresponding frequency component in the output signal. One can predict the existence of limit cycles based on this describing function analysis. If there exist an amplitude A and a frequency s that satisfy (2.4), then the system is likely to have a limit-cycle behavior with the corresponding amplitude and frequency. In our case, the BBPD is memoryless and hence its linearized gain $N(A)$ is a function of amplitude A only.

When there is no noise present at the input of the BBPD, the linearized gain

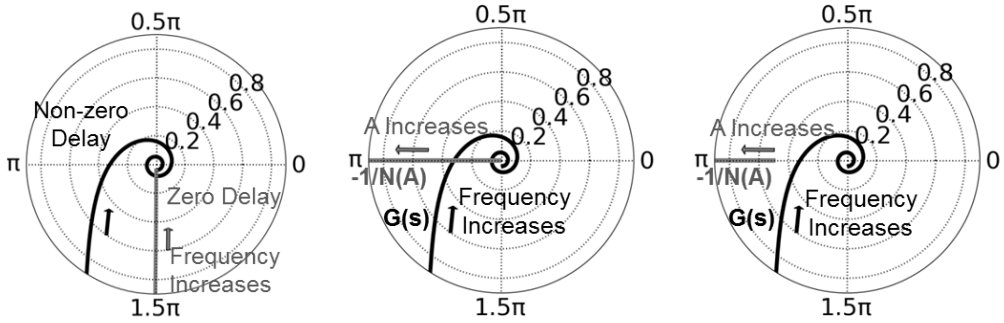
$N(A)$ can be derived as in [11]:

$$\begin{aligned} N(A) &= \frac{\frac{4}{\pi}\int_0^{\pi/2} 1 \cdot sin(\omega t) d(\omega t)}{A} \\ &= \frac{4}{\pi A} \end{aligned} \tag{2.5}$$

The linearized gain $N(A)$ starts from $+\infty$ and decreases toward 0 as the input amplitude A increases, as shown in Fig. 2.3(a). The expression $-1/N(A)$ will then change from 0 to $-\infty$ as A changes from 0 to $+\infty$.

The existence of a solution to Eq. (2.4) can be visualized by plotting both sides of the equation on a Nyquist plot, as shown in Fig. 2.4. This plots the trajectories of $G(s)$ and $-1/N(A)$ on a complex plane with polar coordinates while sweeping the frequency $s = j\omega$ and the amplitude A, respectively. As Fig. 2.4(a) shows, with a non-zero loop delay, the $G(s)$ curve has a shape that intersects with the negative real axis. In this case, there exists a value of A that satisfies Eq. (2.4) because $-1/N(A)$ spans the whole range of negative real values (Fig. 2.4(b)). In other words, the describing function analysis confirms that a bang-bang controlled loop can exhibit dithering behavior when the loop has a non-zero delay.

In contrast, when noise is present at the BBPD input, the noise effectively smoothes out the binary characteristic of the BBPD transfer function and lowers the linearized gain $N(A)$, as plotted in Fig. 2.3(a). To illustrate this simply, let us assume that the input noise is uniformly distributed between $-\Delta\phi_L$ and $\Delta\phi_L$. The effective input-to-output transfer function of the BBPD, calculated as the average output in the presence of noise from each given input, changes to the one shown in Fig. 2.3(b), which can be expressed as a convolution between the original BBPD transfer function and the noise PDF [12]. Intuitively speaking, for inputs smaller



(a) (b) (c)

Figure 2.4: Nyquist plot of bang-bang CDR: (a) $G(s)$ with and without loop delay, (b) $G(s)$ with loop delay and $-1/N(a)$ without noise (intersecting) and (c) $G(s)$ with loop delay and $-1/N(A)$ with noise (not intersecting).

than the noise magnitude $\Delta\phi_L$, the probabilities of +1 and -1 outputs gradually change with the input amplitude, implying a linearized response. With this newly-formed linear region in the BBPD transfer function, the maximum linearized gain $N(A)$ is at most $1/\Delta\phi_L$, even for the smallest A. It then follows that $-1/N(A)$ will span a reduced range from $-\Delta\phi_L$ to $-\infty$.

The above analysis illustrates that sufficient noise in the system can reduce the span of $-1/N(A)$, as illustrated in Fig. 2.4(c), causing the system to not have a solution that satisfies Eq. (2.4) and, hence, to exhibit no dithering. In other words, the bang-bang controlled system is *sufficiently linearized* by the noise.

Note that a bang-bang controlled loop with a longer loop delay takes more noise to linearize. With the longer delay, the $G(s)$ curve intersects with the negative real axis at the lower value (at the higher absolute value) and the larger noise ($\Delta\phi_L$) is required to avoid its crossing with $-1/N(A)$. Without sufficient noise, the output phase will dither with the larger amplitude because the two curves intersect at the point that corresponds to the larger A. We will see later that the excessive loop

delay in a bang-bang controlled timing loop has many adverse effects on the overall performance metrics. It is desirable to keep the loop delay to the minimum possible via careful circuit and architecture designs.

From this analysis it follows that to suppress dithering in a bang-bang controlled loop, the noise in the system must be large enough so that the maximum effective BBPD gain K_{PD} becomes lower than a certain critical threshold K_{PD}^{*}. In the previous analysis, K_{PD} corresponds to the asymptotic value of $N(A)$ as A approaches 0. The threshold K_{PD}^{*} is determined by the linear part of the feedback system $G(s)$:

$$K_{PD}^{*} = -1/Re\{G(j\omega^{*})\} \tag{2.6}$$

where ω^{*} is the smallest ω that satisfies $\mathcal{I}m\{G(j\omega)\} = 0$. It is possible to derive the expression for K_{PD}^{*} in terms of the loop parameters using Eq. (2.2), and we can finally arrive at the necessary condition for the linearized system analysis:

$$K_{PD} < K_{PD}^{*} = \frac{\pi}{2}\frac{1}{\phi_{bb}(N_d + 1)} \tag{2.7}$$

The detailed derivation of the critical gain value K_{PD}^{*} is given in Section 2.3. This criterion confirms the previous results; namely that it takes the larger noise to linearize a bang-bang controlled loop when it has a larger gain (ϕ_{bb}) or a longer delay (N_d) [5]. It should be noted that Eq. (2.7) is the condition to avoid periodic dithering. The system may still exhibit non-periodic dithering even when K_{PD} is smaller than K_{PD}^{*}.

2.3 Derivation of Necessity Condition for the Pseudo-Linear Analysis

This section gives the validity of our pseudo-linear analysis within the suggested K_{PD} range explained in the previous section. By substituting $s = j\omega$ and using the Euler's identity, (2.2) becomes

$$\begin{aligned} G(j\omega) = &- \frac{\phi_{bb}}{\tau_N} \frac{1 + \tau_N T_{ref} j\omega}{T_{ref}^2 \omega^2} \{\cos(\omega T_{ref}(N_d + 1)) \\ &- j \sin(\omega T_{ref}(N_d + 1))\}. \end{aligned} \tag{2.8}$$

Let us define the ratio between the time constant of loop filter and the loop delay κ as

$$\kappa = \frac{\tau}{t_{d,eff}} = \frac{\tau}{T_{ref}} / \frac{t_d + T_{ref}}{T_{ref}} = \tau_N / (N_d + 1). \tag{2.9}$$

Then the smallest ω that satisfies $Im\{G(j\omega)\} = 0$, ω^*, is

$$\begin{aligned} Im(G(j\omega^*)) = &\frac{-\phi_{bb}}{\tau_N T_{ref}^2 \omega^{*2}} \{\tau_N T_{ref} \omega^* \cos(\omega^* T_{ref}(N_d + 1)) \\ &- \sin(\omega^* T_{ref}(N_d + 1))\} = 0 \\ &\tau_N T_{ref} \omega^* = \tan(\omega^* T_{ref}(N_d + 1)) \end{aligned} \tag{2.10}$$

Inserting Eq. (2.9) into Eq. (2.10), we obtain

$$\kappa \omega^* T_{ref}(N_d + 1) = \tan(\omega^* T_{ref}(N_d + 1)). \tag{2.11}$$

Assuming $\kappa >> 1$, which is true in most systems,

$$\begin{aligned} \omega^* T_{ref}(N_d + 1) &\approx \frac{\pi}{2} \\ \omega^* &= \frac{\pi}{2} \frac{1}{T_{ref}(N_d + 1)} \end{aligned} \tag{2.12}$$

Finally, by putting Eq. (2.12) into Eq. (2.6), we obtain

$$K_{PD}^{*} = \frac{1}{Re\{H(e^{j\omega^{*}T_{ref}})\}} = \frac{\pi}{2}\frac{1}{\phi_{bb}(N_d+1)}. \tag{2.13}$$

2.4 A Linearized Model of the Bang-Bang Phase Detector

There have been many efforts to model the bang-bang phase detectors (BBPD) or equivalent one-bit quantizers as linear elements. These efforts were not limited to the context of PLLs and CDRs [6, 8, 12–14], but also included data converters [15]. The representative examples of such prior work are summarized in Tab 2.4. Some of the linear models do not include additive noise sources for modeling quantization noise [8, 12] or do not model the influence of the input noise profile on the effective gain value [13]. It is noteworthy that recent studies have analyzed the effects of quantization noise in so-called, all-digital PLLs, but they may not be easily extended to CDRs because they either assume low noise conditions [16, 17] or neglect the influence of the transition density [6, 14]. In addition, the methods in prior work for deriving effective linear gain were either limited to a specific circuit implementation [8], or based on Markov-chain analysis which does not give a closed-form equation that can be applied to general problems [6, 14, 18]. This section presents a generally applicable linear model for a BBPD that includes all the effects of loop dynamics such as loop delay, quantization noise and transition density.

Let's assume that the phase error (i.e., the phase difference between the input data stream and the recovered clock) consists of two terms. One is the deterministic phase error term $\phi_{e,X}(t)$ (e.g., deterministic ISI or sinusoidal jitter) and the other

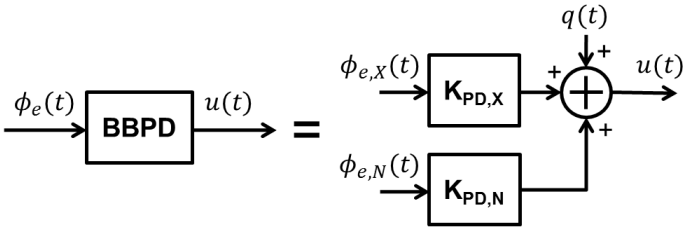


Figure 2.5: A general model of BBPD.

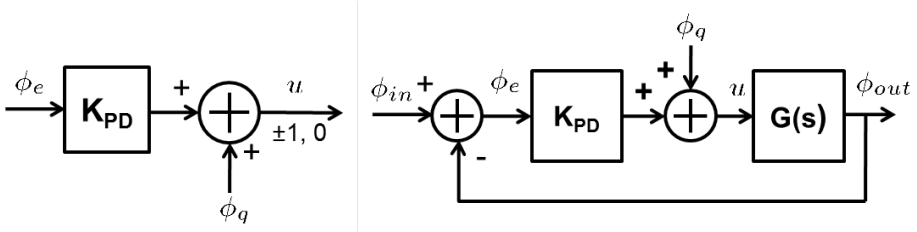
is a zero-mean random error term $\phi_{e,N}(t)$. In expressions:

$$\phi_e(t) = \phi_{e,X}(t) + \phi_{e,N}(t) \tag{2.14}$$

The deterministic term $\phi_{e,X}(t)$ is zero when analyzing the jitter transfer or jitter generation characteristics, assuming a fixed input phase. However, $\phi_{e,X}(t)$ may take a sinusoidal waveform when analyzing the jitter tolerance.

The key feature of our pseudo-linear analysis is that it assumes different gains for components $\phi_{e,X}(t)$ and $\phi_{e,N}(t)$. Such a treatment was originally suggested by [15] for the purpose of analyzing the SNDR of delta-sigma ADCs. Fig. 2.5 illustrates our linearized model of a BBPD. $K_{PD,X}$ and $K_{PD,N}$ are linearized gains for the input components $\phi_{e,X}(t)$ and $\phi_{e,N}(t)$, respectively, and an independent noise $q(t)$ is added to the output to model the quantization effects of the BBPD. When sufficient noise is present in the system and the linearized analysis is valid, the random component $\phi_{e,N}(t)$ is mainly the result of the input phase noise and is uncorrelated with the deterministic term $\phi_{e,X}(t)$ [14].

The following discussion describes how to decompose the input of the BBPD $\phi_e(t)$ into the two components $\phi_{e,X}(t)$ and $\phi_{e,N}(t)$. Let us denote the nonlinear



(a) (b)

Figure 2.6: A model of (a) bang-bang PD and (b) CDR for the purpose of jitter transfer and jitter generation analyses.

mapping of $\phi_e(t)$ into the BBPD output $u(t)$ as $N(\phi_e(t))$:

$$u(t) = N(\phi_e(t)) = N(\phi_{e,X}(t) + \phi_{e,N}(t)). \tag{2.15}$$

The instantaneous difference $\phi_q(t)$ between $u(t)$ and the output of linearized model $K_{PD,X}\phi_{e,X}(t) + K_{PD,N}\phi_{e,N}(t)$ can be considered as the quantization noise. For the closest approximation of the BBPD's behavior, the linearized gains $K_{PD,X}$ and $K_{PD,N}$ should be set to minimize the power of this quantization noise [15]. The power of the quantization noise is then expressed as

$$\sigma_q^2 = E\{[u(t) - K_{PD,X}\phi_{e,X}(t) - K_{PD,N}\phi_{e,N}(t)]^2\}, \tag{2.16}$$

and is minimized when

$$\begin{aligned} \frac{\partial \sigma_q^2}{\partial K_{PD,X}} &= 2K_{PD,X}E\{\phi_{e,X}^2(t)\} - 2E\{\phi_{e,X}(t)u(t)\} = 0 \\ \frac{\partial \sigma_q^2}{\partial K_{PD,N}} &= 2K_{PD,N}E\{\phi_{e,N}^2(t)\} - 2E\{\phi_{e,N}(t)u(t)\} = 0 \end{aligned} \tag{2.17}$$

are satisfied. The equations then respectively yield:

$$\begin{aligned} K_{PD,X} &= \frac{E\{\phi_{e,X}(t)u(t)\}}{E\{\phi_{e,X}^2(t)\}} \\ K_{PD,N} &= \frac{E\{\phi_{e,N}(t)u(t)\}}{E\{\phi_{e,N}^2(t)\}}. \end{aligned} \tag{2.18}$$

It is noteworthy that when Eq. (2.18) is satisfied, the random components of the input $\phi_{e,N}(t)$ and the quantization noise $q(t)$ become uncorrelated, because the expression

$$\begin{aligned} E\{\phi_{e,N}(t)q(t)\} =& E\{\phi_{e,N}(t)u(t)\} - K_{PD,X}\{\phi_{e,N}(t)\phi_{e,X}(t)\} \\ & - K_{PD,N}\{\phi_{e,N}^2(t)\} \end{aligned} \tag{2.19}$$

is 0, given that $\phi_{e,N}(t)$ is independent of $\phi_{e,X}(t)$ and $E\{\phi_{e,N}(t)u(t)\} = K_{PD,N}\{\phi_{e,N}^2(t)\}$ according to Eq. (2.17). This property will be leveraged in the later analyses in this chapter.

2.5 Linearized Gain of a Bang-Bang Phase Detector for Jitter Transfer and Jitter Generation Analyses

This section discusses the derivation of the linearized gain for the analyses of the jitter transfer (JTRAN) and jitter generation (JG) characteristics of a bang-bang controlled CDR, based on the mentioned linear model.

In the case of JTRAN and JG analyses, the input phase is assumed to be constant, implying that the deterministic component $\phi_{e,X}(t)$ is a constant value, and it can be considered as 0 without a loss of generality. Fig. 2.6 shows the analytical model of the BBPD and the overall CDR. The effective linearized gain K_{PD} for the random input $\phi_{e,N}(t)$, which is equal to the phase error input $\phi_e(t)$ in this case, can

Table 2.1: Comparison of bang-bang controlled PLL/CDR analyses reported in literature

Ref.	Main Contributions	Limitations
Walker, 2003 [13]	Analysis of stability, tracking performance and jitter generation property of a bang-bang CDR	The linearized PD gain is fixed at unity with only the qualitative explanation on the effects of random noise
Choi, Lee, 2003 [4, 12]	Derivation of the effective linearized gain of a BBPD in the presence of random noise	Neglects the quantization noise generated by the BBPD and the loop dynamics
Dalt, 2006 [6]	Derivation of the effective linearized gain of a BBPD in consideration of the loop dynamical behavior	Neglects loop delay effects; based on Markov analysis which is basically an inductive method
Chun, 2008 [18]	Extension of [6] that includes the loop delay effects	Results are derived on a case-by-case basis
Dalt, 2008 [14]	JTRAN and JG analysis based on the linearized model	Neglects loop delay effects; quantization noise is derived in an inductive method
Lee, 2004 [8]	JTOL analysis based on nonlinear behavior (slewing and dithering)	Neglects the effects of random noise and loop delay. K_{PD} estimation is based on a specific implementation.

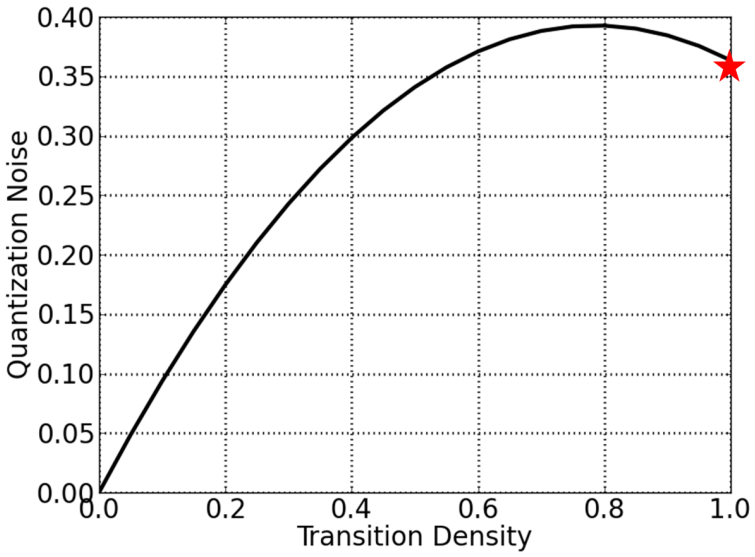


Figure 2.7: Comparison of predicted quantization error power based on our model (solid line) and the model in [14] (star)

be found by minimizing the power of the quantization error:

$$E[\phi_q^2] = E[(u(\phi_e) - K_{PD}\phi_e)^2] \tag{2.20}$$

yielding

$$K_{PD} = \frac{E[u(\phi_e)\phi_e]}{E[\phi_e^2]}. \tag{2.21}$$

Assuming that the phase error input ϕ_e takes a Gaussian distribution, which is a reasonable assumption based on the central limit theorem and given that the recovered phase is the result of multiple integrations, the effective linearized gain of

the phase detector can be computed as

$$\begin{aligned} K_{PD} &= \frac{\int_{-\infty}^{\infty} u(\phi_e)\phi_e f_e(\phi_e) d\phi_e}{E[\phi_e^2]} \\ &= \frac{2\alpha_T \int_0^{\infty} \phi_e f_e(\phi_e) d\phi_e}{\sigma_e^2} \\ &= \sqrt{\frac{2}{\pi}} \frac{\alpha_T}{\sigma_e} \end{aligned} \tag{2.22}$$

where $f_e(\phi_e)$ is the probability density function (PDF) of the phase error ϕ_e and α_T is the transition density of the input data stream which is same with the power of $u(\phi_e)$ ranging from 0 to 1. Eq. (2.22) implies that the effective gain of a bang-bang phase detector is inversely proportional to the standard deviation of the phase error and proportional to the transition density, which is consistent with the earlier findings in [6, 12].

The power of the quantization error can be computed based on the binary characteristic of the PD's output. That is, since the phase detector output $u(t)$ can take +1, -1, or 0, its power is simply equal to the transition density α_T;

$$\begin{aligned} E[u^2] &= E[(K_{PD}\phi_e + \phi_q)^2] \\ &= K_{PD}^2 E[\phi_e^2] + E[\phi_q^2] = \alpha_T. \end{aligned} \tag{2.23}$$

Then, the variance of quantization error σ_q^2 can be calculated as

$$\sigma_q^2 = \alpha_T - K_{PD}^2 \sigma_e^2 = \alpha_T - \frac{2}{\pi}\alpha_T^2 \tag{2.24}$$

where σ_e^2 is the variance of the phase error ϕ_e.

[14] asserted that the standard deviation of the input-referred quantization noise is approximately equal to three-fourths of the standard deviation of input jitter $\sigma_{\phi_{in}}$

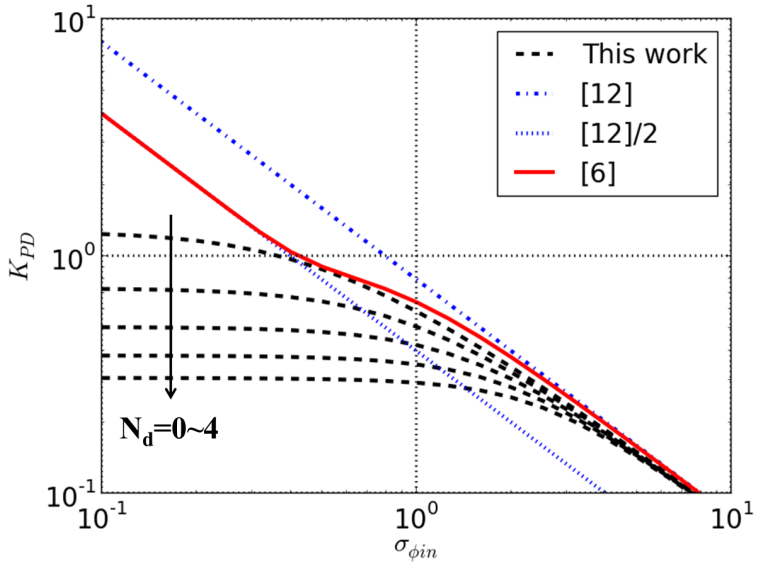


Figure 2.8: Comparison of the effective linear gains of a BBPD described by different models in the literature (normalized with respect to the bang-bang phase step ϕ_{bb}).

and the linearized gain of the BBPD takes an expression of

$$K_{PD} \approx \frac{1}{\sqrt{2\pi}\sigma_{\phi_{in}}}[1 + e^{-\frac{1}{2}(\frac{\phi_{bb}}{\sigma_{\phi_{in}}})^2}] \tag{2.25}$$

when the transition density is 1.0. It follows that the output-referred quantization error for $\alpha_T = 1.0$ can be expressed as

$$\begin{aligned} \sigma_q^2 &= (\frac{3}{4}\sigma_{\phi_{in}})^2 K_{PD}^2 \\ &\approx \frac{9}{32\pi}[1 + e^{-\frac{1}{2}(\frac{\phi_{bb}}{\sigma_{\phi_{in}}})^2}]^2. \end{aligned} \tag{2.26}$$

When $\sigma_{\phi_{in}} \gg \phi_{bb}$, its approximate value of σ_q^2 becomes $9/8\pi \approx 0.358$. It is similar with the result based on (2.24), $1 - 2/\pi \approx 0.363$. As will be discussed in a later section, the simulation results for jitter generation characteristics confirm that our model in Eq. (2.24) is indeed accurate even with arbitrary transition density.

On the other hand, the variance of phase error σ_e^2 can be calculated from the loop dynamical equations:

$$\begin{aligned} S_{\phi_e}(\omega) =& S_{\phi_{in}}(\omega)\frac{1}{|1+K_{PD}G(\omega)|^2} \\ &+ S_{\phi_{VCO,N}}(\omega)\frac{1}{|1+K_{PD}G(\omega)|^2} \\ &+ S_{\phi_q}(\omega)|\frac{G(\omega)}{1+K_{PD}G(\omega)}|^2 \end{aligned} \tag{2.27}$$

where S_{ϕ_e}, $S_{\phi_{in}}$, $S_{\phi_{VCO,N}}$ and S_{ϕ_q} are the power spectral densities of the phase error, input random jitter, VCO's phase noise and BBPD's quantization error, respectively. Using Eq. (2.25) and given that the total noise power is equal to the PSD integrated across the entire frequency range, it follows that

$$\begin{aligned} \sigma_e^2 =& \int_{-0.5}^{0.5} \frac{S_{\phi_{in}}(\omega) + S_{\phi_{VCO,N}}(\omega)}{|1+K_{PD}G(\omega)|^2} d\omega \\ &+ \int_{-0.5}^{0.5} (\alpha_T - \frac{2}{\pi}\alpha_T^2)|\frac{G(\omega)}{1+K_{PD}G(\omega)}|^2 d\omega. \end{aligned} \tag{2.28}$$

Eqs. (2.22) and (2.28) provide a basis for computing the effective linearized gain K_{PD} and the phase error power σ_e^2 when the input phase noise PSD $S_{\phi_{in}}(\omega)$, the VCO phase noise PSD $S_{\phi_{VCO,N}}(\omega)$ and the transition density α_T are given. With the two variables and two equations, one can simultaneously solve them to find the solutions. For example, the solution can be found by finding the intersecting point of two equations graphically.

Fig. 2.8 compares the numerical values of the BBPD's linearized gain between the presented analysis and those in the literature [4, 6, 12, 14]. For instance, one alternate way of estimating the linearized gain is by computing the convolution between the BBPD's ideal input-to-output transfer function and the jitter PDF at

the PD's input [4, 12]:

$$K_{PD} = \left.\frac{\partial E[u(t)]}{\partial \Delta\phi_{in}}\right|_{\phi_{in}=0} = 2\alpha_T f(0) \tag{2.29}$$

where $f(\phi_{in})$ denotes the jitter PDF. In case the input jitter takes a Gaussian distribution with a standard deviation of $\sigma_{\phi_{in}}$, the effective linearized gain can be expressed as:

$$K_{PD} = 2\alpha_T \left.\left(\frac{1}{\sqrt{2\pi}\sigma_{\phi_{in}}} exp\left(-\frac{x^2}{2\sigma_{\phi_{in}}^2}\right)\right)\right|_{x=0} = \sqrt{\frac{2}{\pi}}\frac{\alpha_T}{\sigma_{\phi_{in}}} \tag{2.30}$$

Fig. 2.8 shows that the gain values predicted by [12] agree with our values only for large enough input jitter conditions. It is because the derivation in [12] ignores the fact that the BBPD is within a feedback loop and therefore the input phase can move based on the BBPD's output. In other words, computing the convolution itself relies on the assumption that the input phase value and the input jitter are independent of each other; i.e. the input phase remains at a fixed value while the BBPD gives +1 or -1 outputs. This is true only when the feedback loop has low enough bandwidth, which corresponds to the case with large input jitter and hence low effective PD gain.

On the other hand, our predicted gain values agree better with those according to Eq. (2.25), which are derived based on a Markov-chain analysis that does take the feedback dynamics into account [6]. However, the discrepancies still exist for low jitter conditions, stemming from the different treatments of the quantization noise observed at the BBPD's output. While the BBPD model in [6] directly provides the discrete outputs of -1, 0, and +1, our linearized BBPD model expresses this discrete nature instead with an additive quantization noise of which power level is

derived as in Eq. (2.28). The presence of this quantization noise is the reason why our effective gain values do not keep increasing as the jitter decreases. Nonetheless, this discrepancy is irrelevant since at these low jitter conditions, the feedback loop is not sufficiently linearized and its behavior cannot be described accurately by the presented pseudo-linear analysis anyways.

It is noteworthy that the proposed expression for the effective linearized PD gain in Eq. (2.18) with two separate loops is valid over a wider range than the previously used expression in Eq. (2.29). First, Eq. (2.18) reduces to Eq. (2.29) for infinitesimally small sinusoidal perturbations, for which the detailed derivation is given in Appendix B. On the other hand, the proposed PD gain expression yields the more accurate predictions as the sinusoidal perturbation takes a finite, larger magnitude, as in the case of JTOL analysis. To illustrate this, Fig. 2.9 compares the pseudo transfer functions of a bangbang PLL measured using various amplitudes of the input sinusoidal jitter. The pseudo transfer gain at each frequency is measured by simulating the ratio between the input and output sinusoidal jitter amplitudes. For small input amplitudes, the transfer functions predicted by both the expressions Eq. (2.18) and Eq. (2.29) agree well with the simulated results. However, as the amplitude increases, the proposed PD gain expression Eq. (2.18) yields the better predictions.

In other words, the presented analysis derives the effective PD gain as the one that minimizes the quantization error considering the whole input distribution and therefore provides the better predictions. Especially, our derivation can also be applied to predicting the JTOL characteristics of the CDR without separately considering the case of slew-limiting as in [8,13] even when a large-amplitude sinusoidal

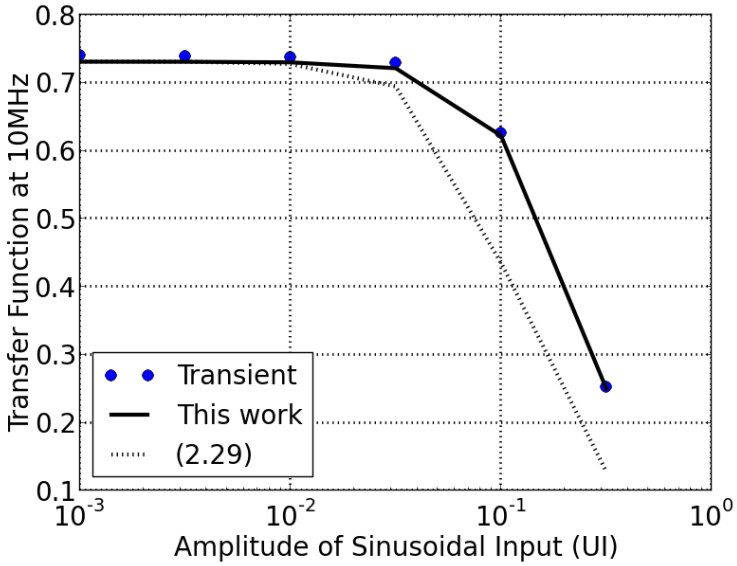


Figure 2.9: Comparison of predicted transfer functions at 10MHz with various amplitudes of sinusoidal input using transient simulation, proposed theory, and (2.29). ϕ_{bb} is 0.005UI, and α_T is 1.0.

jitter is applied to the BBPD's input. The application of the derived effective PD gain to the JTOL analysis will be described in later sections.

2.6 Jitter Transfer and Jitter Generation Analyses

This section applies the previously derived linearized gain of BBPD to the analyses of the CDR's jitter characteristics. The accuracy of the estimation is validated by comparing with the simulation results with various parameters including input noise and loop delay.

The power spectral density of the bang-bang CDR/PLL output phase noise can be derived once the linearized gain K_{PD} and the quantization noise power σ_q^2 are

computed for the pseudo-linear model in Fig. 2.6(b):

$$\begin{aligned} S_{\phi_{out}}(\omega) =& S_{\phi_{in}}(\omega)|\frac{K_{PD}G(\omega)}{1+K_{PD}G(\omega)}|^2 \\ &+ S_{\phi_{VCO,N}}(\omega)\frac{1}{|1+K_{PD}G(\omega)|^2} \\ &+ S_{\phi_q}(\omega)|\frac{G(\omega)}{1+K_{PD}G(\omega)}|^2 \end{aligned} \tag{2.31}$$

where the first term on the right-hand side in Eq. (2.31) corresponds to the input phase noise transferred to the output, while the rest corresponds to the phase noise generated by the internal circuits. Especially, the last term is the contribution of the BBPD's quantization noise, which tends to be ignored by the majority of the prior work [4, 8, 12]. The main advantage of Eq. (2.31) is that it can help one to choose an optimal set of loop parameters that minimize the output phase noise, given the noise conditions at the input and the VCO.

To validate our pseudo-linear model, we compare its predicted results with those of behavioral simulations. Two kinds of behavioral simulation are performed for jitter transfer analysis: the stochastic AC (SAC) analysis outlined in [23] and the numerical model based on Fig. 2.1. The plurality of the results improves the fidelity of our validation.

Fig. 2.10 (a) plots the jitter transfer functions of CDRs for various noise conditions. Gaussian random jitter (RJ) with various standard deviation values (10mUI, 20mUI, 40mUI and 80mUI) is applied to the input while a transition density of 50%, a loop delay of one update cycle ($N_d = 1$), and a τ_N of 1000 are assumed. Default values are $\phi_{bb} = 20mUI$, $\tau_N = 1000$, $\sigma_{\phi_{in}} = 50mUI$, $\alpha_T = 0.5$, and $N_d = 1UI$. Note that the predicted jitter transfer functions based on our theory match well with the simulation results from the stochastic AC analysis and the time-domain simulations.

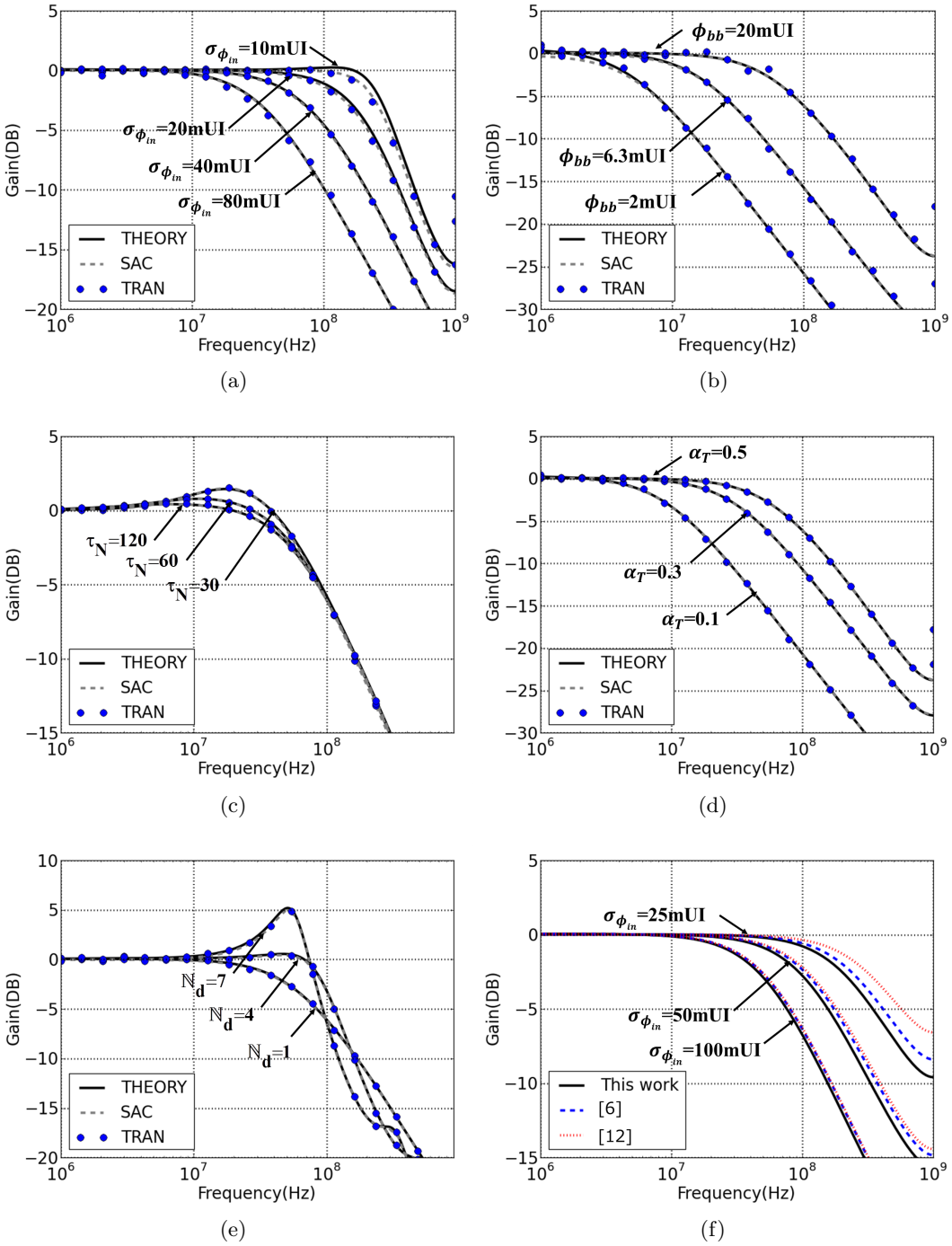
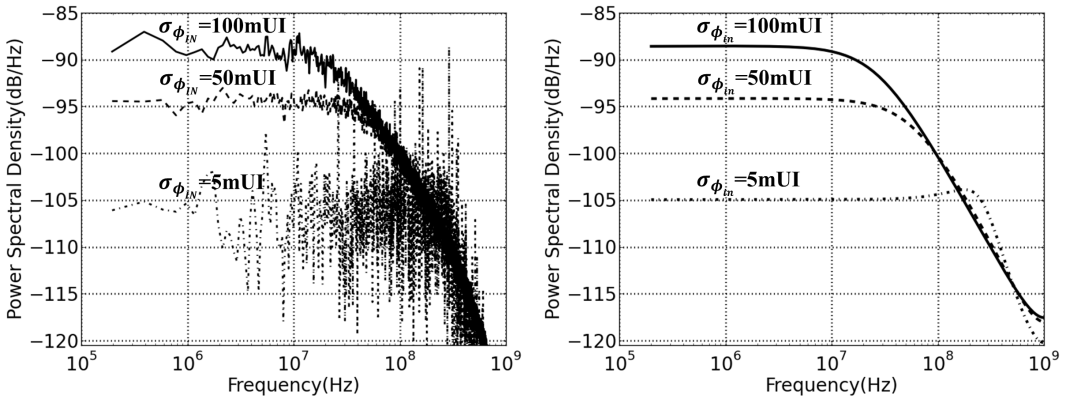


Figure 2.10: Comparison of the jitter transfer functions with various (a) $\sigma_{\phi_{in}}$, (b) ϕ_{bb}, (c) τ_N, (d) α_T, and (e) N_d. (f) is the comparison with [6] when $\alpha_T = 1.0$.

An exception is the case with 10mUI random jitter, in which case the CDR loop is not fully linearized. For comparisons, the predicted jitter transfer functions by other theory [6, 12] are plotted in Fig. 2.10(f). As the theory in [6] is for the PLLs, the comparison is done with 100% of transition density. As expected [12] shows big difference comparing with other theories as it does not include the loop dynamics. The proposed theory shows good agreements with the theory in [6]. Its predicted bandwidth is slightly narrower but the difference is less than 5%. One may find a reason of the difference from the fact that Eq. (2.25) slightly overestimates the linearized gain as it limited the number of states for the simplicity [6].

Fig. 2.10(b), (c), (d) and (e) illustrate the effects of various parameters such as the bang-bang phase step ϕ_{bb}, the normalized proportional-to-integral gain ratio τ_N, the transition density of input data pattern α_T and the loop delay N_d on the jitter transfer function. When the bang-bang phase step or input data transition density is big, the linearized gain of BBPD and the loop bandwidth increases. When τ_N decreases, the zero frequency ω_z shifts toward the higher frequency, reducing the phase margin and possibly resulting a peaking in the transfer function. The loop delay can cause similar peaking as it adds a phase shift to the open-loop transfer function.

The effective -3-dB bandwidth of a BB-PLL (ω_{-3dB}) can be calculated once the effective linearized gain for the BBPD is derived for the given noise/jitter condition. Since the other parts of the PLL are linear systems, the bandwidth computation is the same with that of a linear PLL. That is, the -3-dB bandwidth is the frequency when the closed-loop transfer function $H(s)$ crosses the point -3dB below the DC



(a) (b)

Figure 2.11: Comparison of the output jitter PSDs (a) in time-accurate behavioral simulation and (b) the proposed linear model. Simulation parameters are same with those in Fig. 2.10.

gain value (assumed 1).

$$\left| \frac{K_{PD}G(j\omega_{-3dB})}{1 + K_{PD}G(j\omega_{-3dB})} \right| = \frac{1}{\sqrt{2}}. \tag{2.32}$$

One complication in deriving the closed-form expression for ω_{-3dB} is that the continous-time model $G(s)$ in Eq. (2.2) bears the term $e^{-sT_{ref}(N_d+1)}$ which models the effective loop latency. Since the phase shift caused by this loop latency can result in potential instability for linear PLLs as well as limit cycles for bang-bang PLLs, it must be minimized either by reducing the latency or the loop gain. In fact, if the phase shift at the bandwidth frequency $\omega_{-3dB}T_{ref}(N_d + 1)$ is sufficiently small, the exponential term can be approximated as 1, yielding a simple closed-form expression for ω_{-3dB}:

$$\omega_{-3dB} = K_{PD}\phi_{bb}T_{ref} \tag{2.33}$$

This equation predicts the -3-dB bandwidth within 10% of error as long as the phase shift due to the loop latency $\omega_{3dB}T_{ref}(N_d + 1)$ is less than $\pi/50$ radians.

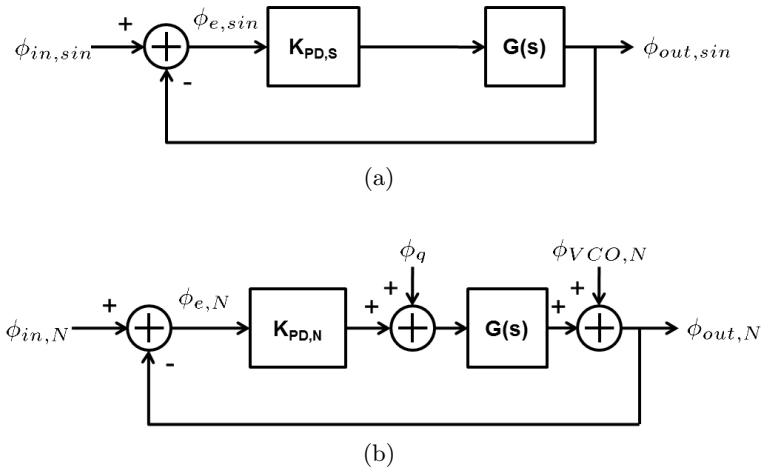


Figure 2.12: A model of bang-bang CDR for the purpose of jitter tolerance (JTOL) analysis.

As with the jitter generation characteristics of the CDRs, the predicted power spectral densities (PSD) of the output jitter are compared against the results from time-accurate behavioral simulations [19]. Fig. 2.11(a) and (b) plot the simulated and predicted output jitter PSDs for various noise conditions for the transition density of 50%. Again, the theory and simulation results are in good agreement with the input random jitter's standard deviation values of 5 mUI_{rms}, 50 mUI_{rms} and 100 mUI_{rms} event with non-100% transition density. Note that the simulated PSD for the 5-mUI_{rms} input jitter shows spurs in multiple positions due to dithering (i.e., limit cycles) that cannot be modeled by any of the linearized models.

2.7 Linearized Gains of a Bang-bang Phase Detector for Jitter Tolerance Analysis

Along with the jitter transfer and jitter generation characteristics, the jitter tolerance (JTOL) is an important metric that describes the maximum tolerable amplitude of

the sinusoidal jitter which generates less than the target BER.

The work in [8] gave the asymptotes of the JTOL curves based on slewing, but it revealed a few limitations. First, it did not model the effects of random noise on the tracking behavior of the loop. Our proposed analysis suggests that the random noise can cause shift in the JTOL curve both in horizontal and vertical directions. Second, [8] did not model the effect of loop delays. Without a loop delay, the under-peaking found in some of the JTOL curves cannot be explained [20]

This section derives the parameters for our linearized BBPD model analysis, including the effective linearized gains and quantization noise. Once the parameters are derived, next subsection describes the estimation of JTOL curve including the high frequency JTOL. We find that there is a good agreement between the predicted JTOL characteristics and the simulated ones.

As mentioned, in the case of JTOL analysis, the BBPD receives a non-zero, time-varying deterministic input $\phi_{e,X}(t)$. Because the jitter tolerance measures the largest sinusoidal jitter that the CDR can tolerate with the specified BER target, it is likely that $\phi_{e,X}(t)$ is a sinusoidal signal. This means that we will be fully utilizing the two-input linearized BBPD model in Fig. 2.5 with two different linearized gains $K_{PD,X}$ and $K_{PD,N}$. Each linearized gain is determined based on Eq. (2.18), which makes the two inputs $\phi_{e,X}(t)$ and $\phi_{e,N}(t)$ uncorrelated with each other.

With proper selection of the two linearized gains that make the two inputs uncorrelated, we can analyze the CDR as two separate feedback loops: one with the deterministic input $\phi_{in,sin}$ and the other with the random input $\phi_{in,N}$. This is illustrated in Fig. 2.12. Because the deterministic input is a sinusoidal one in this case, we use the suffix 'S' for the corresponding linearized gain ($K_{PD,S}$). Based on

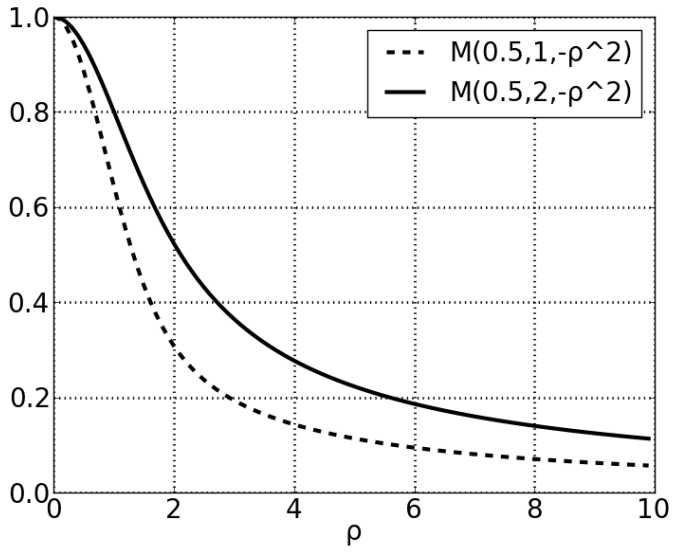


Figure 2.13: The confluent hypergeometric functions

superposition principle, the overall output of the CDR is equal to the sum of the two loops' outputs.

According to Eq. (2.18), the linearized gains that minimize the quantization error are

$$\begin{aligned} K_{PD,S} =& \frac{E\{\phi_{e,sin}(t)u(t)\}}{E\{\phi_{e,sin}^2\}} \\ =& \frac{1}{\sigma_{e,sin}^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\phi_{e,sin}N(\phi_{e,sin}+\phi_{e,N}) \\ & \cdot f_N(\phi_{e,N})f_{sin}(\phi_{e,sin})d\phi_{e,sin}d\phi_{e,N} \end{aligned} \tag{2.34}$$

$$\begin{aligned} K_{PD,N} =& \frac{E\{\phi_{e,N}(t)u(t)\}}{E\{\phi_{e,N}^2\}} \\ =& \frac{1}{\sigma_{e,N}^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\phi_{e,N}N(\phi_{e,sin}+\phi_{e,N}) \\ & \cdot f_N(\phi_{e,N})f_{sin}(\phi_{e,sin})d\phi_{e,sin}d\phi_{e,N} \end{aligned} \tag{2.35}$$

where $\phi_{e,sin}$ and $\phi_{e,N}$ are the phase errors in the sinusoidal input tracking loop

and the random input tracking loop, respectively. $\sigma^2_{e,sin}$ and $\sigma^2_{e,N}$ denote their variances, and $f_{sin}(\phi_{e,sin})$ and $f_N(\phi_{e,N})$ are their probability density functions (PDFs), respectively. Assuming that the input phase during the JTOL test follows a sinusoidal trajectory with an additive Gaussian noise, PDFs $f_{sin}(\phi_{e,sin})$ and $f_N(\phi_{e,N})$ can be expressed as:

$$f_N(\phi_{e,N}) = \frac{2}{\sigma_{\phi_{e,N}}\sqrt{\pi}} e^{-\phi^2_{e,N}/2\sigma^2_{\phi_{e,N}}} \tag{2.36}$$

$$f_{sin}(\phi_{e,sin}) = \frac{1}{\pi\sqrt{(a^2_{in} - \phi^2_{e,sin})}} \tag{2.37}$$

where a_{in} is the amplitude of the sinusoidal jitter. The closed-form solutions to Eq. (2.36) and (2.37) are already given in [15]:

$$K_{PD,S} = \sqrt{\frac{2}{\pi}}(\frac{1}{\sigma_{e,N}})M(0.5, 2, -\rho^2)\alpha_T \tag{2.38}$$

$$K_{PD,N} = \sqrt{\frac{2}{\pi}}(\frac{1}{\sigma_{e,N}})M(0.5, 1, -\rho^2)\alpha_T \tag{2.39}$$

where ρ is the ratio between standard deviations $\sigma_{e,sin}$ and $\sigma_{e,N}$, and $M(a, b, z)$ is the confluent hypergeometric function defined as:

$$\rho = \frac{\sigma_{e,sin}}{\sigma_{e,N}} \tag{2.40}$$

$$M(a, b, \rho) = \sum_{n=0}^{\infty} \frac{(a)_n \rho^n}{(b)_n n!} \tag{2.41}$$

where $(a)_n = a(a+1)(a+2)\cdots(a+n-1)$. It is a solution to Kummer's differential equation [21]:

$$z\frac{d^2w}{dz^2} + (b - z)\frac{dw}{dz} - aw = 0. \tag{2.42}$$

Fig. 2.13 plots the values of this $M(a, b, -\rho^2)$ function for the two pairs of (a, b) used

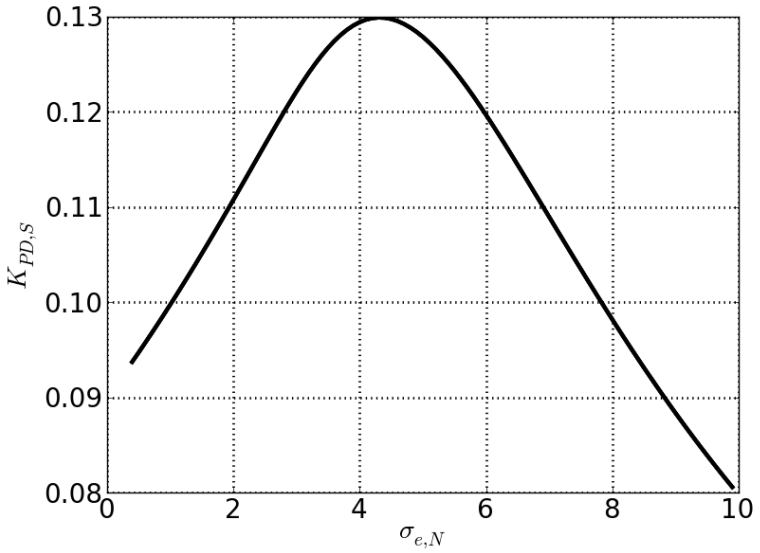


Figure 2.14: The $K_{PD,S}$ versus $\sigma_{e,N}$ when the sum of $\sigma_{e,N}$ and $\sigma_{e,sin}$ is limited to 10.

1.	Find initial values for $K_{PD,N}$ and $\sigma_{e,N}$ assuming $\rho = 0$ (i.e. random jitter only)
2.	Derive initial values for $K_{PD,N}$, $\sigma_{e,sin}$ and ρ: use $K_{PD,S} = K_{PD,N}$ and Eq. (2.43).
3.	Perform the following iteration: a. Calculate $K_{PD,S}$, $K_{PD,N}$ and σ_q from $\sigma_{e,sin}$, $\sigma_{e,N}$ and ρ using Eqs. (2.38), (2.39), (2.46). b. Calculate ρ, $\sigma_{e,sin}$ and $\sigma_{e,N}$ from $K_{PD,S}$, $K_{PD,N}$ and σ_N using Eqs. (2.40), (2.43) and (2.45) c. Repeat a-b until the solutions converge.

Figure 2.15: JTOL calculation procedure.

in Eqs. (2.38) and (2.39).

Fig. 2.13 shows that $M(a, b, -\rho^2)$ is a decreasing function of ρ, which means it is also an increasing function of $\sigma_{e,N}$. It is interesting to note that the inversely proportional relationship between the PD gain and $\sigma_{e,N}$ is weakened by $M(a, b, -\rho^2)$, but it is still a decreasing function of $\sigma_{e,N}$ as $1/\sigma_{e,N}$ decreases faster than the rate at

which $M(a, b, -\rho^2)$ increases. However, when the sum of $\sigma_{e,N}$ and $\sigma_{e,sin}$ is limited, it is no longer a decreasing function of $\sigma_{e,N}$, as shown in Fig. 2.14. This relationship will be used for the explanation of the random noise's effect on JTOL in the next section.

With zero deterministic input (i.e., $\sigma_{e,sin} = 0$), Eqs. (2.38) and (2.39) reduce to Eq. (2.30). On the other hand, as the sinusoidal jitter increases, the sensitivity of the linearized gains with respect to the random noise diminishes. In this case, the phase error is dominated by the sinusoidal portion of the input phase and the random noise has relatively less influence on the linearized gains.

The standard deviation of the phase error in the sinusoidal input tracking loop $\sigma_{e,sin}$ can be derived from the loop's transfer function, evaluated at the sinusoidal jitter frequency ω:

$$\sigma_{e,sin} = \frac{\sigma_{in,sin}}{|1 + K_{PD,S}G(e^{j\omega T_{ref}})|}. \tag{2.43}$$

Because the phase error is also a sinusoidal signal, its amplitude $a_{e,sin}$ can be calculated from its standard deviation:

$$\sigma_{e,sin}^2 = a_{e,sin}^2/2. \tag{2.44}$$

The standard deviation of the phase error in the random input tracking loop $\sigma_{e,N}^2$ must be calculated by integrating its output power spectral density (PSD) over the entire frequency:

$$\begin{aligned}\sigma_{e,N}^2 = &\int_{-0.5}^{0.5} \frac{S_{\phi_{in,N}}(\omega)}{|1 + K_{PD,N}G(\omega)|^2} d\omega \\ &+ \int_{-0.5}^{0.5} \frac{S_{\phi_{vco,N}}(\omega)}{|1 + K_{PD,N}G(\omega)|^2} d\omega \\ &+ \int_{-0.5}^{0.5} \sigma_q^2 |\frac{-G(\omega)}{1 + K_{PD,N}G(\omega)}|^2 d\omega.\end{aligned} \tag{2.45}$$

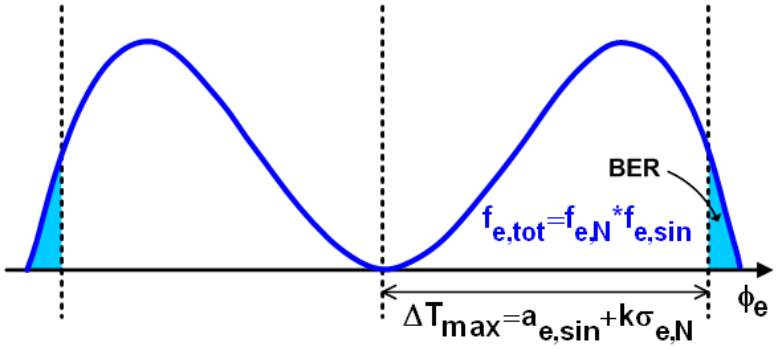


Figure 2.16: BER estimation in presence of sinusoidal and random components in the phase error.

And the quantization error power σ_q^2 can be found by carrying out a similar analysis with Eq. (2.24):

$$\begin{aligned} E[u^2] &= \sigma_q^2 + K_{PD,S}^2\sigma_{e,sin}^2 + K_{PD,N}^2\sigma_{e,N}^2 = \alpha_T \\ \sigma_q^2 &= \alpha_T - \frac{2}{\pi}\rho^2 M^2(0.5, 2, -\rho^2)\alpha_T^2 \\ &\quad - \frac{2}{\pi}M^2(0.5, 1, -\rho^2)\alpha_T^2. \end{aligned} \tag{2.46}$$

In summary, when the CDR's input phase characteristics are given, such as the probability distribution of its random component and the amplitude and frequency of its sinusoidal component, we can determine the parameters for the linearized loops $K_{PD,S}$, $K_{PD,N}$, $\sigma_{e,sin}$, $\sigma_{e,N}$, and σ_q according to Eq. (2.38), (2.39), (2.43), (2.45) and (2.46). Among them, $\sigma_{e,sin}$ and $\sigma_{e,N}$ describe the sinusoidal and random parts of the CDR phase error, which can be used to estimate the bit-error rate (BER) of the CDR.

Unfortunately, the closed-form formulas do not exist for calculating $\sigma_{e,sin}$ and $\sigma_{e,N}$. Instead, one should find the solution to the set of equations via iteration, following the procedure outlined in Fig. 2.15.

2.8 Jitter Tolerance Analysis

The BER of a CDR can be estimated based on the derived phase error components: the amplitude of the sinusoidal component $a_{e,in} = \sqrt{2}\sigma_{e,sin}$ and the standard deviation of the random component $\sigma_{e,N}$. Our assumption here is that there is a prescribed timing margin that achieves the target BER. In other words, the BER is deemed over the limit if the phase error exceeds a certain bound ΔT_{max}. Fig. 2.16 illustrates our method of estimating the BER in the presence of sinusoidal and random jitters. For instance, if there is no sinusoidal jitter, the worst phase error with BER of 10^{-12} is $7\sigma_{e,N}$. Whether the CDR meets the target BER can be determined by checking the following inequality:

$$a_{e,sin} + k(\rho, BER_{target})\sigma_{e,N} < \Delta T_{max} \tag{2.47}$$

where $k(\rho, BER_{target})$ is the multiplication factor of $\sigma_{e,N}$ which generates BER_{target} for a given ρ. Therefore, the JTOL analysis can be carried out by finding the maximum sinusoidal jitter amplitude a_{in} that satisfies the inequality in Eq. (2.47) at each frequency point. Note that it is possible to derive a more elaborate estimate on the BER by combining the statistical distribution of the phase error with that of the received signal (e.g., eye diagram) [22].

The inequality (2.47) can be simplified to a function of m and $\sigma_{e,N}$:

$$\sigma_{e,N} < \ \Delta T_{max}/\{\sqrt{2}\rho + k(\rho, BER_{target})\} \tag{2.48}$$

where $k(\rho, \Delta T_{max})$ can be pre-calculated as a function of ρ and BER_{target}. Assuming that the sinusoidal jitter and the random jitter are independent of each other, the PDF of $\sigma_{e,N} + \sigma_{e,sin}$ can be derived as the convolution between two PDFs in the

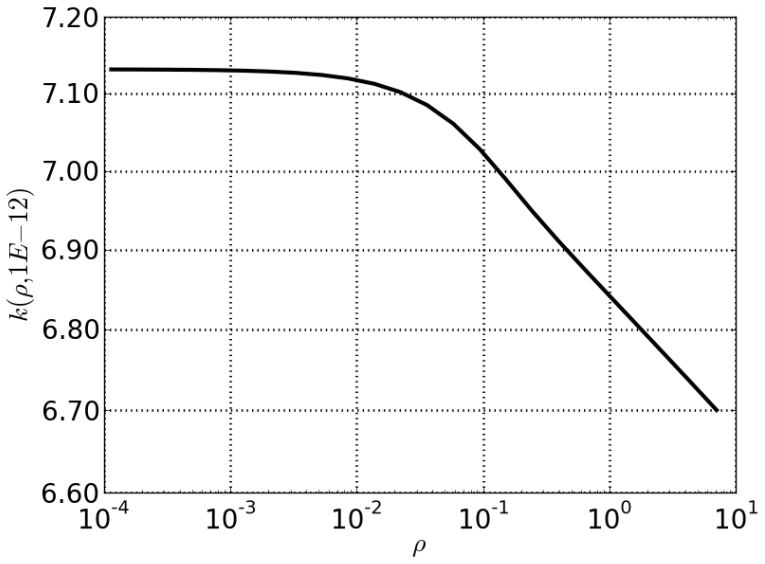


Figure 2.17: $k(\rho, BER_{target})$ when BER_{target} is 10^{-12}.

form of (2.36) and (2.37). The singular points of (2.37) at both ends can be avoided by approximating the PDF with a probability mass function [23]. Fig. 2.17 shows the calculated results when BER_{target} is 10^{-12}. When ρ is small, the random jitter dominates and the value of k is around 7.13, which corresponds to $\sqrt{2}\, erfc^{-1}(10^{-12})$ as expected. On the other hand, as ρ increases, k decreases as the contribution of the sinusoidal term increases.

It is convenient to note that Eq. (2.43) which governs $\sigma_{e,sin}$, hence $a_{e,sin} = \sqrt{2}\sigma_{e,sin}$ is the only equation that contains the sinusoidal jitter's frequency ω, and the other parameters such as $K_{PD,S}$ and $K_{PD,N}$ do not change with the frequency. In summary, the JTOL curve can be expressed as:

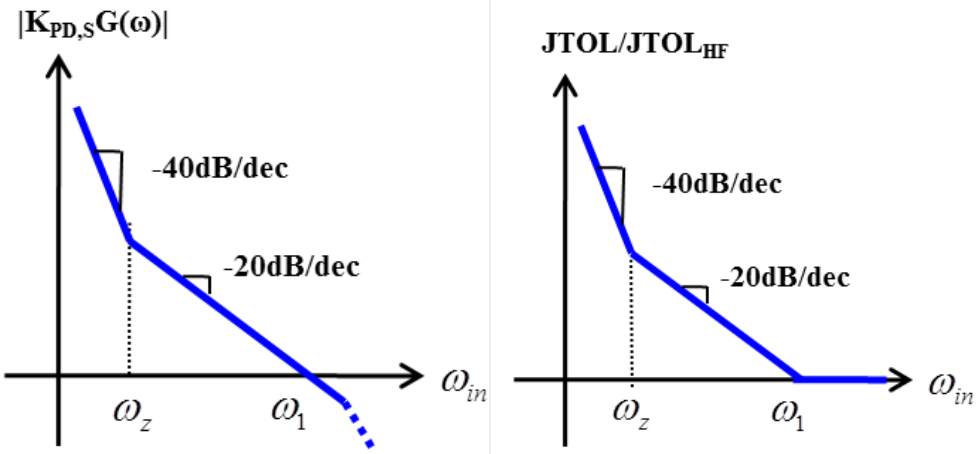
$$\begin{aligned} JTOL(\omega) &= a^*_{e,sin}(\omega)|1 + K^*_{PD,S}G(e^{j\omega T_{ref}})| \\ &= JTOL_{HF}|1 + K^*_{PD,S}G(e^{j\omega T_{ref}})| \end{aligned} \tag{2.49}$$

where $a^*_{e,sin}(\omega)$ is the largest amplitude allowed for the sinusoidal component of the phase error at the excitation frequency of ω and $K^*_{PD,S}$ is the corresponding linearized BBPD gain found by the described iteration. Note that the high-frequency jitter tolerance denoted as $JTOL_{HF}$ is equal to the high-frequency $a^*_{e,sin}(\omega)$, because all the input phase perturbations appear at the input of the BBPD at the frequencies beyond the tracking bandwidth of the CDR.

Eq. (2.49) implies that the JTOL curve can be computed once the linearized open-loop transfer function $K_{PD,S}G(e^{j\omega T_{ref}})$ is derived. Fig. 2.18 illustrates this relationship. For instance, the knee point in the JTOL curve corresponds to the frequency when the open-loop transfer gain is 1 (i.e., the unity-gain frequency). Above ω_1, $JTOL(\omega)$ is constant at $JTOL_{HF} = a_{e,sin}$ and below ω_1, it follows the open-loop transfer gain $K_{PD,S}G(e^{j\omega T_{ref}})$, scaled by $JTOL_{HF}$. For the case of a second-order BB-CDR, the open-loop transfer has two poles at DC and a zero below ω_1 while the other higher-order poles and zeros are kept above ω_1 to guarantee the stability of the feedback loop. The typical open-loop transfer of a second-order CDR is depicted in Fig. 2.18(a). The transfer gain initially falls at the slope of -40dB/decade and switches to the -20dB/decade slope at the zero frequency ω_z before the gain reaches 0dB. As a result, the JTOL curve also exhibits an initial slope of -40dB/decade and switches to -20dB/decade at ω_z before reaching the knee point at ω_1. Fig. 2.18(b) depicts the described asymptotic JTOL curve.

These predictions on the corner frequencies ω_z and ω_1 are consistent with those found by [8], which analyzed the JTOL characteristics of a charge-pump-based BB-CDR based on slewing:

$$\omega_1' = K_{VCO}I_{CP}R/2 \quad (\approx \omega_1 = K_{PD}K_{VCO}I_{CP}R/2\pi)$$



(a) (b)

Figure 2.18: (a) The linearized open-loop transfer function of a second-order BB-CDR and (b) its asymptotic JTOL curve showing the shift in slope at the zero frequency (ω_z) and the unity-gain frequency (ω_1)

$$\omega_z' = 0.63\pi/RC \approx 1.98 \cdot \omega_z \tag{2.50}$$

where ω_z' and ω_1' denote the corner frequencies predicted by [8]. It should be noted that the analysis in [8] did not include the effects of noise, while ours does. The proposed analysis validates the previous analyses of BB-CDR characteristics and extends them to include the effects of random noise, transition density and loop delay.

The predicted JTOL curves based on Eq. (2.49) are compared with the results from the time-accurate behavioral simulations. Fig. 2.19 (a) and (b) plot the JTOL curves for different CDRs with different ϕ_{bb} and τ_N values, respectively. The theoretical predictions (in solid lines) slightly overestimates the JTOL, but they are in good agreement with the simulation results (in dashed lines) with matching corner frequencies for all the cases. As ϕ_{bb} increases the tracking capability of the loop also

improves, and ω_1 moves toward the higher frequency as shown in Fig. 2.19 (a). On the other hand, Eq. (2.2) suggests that as τ_N increases, the zero frequency ω_z should move toward the lower frequency as observed in Fig. 2.19(b), which manifests itself as a change in the corner frequency at which the slope changes from -40dB/decade to -20dB/decade.

The effect of random noise on the jitter tolerance characteristic is shown in Fig. 2.19(c). As eq. (2.48) suggests, the random noise leads directly to a degradation in the high-frequency JTOL. It is interesting to note that the knee point shifts to a higher frequency as the random noise increases, whereas the -3dB bandwidth of jitter transfer decreases. This trend stems from the proportional relationship between the random noise and the PD gain when $\sigma_{e,N} < \sigma_{e,sin}$, as shown in Fig. 2.14. When the target BER is determined, the sum of the sinusoidal error and random error is limited by Eq. (2.48) and the PD gain and ω_1 become proportional to the amount of random noise.

The result based on [8] is overlayed on Figs. 2.19(a), (b) and (c). As the theory does not include the effect of input jitter or transition density $\sigma_{\phi_{in}} = 0$ and $\alpha_T = 0.5$ are assumed. Default parameters are ϕ_{bb}=$2mUI$, τ_N=100, $\sigma_{\phi_{in}}$=$50mUI$, α_T=50%, N_d=$0UI$, and BER_{target} is 10^{-3} The corner frequencies based on both theories match with various ϕ_{bb} and τ_N, but the predicted JTOL based on the proposed theory is smaller than the one based on [8] even when there is no input noise. The predicted high-frequency JTOL is 0.5 because it does not include the effect of loop behavior in this region. It is apparent that the high frequency JTOL should be less than 0.5 UI in the actual case because the loop does not stays at one state. When the result based on [8] is shifted so that the high frequency JTOL is same with

the one predicted by the proposed theory, both theories show good agreements as depicted in Fig. 2.19 (c).

Figs. 2.19(d) and (e) illustrate the effects of transition density and loop delay on the jitter tolerance, respectively. Since the linearized gain $K_{PD,S}$ is proportional to the transition density according to Eq. (2.38), it is expected that the corner frequency increases along with it.

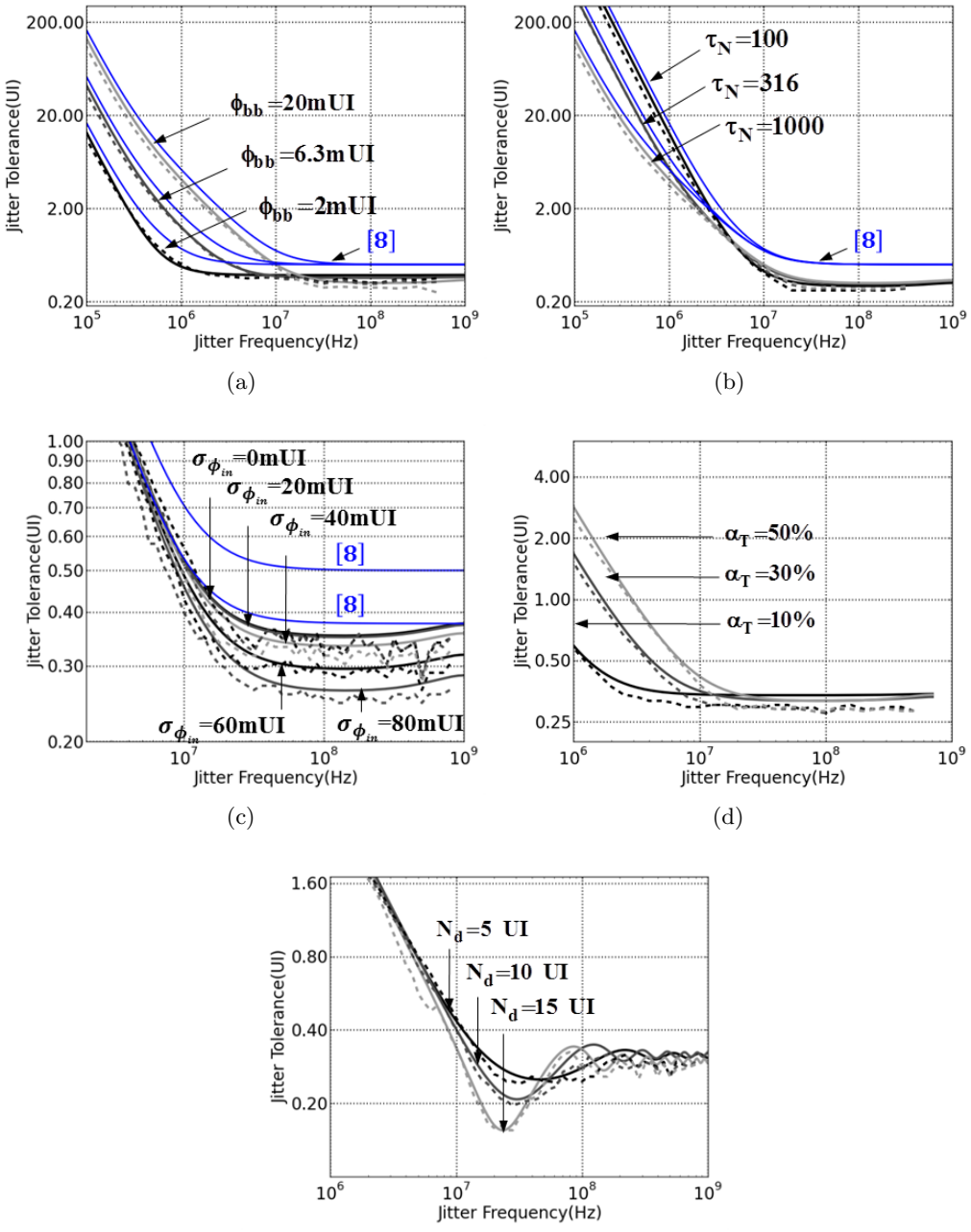


Figure 2.19: Comparison of the JTOL curves between the theoretical (solid) and simulation results (dashed) on BB-CDRs with various range of design parameters: (a) bang-bang phase step (ϕ_{bb}), (b) normalized time constant of loop filter (τ_N), (c) input rms jiiter ($\sigma_{\phi_{in}}$), (d) transition density (α_T) and (e) loop delay (N_d).

Chapter 3
Nonlinear Analysis of Bang-Bang Controlled Loops

When there is no sufficient noise to linearize the loop, nonlinear behavior such as dithering and slewing dominates the loop's behavior. The difficulty with a non-linear system model is that there is no single analysis technique that can account for all nonlinear phenomena. This chapter introduces various non-linear analysis techniques that have been used for the prediction of bang-bang PLLs, and extends them to the CDRs. During the explanation, the model and notations described in chapter 2 will be used.

3.1 Transient Analysis of Bang-Bang Controlled Timing Loops

Transient simulation is the most versatile way of analyzing the behavior of dynamical systems. However, they may require an impractically long simulation time in order to estimate the statistical property of rare events such as the bit-error rate (BER) of high-speed I/Os. For instance, the confidence interval analysis shows that nearly 4×10^{14} bit times would be necessary to estimate a target BER of 10^{-12} with 10% accuracy and 95% confidence. Even if the simulator is capable of simulating 10,000 bits per second, it would take almost 1,270 years to collect all these samples.

For the fast analysis, it is possible to compute the statistics directly based on

analytical methods. For instance, the distribution of a sum of two random variables can be computed as the convolution between the two probability density functions (PDFs). There have been many solutions using this approach to estimate the BERs in high-speed I/O interfaces [22, 24, 25]. However, to simplify the computations, certain approximations may be made such as ignoring the correlations among noisy signals. Furthermore, the analytical formulations and approximations are strongly tied to the assumed transceiver configureation or clocking architecture and a new set of formulations will be required if the configureation or architecture changes. For this reason, most tools in this category only take a set of parameter values for the preconfigured I/O interface as the inputs.

This section introduces an efficient way of simulating the statistical properties of dynamical systems leveraging the versatility of conventional transient simulation while improving its efficacy by supplementing the time-domain simulation results with conditional PDFs. The conditional PDF (CPDF) in our context refers to the probability distribution of the signal x at the present time n when all the sample values at prior times $x[n-1]$, $x[n-2]$, ... are given:

$$\begin{aligned} &f_X(x_i[n] \mid \text{past } x_i[\cdot]\text{samples}) \\ &= f_X(x_i[n] \mid x_i[n-1] = x_{-1},\ x_i[n-2] = x_{-2}, ...) \end{aligned} \tag{3.1}$$

In other words, the simulator calculates all the possible values with their associated probabilities given the past samples. For example, if the transmitter is transmitting 1, the CPDF of driver output with voltage noise will have distribution around its high level while conventional time-domain simulator gives only one sample at any given time. As the CPDF contains richer information than a single time-domain simulation sample on the signal's statistics at the present time, it helps to achieve

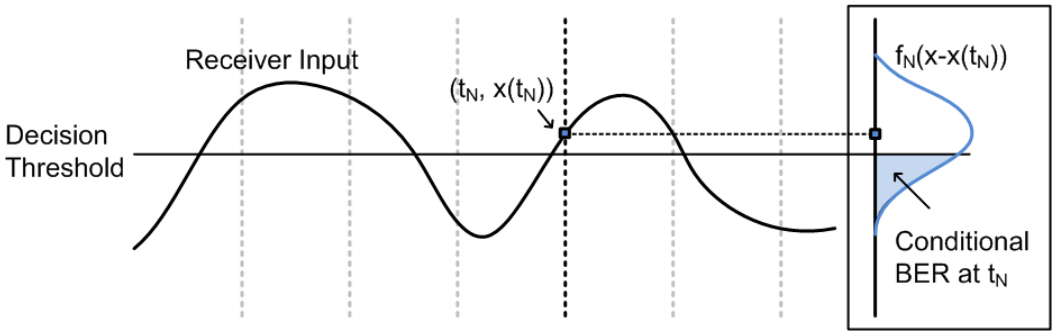


Figure 3.1: An example of CBER calculation.

higher accuracy than estimations made with samples only.

Leveraging the rich information of CPDF, various statistics of a random process such as the mean, PDF, and auto/cross-correlations can be computed based on the CPDF. The mean and PDF are derived by averaging the conditional ones with various conditions as follows:

$$\mathrm{E}\left[x[n]\right] \approx \frac{1}{N}\sum_{i=1}^{N}\mathrm{E}\left[x_i[n] \mid \text{past } x_i[\cdot]\text{samples}\right] \tag{3.2}$$

$$f_X(x[n]) \approx \frac{1}{N}\sum_{i=1}^{N} f_X(x_i[n] \mid \text{past } x_i[\cdot]\text{samples}) \tag{3.3}$$

where N is the total number of samples and $x_i[n]$ denotes the i-th sample of the signal x at the present time n. Similarly, the auto/cross-correlations can be computed as follows:

$$\begin{aligned} R_{XX}(k) &= \mathrm{E}\left[x[n]\cdot x[n-k]\right] \\ &\approx \frac{1}{N}\sum_{i=1}^{N}\mathrm{E}\left[x_i[n] \mid \text{past } x_i[\cdot]\text{samples}\right]\cdot x_i[n-k] \end{aligned} \tag{3.4}$$

Likewise, the BER can be estimated as the time-average of the conditional BERs (CBERs). The first thing need to be done for this analysis is to derive the CPDF

of the sampled input. In general, it is computed by combining all the CPDFs of the mutually-independent noises via convolution. Assuming that the effective voltage noise at the input of the system can be derived, the CPDF has the same distribution of that noise with its mean at the time-domain sample. Next, the CBER of the corresponding bit can be computed as the total conditional probability of the sampled voltage exceeding the decision threshold. Fig. 3.1 shows an example of CBER calculation. For the input voltage sampled at t_n, the CBER is

$$CBER = \int_{threshold}^{\infty} f_N(x - x(t_n))dx \tag{3.5}$$

where f_N is the PDF of the effective voltage noise at the input. Once the CBER at each sample is calculated, the BER and its confidence interval can be derived from the mean and variance of measured CBERs, respectively.

This technique was integrated to the event-driven HDL simulator [19], and applied to measure the BER of a 12.5Gbps serial I/O system consists of driver, transmitter-side PLL, channel, receiver, and receiver-side clock and data recovery circuit (CDR). The measurement of BERs less than 10^{-12} with 10% accuracy and 95% confidence required only 1.6×10^7 of symbols, which is $1/(4 \times 10^4)$ times fewer than the conventional time-domain analysis.

3.2 Phase-portrait Analysis of Bang-Bang Controlled Timing Loops

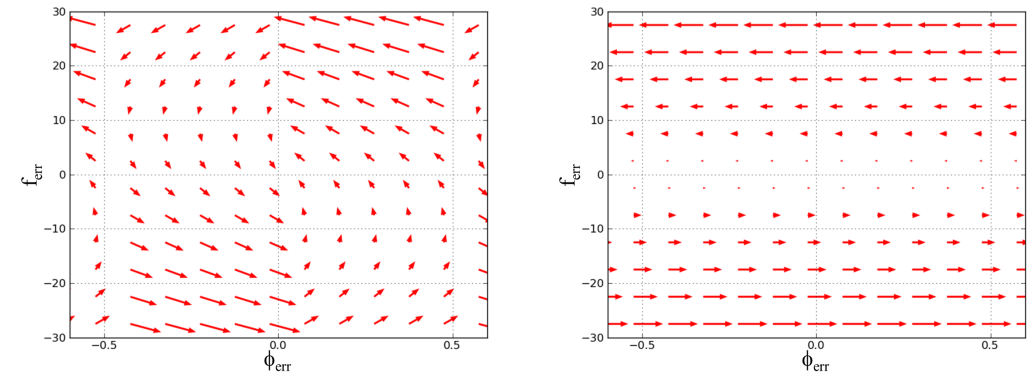
For analyzing the deterministic beahviors such as dithering and loop stability, the phase-portrait, a two-dimensional vector plot of loop variables, has been shown effective [5, 9]. It draws the direction and amplitude of the state transition at each

point in a two-dimensional design space. As an example, Fig. 3.2 plots the trajectory directions of a 2nd order BBPLL in a bidimensional phase plane (ϕ_{err}, f_{err}) where ϕ_{err} and f_{err} represents phase error and frequency error, respectively.

From Fig. 3.2 (a), it can be seen that there is a finite region converging to the lock point at the center. When the phase error is less than a half UI and the frequency error is small, the phase error and frequency error gradually decrease. However, they dither around the lock point in a steady state rather than converging to a single point because the BBPD always tells UP or DOWN. In the state space, the loop follows a circular trajectory and forms a limit cycle. The bang-bang controlled loop is regarded to be stable in a wide sense when the loop has a limit cycle.

Outside the convergence region, the loop does not converge to the lock point but crosses the bit boundary. Even when the phase error is less than a half UI, the output phase can cross the bit boundary when the frequency error is large as shown in Fig. 3.2 (a). This phenomenon which is called bit-slipping happens when the frequency error is bigger than the BBPD's 'pull-in range' which is the range where the BBPD can pull the loop to the lock point. Most PLLs do not experience bit-slipping once the loop is stabilized because the dithering radius is quite small comparing with the region of convergence. However, CDRs can lose data due to the bit-slipping especially when the loop has large dithering radius and its input has low transition density. If the input does not have the bit-transition BBPD cannot adjust the phase and the output phase drifts according to the frequency error as shown in Fig. 3.2 (b).

To avoid bit-slipping, small limit cycle and high transition density of the input signal is preferrable. Limit cycle can be reduced by minimizing the loop delay [32]



(a) (b)

Figure 3.2: Phase-portrait of bang-bang controlled timing loop when the transition density is (a) 100% and (b) 0%.

or using decimation [33] that will be explained in Section 3.4.3. Other than that, many of modern high-speed I/Os adopt data coding to ensure a certain level of transition density [34]. A decimation technique that ensures constant jitter performance regardless of the transition density will be introduced in Chapter 4.

3.3 Markov-chain Analysis of Bang-Bang Controlled Timing Loops

To find the statistical characteristics such as jitter distribution, modeling the bang-bang controlled loop as a Markov chain has been found effective [6, 17]. It models a system in a quantized state space with predictable transition probability to find the final distribution. Even though that technique was originally applied to find the linearized gain of the bang-bang controlled loop, it can help to find the statistical information of CDRs especially when predicting the bit error rate (BER).

The Markov-chain analysis finds the distribution of output phase in a stochastic

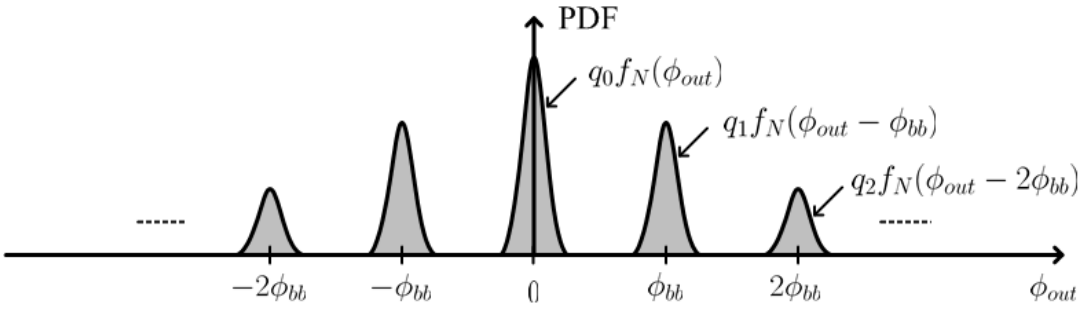


Figure 3.3: Probability density function of bang-bang controlled loop's output phase.

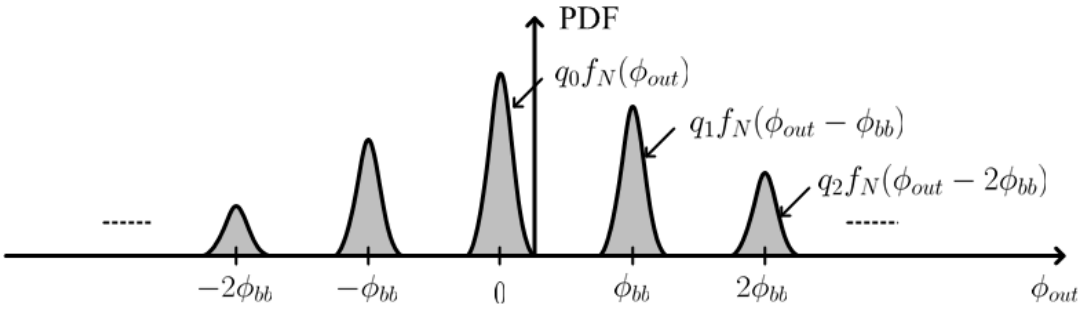


Figure 3.4: Asymmetric stabilized phase distribution

sense. Firstly, it quantizes the output phase with ϕ_{bb} of step assuming that the integral path is negligible comparing with the proportional path. Fig. 3.3 shows the probability density function (PDF) of output phase where the probability density at $n\phi_{bb}$ is q_n. Among the quantized phases, we denoted the one at the ideal position to be 0. From this PDF, the PDF of timing error can be found by convolutioning it with the PDF of total input-referred random noise, $f_N(\phi)$. When the PDF of timing error is not centered around 0, the BBPD generates more UPs or DOWNs according to the polarity of the bias, and the loop is stabilized when the cummulative probability density of the timing error under 0 is same with the one over the lock point.

Next, the transition probability from each output phase is calculated to build a

transition probability matrix. For example, if the current output phase is ϕ_x and the random noise has $f_N(\phi)$ of probability density function (PDF), the probability of UP and DOWN can be calculated by

$$\begin{aligned} P_{UP} &= \int_{-\infty}^{0} f_N(\phi - \phi_x) d\phi \\ &= \int_{-\infty}^{-\phi_x} f_N(\phi) d\phi \\ P_{DN} &= \int_{0}^{\infty} f_N(\phi - \phi_x) d\phi \\ &= \int_{-\phi_x}^{\infty} f_N(\phi) d\phi. \end{aligned} \tag{3.6}$$

Likewise, the transition probability from an arbitrary phase $i\phi_{bb}$ to the next phase $(i+1)\phi_{bb}$ in a quantized phase domain can be generalized as

$$\begin{aligned} G_{-i} &= F_N(-i\phi_{bb}) \\ &= \int_{-\infty}^{0} f_N(\phi - i\phi_{bb}) d\phi \\ &= \int_{-\infty}^{-i\phi_{bb}} f_N(\phi) d\phi \end{aligned} \tag{3.7}$$

where F_N is the cummulative distribution function of the total input-referred noise. Therefore, the transition probability matrix T where its element (i, j) is the proba-

bility of transition from ϕ_i to ϕ_j can be defined as

$$T = \begin{bmatrix} \ddots & & & \vdots & & & \\ & 0 & G_2 & 0 & 0 & 0 & \\ & 1-G_1 & 0 & G_1 & 0 & 0 & \\ \cdots & 0 & 1-G_0 & 0 & G_0 & 0 & \cdots \\ & 0 & 0 & 1-G_{-1} & 0 & G_{-1} & \\ & 0 & 0 & 0 & 1-G_{-2} & 0 & \\ & & & \vdots & & & \ddots \end{bmatrix}$$

Finally, the stationary probabilities q_n can be found by solving a Chapman-Kolmogorov equation

$$\mathbf{q} = \mathbf{q} \cdot \mathbf{P} \tag{3.8}$$

where $\mathbf{q}$ is the row vector $\begin{bmatrix} \cdots & q_{-2} & q_{-1} & q_0 & q_1 & q_2 & \cdots \end{bmatrix}$. The solution of this equation can be found by iteration or deduction assuming symmetry of f_N around 0 [6]. This equation usually can have multiple of periodic solutions with period of 2. As we are finding the steady-state solution, the two distributions must be averaged so that a single steady state distribution can represent the overall state distribution.

During the analysis, the ideal phase was assumed to be ϕ_0, but this is impossible when the loop has finite number of pre-determined phases. For these systems, the stabilized phase distribution can be asymmetric as shown in Fig. 3.4. The steady state can have asymmetric distribution only if the accumulated probabilities above/under the origin have the same value. Even for the conventional 2nd-order bang-bang phase lockd loop with symmetric f_N, there is another stabilized phase distribution beside the case where ϕ_0 is at the center of the phase distribution; the

ideal phase can exist at the middle of two phases. For a complete analysis of the loop behavior, all the possible cases aforemetioned need to be considered. Especially when the input and output has small frequency offset, the relative phase of the input slowly drifts and the phase ditribution slowly changes between Fig. 3.3 and Fig. 3.4. However, as the phase drift is quite slow assuming small frequency offset, analyzing the extreme two cases in the figure without considering time-varying offset can guarantee the completeness of that analysis without loss of accuracy.

3.4 Analysis of Clock-and-Data Recovery Circuits

Clock-and-Data recovery (CDR) circuits have different characteristics and evaluation metrics comparing with PLLs. For example, their input is not a periodic clock but a random data sequence that has less than 100% of transition density. This section extends the analyses explained earlier in this chapter to predict the bit-error rate (BER), the most important metric of CDRs. The analysis includes the effect of various design parameters such as transient density, decimation and deadzone width.

3.4.1 Prediction of Bit-Error Rate

Comparing with PLLs that give the highest priority to low jitter, CDRs have different metrics for the evaluation. The key criterion for CDRs is the bit-error rate (BER). As most of I/Os require less than 10^{-12} of BER, its simulation based on traditional transient simulation is quite unrealistic. Therefore, the analysis technique that can efficiently predict the BER is essential for the design of bang-bang controlled CDRs. For example, the CPDF-based analysis explained in Section 3.1 is quite useful for the prediction of BER. However, it still needs long simulation time because it needs to collect multiple samples.

In this context, the Markov-chain analysis explained in Section 3.3 is time-efficient to predict the steady-state BER. Once the distribution of output phase, **q** is found, the BER can be calculated by accumulating the probability when the timing error exceeds the bit boundary:

$$BER = \sum_{n=-\infty}^{\infty} q_n \left(F_N(\phi_{left} - n\phi_{bb}) + 1 - F_N(\phi_{right} - n\phi_{bb}) \right) \tag{3.9}$$

where ϕ_{left} and ϕ_{right} represents the positions of left and right bit boundaries, respectively.

For the accurate prediction of CDR's performance with Markov-chain analysis, various design parameters such as transition density, decimation length and deadzone width must be considered when deriving the transition matrix. Following sections will explain the effect of these parameters.

3.4.2 Effect of Transition Density

The most eminent difference of CDR from PLL is that the CDR input has lower than 100% of transition density. As the transition density is closely related with the behavior of bang-bang controlled loops, its effect must be carefully considered when extending the analysis basically used for the PLLs to the CDRs.

Basically, less than 100% of transition density reduces the number of effective input samples as the loop cannot detect and adjust the phase without transition edge in the input signal. Therefore, low transition density leads to narrow loop bandwidth and poor tracking capability. For the same reason low transition density incurs phase drift resulting in bit slippling described in Section 3.2. In addition, it also affects the BER. Detailed explanation will be given later in this section.

The Markov-chain analysis described in Section 3.3 requires modification of the

transition probability matrix to take the transition density into account:

$$T = \begin{bmatrix} \ddots & & & \vdots & & & \\ & 1-\alpha & \alpha \cdot G_2 & 0 & 0 & 0 & \\ & \alpha \cdot (1-G_1) & 1-\alpha & \alpha \cdot G_1 & 0 & 0 & \\ \cdots & 0 & \alpha \cdot (1-G_0) & 1-\alpha & \alpha \cdot G_0 & 0 & \cdots \\ & 0 & 0 & \alpha \cdot (1-G_{-1}) & 1-\alpha & \alpha \cdot G_{-1} & \\ & 0 & 0 & 0 & \alpha \cdot (1-G_{-2}) & 1-\alpha & \\ & & & \vdots & & & \ddots \end{bmatrix}$$

where α stands for the transition density ranging from 0 to 1.0. Comparing with Eq. (3.7), the transition probability to adjacent phases are scaled by α while the output phase holds current status with $1-\alpha$ of probability.

Even though the transition density changes the transition probability matrix, it does not affect the steady-state distribution. It can be easily verified with simple mathematics as follows. Let's assume that the origital transition probabilities from A to B and B to A as G_{AB} and G_{BA}, respectively. Then, the steady state probabilities of the states, P_A and P_B must satisfy

$$P_A \cdot G_{AB} = P_B \cdot G_{BA}. \tag{3.10}$$

On the other hand, the steady state probability with non-100% transition density satisfies

$$\alpha \cdot P_A \cdot G_{AB} = \alpha \cdot P_B \cdot G_{BA}. \tag{3.11}$$

It can be seen that the probabilities P_A and P_B satisfies the Eq. (3.10) also satisfies Eq. (3.11). This result can be explained in a quantitative way. Let's assume that

the loop is in a steady state $\mathbf{q}$ that satisfies Eq. (3.8) when the transition density is 100%. If the next bit has bit-transition, the steady state distribution will not change. On the other hand, if there is no transition in the input, the loop does not change the current output phase and holds the current phase distribution only when there is no frequency offset.

Considering that the jitter transfer bandwidth of conventional linear CDR changes along with the transition density of its input, this is an interesting observation. The difference comes from the nonlinear characteristics of the system. In a linear system, random input noise is filtered and shaped by the transfer function of the system. On the other hand, the results explained in the chapter is showing the jitter caused by the dithering which is a special behavior of nonlinear system. The small-signal analysis of pseudo-linear model described in Chapter 2 shows that the jitter transfer of the bang-bang controlled system does change according to the transition density of the input. However, in the case when the dithering dominates the random noise, the jitter distribution of the output is independent of the transition density while the frequency-domain spectrum can change.

Once the steady-state distribution is found by solving Eq. (3.8) with Eq. (3.4.2), the expected BER can be derived as was done in Section 3.4.1. It is remarkable that the BER is related with the transition density even though the transition density does not affect the steady-state distribution. The BER is scaled by the transition density (α) as the sampling of neighboring bit does not generate bit-error if the poliarity of the next bit is same with the current one. Including this effect, Eq. (3.9)

becomes

$$BER = \sum_{n=-\infty}^{\infty} \alpha \cdot q_n \left(F_N(\phi_{left} - n\phi_{bb}) + 1 - F_N(\phi_{right} - n\phi_{bb}) \right). \tag{3.12}$$

In summary, the BER is proportional to the transition density of the input in steady-state while the dithering amount does not change.

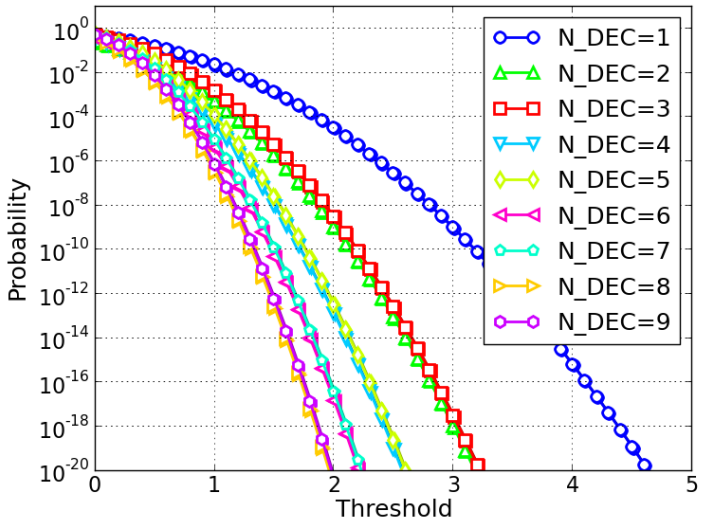
3.4.3 Effect of Decimation

Many of bang-bang controlled timing loops collect more than one phase information before making a decision to improve the reliability. Namely, the loop decimates the BBPD outputs.

The decimation poses two major effects on the loop behavior. First, it reduces the effective delay and limit cycle. As the decision is made sparsely, effective update cycle (T_{ref}) is increased by the decimation ratio, N_{DEC}. Therfore, the loop delay in update cycle unit (N_d) is scaled down by the same factor. As the dithering amount is related with the effective loop delay, decimation and short loop delay help to suppress the dithering.

However, decimation length cannot be set too long because increased update cycle limits the tracking bandwidth. To maintain high tracking bandwidth even with decimation the system needs a large phase adjustment step (ϕ_{bb}), which increases the dithering amount again unless the dithering is completely eliminated. Consequently, decimation needs to be done carefully considering both the tracking bandwidth and dithering amount.

Dither can be suppressed also by minimizing the loop delay itself rather than using decimation. Following this approach, some timing systems exploit feed-forward paths that directly apply the PD output to the clock generator [32]. As this technique



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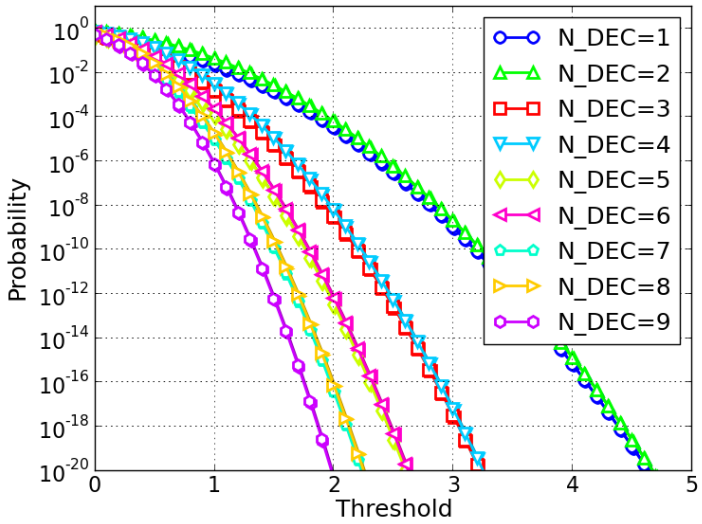


(b)

Figure 3.5: Error probability of gaussian distributed random jitter $N(0, \sigma_N)$ exceeding the threshold when majority voting algorithm with N_{DEC} of samples are performed. For the tie of votes, (a) does not decide it to be an error while (b) does.

does not increase the update cycle, it is commonly used when the system needs a high loop bandwidth. For example, it is widely used for the BBPLLs which have clean reference clock because the high bandwidth helps to suppress the effect of the phase noise generated by a clock generator. Meanwhile, most CDRs have jittered inputs caused by inter-symbol interference (ISI), crosstalk and power supply noise of transmitter. Accordingly the high loop bandwidth does not always result in the best performance. In this reason many CDRs adopt decimation rather than exploiting feed-forward path.

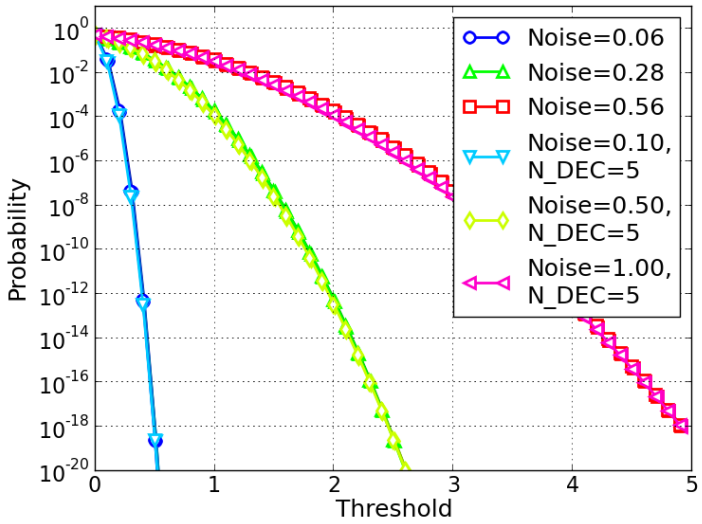
Secondly, the decimation improves the confidence level of the decision. The accuracy of statistics can be evaluated using the confidence analysis based on the central limit theorem. For instance, the true value of $\mathrm{E}[x[n]]$ is expected to lie within the interval [36]:

$$|\mathrm{E}[x[n]] - \overline{X}| \leq \rho \frac{\sigma_X}{\sqrt{N_{DEC}}} \tag{3.13}$$

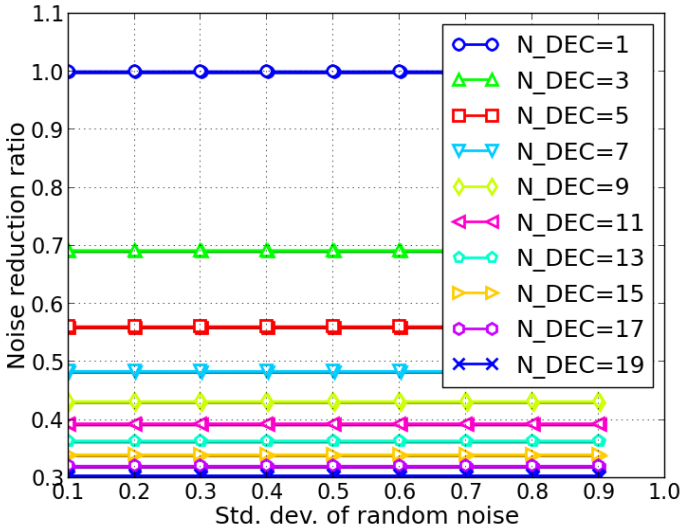
where $\overline{X}$ is the sample mean and σ_X^2 is the variance of $x[n]$. The constant ρ is determined by the confidence level. For example, ρ is 2 when estimating the 95% confidence interval. Eq. (3.13) indicates that the accuracy of the estimate improves with the number of samples, N_{DEC}.

Among various decimation algorithms, majority voting is the most popular one due to its simplicity. It selects the alternative that has the majority. For example, if the BBPD decides UP for 5 out of 8 samples, the majority voting loop controller decides to advance the output phase.

Fig. 3.5 shows the probability that the gaussian distributed random jitter $N(0, \sigma_N)$ exceeding the threshold when majority voting algorithm with various N_{DEC} is applied where σ_N is the standard deviation of the random jitter. In other words, it is



(a)



(b)

Figure 3.6: (a) The error probabilities with majority voting with decimation for σ_N=0.1, 0.5 and 1.0 (ϕ_{bb}) and the ones without decimation that gives the same results. (b) The simulated noise reduction ratio of majority voting decimation.

plotting

$$\int_{threshold}^{\infty} \sum_{ceil(N_{DEC}/2)}^{N_{DEC}} \frac{1}{\sqrt{2}\pi} exp(-\frac{x^2}{2\sigma}) dx \tag{3.14}$$

where $ceil(\cdot)$ represents the minimum integer value greater or equal to the input value. This error probability corresponds to the BER when the threshold is set to the distance of bit boundary from the sampling position. It can be clearly seen that the higher decimation ratio reduces the probability of the errors because of the improved confidence level. One interesting thing is that the trend with even N_{DEC} is totally different according to the decision of tie. If the loop changes the output phase when exactly a half of votes were correct while another half was wrong, the resulting error is smaller comparing even with the decimation of one more bit as shown in Fig. 3.5(a). On the other hand, if the tie is regarded as an error, the error probability is higher than the one with the decimation of one less bit as shown in Fig. 3.5(b). In this thesis, we regard the tie as a correct bit, which corresponds to the results of Fig. 3.5(a).

It is notable that the improved confidencel level due to the decimation is effectively same with the reduction of random noise. That is, decimation of multiple samples can have the same level of confidence with the one-time sampling under less noisy condition.

The noise reduction effect of majority voting can be quantified by finding the standard deviation of the noise distribution that gives the same error probability. Fig. 3.6(a) overlays the error probabilites derived with 5-bit decimation over the ones with no decimation and larger noise that gives similar results. It can be observed that the noise reduction ratio is around 0.6 for all the cases. Fig. 3.6(b) clearly shows that the noise reduction ratio is independent of σ_N. There is a negative relationship

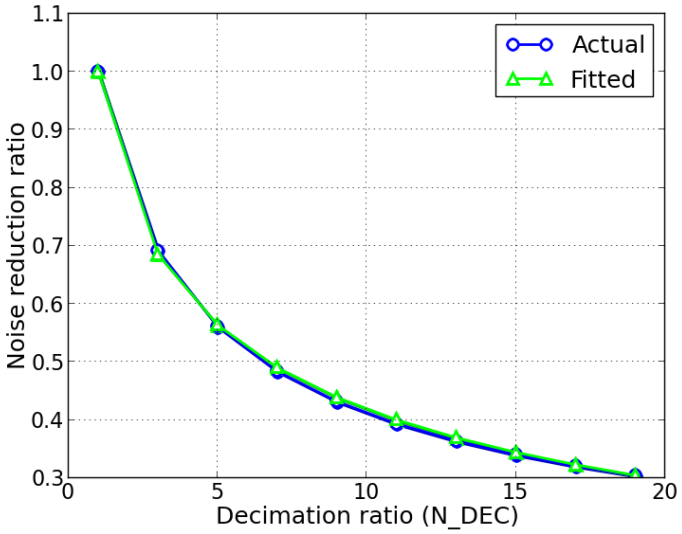


Figure 3.7: The comparison between simulated noise reduction ratio and Eq. (3.15).

between the noise reduction ratio and the decimation ratio where the noise reduction ratios for various decimation lengths are summarized in Fig. 3.7. For example, the ratio is about 0.7 when N_{DEC} is 3 and decreases to 0.3 when N_{DEC} is 19. The fitted noise reduction ratio is

$$f_{NR} = \frac{1}{0.94N_{DEC}^{0.28} + 0.06N_{DEC}}, \tag{3.15}$$

and the maximum error is 1.71% when N_{DEC} is 5. This fitted equation is useful when estimating the effect of majority voting.

3.4.4 Analysis of Oversampling Phase Detectors

One problem of BBPD is that the effective PD gain changes along with the distribution of phase error as explained in Chapter 2. As the designers want the PD gain and the loop bandwidth to be predictable, stable PD gain is desired.

As a solution to that problem, more than 2× of oversampling phase detectors are used. Fig. 3.8 shows the transfer curve of oversampling phase detectors with 2∼4 of oversampling ratio. A 2× oversampling phase detector as called as BBPD tells only the polarity while 4× oversampling phase detectors tell the magnitude in two quantized levels. For example, the output in the figure has twice bigger magnitude when the phase error exceeds $\phi_{4-} \sim \phi_{4+}$. With higher oversampling ratios, the transfer curve approaches to the linear one. Especially when the phase detector experiences the random noise, the transfer function is smoothed and become linear in a stochastic sense.

On the other hand, phase detection with odd number of oversampling phases has an input phase interval with zero gain which is called a dead-zone. If the detected phase error is inside the deadzone, the phase detector asserts 'HOLD', and the loop does not change the sampling clock phase. For example, the 3× oversampling phase detector in Fig. 3.8 generates 'HOLD' when its input phase is in the deadzone ranging from ϕ_{3-} to ϕ_{3+}.

As the loop holds the current output phase when the desired phase is inside the deadzone, it can basically eliminate the dithering, but it has some drawbacks. Firstly, the output phase can wander inside the deadzone, which can increase the jitter especially when the deadzone is wide. As the loop cannot correct the phase error in the deadzone, jitter cannot be rejected by the feedback loop. Secondly, it does not guarantee the ideal output phase. Even when the neighboring phase is better than the current one, the loop holds the current status only if the phase error does not cross the boundary of deadzone. Finally, it can result in poor tracking performance. For the systems with non-zero frequency error between the transmitter

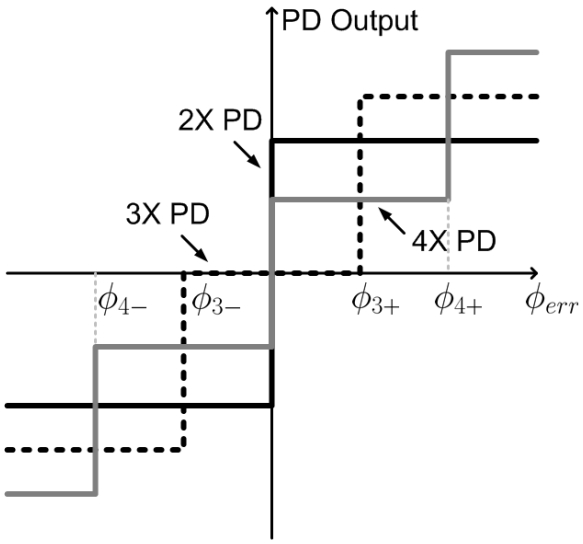


Figure 3.8: Input-to-output relationships of oversampling phase detectors.

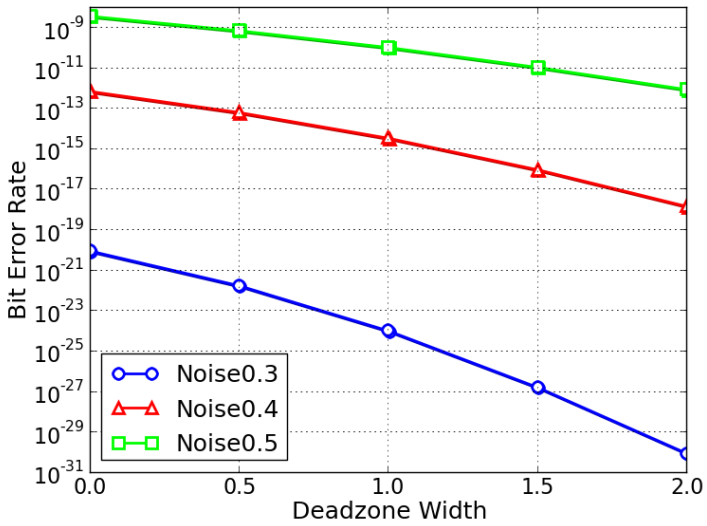


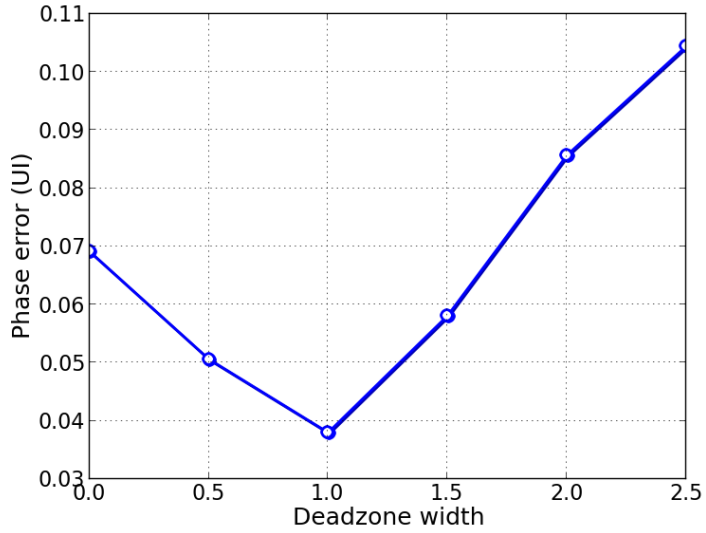
Figure 3.9: The expected BER of the 3× oversampling timing loop with various width of deadzones.

and the receiver, the loop must track the phase error. In theses systems, the phase detector with deadzone acts as a BBPD with the offset as large as a half of the deadzone width. The reduction of tracking bandwidth can be critical for the systems with spread-spectrum clock generation as their clock phase changes continuously.

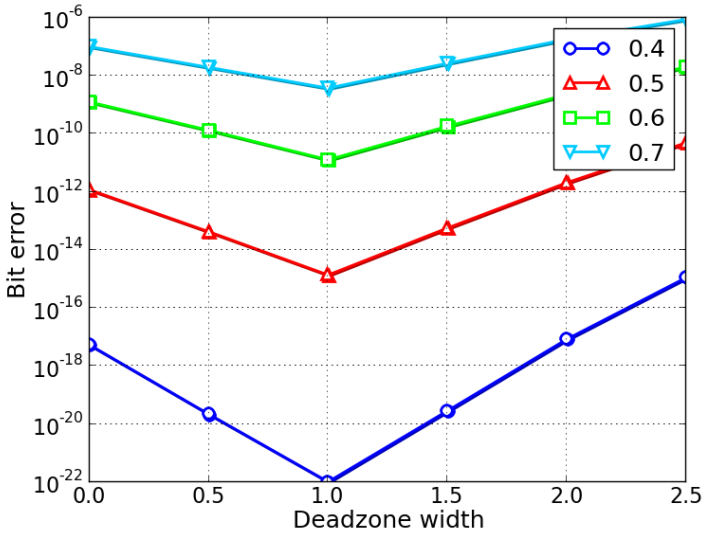
This section explains the effect of deadzone to the loop dynamics of the CDRs. Especially, the relationship between the deadzone width and BER will be examined. Even though many of more than 2× oversampling systems aim to linearize the loop behavior, this section assumes nonlinearized condition that includes small amount of random noise. Linear analysis of more than 3× oversampling phase detectors can be done with a similar technique described in Chapter 2.

Basically, the wider deadzone tends to result in lower BER assuming that the loop is initially locked and there is no frequency offset between the input and the output. Fig. 3.9 shows the expected BER versus the deadzone width of 3× oversampling timing loop derived by the Markov-chain analysis in Section 3.3. The results show that the BER decreases faster than exponential as the deadzone width increases. This is because the loop with wider deadzone may hold the ideal phase rejecting the random jitter, once the lock is acquired. As the ideal phase has the largest steady-state probability, the steady-state distribution gets narrower when the deadzone width increases.

However, when there is non-zero frequency offset, or the ideal selective phase changes in time, a wider deadzone does not always results in the better BER. Fig. 3.10 shows the average phase error and BER measured using the transient simulation described in Section 3.1. In the figure, the width of dead zone is normalized with ϕ_{bb} and the results with $0 \sim 2.5$ (ϕ_{bb}) of deadzone width are plotted. As



(a)



(b)

Figure 3.10: Simulated (a) average of phase error and (b) expected BER of a bang-bang controlled loop. Phase is normalized with the phase adjustment step (ϕ_{bb}).

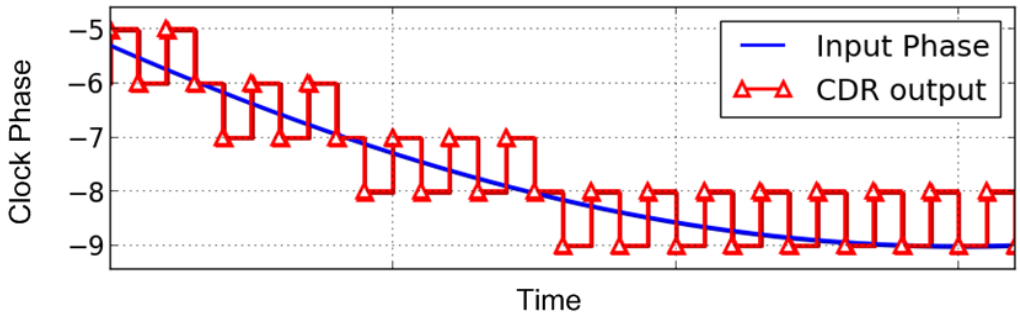
can be seen from the figure, the BER has the minimum value when the dead-zone width is ϕ_{bb}, and increases as the deadzone width deviates from ϕ_{bb}. This result can be explained with the transient simulation waveform plotted in Fig. 3.11. When the deadzone width is too small, the probability of phase change increases even when the current output phase is the best selectable one. In extreme case, if there is no deadzone, the PD becomes a binary one, and the dithering of the loop degrades the performance. On the other hand, when the deadzone is too wide, tracking performance is degraded and the resulting phase offset between the input and output increases the BER.

It is important to note that the BER is minimized when the deadzone width is same with ϕ_{bb}. This is because the 3× phase detector checks whether the ideal phase lies in the interval where the selectable gives the minimum phase error or not. This characteristic will be reexamined and extensively used in Chapter 4.

Meanwhile, the decimation technique explained in Section 3.4.3 can be applied at the same time with the 3× oversampling. Both of them can act together to reduce the uncertainty of the random distributed input phase.

Fig. 3.12 (a) shows the expected BER with various deadzone widths and decimation depths derived from Markov-chain analysis. In this analysis the transition density was assumed to be 100%. As expected, wider deadzone width and longer decimation length results in lower BER.

With non-100% transition density, it is interesting to see that the same number of transitions in a decimation results in constant BER divided by the transition density as shown in Fig. 3.12 (b). For example, the case with 100% of transition density and 20 bits of decimation depth gives the same results with the one with



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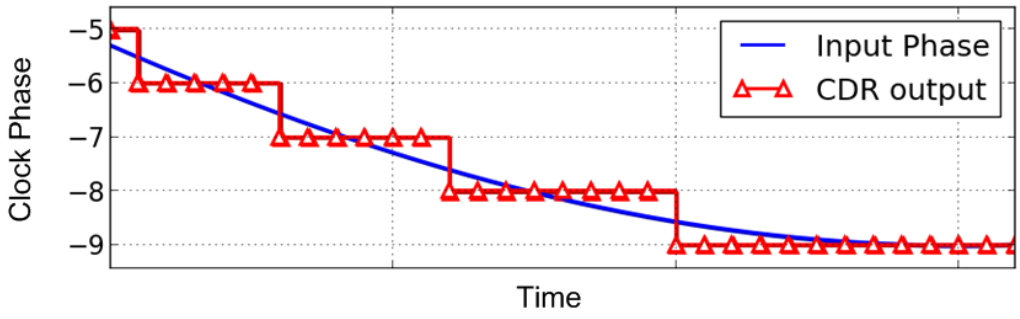

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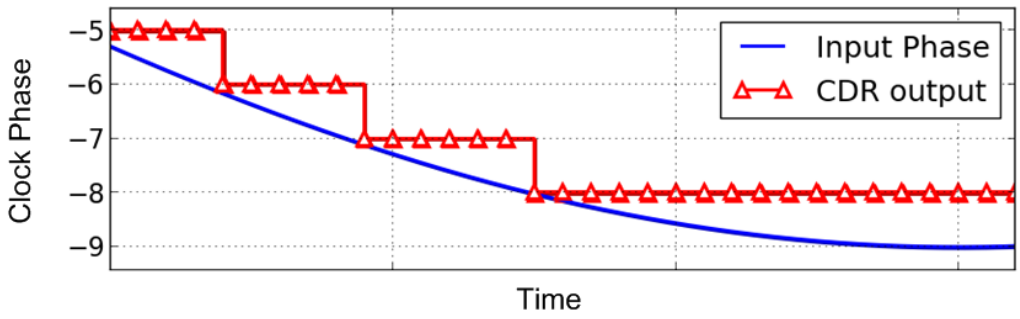
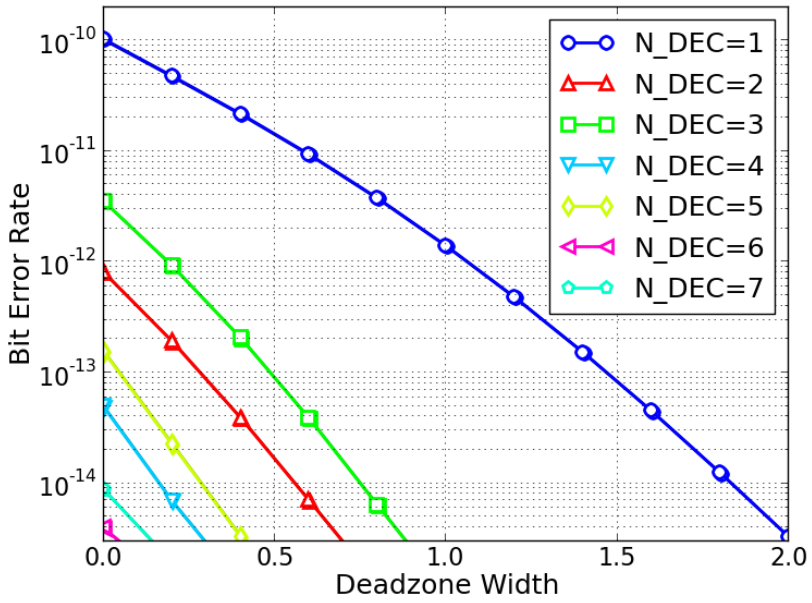


(c)

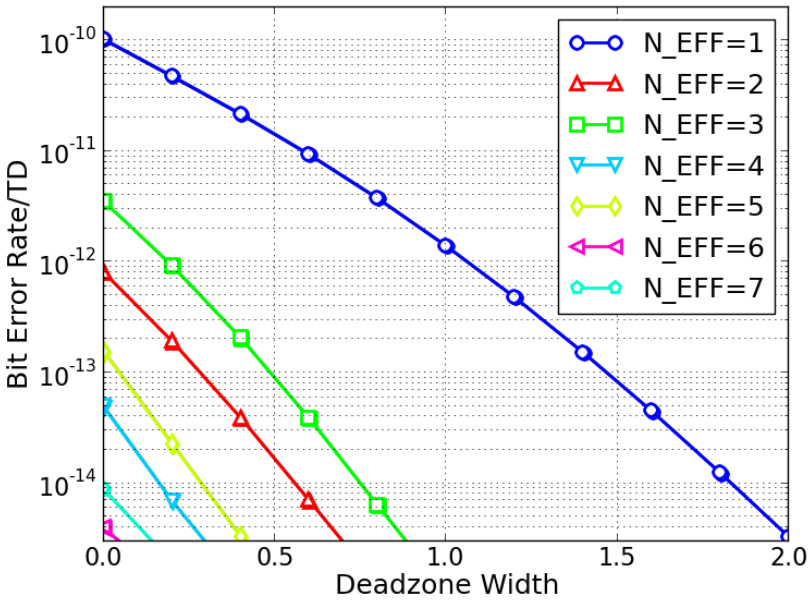
Figure 3.11: Transient response of 3× oversampling timing loop to sinuoidal input phase where W_{DZ}=0, 1.0, and 2.0 (ϕ_{bb}).

50% of transition density and 10 bits of decimation depth. It implies that N_{EFF}, the multiplication of the transition density and the decimation depth, decides the distribution of phase error. That is, the distribution and confidence level of phase error is decided by N_{EFF}.

This is an important characteristic to implement a decimation circuit that assures stable confidence level independent of the transition density. When the input has sparse transitions, the decimation depth must be increased to maintin constant confidence level or BER. An implementation of decimating loop filter that adjusts the decimation depth according to the transition density will be introduced in Chapter 4.



(a)



(b)

Figure 3.12: BER with various deadzone widths and decimation depths. (a) assumes 100% of transition density while (b) is measred with various N_{EFF}.

Chapter 4
Design of Ditherless Clock and Data Recovery Circuit

Dithering in bang-bang controlled CDRs poses conflicting requirements on the phase adjustment resolution as one tries to maximize the tracking bandwidth and minimize jitter. This chapter introduces an optimal phase interval detection scheme, that can retain the advantages of BB-PDs while avoiding the limitations due to dithering. Eliminating dithering in bang-bang CDRs greatly relaxes the requirement on the phase step resolution and save power dissipation. In our prototype phase-interpolator based CDR, a 41-mUI_{pp} jitter was achievable with a coarse phase adjustment step of 0.11-UI and only 1-mW dissipated in the phase interpolator stages. The improved trade-offs between the tracking bandwidth and jitter is demonstrated by the CDR's jitter tolerance characteristics (JTOL), measured by a digitally-controlled in-situ testing circuit.

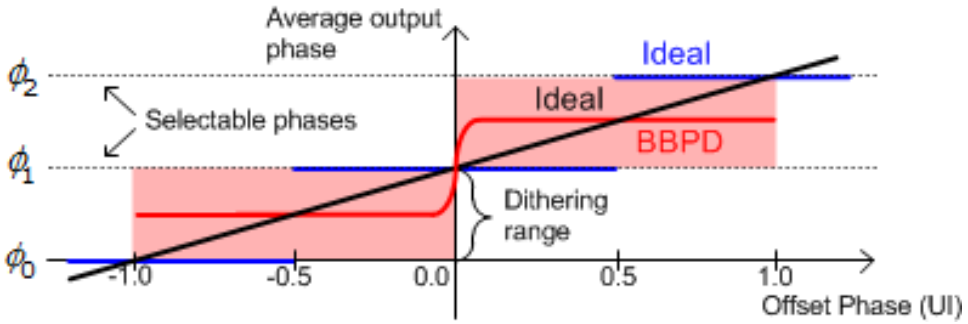
4.1 Optimal Phase Detection

Typical bang-bang controlled CDRs exhibit dithering, and the dithering has adverse effects on the CDR's performance as explained in Chapter 1. For example, it degrades the sampling timing margin and poses the trade-off between the tracking bandwidth and jitter. A fine phase step is helpful to minimize the dithering, but it requires circuits with finer resolution that consumes large power and area. In

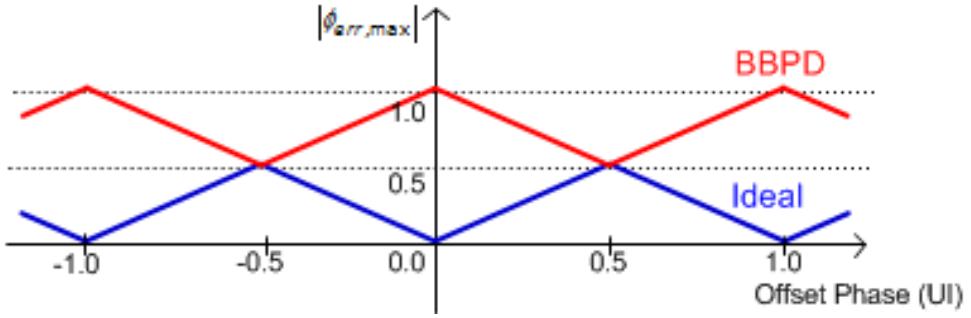
addition, fine resolution also requires narrower confidence interval for prudent decision, which needs decimation for longer period. This longer decimation weakens the tracking performance of the CDR along with the small phase adjustment step. In this background, this section introduces an optimal phase detection technique that can minimize the effect of dithering without requiring fine phase resolution.

Before explaining the optimal phase detection, let's find the cause of dithering in BBPDs to help the understanding of the proposed technique. CDRs with BB-PDs exhibit dithering because the phase detector compares the clock's phase with a single reference point, i.e., the optimal locking point. A problem is that compared to this single reference point, the clock phase is never correct; it is either too early or too late. While linear phase detectors detects and corrects the amount of phase error to drive the loop to the locking point, BBPDs adjusts the output phase with a fixed amount regardless of the phase error. Therefore, in response to such BB-PD outputs providing only the polarity information of the phase error, the clock phase has to be changed every time and in fixed steps, resulting in dithering.

For CDRs that adjust the clock phase in quantized steps, e.g. the phase-interpolator based DLLs [2] or blind oversampling CDRs [26], such dithering results in the phase errors larger than the minimum possible, i.e. a half of the step size. Fig. 4.1 compares the bang-bang phase detection and optimal phase detection for various phase offsets between the ideal phase and selectable phases. When the optimal phase is always selected, the maximum phase error can be kept less than 0.5 phase step. On the contrary, the clock phase of bang-bang controlled loop still dithers even when the lock point is very close to one of the selectable phases, and the maximum phase error can be as large as a phase step. For example, when the



(a)



(b)

Figure 4.1: Comparison of BBPD and optimal phase detection in (a) output phase and (b) maximum phase error.

offset phase is slightly larger than 0 in Fig. 4.1 (a), optimum selectable phase is ϕ_1, but the bang-bang controlled loop toggles between ϕ_1 and ϕ_2. Fig. 4.2 compares the output phases of such an optimal CDR and a bang-bang CDR for the case with a sinusoidal input phase. It can be seen that the output phase of the optimal CDR is always within one half of the phase step from the input and changes only in the direction of the input change while BBPD has one full UI of phase error at maximum and its output phase repeatedly goes in the opposite direction of the input phase.

Such an optimal CDR can be realized with a phase interval detector (PID), which looks for the phase interval that encloses the desired lock point, rather than looking for a non-existent, selectable phase that is exactly equal to the lock point. Once

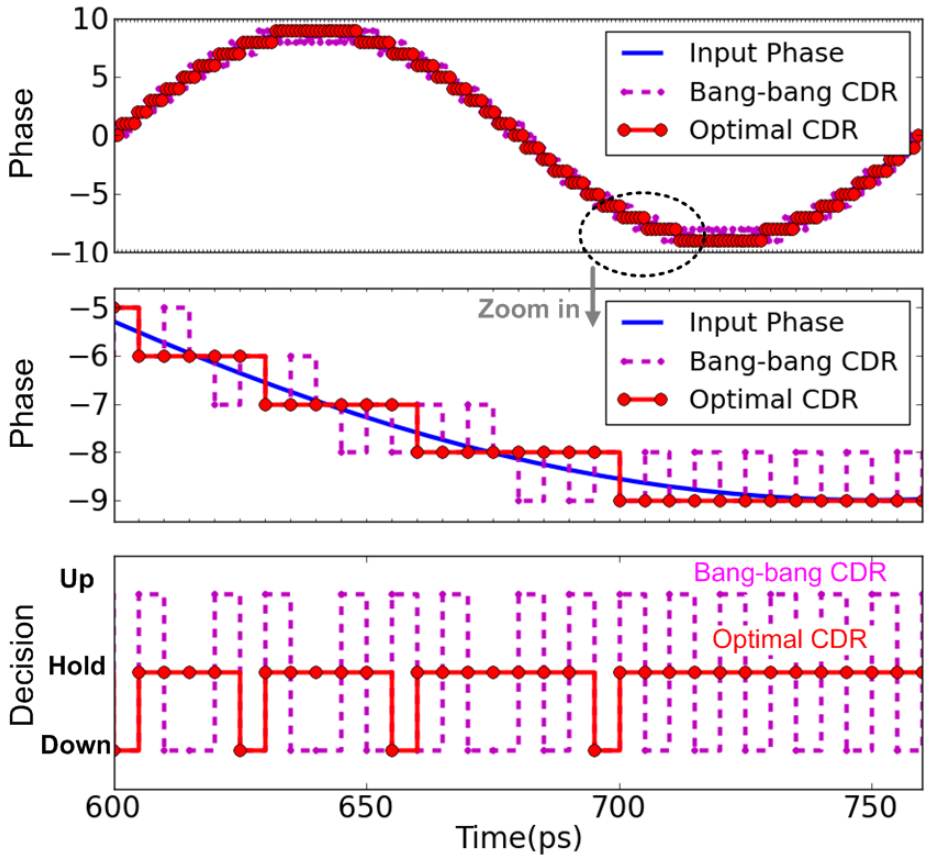


Figure 4.2: Response of bang-bang controlled system without loop delay to sinusoidal input phase and its comparison with the optimal phase.

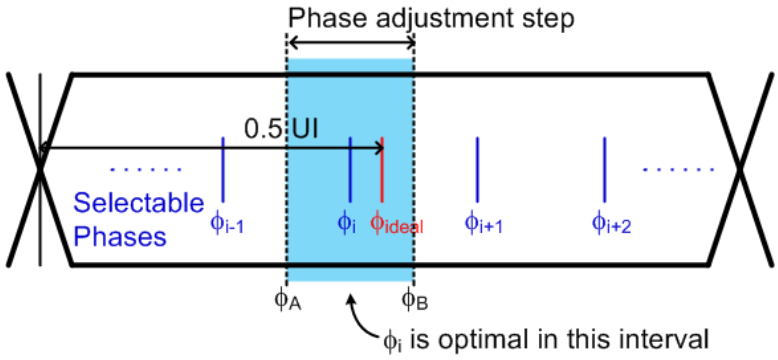


Figure 4.3: Optimal phase selection with phase interval detection technique.

the optimal phase interval is found, then the best selectable phase that minimizes the quantization error is at the mid-point of the interval. With this phase interval detector, the CDR can always select the optimal phase and need not dither.

The proposed phase interval detection is for CDRs that adjusts the phase in quantized steps, or equivalently, that select one from a set of a finite number of available phases [2, 26, 27]. It aims to select the phase that is closest to the desired lock point and thus minimizes the phase quantization error.

The phase interval detection is basically performed by a pair of bang-bang phase detectors, each sampling at the mid-point between the current phase (ϕ_i) and one of its adjacent phases (ϕ_{i-1} or ϕ_{i+1}), as depicted in Fig. 4.3. If the desired lock point is located later than the earlier sampling phase (ϕ_A) and earlier than the later sampling phase (ϕ_B), it can be deduced that the lock point is within the interval spanned by the two sampling points. Then, the selectable phase (ϕ_i) which is at the middle of the interval is the optimal phase that minimizes the error.

With an odd number of selectable phases spanning one unit-interval (UI), those sampling phases (ϕ_A and ϕ_B) need not be generated separately, as illustrated in Fig. 4.4 for the case with 9 phases. To measure timing, the BB-PDs sample at the

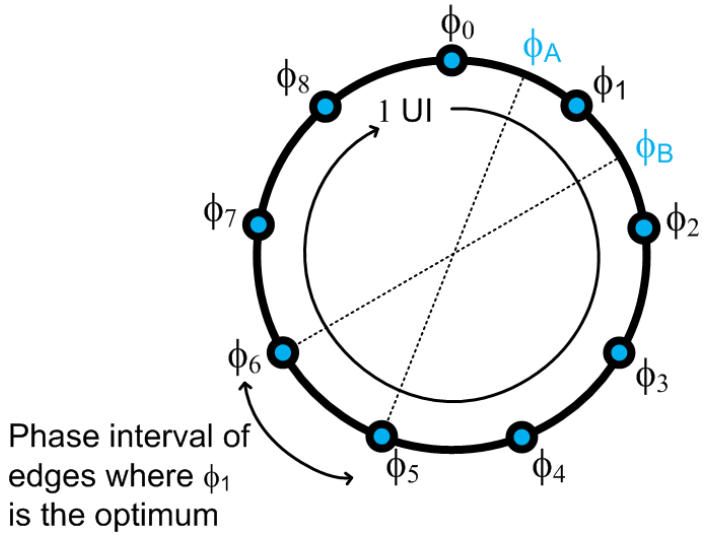


Figure 4.4: Phase relationship of phase interval detection.

vicinity of the data transition edge, which is nominally 0.5-UI spaced from the data sampling position. With an odd number of phases, the 0.5-UI shifted versions of ϕ_A and ϕ_B coincide with the available phases, in this case, ϕ_5 and ϕ_6, respectively. If the data sampling phase is not a half UI spaced from the data transition edge, the number of phases does not need to be odd. For example, [31] intentionally shifts the sampling point prior to the center of the bit symbol to reduce the pre-cursor of the inter-symbol interference. In this case, the number of selectable phase can be chosen freely.

The implementation of the proposed technique is basically same with the 3x oversampling phase detectors where the deadzone width is a half of phase step. It has been already shown in Chapter 3 that the optimal width of deadzone that generates the least bit-error is a half of the phase step. That result matches with the concept of the phase interval detection technique, and assures the strength of the proposed technique.

4.2 Proposed Architecture

A prototype 5-Gb/s CDR with the described phase interval detection is organized as shown in Fig. 4.5. It is basically a phase-interpolator based, infinite-range delay-locked loop (DLL) [2]. A phase-locked loop (PLL) generates a set of 6 phases of 2.5-GHz half-rate clocks and each of the phase interpolating stages can synthesize a phase in-between in 3 steps, providing total of 18 selectable phases over one clock period, or 9 phases over 1-UI. Each receiver slice in this half-rate CDR consists of one data sampler, two edge samplers, and one additional sampler for on-chip eye monitoring and margin measurements (described later). With two slices, the CDR has total of 8 samplers and 4 differential phase interpolating stages.

Note that the phase resolution of the CDR is considerably low at 9 phases per UI, compared to 64 128 phases/UI in most other implementations [2, 28]. Such a coarse resolution is possible because the proposed phase interval detector eliminates dithering. With the minimum device width dictated by the design rules and linearity/mismatch requirements, the power and area of a phase interpolator increase super-linearly with the number of interpolation steps [28]. Therefore, the coarse phase resolution of our CDR is expected to bring 4∼6 times reduction in both the power and area consumption in the phase interpolators. Also, the coarse phase step is advantageous in improving the tracking bandwidth of the CDR. In other words, eliminating dithering in digitally-controlled CDRs can greatly alleviate the trade-off between the jitter and tracking bandwidth, enabling designers to improve one without degrading the other.

However, with a coarse phase step, the penalty of making a wrong move is high and each phase adjustment must be made prudently. To reduce the sensitivity

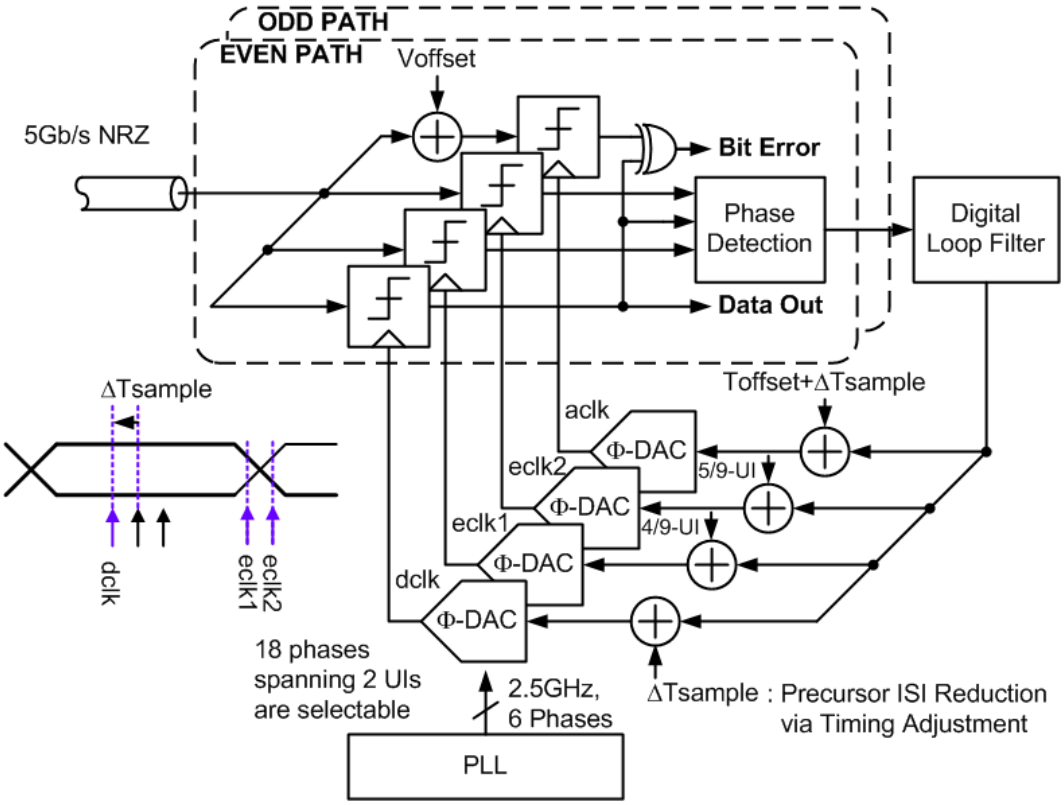


Figure 4.5: Overall architecture of the prototype CDR with phase interval detector (PID).

to noises as well as to loop latency effects [5], the timing error decision is made only after collecting sufficient distribution information of the PD output samples. For each data transition, the set of two BB-PDs provides one of three possible outputs indicating: both of the sampling phases (ϕ_A and ϕ_B) being late (UP), both being early (DOWN), and one being late and the other being early (HOLD). The occurrences of each output value are individually counted until one of the occurrence counts reaches 16 (either the count in one of the slices reaching 16 or those in both slices reaching 8).

Once the sufficient counts of UP, DOWN, and HOLD incidents are collected, the digital loop filter finally makes a decision and adjusts the sampling phase based on the accumulated counts (N_{UP}, N_{DN}, and N_{HD}, respectively). The decision algorithm for the phase adjustment is slightly different from the conventional majority voting algorithm. Comparing with the majority voting algorithm that finds the most possible candidate, the proposed algorithm checks whether the change of output phase would reduce the sampling timing error or not. For example, let's assume that the the counted information tells $N_{UP} = 4$, $N_{HD} = 4$ and $N_{DN} = 7$. Even though the DN has the most votes, the decision must be 'HD'. If the loop filter decides DN and lags the sampling clock phase, the next decision will be UP and return to the previous state because the counted N_{UP} will be 8 while N_{HD} is less than 7. In this reason, the CDR advances the phase to an earlier position when more than half of the outputs are UP's ($N_{UP} > N_{HD} + N_{DN}$). Likewise, if the majority of the outputs are DOWN's ($N_{DN} > N_{HD}+N_{UP}$), the CDR moves the phase to a later position. On the other hand, if none of the above conditions is true, the current phase position is considered the optimum and no adjustment is made.

It should be noted that a similar phase detection scheme was reported for bang-bang controlled PLLs [4, 29] but did not possess the advantages described in this thesis. The key distinction stems from the fact that bang-bang PLLs adjust the frequency in quantized steps, not the phase. With a deadzone introduced by a pair of BB-PDs, any drift in phase would increase the jitter by at least the dead-zone width. To circumvent this, the deadzone had to be made narrower than the width of the underlying jitter distribution [29], or adjustable [4]. Hence, the required phase resolution was still high. On the other hand, the proposed phase interval detector can eliminate dithering without any penalty in jitter due to phase drifting and coarse phase steps.

Also, one can find some similarities of this CDR with the blind oversampling CDRs using phase picking [26, 27]. Blind oversampling CDRs sample the incoming signal at all available phase positions and find the phase interval that bears the most data transitions within a specified time window. They also typically use an odd number of phases (3 or 5). Despite this similarity, the advantage of our CDR is that the number of phases can be increased without incurring the hardware cost of sampling at all the phases and processing their outputs to make timing decisions.

4.3 Analysis of the CDR with Phase Interval Detection

As stated in previous section, using coarse phase resolutions helps to reduce area and power consumption only if its performance such as jitter and tracking bandwidth satisfies the specification of its application. The target of the prototype CDR is Universal Serial BUS (USB) 3.0 [50], and its jitter tolerance requirement is depicted in Fig. 4.6. It requires the sampling timing margin larger than $0.17UI_{pp}$ or $0.085UI_{peak}$

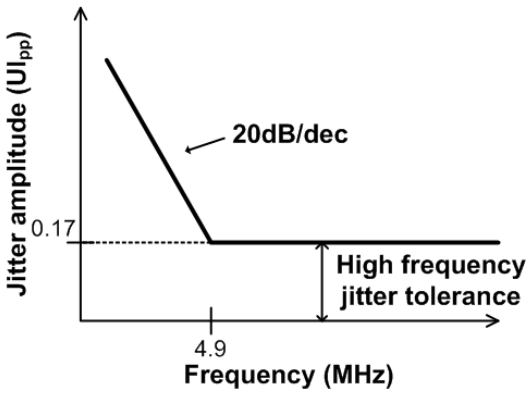


Figure 4.6: Jitter tolerance requirements of USB 3.0.

at $4.9MHz$. Assuming $0.35UI_{pp}$ of deterministic jitter (ϕ_{DJ}) and gaussian random jitter with $0.015UI$ of standard deviation (σ_{RJ}), the timing margin of the proposed CDR satisfying less than 10^{-12} of BER is

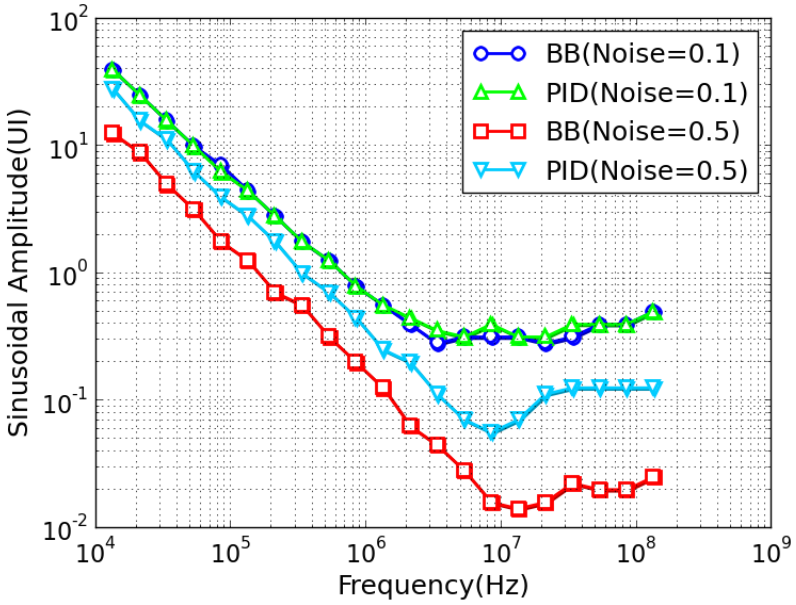
$$TM = 0.5 - \phi_{DJ} - 7\sigma_{RJ} - \phi_{dither}(rad) \tag{4.1}$$

where ϕ_{dither} stands for the maximum phase error due to the dithering. As the proposed phase interval detection technique guarantees less than a half phase adjustment step of phase error, ϕ_{dither} can be expressed as $0.5/N$ where N represents the number of selectable phases in a UI. When N is 9 as is in the prototype CDR, the timing margin is $0.164UI$, about twice of the required timing margin.

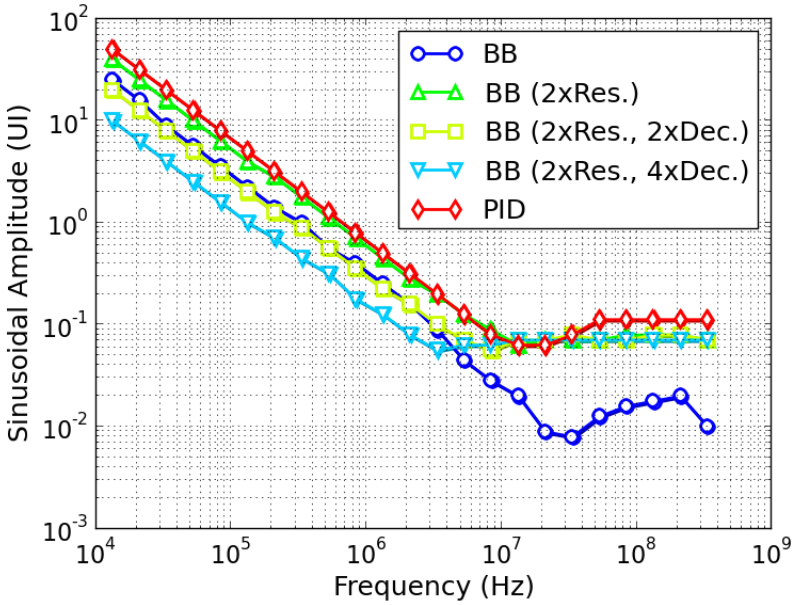
Fig. 4.7 (a) compares the simulated JTOL curves of proposed CDR and conventional bang-bang controlled loop for two different input jitter conditions; $\sigma_{RJ} = 0.1\phi_{bb}$ and $0.5\phi_{bb}$. The BER target is 10^{-12} and the statistical simulation technique described in Section 3.1 was used. Other than the phase detection technique, everything including the decimation depth and input bit stream is same for both circuits. The benefit of proposed technique can be clearly seen when σ_{RJ} is $0.1\phi_{bb}$. The high-

frequency JTOL is at least 4 times lager and the tracking bandwidth is 2∼3 times larger than the conventional one. The improvement of JTOL is larger than $0.5\phi_{bb}$ because the possibility of BBPD's phase change to the opposite direction of the input increases exponentially as the random jitter increases. With the continuously changing input phase, one output change in the opposite direction is critical as the phase error will get bigger by the next phase adjustment time. On the other hand, the benefit is hard to see when the random noise is small. In this case, additional $0.5\phi_{bb}$ of timing margin attained from optimal phase detection does not affect the BER significantly, and the improvement of JTOL is only $0.5\phi_{bb}$ or $0.056UI$ in the figure.

It can be argued that the BBPD with 2× finer phase resolution could show similar performance with the proposed one as the additional phase margin attained by the proposed technique is $0.5\phi_{bb}$, but its performance is actually worse than the proposed one. Firstly, it needs 4× larger area and more than 2× larger power consumption. Next, 2× finer phase resolution requires 2× narrower confidence interval, which needs 4× longer decimation length. 2× finer phase resolution and 4× longer decimation length will result in 8× slower tracking bandwidth barring other effects such as dither reduction due to finer phase resolution. Fig. 4.7 (b) compares the JTOL of the proposed CDR and the conventional BBPD-based CDRs with various decimation lengths and phase resolutions. Even though the conventional BBPD-based CDR consumes larger area and power, its performance is worse than the proposed one due to the inferior confidence level of the decision. The conventional one with 2× finer phase resolution and 4× longer decimation length shows better performance around $10MHz$, but it definitely has slower tracking bandwidth.

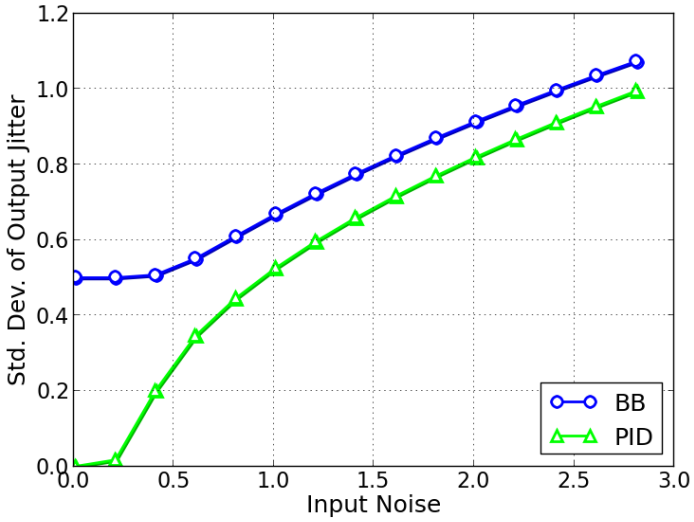


(a)

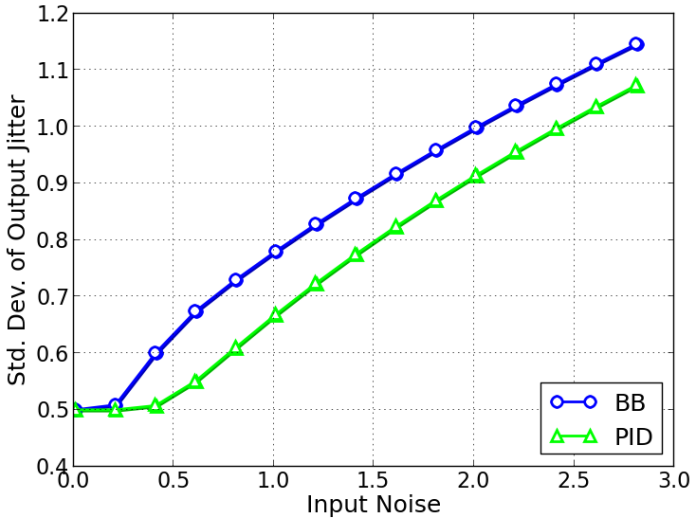


(b)

Figure 4.7: Simulated jitter tolerance comparing BBPD and PID with (a) different noise conditions, (b) various decimation lengths and phase resolutions. The 'Noise' in the figure represents the standard deviation of the input jitter in ϕ_{bb} unit.



(a)



(b)

Figure 4.8: Simulated output jitter vs. input jitter for BBPD and PID (a) when the ideal phase coincides with a selectable phase and (b) when the ideal phase is at the middle of two adjacent selectable phases. The phases are normalized with the phase adjustment step (ϕ_{bb}).

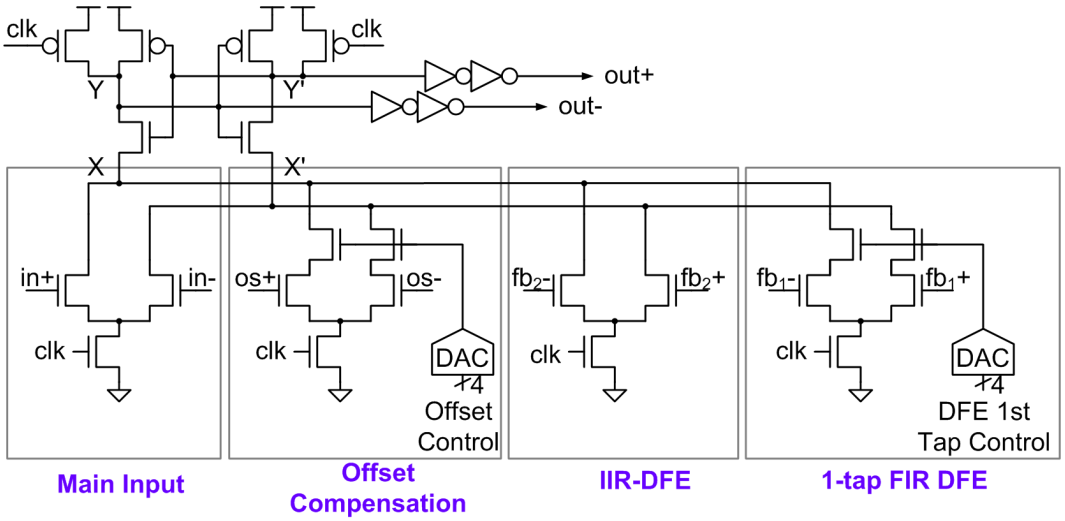


Figure 4.9: The sampling receiver with signal summation and offset calibration capability.

The proposed CDR also has superior jitter performance comparing with the conventional one. Fig. 4.8 shows the steady-state output jitter for various input jitter conditions derived using the Markov-chain analysis described in Section 3.3. For the complete analysis, two extreme cases, when the phase offset between the ideal phase and the selectable phase is 0 or $0.5\phi_{bb}$, are tested. As expected, the proposed CDR keeps the output jitter less than $0.5\phi_{bb}$ while the conventional one generates $0.5\phi_{bb}$ $1.0\phi_{bb}$ of output jitter under small input jitter conditions. The output jitters of both circuits increase along with the increase of input jitter, but the proposed one always generates less jitter comparing with the conventional one.

4.4 Circuit Implementation

4.4.1 Sampling Receiver

Fig. 4.9 shows the circuit schematic of the regenerative latch that also performs signal summation without dissipating static current. The circuit is basically a StrongARM

latch with multiple input pairs connected in parallel. There are four input pairs. First, the main input pair (in+, in-) samples the incoming data signal. Second, the first feedback input pair (fb1+, fb1-) receives the data output of the alternative-phase regenerative latch and subtracts it from the incoming signal to cancel the first post-cursor ISI, realizing a 1-tap direct-feedback FIR DFE. Third, the second feedback input pair (fb2+, fb2-) receives the output of the shared single-pole IIR DFE filter and subtracts it to cancel the trailing post-cursor ISIs. Lastly, the final input pair (os+, os-) receives a binary signal that determines the polarity of the offset voltage to be compensated. Since the input pairs of (fb1+, fb1-) and (os+, os-) receive the binary signals from the other regenerative latch and external digital control, respectively, their analog weights are adjusted by the gate bias voltages of the current-starving devices, connected in series with the input pair devices. These gate bias voltages are digitally controlled via 4-bit resistor-ladder digital-to-analog converters (DACs).

When the clock (clk) rises, the current steered by each of the input pairs according to its respective differential input discharges the internal nodes (X and X') of the comparator. The individual currents from the input pairs are linearly added and hence the comparator makes the final decision based on the sum of the input differences. Therefore, the signal summation can be done at much lower costs in power and speed than the current-mode summation stage in Fig. 4.9.

It is noteworthy that even though the parallel input pairs increase the capacitance (C) on the internal nodes X/X', the total discharging current (I) also increases, keeping the sampling aperture of the comparator roughly the same. In addition, the regeneration bandwidth and power dissipation are largely determined by the

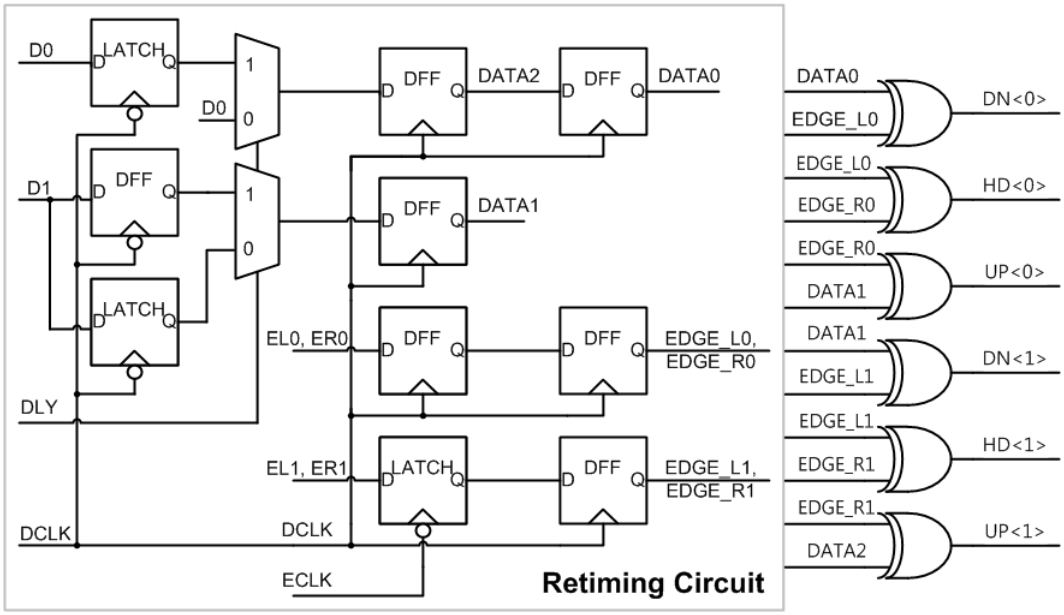


Figure 4.10: A half-rate phase interval detector with retiming circuit.

capacitance on the nodes Y/Y', which is weakly dependent on the number of input pairs [47].

4.4.2 Phase Detector

Phase detector investigates the oversampled data to find the interval where the input data has the transition. Fig. 4.10 shows a half-rate phase interval detector of the proposed CDR. In includes a retiming circuit prior to the XOR gates that compares the sampled values. As the sampled data have different sampling timings, they need to be aligned before comparison. For example, even-phase edge samples ($EDGE_{L0}$ and $EDGE_{R0}$) are re-sampled with $DCLK$ for twice, which leads to about 1.75 cycles of delay.

This phase detector needs more than one bit duration of timing adjustment capability for the equalization. The prototype CDR is used for a low-power decision-

feedback equalizing (DFE) receiver front-end [35]. The receiver achieves a high energy efficiency by the combination of a direct-feedback finite-impulse-response (FIR) DFE, an infinite-impulse-response (IIR) DFE, and a clock-and-data recovery (CDR) circuit with adjustable timing offsets as shown in Fig. 4.11. In this receiver the timing-critical first post-cursor ISI tap is cancelled by a direct-feedback finite-impulse-response (FIR) DFE, and an infinite-impulse-response (IIR) filter is utilized to subtract the remaining post-cursor ISIs. The pre-cursor ISIs are suppressed by passive inductors added in series with the termination resistors and by shifting the data sampling phase from its nominal position, removing the CTLE and limiting amplifier stages. To achieve this, the prototype CDR has the capability of shifting the data sampling timing according to the digital control bits.

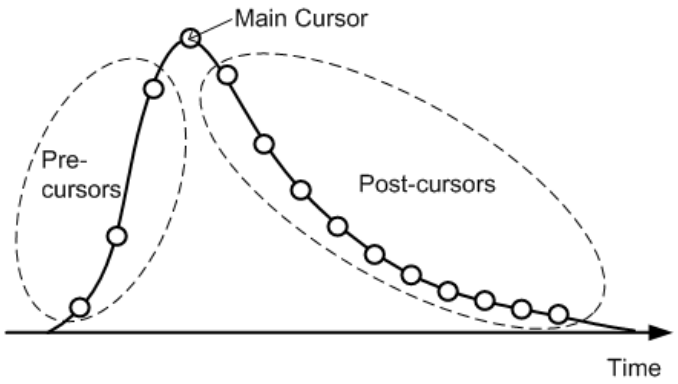
The long timing gap between the shifted data sample and edge samples are aligned by changing the delay of data samples appropriately according to the 'dly' signal. When the equalizer changes the data sampling timing to reduce the pre-cursor, the data samples are generated earlier than the normal case. As can be seen from Fig. 4.12 (a), the timing margin of the flip-flop for normal operation (dly=0) is

$$T_{MARGIN} = T_{CQ} - T_{HOLD}. \tag{4.2}$$

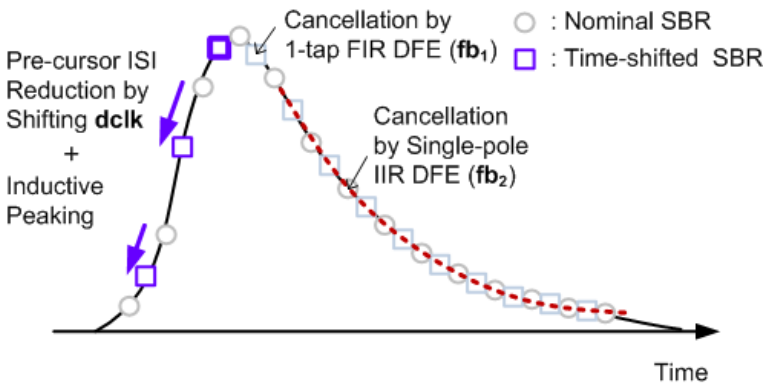
where T_{CQ} and T_{HOLD} represents the clock-to-Q delay and hold timie of the flip-flop.

On the other hand, when dly=1, the timing margin described in Eq. (4.2) becomes negative as shown in Fig. 4.12 (b). To resolve this timing issue, data samples are delayed by additional a half UI, and the timing margin becomes

$$T_{MARGIN} = 0.5T_{ref} + T_{CQ} - T_{HOLD} - \Delta T_{sample}. \tag{4.3}$$

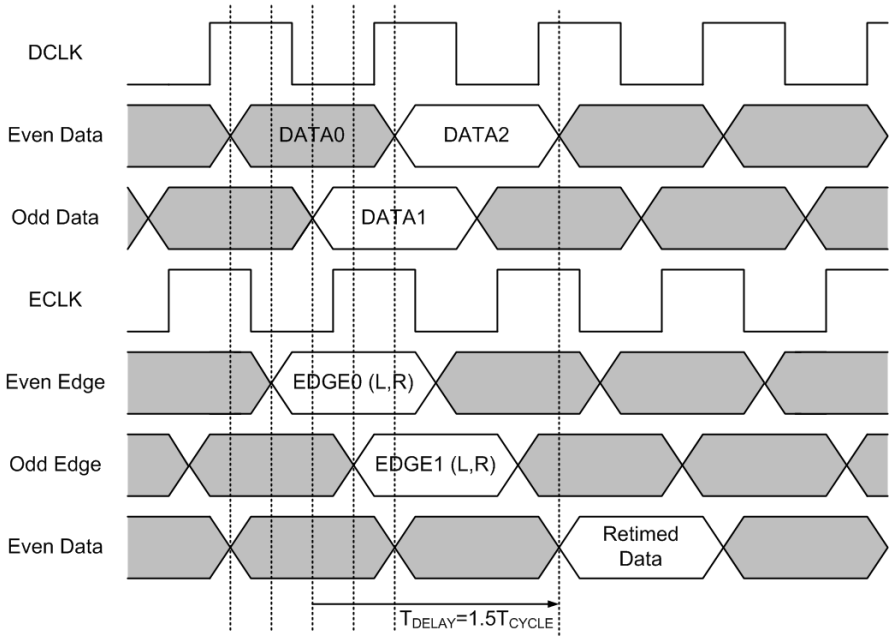


(a)

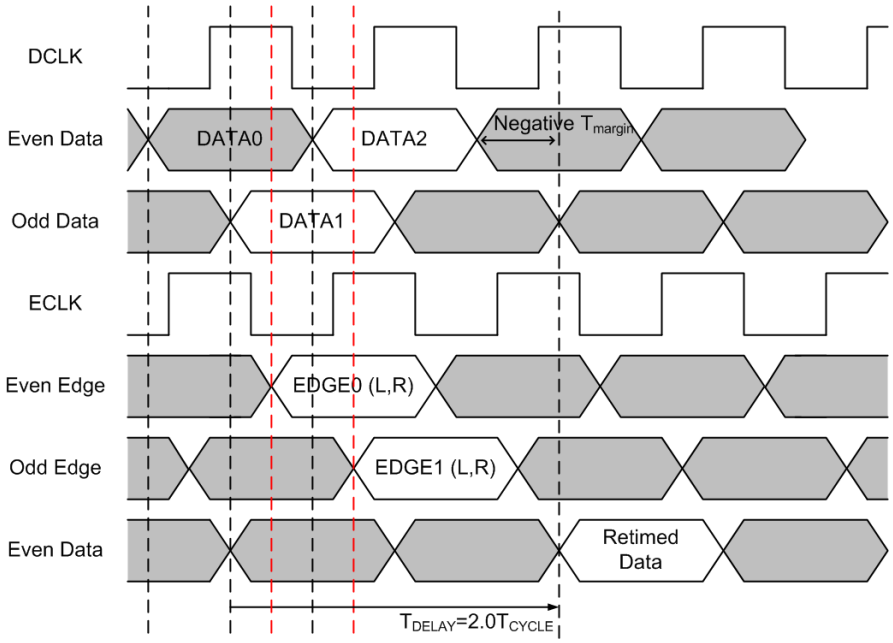


(b)

Figure 4.11: Equalization technique applied to the prototype system.



(a)



(b)

Figure 4.12: Timing diagram of phase interval detector's operation when (a) dly=L and (b) dly=H.

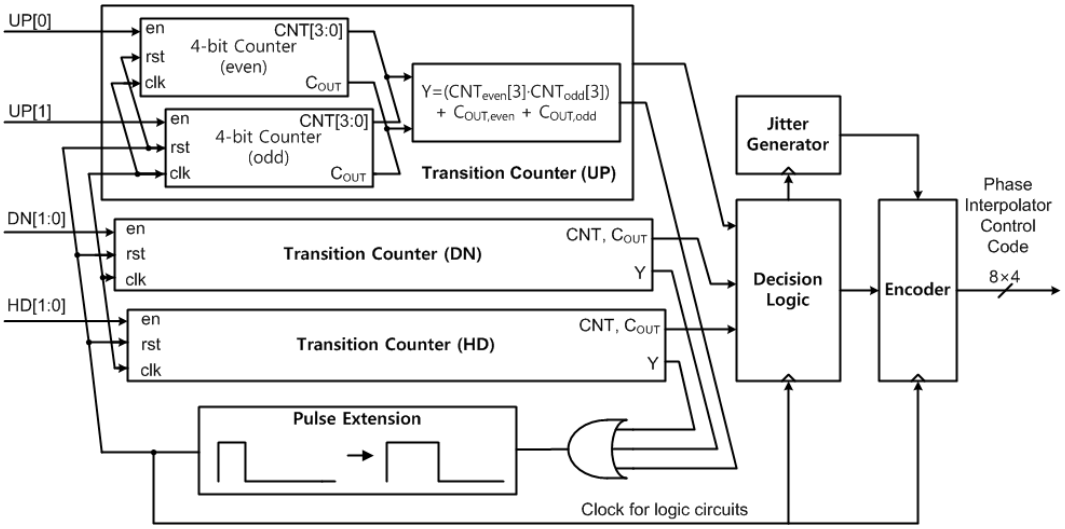


Figure 4.13: Block diagram of the digital loop filter.

where T_{sample} is the amount of data sampling timing shift caused by the equalizer.

4.4.3 Digital Loop Filter

A digital loop filter following the phase detector decides the phase direction and generates appropriate control code for the phase interpolators. It consists of transition counters, decision logic, jitter generator and an encoder as described in Fig. 4.13. When the transition counter counts sufficient number of transition edges, the rising edge of CLK_{DLF} is asserted, and the decision logic compares the counted UP, DN and HD to make the decision. The digital loop filter includes a jitter generator that is used for the on-chip jitter tolerance measurement where it adds intentional phase error to stress the loop. The encoder combines the outputs of the decision logic and the jitter generator, and controls 8-bit codes for each of the 4 phase interpolators that sample data center, two edges, and eye monitoring position, respectively.

The transition counter ensures the confident decision by adjusting the interval of

phase control change. It asserts the rising edge of CLK_{DLF} when one of the number of UP, DN or HD reaches more than 16 samples. As discussed in 3.4.3, decimation reduces the effective amount of random noise and ensures prudent decision. For the simplicity of the implementation, a set of 4-bit counters count BBPD's even-phase output and odd-phase output separately. The number of samples are considered to be sufficient when one of the counter output exceeds 16 or both even and odd phase output exceeds 8. When sufficient information is collected, that is when the output of the transition counter asserts carry out, decision is made and appropriate control bits are generated. For the operation of the digital loop filter, a clock signal with a fixed frequency is unnecessary, because the carry out signal is used as the clock for the following logic blocks. As the duty of the carry out bit can be too narrow for the fully synthesized logic blocks, a pulse extension block ensures at least $8T_{ref}$ of high duration for CLK_{DLF}.

Proposed decimation technique based on sufficient information helps to ensure robust operation over change of transition density. Fig. 4.14 shows the jitter histograms of a conventional CDR that has a fixed decimation frequency experiencing two different transition densities. When the transition density drops from 100% to 25%, the effective information in a decimation period gets sparse and the confidence level gets worse. Therefore, it can be clearly seen that the case with 25% of transition density generates larger jitter comparing with the one with 100% of transition density. On the contrary, the proposed decimation technique collects a fixed number of *effective* information before making a decision. Namely, it makes decision with a fixed number of transition edges. As it counts the phase detections made upon each transition edge, the decimation period of the prototype CDR is

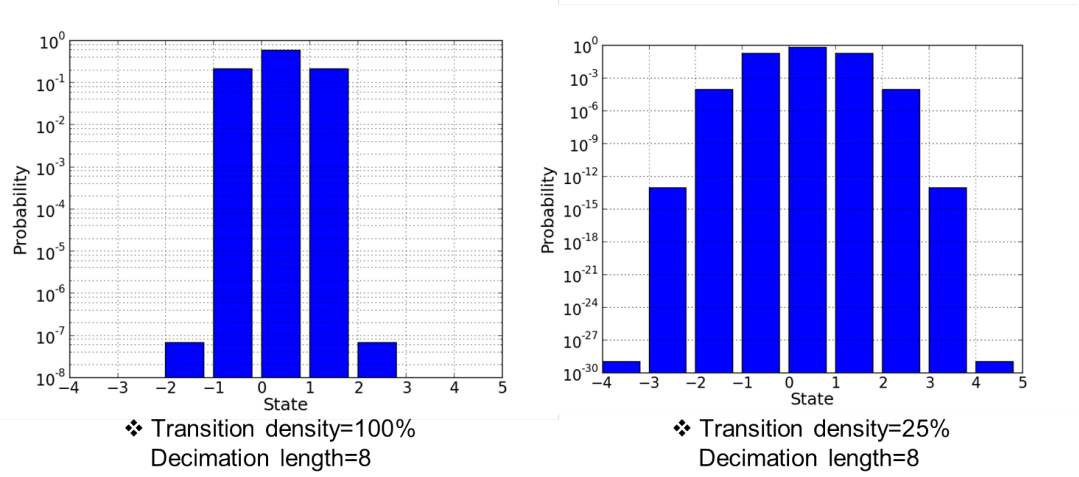


Figure 4.14: Jitter histogram of conventional CDR's output with transition density of 100% and 30%.

automatically adjusted according to the transition density of the input. As can be seen from Fig. 4.15, the proposed CDR shows constant output jitter regardless of the transition density of the input.

On the other hand, the CDR includes a digital jitter generator to inject the ramp or step jitter on the recovered clock phase for the in-situ JTOL measurement. The ramping phase is generated by adding a periodic step signal to the digital loop filter output. For instance, the jitter generator applies a step change of ϕ_{STEP} to the digital loop filter output every N cycles of the controller clock. As a result, the phase detector (PD) will experience a linear-ramping feedback clock phase of which slope is equal to

$$\frac{\Delta\phi_{ERR}}{\Delta t} = \frac{\phi_{STEP}}{NT_{CTRL}} \tag{4.4}$$

where T_{CTRL} and ϕ_{STEP} are the period of the controller clock and the minimum phase resolution of the phase interpolator, respectively. In this implementation, the magnitude of each injection is fixed at the unit phase adjustment step size of

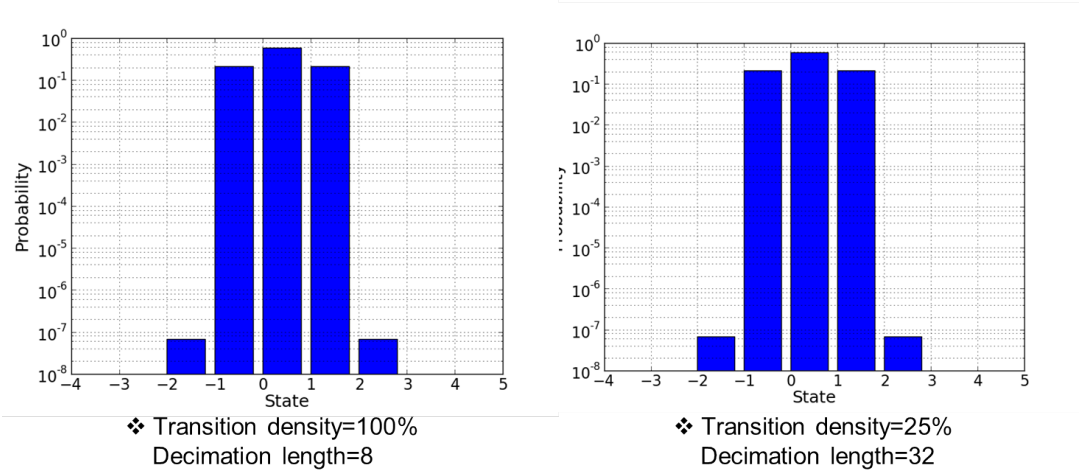


Figure 4.15: Jitter histogram of proposed CDR's output with transition density of 90% and 30%.

the phase interpolator, ϕ_{bb}, and the effective tracking bandwidth is set by the time interval of the phase injection, N. Detailed measurement steps will be explained later in 4.5.

4.4.4 Phase Locked-Loop

For the clock generation, the prototype system includes a type-II integer-N PLL that generates 2.5GH 6 clock phases from 125MHz clock. It consists of PFD, charge pump, capacitive loop filter, voltage regulated ring VCO and a frequency divider as shown in Fig. 4.16. PFD converts the frequency and phase error to the width of its output pulse, and the charge pump charges or discharges the loop filter according to the PFD output. The capacitive loop filter consists of three capacitors where two small capacitors connected by a cross switch serve as a proportional path while a large capacitor works as an integral path. The proportional path similar with the one introduced in [48] is reset every reference cycle by flipping one of the two small

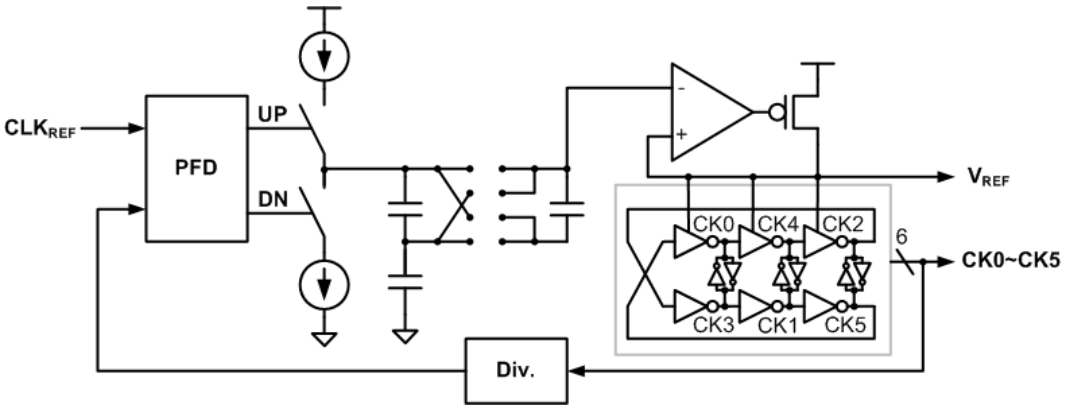


Figure 4.16: The 6-phase frequency synthesizing phase locked loop used for the prototype CDR.

capacitors. Therefore, the effective resistance becomes

$$R_{eff} = \frac{T_{ref}}{C}. \tag{4.5}$$

As the effective resistance changes in proportion to T_{ref}, the loop bandwidth is adaptively scaled with the input frequency [7]. Lastly, the supply regulated ring oscillator generates 6 clock phases that are used for the interpolators to achieve 1/9 UI of phase resolution. The regulator includes the feed-forward path that increases the power supply noise rejection bandwidth [49]. The reglated voltage (V_{REF}) is also forwarded to the phase interpolator to improve the linearity of the phase interpolator.

4.4.5 Phase Interpolator

Fig. 4.17 illustrates the circuit implementation of the phase interpolator stage. Among 6 clock phases generated from the PLL a pair of muxes select two adjacent clock phases. The selected clock phases are buffered by 6 tri-state buffers where their outputs are shorted to interpolate between two adjacent phases in 3-step resolution. The minimum-size inverters are always on while two sets of two 2x sized inverters

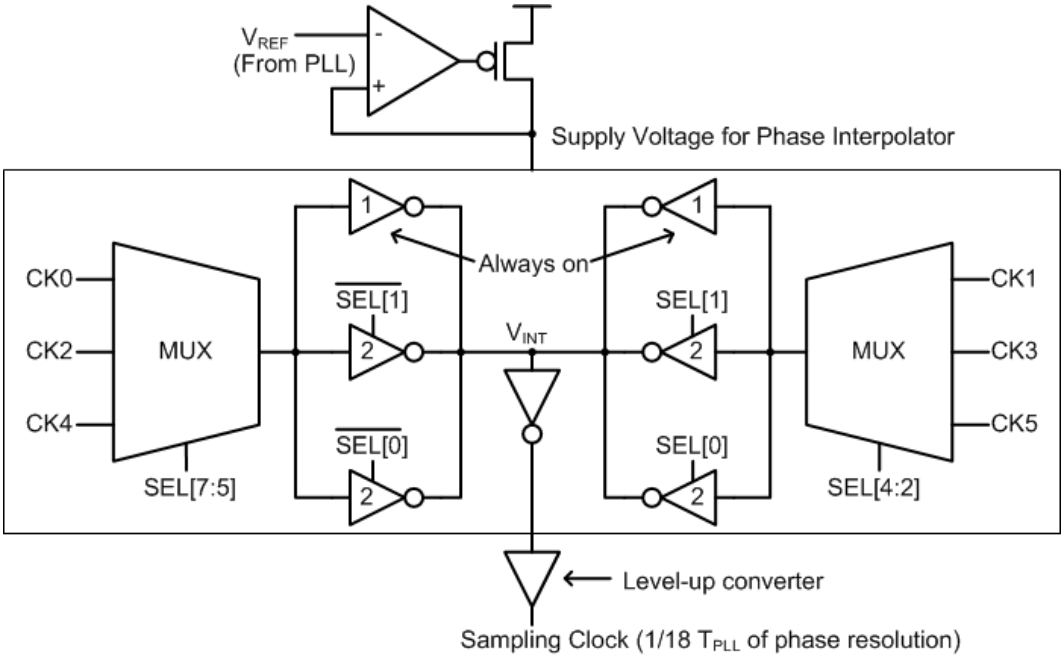


Figure 4.17: 3x interpolating phase interpolator.

are turned on and off complementarily. Therefore the possible interpolation weights are 1/6, 3/6, and 5/6 with no redundancy between the control codes [30]. Fig. 4.18 describes the operation of the phase interpolator. When SEL[1:0]=00, all the inverters in the CK0 braches are turned on while only one inverer is turned on in the CK1 branch, and the shorted inverter output crosses the threshold at 1/6 of those two clock phases. On the other hand, when SEL[1:0]=01, both braches have equal number of inverters turned on, and the interpolation weight becomes 3/6.

Comparing with the conventional phase interpolators that have redundant phases when one clock phase has the full weight, it simplifies the control code. For example, when there is no always-turned on inverer, the code that gives the full strength to the right branch results in the same output phase regardless of the left branch's mux output. Therefore, the control code needs to skip these redundant codes. Moreover,

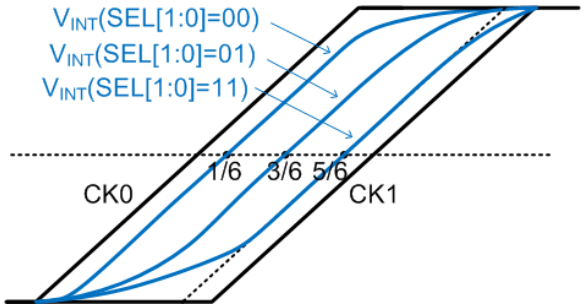


Figure 4.18: Timing diagram of phase interval interpolator's operation.

the skipping of redundant codes needs simultaneous change of mux and inverters. As it can't be done at a perfect timing, it can result in glitches or loss of one clock edge. The proposed phase interpolator does not have this problem as it changes only one of the inverters or the muxes at each code transition.

To maintain good phase linearity of the interpolators across a wide frequency range and PVT conditions, the supply voltage of the tri-state buffers is regulated to the same voltage as that of the inverter-based ring oscillator (V_{REF}). The phase linearity of this type of phase interpolators are sensitive to the PVT variations because it cannot interpolate the clock phase when there is no overlap between two adjacent clock phases. The regulated supply voltage of the ring VCO is a nice indicator of the PVT variation as the inverter has the same structre with the one inside the phase interpolator. Adjusting the supply voltage of the phase interpolator according to V_{REF} cancelles out the effect of PVT variaion, and helps to maintain nice phase linearity over wide variations.

Fig. 4.19 compares simulated differential nonlinearity (DNL) of interpolators with/without voltage regulation. Without voltage regulation, DNL is as high as 0.5 $\phi_{bb,pp}$ at FF corner. FF corner is the worst condition for the interpolator because

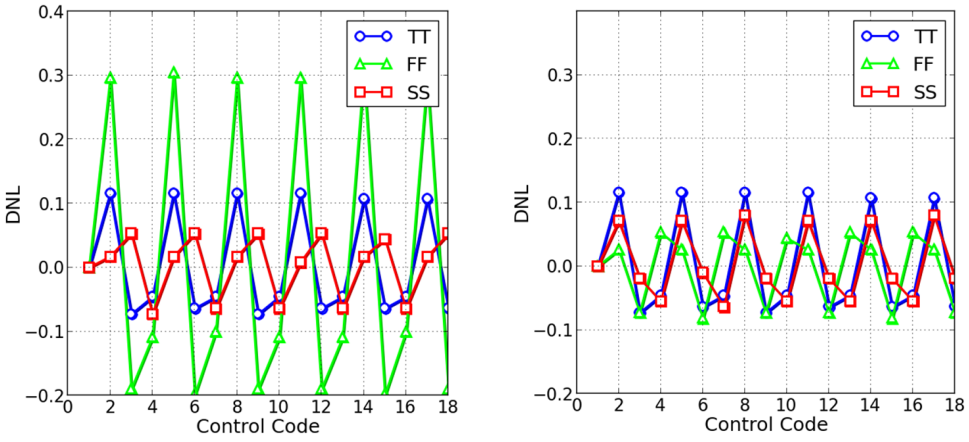


Figure 4.19: Process variation of interpolator's differential nonlinearity (DNL) (a) without voltage regulation and (b) with regulation.

the transitioning edges of internal signals do not overlap in this corner due to its short transition time. The improvement of linearity due to the voltage regulation can be clearly seen in Fig. 4.19 (b) where the maximum DNL is decreased down to 0.2 $\phi_{bb,pp}$.

4.5 Built-In Self-Test Circuit for Jitter Tolerance Measurement

A JTOL test is costly both in the test setup and test time because it requires repetitive measurements of the BER while varying the magnitude and frequency of the sinusoidal jitter (SJ) being imposed onto the data stream input, running at multi-Gbps data rate. For instance, each BER measurement takes at least 100 seconds for a 10-Gbps system, in order to collect sufficient samples to estimate the BER less than 10^{-12}. In addition, the JTOL is typically measured over 20$\sim$50 SJ frequency points and at each point, multiple BER measurements are required to find

the SJ magnitude that yields the target BER. As a result, a thorough JTOL test can take a few hours. Besides, the equipment that can generate multi-Gbps data streams with variable SJ frequency and magnitude is very expensive.

While many solutions to reduce the testing cost and time of JTOL measurement have been investigated, most of them focused on the cost-effective ways of generating the data streams with the desired SJ [37–43]. It implies that additional efforts beyond just designing the CDR are necessary in order to test the JTOL of the CDR itself.

This section explains a simple and efficient technique for the CDR to measure its own JTOL characteristic while operating with an ordinary transmitter.

The on-chip JTOL measurement technique proposed in this dissertation extends the digitally-controlled receiver-side jitter injection method described in [43] so that the necessary hardware and testing time are further reduced by separately measuring the low-frequency and high-frequency JTOL characteristics of the CDR.

The basic idea is to measure the tracking bandwidth and timing margin (i.e., the high-frequency JTOL) of the CDR in two separate measurements. The JTOL curve can be divided into two linear segments that represent two key information of the CDR. The low frequency segment with -20dB/dec of slope represents the required tracking bandwidth of the CDR, while the horizontal segment at high frequencies indicate the necessary timing margin of the CDR [44]. Therefore, the JTOL characterization can be effectively substituted by the two measurements measuring the tracking bandwidth and timing margin.

A similar idea was introduced in [45], where the high-frequency JTOL was estimated from the jitter measured by an on-chip jitter measurement circuit and the

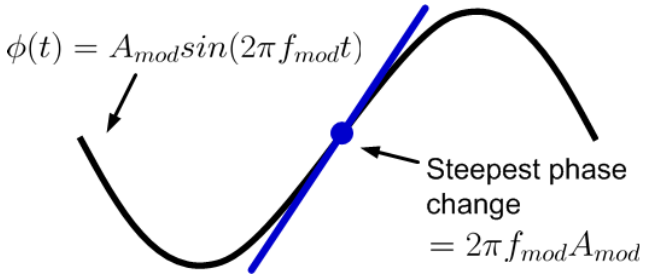


Figure 4.20: An example of the sinusoidal jitter.

low-frequency JTOL was measured by applying an SSC-modulated input to the CDR and measuring the resulting jitter in the recovered clock. However, the technique still calls for repetitive measurements at multiple SSC-modulation frequencies in order to construct the complete JTOL curve of the CDR. In comparison, it will be shown that the proposed technique can estimate the complete JTOL curve by performing just two measurements without sweeping the SJ frequency. It can greatly relax the requirement on the necessary hardware and also reduce the testing time.

To measure the low-frequency JTOL, the proposed technique applies a linear ramp to the recovered clock phase instead of a sinusoid to avoid the need of generating the sinusoidal waveform. Note that in case of using a SJ with a modulation frequency of fmod and amplitude of A_{mod}, the SJ has the maximum change rate of:

$$\frac{d}{dt}A_{mod}sin(2\pi f_{mod}t) = 2\pi f_{mod}A_{mod} \tag{4.6}$$

as illustrated in Fig. 4.20. Therefore, by applying a linearly-ramping phase that has the same slope as Eq. (4.6), the effective tracking bandwidth and hence the low frequency JTOL curve can be estimated. For example, if the CDR tolerates a ramp phase with a slope of f_{ramp}, it can be deduced that the JTOL curve at low frequency

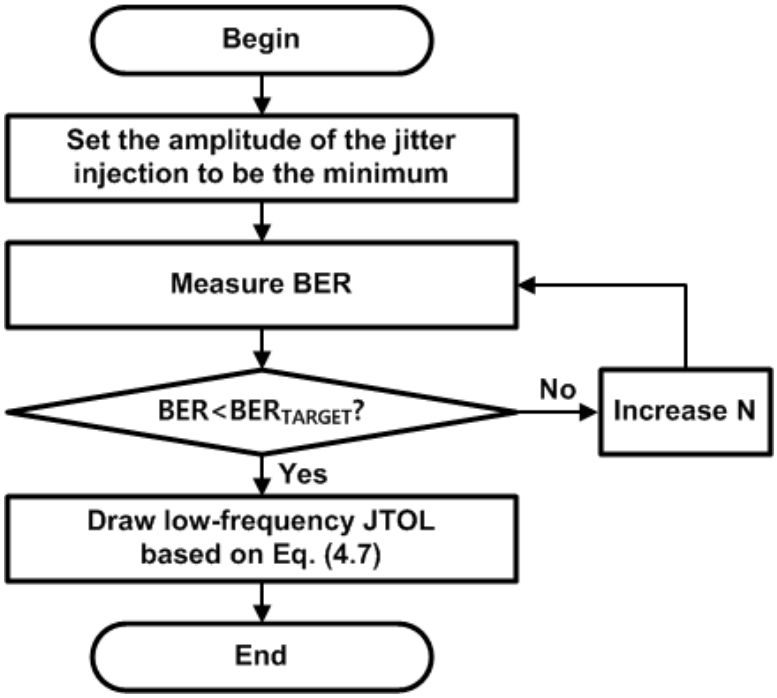


Figure 4.21: Proposed procedure to measure the low-frequency JTOL.

is higher than

$$A_{mod}(f_{mod}) = \frac{f_{ramp}}{2\pi f_{mod}}. \tag{4.7}$$

On the other hand, the high frequency JTOL, or equivalently, the timing margin of the CDR is measured by applying a periodic step change to the recovered clock phase. Since the abrupt change of the clock phase cannot be tracked by the CDR feedback loop, the maximum tolerable step change in the phase indicates the high-frequency JTOL. For example, if the BER does not exceed the specified rate even with a 2/9-UI phase step change, one can deduce that the high-frequency JTOL of the CDR is higher than 2/9 UI.

Fig. 4.21 summarizes the overall procedure of the proposed low-frequency JTOL measurement. Basically, the procedure finds the steepest ramp slope of the added

jitter that can be tolerated by the CDR. Once this slope value is found, the low-frequency JTOL curve can be estimated using Eq. (4.7) without making multiple measurements at different SJ frequencies. The similar procedure also applies to the high-frequency JTOL measurement. In that case, the only difference is that it looks for the largest step magnitude in the clock phase that can be tolerated instead of the steepest ramp slope.

The proposed JTOL measurement technique greatly saves the testing time by avoiding the repetitive measurements at multiple SJ frequencies and reduces the hardware costs by using a simpler jitter pattern (i.e. ramp and step) than a sinusoid. In other words, the described measurement procedures find the slope and position of the two JTOL curve lines, each corresponding to the tracking bandwidth and timing margin, respectively, instead of finding a single JTOL value for each SJ frequency.

It should be noted that the testing time can be further improved if the proposed technique is combined with some other previously reported techniques. For example, ref. [46] described an efficient method to find the parameter value that yields the BER of 10^{-12} with far fewer samples of 106 bits. Also, ref. [39] described a way to perform simultaneous JTOL measurements on multiple receivers in parallel, to speed up the ATE production tests.

4.6 Measurement Results

The described prototype CDR was fabricated in a 65nm LP CMOS technology and its chip photograph and performance summary are given in Fig. 4.22 and Tab. 4.6, respectively. The CDR occupies the total area of $0.026mm^2$, including the equalizing receivers. The CDR acquires the correct lock and achieves BERs less than 10^{-12}

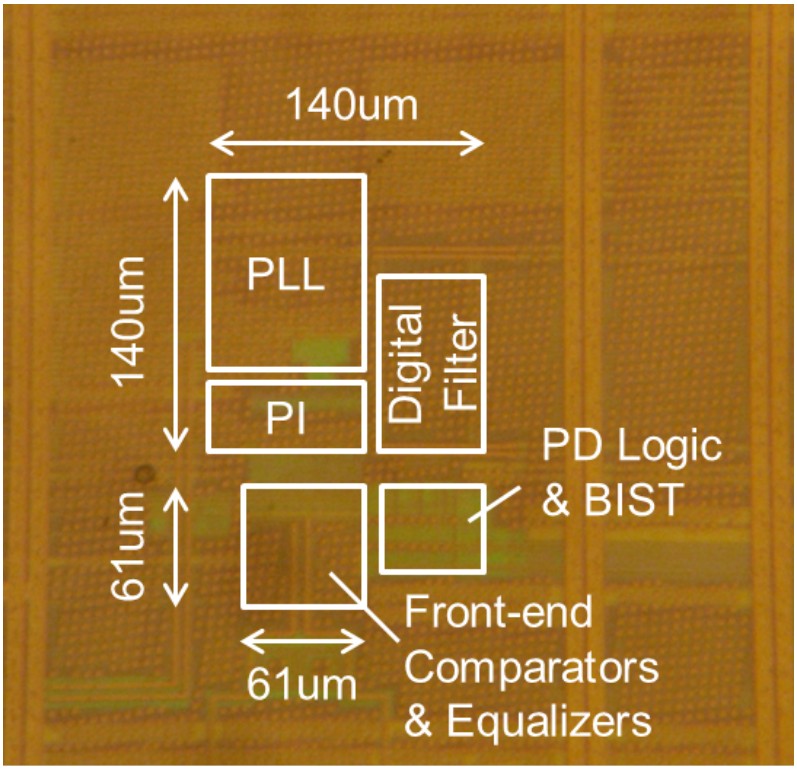


Figure 4.22: The die photograph of the prototype CDR with equalizing receiver fabricated in 65nm CMOS.

while operating at 4.6∼5.6-Gbps and a nominal 1.2V supply. When the supply voltage is increased to 1.3V, the operating range is extended to 5.4 7.6-Gbps. The lowest data rate is limited by the level converters that fail to convert the low VCO clock swing to a full VDD swing when the clock frequency and hence the regulated VCO supply (V_{REG}) are low. When operating at 5-Gbps, the CDR consumes the total of 8.4-mW from the 1.2V supply, corresponding to an energy efficiency of 1.7-pJ/bit. By virtue of the coarse resolution of only 3 steps, the 4 differential phase interpolating stages consume only 1mW in total.

The jitter histograms of the recovered clock with and without the frequency

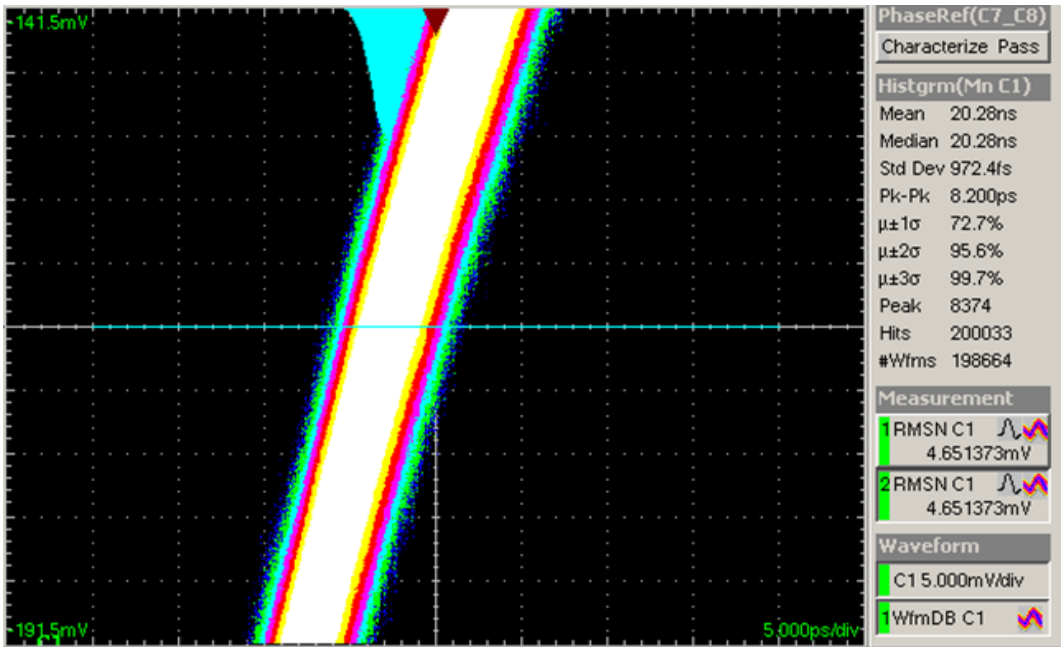
Table 4.1: The Prototype Chip Performance Summary

Technology		TSMC 65nm low-power process
Supply Voltage		1.2V
Data Rate	VDD=1.2V VDD=1.3V	4.6 5.6Gb/s 5.4 7.6Gb/s
Data Pattern		PRBS $2^7 - 1$
Jitter Tolerance	at 10MHz at 100kHz	0.14 UI 10UI
Recovered Clock Jitter	Meso-chronous Plesio-chronous	$0.97ps_{rms}$, $8.2ps_{pp}$ $2.7ps_{rms}$, $25.3ps_{pp}$
Total Area		$0.026mm^2$
Power Efficiency		1.7pJ/bit

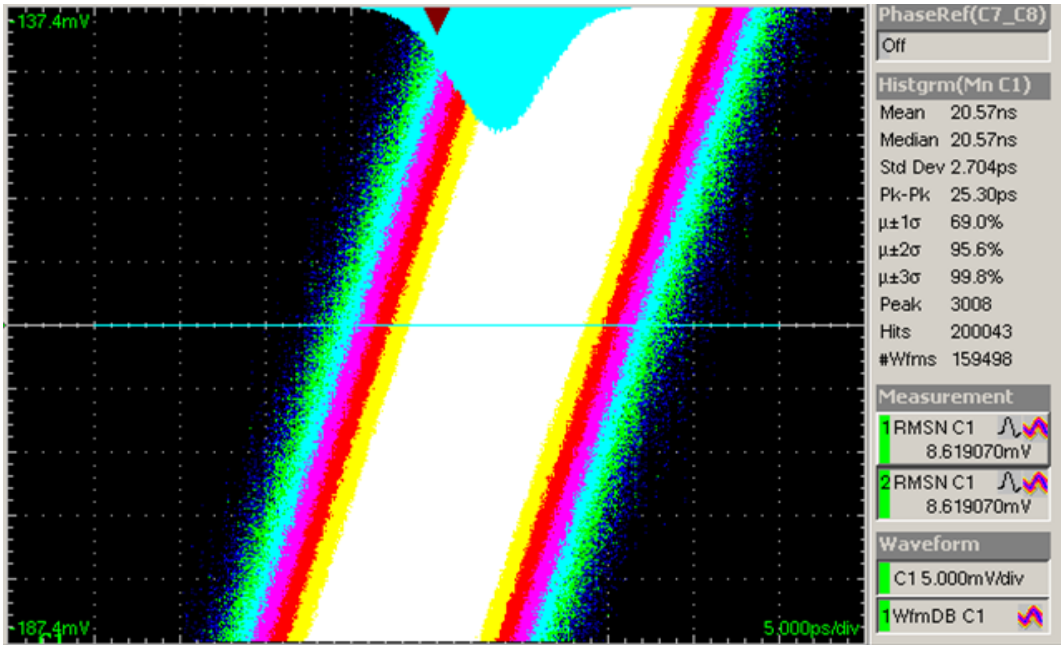
offset between the data and the PLL reference clock is shown in Fig. 4.23. Without a frequency offset (i.e. mesochronous mode), the CDR keeps selecting just one phase without dithering, and the 2.5-GHz clock output has the jitter of $0.97ps_{rms}$ and $8.2ps_{pp}$. With a 100-ppm frequency offset applied (pleisiochronous mode), the jitter is increased to $2.7ps_{rms}$ and $25.3ps_{pp}$ as the CDR phase shifts through all the available phases.

Fig. 4.24 shows the CDR's response to a 1-MHz sinusoidally-changing input phase, demonstrating that the recovered phase indeed does not dither. The waveforms of the final phase detector signals UP and DN indicate that the CDR's output phase moves only in the direction of the input change without any wandering, as typically seen in BB-CDRs.

Fig. 4.25 shows the jitter histograms of the recovered clock as the timing offset between the data and PLL reference clock is varied. As expected from our analysis, for most cases, the clock does not exhibit dithering and the histogram has only one peak. However, when the desired lock point is close to the middle between two selectable phases, both the neighboring phases are equally optimal and the CDR may



(a)



(b)

Figure 4.23: Measured jitter of the recovered clock at 5Gbps in (a) meso-chronous configuration and (b) plesio-chronous configuration.

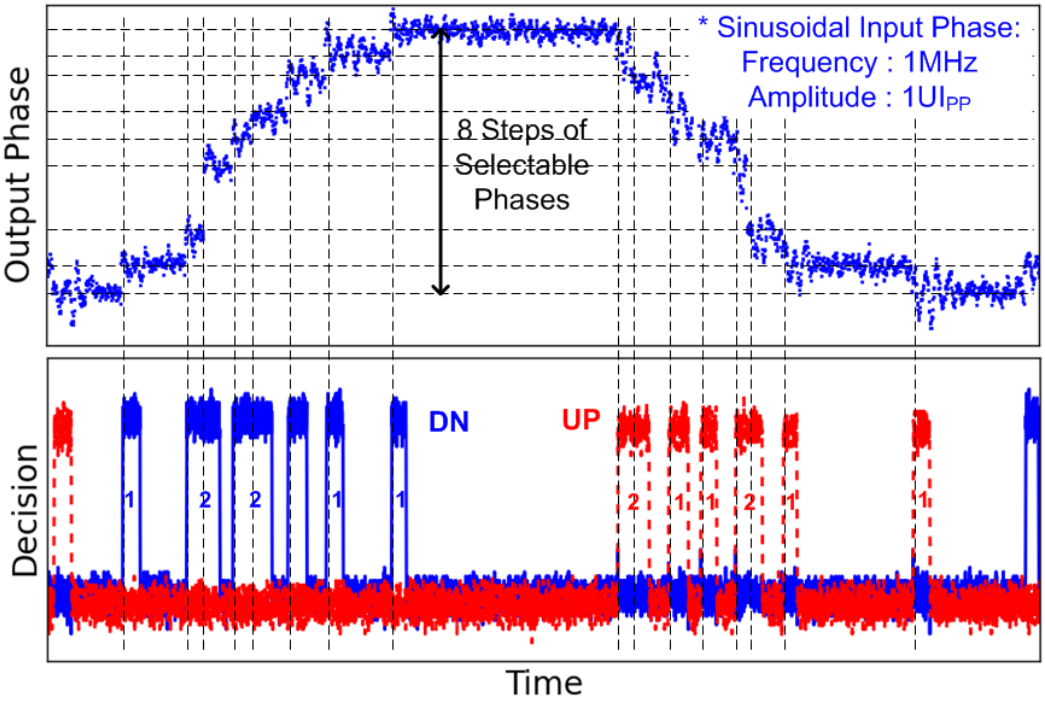


Figure 4.24: Output phase and the decision of the loop when 1MHz, $1UI_{pp}$ of sinusoidal input phase is applied. The applied data pattern is $2^7 - 1$ PRBS.

alternate between the two. Nonetheless, the worst-case phase quantization error is still limited to one half of a unit phase step. The estimated worst-case phase error is 26ps, which corresponds to roughly one-half of the phase step (11-ps) plus 4.4-σ of the random jitter ($\sigma = 3.4ps_{rms}$). Note that the results in Fig. 4.25 were measured with a real-time oscilloscope, which tends to give worse jitter characteristics than a sampling oscilloscope due to its limited time resolution and trigger precision.

With additional samplers in the receiver that sample the data with adjustable timing and voltage offsets, one can measure the effective eye opening seen by the receiver by comparing their outputs with those of the data samplers [31]. Fig. 4.26 shows the measured effective eye diagram with the BER target of 10^{-3} when a $2^7 - 1$

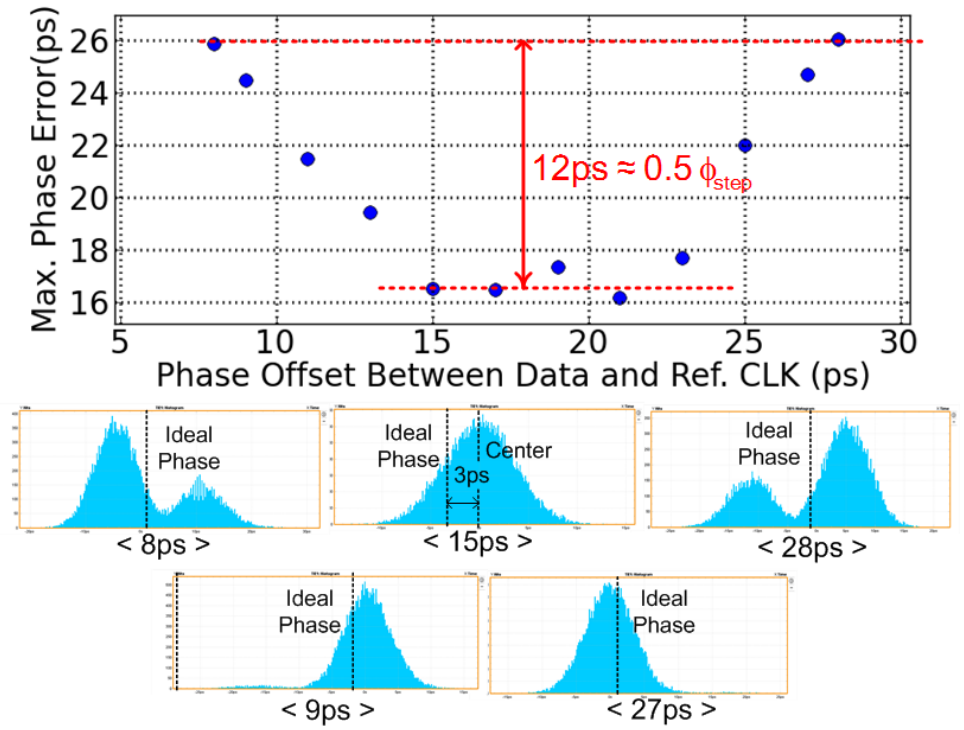


Figure 4.25: Jitter histograms and the maximum phase error with various timing offsets between data and PLL reference clock.

PRBS pattern with 100m$V_{pp,diff}$ swing is applied to the input. The measured eye opening is 6/9-UI wide and 65-mV tall. The opening is narrower than the one seen externally, as it includes the effects of the sampling clock jitter and the receiver's voltage offset and noise. For instance, the vertical shift in the eye due to a -30mV input-referred offset can be clearly seen in the figure.

The CDR's jitter tolerance (JTOL) characteristics were also measured with the proposed in-situ JTOL measurement technique. Fig. 4.27 compares the JTOL characteristics estimated by the described on-chip method and measured by external equipments (e.g. BERT). Due to the coarse phase resolution of our CDR, the on-chip method can only predict the region where the JTOL curve is expected to lie in,

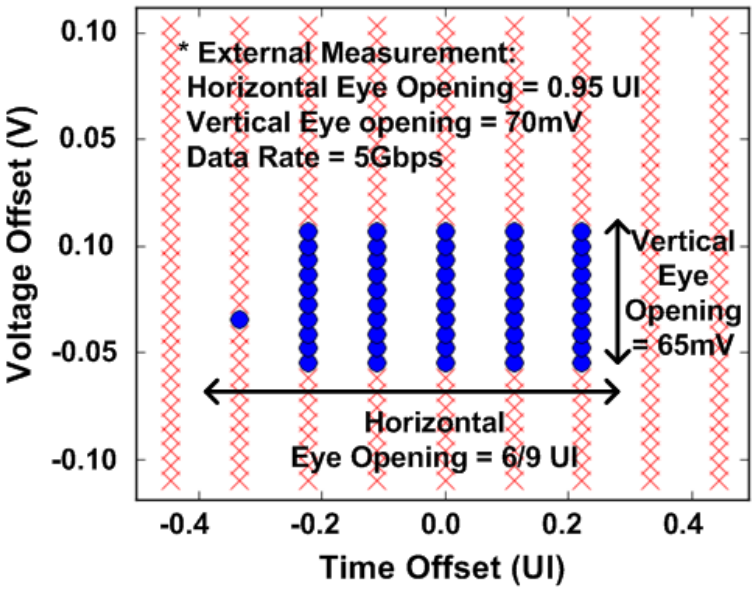


Figure 4.26: Measured on-chip eye diagram.

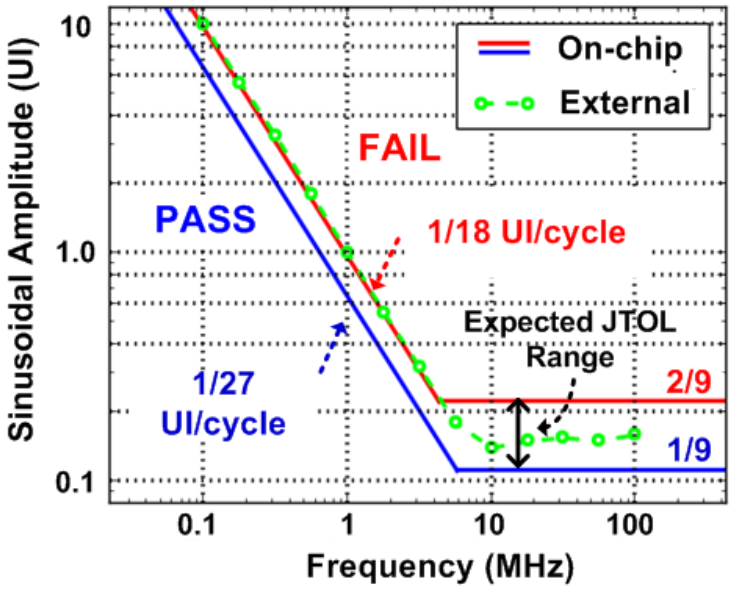


Figure 4.27: Comparison of JTOLs measured with internal and external phase modulation.

and the actual JTOL curve measured by the external equipments indeed lies within this region. The upper and lower bounds of the low-frequency JTOL correspond to the phase ramps of 1/18 UI/cycle (pass) and 1/27 UI/cycle (fail), respectively. The high-frequency JTOL is estimated to be at least 1/9 UI, as the CDR can tolerate an instantaneous change in the phase offset by 1/9 UI without any loss in the BER.

Chapter 5
Conclusion

To understand and minimize the dithering of bang-bang controlled timing loops, various analysis techniques and a novel phase interval detector that finds the optimal phase have been presented.

The pseudo-linear analysis explained in Chapter 2 employs two-input linearized BBPD model with an additive quantization noise. Various simulation results including jitter transfer, jitter generation and jitter tolerance demonstrated that it can accurately model the effects of the random noises, transition density, and loop delay. In addition the necessary conditions for this pseudo-linear analysis to be valid are derived. As long as sufficient noise is present in the system, the design of BB-CDRs or all-digital PLLs can leverage the design insights with the linear systems. When compared with the time-accurate simulation results, the proposed analysis provides more accurate predictions than the previously reported models [8, 12, 14, 18].

Chapter 3 explained three techniques to analyze the bang-bang controlled loops without approximating them to a linearized one, and discussed the strength of each technique. The stochastic transient analysis can be applied to most of non-linear circuits without any assumption while improving the simulation speed by exploiting the stochastic information of random noise sources. Phase-portrait analysis has strength when analyzing locking behavior or bit-slipping. Lastly, Markov chain model is the most efficient way to find the steady-state bahavior. The stochastic

analysis technique and Markov chain model were extensively used for the analysis of phase interval detector in Chapter 4

The phase interval detector, consisting of a pair of bang-bang phase detectors and an odd number of selectable phases effectively removes dithering in bang-bang controlled CDRs. As a result, a CDR can achieve low jitter even with a coarse phase step and save power in the phase adjustment circuits. The prototype CDR has only 9 selectable phases in a UI and consumes 8.4mW of power where the interpolators consume only 1mW. The area of the CDR is only $0.026mm^2$, which is the smallest one among previously reported ones achieving over 5Gbps of data rate. Even with corase phase resolution the measured jitter is as low as $0.97ps_{rms}$ without a frequency offset, which increases to $2.7ps_{rms}$ with a 100-ppm frequency offset. In the case when the small output clock jitter must be achieved even with more power and area, increasing the phase resolution of the circuit can be a better solution, but the proposed phase interval detection technique is efficient when achieving low power and small area.

A fast and efficient on-chip JTOL measurement technique that does not require a high-cost pattern generator with a jitter generation capability has been also described. The proposed technique measures the tracking bandwidth and timing margin of the CDR by applying a ramp and step change in the recovered clock phase, respectively, and achieves a 20× reduction in the testing time. The experimental results with the prototype CDR and on-chip JTOL measurement circuit fabricated in a 65nm CMOS demonstrate that the presented technique can estimate the actual JTOL curve well while requiring only $480\mu m^2$ of the additional area, which corresponds to only 1.8% of the total CDR area.

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초 록

Bang-bang 위상 검출 회로는 단순하면서도 빠르고 정확하며 디지털 구현이 용이한 특성 때문에 고속 통신용 위상 동기 회로 (Phase-locked loop), 지연 동기 회로 (Delay-locked loop), 클럭 및 데이터 복원 회로 (Clock-and-data recovery loop) 등에 널리 사용되고 있지만 비선형적인 특성을 가지기 때문에 전체 루프의 설계와 분석에 어려움이 있다. 특히 디더링은 해상도에 따른 bang-bang CDR의 트랙킹 속도와 지터 잡음간의 트레이드오프 관계의 원인이 된다. 고해상도의 위상 조절은 디더링을 줄이는데에 효과적이지만 전력 및 면적 소모를 증가시키는 단점이 있다. 이러한 배경에서 이 논문은 고해상도의 회로 없이 디더링 문제를 해결할 수 있는 최적 위상 검출 기술을 제안한다. 제안하는 위상 구간 검출 회로는 이상적인 위상 지점을 포함하는 위상 구간을 찾음으로서 최적 위상을 검출하고 디더링을 제거한다. 65nm CMOS공정으로 구현된 디지털 방식의 phase-interpolating DLL 기반의 CDR은 $0.11UI$의 낮은 해상도를 사용하며 $0.026mm^2$의 작은 면적과 $41mUI_{p-p}$의 저잡음 성능을 보이면서도 $5Gbps$로 동작시 $8.4mW$의 저전력을 소모한다. 또한 이 논문은 bang-bang controlled 시스템의 분석을 위한 다양한 기법을 소개한다. 소개된 기법들은 linearized 루프와 non-linear 루프에 모두 적용 가능하며, 제안된 위상 검출 기법의 특성을 검증에 사용되었다.