Ph.D.Dissertation

Design of DisplayPort Receiver with Video Clock Frequency Error Compensation Scheme

비디오 클럭 주파수 보상 구조를 이용한 디스플레이포트 수신단 설계

by

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August, 2014

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Design of DisplayPort Receiver with Video Clock Frequency Error Compensation Scheme

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이 논문을 공학박사 학위논문으로 제출함
2014 년 8 월

서울대학교 대학원
전기·컴퓨터공학부
김 태 호

김태호의 박사 학위논문을 인준함
2014 년 8 월

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위 원 _____ (인)

위 원 _____ (인)

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A Dissertation Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy
at
SEOUL NATIONAL UNIVERSITY

August, 2014

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Abstract

This thesis presents the design of DisplayPort receiver which is a high speed digital display interface replacing existing interfaces such as DVI, HDMI, LVDS and so on. The two prototype chips are fabricated, one is a 5.4/2.7/1.62-Gb/s multi-rate DisplayPort receiver and the other is a 2.7/1.62-Gb/s multi-rate Embedded DisplayPort (eDP) receiver for an intra-panel display interface.

The first receiver which is designed to support the external box-to-box display connection provides up to 4K resolution (4096×2160) with the maximum data rate of 21.6 Gb/s when 4 lanes are all used. The second one aims to connect internal chip-to-chip connection such as graphic processors to display panels in notebooks or tablet PCs. It supports the maximum data rate of 10.8 Gb/s with 4-lane operation which is able to provide the resolution of WQXGA (2560×1600). Since there is no dedicated clock channel, it must contain clock and data recovery (CDR) circuit to extract the link clock from the data stream. All-Digital CDR (ADCDR) is adopted for area efficiency and better performances of the multi-rate operation. The link rate is fixed but the video clock frequency range is fairly wide for supporting all display resolutions and frame rates. Thus, the wide range video clock frequency synthesizer is essential for reconstructing the transmitted video data.

A source device starts link training before transmitting video data to recover the clock and establish the link. When the loss of synchronization between the source device and the sink device happens, it usually restarts the link training and try to re-establish the link. Since link training spends several milliseconds for initializing, the

video image is not displayed properly in the sink device during this interval. The proposed clock recovery scheme can significantly shorten the time to recover from the link failure with the ADCDR topology. Once the link is established after link training, the ADCDR memorizes the DCO codes of the synchronization state and when the loss of synchronization happens, it restores the previous DCO code so that the clock is quickly recovered from the failure state without the link re-training.

The direct all-digital frequency synthesizer is proposed to generate the cycle-accurate video clock frequency. The video clock frequency has wide range to cover all display formats and is determined by the division ratio of large M and N values. The proposed frequency synthesizer using a programmable integer divider and a multi-phase switching fractional divider with the delta-sigma modulation exhibits better performances and reduces the design complexity operating with the existing clock from the ADCDR circuit. In asynchronous clock system, the transmitted M value which changes over time is measured by using a counter running with the long reference period (N cycles) and updated once per blank period. Thus, the transmitted M is not accurate due to its low update rate, transport latency and quantization error. The proposed frequency error compensation scheme resolves these problems by monitoring the status of FIFO between the clock domains.

The first prototype chip is fabricated in a 65-nm CMOS process and the physical layer occupies 1.39 mm^2 and the estimated area of the link layer is 2.26 mm^2. The physical layer dissipates 86/101/116 mW at 1.62/2.7/5.4 Gb/s data rate with all 4-

lane operation. The power consumption of the link layer is 107/145/167 mW at 1.62/2.7/5.4 Gb/s. The second prototype chip, fabricated in a 0.13μm CMOS process, presents the physical layer area of 1.59 mm^2 and the link layer area of 3.01 mm^2. The physical layer dissipates 21 mW at 1.62 Gb/s and 29 mW at 2.7 Gb/s with 2-lane operation. The power consumption of the link layer is 31 mW at 1.62 Gb/s and 41 mW at 2.7 Gb/s with 2-lane operation. The core area of the video clock synthesizer occupies 0.04 mm^2 and the power dissipation is 5.5 mW at a low bit rate and 9.1 mW at a high bit rate. The output frequency range is 25 to 330 MHz.

Keywords : DisplayPort, high speed serial link, display interface, video clock synthesizer, video clock frequency control, frequency error compensation

Student Number : 2009-30188

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Chapter 1

Introduction

1.1 Background

Recently, the growing broad adoption of digital display device such as Liquid Crystal Display (LCD) has been standardized due to the primary disadvantages of analog signal processing like signal distortion, crosstalk noise and so on. Beginning with the development of Digital Visual Interface (DVI), which is available in both the analog plus uncompressed digital video and digital-only forms, various digital display interfaces have emerged within the last few decades. And higher bandwidth for display interface is required as increasing demands for high resolution displays [1]-[7].

In the digital display interface, the digital video data is transmitted from a display source device connected to a display sink device such as a computer monitor or TV.

the display sink device reconstructs the video pixel data (RGB), a vertical synchronization (VSYNC) and a horizontal synchronization signal (HSYNC) accompany with the video pixel clock as shown in Fig. 1.1.

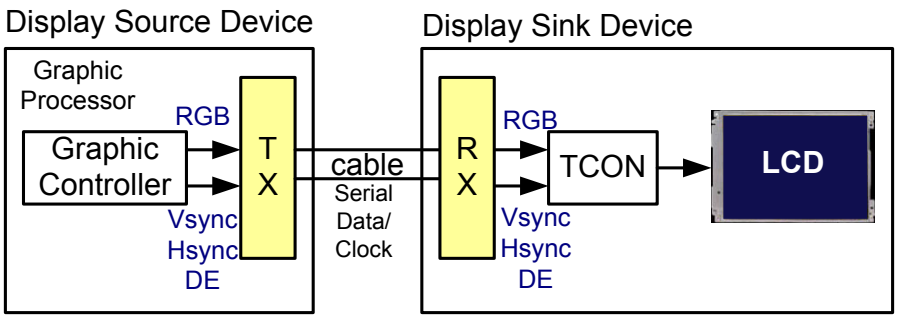


Fig. 1.1 Digital display interface

High Definition Multimedia Interface (HDMI) is a compact audio and video interface for transferring uncompressed video data and compressed or uncompressed digital audio data from a HDMI-compliant source device to a compatible Consumer Electronics (CE) devices such as TVs, DVD players, video game consoles, set-top receivers and so on [8]. The maximum bandwidth higher than DVI is supported as the growing needs for the better performances of displays featuring higher refresh rates, color depths and display resolutions. Also the concerns over content protection are prompting significant changes in digital display interface technology [9]. HDMI supports the Intel High Definition Content Protection (HDCP) copy-protection

scheme for required products in the CE market. These days HDMI has become one of the most popular digital display interface and widely used in display devices.

The demand for new digital display interface standard to meet future demands on the digital display interface and to provide cost-effective, scalable industry standard and to reduce complexity has been raised lately. The imposed loyalty for HDMI development and the need for extensible interface suited for both external device and internal display interfaces prompted the development of the next generation of the digital display interface. DisplayPort, which is an open-standards based and royalty-free digital display interface, offers many advantages of the proprietary DVI, HDMI and legacy LVDS interfaces. DisplayPort is a scalable digital display interface with uncompressed video data transmission, optionally audio data carrying and content protection capability for broad application within computer and CE devices. The interface is designed to satisfy several needs in computer and CE industries by supporting both box-to-box digital display connections that includes display connections between computers and monitors, projectors, and TV displays and internal chip-to-chip connection that includes usage within a notebook PC and a tablet PC for driving a panel from a graphics processor. It replaces both external and internal connection with the advantages [10].

1.2 Motivation

The maximum resolutions and data rates of the digital display interfaces are dramatically increasing as shown in Fig. 1.2 [11]. Currently, Ultra High Definition Television (UDTV) including 4K (3840×2160) and 8K (7680×4320) has been developed and will be provided in the near future. Displayport version 1.2 offers maximum link bandwidth up to 21.6 Gb/s with 4-lane operation, supporting 4K resolution and future version will provide maximum link bandwidth up to 32.4 Gb/s in total which is available to support 8K resolution.

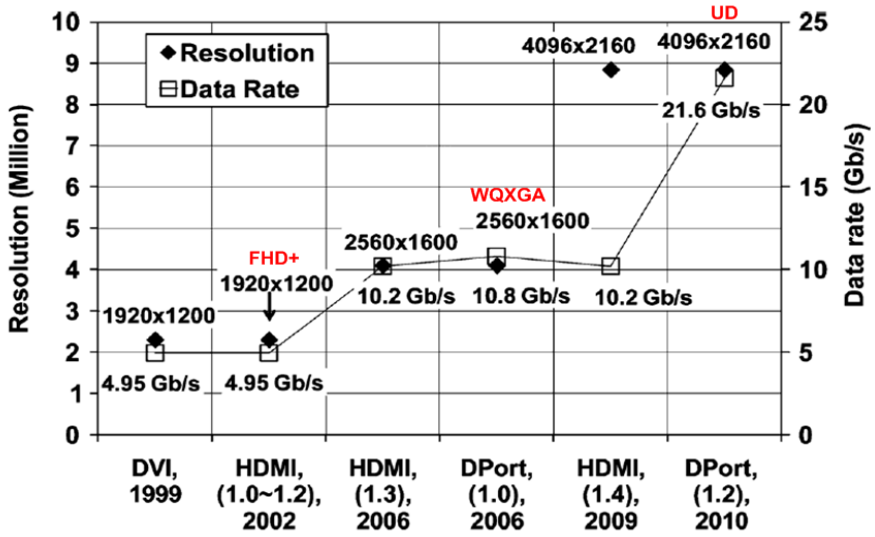


Fig. 1.2 Digital display interface trends

DisplayPort data transport link consists of a main link, an auxiliary channel (AUX CH) and a Hot Plug Detect (HPD) signal line as shown in Fig. 1.3. The main link is a unidirectional, high-bandwidth and low-latency channel used to transmit uncompressed video and audio data. The AUX CH is a half-duplex bidirectional channel used for link initialization, link training and device configuration by hand-shaking. The HPD signal serves as a notification of the connection and an interrupt request by the receiver device.

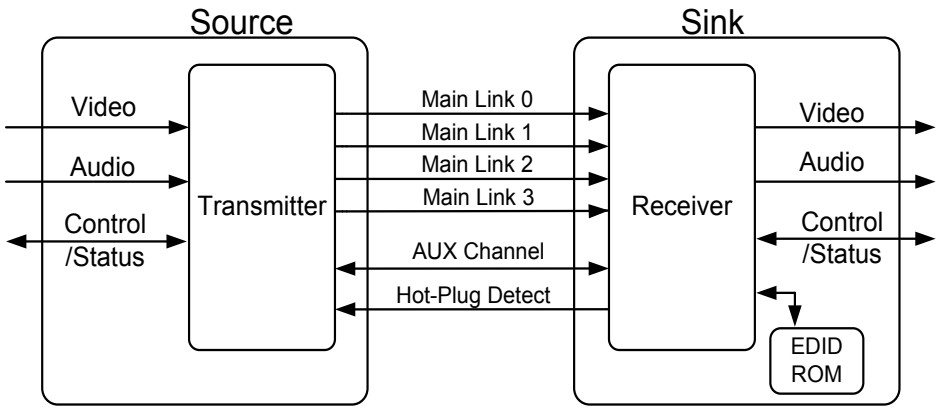


Fig. 1.3 DisplayPort data transport channels

According to DisplayPort version 1.2, main link should support three link rates of high bit rate 2 (HBR2), high bit rate (HBR), and reduced bit rate (RBR) which are 5.4Gb/s, 2.7 Gb/s and 1.62 Gb/s per lane, respectively. Since there is no dedicated

clock channel, the clock is extracted from the data stream in receiver side. Clock and Data Recovery (CDR) circuit is an essential component in this interface.

It supports a fixed link rate regardless of the display types and the link rate is decoupled from the pixel rate. All-Digital CDR (ADCDR) is adopted in this work with its primary advantages. By replacing the analog circuits with digital ones, it alleviates a filter leakage and a reduced dynamic range issues. The area efficiency can be improved because large passive components are not required and PVT variation can be covered more easily so that the better stability with digital filter can be obtained [12]-[15]. Frequency and phase information can be processed more flexibly by initializing and memorizing Digitally Controlled Oscillator (DCO) codes. Since the receiver needs to be capable of the multi-rate operation as shown in Fig 1.4, the usage of digital codes makes the mode changing efficient.

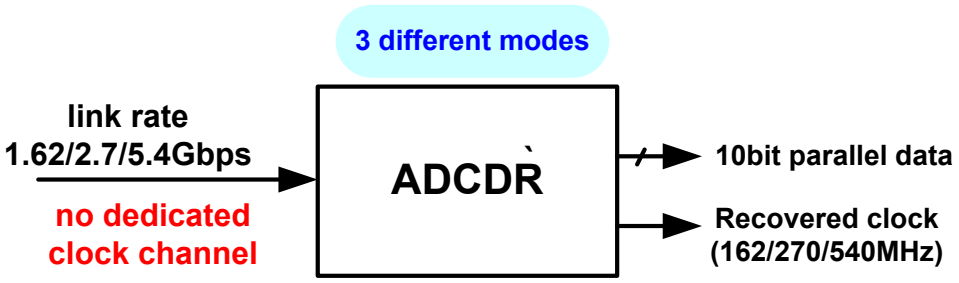


Fig. 1.4 Clock and data recovery with multi-rate operation

Upon HPD signal detected, a source device starts link training before transmitting video data to configure the link capacity and recover the clock for establishing the link. The number of lanes, the link rate and the correct drive current and equalization level are determined through handshaking between the transmitter and receiver via AUX CH. Once link training is finished successfully, normal operation follows and the sink device may notify a loss of synchronization by asserting the HPD signal to request interrupt. When the link failure happens, the source device usually checks the receiver status through AUX CH and try link training again to re-establish the link. Since link training spends several milliseconds for checking the receiver status and re-initializing the link configuration, the sink device displays wrong screen during this interval. However, this unwanted interval can be significantly shortened by the proposed clock recovery scheme which uses ADCDR topology of memorizing and initializing the start DCO codes. Once the link is established after link training, the ADCDR remembers the DCO codes of the synchronization state and when the loss of synchronization happens, it restores the previous DCO code so that the clock is quickly recovered to the normal operation without link re-training. Fig. 1.5 shows the simplified operation flow of the proposed clock recovery scheme.

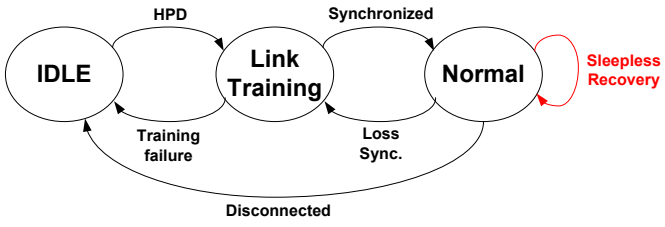


Fig. 1.5 Simplified operation flow of the proposed clock recovery

Link must be operating at the fixed link rate regardless of the display types and it is decoupled from the pixel rate. The video clock frequency range is fairly wide for supporting all display resolutions and frame rates. Thus, the wide range video clock frequency synthesizer is essential for reconstructing the transmitted video data. The video stream clock is regenerated from the link rate using the time stamp values M and N which are transmitted with the data stream. Fig. 1.6 illustrates the video stream clock reconstruction scheme in the DisplayPort transceiver.

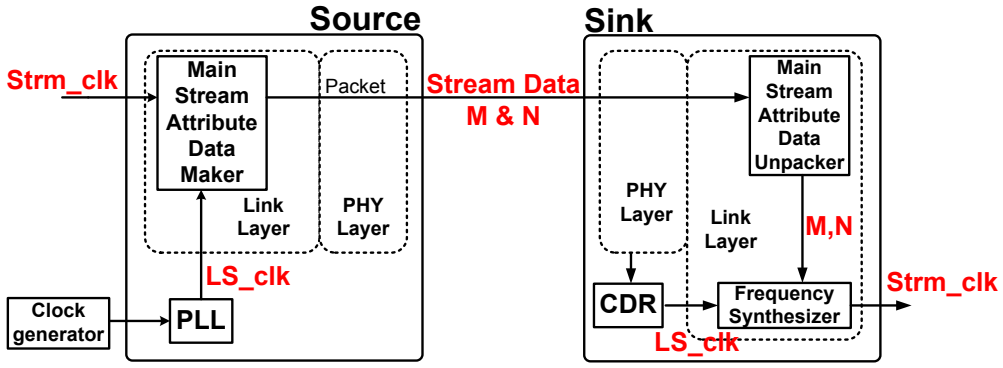
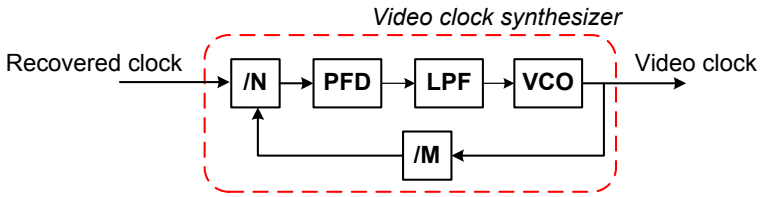


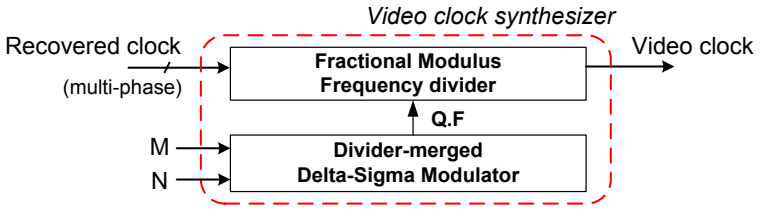
Fig. 1.6 Video stream clock recovery in sink device

Phase-locked loop (PLL)-based frequency synthesizer, which is one of the most popular classes, can be considered for video clock synthesis as shown in Fig. 1.7 (a). However, it is difficult to design because M and N value is very large so that it should have a very large number front divider and very high multiplication ratio

which results in a low loop bandwidth and poor performance such as slow dynamics, high 1/f noise, and large jitter. And the wide output frequency range is also challenging in the PLL design [16]-[20]. On the other hand, direct all-digital frequency synthesizer, which is shown in Fig. 1.7 (b), is suitable architecture for the DisplayPort application because the wide output frequency range and the fast frequency switching can be achieved more easily compared to the PLL-based design [21]-[27]. Since high frequency multi-phased clocks which are recovered from the fixed data rate already exist in this work, only a little additional hardware is required to enhance the resolution.



(a)



(b)

Fig. 1.7 (a) PLL-based frequency synthesizer. (b) direct all-digital frequency synthesizer.

There are two decoupled clock domains and the transmitted video data passes the boundary of the recovered clock domain and the video stream clock domain. An asynchronous FIFO is a safe way to pass multi-bit values between the completely decoupled clock domains. The write clock for the dual-port buffer is the fixed rate but the read clock varies over wide range depending on the display types. Since the time stamp value M and N is the only way to determine the video stream clock frequency. The transmitted M value should be accurate enough to synthesize fine video clock frequency. If the transmitted M value has some errors, the video clocks of the transmitter and the receiver have a frequency offset. This can raise serious problems in FIFO operation which cause data to be lost due to FIFO overflow or invalid data to be read from the FIFO due to an attempt to read the same data again. There are several systematic elements that cause the M value error in data transport services. To overcome this, the frequency error compensation scheme is proposed in this work. The proposed scheme makes up the M value error by monitoring FIFO status and applies the modified M value to the frequency synthesizer core.

In this thesis, two types of DisplayPort receivers are designed. One is a 5.4/2.7/1.62-Gb/s Receiver for DisplayPort version 1.2 and the other is 2.7/1.62-Gb/s Receiver for Embedded DisplayPort (eDP) version 1.2 for intra-panel display interface. Both have ADCDR circuits inside the physical layer which are capable of the multi-rate operation. The second eDP receiver includes the proposed clock recovery scheme. And the direct all-digital frequency synthesizer for video stream clock generation is presented. The proposed synthesizer employs the programmable integer divider and the multi-phase switching fractional divider with the delta-sigma modulator (DSM). The lower design complexity and the better performance can be

achieved by choosing the direct all-digital method. The frequency error compensation scheme resolves the FIFO false operation caused by the transmitted M value error.

1.3 Thesis Organization

This thesis is organized as follows. In Chapter 2, the Digital Display Interface including DisplayPort is described. The existing interfaces are compared and the overview of DisplayPort interface is presented. In Chapter 3, the first design which is 5.4/2.7/1.62-Gb/s Receiver for DisplayPort version 1.2 is described in detail. Chapter 4 deals with the second design of 2.7/1.62-Gb/s Receiver for Embedded DisplayPort (eDP) version 1.2 and the proposed cock recovery scheme is explained. Chapter 5 provides the proposed architecture of the video clock synthesis circuit which is capable of frequency error compensation. Chapter 7 concludes this thesis.

Chapter 2

Digital Display Interface

2.1 Overview

In the last few decades, a number of new and competing digital display interfaces have emerged. Some of them claim to have special benefits, whereas there are some overlaps. As the most of CRT monitors were replaced by LCD monitors or other new display technologies, the old VGA interface was moving to change to all-digital interface. Since the early 1990s, various plans including digital and analog hybrid approaches and several all-digital display interfaces have been proposed. The Digital Visual Interface (DVI) was developed by the Digital Display Working Group (DDWG) in 1999. DVI became the first reasonably-successful digital display Interface for PC monitors. It replaced the older analog VGA interface. The analog video

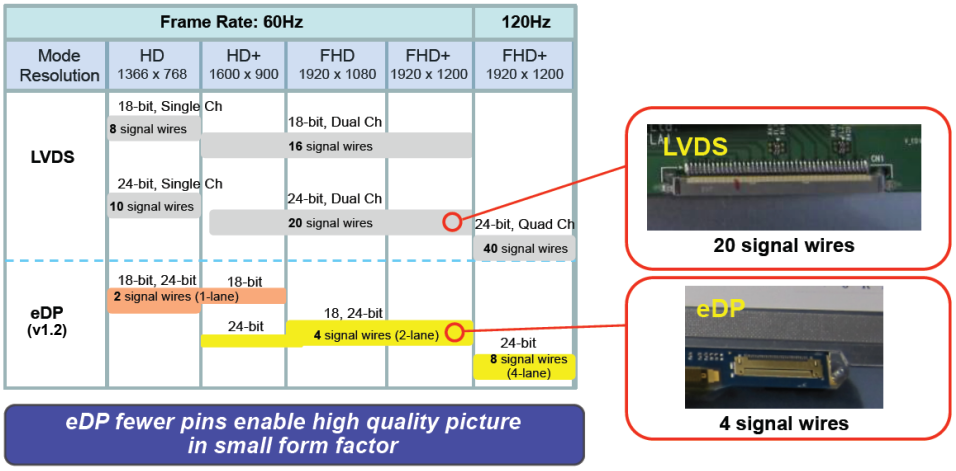
bandwidth of DVI is much higher than that of VGA so that the higher resolution and frame rates could be supported. Silicon Image suggested a new consortium to develop a digital interface specifically for the Consumer Electronics (CE) market. As a result, CE market has started to migrate from the previous analog interfaces to the all-digital connection such as High Definition Multimedia Interface (HDMI). The HDMI interface has become widely successful. It became the most common digital display interface in TVs, set-top boxes, blu-ray players, A/V receivers, gaming consoles, cam-coders, and digital cameras. Also it has been included in some smart phones and tablet PCs. Most recently, a new digital display interface standard, DisplayPort specification, has been suggested by the Video Electronics Standards Association (VESA). The interface is simple and royalty-free, and the relatively low cost of implementation compared to other interfaces. It supports both box-to-box connection and internal chip-to-chip connection. Thus, it is possible to replace Low-Voltage Differential Signaling (LVDS) which is the most popular intra-panel display interface. DisplayPort differs from the earlier TMDS-based DVI and HDMI in protocol. It is the first digital display interface to use packetized data transmission method and unlike legacy standards that differential pairs are fixed to transmitting a dedicated clock signal with each output channel, it can embed the clock signal within the data packet stream. It also supports to transmit audio and video simultaneously and a bi-directional, half-duplex auxiliary channel (AUX CH) delivers device configuration and management data for the link establishment. Table 2.1 shows the basic comparison of various digital display interfaces with DisplayPort interface [28], [29].

Table 2.1 Comparison of Digital Display Interface

	DisplayPort	DVI	HDMI	LVDS
No. of data & clock pairs	1~4 data pairs no separate clock pairs	3 or 6 data pairs 1 clock pair	3 or 6 data pairs 1 clock pair	8 data pairs 2 clock pairs
Bit rate, per pair	1.6, 2.7 or 5.4 Gbps (v1.2) or 8.1 Gbps (v1.3)	~1.65Gbps	~3.4 Gbps (v1.4) ~6 Gbps (v2.0)	945 Mbps (135MHz clock)
Total throughput	~21.6 Gbps (v1.2) ~32.4 Gbps (v1.3)	~4.95 Gbps ~9.9 Gbps(dual)	~10.2 Gbps (v1.4) ~18 Gbps (v2.0)	~7.56 Gbps
Clock	Embedded	Separate pair	Separate pair	Separate pair
Max consumer resolution	3840×2160 @60 (v1.2) 8102×4320 @60 (v1.3)	1920×1200 @60 3840×2400 @33 (dual)	4096×2160 @30 (v1.4) 4096×2160 @60 (v2.0)	2048×1536 @60 (dual)
Other channel	1 Mbps or 720 Mbps (AUX or Fast AUX)	DDC(I2C)	DDC(I2C)	DDC(I2C)
Channel cod-ing	ANSI8B10B	TMDS	TMDS	None
Content Protection	DPCP/HDCP	HDCP	HDCP	None
Protocol	Packet-based (extensible to add features)	Serial data stream	Serial data stream with embedded audio	Sequential data stream

The DisplayPort interface have 1,2 and 4 differential data pairs in a main link, each lane has a bandwidth of 1.62, 2.7 or 5.4 Gb/s with internal clock running at 162, 270 or 540 MHz. With 8b/10b encoding, the effective data rates after decoding are 1.296, 2.16, and 4.32 Gb/s per lane which is 80% of the total. The future version of DisplayPort will increase overall transmission bandwidth to 32.4 Gb/s featuring 8.1 Gb/s per lane. This will support 8K resolution or 4K@120Hz and 3D in 4K resolution.

Embedded DisplayPort (eDP) was developed to be used specifically in embedded display applications link notebook, net-book, tablet PCs or all-in-one PCs. eDP is based on the VESA DisplayPort standard with same electrical interface and can share the same video port on the Graphic Processing Unit (GPU). Protocol is basically the same with DisplayPort but with some differences added for eDP. In PC applications, eDP will replace LVDS over the next few years while reducing system cost, power and size. One of the differentiated advantages of eDP versus LVDS is use of fewer signal wires than LVDS. Fig. 2.1 shows the comparison of the number of wires used in LVDS and eDP. eDP fewer pins enable high quality picture in small form factor. For the full HD (1920×1080@60Hz) display resolution, eDP requires only 1-lane@5.4Gb/s while LVDS requires 20 signal wires. In order to support the higher resolution and refresh rate, LVDS needs more wire counts with the wider cable. eDP reduces PCB trace and data signal wire count and signal type is more compatible with new chip processes. No separate video port needed because eDP can use a DisplayPort GPU interface and overall system power is reduced, increasing battery life. Lower EMI which means less system shielding can be achieved [30], [31].



[Source : VESA]

Fig. 2.1 Comparison of the number of wires used in LVDS and eDP.

2.2 DisplayPort Interface Characteristics

2.2.1 DisplayPort Version 1.2

In this thesis, the first fabricated prototype chip is targeted on DisplayPort version 1.2. Before implementing the detail in the next section, the brief overview about first chip is described in this section. The target specification is presented in Table 2.2. The chip is designed to convert DisplayPort interface to HDMI interface. The bandwidth of the interface is 5.4 Gb/s per lane and support 2.7 and 1.62 Gb/s. ADCDR which is capable multi-rate operation is included and the digital link operate at 1/10 of link rate with 10-bit de-serialized data. With 4-lane operation, the maximum bandwidth of the interface touches 21.6 Gb/s in total. The supported video format is up to 4k resolution in 2D format, and primary 3D video format. Component bit depths of 8, 10 and 12 are supported with the color formats of RGB, YCbCr 4:4:4/4:2:2 regardless of the number of main link lanes. Since there is no dedicated clock channel, the clock is extracted from the data stream itself with the video clock frequency synthesizer which supports the output frequency from 25 to 350 MHz of single pixel per clock. The optional insertion of secondary-data packets such as an audio stream packet is supported. The link training method is only full link training mode with handshaking of AUX CH. It supports an optional robust content protection schemes that is recommended High-bandwidth Digital Content

Protection System (HDCP) version 1.3. The reference equalization circuit is placed on the front end and the electrical signals of the incoming data have 4 peak-to-peak voltage swing and 4 pre-emphasis levels. In the external interface, the cable length is convertible, so the eye monitoring scheme for optimizing the equalization strength is contained. In order to reduce EMI, Spread Spectrum Clock (SSC) mode and data scrambling are supported. Based on a packetized protocol, it allows easy expansion of the standard with multiple data types and flexible allocation of available bandwidth between audio data and video data. 8B/10B channel encoding helps DC-balancing with AC-coupled signaling, byte synchronization and frequency compensation by stuffing dummy data.

Table 2.2 Specification of DisplayPort v1.2 chip

	Description
Target	DisplayPort v1.2 DP-to-HDMI conversion
Link Capability	1.62, 2.7 and 5.4Gbps 1,2 or 4 lanes 1.62 - 21.6Gbps
Supported Video format	2D : up to 3840×2160@30Hz and 4096×2160@24Hz (350MHz) Primary 3D video format support RGB/YCbCr444/YCbCr422 8, 10 and 12 bit per pixel
Video clock frequency	Single pixel per clock 25~350MHz
Audio	Supported (I2S and S/PDIF)
Link Training	Full Link Training Mode
Content Protection	HDCP v1.3
Electrical Signaling	4 peak-to-peak voltage swing and 4 pre-emphasis levels Receiver equalization
EMI reduction	Support Spread Spectrum Clock and Scrambling
Channel coding (8B/10B)	DC-balancing (AC-coupled signals) Byte synchronization (K-character) Channel alignment (K-character) Packetize Frequency compensation (insert dummy)
AUX CH	1Mbps, Manchester II coding

2.2.2 Embedded DisplayPort Version 1.2

The second fabricated prototype chip is targeted on eDP version 1.2 which aims to define a standardized display panel interface for internal connection. This interface is the electrical transport for video and auxiliary data between the graphics hardware and the display panel. Although the external box-to-box interface must interoperate with any connected compliant system over a variety of compliant cables, eDP usually connected on the board with the fixed wire line. Thus, the equalization circuit is just simple linear equalizer without adaptation and the full link training does not need to perform again if the well-known-good or last-known-good link configuration exists. Not only full link training mode, fast link training and no link training mode are contained in this design. This helps to finish link initializing and establishing much faster than the full link training. Link bandwidth is support 2.7 and 1.62 Gb/s per lane and supported video format is up to 2560×1600@60Hz. The color format supports only RGB with component bit depth of 6, 8 and 10 bit per pixel. The video pixel clock operates at dual pixel per clock mode, so only half pixel rate is needed. Audio transmission is excluded in this design and the content protection is implemented with the alternative scrambler seed reset and alternate framing. The design target of this chip is typical eDP to timing controller (TCON) interface. The eDP source is typically integrated into the graphics processor unit and the eDP sink is normally integrated into the display processor, such ad in the LCD timing controller inside the device. Table 2.3 shows the specification of the second proto type chip.

Table 2.3 Specification of eDP v1.2 chip

	Description
Target	DisplayPort v1.1a and Embedded DisplayPort v1.2 eDP-to-TCON interface
Link Capability	1.62 and 2.7Gbps 1,2 or 4 lanes 1.62 - 10.8Gbps
Supported Video format	up to 2560×1600@60Hz (348.5MHz) only RGB support 6,8 and 10 bit per pixel
Video clock frequency	dual pixel per clock 20~180 MHz
Audio	None
Link Training	Full/Fast/No Link Training Mode
Content Protection	Alternative scrambler seed reset Alternate framing mode
Electrical Signaling	4 peak-to-peak voltage swing and 4 pre-emphasis levels Receiver equalization (without adaptation)
EMI reduction	Support Spread Spectrum Clock and Scrambling
Channel coding (8B/10B)	DC-balancing (AC-coupled signals) Byte synchronization (K-character) Channel alignment (K-character) Packetize Frequency compensation (insert dummy)
AUX CH	1Mbps, Manchester II coding

2.3 DisplayPort Interface Architecture

2.3.1 Layered Architecture

As shown in Fig. 2.2, the interface is basically constructed as a layered architecture. It broadly comes in two layers that are a physical layer and a link layer. And the physical layer consists of electrical sub-blocks and logical sub-blocks. Even if the specification of the interface is advanced in the future, the physical layer may be replaced while the link layer remains unchanged. This allows the interface to develop along with the advanced technology to maintain its cost and performance.

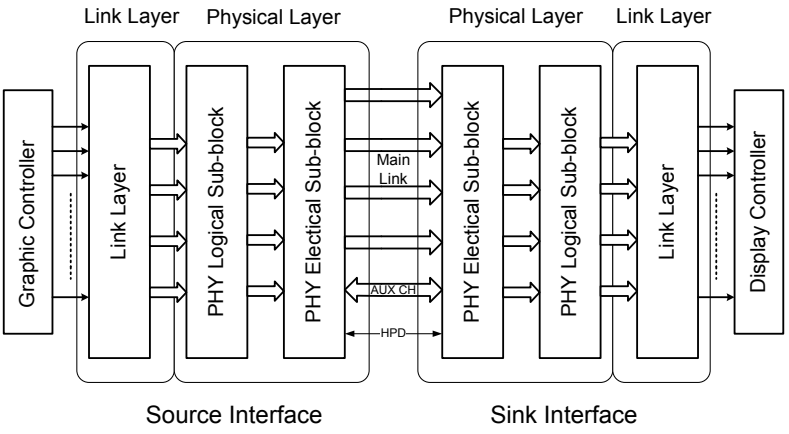


Fig. 2.2 Layered architecture of transceiver.

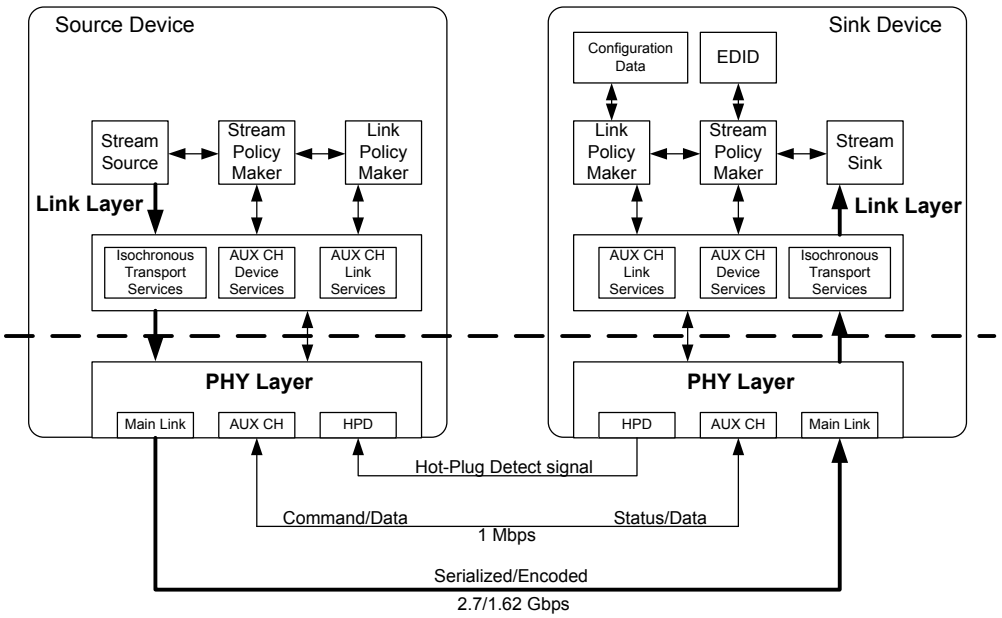


Fig. 2.3 Overview of layered architecture

The link layer is composed of isochronous transport services over the main link and link and device management services over the AUX Ch. The main link transfer the video and audio stream data which is mapped onto the main link symbols with a set of rules based on micro packet architecture. The transmitted data stream is correctly reconstructed into the original source format and timing information in the receiver device. AUX CH provides the link services and the device services. The transceiver exchanges the link and device configuration data through AUX CH. Link services are used for discovering, configuring and maintaining the link by read or write accessing to DisplayPort Configuration Data (DPCD) address. Device services

provide device-level applications such as Extended Display Identification Data (EDID) read and authentication for content protection.

The physical layer is divided into three categories of HPD, AUX CH and main link. HPD circuitry is responsible for both works. The electrical sub-block detects a Hot Plug/Unplug event and the logical sub-block notifies the events to the link layer. AUX CH circuitry is the half-duplex bidirectional channel and uses Manchester-II encoding with 1Mbps bandwidth. The electrical sub-block consists of a single differential pair which is equipped with driver and receiver for half-duplex bidirectional operation on both ends. AUX CH driver drives a terminated, AC-coupled differential compliant with the AUX CH electrical specification for the appropriate Manchester-II encoding. AUX CH receiver receives the input differential signal and reconstructs the original data by decoding. The logical sub-block generates and detects the transaction start/stop signals and locks to the synchronization pattern. Main link circuitry in the physical layer supports the transport of video streams and secondary-data packets including audio streams. The electrical sub-block consists of four differential pairs and the incoming differential signals and recovers the data and clock with its CDR circuits. The logical sub-block performs de-scrambling, 8b/10b decoding, de-serializing, link training, and link quality test for measurement. Then the 8-bit de-serialized and decoded data is delivered to the link layer for reconstruction of the original source video/audio data and timing information. Fig. 2.4 shows the summary of the functions of the layered architecture. The details of each function will be described in the next chapters.

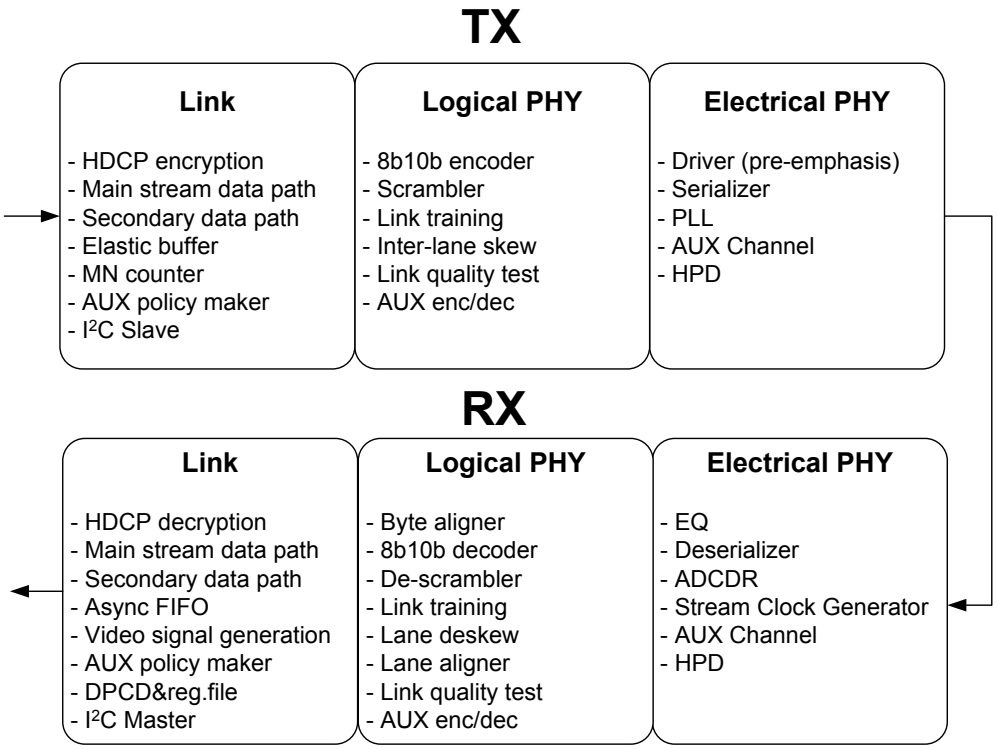


Fig. 2.4 Functions of the layered architecture.

2.3.2 Main Stream Protocol

The interface basically uses the packetized protocol to enable support for expansion with multiple data types, flexible allocation of available bandwidth between video and audio and multiple video streams over single physical connection. The main stream packetizing is made up of 4 fundamental mapping processes. They are packing/unpacking, stuffing/un-stuffing, framing/un-framing and inter-lane skewing/de-skewing. The receiver extracts the original source data from the transmitted packet by un-mapping process. Because the transmitted data is 8b/10b encoded, the k-character symbols which are the non-encoded special character symbols are used as the control symbols for packing, stuffing and framing. The main stream data reconstruction process on receiver side is simply illustrated in Fig. 2.5.

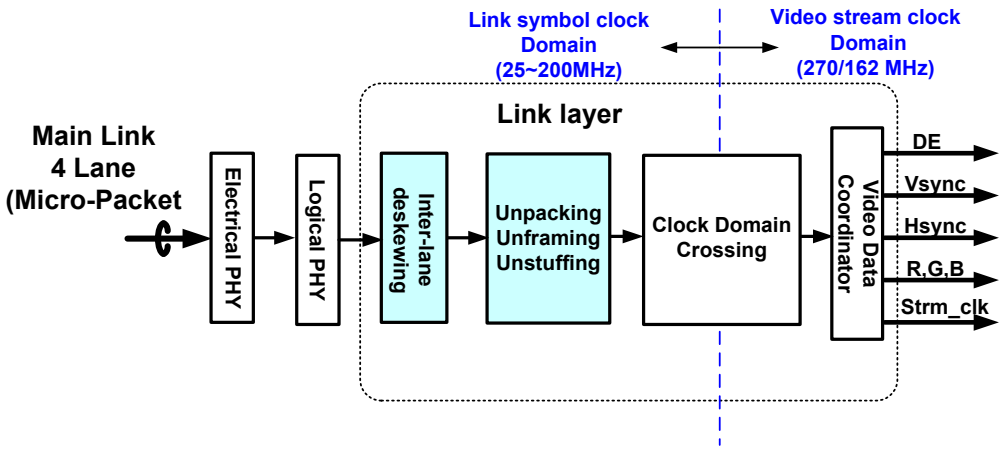


Fig. 2.5 Main stream data reconstruction process

First of all, the framing indicates the active data period and the blanking period. Thus, the framing is repeated every vertical and horizontal blanking period with the inserted blanking start (BS) symbol and blanking end (BE) symbol as shown in Fig. 2.6. BE is placed immediately before the first active pixel of video data only during the vertical display period and BS is inserted after the all active pixel data is transferred. During the blanking period from BS to BE, audio data streams and the secondary-data packets which are the information of the current video format are transmitted.

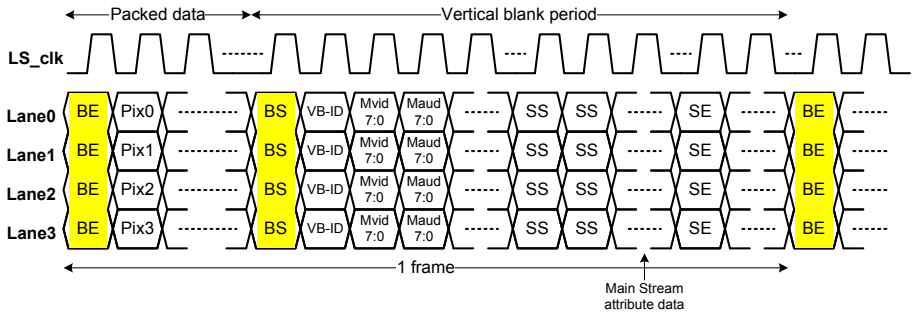


Fig. 2.6 Main stream data framing for a four lane main link.

The unit of the transmitted packet is called Transfer Unit (TU). Since the link symbol rate is fixed and the packed data rate varies depend on the video resolution, color depth and refresh rate, dummy data symbols must be inserted between Fill Start (FS) and Fill End (FE) as shown in Fig. 2.7. The packed data rate that is related to the video stream clock must be lower than the link symbol rate to prevent exceeding the maximum link bandwidth. By stuffing dummy symbols, the interface supports various display formats with the fixed link bandwidth.

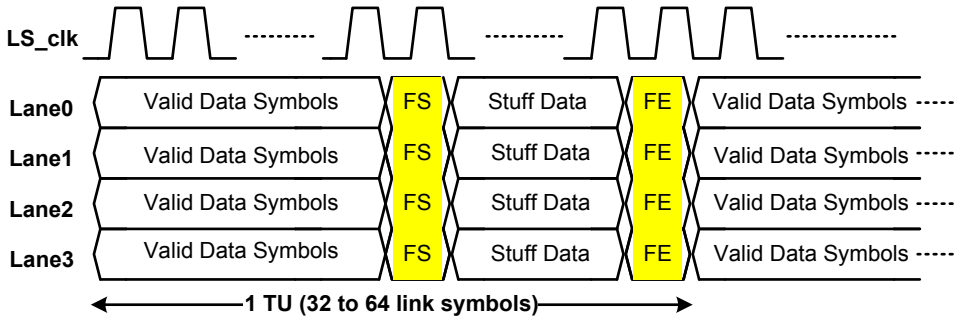


Fig. 2.7 Main stream data packing and stuffing for a four lane main link.

In order to increase the noise immunity of the main link, the transmitter insert a skew of two link symbol clock cycles between adjacent lanes. Fig. 2.8 shows how the symbols must be transported after inter-lane skewing. It prohibits the same symbols are corrupted at the same time by the external noise, so that the possibility of a corruption of important information is reduced.

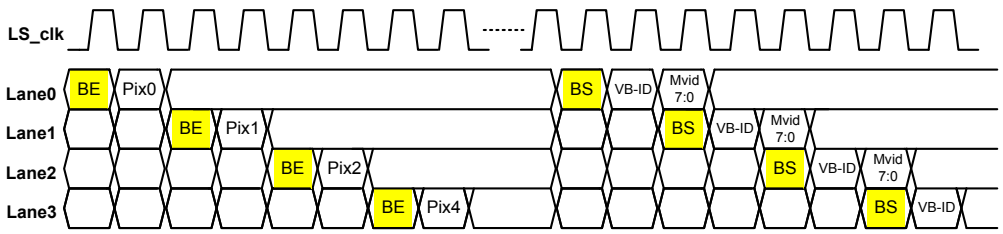


Fig. 2.8 Main stream data inter-lane skewing for a four lane main link.

2.3.3 Initialization and Link Training

When a source device has been connected to a sink device or disconnected from a sink device, HPD is used as a communication mechanism that makes the source device aware of connection. HPD instantiates a start-up communication sequence to the source device and the link is initialized. The source device access to the EDID and DPCD in the sink device and configures the link through link training. The link initialization and establishment is performed via AUX CH transaction.

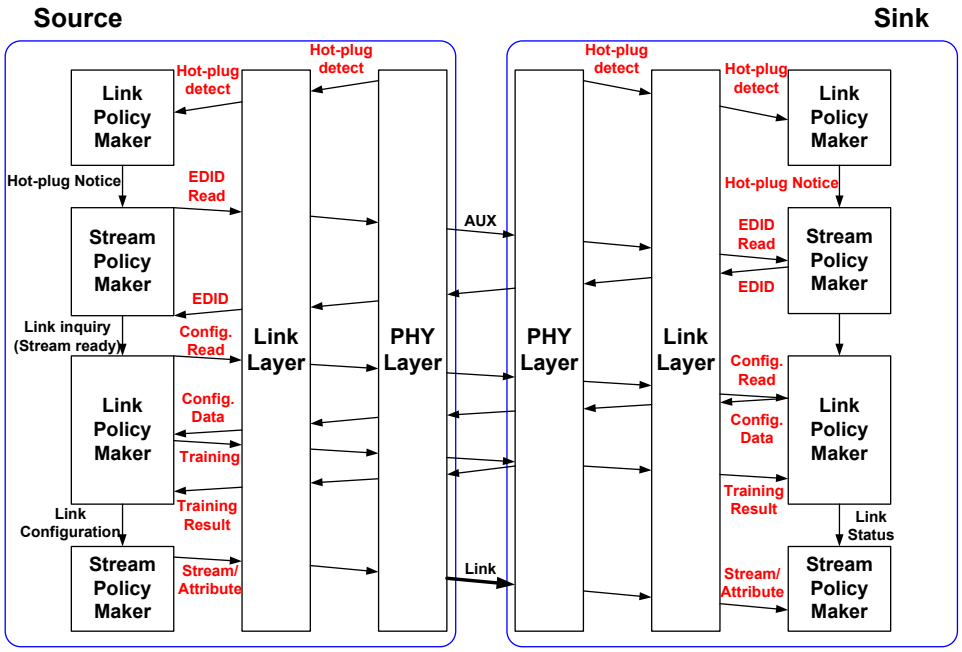


Fig. 2.9 Action flow sequences of the source upon HPD event.

Upon HPD signal detected, the source device read EDID in the sink device above all. EDID is a set of data physically stored in sink device that contains display information about the device supported features and capability. After that, the source device read the receiver capability field of the DPCD to discover the supported lane count and maximum bandwidth. The link training is started by set up the lane count and link rate for the current display. The link training consists of two distinct sequences that should be successfully completed to establish the link. The first sequence is the clock recovery sequence. The transmitted data in this sequence is a repetition of clock pattern (TPS1) at the minimum voltage swing level and pre-emphasis level. The source device waits for at least the period of time specified in DPCD field, usually 100 μs. Then, it checks whether the receiver finishes the clock recovery by reading the link status field in DPCD. If the clock recovery is not done, the transmitter increase the voltage swing level or the pre-emphasis level and try to send TPS1 again. When the clock recovery sequence is correctly ended, the transmitter starts the next sequence, the channel equalization sequence. In the channel equalization sequence the transmitter sends the repeated equalization pattern (TPS2 or TPS3) without scrambling. As the clock recovery sequence, the transmitter waits for at least the period of time specified in DPCD field, usually 400 μs and reads the link status field in DPCD to confirm the success of the link equalization. If not, it also raise the voltage swing level or the pre-emphasis level and transmit the equalization pattern again. The transmitter begins to send the normal video/audio data after all the link training sequences has been done successfully.

There are several cases that the source device terminate the transport of the main stream data and re-establish the link. If the stream timing or display format changes,

the transmitter requests the link re-training through AUX CH. This is the general case of the stream termination. However, there must be some abnormal events of the stream termination. When the loss of synchronization happens in the sink device, Interrupt Request (IRQ) signal is asserted by the receiver through the HPD pulse. After IRQ pulse is detected in the source device, the transmitter must start the link initialization sequence including the link training to establish the link again. Fig. 2.10 shows the process of the link establishment.

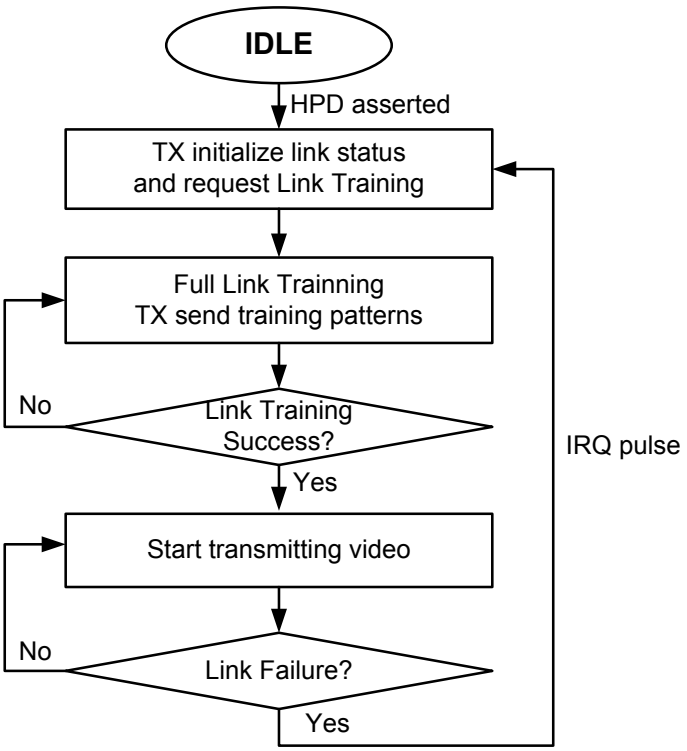


Fig. 2.10 Process of the link establishment.

All the process of the link establishment is carried out via AUX CH transaction. Since AUX CH is a half-duplex, bidirectional channel, the transmitter must initiate a request transaction and the receiver responds with a reply transaction. As shown in Fig. 2.11, the transmitter must transition to “Talk Mode” after the sink is noticed by HPD assertion and issue the request transaction. The transmitter needs to wait 400 μs for the reply from the receiver and the receiver must respond within a maximum of 300 μs to avoid time-out. Thus, the link initialization and link training sequence takes several milliseconds to finish all. Whenever the stream timing, display change or loss of synchronization happens, the link establishment has to be performed again. It raises discomforts in the sink device because the video image cannot be displayed well during this period. By shortening the time to establish the link, it can be improved. When the first link training has been succeeded, the last-well-known configuration must exist and the sequence of the link establishment can be simplified by omitting AUX CH transactions. Several methods implemented for reducing the link establishment time are detailed in the chapter 4.

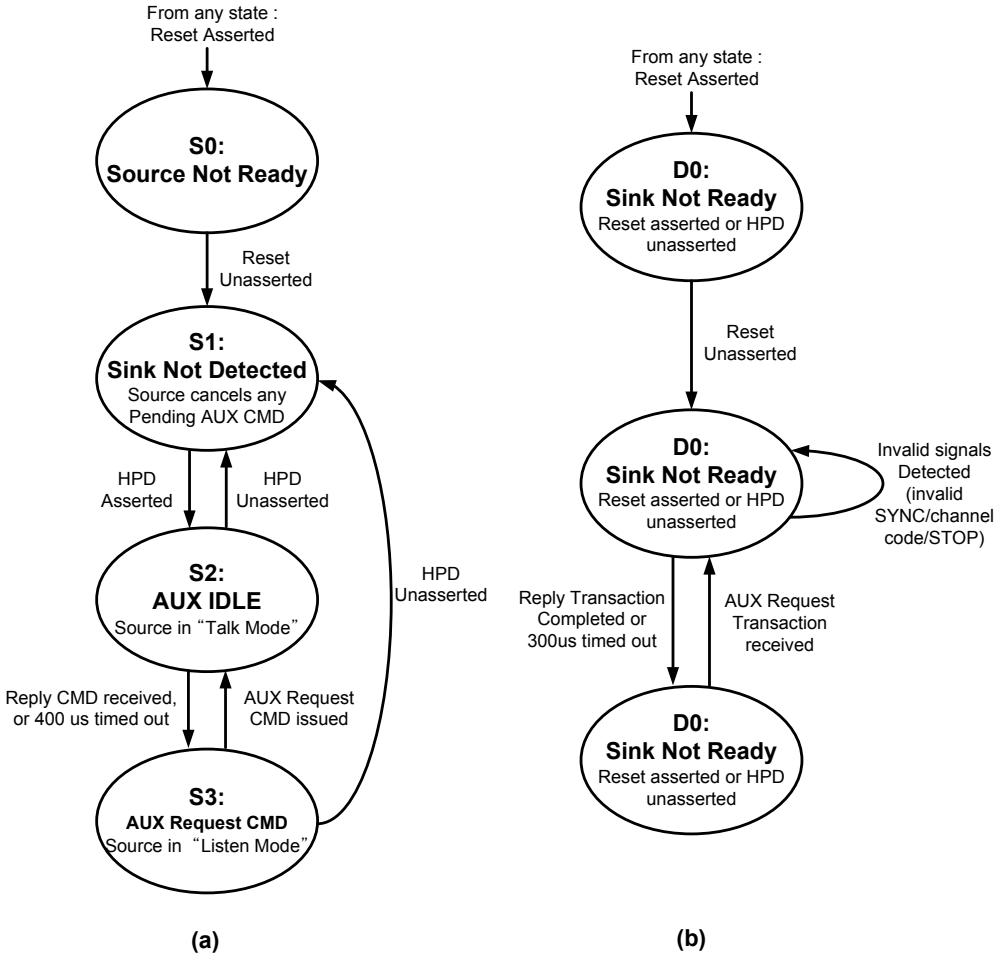


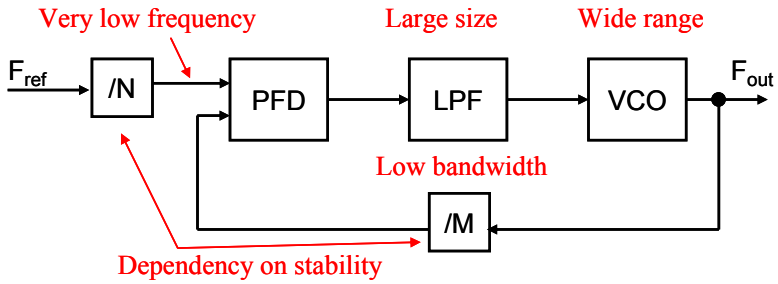
Fig. 2.11 AUX CH transaction state diagram : (a) transmitter (b) receiver.

2.3.3 Video Stream Clock Recovery

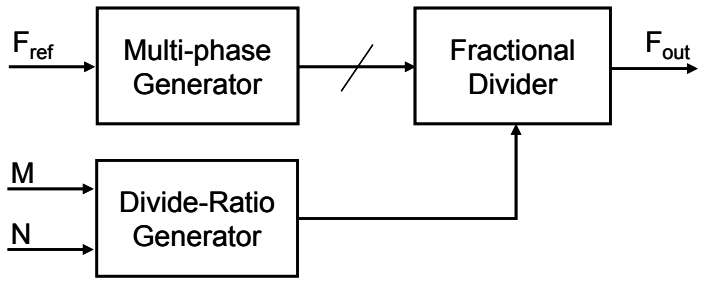
The video pixel clock is totally decoupled from the link rate. Thus, the video clock synthesis is essential to transfer the video data to display device. Due to the various resolution of the display format, different bit number for the color depth, and the different refresh rate, various clock frequencies have to be synthesized for each display. The video clock is regenerated from the link symbol clock using the time stamp values M and N which is transferred during the blanking period. Usually, integer-N phase-locked loop (PLL) is employed to generate the video clock frequency corresponding to the division number N and M as shown in Fig. 2.12 (a). Because the resolution of the clock generator depends on the input reference clock of the phase detector in integer-N PLL, input reference clock should be low enough to cover the frequency necessary to each display type. This decreases the bandwidth of the clock generator and results in large size loop filter and poor performances such as slow dynamics, high 1/f noise and large jitter. And moreover, the output clock frequency coupled to the input N and M may affect the stability of the feedback loop, therefore the design complexity of the clock generator is increased.

Fig. 2.12 (b) shows the conceptual block diagram of the circuit that accomplishes the same function of integer-N PLL. The output frequency is synthesized directly from a multi-phase clock by the fractional divider. The divide-ratio generator provides the appropriate division number to the fractional divider. The direct clock synthesizer decouples the tradeoff between the high resolution of output frequency and the fast frequency switching. Moreover, some advantages are expected due to the

fixed output frequency and the high bandwidth of the multi-phase generator. In this work, a finely spaced multi-phase generator and fine resolution fractional divider are adopted to synthesize a video clock instead of the integer-N PLL. With the proposed architecture, a high bandwidth clock synthesizer having low jitter performance can easily be designed provided that the resolution of fractional divider is high enough [32]-[34] .



(a)



(b)

Fig. 2.12 Video clock synthesizer (a) integer-N PLL (b) direct clock synthesizer with multi-phase clock.

The fractional divider used in this work is based on the phase switching technique proposed in [35]. When the phase switching technique is used, the glitch problem should be carefully handled. A spike-free buffer, reversed order switching and a retiming circuit were proposed to eliminate the glitch problem. [35]-[37]. However, k-times sequential phase switching events are required to complete the k steps of phase shift in most previous works. Such a step-by-step phase switching method has a critical demerit of the low fractional resolution when the integer part of the division number is small. Since the number of phase switching event is limited to the integer number, the fractional resolution cannot be enhanced beyond the integer number. A method disclosed in [38] solves the problem of sequential phase switching with switching the total amount of phase shift at a time. But the timing critical control circuit used for glitch free phase switching has little timing margin when the fractional resolution is high because the control circuit exploits the time gap between the two adjacent clock phases as a setup time of the next sampling circuit and clock to output time of the current sampling circuit. In the proposed architecture, the glitch-free phase switching can be achieved simply by delaying the multi-phase aligned clocks for a few cycles.

Once the video data is extracted from the received packet, it must cross the clock domain from link symbol clock to video pixel clock. An asynchronous FIFO memory is inserted between the completely decoupled clock domains to deliver the video data. Fig. 2.13 shows the overall block diagram of the video clock synthesis and clock domain crossing. To compensate the error of the transmitted M value which is the potential frequency offset source, the proposed scheme is included in the design. The frequency error makes serious problems in FIFO operation which

cause data to be lost due to FIFO overflow or invalid data to be read from the FIFO due to an attempt to read the same data again. The proposed frequency synthesizer employs FIFO monitoring scheme and compensate the M value to make up the video clock frequency correctly. The details of the proposed scheme are described in the chapter 5.

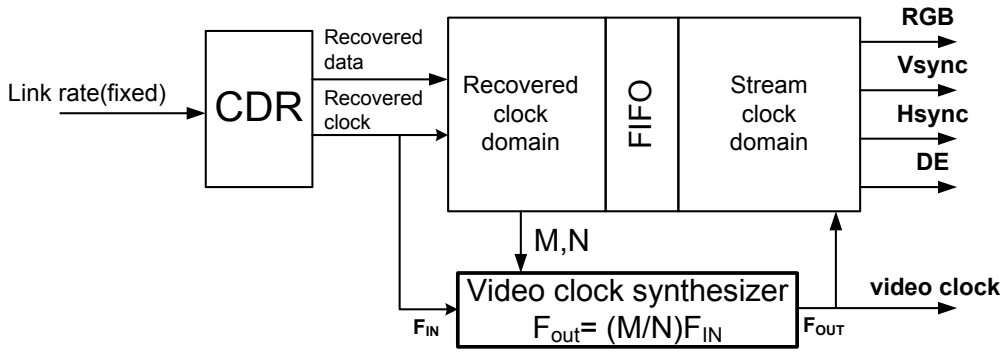


Fig. 2.13 The overall block diagram of video clock reconstruction and clock domain crossing

Chapter 3

Design of DisplayPort Receiver

3.1 Overview

The first design aims to deliver the video and audio data from DisplayPort source device to HDMI display device. Both the DisplayPort receiver and HDMI transmitter is included inside the prototype chip. The data stream from the DisplayPort source device comes into the DisplayPort receiver and the reconstructed video/audio data and clock are passed on to the HDMI transmitter. The chip can be used as the bridge to hook up the devices which support different display standards.

Fig. 3.1 shows the usage of the prototype chip in the display transport system. The source device such as a PC motherboard or a graphic card that contains DisplayPort transmitter sends the video/audio data stream through the DisplayPort cable. The video/audio data, clocks, and video timing signals which are reconstruct-

ed by the DisplayPort receiver delivered to the HDMI transmitter. It connected to the HDMI display sink device with HDMI cable. In short, the design performs the interface media conversion from the incoming DisplayPort stream to the outgoing HDMI stream. The chip consists of a DisplayPort receiver, a HDMI transmitter, a power management block, an audio conversion module, a HDCP key rom, a EDID rom and a local host I^2C module.

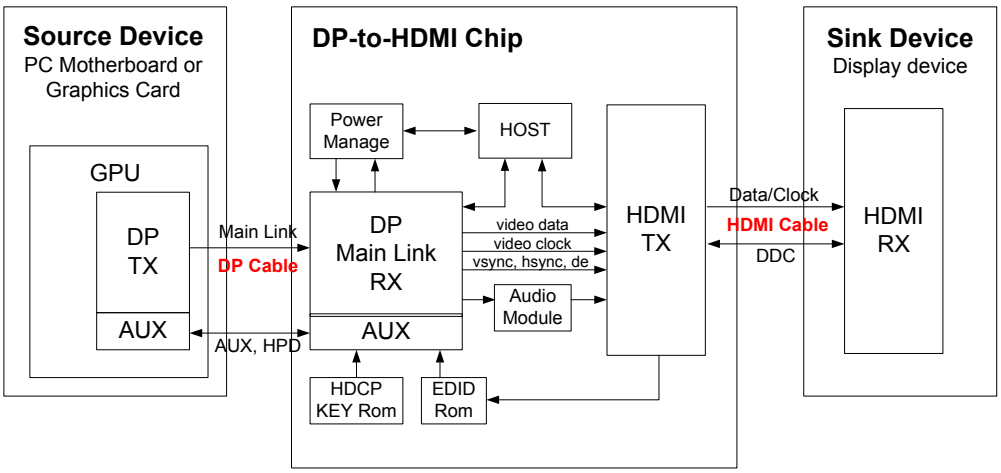


Fig. 3.1 The usage of the first design as a DisplayPort-to-HDMI converter.

The target video format supported is defined as follow: the maximum resolution is up to 4096×2160@30Hz in 2D format and the minimum resolution of the display is 640 ×480@60Hz. The video pixel clock frequency range is from 25 MHz to 350 MHz. Interlaced video format and primary 3D video and secondary 3D video format

timing are supported. The supported color depth is 8, 10 and 12-bit per color and RGB and YCbCr 4:4:4/4:2:2 color spaces are supported. The design has two buses to support audio inputs, four Inter-IC Sound (I^2S) inputs and Sony/Philips Digital Interconnect Format (S/PDIF) inputs. The audio clock is supplied by the integrated audio stream clock generator which is designed as same as the video frequency synthesizer. The I^2C and S/PDIF interfaces support sampling frequencies of 44.1, 48, 64, 88.2, 96, 176.4 and 192 KHz and data bit support 16, 20 and 24 bit. Audio mute is supported with P bit re-calculation and audio fade-in, fade-out are supported for Linear Pulse Code Modulation (LPCM) stream. Video and audio data are combined into an HDMI-compliant stream for output over the three TMDS output data pairs.

The DisplayPort receiver has several clock domains of link symbol clock, video stream clock, AUX CH clock, audio stream clock and so on. Table 3.1 shows a specific description on clock domains in the design. The link symbol clocks are recovered from the incoming data stream by ADCDR circuits. The serial data stream is de-serialized into 10-bit data, so that the link symbol clock used inside the design is 1/10 of the link rate. Since each lane has an independent ADCDR circuit, four recovered clocks are extracted and the received data in all lanes are aligned with the representative clock which is usually the recovered in lane 0. The two frequency synthesizers are included in the design. The architectures of them are basically the same but the output frequency is different according to the supported video/audio formats. Host clock and GPIO clock are incoming externally from outside of the chip. An internal oscillator to generate AUX CH clock of 16 MHz is included in the design.

Table 3.1 Clock domains in the first design.

Name	Description
link symbol clock	Recovered link symbol clock from ADCDR. Clock frequency: 162MHz, 270MHz, 540MHz
video stream clock	Stream clock. Clock frequency: 25MHz ~ 350MHz, which depends on video format.
audio stream clock	Audio clock. Clock frequency: 16.384MHz(32kHz x 512) ~ 98.304MHz(192kHz x 512).
Host clock	External 16MHz clock for a local host I^2C Clock frequency: 16MHz.
AUX clock	Auxiliary channel clock. Clock frequency: 16MHz (Min: 12MHz, Typ: 16MHz, Max: 20MHz)
GPIO clock	External GPIO channel clock. Clock frequency: upto 80MHz

3.2 Physical Layer

The physical layer connects a physical medium of DisplayPort cable to the link layer of the sink device. It decouples the data transmission electrical specifications from the link layer. It is further sub-divided into electrical and logical functional sub-blocks. The overall block diagram of the physical layer is illustrated in Fig.3.2. In the electrical part, four ADCDR circuits are placed on the individual lanes for recovering link symbol clocks from the incoming differential signals. A video/audio clock generator synthesizes a video/audio stream clock with the recovered clock and time stamp values extracted from the data stream. AUX CH and HPD circuitry are included and on-chip oscillator generates a 16 MHz clock.

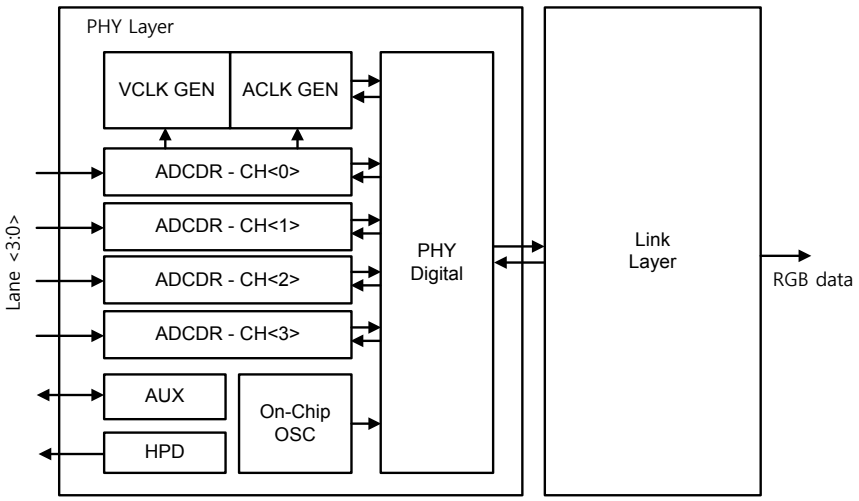


Fig. 3.2 Block diagram of physical layer

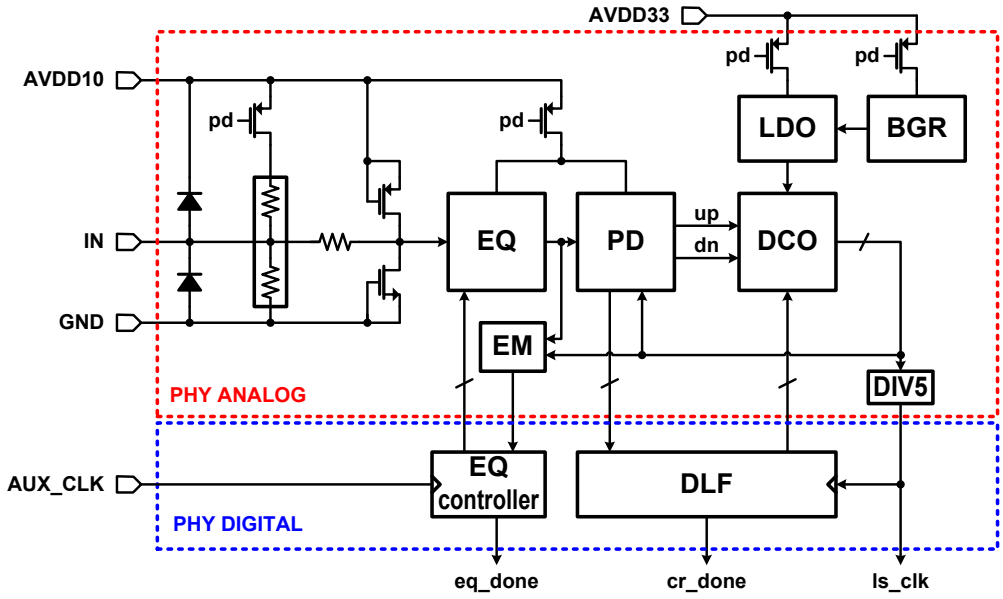


Fig. 3.3 ADCDR architecture

Fig. 3.3 shows the architecture of the ADCDR, and the equalization circuit (EQ) with the eye opening monitor (EM) scheme on the front end of each lane. On-chip termination resistors and ESD protection network with diodes and clamp circuits are placed in front of the equalization circuit. The ADCDR adopts a half-rate architecture as it relaxes the required clock frequency for a given bit rate. The phase detector (PD) which is a half-rate bang-bang type detects the phase difference between the incoming data stream and the recovered clock from a digitally-controlled oscillator (DCO). The PD output delivered to the DCO along proportional and integral paths. The error signals are directly carried into the DCO so that the phase error is correct-

ed promptly. The integral path which is implemented with a digital loop filter (DLF), accumulates the phase errors for tracking the frequency. The DCO generates half—rate 8-phase clocks which are fed back to the half-rate bang-bang PD for phase comparison and one of the output clock divided by 5 to generate a link symbol clock for the link layer operation [39].

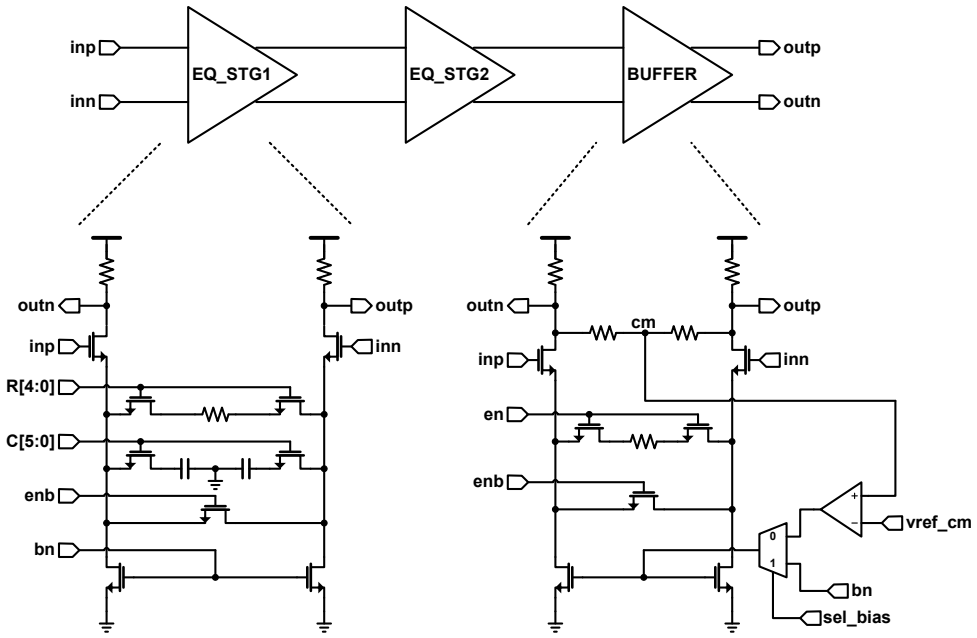


Fig. 3.4 Equalization circuit.

The equalization circuit is composed of two stages plus a buffer for adjusting the common mode voltage of the output signals. Each stage is a fairly conventional continuous time linear equalizer with a RC source-generated differential structure. The

amount of degeneration is controllable by adjusting the resistance and the capacitance [40]. The circuit implementation of each stage is presented in Fig. 3.4. The control bits of the resistance and the capacitance are adaptively adjusted by the eye monitoring scheme which is shown in Fig. 3.5. The differential output data are compared with differential reference levels by the differential flip-flips and XOR gates. The polarities of outputs of the flip-flops contain the information of the monitored eye levels and the strength of the equalization stage is controlled until the result of the eye opening monitor is satisfied with the reference voltage conditions [41]. Fig. 3.6 shows the adaptive control operation in the equalization stages.

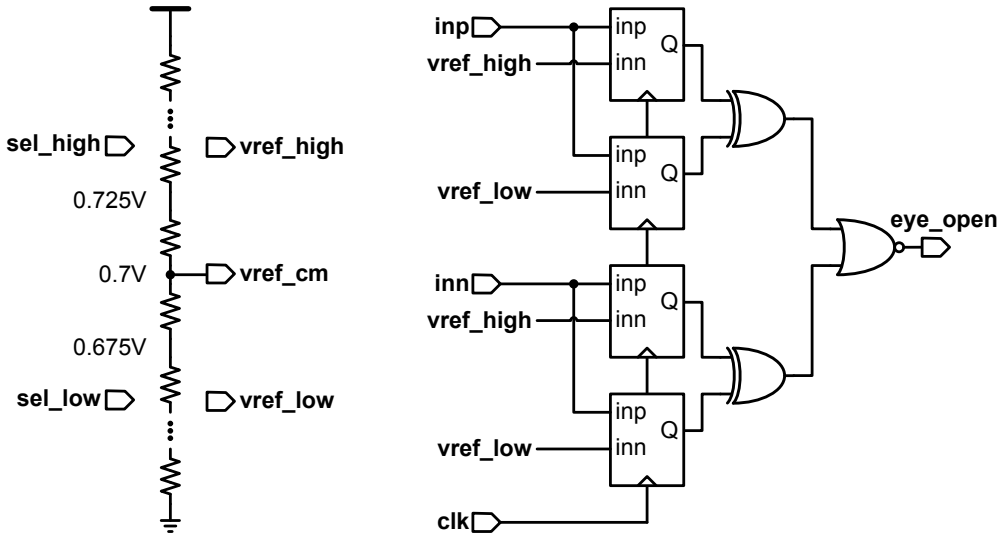


Fig. 3.5 Eye opening monitor scheme.

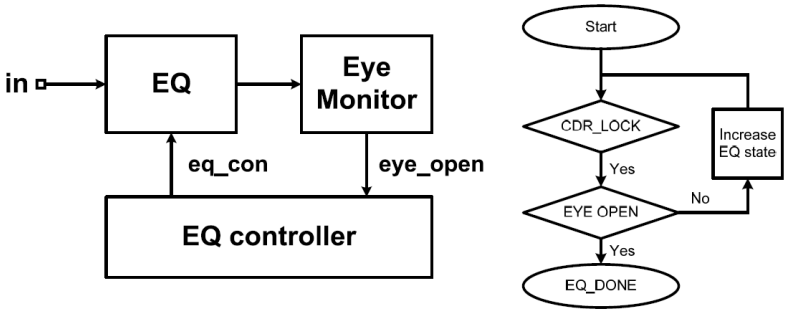


Fig. 3.6 Operation of the adaptive equalization.

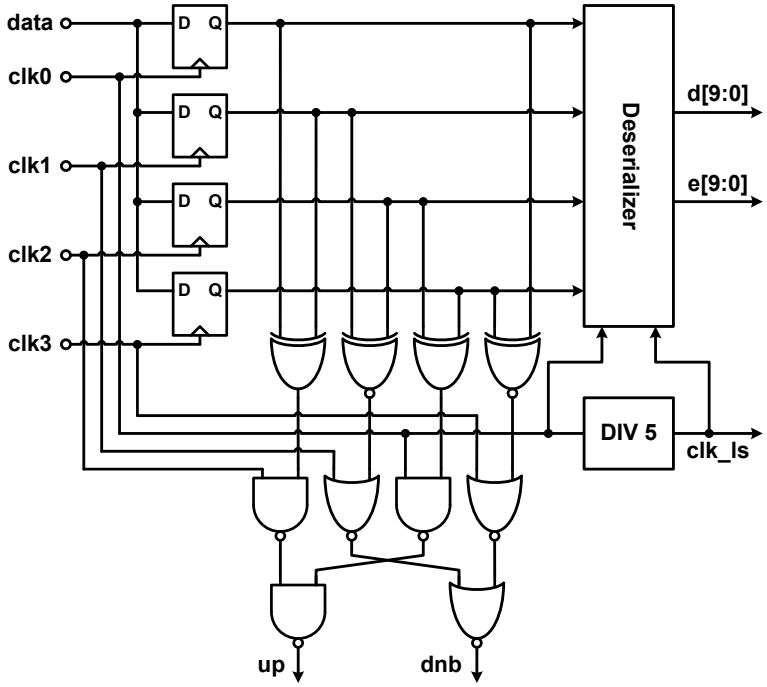


Fig. 3.7 Half-rate bang-bang phase detector..

The circuit implementation of the half-rate bang-bang PD is shown in Fig. 3.7. The incoming data is sampled by the multiphase clocks from the DCO and the phase errors are provided by XOR operations of the data sampling and the edge sampling. The result of full-rate error signals are forwarded directly to the DCO as the proportional path control [42]-[47]. Also the phase errors are de-serialized and synchronized with the divide-by-5 clock of the recovered half-rate clock and delivered to the DLF as the integral path control. Finally, the 10-bit de-serialized data and the recovered link symbol clock which is 1/10 of link rate are delivered to the link layer. The de-serializer used in this design is presented in Fig. 3.8.

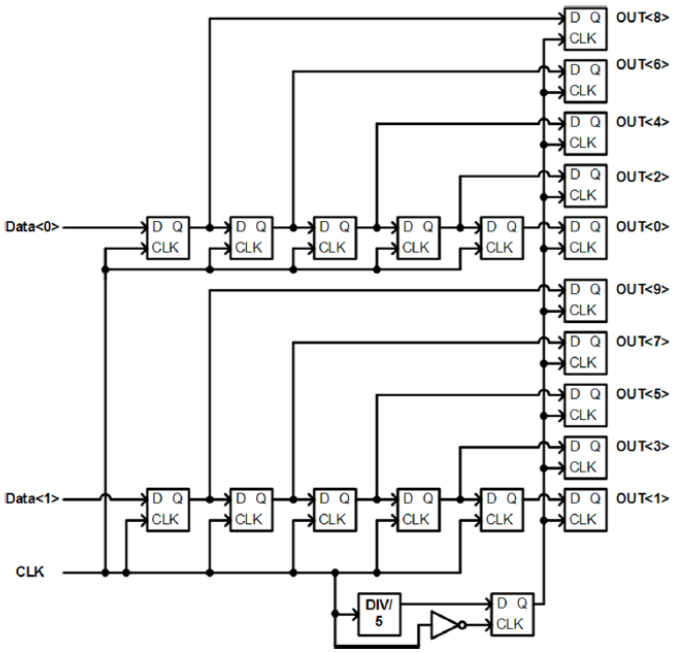


Fig. 3.8 2:10 de-serializer.

The DCO is four-stage ring type oscillator using a pseudo-differential inverter chain. It consists of a digitally-controlled resistor (DCR), delay elements with varactor loads, and level converters. It has triple modes wide-range to support 1.62, 2.7 and 5.4 Gb/s link rates. The strength of the inverter unit is scalable depends on the link-rate selected. The frequency of the output clock is controlled by the integral path control word by alters the resistance of the DCR so as to vary the supply voltage of the core oscillator. The phase errors from the proportional path control the varactors which are composed of NMOS transistors with sources and drains tied together. They varies the loading capacitance of the inverter outputs, thereby the phase tracking can be achieved.

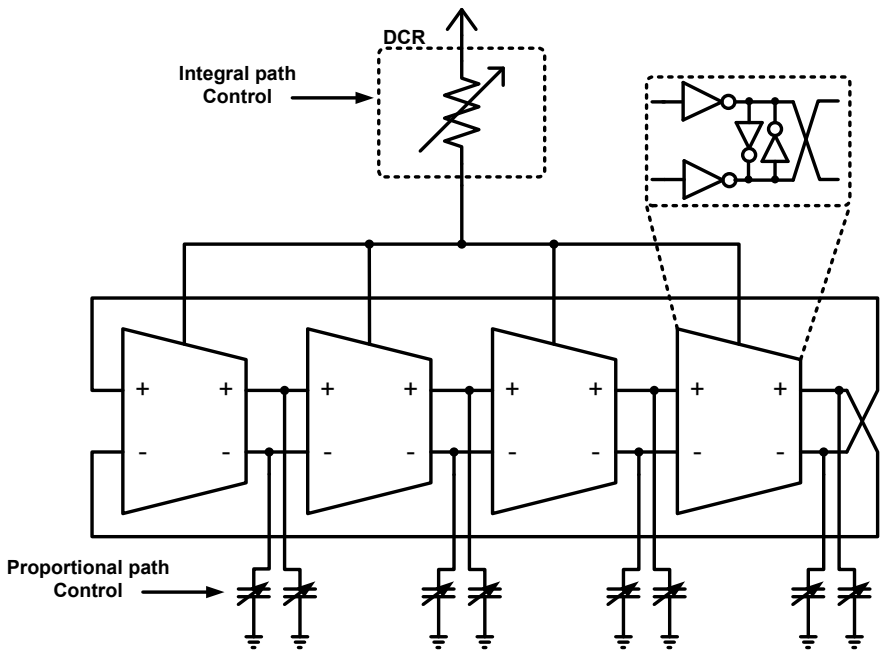


Fig. 3.9 Digitally-Controlled Oscillator.

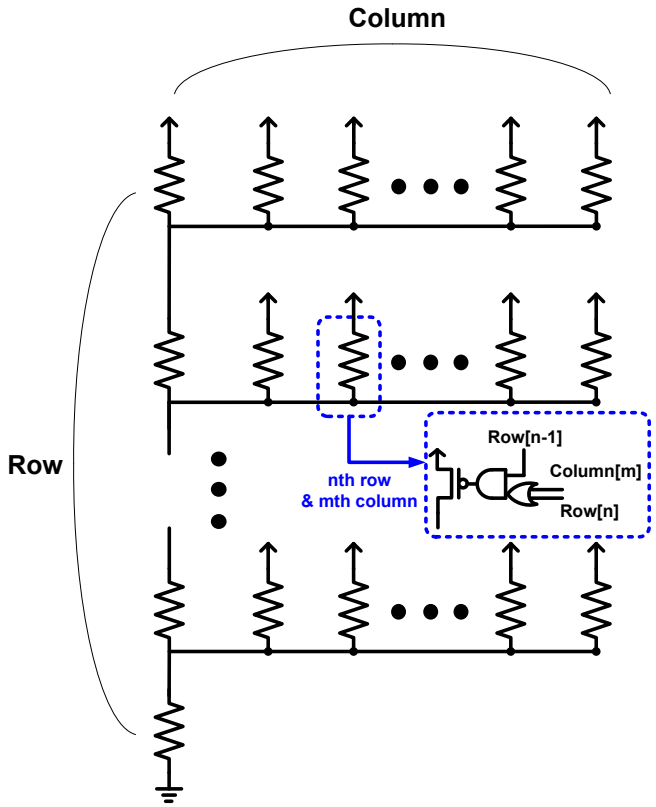


Fig. 3.10 Digitally-Controlled Resistor.

Fig. 3.10 shows the linear DCR scheme. It consists of a row decoder, a column decoder, and a series variable resistor. It achieves reduced switching noise and monotonic frequency characteristics. Segmented thermometer codes are used for minimizing glitch during control codes transition [48]. The control codes for adjusting the resistance are generated by decoding the integral word from the DLF. The total of 31-bit column and 31-bit row codes are generated from the 11-bit integral word.

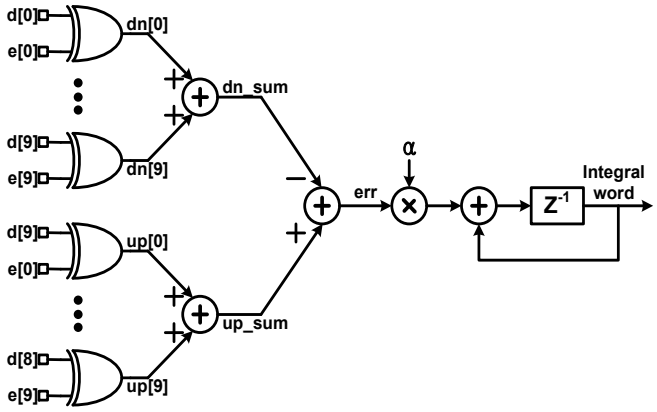


Fig. 3.11 Digital Loop Filter.

The DLF which is used as the integral path control for the output frequency of the DCO is illustrated in Fig. 3.11. The de-serialized phase errors, generated by sampling the data and edge of the incoming data in the half-rate bang-bang PD, are accumulated and dithered by a first-order delta-sigma modulator (DSM). The integral path gain is determined to satisfy the loop bandwidth specification. The 11 MSBs of the accumulator delivered to the DCR for adjusting frequency of the output clock. DSM effectively reduces the integral step. Since DLF is entirely implemented with digital circuits, it has the advantages of resolving leakage problems of poor switching and capacitors, and achieving a low integral gain with a small area, in contrast to the analog RC filters used in Charge-Pump PLL (CPPLL).

An internal oscillator to generate 16 MHz clock is illustrated in Fig. 3.12. Comparator-based relaxation oscillator is adopted to generate the clock signal. The circuit is composed of a feedback loop including comparators, RC circuit and SR latch. The operating frequency is controllable by adjusting the register sets.

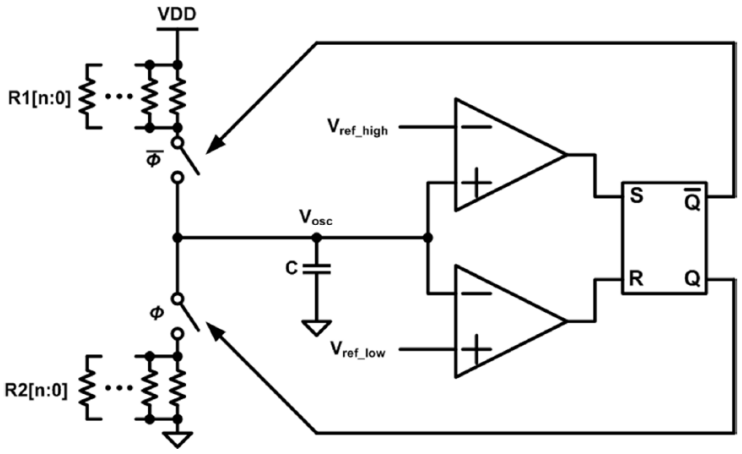


Fig. 3.12 Internal Oscillator.

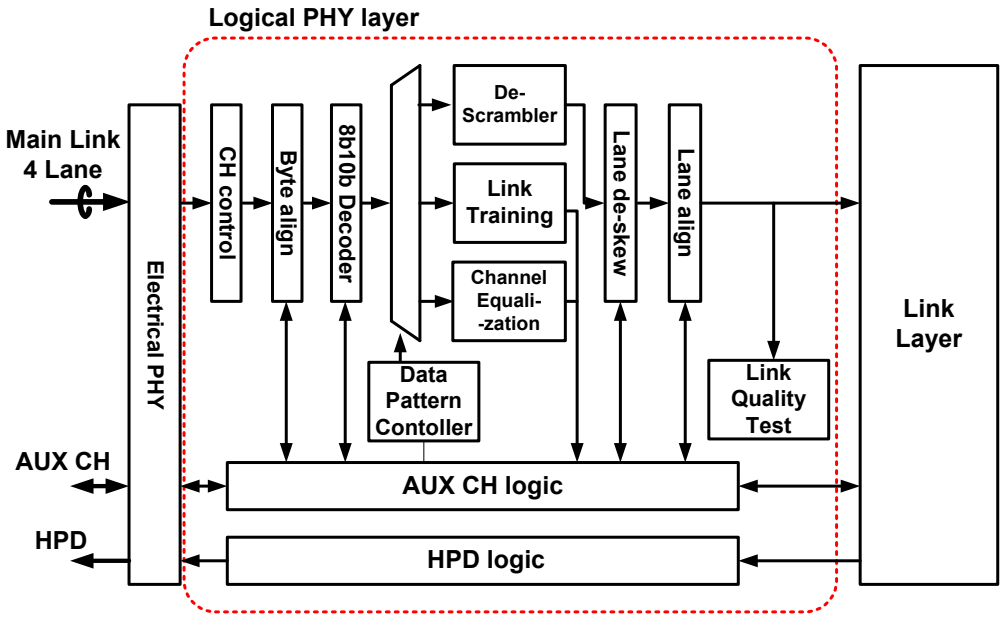


Fig. 3.13 Block diagram of logical PHY layer

Fig. 3.13 shows a block diagram of logical sub-blocks of the physical layer. The logical PHY layer receives de-serialized 10-bit data stream from the electrical PHY layer, handles link training with AUX CH and sends decoded and aligned raw data to link layer. The functional descriptions of the logical sub-blocks are defined as follow. A channel (CH) control module handles miscellaneous jobs based on register configuration. For a received de-serialized 10-bit data stream from the electrical PHY layer, the function block applies lane swapping between lane0, lane1, lane2 and lane3. The module also provides additional features of polarity inversion and bit ordering reverse on a specific lane with user configuration. A byte align module aligns de-serialized 10-bit parallel data using pre-defined special k-character codes of 8b/10b encoding. A 8b/10b decoder recovers 8-bit data of sender for a encoded data by transmitter. The 8b/10b encoding aims to ensure sufficient data transitions and DC balancing for clock and data recovery. A de-scrambler recovers original message with a pre-defined linear feedback shift register (LFSR) for manipulated data by scrambler of transmitter. Link training and a channel equalization module check errors in the pre-defined pattern during the link training and channel equalization process and establish the link by synchronizing recovered symbols. The transmitter adds intentional skew to data of individual lanes to prevent interference. A lane de-skew block adjusts this skews between adjacent lanes, which makes original data pattern. After inter-lane de-skewing, a lane align module cancels skew between each lane by comparing k-characters. The outputs of the logical PHY layer are totally aligned by this module. A link quality test module is used for measuring the link quality by handling pre-defined link test patterns. The supported measurements are recovered link clock quality measurement and link symbol error rate measurement

with the test patterns of un-scrambled nyquist pattern, symbol error mesurement pattern, PRBS7 bit pattern, custom 80 bit repeating pattern and High Bit Rate 2 (HBR2) compliance EYE pattern.

The PHY layer testability is operated with link quality test module. The link quality test module can calculate symbol error rate by its supported measurement scheme. When a symbol error rate measurement pattern is transmitted to the source device, the sink device starts increasing the symbol error count of each lane in each time. Once the sink device starting to check the symbol error, the source device should read the counted error value after a specific time, thereby it can calculate the approximate symbol error rate. The symbol error rate is calculated as Table 3.2.

Table 3.2 Symbol Error Rate calculation.

Data rate	Equation
5.4Gbps	Symbol Error Rate in units of 10^{-9} = Error_Count/(0.54*Measurement Period in Second)
2.7Gbps	Symbol Error Rate in units of 10^{-9} = Error_Count/(0.27*Measurement Period in Second)
1.62Gbps	Symbol Error Rate in units of 10^{-9} = Error_Count/(0.162*Measurement Period in Second)

The physical layer testability is also supported with internal automatic test equipment (ATE). With this test scheme, user can check bit error rate for a predefined PRBS or custom 80bit test patterns. When the external source device sends the measurement pattern, the sink device can detect bit error status of each lane for this dedicated test mode. The test result can be checked when the register status is set to high.

3.3 Link Layer

3.3.1 Overall Architecture

The link layer operates at 540, 270 and 162 MHz of link symbol clock according to the selected link rate. It provides services of discovering, configuring, and maintaining the link by accessing DPCD via AUX CH. The aligned 10-bit data stream from the physical layer delivered to link layer to extract video/audio data and the information for video timing and clock generation. The overall architecture of the link layer is illustrated in Fig. 3.14.

When the content protection is supported, the data stream is decrypted by a HDCP decryption module first. The main stream packet contains active data, main stream attribute data, secondary data and dummy data. An un-framing controller classifies the incoming data by detecting control symbols ahead the packet. The active video data is reconstructed as the pixel data corresponding to the video format, color depth and color space. Since it has to be converted into the video pixel clock domain, a FIFO is used for clock domain crossing. The FIFO used in this design is dual line buffer and operate with double buffering scheme. During writing one horizontal line data on the link symbol clock domain, the other line is read by the main stream sink module with the video stream clock which is generated by the stream

clock generator. The size of the FIFO is 4096×36×2 bit to support 4K video resolution with 36-bit/pixel color depth.

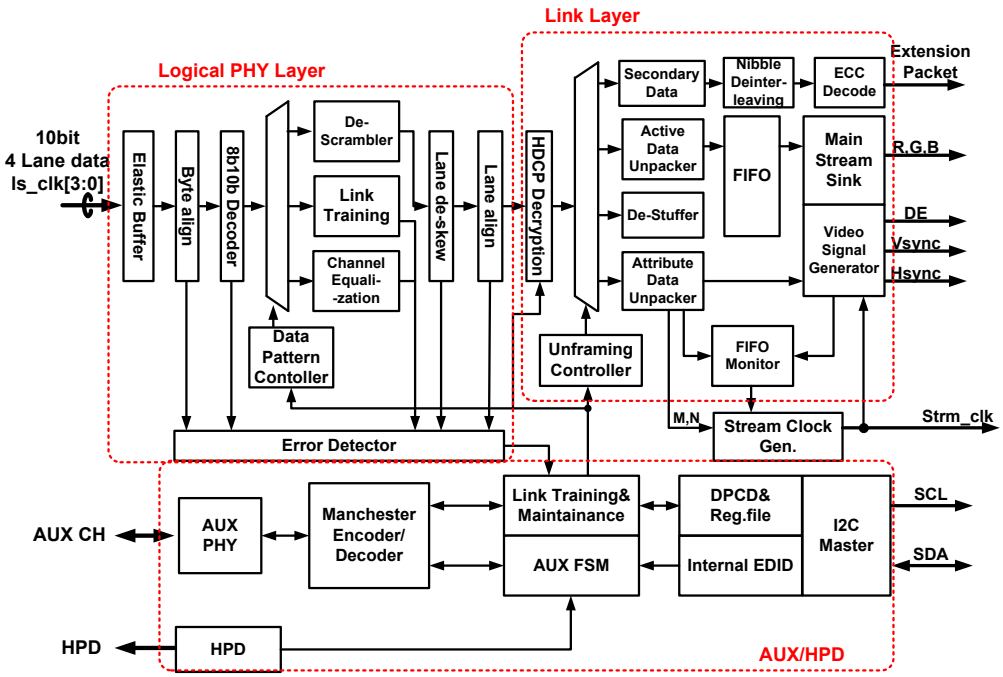


Fig. 3.14 Overall Architecture of the link layer

A de-stuffer eliminates dummy data included in the main stream data packet. Usually, dummy data symbols are inserted in all lanes during packing the data stream in the transmitter because the pixel data rate is equal to or lower than the link symbol rate. The dummy data symbols are inserted both between FS and FE, and between BS and BE. It can be detected by the un-framing controller and delivered to

the de-stuffer to be removed. In the blanking period, main stream attribute data packet and secondary data packet including audio data stream are transported. The main stream attribute data contains the information of video timing and clock regeneration. The time stamp value M and N for synthesizing the video stream clock, the length and polarity of horizontal synchronization (Hsync), vertical synchronization (Vsync) and data enable (DE) signals. A attribute data un-packer extracts these information and send them to the video signal generator to reconstruct Hsync, Vsync and DE signals. The video timing generation scheme will be explained in section 3.3.4. The secondary data packets are delivered to the audio stream path and it will be discussed in section 3.3.6.

3.3.2 AUX Channel

AUX CH transaction is performed with Manchester II code for the self-clocked transmission of signals. Whenever the request transaction is started by the transmitter, pre-charge signals which are 10 to 16 consecutive 0's in Manchester II code are transmitted. After pre-charging a common mode voltage, AUX sync pattern is sent with 16 consecutive 0's in Manchester II code. There are 26 to 32 consecutive 0's in total including active pre-charge pulses. At the end of the AUX sync pattern, high for a two bit period which is 2 μs with bit rate of 1Mbps and low for a two bit period to notify the receiver end of the sync pattern. The data transaction is driven according to the AUX CH syntax following the sync pattern. STOP condition must be asserted at the end of the data transaction and the transmitter releases AUX CH immediately after the STOP condition. For the receiver, the reply transaction is performed with the same sequences.

Fig. 3.15 shows the sampling method of the AUX Sync pattern. Basically, the AUX CH logic in this design uses oversampling topology for receiving and transmitting the AUX CH transaction. A 16 MHz clock from an internal oscillator is used for sampling sent data. It must be considered to be tolerant of +/-20% of frequency offset between the transmitter and the receiver and 0.05UI cycle-to-cycle jitter. During sampling the sync pattern, the frequency offset calibration logic adjusts the oversampling rate of the received data. It measures the moving average of periods of the consecutive zero pattern which is clock pattern in Manchester II code and compensate the frequency offset between the transmitter and the receiver to recover the data

transaction correctly. A pulse less than three periods are removed and noise before the sync pattern started are ignored as it detected an error. The oversampling and calculation of the moving average of the received data is illustrated in Fig. 3.16. As a result, more than +/-30% of frequency offset can be covered by this architecture.

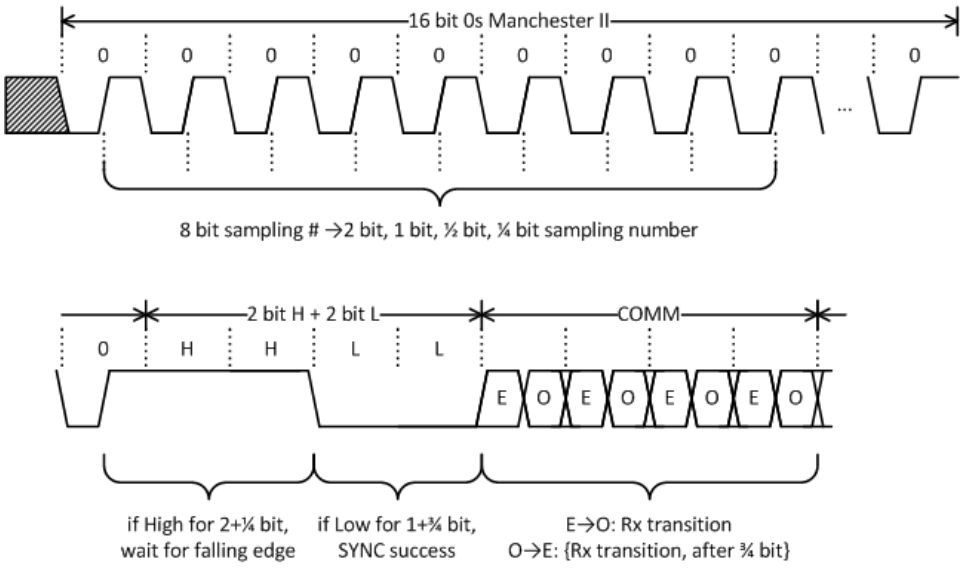


Fig. 3.15 Sampling of the AUX Sync pattern

AUX CH services are classified two types, link services and device services. The link services include a link capability read, link configuration, link training and link status read. The device services include EDID read and Monitor Command and Control Set (MCCS) control. The nested transactions are not possible. Thus, one

transaction must be finished before another transaction can be started. AUX CH syntaxes are categorized by two types. One is native AUX CH syntax which is used for accessing DPCD field inside the receiver to provide link services. And the other is I^2C-over-AUX syntax that is used for reading external EDID to serve device services. The data transaction after the pre-charging and sync pattern consists of command, address and data. In case of I^2C-over-AUX transaction, I^2C command, address and data are mapping onto the AUX CH transaction and the AUX CH is just used as the repeater to deliver the I^2C transaction from a master in a source device to a slave in a sink device.

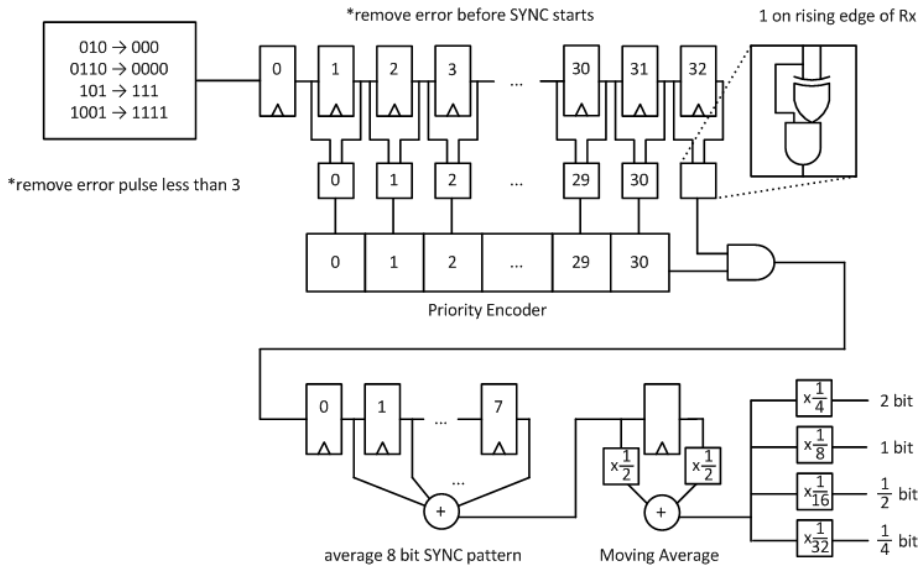
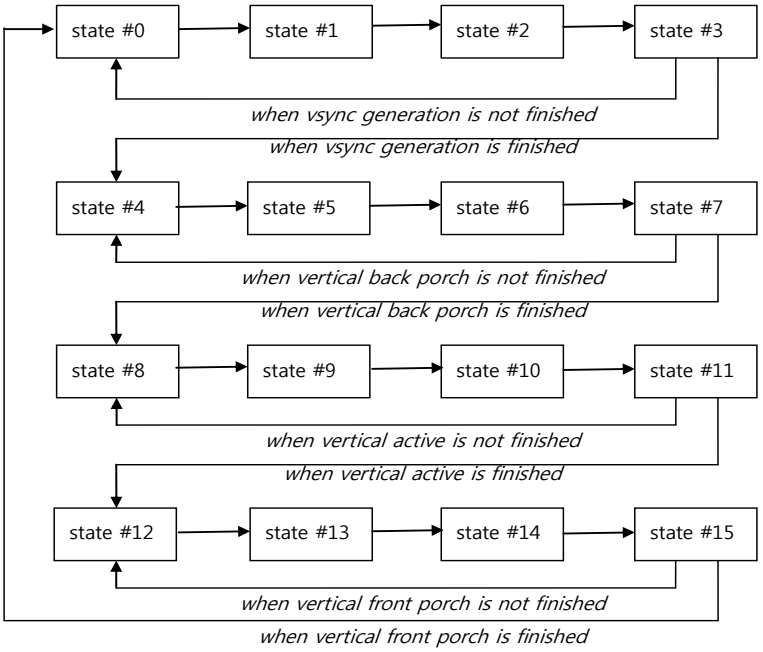


Fig. 3.16 Oversampling and moving average.

3.3.3 Video Timing Generation

In the sink device, video timing signals are reconstructed as well as the video pixel data. The information on Hsync, Vsync and DE signals are contained in main stream attribute data which is transmitted during the vertical blanking period of the main video stream. The un-packed main stream attribute data is delivered to the video timing generator. It contains horizontal and vertical totals of the transmitted main video stream, in pixel and line counts, respectively. Also, horizontal and vertical active start from the leading edges of Hsync and Vsync in pixel and line counts is included. Sync pulse width and polarity of Hsync and Vsync is contained as well.

The state-machine of video timing generation is presented in Fig. 3. 17. Each state has a counter to generate the corresponding timing signals that defined in the state definition. The counter value of each state is calculated based on the extracted information from the main stream attribute data. Only the state 10 is period of the active data transmission and another states are considered as horizontal or vertical blanking periods. Thus, DE signal is only asserted in the state 10 and the FIFO read for sending the pixel data operates during this period. The modified state machines that have some additional states are used for the interlaced video and 3D stereo video formats, but they are also based on counting the timing information which is obtained by un-packing the main stream attribute data.



state definition

- **state 0: horizontal sync & vertical sync**
- **state 1: horizontal back porch & vertical sync**
- **state 2: horizontal active & vertical sync**
- **state 3: horizontal front porch & vertical sync**
- **state 4: horizontal sync & vertical back porch**
- **state 5: horizontal back porch & vertical back porch**
- **state 6: horizontal active & vertical back porch**
- **state 7: horizontal front porch & vertical back porch**
- **state 8: horizontal sync & vertical active**
- **state 9: horizontal back porch & vertical active**
- **state 10: horizontal active & vertical active**
- **state 11: horizontal front porch & vertical active**
- **state 12: horizontal sync & vertical front porch**
- **state 13: horizontal back porch & vertical front porch**
- **state 14: horizontal active & vertical front porch**
- **state 15: horizontal front porch & vertical front porch**
- **state 16: idle**

Fig. 3.17 State diagram of video timing generation

3.3.4 Content Protection

Recently, the content protection is recommended in order to minimize incompatibilities between the display devices in the market. Among various methods for content protecting, High-bandwidth Digital Content Protection System (HDCP) version 1.3 is adopted in this design [18]. When the content protection is supported, the outputs of the physical layer are encrypted. Thus, the decryption block should be inserted between the physical layer and the link layer to reconstruct the main stream data properly.

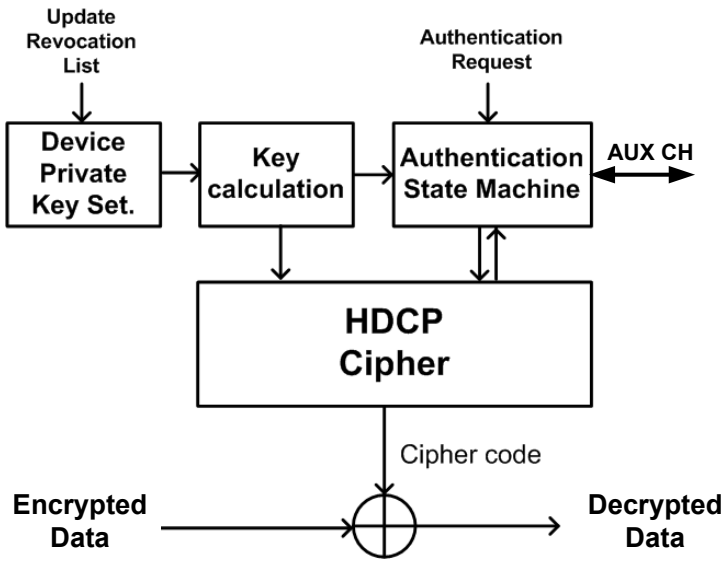


Fig. 3.18 HDCP decryption.

Fig. 3.18 shows the block diagram of HDCP decryption. In the transmitter, the data stream is bit-wisely XORed with a 32-bit pseudo-random bits produced by a HDCP Cipher. New pseudo-random bits are generated for every link symbol clock cycle. The receiver must produce the same pseudo-random bits for decryption being synchronized with the transmitter. The synchronization between the devices is accomplished by an authentication protocol. Each device has a unique set of Device Private Keys and a non-secret corresponding identifier. Once the content protection request is detected, the transmitter and the receiver exchange the calculated keys to prove that each device is authorized to support the content protection. The key calculation is performed by selecting several keys from the Device Private Key Set according to the corresponding identifier. If the devices are authorized, the generation of the cipher code is enabled and synchronized.

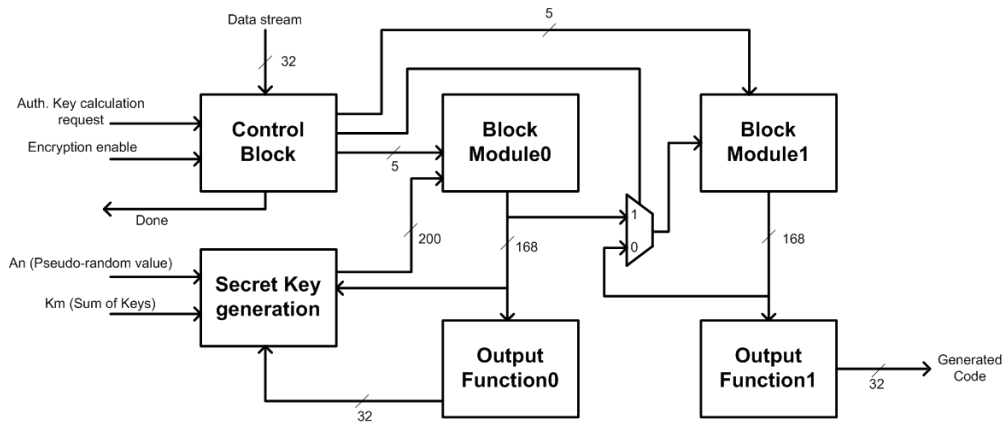


Fig. 3.19 HDCP Cipher Structure.

THe HDCP Chiper is the core logic to produce a 32-bit block of pseudo-random bits for every clock pulse. The HDCP Cipher structure is illustrated in Fig. 3.19. During the authentication process, a secret key generation module calculates the initial keys to exchange with the transmitter. A control block detects a special symbol to synchronize with the transmitter when the content protection is enabled. Two block modules are composed of Linear Feedback Shift Register (LFSR), shuffle network, S-box function and diffusion network. Two output functions have their unique formulas to generate 32-bit pseudo random outputs. Refer to [49] for further details of operation and procedure of sub-blocks.

3.3.5 Audio Transmission

An audio data stream is transmitted in various types of packet. An audio stream packet contains audio data itself and some information such as audio coding type and channel count. It includes status information about parameters of the audio data stream depending on the coding type. An audio info-frame packet contains detailed attribute data of audio data stream. An audio time-stamp packet contains M, N values which are used for generating audio stream clock as same as video stream clock generation. The audio packets are transmitted only during blanking period which there are no main video stream. Although the audio stream is a continuous stream of audio samples, the audio packet must wait for an available time slot.

Fig. 3.20 shows block diagram of the audio data stream transmission. During the blanking period, the received audio packets are extracted from the main video stream path. The received audio data is nibble interleaved in order to further enhancement of an error correcting capability. Thus, the nibble de-interleaving is performed and Error Correcting Code (ECC) module detects and corrects an error in the received packet. ECC is based on Reed-Solomon code, RS (15, 13), which error correction capability is 1 symbol error. By combining the nibble interleaving, the capability increases up to 2 byte error in 16 byte data block. Audio packets are classified by detecting a header that has information about packet types. Audio stream packets are written in FIFO which aims to change clock domains from the link symbol clock to the audio stream clock. And FIFO is also used for stretching the audio stream to the continuous data stream since a quantity of the audio packets are received at once

during the short blanking periods. The audio info-frame packet is un-packed and delivered to the downstream audio device and the time stamp values are used in the audio frequency synthesizer to reconstruct the audio stream clock [50]-[57].

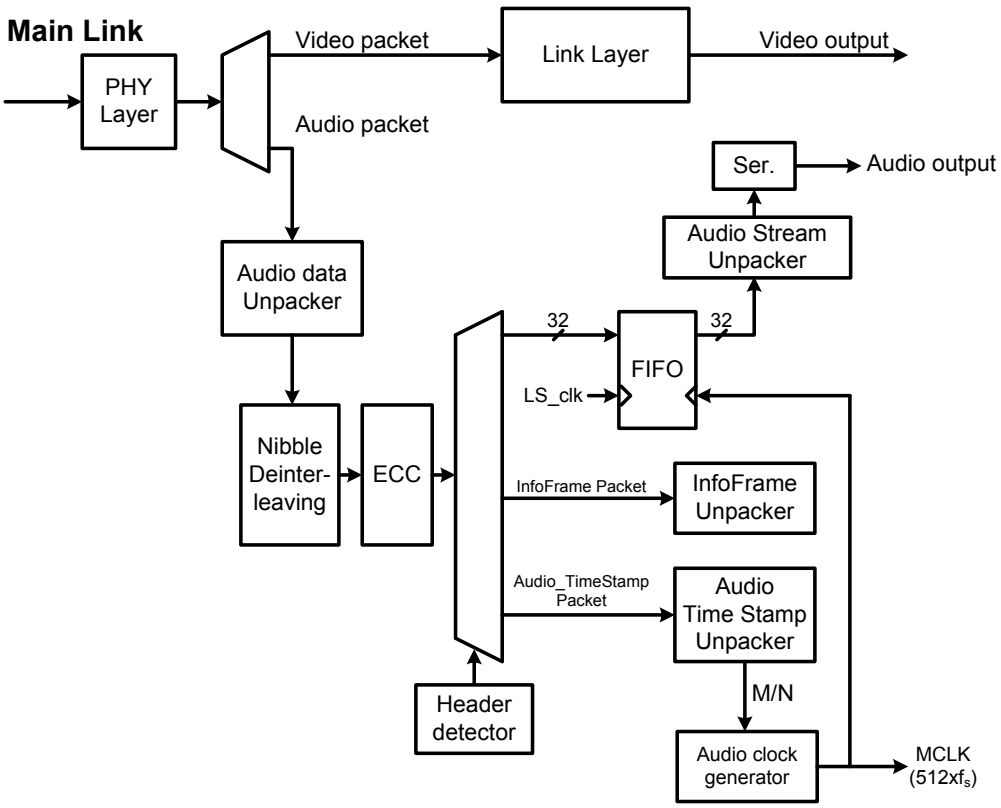


Fig. 3.20 Block diagram of audio data transmission.

3.4 Experimental Results

The prototype chip was fabricated in a 65-nm CMOS GP process. An Agilent J-BERT N4903A and a Tektronix oscilloscope DPO70804B are used for PHY layer compliance test. Link layer compliance test is performed with a Quantumdata Link analyzer 882EA-DP. The test environment for the fabricated chip is shown in Fig. 3.21.

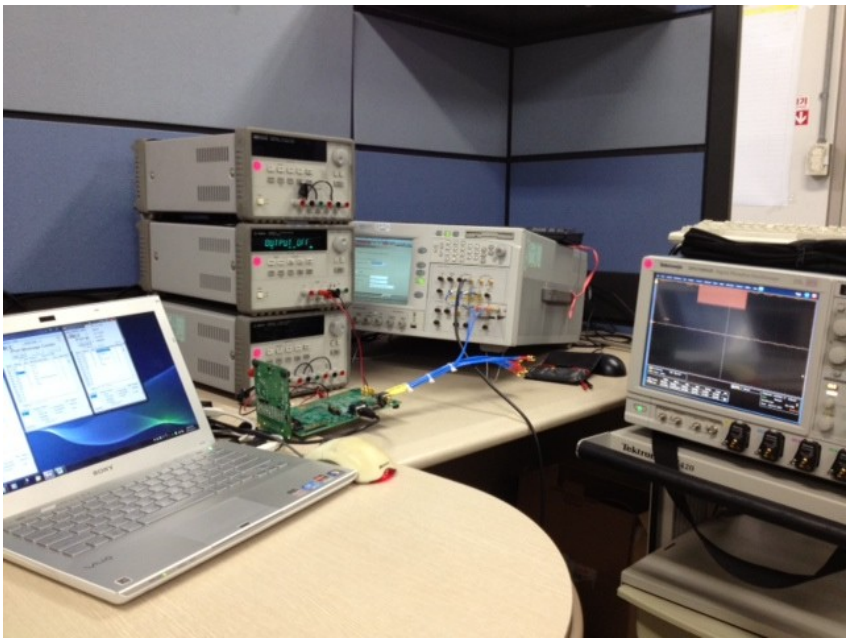


Fig. 3.21 Test environment for the fabricated chip..

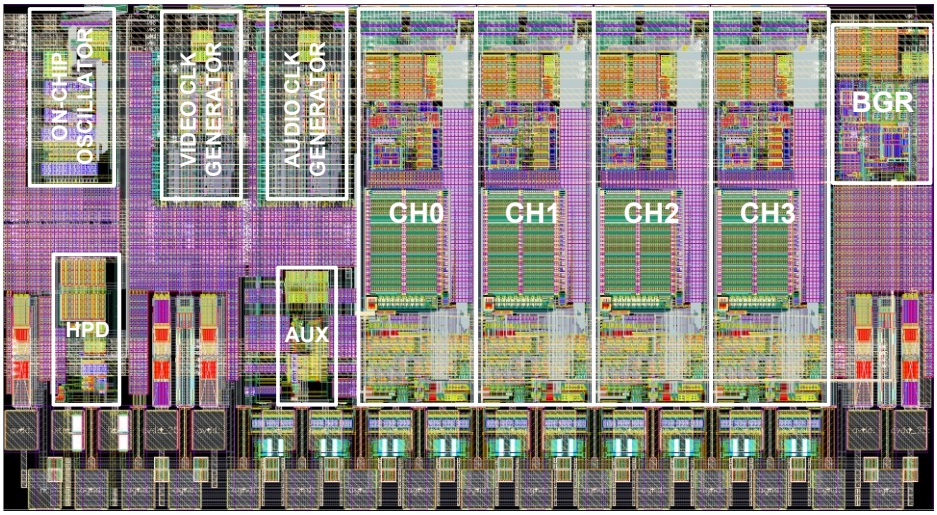


Fig. 3.22 Layout of electrical PHY.

The layout of the electrical PHY layer is illustrated in Fig. 3.22. Four ADCDRs are placed in the individual channel to support 4-lane operations. A band-gap voltage reference (BGR) circuit is included to provide a PVT independent voltage reference for the DCO supply. It converts a 3.3-V external supply voltage to an 1-V internal DCO core voltage, and consumes less than 1-mA current. Two direct digital frequency synthesizers for generating video and audio stream clocks are implemented respectively. An on-chip oscillator for generating 16 MHz internal clock is implemented and AUX CH and HPD circuits are composed of transmitting drivers and receiving samplers. The overall electrical PHY layer occupies $1600\times870\mu m^2$.

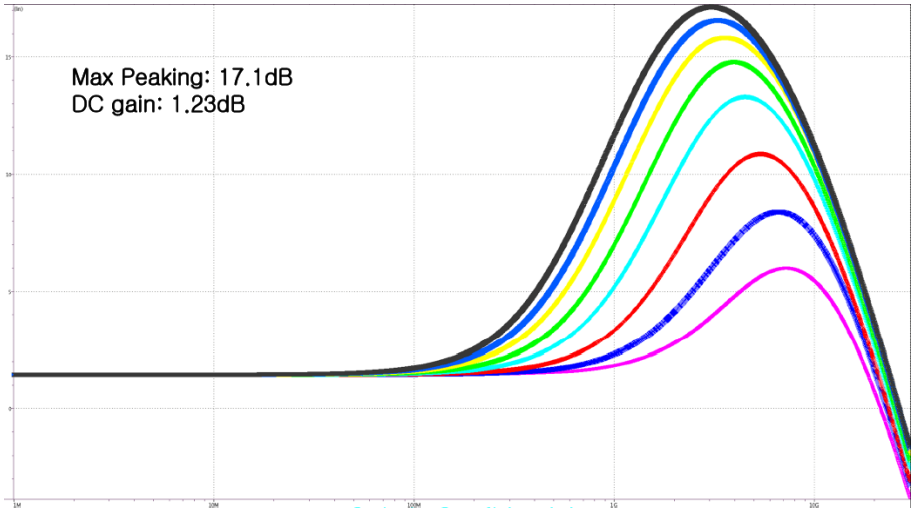


Fig. 3.23 AC analysis of equalization circuit.

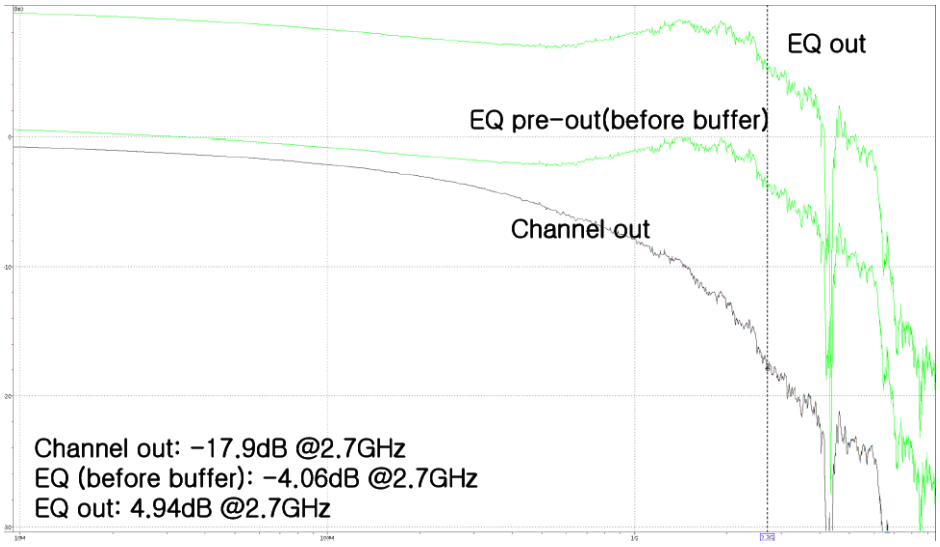


Fig. 3.24 AC analysis of equalization circuit with channel loss.

The equalization circuit in each channel exhibits maximum peak gain of 17.1 dB with the two stage topology. Fig. 3.23 shows the simulation result of the AC analysis of the equalizer. The AC gain is controllable by configuring the source degeneration RC filter. The eye monitoring block adaptively adjusts moderate setting of RC values by detecting vertical eye opening of equalized outputs. As shown in Fig. 3.24, the power loss of the channel is -17.9 dB at 2.7 GHz. The two-stage linear equalizer plus a output buffer compensates channel loss and the output of the overall equalizer exhibits 4.94 dB at 2.7 GHz. The simulated eye diagram of the equalized outputs with the 8-different RC filter configurations are shown in Fig. 3.25.

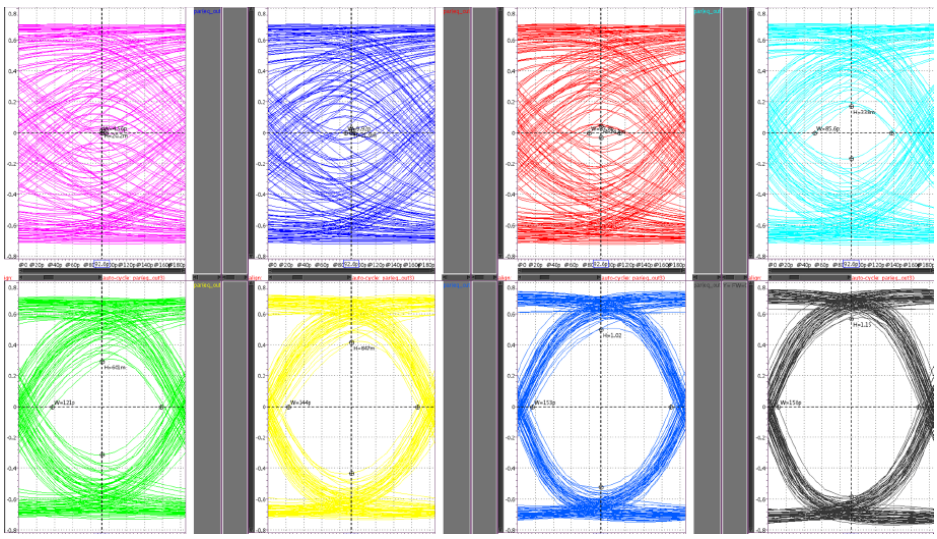


Fig. 3.25 Simulated eye diagram of equalizer outputs.

Fig. 3.26 shows the simulation result of the eye monitor operation. The eye diagram of the equalized output is closed at the start of the simulation. When the output

flag of the eye monitoring block is zero, it increases the AC gain by updating the capacitor configuration in RC filter. If the AC gain is not sufficient, the eye opening flag cannot be settled such as shown in middle of the simulation. After the second update of the capacitor configuration, the eye opening is enough to satisfy the minimum opening and the output flag settled to stable high state.

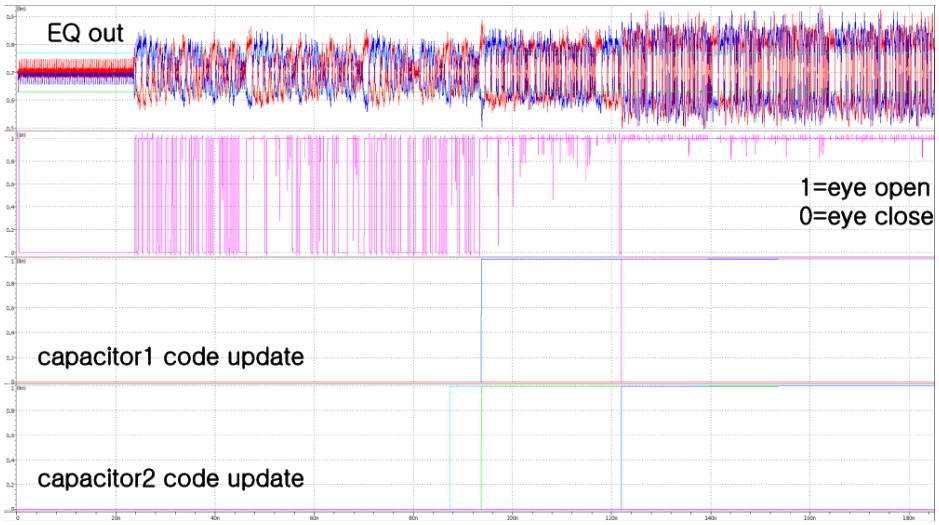


Fig. 3.26 Eye monitor simulation.

Fig. 3.27 and Fig. 3.28 illustrate the simulation results of the DCO curve with layout parameter extraction (LPE) in three modes. In HBR/HBR2 mode, the target frequency of 2.7 GHz is satisfied with various PVT corner cases. The target frequency is 2.4GHz in the RBR mode, and it also satisfied in all PVT variations.

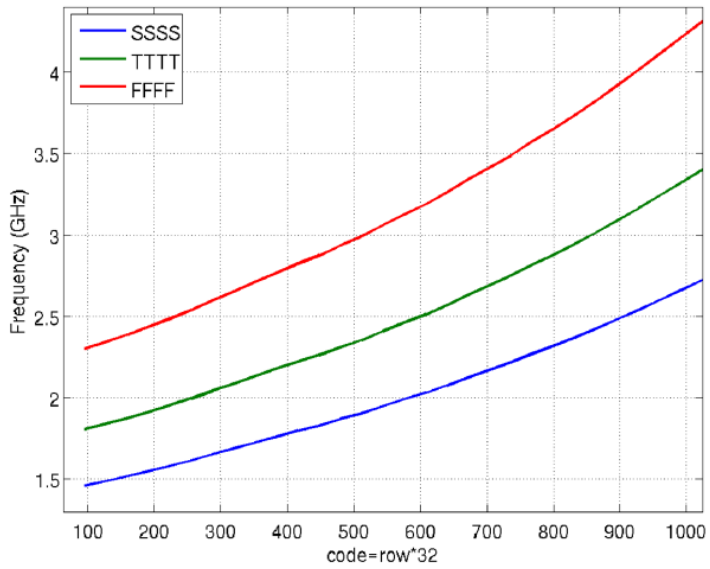


Fig. 3.27 Simulated DCO curve in HBR/HBR2 mode.

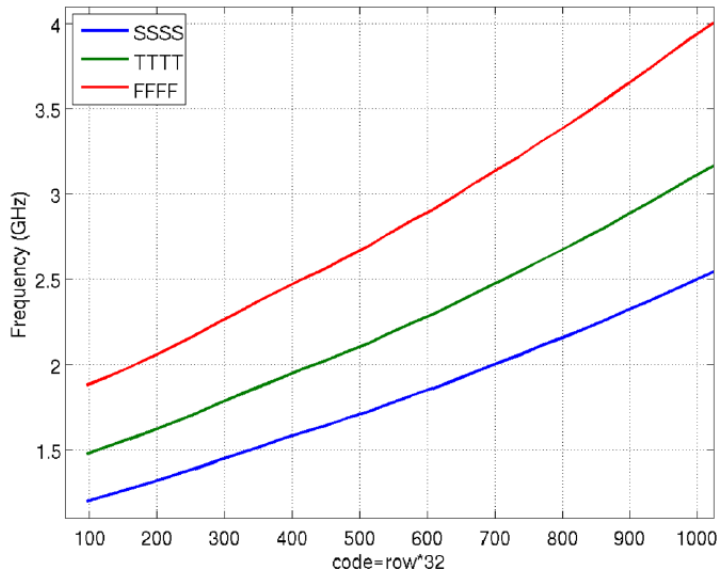


Fig. 3.28 Simulated DCO curve in RBR mode.

PHY compliance test specification outlines a minimum eye diagram which is measured at test point 3 (TP3) as shown in Fig. 3.29. TP3 means the measurement point where a test access fixture as close as possible to the receiver. The eye diagram shows the amplitude of the signal applied for the receiver. The receiver must sustain a 10^{-9} BER under most severe signaling conditions permitted by Fig. 3.29.

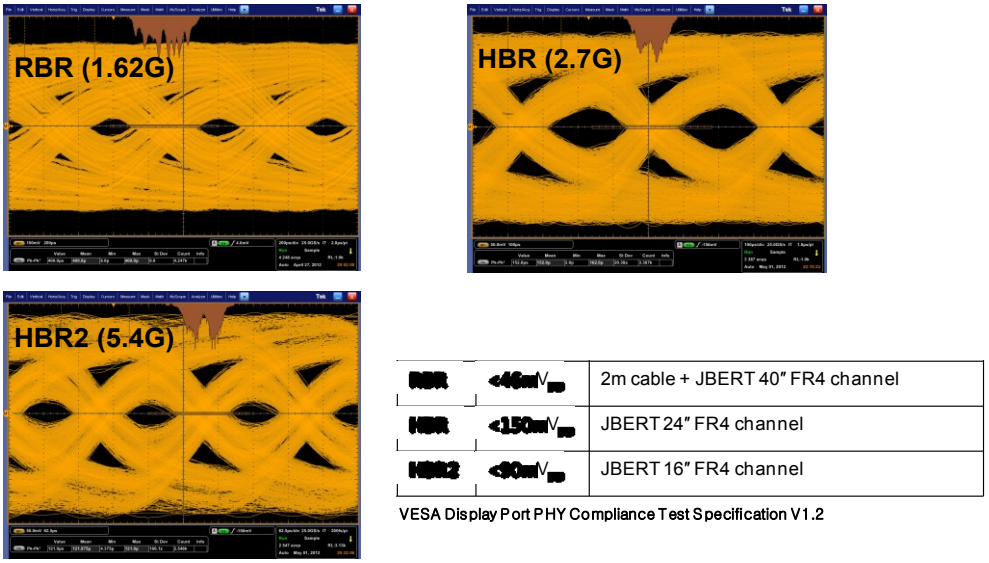


Fig. 3.29 Measured eye diagram at TP3 for PHY compliance test.

Figures from 3.30 to 3.32 show the measured jitter tolerances. Since the used equipment cannot generate the large jitter amplitude at low jitter frequencies, the projected value is illustrated in the measurement result in RBR mode. The ADCDR circuit satisfies the target jitter tolerance specification.

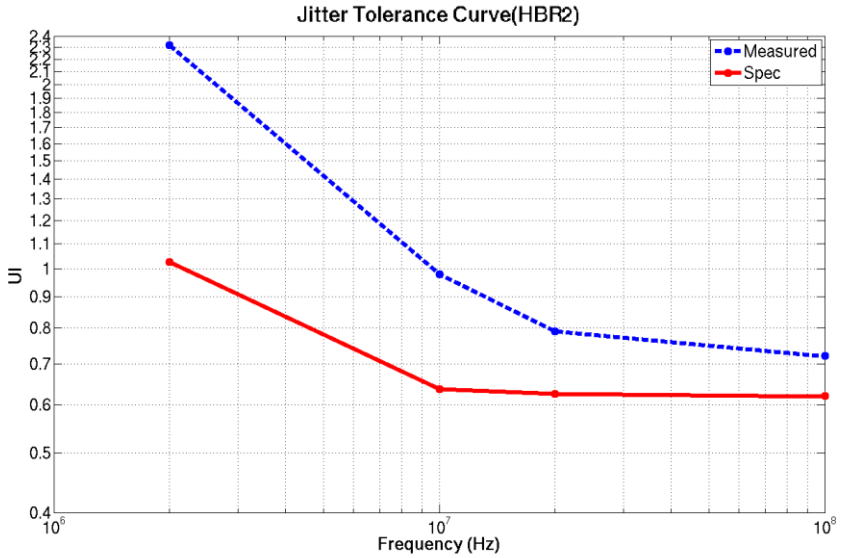


Fig. 3.30 Jitter tolerance measurement in HBR2 mode.

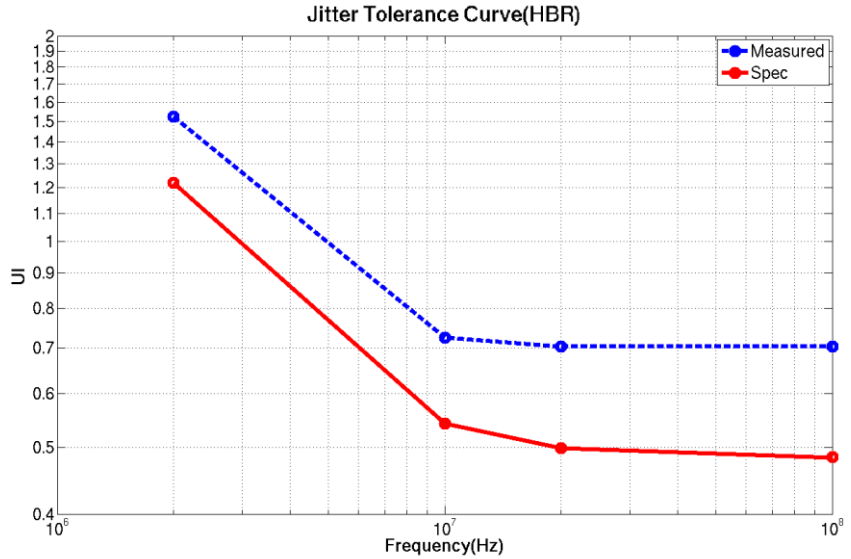


Fig. 3.31 Jitter tolerance measurement in HBR mode.

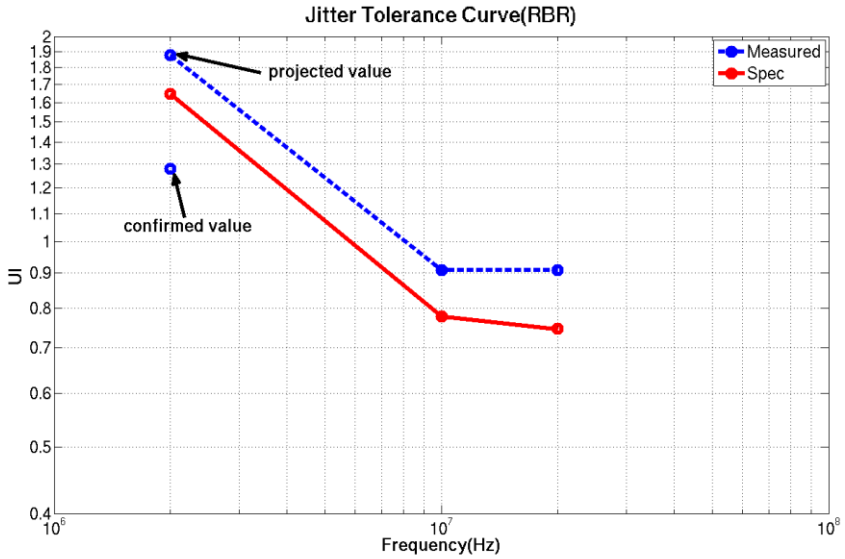


Fig. 3.32 Jitter tolerance measurement in RBR mode.

Fig. 3.33 shows the PCB board for test of the fabricated chip. The purpose of the test chip is a conversion from Displayport data stream to HDMI transportation. Thus, a Displayport connector and a HDMI connector are mounted on the board. The data from a Displayport source device is received by the test chip and the reconstructed video/audio data and clock are delivered to the HDMI transmitter inside the test chip. The test chip sends the data to the external display device through a HDMI cable. A display demonstration using the test board is shown in Fig 3.34. An Apple Mac-book Air is used as a DisplayPort source device and a Dell monitor is used as a HDMI sink device. The test board operates well as a DisplayPort-to-HDMI convert-er.

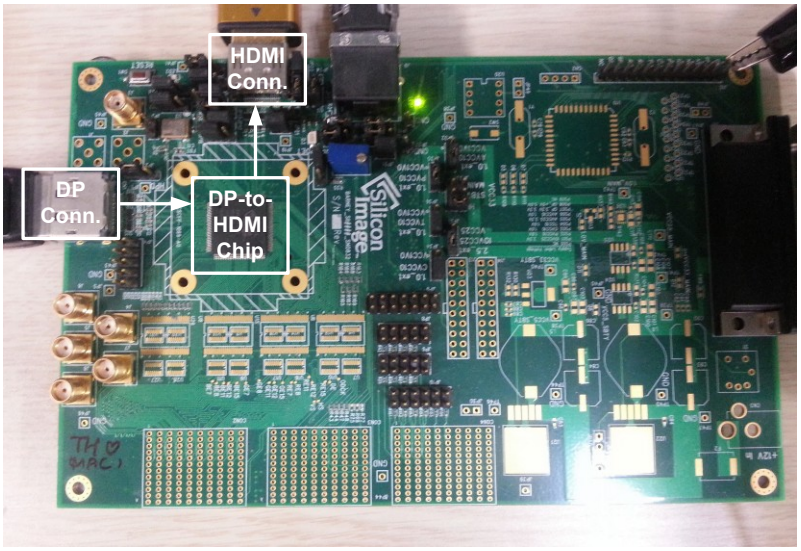


Fig. 3.33 Test board for measurement.

Fig. 3.34 Display demonstration with test board.

Table 3.3 Estimated area of digital block.

Hierarchical Cell	Percent Total	Gate Count	Estimated Area(mm^2)
Top	100	1101150	2.26
PHY	11.3	34034	0.07
Link	52.2(5.6)	575284(59898)	1.18(0.08)
FIFO	46.8	515386	1.06
AUX	16.2	177955	0.36
Audio	16.2	177962	0.36

Table 3.3 shows the estimated area of the link layer which is implemented in digital circuit design. The data is extracted from back-end process of the digital block. It occupies 2.26 mm^2 with a dual-port SRAM that used as the FIFO form clock domain crossing between the link symbol clock and the video stream clock. The power break downs of the electrical PHY layer are presented in Table 3.4 and Table 3.5. The measured power is almost the same with expected results of simulations. The summary of the measured power consumption for the overall receiver is presented in Table 3.6. The physical layer dissipates 86 mW at 1.62 Gb/s, 101 mW at 2.7 Gb/s and 116 mW at 5.4 Gb/s with all 4-lane operation. The power consumption of the link layer is 107 mW at 1.62 Gb/s, 145 mW at 2.7 Gb/s and 167 mW at 5.4 Gb/s. The total power consumption is about 219/282/313 mW at 1.62/2.7/5.4 Gb/s data rate.

Table 3.4 Average current of electrical PHY in RBR mode

			Simulation	Measurement
ADCDR (1 lane)	Termination		8 mA	16 mA
	Equalizer		4 mA	
	Sampler+PD+DES+etc		4 mA	
	DCO		2 mA	2 mA
	Total		18 mA	18 mA
Etc.	AUX	Termination	8 mA	23 mA
		Driver	8 mA	
	Video clock generator		3 mA	
	Audio clock generator		3 mA	
	Internal oscillator		2 mA	
	Total		24 mA	23 mA

Table 3.5 Average current of electrical PHY in HBR mode

			Simulation	Measurement
ADCDR (1 lane)	Termination		8 mA	19 mA
	Equalizer		4 mA	
	Sampler+PD+DES+etc		5 mA	
	DCO		3 mA	3 mA
	Total		20 mA	21 mA
Etc.	AUX	Termination	8 mA	27 mA
		Driver	8 mA	
	Video clock generator		4 mA	
	Audio clock generator		4 mA	
	Internal oscillator		2 mA	
	Total		26 mA	27 mA

Table 3.6 Summary of measured power consumption

RBR mode				
	PHY		**digital**	**Total (mW)**
	3.3V	**1.0V**	**1.0V**	
1lane	6.6	39	97	142.6
2lane	13.2	55	101	169.2
4lane	26.4	86	107	219.4
HBR mode				
	PHY		**digital**	**Total (mW)**
	3.3V	**1.0V**	**1.0V**	
1lane	9.9	46	131	186.9
2lane	19.8	65	136	220.8
4lane	36.3	101	145	282.3
HBR2 mode				
	PHY		**digital**	**Total (mW)**
	3.3V	**1.0V**	**1.0V**	
1lane	9.9	53	162	224.9
2lane	19.8	75	163	257.8
4lane	29.7	116	167	312.7

Chapter 4

Design of Embedded DisplayPort Receiver

4.1 Overview

The second design aims to connect internal display source to the display panel. Both the eDP receiver and TCON is included inside the prototype chip. The data stream from the graphic hardware comes into the eDP receiver and the reconstructed video/audio data and clock are delivered to the TCON for. Fig. 3.2 shows the usage of the prototype chip in a internal chip-to-chip display interface. The eDP source is typically integrated into the graphics processor on a motherboard and the sink is usually integrated into the display processor, such as in the TCON of a notebook PC. The chip consists of the eDP receiver, TCON, backlight control and EDID rom. The

reconstructed video pixel data and clock from the received data are delivered to a row and column drivers for displaying and the backlight control is available through the AUX CH. Audio data transport is not supported in this design and the content protection is performed using alternative methods such as an alternative scrambler seed reset and an alternate framing mode.

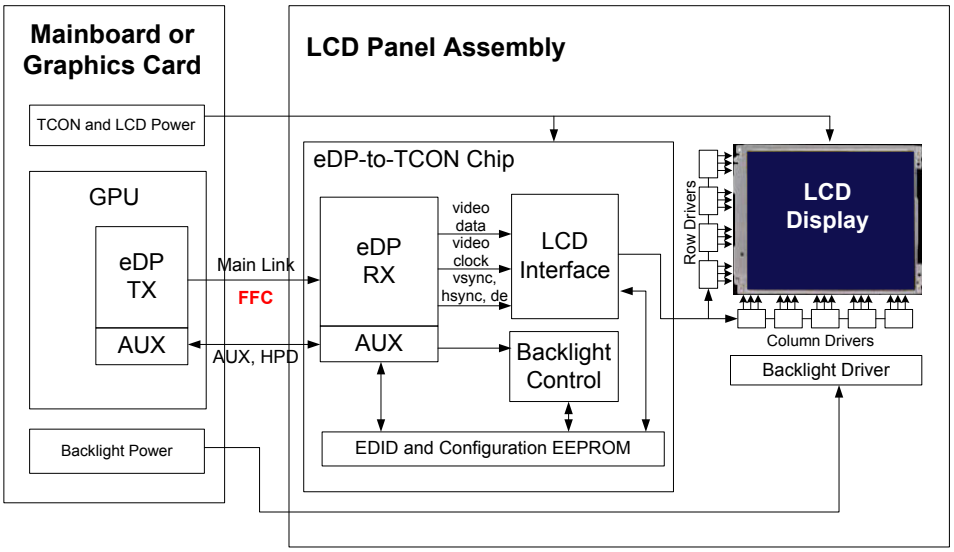


Fig. 4.1 The usage of the second design in a intra-panel interface.

The target video format supported is defined as follow: the maximum resolution is up to 2560×1600@60Hz and the minimum resolution of the display is 640 ×480@60Hz. The video pixel clock frequency range is from 20 MHz to 180 MHz

with transmissions of dual pixel per clock. The supported color depth is 6, 8 and 10-bit per color and only RGB space is supported. Table 4.1 shows a description on clock domains in the design. The link symbol clock is recovered from the incoming data stream by ADCDR circuit which has dual modes for supporting data rates of 1.62 and 2.7 Gb/s. The serial data stream is de-serialized into 10-bit data, so that the link symbol clock used inside the design is 1/10 of the link rate. Since each lane has an independent ADCDR circuit, four recovered clocks are extracted and the received data in all lanes are aligned with the representative clock which is usually the recovered in lane 0. The direct digital frequency synthesizers are included for generating the video stream clock.

Table 4.1 Clock domains in the second design.

Name	Description
link symbol clock	Recovered link symbol clock from ADCDR. Clock frequency: 162MHz, 270MHz
video stream clock	Stream clock. Clock frequency: 20MHz ~ 180MHz, which depends on video format.
AUX clock	Auxiliary channel clock. Clock frequency: 16MHz (Min: 12MHz, Typ: 16MHz, Max: 20MHz)

4.2 Physical Layer

The architecture of the physical layer is basically the same with the first design. However, a frequency synthesizer for an audio clock generation and an internal oscillator are removed in this design. The detailed block diagram of the electrical PHY physical layer is illustrated in Fig.4.2. Four ADCDR circuits are placed on the individual lanes for recovering link symbol clocks from the incoming differential signals. A video clock generator synthesizes a video/audio stream clock with the recovered clock and time stamp values extracted from the data stream. AUX CH, HPD circuitry and low-dropout regulator (LDO) with band-gap reference (BGR) circuit for providing DCO supply are included.

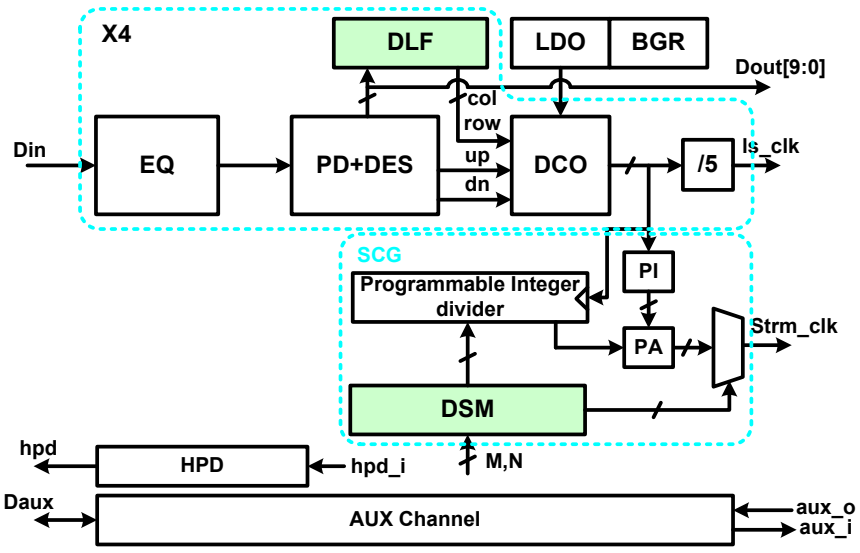


Fig. 4.2 Architecture of electrical PHY layer.

The equalization circuit (EQ) on the front end of each lane. It excludes the eye monitoring scheme since the internal interface connected with the fixed channel. The optimum configuration of the equalizer can be determined by manual optimization. The ADCDR topology is similar with the one in the first design. It also adopts a half-rate architecture as it relaxes the required clock frequency for a given bit rate. The phase detector (PD) which is a half-rate bang-bang type detects the phase difference between the incoming data stream and the recovered clock from a digitally-controlled oscillator (DCO). The PD output delivered to the DCO along proportional and integral paths. The integral path which is implemented with a digital loop filter (DLF), accumulates the phase errors for tracking the frequency. The DCO generates half—rate 8-phase clocks which are fed back to the half-rate bang-bang PD for phase comparison and one of the output clock divided by 5 to generate a link symbol clock for the link layer operation.

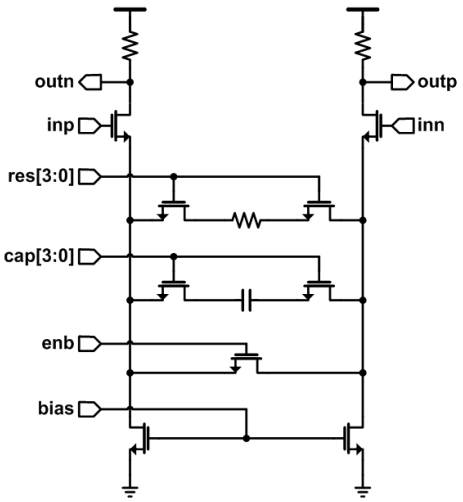


Fig. 4.3 Equalization circuit.

The equalization circuit is only one stage continuous time linear equalizer with a RC source-generated differential structure. Compared to the first design which supports the maximum data rate of 5.4 Gb/s, this only supports up to 2.7 Gb/s. Thus, the single stage equalization is enough to compensate the channel loss. The circuit implementation of the equalization circuit is presented in Fig. 4.3.

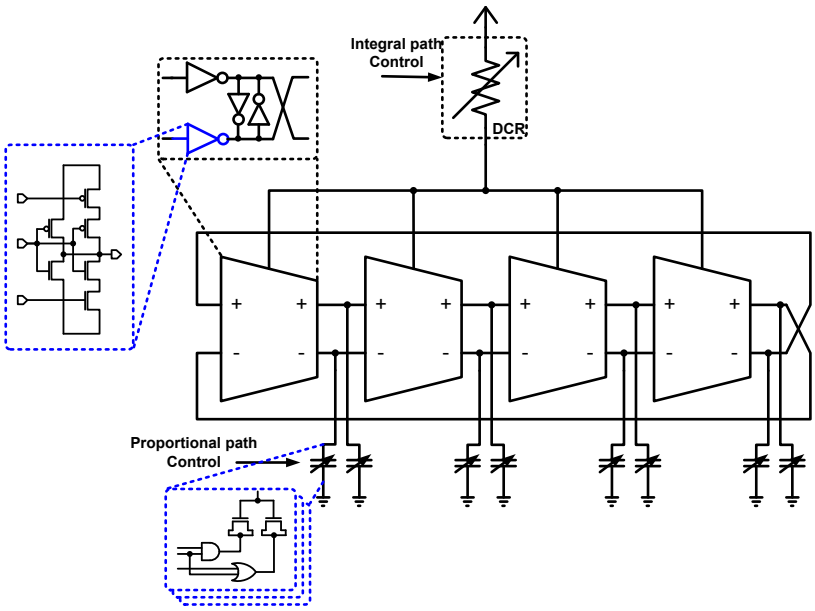


Fig. 4.4 Digitally-Controlled Oscillator.

The DCO is four-stage ring type oscillator using a pseudo-differential inverter chain that is same with the first design. It consists of a digitally-controlled resistor

(DCR) for integral path control and delay elements with varactor loads for proportional path control. The difference is the reduction of the bit width of the integral path control. The overall DCO codes are reduced by half and the resistor cells in DCR are also cut in half which brings the advantage of reduced are. It has dual modes wide-range to support 1.62 and 2.7 link rates. The strength of the inverter unit is scalable depends on the link-rate selected as shown in Fig. 4.4.

The structure of the logical PHY layer is exactly the same with the first design. Since the detail description is implemented in Chapter 3, it is leaved out in this Chapter.

4.3 Link Layer

4.3.1 Overall Architecture

The link layer is modified from the previous design because some features are not needed to be supported in eDP design. Audio and HDCP blocks are totally removed from the design, and video data reconstruction is simplified due to the reduction of the supported video formats. Each block is more optimized to reduce the area occupation and power consumption. Especially, the individual lanes are totally separated to operate independently for more power saving. In one or two lane mode, the unused lanes are completely power-downed. This also has the advantage of modifying the design to only support fixed lane count for a specific purpose in the future. The overall block diagram of the link layer is illustrated in Fig. 4.5. There is no secondary data path and a HDCP decryption block is removed. A active data unpacking scheme is simplified compared to the previous design. The FIFO for the clock domain crossing from the link symbol clock to the video stream clock is only 1-line buffer which is reduced by half from the previous one. The memory used as the FIFO does not operate up to 270 MHz in the worst PVT corner. Thus, the half clock writing scheme is adopted in this design. The video pixel data and timing signals should be transmitted to TCON with the half rate of the supported video format. The blocks in the stream clock domain are modified to operate at half video stream clock

frequency. The modified video data reconstruction scheme is detailed in the next section.

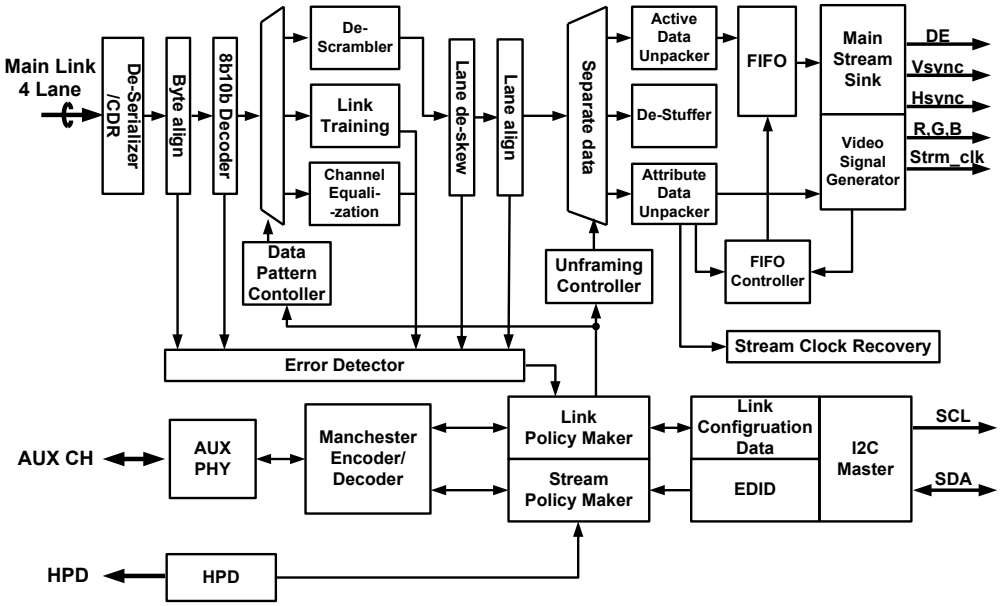


Fig. 4.5 Overall Architecture of the link layer

4.3.2 Main Link Stream

The eDP must be fully compatible with the DisplayPort standard. Typically conly one or two main link lanes are needed due to the limited panel resolution normal for embedded application. Since all 4-lane operation is supported in this design, the architecture of the main link is implemented based on the previous work. The detail scheme for video data reconstruction is presented in Fig. 4.6.

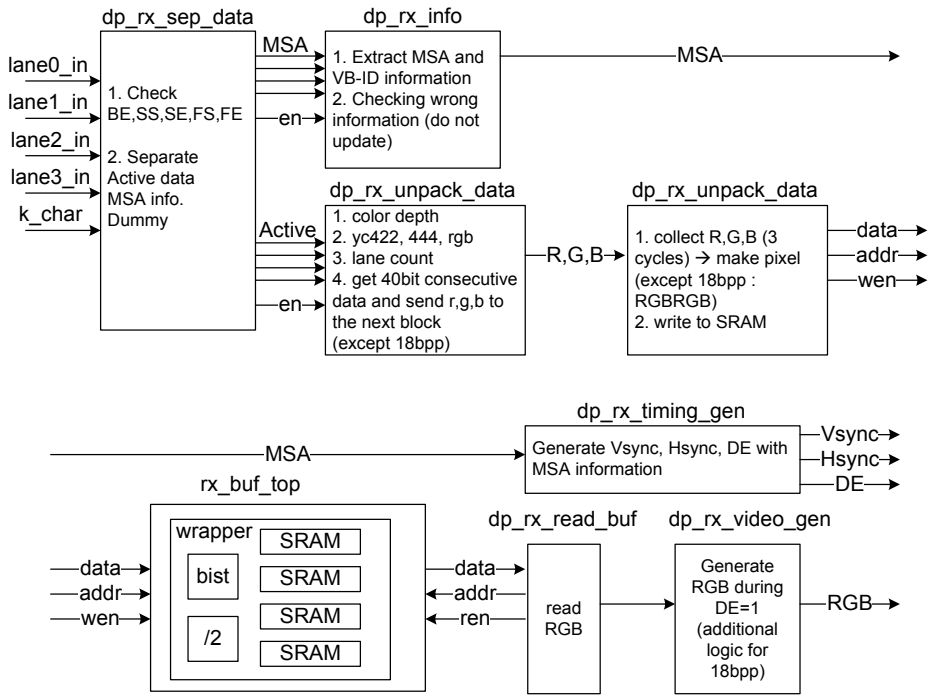


Fig. 4.6 Detail scheme for video data reconstruction

The main link data stream incoming from the physical layer is separated to the active video data and main stream attribute data by detecting the special characters. The main stream attribute data is delivered to the video timing generator which produces Vsync, Hsync and DE signals. The data un-packer combined the video pixel data depends on the color depth, color space and lane count. In order to deliver the reconstructed data to the stream clock domain, the pixel data is written in the FIFO. Data un-packing should be performed regardless of the color space and color depth of the video stream. To achieve this constraint, five consecutive data stream are collected and one pixel data is extracted among them. In the FIFO, one pixel data is located in each address to reduce the design complexity in the stream clock domain. Then, the video data generator reads the pixel data from the FIFO every cycle during the data enable period. Half rate write operation is adopted because memory writing operation cannot operate at full link rate due to the process limitation. A small elastic buffer is placed in front of the FIFO to lower the memory writing frequency. The half rate memory writing scheme is illustrated in Fig. 4.7.

The video stream clock is half rate, so that dual pixel data is delivered to the TCON in each clock cycle. By using four separate memory blocks in the FIFO, read of multi pixel data is possible. Thus, this can be simply implemented by modifying the read operation to access to two memory blocks at single clock cycle.

The size of the FIFO is reduced to one line buffer in contrast with the previous design which is implemented with two line buffer. This drastically reduces the area occupation of large size of memory. The size of the FIFO is 2560×30 bit to support video resolution of 2560×1600 with 30-bit/pixel color depth. When the write operation is progressed to half line, the read operation begins in this scheme. There are

some difficulties to implement the FIFO due to the frequency error of the regenerated video stream clock. Especially, the reduced FIFO size makes it harder. False operations in the FIFO cause fatal problems in panel display. The detail about the problem with frequency error and the method to compensate this will be described in Chapter 5.

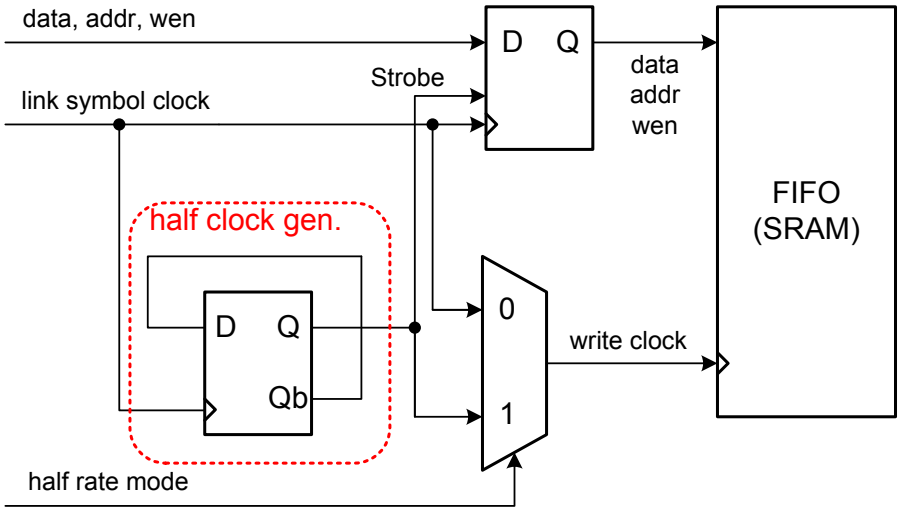


Fig. 4.7 Half rate write operation in FIFO

4.3.3 Content Protection

Typically, HDCP is recommended for protecting content sent to the integrated display. Unless HDCP is used for content protection, a mechanism must be employed to assure the protected content is being sent to the integrated display rather than to a non-HDCP external display or other sink device. There are several optional eDP display authentication and content protection methods. In this design, two protocol-based methods are adopted for content protection. First one is usage of an alternative scrambler seed reset for panel communications. Scramblers reset the LFSRs in the source and sink to FFFFh, in place of the normal FFFFh in this operation. It can be enabled and disabled at any time by the source writing the configuration in DPCD register. Upon changing the scrambler reset seed, the sink should wait for 5 reset symbols in the attempt to resynchronize to the source's scrambler before triggering a link failure event. Since display noise may occur during resynchronization, the source must conceal such possible display noise by forcing black video during this operation. The other method employed is alternate framing for eDP panel communication. It is normally enabled upon link training and continues to be used until the display is powered off. When enabled. the eDP sink must operate only in enhanced framing mode. The source can immediately disable enhanced framing mode at any point during the normal display by writing the configuration in DPCD register.

4.4 Proposed Clock Recovery Scheme

DisplayPort interface basically applies embedded clock architecture to reduce electromagnetic interference (EMI) susceptibility and physical wire count. Thus, the clock must be recovered from the transmitted data stream. Before a normal operation, link training is performed to establish the link by recovering the link symbol clock and equalizing the channel. The full link training sequence, which is shown in Fig. 4.8, is typical method of link training. Upon the HPD detected, a transmitter initializes link status and requests link training by accessing to DPCD fields in a receiver. Full link training consists of two distinct tasks which must be completed successfully in sequence to establish the link. The first sequence is clock recovery that locks the receiver CDR circuit to the repetition of clock patterns. The second sequence is channel equalization that achieves the symbol-lock and inter-lane alignment. During the full link training, each step is performed by AUX CH transactions. Due to the bit rate of 1Mbps for AUX CH transaction, it requires several hundred micro-seconds for each transaction. Therefore, it takes at least several milliseconds to finish the full link training. When the link failure which means a loss of synchronization between the transmitter and the receiver happens, IRQ pulse is generated on HPD wire and the transmitter must restart the full link training sequence to re-establish the link.

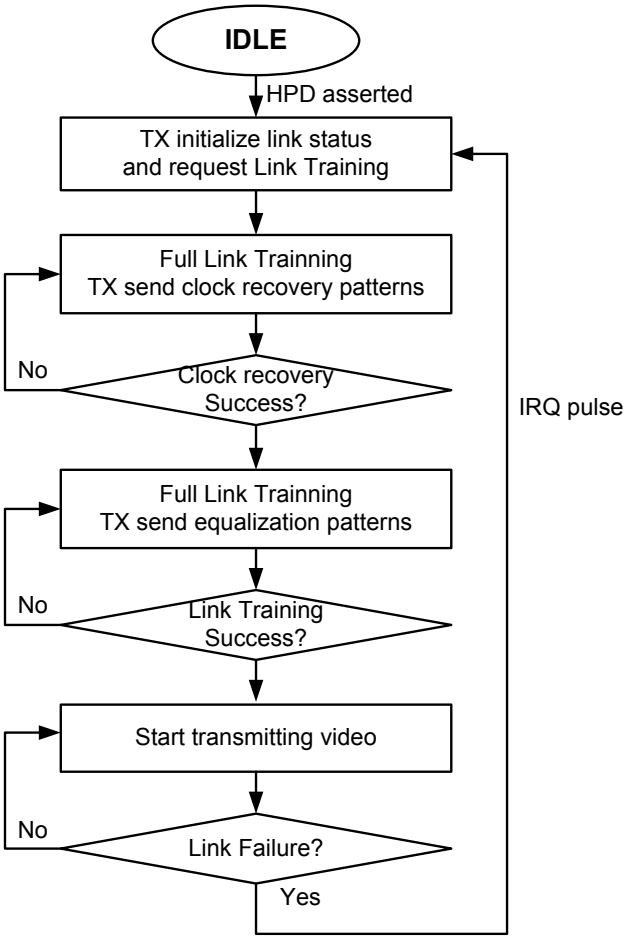


Fig. 4.9 Full link training sequence

In this design, two methods are added for reducing time consuming of link training. They are fast link training and no link training. The state diagrams of each method are presented in Fig. 4.9 and Fig. 4.10, respectively. Fast link training excludes a channel equalization sequence. After the clock recovery sequence, it enters

to the normal operation immediately. Symbol-lock and inter-lane alignment are achieved during the normal operation with the special symbols. Since the error may occur right after the link training, error must be masked until symbol-lock and inter-lane alignment are finished.

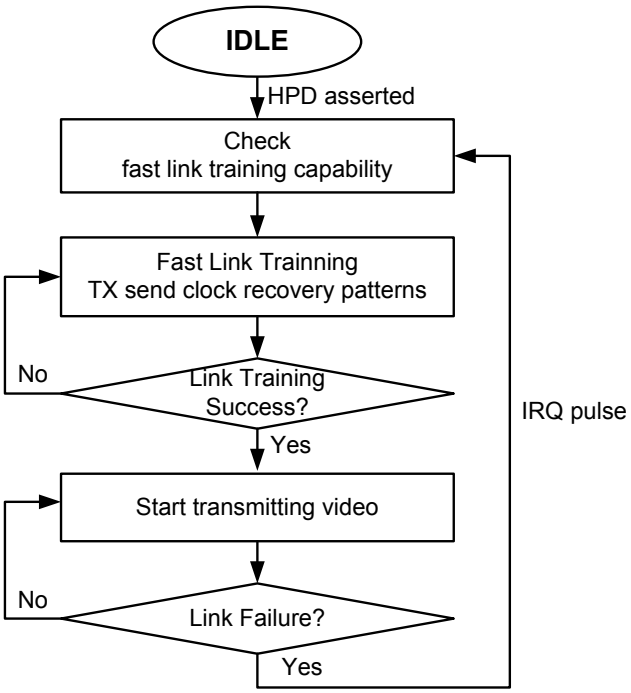


Fig. 4.10 Fast link training sequence

No link training is progressed without AUX transactions. After HPD asserted, a transmitter immediately sends the clock pattern for a specific duration. The receiver

also must be ready to recover the clock whenever it connected to a transmitter. After a specific time for transmitting the clock pattern, the transmitter sends the equalization pattern. The receiver is waiting for the equalization pattern after clock recovery has been done. It should achieve symbol-lock and inter-lane alignment within a specific period for the channel equalization. Since there is no AUX transaction during all the sequences, it takes under 1 millisecond which is extremely decreased compared to the full link training sequence.

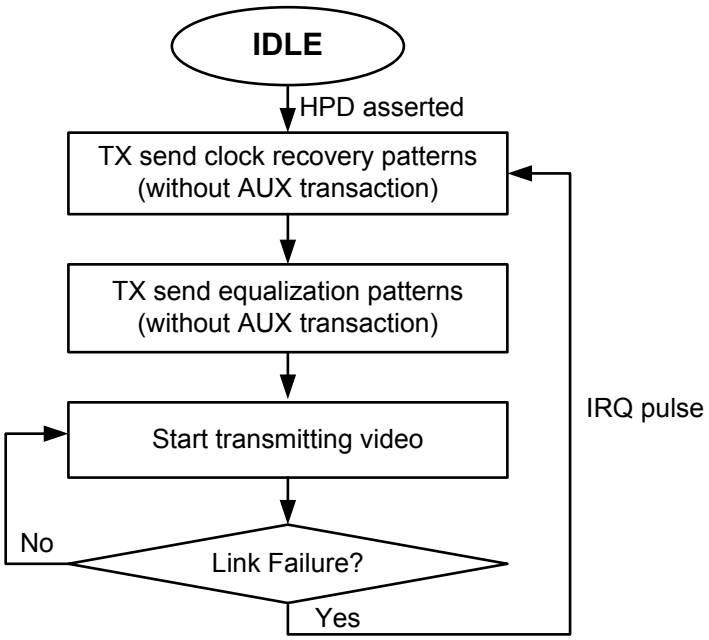


Fig. 4.11 No link training sequence

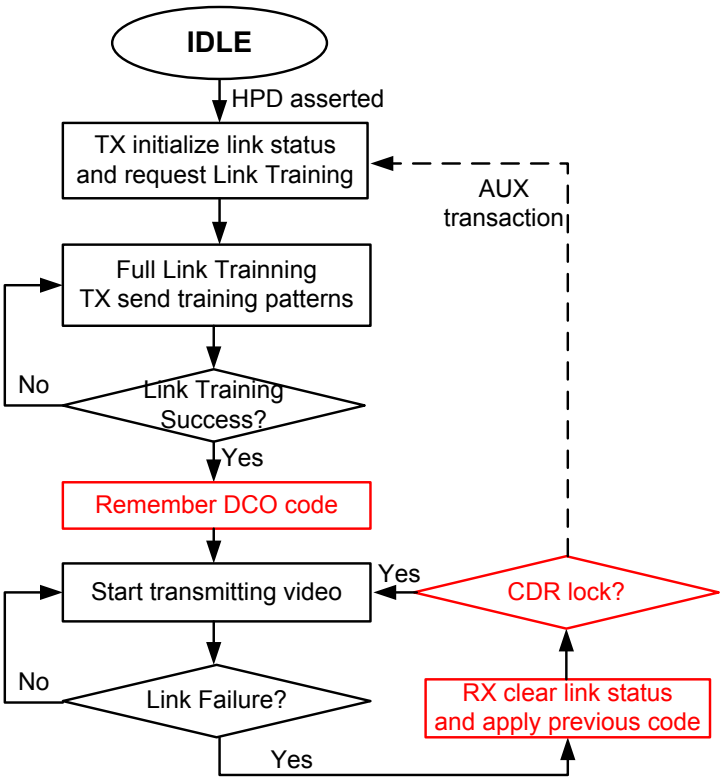


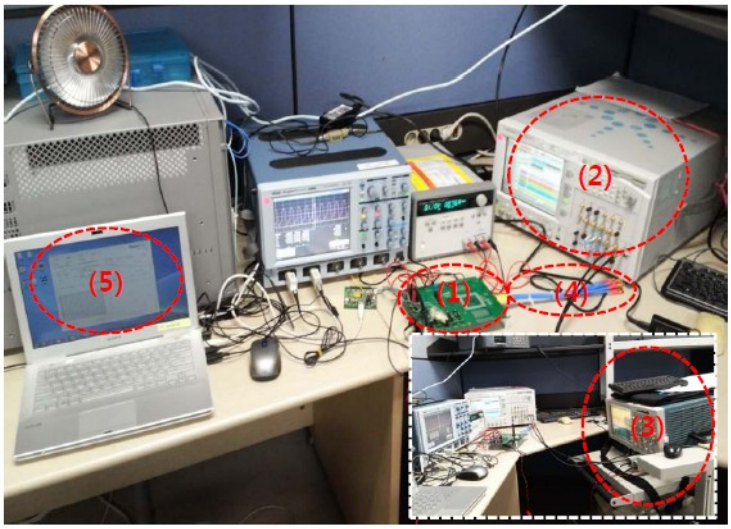
Fig. 4.12 Resynchronization without link training

When the loss of synchronization happens, the receiver notifies the situation to the transmitter by toggling HPD line. HPD pulse with the length of 0.5 to 1 milli-second means IRQ. The transmitter must respond to IRQ events by starting to read the DPCD fields of the receiver device via AUX CH to find out the reason of the IRQ requests. And it restarts the link re-initialization and link training. During this period, the display noise occurs on the display panel. Since it usually takes several

milliseconds for recovering, it causes the discomforts for the device user. Thus, the resynchronization method is proposed to reduce the time to recover from the link failure in this work. The state diagram of the proposed scheme is illustrated in Fig. 4.12. After the link established by link training, DCO memorizes the code in the lock state. It is a benefit of ADCDR topology that the digital code is used for generating oscillation frequency. When a loss of synchronization occurs during the normal operation, the receiver refreshes the link status itself and loads the previous well-locked DCO code instead of generating IRQ pulse to the transmitter. ADCDR tries to recover it lock state while the transmitter does not notice the link failure situation. Within several cycles of the link clock, the receiver recovers the synchronized state and it sufficiently reduces the duration of display noise by shortening the link re-establishing sequence.

4.5 Experimental Results

The prototype chip was fabricated in a 0.13-μm CMOS process. An Agilent J-BERT N4903A and a Tektronix oscilloscope TDS7704 are used for PHY layer compliance test. Link layer compliance test is performed with a Quantumdata Link analyzer 882EA-DP. The test environment for the fabricated chip is shown in Fig. 4.13.



(1)	DUT	eDP-to-TCON Test Board
(2)	Signal Generator	N4903A (BERT, Agilent)
(3)	Oscilloscope	TDS7704 (7GHz B/W, 20G/s)
(4)	DP plug	SMA to DP plug
(5)	Bit Error Counter	Register read

Fig. 4.13 Test environment for the fabricated chip..

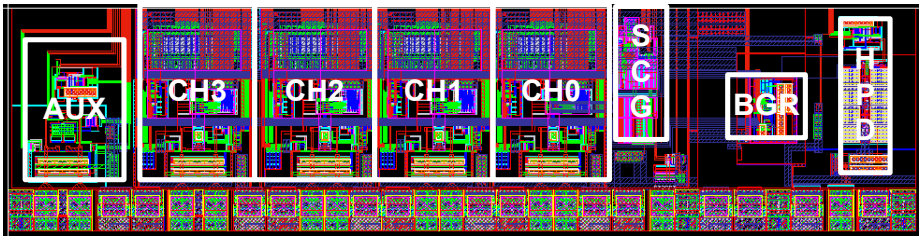


Fig. 4.14 Layout of electrical PHY.

The layout of the electrical PHY layer is illustrated in Fig. 4.14. Four ADCDRs are placed in the individual channel to support 4-lane operations. A band-gap voltage reference (BGR) circuit is included to provide a PVT independent voltage reference for the DCO supply. It converts a 1.8-V external supply voltage to an 1.2-V internal DCO core voltage, and consumes less than 1.2-mA current. A direct digital frequency synthesizer for generating stream clock is implemented. An AUX CH and HPD circuits are composed of transmitting drivers and receiving samplers. The overall electrical PHY layer occupies 2540×625μm^2.

The equalization circuit in each channel exhibits maximum peak gain of about 9 dB with a single state. Fig. 4.15 shows the simulation result of the AC analysis of the equalizer. The AC gain is controllable by changing the register configurations of source degeneration RC filter. The peak gain and the bandwidth can be controlled by adjusting the capacitance and DC gain can be controlled by changing the resistance. The simulated eye diagram of the equalized outputs with the 6-different RC filter configurations are shown in Fig. 4.16.

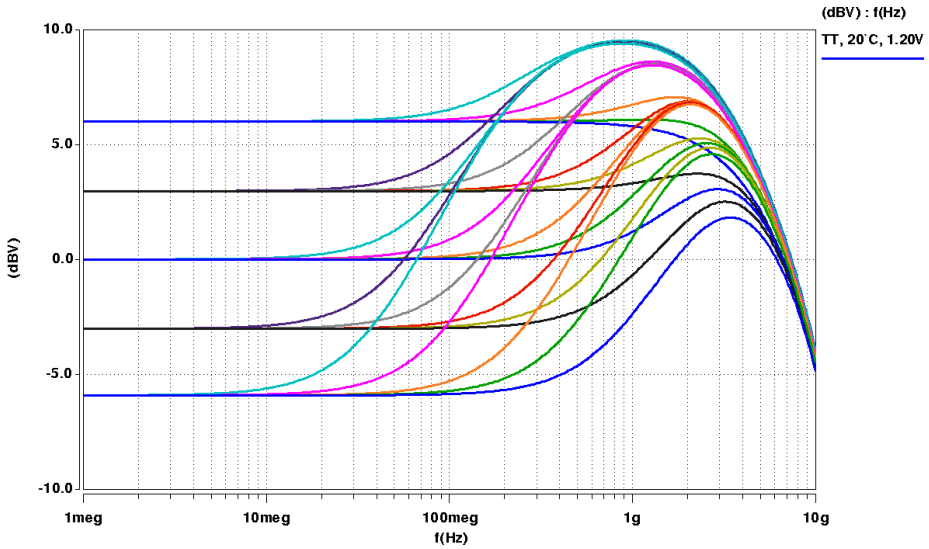


Fig. 4.15 AC analysis of equalization circuit.

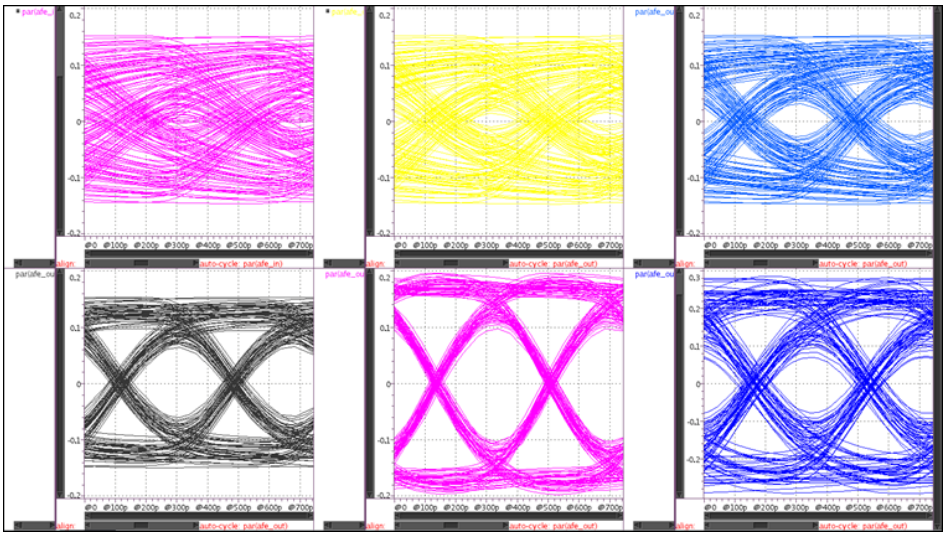


Fig. 4.16 Simulated eye diagram of equalizer outputs.

Fig. 4.17 illustrates the measurement results of the DCO curve in RBR and HBR mode. Since it employs half-rate architecture, the recovered clock frequencies are 810 MHz and 1.35 GHz, respectively. The lock times are about 11μs in RBR mode and 7μs in HBR mode. The results of the lock time measurements are presented in Fig. 4.18. The signal "cr_active" is asserted high when the link training is started. The signal "cr_done" goes high when the clock recovery has been done successfully.

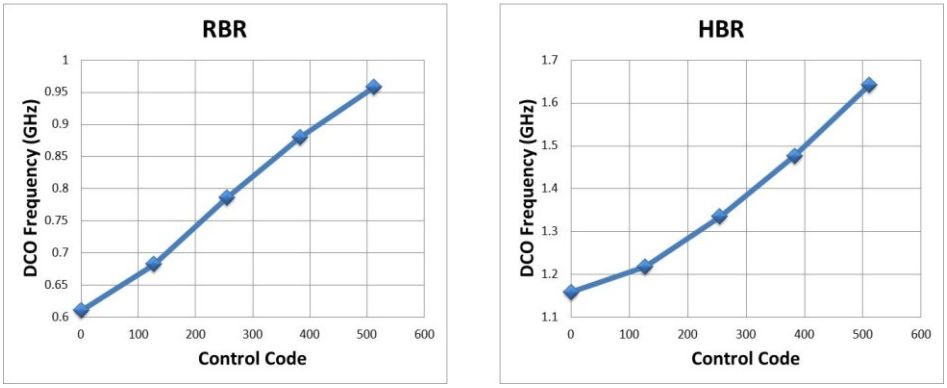


Fig. 4.17 Measured DCO curves in RBR/HBR mode.

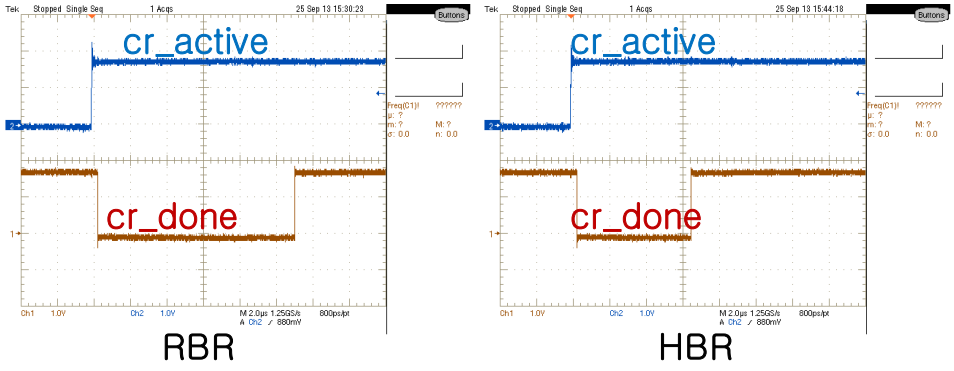


Fig. 4.18 Measured lock times in RBR/HBR mode.

Figures from 4.19 to 4.23 show the measured jitter tolerances with the variations of several conditions. Fig 4.19 presents the jitter tolerance curve according to the supply variations. BGR circuits are included in the design, so that the variations of the measurement results are almost unnoted.

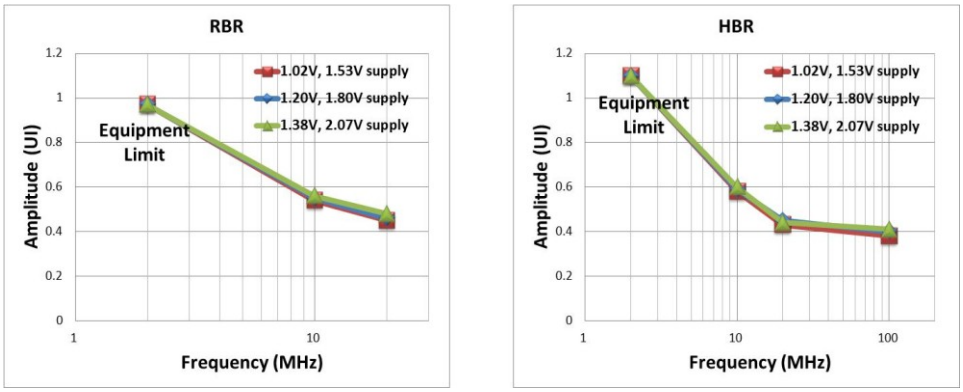


Fig. 4.19 Jitter tolerance measurement with supply variations.

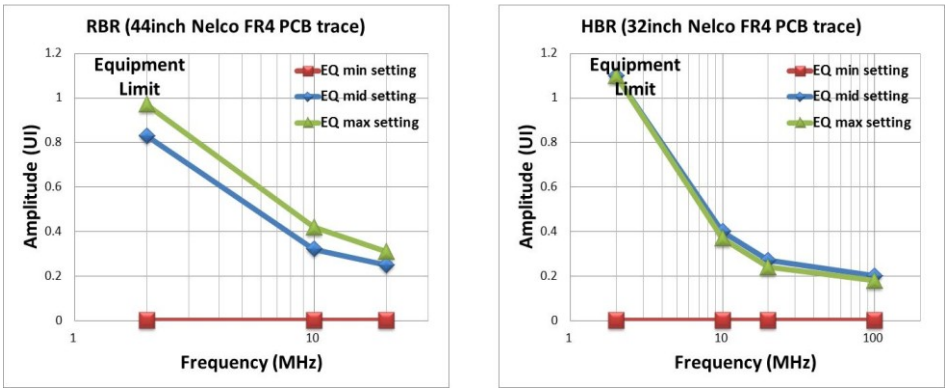


Fig. 4.20 Jitter tolerance measurement with equalization settings.

Fig. 4.20 shows the results with the equalization gain configurations. 44-inch and 32-inch Nelco FR4 PCB traces are used for the channel in RBR and HBR modes, respectively. The jitter tolerance cannot be satisfied with only minimum equalization setting. The results in Fig. 4.21 and Fig. 4.22 are obtained by configuring the proportional path and integral path for the DCO-gain controls.

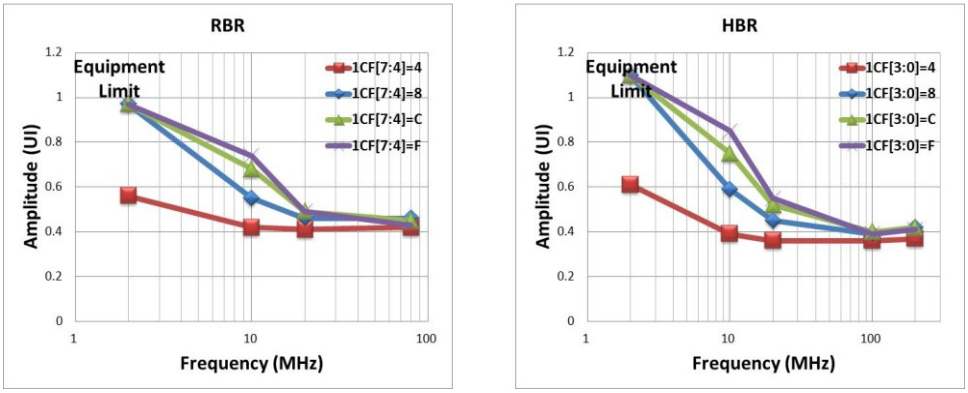


Fig. 4.21 Jitter tolerance measurement with proportional path gains.

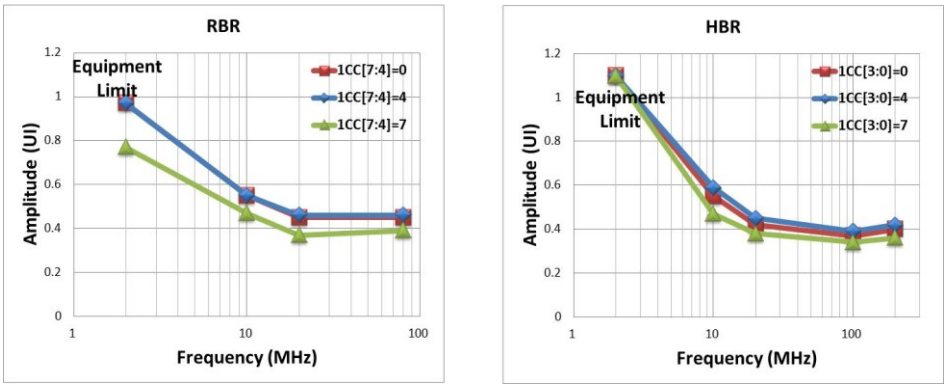


Fig. 4.22 Jitter tolerance measurement with integral path gains.

The simulation results of link training and re-synchronization are shown in figures from 4.23 to 4.26. Full link training sequence normally takes several milliseconds to finish clock recovery and channel equalization as shown in Fig. 4.23. The alternative method that performs link training without AUX transaction reduces the time to establish the link. In this case, the transmitter and receiver may be set to pre-calibrated parameters without going through the full link training sequence since the cable length is fixed in a closed embedded connection. The transmitter starts a normal operation following transmission of clock recovery pattern and channel equalization pattern with pre-calibrated drive current and pre-emphasis level. The simulated result is presented in Fig. 4.24.

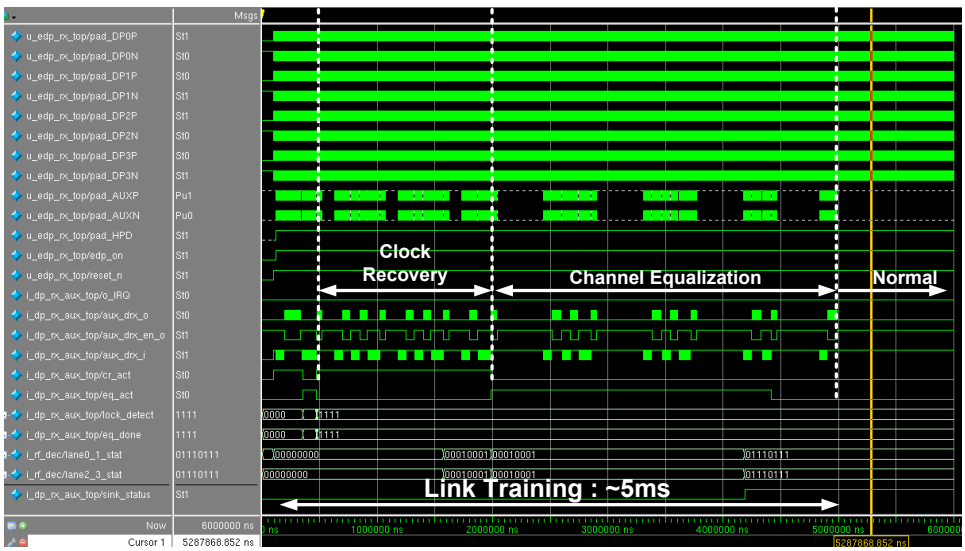


Fig. 4.23 Simulation of full link training sequence.

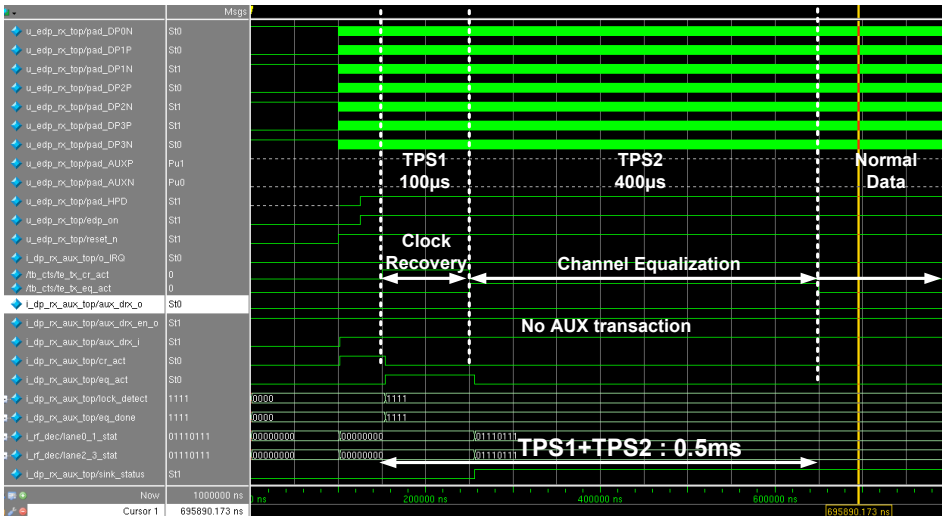


Fig. 4.24 Simulation of link training without AUX transaction.

When a loss of synchronization occurs during a normal operation, the sink typically generates IRQ pulse through the HPD line. Fig. 2.5 shows the simulation of link re-training after IRQ pulse generation. It also takes several milliseconds of full link training sequences. However, the proposed self recovery scheme does not generate IRQ pulse and re-establishes the link with the short interval. During a normal operation, the special characters appear every blank periods which is the same frequency of Hsync. Usually, the special characters are shown at least once within 30 µs. Thus, the recovery is achieved within 0.1 millisecond. Fig. 4.26 shows the simulated result of resynchronization with the proposed self recovery scheme.

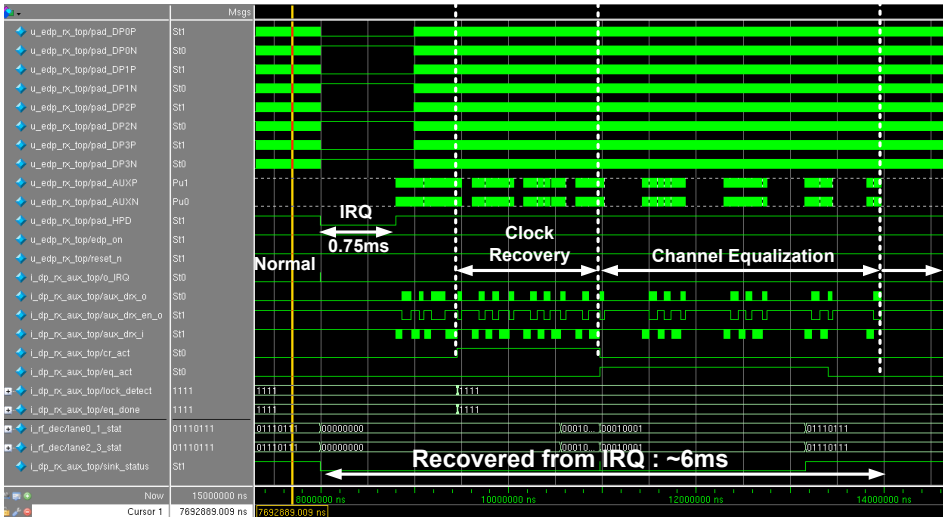


Fig. 4.25 Simulation of link re-establishment after IRQ.

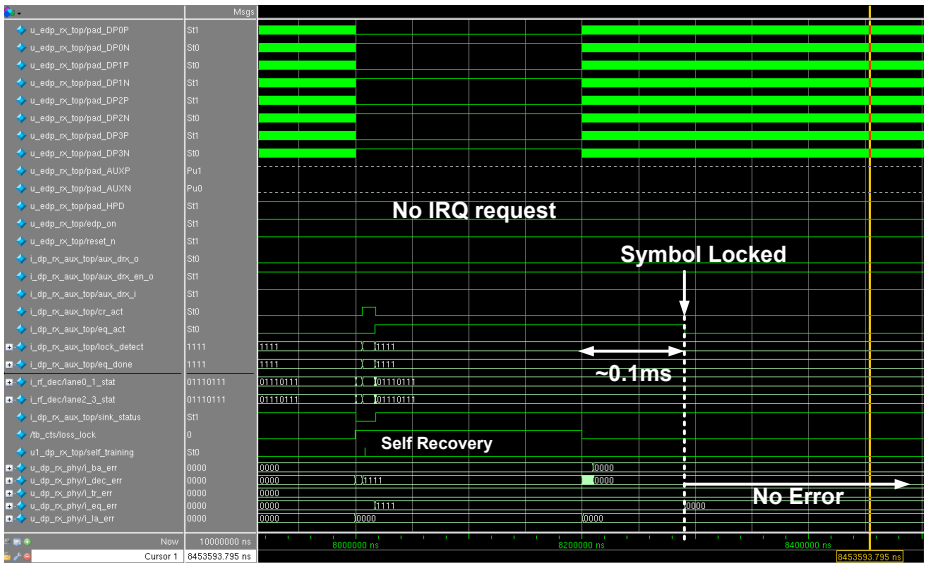


Fig. 4.26 Simulation of resynchronization without IRQ.

Fig. 4.27 shows the PCB board for test of the fabricated chip. The received data stream is reconstructed to the video pixel data and timing signals and delivered to TCON inside the test chip for panel display. Thus, a DisplayPort connector and a flexible flat cable connector for connecting to a panel are mounted on the board.

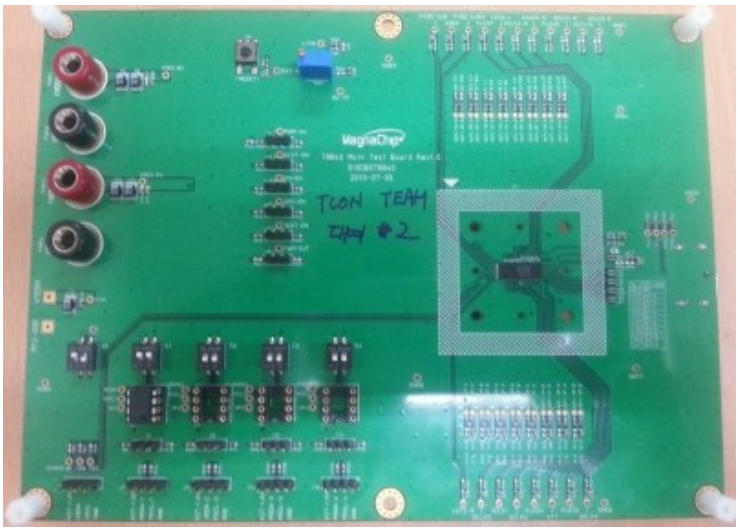


Fig. 4.27 Test board for measurement.

Table 4.2 Estimated area of digital block.

Hierarchical Cell	Percent Total	Gate Count	Estimated Area(mm^2)
Top	100	413712	3.01
PHY	7.8	32341	0.24
Link	53.9(12.8)	222703(52866)	1.61(0.38)
FIFO	41.1	169837	1.23
AUX	14.8	61403	0.45

Table 4.2 shows the estimated area of the link layer which is implemented in digital circuit design. The data is extracted from back-end process of the digital block. It occupies 3.01 mm^2 with a dual-port SRAM that used as the FIFO form clock domain crossing between the link symbol clock and the video stream clock. The power break downs of the electrical PHY layer are presented in Table 4.3 and Table 4.4. The measured power is almost the same with expected results of simulations. The summary of the measured power consumption for the overall receiver is presented in Table 4.5. The physical layer dissipates 21 mW at 1.62 Gb/s and 29 mW at 2.7 Gb/s with 2-lane operation. The power consumption of the link layer is 31 mW at 1.62 Gb/s and 41 mW at 2.7 Gb/s with 2-lane operation. Total power consumptions are about 52/70 mW at 1.62/2.7 Gb/s data rate with 2-lane operation.

Table 4.3 Average current of electrical PHY in RBR mode

Block		1.2V	1.8V	Comments
CDR	Equalizer	0.8 mA	0	
	Phase Detector	2.0 mA	0	
	LDO + DCO	0.5 mA	1.0 mA	
	Total	3.3 mA	1.0 mA	1 lane
AUX	Oscillator	0.3 mA	0	
	Driver/Receiver mode	16/0.5 mA	0	Normally receiver mode
HPD	Charge Pump	0	1.0 mA	
Video clock generator		4.6 mA	0	
BGR		0	0.5 mA	
Total		8.7 mA	2.5 mA	Assume aux receiver mode

Table 4.4 Average current of electrical PHY in HBR mode

Block		1.2V	1.8V	Comments
CDR	Equalizer	0.8 mA	0	
	Phase Detector	3.0 mA	0	
	LDO + DCO	1.0 mA	1.2 mA	
	Total	4.8 mA	1.2 mA	1 lane
AUX	Oscillator	0.3 mA	0	
	Driver/Receiver mode	16/0.5 mA	0	Normally receiver mode
HPD	Charge Pump	0	1.0 mA	
Video clock generation		7.6 mA	0	
BGR		0	0.5 mA	
Total		13.2 mA	2.7 mA	Assume aux receiver mode

Table 4.5 Summary of measured power consumption

RBR mode				
	PHY		**digital**	**Total (mW)**
	1.8V	**1.2V**	**1.2V**	
1lane	4.5	10.4	19	33.9
2lane	6.3	14.4	31	51.7
4lane	9.9	22.4	47	79.3
HBR mode				
	PHY		**digital**	**Total (mW)**
	1.8V	**1.2V**	**1.2V**	
1lane	4.9	15.8	25	45.7
2lane	7.1	21.6	41	69.7
4lane	11.8	33.2	56	101

Table 4.6 shows the comparison of this work with other CDR performances. Our work outperforms those in terms of the power consumption.

Table 4.6 Performance Comparison

	This Work	**2012[58]**	**2012[11]**	**2010[59]**
Data rate	1.62/2.7 Gb/s	1.62/2.7/5.4 Gb/s	1.62/2.7/5.4 Gb/s	1.62/2.7 Gb/s
Process	0.13 μm	65 nm	65 nm	0.13 μm
Supply	1.2 V	1.2 V	1.2 V	1.2 V
Power	7.9 mW @2.7 Gb/s	11 mW @2.7 Gb/s	147.6 mW @5.4 Gb/s	87 mW @2.7 Gb/s
BER	$< 10^{-12}$	$<10^{-12}$	$< 10^{-12}$	$<10^{-7}$
Jitter (rms/p-p)	5.1 ps /38 ps @2.7 Gb/s	5.6 ps /43.1 ps @2.7 Gb/s	3.2 ps /29.9 ps @5.4 Gb/s	29 ps /154 ps @2.7 Gb/s
Area	0.15 mm^2	0.12mm^2	0.44 mm^2	0.4 mm^2

Chapter 5

Proposed Video Clock Synthesizer and Frequency Control Scheme

5.1 Motivation

In a digital display interface, the video clock synthesis is essential to transfer the video data to a display device. Due to the various resolution of the display device, different bit number for the color depth, and the different frame rates, wide range clock frequencies should be synthesized for supporting each display. The frequency synthesizer is essential to generate video clock frequencies. As discussed in the previous chapters, PLL-based frequency synthesizer has been the most popular choice

for video clock generation. However, it is difficult to design because M and N value is very large so that it should have a very large number front driver and very high multiplication ratio which results in a low loop bandwidth and poor performance such as slow dynamics, high 1/f noise, and large jitter. A direct all-digital frequency synthesizer is suitable architecture for the DisplayPort application because the wide output frequency range and the fast frequency switching can be achieved more easily compared to the PLL-based design. Since there already are multi-phased clocks which are the recovered link symbol clocks, only a little additional hardware is required to enhance the resolution.

There are two decoupled clock domains, which are the recovered link symbol clock and the reconstructed video stream clock. The transmitted video data must pass the boundary of them. An asynchronous FIFO is contained to pass multi-bit values between the completely decoupled clock domains. During the FIFO operation, the write clock is the fixed rate but the read clock varies over wide range depending on the display types. Since the M and N value is the only way to determine the video clock frequency. The transmitted M value should be accurate enough to synthesize fine video clock frequency. If the transmitted M value has some errors, the video data throughputs of the transmitter and the receiver are not the same due to the frequency offset. This can raise serious problems in FIFO operation which cause data to be lost due to FIFO overflow or invalid data to be read from the FIFO due to an attempt to read the same data again. There are several systematic elements that cause the M value error in data transport services. The proposed scheme makes up the M value error by monitoring FIFO status and applies the modified M value to the frequency synthesizer core.

5.2 Proposed Video Clock Synthesizer

Fig. 5.1 illustrates the architecture of the proposed direct all-digital frequency synthesizer. It is composed of a phase interpolator, a programmable integer divider, a multi-phase aligning block, a phase selector and a divider-merged DSM. The operation of the proposed frequency synthesizer is based on the phase-switching fractional divider which exploits a phase-switching technique for a non-integer fractional divider. Whereas the phase-switching for the fractional part of the frequency division is performed before the integer divider in the previous works, the proposed architecture divides the input recovered clock with the programmable integer divider first and the fractional part divider switches the phase of the integer-divided clocks which are aligned with the multi-phase clocks. This reduces the burden of the phase switching because the extended switching timing margin can be obtained by lowering the clock frequency.

The M and N value which are extracted from the data stream fed into the divider merged DSM. The first order DSM is used for an arithmetic divider to generate the division ratio (Q, F) by dividing N by M. The upper 9-bit value Q is used for the programmable integer divider and the lower 4-bit value select the phase for the fractional part division. The phase interpolator generates evenly spaced 16-phase clocks from 8 multi-phase clocks from a clock and data recovery (CDR) circuit used in this work. The integer-divided clock from the programmable integer divider is aligned with the 16 multi-phase clocks from the phase interpolator by the multi-phase align-

er and delayed by several cycles for the switching timing margin of the phase selector. Usually, a glitch problem is one of the critical drawbacks of the phase-switching technique and some additional logics or complicated operations are required for the glitch-free design. However, in this architecture, the glitch-free phase switching can be achieved simply by delaying the multi-phase aligned clocks for a few cycles. The operational principle is illustrated in Fig. 5.2. The phase selection signal is calculated every video clock cycle with 1.5-cycle delay by DSM. The phase switching timing margin and the glitch-free design is attained by delaying the multi-phase aligned clocks for 3 cycles. As the DSM switches phase shift value k and k+1 with a specific ratio, the period of the video clock is varies between the adjacent multi-phase aligned clocks which exhibits the maximum deterministic jitter of TRCVDCLK/16. The amount of the deterministic jitter is acceptable due to the high bit rate of the recovered clock.

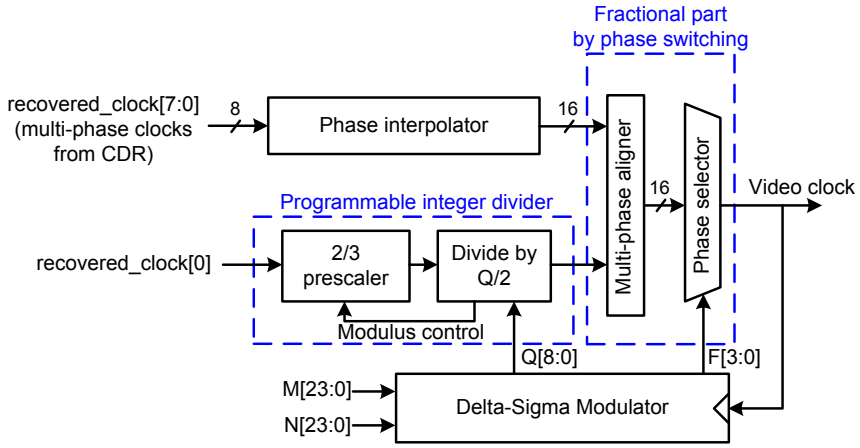


Fig. 5.1 Proposed direct all-digital frequency synthesizer architecture.

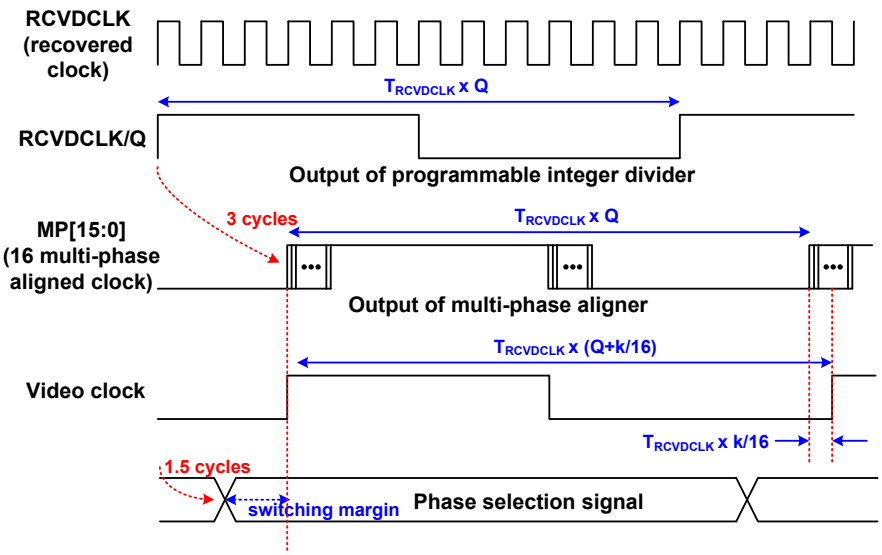


Fig. 5.2 Operational principle of the proposed architecture.

The programmable integer divider is composed of the conventional 2/3 dual-modulus prescaler and the counter-based divide-by-Q/2 using RS-latch. Since the integer divisor Q is 9 bit value, it is not easy to design counter-based integer divider operate at 1.35 GHz which is the maximum frequency of the recovered clock. The prescaler helps the divider to operate at a high frequency by dividing by 2 or 3 depending on the modulus control (MC) signal [60], [61]. The flow char of the operation of the programmable integer divider is shown in Fig. 5.3. When Q is even (Q[0]=0), the prescaler acts as divide-by-2 with MC = 0. Otherwise, the prescaler divides the input clock by 3 with MC = 1. After pre-dividing the input clock, the divide-by-Q/2 block increases the value of the counter by one every output clock of the prescaler. If the value of the counter reaches to Q/4, the RS-latch reset the output

signal to be zero which means a falling edge of the divided clock. The counter is still increasing and the output signal goes to high when the value of the counter is equal to Q/2. At every rising edge of the divided clock, the value of the counter resets to zero. It does not require an additional circuit to correct the duty cycle of 50%. If the second LSB of Q is one, which means value of Q/2 is an odd number, the RS-latch resets the output on the falling edge of the output clock of the prescaler. This method facilitates the duty cycle of the divided clock to approach as close to 50% without any duty cycle correction circuit. Since the value of Q/4 is obtained simply by shifting 2 bits of Q, the value of Q must not be smaller than 4.

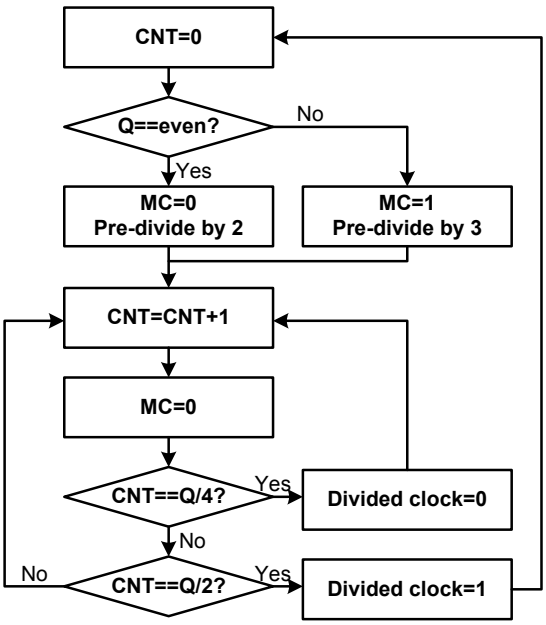


Fig. 5.3 Flow chart of the operation of the programmable integer divider.

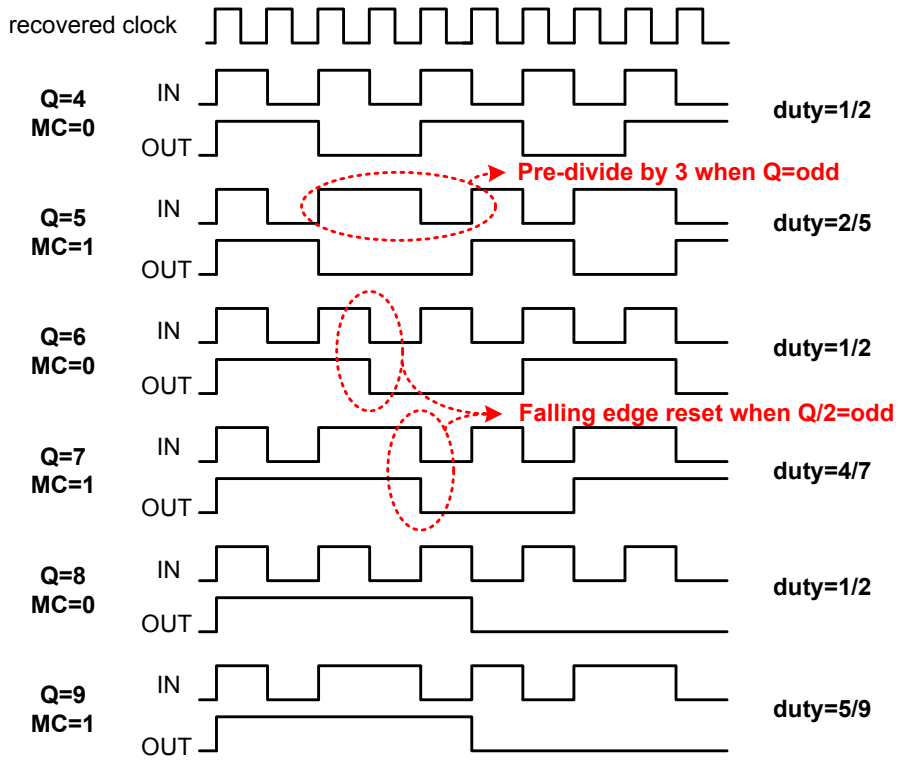


Fig. 5.4 Timing diagram of divide-by-Q/2.

In DisplayPort applications, Q is always larger than 4 for all supported display types. However, even if an unexpected instant situation happens, it can be recovered to the normal operation by the additional logic which makes N the arbitrary number 16 when N is smaller than 4. Fig. 5.4 illustrates the timing diagram of the divide-by-Q/2 block. The output of the prescaler is IN of the divide-by-Q/2 block and OUT is the divided output of the overall programmable integer divider. With the even value of the divisor Q, the prescaler always operates as divider-by-2 and the duty

cycle of 50% can be achieved by triggering the output signal on the next falling edge of the pre-divided clock when the value of the counter reaches to Q/4. Although the perfect duty cycle correction cannot be accomplished for the odd value of Q, only a half cycle of the recovered clock is the amount of the duty cycle mismatch for all possible Q values in this design.

5.3 Building Blocks

There are 8 multi-phase clocks recovered from the CDR in this work. Since the accuracy of the synthesized frequency is determined by the space of the multi-phase clocks, the phase interpolator is used to produce more number of multi-phase clocks for the finer resolution. The implementation of the phase interpolator is shown in Fig. 5.5. The phase interpolator is constructed by the simple dual-input inverting buffers which shorts the output signals of the two inverters to produce the medium phase between the two input signals [62].

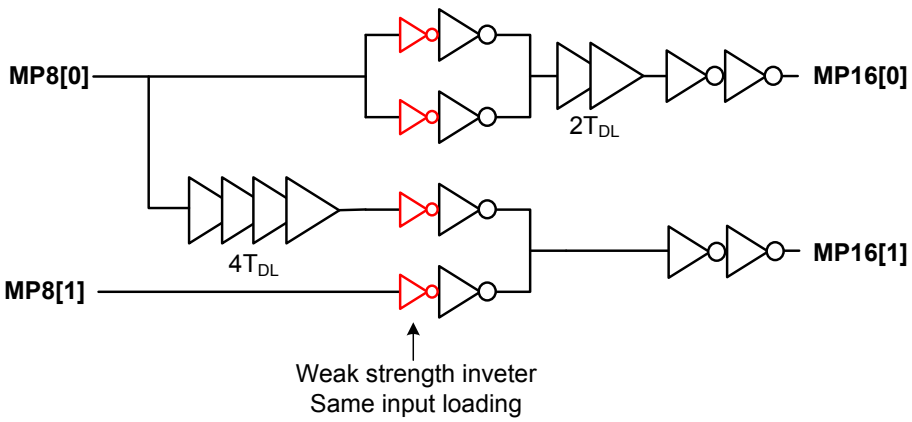


Fig. 5.5 Phase interpolator.

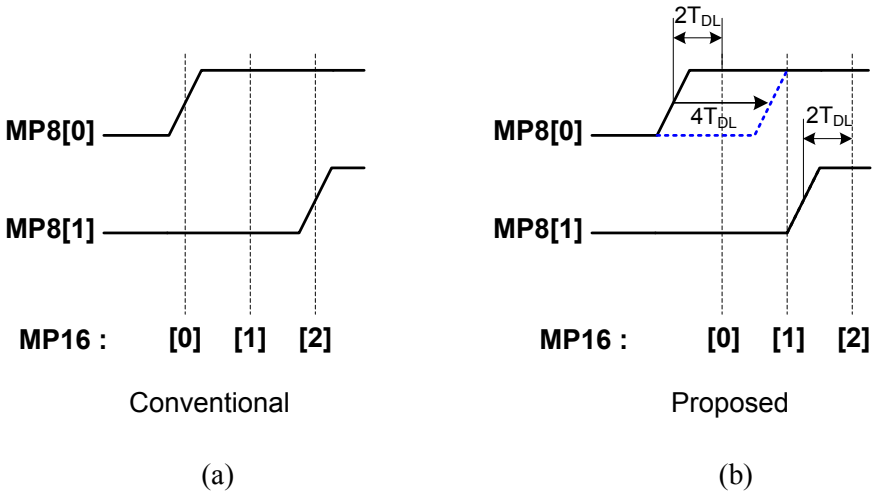


Fig. 5.6 Timing diagrams of (a) the conventional phase interpolator and (b) the proposed architecture.

The wide overlap of the transition times of the two input signals is required for the linearity of the multi-phase output signals. The weak strength inverts are inserted on each input stages to reduce the slew rate of the input signals for the wide overlapping time. And the uniformity of the output phases is improved by inserting delay elements on the input and output stages [63]. The timing diagram of the input and output signals of the phase interpolator is presented in Fig. 5.6. In the conventional case, the overlapping of the input signals may not be good, which results in a poor linearity. On the other hands, in the proposed architecture, the transitions of the input signals can overlap by inserting the delay elements. The phase of the output signal is not related to the delay of the buffer (T_{DL}).

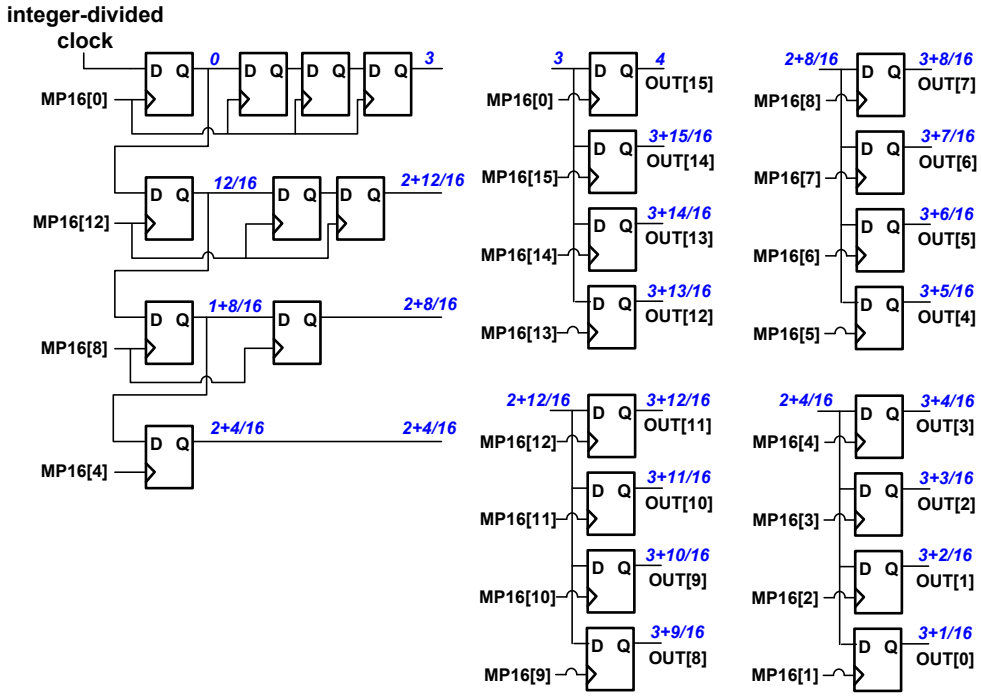


Fig. 5.7 Multi-phase aligner.

The integer-divided clock should be aligned by the multi-phase outputs of the phase interpolator in order to select the phases for the fractional part of the frequency division. The multi-phase aligner samples the integer-divided clock with the multi-phase clock. For the switching timing margin of the phase selection, the clocks are delayed by 3 cycles. The implementation of the multi-phase aligner is illustrated in Fig. 9. In the figure, the annotated numbers are relative delay from MP[0]. The timing violation may occur due to the narrow space of the multi-phase clocks when sampling in consecutive order. First, the sampling is performed by the 12-spaced

multi-phase clocks to generate 3, 2+12/16, 2+8/16 and 2+4/16 cycle delayed clocks. Each delayed clock is sampled by the rest of phases far away from it. All the flip-flops have enough timing margin for sampling in this architecture.

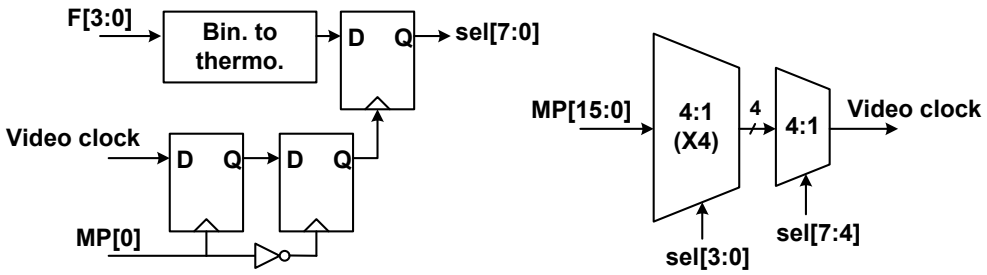


Fig. 5.8 Phase selector.

Fig. 5.8 shows the block diagram of the phase selector which is simply cascaded-MUX structure. The fractional resolution is assumed to be 4-bit and it is converted to 8-bit thermometer code that is used for selecting the phase with two 4:1 cascaded-MUXs. The additional glitch rejecting circuit is unnecessary due to the sufficient timing margin provided by the multi-phase aligner as explained in the previous section.

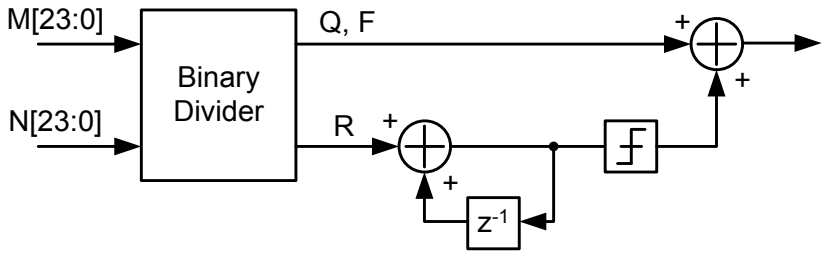


Fig. 5.9 Divider-merged DSM.

The DSM shown in Fig. 5.9 generates 13-bit binary number for the division ratio N/M which is to be used in the fractional divider. Upper 9-bit Q[8:0] is used for integer division and lower 4-bit F[3:0] is used for fractional division. Though the output of the DSM is quantized to finite bit length, the granularity of the frequency synthesis is not restricted due to the dithering of the DSM. But the dithering of the division ratio induces a bang-bang jitter to the output clock. The expected amount of this systematic jitter in the proposed architecture is bounded to the time difference of two adjacent multi-phase clocks in the view of period jitter or cycle-to-cycle jitter which is one of the most important measures of the video clock performance.

5.4 Frequency Error Compensation

The asynchronous FIFO, which is implemented as a dual-port memory, is included in the design for clock domain crossing. While a dual-line buffer is used in the first chip, a single-line buffer is used in this design to reduce the area of the memory. Since it occupies relatively large area compared to the other digital logic, the reduced FIFO size results in substantial area saving.

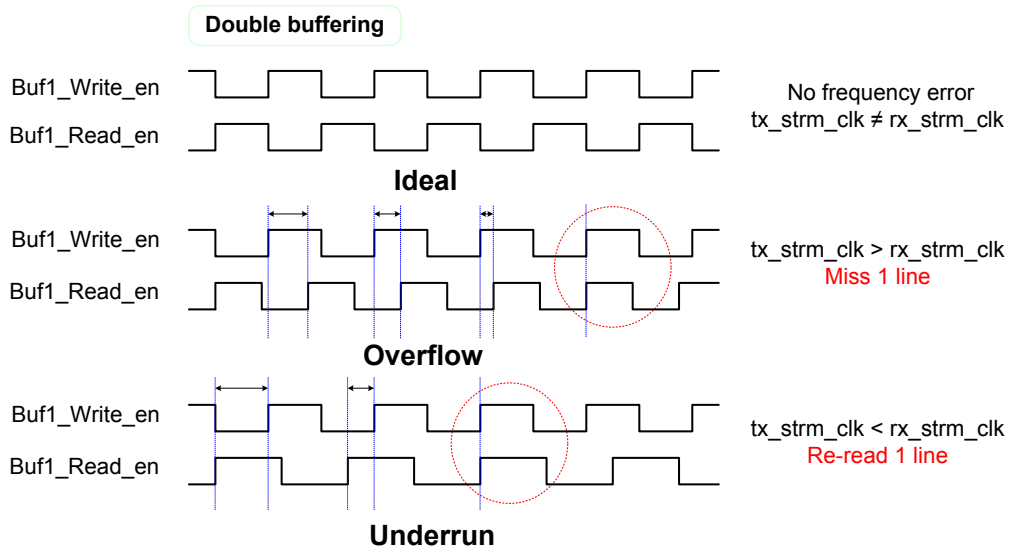


Fig. 5.10 False operation of FIFO.

Basically, the FIFO operation should be stable, which means writing rate and reading rate must be same not to cause false operation. In other words, the write pointer and the read pointer must keep a steady distance. In this system, the write clock is the link symbol clock recovered from the data stream with a fixed data rate and the read clock is the video stream clock generated by the frequency synthesizer which is a flexible frequency depends on the video resolution. If the throughputs of each clock are different, the FIFO false operations happen. The data in the FIFO is lost due to FIFO overflow or invalid data is read from the FIFO due to an attempt to read the same data again as shown in Fig. 5. 10 [64]-[66].

The key factor that maintains the stable operation of the FIFO is the transmitted M value for regenerating the video stream clock. It is the only way for the receiver to obtain the information of the video stream clock. Therefore, when the transmitted M value is wrong, the frequency of the video stream clock has an offset from the pixel rate of the source device. It causes the difference of throughputs between the writing rate and the reading rate in the FIFO operation. As a result, the false operation of the FIFO brings the display noise in the sink device such as a vertically shifted display.

There are some reasons that raise an error in the transmitted M value. First of all, M cannot express the exact ratio between the link rate and the pixel rate due to its finite bit length. It has a quantization error to represent the fractional ratio with the digital value. If M value is not precisely calculated in the source, the regenerated video stream clock with the transmitted M value has the frequency offset for sure. M is typically calculated every N cycles of the link symbol clock and it is transmitted in the blanking period. As shown in Fig. 5.11 and Fig. 5.12, the update rates of M

value in the source and the sink are different. It raises the frequency error in a specific duration. If the size of the FIFO is large enough to endure the frequency offset for a while, the frequency is compensated with the next updated M value. However, the reduced size of the FIFO makes it fragile to tolerate a frequency offset. Moreover, a video clock in the source may have the spread spectrum clocking and the timing jitter also affects the calculation of M value.

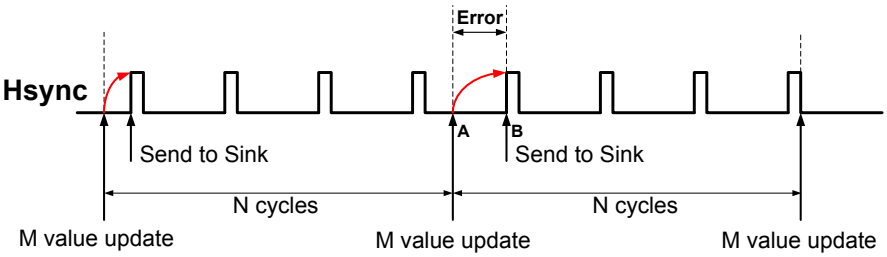


Fig. 5.11 Update rate of M value.

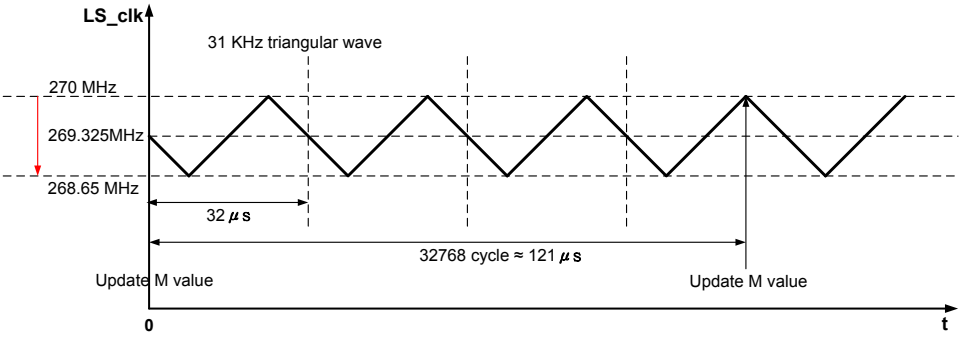


Fig. 5.12 M value error with spread spectrum clocking.

In order to prevent the false operation of the FIFO, the frequency error calculation scheme is proposed. Fig. 5.13 shows the proposed frequency compensation scheme which operates with the video stream clock generator. By monitoring the FIFO states of writing and reading pointers, when the distance between the pointers becomes far or close, the M value is modified to make the generated video stream clock faster or slower. The gain control block adjusts the amount of the compensation according to the monitoring status. M value filtering is included not to update when different between old M and new M is too large. It prevents the drastic change of the video clock frequency. The filter block employs moving average topology for gradual change of the M value. The amount of the compensation is 30~600 KHz, so that the variation of the video stream clock frequency does not exceed 0.5%.

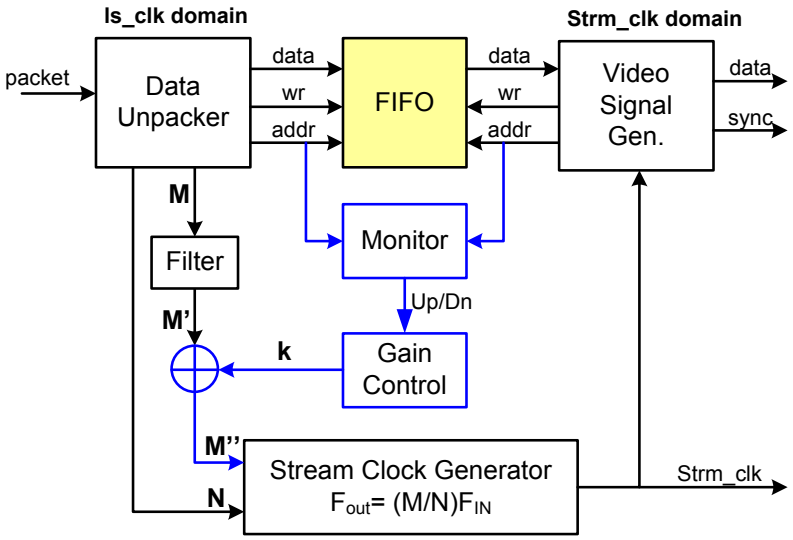


Fig. 5.13 Proposed frequency compensation scheme.

With the proposed scheme, it is possible to use well-known fixed M value for generating the video clock frequency while excluding the transmitted M value. The proposed frequency compensation scheme guarantees the stable FIFO operation by adjusting the video stream clock frequency minutely.

5.5 Experimental Results

The output frequency range of the video stream clock generator is 25 to 330 MHz to support up to the resolution of 2560x1600@60Hz. The top simulation result of the frequency synthesizer is shown in Fig. 5.14. The desired output frequency is 85.4956 MHz with N=32768 and M=10376. The output frequency is dithering from 85.4 to 85.7 MHz and the overall effective frequency is the same with the desired value.

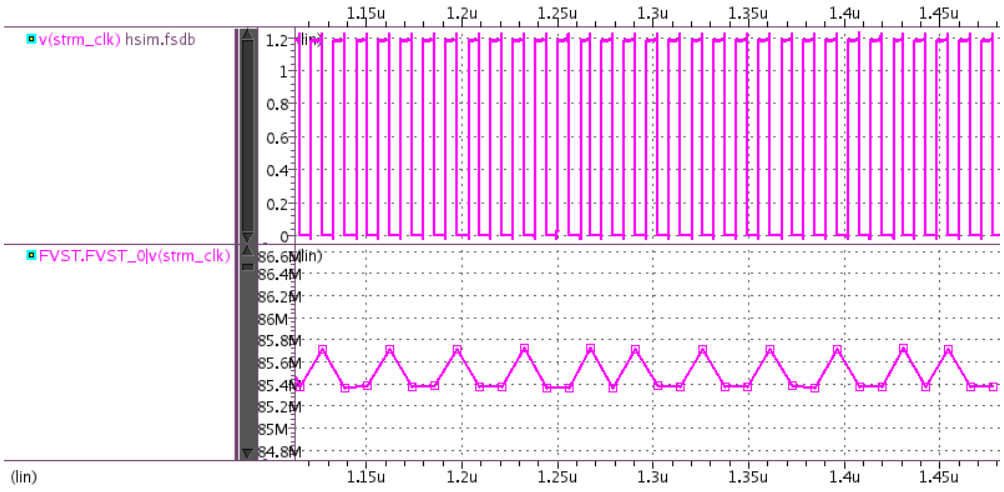


Fig. 5.14 Top simulation result of the frequency synthesizer.

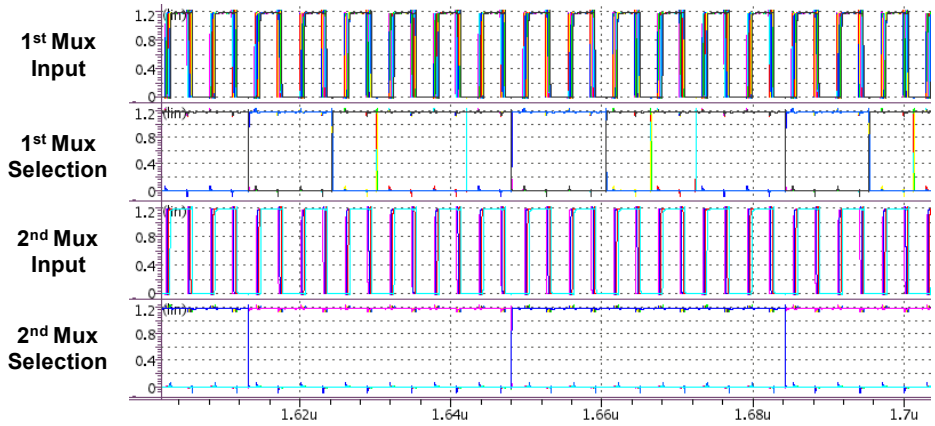


Fig. 5.15 Simulation result of phase selection.

Fig 5.15 presents the waveform of the phase selector inputs and selection of the output frequency. The inputs of the first MUX stage are aligned to 16 multiphase signals. The first MUX stage selects four multiphase signals among them and the final output phase is selected by the second MUX stage. As expected, there are enough switching margin to make the output glitch-free.

The simulation result of the frequency change is shown in Fig. 5.16. With the link rate of 2.7 Gb/s, the output frequency is changed according to the display resolution. It changes the display resolution from HD to FHD at 2 μs and to WQXGA at 3.25 μs. The frequency lock time is less than dozens of nanosecond due to its direct digital synthesis method that takes few clock cycles to generate the output frequency. The power break down of the frequency synthesizer depends on the integer divider value is presented in Fig. 5.17.

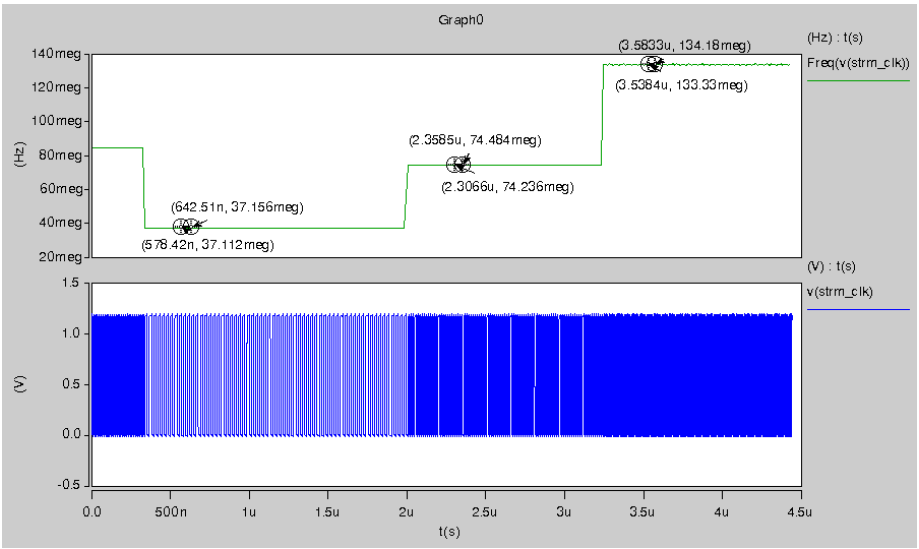


Fig. 5.16 Simulation result of frequency conversion.

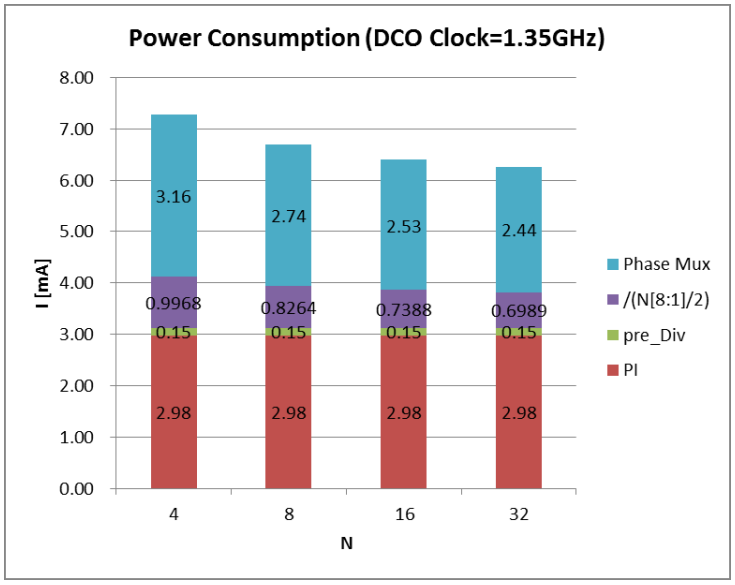


Fig. 5.17 Simulated power breakdown of the frequency synthesizer.

The simulation result of the FIFO normal operation is presented in Fig. 5.18. In the normal case, the distance between write pointer and read pointer should be maintained at the half line. However, if there is an error in the transmitted M value, the reconstructed video stream clock has an offset with the source video clock. It cause the mismatch of the throughputs in the FIFO operation. Fig. 5.19 shows the simulation result of the FIFO false operation. The video stream clock in the receiver is not accurate since the transmitted M value has an error. The read pointer is advanced to the write pointer at some point, so that the false operation happens. It appears as the vertical shift of the display on the panel. The proposed frequency error compensation scheme resolves the problem by monitoring the FIFO status and keeping the distance.

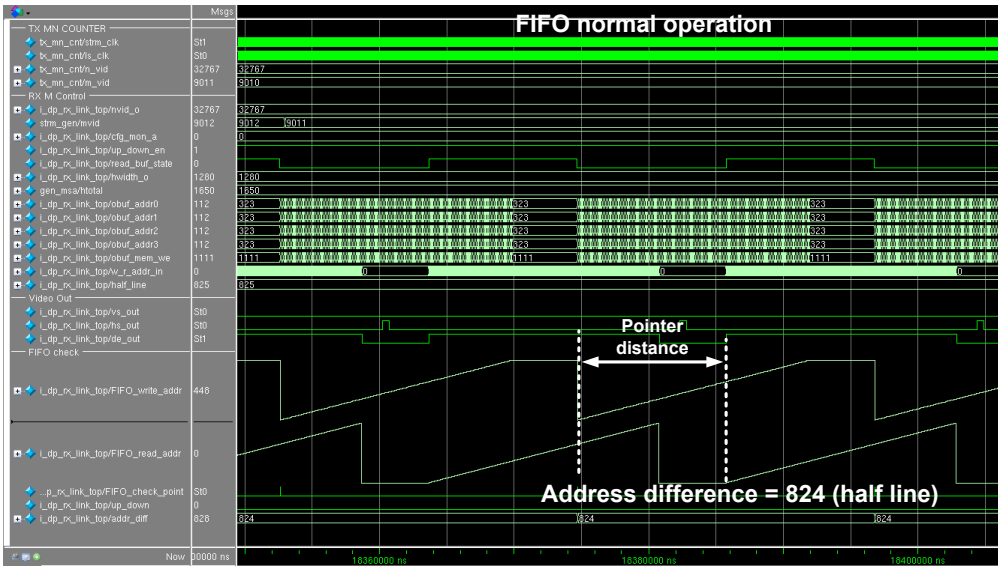


Fig. 5.18 Simulation result of FIFO normal operation.

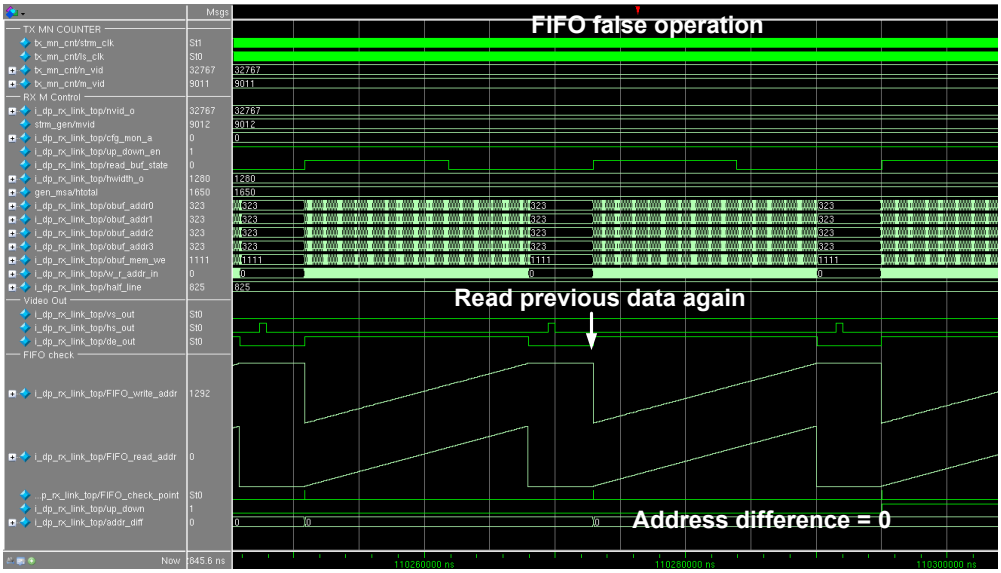


Fig. 5.19 Simulation result of FIFO false operation.

Figures from 5.20 to 5.22 show the jitter performances of the video pixel clock. The division number of each measurement is set to 20, 20+1/16 and 20+1/24+1/48 respectively. The measured peak-to-peak jitter is 38 ps, 49 ps and 83 ps respectively. The last figure shows that the systematic bang-bang jitter due to the dithering of the DSM. The histogram is in accordance with the input. One third of the output frequency is divided by 20+2/16 and the others are divided by 32+1/16 as expected. The distance of the two peaks of histogram is close to the phase difference of 46.3 ps between two adjacent 16-phase clocks at 1.35 GHz. The measured peak-to-peak jitter is just 0.56% of the period for the video pixel clock frequency of 67.2 MHz. A comparison of the frequency synthesizer with other works is shown in Table 5.1.

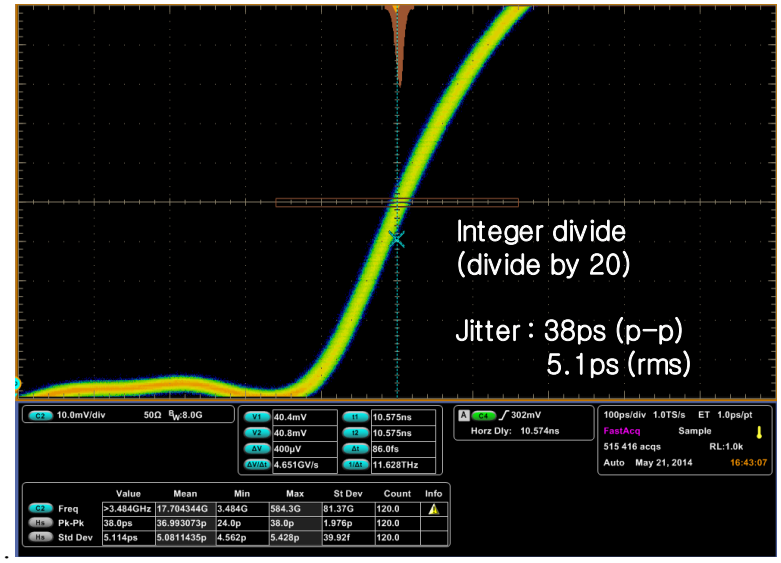


Fig. 5.20 Measured jitter with division number 20 (integer).

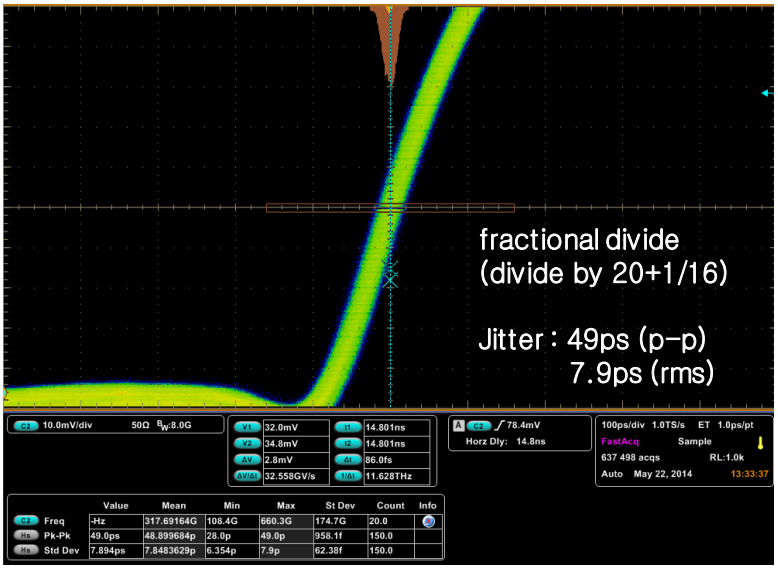


Fig. 5.21 Measured jitter with division number 20+1/16 (fractional).

Fig. 5.22 Measured jitter with division number 20+1/24+1/48 (DSM dithering).

Table 5.1 Performance Comparison

	This Work	**2009[27]**	**2007[5]**	**2006[6]**
Frequency Range	2.6 MHz ~ 330MHz	1.3 MHz ~ 330MHz	2 MHz ~ 196 MHz	2.4 MHz ~ 378 MHz
Design Approach	DDFS	DDFS	DDFS	ADPLL
Process	0.13 μm	0.13 μm	90 nm	0.18 μm
Supply	1.2 V	1.2 V	1.1 V	1.8 V
Power	9.1 mW @1.35 GHz	31 mW @1.35 GHz	10 mW @1.2 GHz	15 mW @378 MHz
Jitter (p-p)	83 ps @67.2 MHz	120 ps @42 MHz	90ps @148.5 MHz	208ps @134.7 MHz
Area	0.12 mm^2	0.24 mm^2	0.15 mm^2	0.16 mm^2

Chapter 6

Conclusion

In this thesis, two receivers for the digital display interface are presented. One is a 5.4/2.7/1.62-Gb/s multi-rate receiver for DisplayPort version 1.2 which supports external box-to-box connections with flexible cable length and the other is a 2.7/1.62-Gb/s multi-rate receiver for Embedded DisplayPort which is used for intra-panel display connections.

All digital clock and data recovery circuit is employed to recover the link clock from the data stream. The proposed clock recovery scheme can significantly shorten the time to recover from the link failure with the benefit of ADCDR topology. Once the link is established after link training, the ADCDR memorizes the DCO codes of the synchronization state and when the loss of synchronization happens, it restores the previous DCO code so that the clock is quickly recovered from the failure state without the link re-training.

The proposed direct-digital frequency synthesizer is fairly suitable for generating

the video stream clock since the video clock frequency has wide range to cover all display formats and is determined by the division ratio of large M and N values. The proposed frequency synthesizer using a programmable integer divider and a multi-phase switching fractional divider with the delta-sigma modulation exhibits better performances and reduces the design complexity operating with the existing clock from the ADCDR circuit. The proposed frequency error compensation scheme enhances the stable operation of the asynchronous clock system. The transmitted frequency ratio M and N values may not be accurate due to its low update rate, transport latency and quantization error. It can cause false operations of the asynchronous FIFO which is used for clock domain crossing. The proposed frequency error compensation scheme resolves these problems by monitoring the status of FIFO between the clock domains.

The fabricated chips can be well used as the future digital display interfaces with the advantages of the proposed schemes. The all digital topology is fairly suitable for the display system with the advanced technology. And the direct digital frequency synthesis is easily expandable for the growing video resolution without additional design complexity.

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초 록

본 논문에서는 기존의 DVI, HDMI, LVDS 등을 대체하는 고속 디지털 디스플레이 인터페이스인 DisplayPort 수신기의 설계를 제안한다. 첫 번째 칩은 5.4/2.7/1.62-Gb/s 의 전송률을 지원하는 DisplayPort 수신기이고 두 번째 칩은 내부 패널 연결에 사용되는 2.7/1.62-Gb/s 의 전송률을 지원하는 Embedded DisplayPort (eDP) 수신기이다.

첫 번째 수신기는 외부 디스플레이 장치를 연결하는데 사용되고 최대 21.6 Gb/s 의 전송률을 지원하여 4K (4096x2160)의 해상도를 가지는 디스플레이까지 전송 가능하다. 두 번째 수신기는 노트북이나 태블릿 PC 등의 내부 칩 간의 연결에 사용하기 위한 목적으로 설계되었다. 최대 전송률은 4 개의 채널을 사용하였을 때 10.8 Gb/s 이고 WQXGA (2560x1600)의 해상도까지 지원한다. DisplayPort 에는 클럭 채널이 따로 없기 때문에 전송되는 데이터에서 클럭을 복원하기 위한 Clock and Data Recovery (CDR) 회로가 필요하다. 본 설계에서는 All-Digital CDR (ADCDR)을 적용하여 면적 효율을 높이고 성능을 향상시켰다. 데이터 전송률은 고정되어 있는데 반해 비디오 클럭 주파수는 지원하는 디스플레이 포맷에 따라 다양하기 때문에 넓은 범위를 가지는 주파수 합성기가 필요하다.

송신기는 비디오 데이터를 보내기 전에 link training 을 통해 클럭을 복원하도록 한다. 또한 데이터 전송 중에 채널에 문제가 발생한 경우 다시 link training 을 하여 전송 환경을 초기화 한다. 이러한 link training 을 수행하는데 수 ms 의 시간이 소요되기 때문에 수신단의 비디오 화면이 link training 기간 동안 정상적으로 디스플레이 되지 않는다. 제안하는 클럭 복원 구조를 이용하면 채널에 문제가 발생했을 때 link training 을 수행하지 않고 바로 정상 동작으로 복귀하도록 하여 디

스플레이 노이즈가 발생하는 시간을 상당히 줄였다. 정상적인 link training 이 수행된 경우의 ADCDR 환경을 저장해 놓은 뒤, 문제가 발생했을 때 정상 동작 환경으로 바로 복귀하는 방식을 사용하였다.

비디오 클럭 주파수를 합성하기 위해 direct all-digital 주파수 합성기를 제안한다. 제안된 주파수 합성기는 가변 정수 디바이더와 위상 선택을 통한 소분할 디바이더로 구성되어 있고 델타 시그마 모듈레이터를 통해 성능을 향상시켰다. DisplayPort 는 비동기식 클럭 시스템이기 때문에 전송되는 M 값에 의해 비디오 클럭의 주파수가 결정되는데 전송되는 M 값에 오차가 있을 경우 비디오 클럭이 정확하게 합성되지 않아서 문제가 생기게 된다. 이러한 문제를 해결하기 위해 FIFO 를 관찰하여 주파수 에러를 보상해 주는 구조를 제안한다.

첫 번째 칩은 65-nm CMOS 공정으로 제작되었고, PHY 는 1.39 mm2, Link 는 2.26 mm2 의 면적을 차지한다. PHY 는 1.62/2.7/5.4 Gb/s 전송률의 4 채널 동작에서 각각 86/101/116 mW 의 전력을 소모하고, Link 는 각각 107/145/167 mW 를 소모한다. 두 번째 칩은 0.13 μm CMOS 공정으로 제작되었고, PHY 는 1.59 mm2, Link 는 3.01 mm2 의 면적을 차지한다. PHY 는 1.62/2.7 Gb/s 전송률의 2 채널 동작에서 각각 21/29 mW 의 전력을 소모하고, Link 는 각각 31/41 mW 를 소모한다. 비디오 클럭 주파수 합성기의 면적은 0.04 mm2 이고, 1.62 Gb/s 에서 5.5 mW, 2.7 Gb/s 에서 9.1 mW 의 전력을 소모하며 출력 주파수 범위는 25~350 MHz 이다.

주요어 : 디스플레이포트, 고속시리얼링크, 디스플레이 인터페이스, 비디오 클럭 합성, 비디오 클럭 주파수 에러 보상

학 번 : 2009-30188