



저작자표시-비영리-변경금지 2.0 대한민국

이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:



저작자표시. 귀하는 원저작자를 표시하여야 합니다.



비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.



변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 [이용허락규약\(Legal Code\)](#)을 이해하기 쉽게 요약한 것입니다.

[Disclaimer](#)

Ph.D. DISSERTATION

L-shaped Tunnel Field-Effect Transistors
(L-shaped TFETs) with High Current
Drivability and Low Subthreshold Swing

높은 구동 전류와 낮은 문턱전압 이하 스윙을 가
지는 L자 형태의 터널링 전계효과 트랜지스터

BY

SANG WAN KIM

February 2014

DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

L-shaped Tunnel Field-Effect Transistors (L-shaped TFETs)
with High Current Drivability and Low Subthreshold Swing

높은 구동 전류와 낮은 문턱전압 이하 스윙을 가지는
L자 형태의 터널링 전계효과 트랜지스터

指導教授 朴 炳 國

이 論文을 工學博士 學位論文으로 提出함

2014 년 2 월

서울대학교 大學院

電氣·情報 工學部

金 相 完

金相完의 工學博士 學位論文을 認准함

2014 년 2 월

委 員 長 : 박 명준 (印)

副委員長 : 박 병국 (印)

委 員 : 이 종호 (印)

委 員 : 조 성재 (印)

委 員 : 최 우영 (印)



Abstract

In order to solve power crisis in highly-scaled CMOS technology, a novel tunnel field-effect transistors (TFETs), named L-shaped TFETs, have been proposed and its electrical properties are examined. It features band-to-band tunneling (BTBT) direction parallel to the normal electric field induced by gate electrode. Because carrier injection is occurred perpendicular to the channel direction, cross-sectional area and barrier width of BTBT junction could be defined by structural parameters.

Using the commercial TCAD device simulator, its electrical characteristics are examined and optimized. It is expected that the L-shaped TFETs will reveal better performance than conventional ones in terms of subthreshold swing (S), on-current (I_{on}) and short channel effect. In addition, the performance of L-shaped TFET inverters has been compared with that of conventional TFET ones for its complementary logic application.

After the key process techniques are obtained, control and comparison samples are fabricated at Inter-University Semiconductor Research Center (ISRC) of Seoul National University (SNU), Korea. The main process technique is as follow: in-situ doped epitaxial layer growth for constantly doped source region, selective epitaxial layer growth of silicon at low temperature for tunneling region, and guarantee sub-3-nm gate dielectric.

From the electrical measurement of transfer and output characteristics, it is verified that 102 mV/dec minimum S in conventional TFET is improve to 7, 34 and 59 mV/dec in L-shaped TFET. In addition, the I_{on} of L-shaped TFET is more than 10 times larger than that of conventional one. Extracting several parameters such as source/drain resistance, channel resistance, mobility, and tunneling resistance, it is clear that the improved performance comes from the reduction of tunneling resistance.

From this study, it is demonstrated that L-shaped TFET will be one of the most promising candidate for a next-generation low-power device.

Key Words: band-to-band tunneling, tunnel field-effect transistor, TFET, low-power device, L-shaped TFET, subthreshold swing, current drivability

Student Number: 2008-30869

Contents

Abstract.....	i
Contents	iii
List of Tables.....	v
List of Figures	vi

Chapter 1

Introduction	1
1.1 NECESSITY OF ALTERNATIVES TO CMOS	1
1.2 TUNNEL FIELD-EFFECT TRANSISTORS (TFETs)	4
1.3 TECHNICAL ISSUES OF TFETs	7
1.4 SCOPE OF THESIS	10

Chapter 2

L-shaped TFET	11
2.1 FEATURES OF L-SHAPED TFET.....	11
2.2 DESIGN OPTIMIZATION	17
2.3 CORNER EFFECT	27
2.4 FURTHER IMPROVEMENT AND CIRCUIT APPLICATION	36
2.5 SUMMARY OF TARGET DEVICE	40

Chapter 3

Device Fabrication	42
3.1 FABRICATION OF CONTROL TFETs	42
3.2 KEY PROCESS DESIGNS FOR L-SHAPED TFETs	45
3.3 FABRICATION OF L-SHAPED TFET	51
3.4 SIDEWALL SPACER FOR MINIMIZATION OF MIS-ALIGNMENT	56

Chapter 4

Device Characteristics	59
4.1 METAL-OXIDE-SEMICONDUCTOR (MOS) CAPACITOR.....	59
4.2 CONTROL SAMPLES OF CONVENTIONAL PLANAR TFETs	63
4.3 L-SHAPED TFETs	71
4.4 EXTRACTION OF SEVERAL ELECTRICAL PARAMETERS	76

Chapter 5.....	80
-----------------------	-----------

Conclusions	80
--------------------------	-----------

Bibliography	82
---------------------------	-----------

Abstract in Korean.....	89
--------------------------------	-----------

Curriculum Vitae	91
-------------------------------	-----------

List of Tables

Table. 2.1 Simulated Device Parameters to Test Basic Operation of L-shaped TFET	12
--	-----------

List of Figures

Chapter 1

Fig. 1.1 Trade-off correlation between I_{off} and V_{th} scaling.....	2
Fig. 1.2 The V_{dd} reduction can be achieved by the use of steeper switching device without I_{on} and I_{off} degradation	3
Fig. 1.3 Schematic diagram of n-channel TFET structure. In the case of p-channel TFET, n^+ -doped source and p^+ -doped drain is used. In general, the TFET is fabricated on the silicon-on-insulator (SOI) substrate to suppress junction leakage current through the substrate	5
Fig. 1.4 Energy band diagram of n-channel TFET from source to drain. The TFET is under (a) off-state and (b) on-state	6
Fig. 1.5 Technical issues of TFETs. The simulation is done for and n-channel TFET with the gate length (L_g) of 50 nm and gate dielectric of 2-nm silicon dioxide (SiO_2). Simulation tool: Silvaco Atlas TM	7
Fig. 1.6 Conventional planar TFETs with (a) low- V_g and (b) high- V_g . The tunneling junction is turned-on in sequence depending on V_g and gradual doping profile.....	9

Chapter 2

Fig. 2.1 Simulated device structure of (a) planar TFET and (b) L-shaped TFET. The insets of figures indicate electron tunneling direction.....	13
Fig. 2.2 2-D contour plot of electron BTBT current. (a) Planar and (b) L-shaped TFET. Simulation tool: Silvaco Atlas TM	14
Fig. 2.3 Energy band diagrams of a conventional TFET along the line from the source to the channel at a distance of 5 Å below SiO_2 -Si interface with the variation of V_g . Simulation tool: Silvaco Atlas TM	16

Fig. 2.4 Energy band diagrams of an L-shaped TFET from the source to the gate dielectric via tunneling region, at the middle of Si mesa region with various V_g 's. Simulation tool: Silvaco Atlas TM	17
Fig. 2.5 (a) Transfer curves with the variation of L_t . (b) Extracted $V_{\text{turn-on}}$ and S_{avg} . Simulation tool: Silvaco Atlas TM	20
Fig. 2.6 (a) An equivalent capacitor model between the gate and the source. (b) Relationship between ϕ_s , ε and L_t at $V_g - V_{\text{fb}} = 1$ V. Simulation tool: Silvaco Atlas TM	21
Fig. 2.7 (a) Transfer curves with the variation of H_t . The inset shows the relationship between $V_{\text{turn-on}}$ and H_t . (b) I_{on} as a function of H_t . Simulation tool: Silvaco Atlas TM	23
Fig. 2.8 Transfer curves of conventional and L-shaped TFETs. Simulation tool: Silvaco Atlas TM	24
Fig. 2.9 Transfer curves with the variation of L_g . (a) Planar and (b) L-shaped TFETs. Simulation tool: Silvaco Atlas TM	26
Fig. 2.10 Transfer curves simulated by Synopsys Sentaurus TM and Silvaco Atlas TM . Due to a kink, S_{avg} and I_{on} properties are degraded	27
Fig. 2.11 2-D contour plots of BTBT rates with various V_g 's. Simulation tool: Synopsys Sentaurus TM	28
Fig. 2.12 (a) Schematic diagram of an L-shaped TFET with rounded source corner and several device parameters. (b) 2-D contour plot of dopant concentration based on device simulation. (c) 2-D contour plot of doping concentration and depletion region. (d) Extracted doping profile at source and channel junction indicated in Fig. 2.12(b). Simulation tool: Synopsys Sentaurus TM	30, 31
Fig. 2.13 Transfer curves with the structure shown in Fig. 2.12(b). Simulation tool: Synopsys Sentaurus TM	32
Fig. 2.14 Key fabrication steps	34
Fig. 2.15 (a) Device structure obtained by process simulation. The critical process conditions are listed in the inset. Shortly, the thickness of epitaxially grown Si for	

source (T_{source}) is 40 nm and the amounts of Si etch for mesa (T_{mesa}) is 70 nm. (b) Transfer curves simulated with the device in Fig. 2.15(a). Simulation tool: Synopsys Sentaurus TM	35
Fig. 2.16 Schematic of an inverter and its input pulse	37
Fig. 2.17 (a) Transfer and (b) output curves of n-and p-channel L-shaped TFETs. Simulation tool: Silvaco Atlas TM	38
Fig. 2.18 Transient simulation results of L-shaped TFETs inverters with various gate dielectric. (a) Transient simulation results, (b) an enlarged image of indicated region in (a), and (c) extracted delay time. Simulation tool: Silvaco Atlas TM	39, 40

Chapter 3

Fig. 3.1 Device fabrication flow for conventional planar TFETs.....	43
Fig. 3.2 Microtrenching effect	44
Fig. 3.3 Gate patterning with two-tiered RIE process.....	45
Fig. 3.4 Modified fabrication flow	46
Fig. 3.5 TEM images about SEG process with source formed by ion implantaion .	47
Fig. 3.6 (a) TEM image and (b) SIMS profile of epitaxially grown source region ..	48
Fig. 3.7 SIMS profile from SEG region to source	49
Fig. 3.8 TEM images of tunneling region, <i>i.e.</i> SEG region	50
Fig. 3.9 SEM images after mesa patterning. (a) Source and channel. (b) Drain. The inset of Fig. 3.9(a) is TEM image at the same point after all the process is finished	53
Fig. 3.10 In-line SEM image after photolithography of PLY layer.....	54
Fig. 3.11 TEM image of High- κ /metal gate stack.....	54
Fig. 3.12 TEM images after TiN gate patterning. (a) Source and (b) drain side.....	55
Fig. 3.13 TEM images of fabricated L-shaped TFET	56
Fig. 3.14 Modified process flow to minimize mis-alignment	57
Fig. 3.15 SEM images of TiN sidewall spacer	58

Chapter 4

Fig. 4.1 C - V curves of MOSCAP using high- κ /metal gate stack. The symbols represent measured results with four different frequencies of 50, 100, 200, 300 kHz and the solid lines denote compensated C - V curves using two-frequency method with different six combinations of four frequencies ($4C_2 = 6$). They are converged on one curve and EOT is calculated from that.....	60
Fig. 4.2 Two-frequency method to remove frequency dispersion components	61
Fig. 4.3 (a) Extracted EOTs and (b) V_{fb} as a function of HfO_2 thickness	62
Fig. 4.4 (a) Transfer and (b) output curves of n-channel TFETs	64
Fig. 4.5 (a) Transfer and (b) output curves of p-channel TFET	65
Fig. 4.6 Output characteristics of (a) n- and (b) p-channel TFETs.....	68
Fig. 4.7 Simulated output characteristics of n-channel TFET. Simulation tool: Synopsys Sentaurus TM	69
Fig. 4.8 Ambipolar behavior caused by V_d . (a) Energy band diagrams. (b) 2-D contour plot of BTBT rates. Simulation tool: Synopsys Sentaurus TM	70
Fig. 4.9 A p-i-n junction characteristic depending on V_d	72
Fig. 4.10 (a) Transfer and (b) output curves of n-channel L-shaped TFETs.....	73
Fig. 4.11 Comparisons of fabricated TFETs	74
Fig. 4.12 Hysteresis in transfer characteristics	75
Fig. 4.13 R_{sd} extraction with Terada-Muta method.....	77
Fig. 4.14 μ_{eff} as a function of (a) V_g and (b) \mathcal{E}_{eff}	78
Fig. 4.15 Extraction of (a) R_{ch} from MOSFETs and (b) R_{tun} from TFETs.....	79

Chapter 5

Fig. 5.1 Transfer curves of L-shaped TFETs using Si and SiGe source with HfO_2 gate dielectric. Simulation tool: Synopsys Sentaurus TM	81
---	----

Chapter 1

Introduction

1.1 Necessity of Alternatives to CMOS

Although the integration density of transistor has been rapidly increased, the reduction of supply voltage (V_{dd}) has been behind the scaling speed of device size, since the development of metal-oxide-semiconductor field-effect transistor (MOSFET) and commercial integrated circuit (IC) from Bell laboratory in 1960 and from Fairchild Semiconductor Corporation in 1961, respectively [1], [2]. As a result, power density has been increased exponentially and now, it is one of the most important constraints for the CMOS design. In addition, the exploding mobile market including smart phones, tablet personal computers (PCs), and wearable computers using flexible display technique also demand high-energy efficiency and low operating and standby power semiconductor devices.

In order to reduce dynamic power (CV_{dd}^2f) as well as static power ($I_{off}V_{dd}$) of semiconductor device, the V_{dd} should be scale down. However, scaling of threshold voltage (V_{th}) is contradictory to off-state leakage current (I_{off}) which is proportional to $\exp(-qV_{th}/mk_B T)$ as presented in Fig. 1.1. In the exponential expression, q represents electron charge and k_B , m , and T denote Boltzmann's constant, body coefficient, and temperature. In addition, without the V_{th} scaling, reduction of V_{dd} results in poor current drivability. In order to overcome above mentioned problems, there have been several approaches and significant changes over the last decades. For example, strained silicon (Si) technology, high- κ /metal gate stack, and FinFET based tri-gate structure have been introduced at 90, 45, and 22-nm technology nodes, respectively [3].

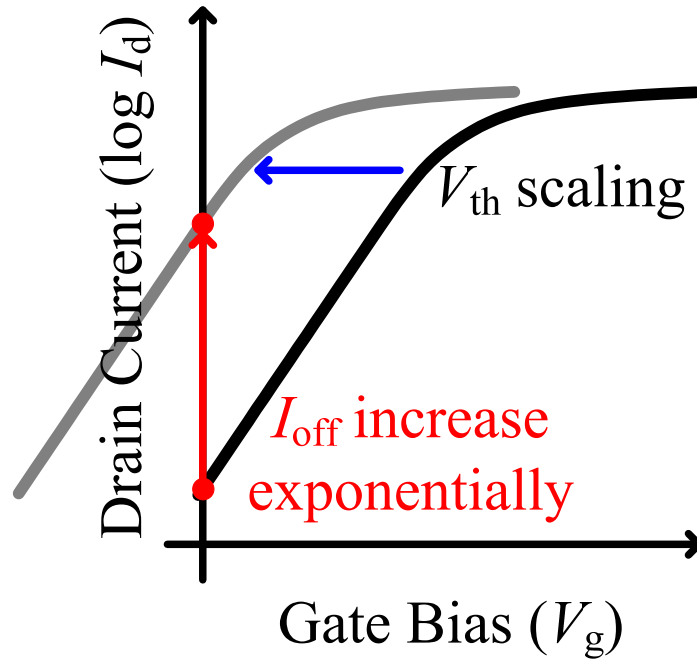


Fig. 1.1. Trade-off correlation between I_{off} and V_{th} scaling.

In spite of these efforts, the V_{dd} below 0.6 V still remains one of the most difficult roadblocks for further scaling of MOSFETs [4]. For the reduction of power consumption in transistors while maintaining high on-current (I_{on}) and low-level I_{off} , subthreshold swing (S) as well as V_{dd} should be scaled down (Fig. 1.2). However, MOSFETs cannot implement sub-60-mV/dec ($\sim 2.3k_B T/q$) S at room temperature because they use thermionic emission as a carrier injection mechanism [5]. Therefore, a novel device based on the different operation mechanism is necessary for sub-60-mV/dec S and further V_{dd} reduction.

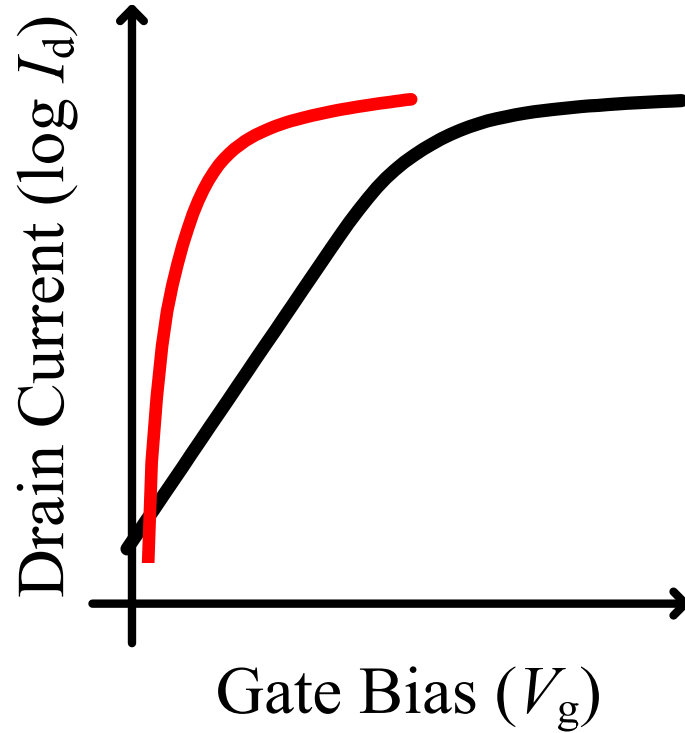


Fig. 1.2. The V_{dd} reduction can be achieved by the use of steeper switching device without I_{on} and I_{off} degradation.

1.2 Tunnel Field-Effect Transistors (TFETs)

In order to reduce S below 60 mV/dec, various novel devices such as the impact-ionization MOS devices, nano-electro-mechanical FETs, negative gate capacitance FETs, and TFETs have been proposed [5-8]. Among them, a TFET is considered one of the most promising candidates for ultra-low-power application due to complementary MOS (CMOS) process compatibility and scalability.

As shown in Fig. 1.3, the TFET is a gated p-i-n diode operating under reverse bias. In the case of n-channel TFET, source, drain and channel form $p^+ - i - n^+$ structure. Unlike the MOSFETs, carrier injection of TFET is based on band-to-band tunneling (BTBT). In off-state, the energy band diagram from source to drain is depicted in Fig. 1.4(a). Because the conduction band minimum of channel ($E_{C-ch,min}$) is higher than valence band maximum of source ($E_{V-s,max}$), the valence electrons at the source cannot find any empty state. Therefore, there exists only a very small leakage current that comes from drift of minority carriers and tunneling to the trap site in the energy gap (E_g). When the $E_{V-s,max}$ and $E_{C-ch,min}$ are aligned with gate bias (V_g), there exist plenty of empty states across the barrier. As a result, if the potential barrier is thin enough, a significant tunneling current starts to flow because the valence electrons appear at the channel depending on tunneling probability ($P_T(E)$). If the ideal triangular potential barrier is assumed, $P_T(E)$ is expressed as Eq. (1.1), (1.2). In these equations, m^* , \hbar , \mathcal{E} , and W_t denote electron effective mass, reduced Plank constant, electric field, and tunneling barrier width, respectively. Therefore, $P_T(E)$ increases exponentially as a function of V_g [9].

$$P_T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3q\hbar\mathcal{E}}\right) \quad (1.1)$$

$$\mathcal{E} = \frac{E_g}{qW_t} \quad (1.2)$$

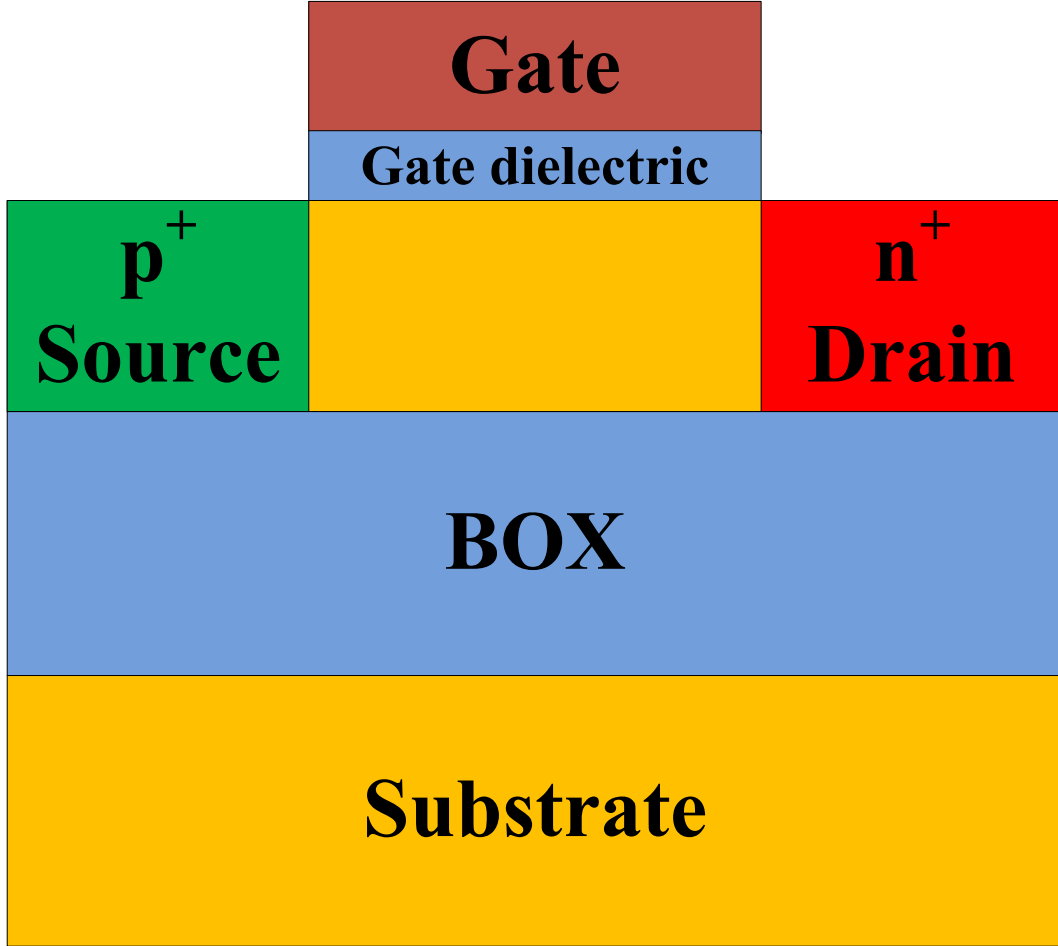


Fig. 1.3. Schematic diagram of n-channel TFET structure. In the case of p-channel TFET, n⁺-doped source and p⁺-doped drain is used. In general, the TFET is fabricated on the silicon-on-insulator (SOI) substrate to suppress junction leakage current through the substrate.

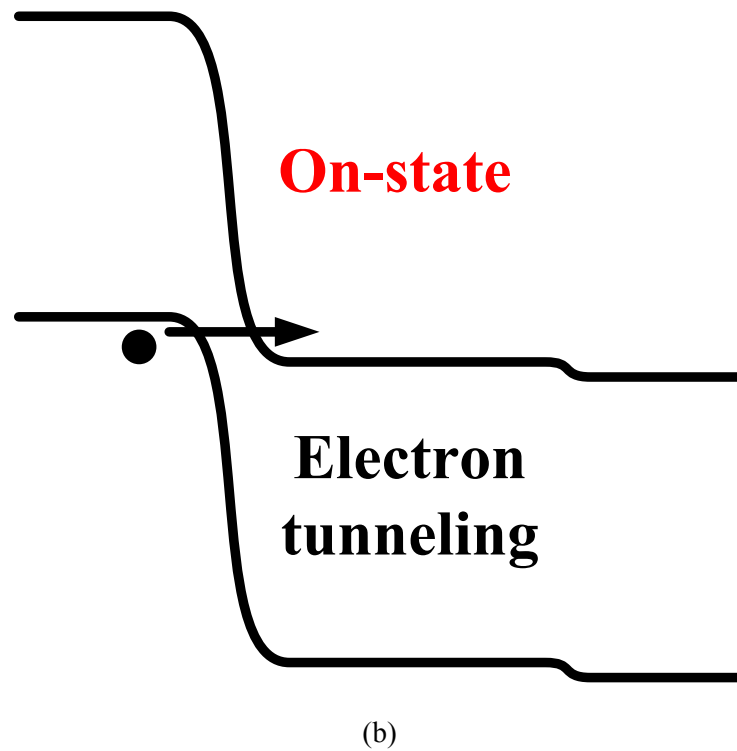
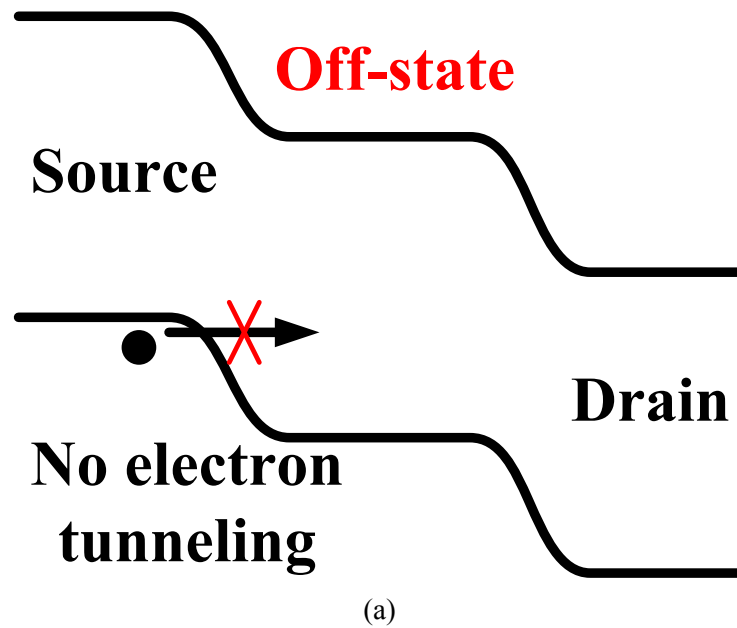


Fig. 1.4. Energy band diagram of n-channel TFET from source to drain. The TFET is under (a) off-state and (b) on-state.

1.3 Technical Issues of TFETs

Although the TFET has been regarded as one of the most prospective alternatives to MOSFETs in the future low-operating power branch, its commercialization has been blocked by several technical issues. In terms of device performance, they can be summarized by low I_{on} and larger S than theoretical prediction (Fig. 1.5), increased of I_{off} due to ambipolar behavior, and short channel effect (SCE) called drain-induced current enhancement (DICE) or drain-induced barrier thinning (DIBT) [10-16].

First of all, poor I_{on} is in part attributed to small tunneling junction cross-sectional area (A_t) determined by channel inversion layer thickness (only a few nm) [17-22]. In

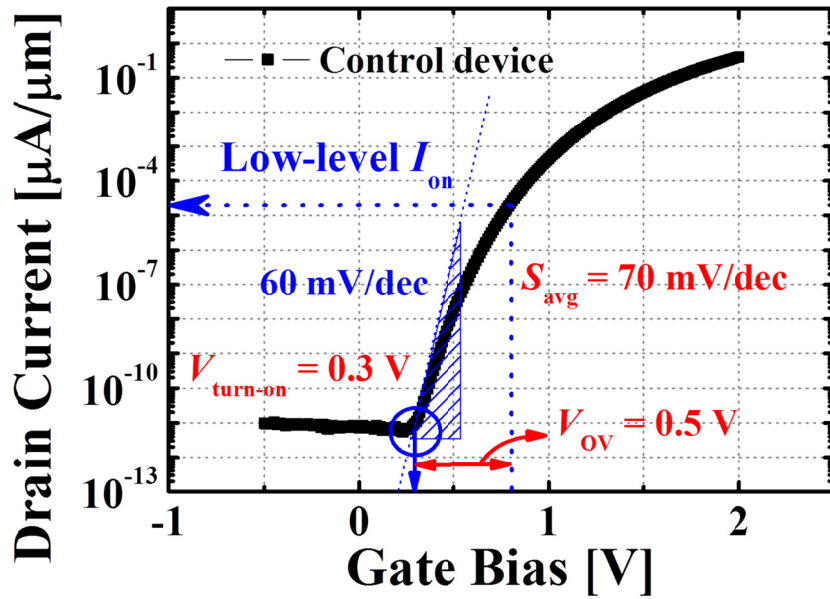


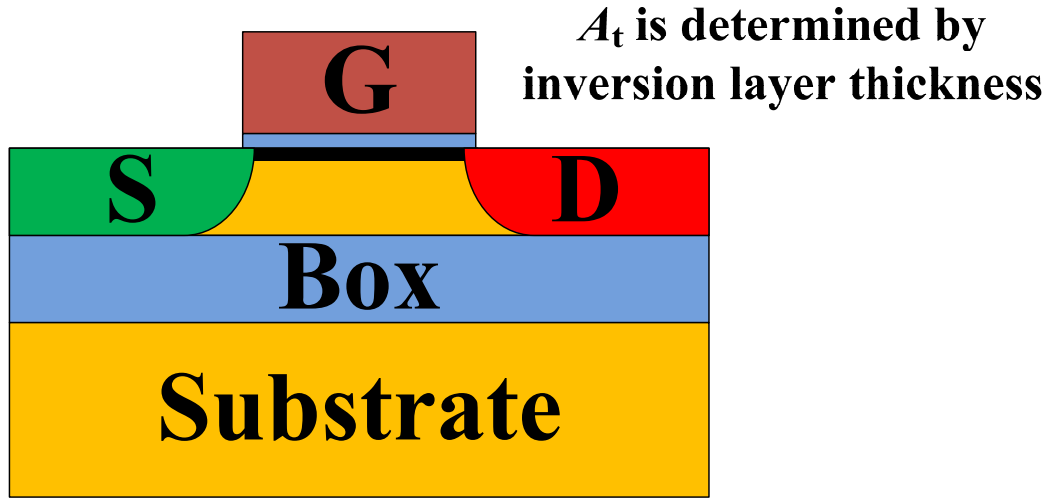
Fig. 1.5. Technical issues of TFETs. The simulation is done for an n-channel TFET with the gate length (L_g) of 50 nm and gate dielectric of 2-nm silicon dioxide (SiO_2). Simulation tool: Silvaco AtlasTM.

order to improve I_{on} , several strategies have been investigated. One of the approaches is the introduction of narrow E_g materials such as SiGe, Ge, GeSn, graphene, carbon nanotube (CNT), and III-V compound semiconductors. Because $P_T(E)$ is proportional to $\exp(-E_g^{3/2})$, the I_{on} is increased hyper exponentially with the help of alternative materials with smaller E_g . The other approach is the increment of A_t adopting a novel structure which uses BTBT current perpendicular to the channel.

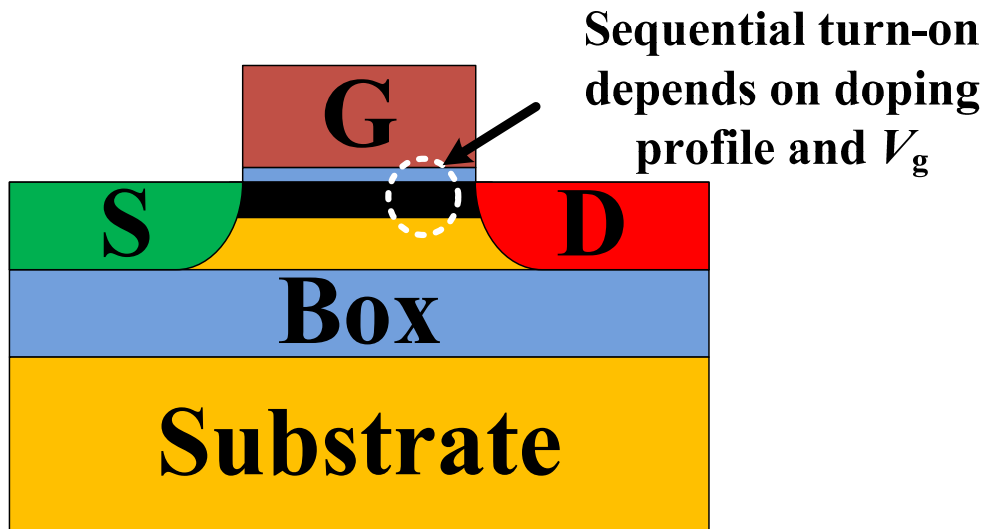
Secondly, the disappointing S characteristic is in part related to the dependency of tunneling barrier width (W_t) on V_g and in part related to sequential turning-on of devices due to the V_{th} variations caused by doping gradient (Fig. 1.6). A plenty of previous studies have revealed that abrupt doping profile is helpful for the scaling of S . For example, an introduction of n^+ -pocket region beside p^+ -source or dopant segregation method with the nickel (Ni) silicide process is well known representatives for abrupt band bending at source-channel junction. The other point of view, S of TFET is deeply related to W_t once the $E_{V-s,\text{max}}$ is horizontally aligned with the $E_{C-\text{ch},\text{min}}$. However, in the case of conventional TFETs, W_t is determined by junction depletion width (W_d) which is expressed as function of V_g . Consequently, it is difficult to achieve small W_t even if two energy bands are aligned. In addition, reduction of effective oxide thickness (EOT) of gate dielectric with the use of high- κ gate dielectric is also necessary for further improvement of S properties [16], [21-29].

Last of all, an ambipolar current (I_{amb}) comes from BTBT at channel/drain junction with negative V_g . In detail, if the gate is biased negatively, channel potential is decreased

and energy bands are aligned at the channel/drain junction. Finally, undesired tunneling current is flow and results in poor off characteristic. It could be restricted with the help of gate-drain underlap region and moderated doping concentration of drain [15], [18].



(a)



(b)

Fig. 1.6. Conventional planar TFETs with (a) low- V_g and (b) high- V_g . The tunneling junction is turned-on in sequence depending on V_g and gradual doping profile.

1.4 Scope of Thesis

According to the discussion so far, the main objective of this work is to present a novel TFET with high current drivability and low S . In order to achieve it, several strategies have been implemented with the help of novel structure. The key idea is that, unlike the conventional TFETs in which A_t and W_t are determined solely by the electrical field, the proposed device approaches the technical issues by converting them to design parameters.

In Chapter 2, L-shaped TFET features are examined and its design guidelines are determined with the help of TCAD device simulation of Silvaco AtlasTM and Synopsys SentaurusTM. In addition, complementary logic application of L-shaped TFETs is also examined by mixed-mode simulation. Chapter 3 will cover the key process flows for conventional planar TFET and L-shaped TFETs. After the fabrication flow of planar TFET is briefly introduced, the key process designs for L-shaped TFETs are explained in detail. In Chapter 4, electrical characteristics of fabricated device are examined. Here, metal-oxide-semiconductor capacitor composed of high- κ /metal gate stack will be reviewed first. Then, the electrical performance of the control group (planar TFETs) is compared with that of the L-shaped TFETs. Finally, in Chapter 5, the work will be concluded with summary and suggestions for future work.

Chapter 2

L-shaped TFET

In this chapter, the features of L-shaped TFET, the effect of device parameters, and the optimal fabrication flow considering corner effects are examined with the help of TCAD device simulation. A non-local BTBT model is used with Synopsys SentaurusTM (version G-2012.06 and H-2013.03) and Silvaco AtlasTM (version 5.16.3.R) [30-32]. According to the simulation purpose, more appropriate tool is selected for the high reliability and efficiency.

2.1 Features of L-shaped TFET

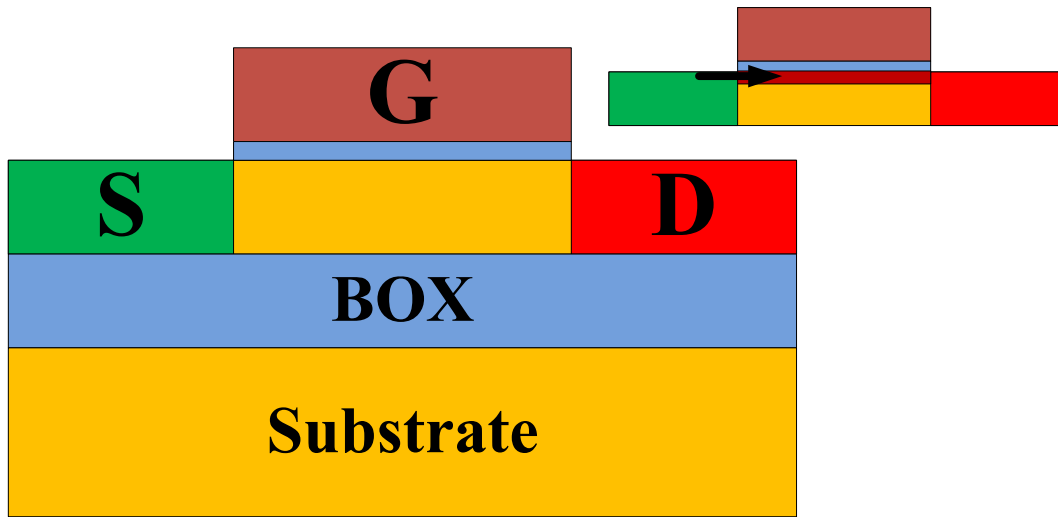
Figure 2.1 shows the simulated structure of a conventional and the proposed TFET to overcome previously mentioned TFETs' technical issues. The proposed one is called an "L-shaped TFET" because its channel resembles the alphabet L [20-22]. L-shaped TFETs feature mesa-shaped p⁺-doped source and intrinsic Si regions which are located between the source and the gate dielectric layer. The intrinsic Si layer is named as

“tunneling region” because it plays the important role of determining L-shaped TFETs’ electrical performance which will be discussed later. The length and height of a TFET are represented by L_t and H_t . The other device parameters are also listed in Table 2.1

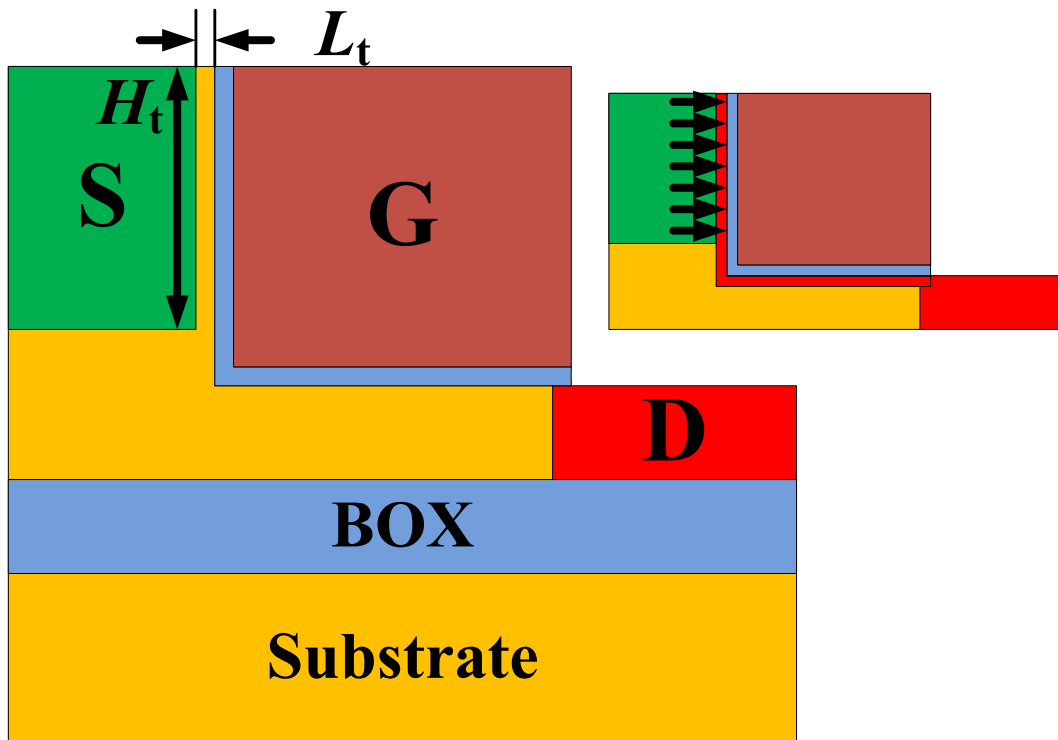
The results of L-shaped TFET simulation are as follows. First, as shown in the inset of Fig. 2.1(a), conventional TFETs have A_t defined by the channel inversion layer thickness which is only a few nm. Because BTBT current flows across the small cross-sectional area, low I_{on} is inevitable. On the other hand, L-shaped TFET shows BTBT current perpendicular to the channel direction as shown in the inset of Fig. 2.1(b). Thus, as H_t increases, A_t increases, and this leads to higher I_{on} . Fig. 2.2 shows two-dimensional (2-D) contour plot of electron BTBT rates for the conventional planar TFET and the L-shaped TFET when the devices are fully turned-on. Unlike the planar TFET, the L-shaped TFET shows BTBT occurred all over the tunneling region simultaneously with almost the same amount.

Table. 2.1. Simulated Device Parameters to Test Basic Operation of L-shaped TFET

Symbol	Quantity	Magnitude
L_g	lateral gate length	50 nm
T_{ox}	EOT of gate dielectric	2 nm
T_{SOI}	SOI thickness	20 nm
H_t	height of tunneling region	40 nm (variable)
L_t	length of tunneling region	4 nm (variable)
\mathcal{W}_{fin}	gate work function	n ⁺ -polycrystalline Si (poly-Si)
N_S	doping concentration of source	10^{20} cm^{-3}
N_B	doping concentration of body	10^{15} cm^{-3}
N_D	doping concentration of drain	10^{18} cm^{-3}

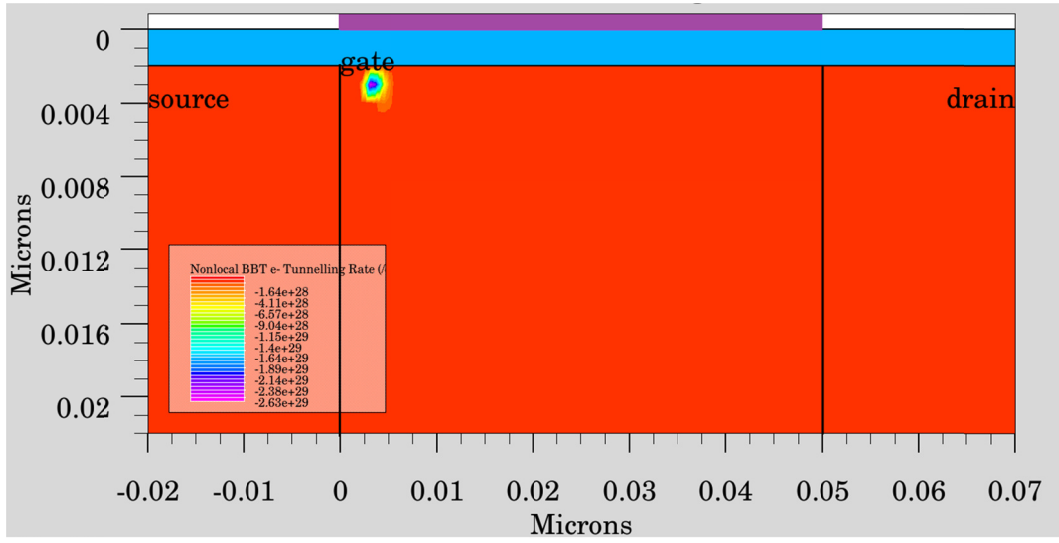


(a)

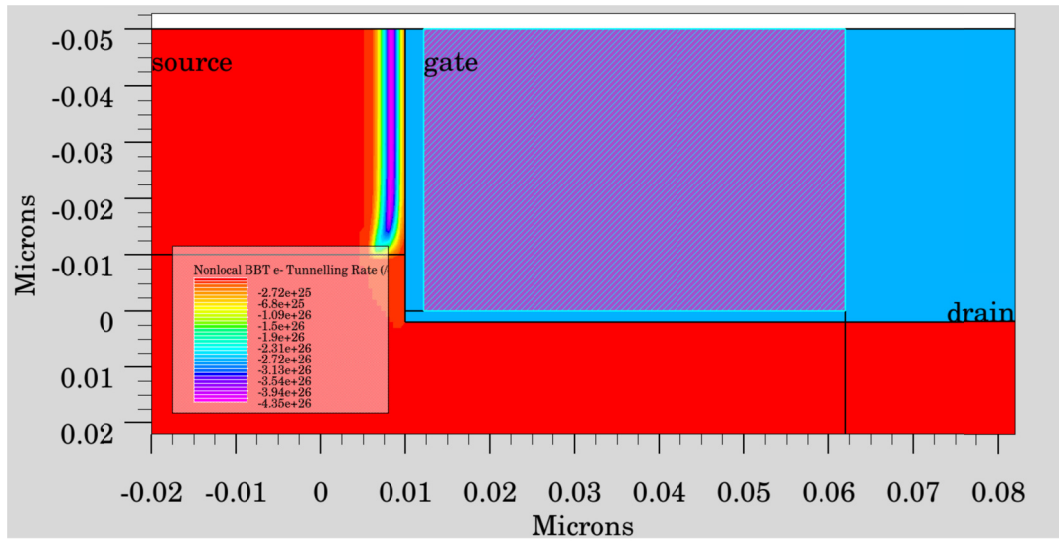


(b)

Fig. 2.1. Simulated device structure of (a) planar TFET and (b) L-shaped TFET. The insets of figures indicate electron tunneling direction.



(a)



(b)

Fig. 2.2. 2-D contour plot of electron BTBT current. (a) Planar and (b) L-shaped TFET. Simulation tool: Silvaco AtlasTM.

The other expected effect with L-shaped TFET is scaling of S . In order to induce BTBT, two conditions should be satisfied as mentioned in the previous chapter. First, $E_{V-s,max}$ should be aligned with the $E_{C-ch,min}$. Second, W_t between them should be small enough to induce BTBT because $P_T(E)$ depends on W_t hyper-exponentially. Among them, the latter factor of W_t , especially at the moment of both energy bands are aligned, is more deeply related to the determination of S characteristic. In other words, W_t should be small enough to induce large tunneling current when the device enters to the on-state, i.e. $E_{V-s,max}$ and $E_{C-ch,min}$ are aligned, for abrupt on-off transition [21]. Thus, the tunneling phenomenon can be discussed by using energy band diagrams as shown in Fig. 2.3 and 2.4.

In these figures, the hatched triangle shows the approximated BTBT barrier when the $E_{V-s,max}$ is aligned with the $E_{C-ch,min}$. In the case of conventional TFETs, as shown in Fig. 2.3, W_t varies as a function of V_g because it is determined by junction depletion width. At low V_g , although the $E_{C-ch,min}$ is aligned with the $E_{V-s,max}$, $P_T(E)$ is low due to large W_t . Thus, there still exists small BTBT current and it varies as a function of V_g . As a result, it makes the on-off transition less abrupt and the S larger. Furthermore, when the L_g is short, the I_{off} degrades the device performance severely, which is analogous to the punch-through current of MOSFETs.

On the other hand, in the case of L-shaped TFETs, as shown in Fig. 2.4, maximum W_t could be the same as L_t once $E_{V-s,max}$ is aligned with $E_{C-ch,min}$. It means that W_t is determined by L_t which is not controlled by electrical bias but defined by fabrication

process. At low V_g , L-shaped TFETs show low I_{off} in spite of small W_t because the valence electrons of source cannot “see” the empty state of channel at conduction band edge. Thus, L-shaped TFETs show lower S than conventional TFETs.

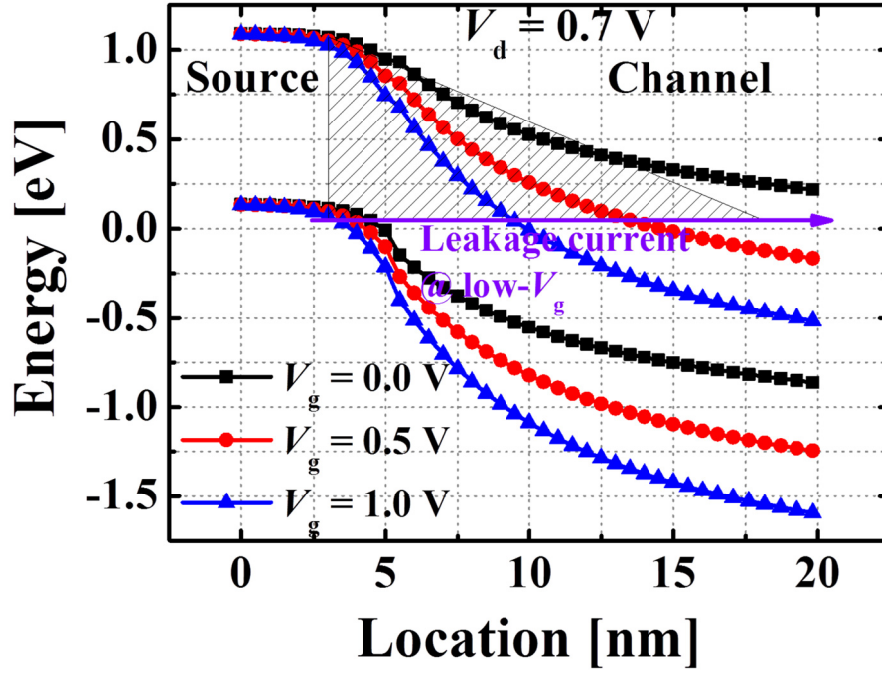


Fig. 2.3. Energy band diagrams of a conventional TFET along the line from the source to the channel at a distance of 5 Å below SiO_2 -Si interface with the variation of V_g . Simulation tool: Silvaco AtlasTM.

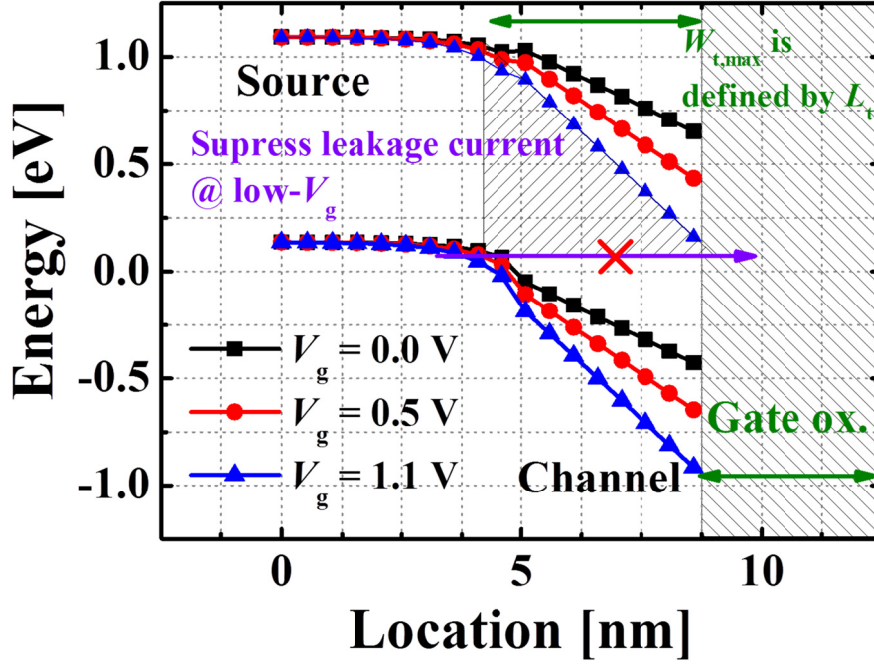


Fig. 2.4. Enegy band diagrams of an L-shaped TFET from the source to the gate dielectric via tunneling region, at the middle of Si mesa region with various V_g 's. Simulation tool: Silvaco AtlasTM.

2.2 Design Optimization

In order to analyze the effect of restricted W_t on S characteristics in more detail, the dependency of device performance on the L_t has been simulated. Because the drain current (I_d) of TFETs responds to V_g more sensitively than the case of MOSFETs, it is necessary to use modified metrics. In this study, the turn-on voltage ($V_{turn-on}$) and average S (S_{avg}) substitute for the V_{th} and S . $V_{turn-on}$ is defined as the V_g when BTBT conditions are satisfied and I_d starts to increase from the level of $\sim 10^{-12}$ $\mu A/\mu m$. On the

other hand, the S_{avg} indicates the reciprocal of mean ratio of change in the $\log(I_d)$ - V_g curve when I_d is increased by five orders of magnitude. I_{on} means the I_d where V_g is equal to gate overdrive (V_{ov}) [33].

Figure 2.5 shows transfer curves and extracted parameters under the various V_g condition. Fig. 2.5(b) shows that S_{avg} increases as L_t increases from 2 to 10 nm. When L_t is large, even if $E_{V-s,\text{max}}$ is aligned with $E_{C-\text{ch},\text{min}}$, W_t is still large, which is the same as in conventional TFETs. It leads to high I_{off} and large S_{avg} . Furthermore, I_{off} increase lowers $V_{\text{turn-on}}$ as shown in Fig. 2.5. On the other hand, as L_t becomes smaller, W_t gets smaller as long as $E_{V-s,\text{max}}$ is aligned with $E_{C-\text{ch},\text{min}}$. At the same time, it becomes more difficult to make $E_{V-s,\text{max}}$ aligned with $E_{C-\text{ch},\text{min}}$ due to small L_t . It results in small S_{avg} and high $V_{\text{turn-on}}$.

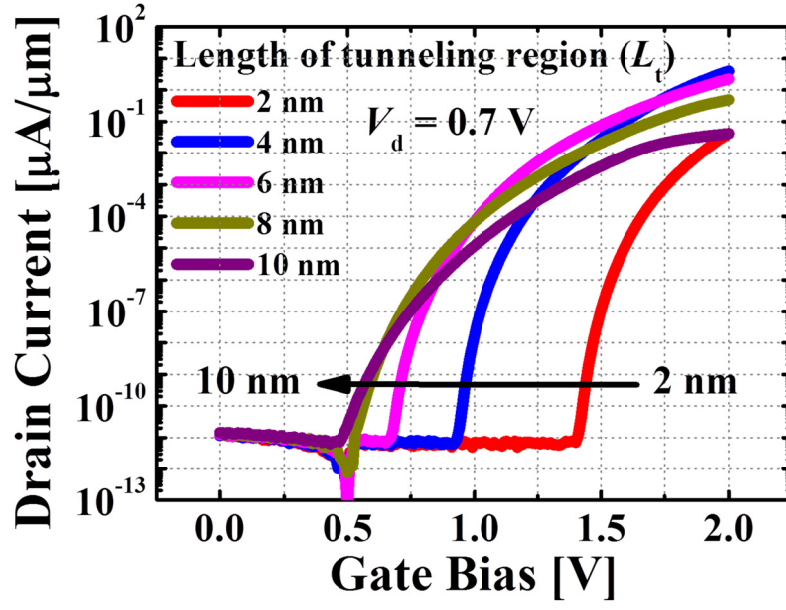
Quantitative analysis has been performed for more detailed discussion by using simple capacitance model. The tunneling region and the gate dielectric can be modeled as two capacitors in series as shown in Fig. 2.6 (a). Equation 2.1 shows the surface potential of the channel (ϕ_s), where C_{ox} means density of gate oxide capacitance ($\epsilon_{\text{ox}}/T_{\text{ox}}$) and C_d denotes density of depletion capacitance (ϵ_{Si}/W_d). If L_t is small, the whole tunneling region is fully depleted and the depletion region in the source is ignorable because the maximum W_d (W_{dm}) of 10^{20} cm^{-3} doped p-type Si is ~ 1 nm. In this case, the W_d is assumed to be the same as L_t which is independent on V_g and ϕ_s can be expressed as a function of L_t as Eq. 2.2. Furthermore, \mathcal{E} across the Si tunneling region has an almost constant value calculated by using Eq. 2.3.

$$\phi_s = \frac{C_{ox}}{C_{ox} + C_d} (V_g - V_{fb}) = \frac{\frac{\epsilon_{ox}}{T_{ox}}}{\frac{\epsilon_{ox}}{T_{ox}} + \frac{\epsilon_{si}}{W_d}} (V_g - V_{fb}) \quad (2.1)$$

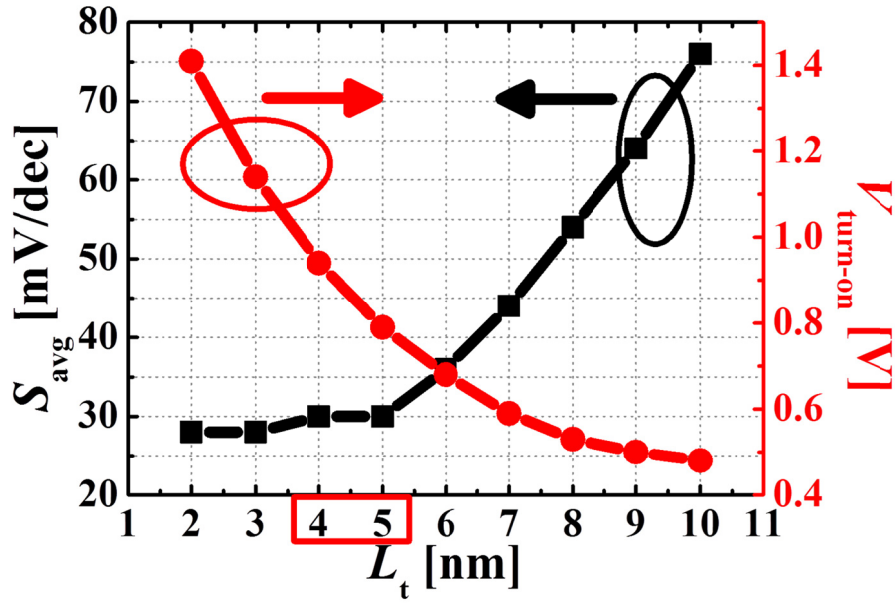
$$\phi_s = \frac{1}{1 + 3 \frac{T_{ox}}{L_t}} (V_g - V_{fb}) = \left(1 - \frac{3T_{ox}}{L_t + 3T_{ox}}\right) (V_g - V_{fb}), \text{ where } \epsilon_{si} \approx 3\epsilon_{ox} \quad (2.2)$$

$$\mathcal{E} = \frac{\phi_s}{L_t} = \left(\frac{1}{L_t + 3T_{ox}}\right) (V_g - V_{fb}) \quad (2.3)$$

Figure 2.6(b) shows the calculation results of ϕ_s and \mathcal{E} with the variation of L_t at $V_g - V_{fb} = 1$ V, where V_{fb} represents flat band voltage. It has been found that ϕ_s gradually increases due to the decrease of the capacitance in the Si tunneling region as L_t increases. Thus, $V_{turn-on}$ becomes smaller as shown in Fig. 2.6(b). On the other hand, \mathcal{E} across the tunneling region is inversely proportional to L_t . Because \mathcal{E} corresponds to the slope of energy band diagram, weak \mathcal{E} at large L_t means less abrupt band bending, which leads to larger S_{avg} . The relationship between $V_{turn-on}$, S_{avg} and L_t in Fig. 2.5(a) can be explained by Fig. 2.6(b). Considering that low S_{avg} and $V_{turn-on}$ are suitable for low operating power (LOP) applications, there is a trade-off between S_{avg} and $V_{turn-on}$ with the variation of L_t . Finally, it is determined that the optimum L_t is 4 nm. If L_t is more than 4 nm, minimal S_{avg} cannot be achieved in spite of small $V_{turn-on}$. However, if L_t is less than 4 nm, $V_{turn-on}$ is high in spite of the same S_{avg} value. To sum up, when L_t is 4 nm, minimal S_{avg} value is achieved with reasonable $V_{turn-on}$ [21].

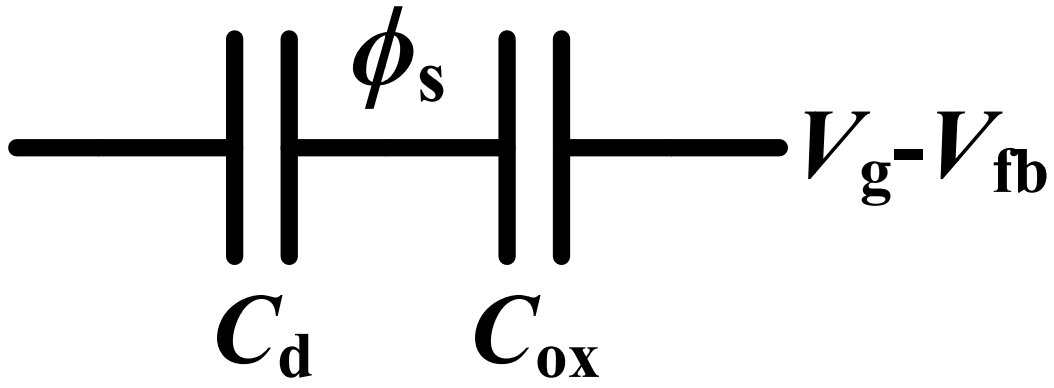


(a)

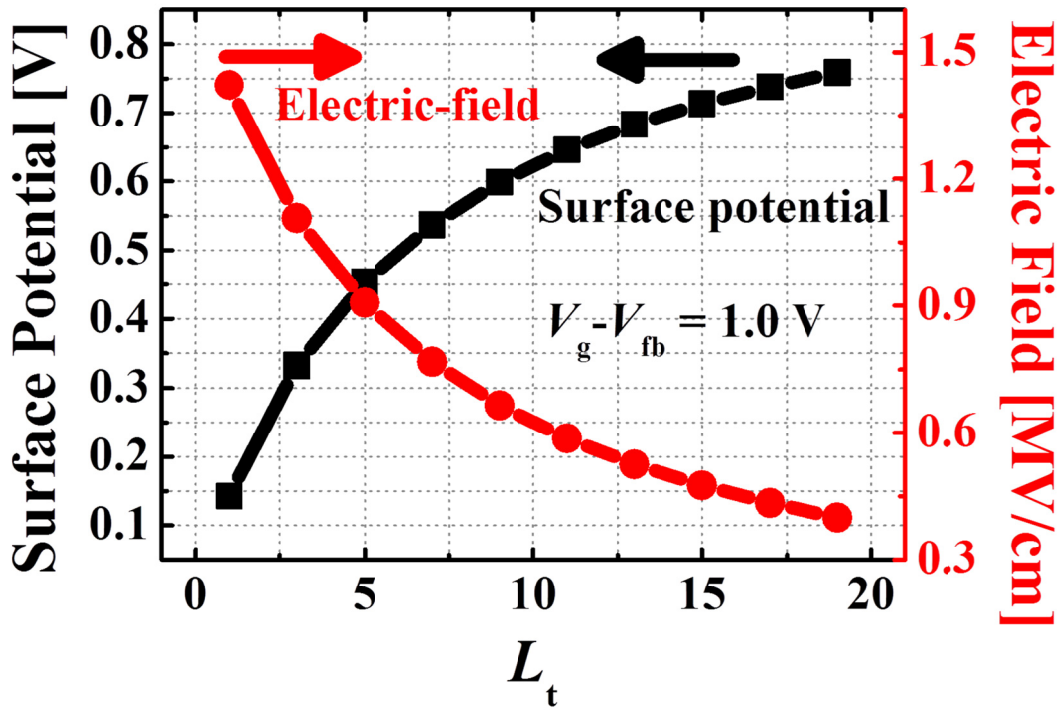


(b)

Fig. 2.5. (a) Transfer curves with the variation of L_t . (b) Extracted $V_{\text{turn-on}}$ and S_{avg} . Simulation tool: Silvaco AtlasTM.



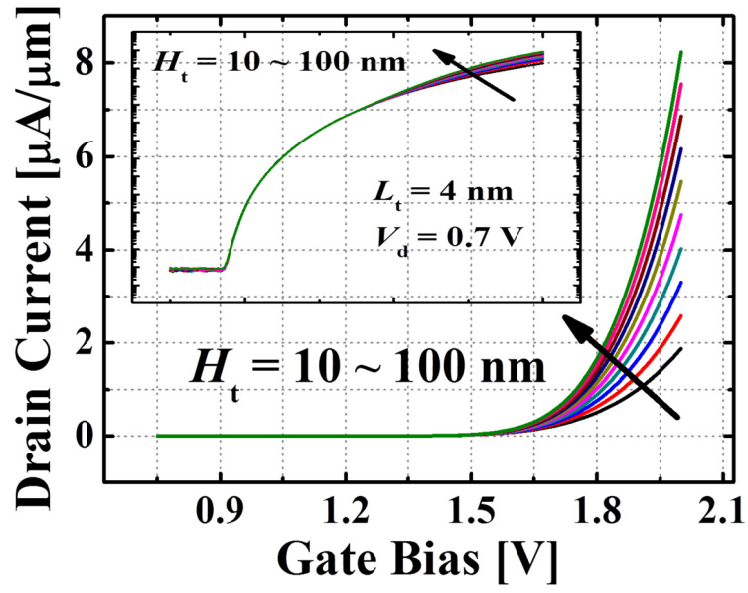
(a)



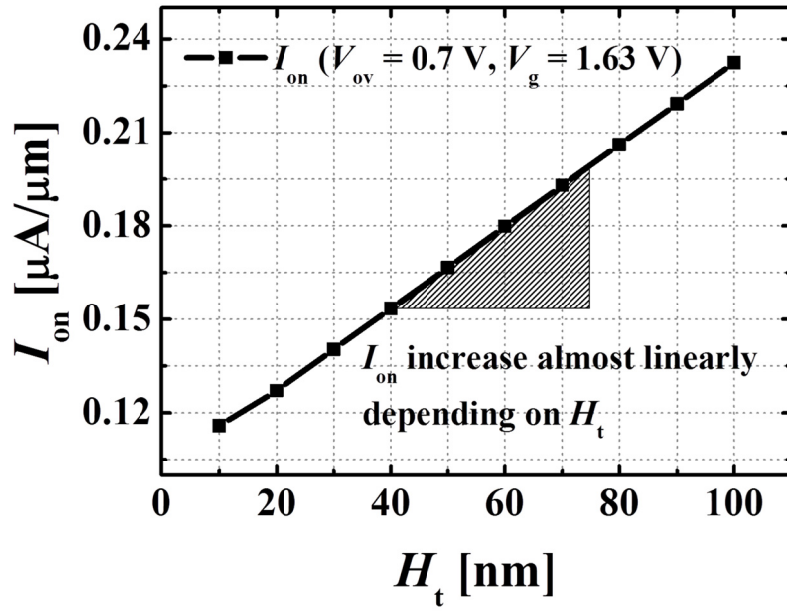
(b)

Fig. 2.6. (a) An equivalent capacitor model between the gate and the source. (b) Relationship between ϕ_s , \mathcal{E} and L_t at $V_g - V_{fb} = 1$ V. Simulation tool: Silvaco AtlasTM.

So far, L-shaped TFETs have been compared with conventional ones from the viewpoint of S_{avg} . From now on, the former will be compared with the latter in terms of I_{on} . As mentioned above, at the same V_{ov} , the L-shaped TFETs show higher I_{on} than conventional ones. In part, it is attributed to the low S_{avg} of L-shaped TFETs as explained in the previous paragraph. Another reason for I_{on} boosting is the large A_t of L-shaped TFETs. As shown in the inset of Fig. 2.1(a), conventional TFETs have A_t defined by the channel inversion layer thickness which is only a few nm. Because BTBT current flows across the small A_t , low I_{on} is inevitable. On the other hand, L-shaped TFETs have the tunneling direction perpendicular to the channel as shown in the inset of Fig. 2.1(b). Thus, as H_t increases, A_t increases, which leads to higher I_{on} . Figure 2.7(a) shows the simulated transfer characteristics of L-shaped TFETs as a function of H_t ranging from 10 to 100 nm. L_t is fixed at 4 nm and I_{on} is extracted when the V_{ov} is 0.7 V at the same drain bias (V_d). In spite of H_t variation, $V_{\text{turn-on}}$ is fixed at ~ 0.93 V as shown in the inset of Fig. 2.7(a). Figure 2.7(b) shows the relationship between I_{on} and H_t . It has been observed that I_{on} is linearly dependent on H_t . As H_t increases from 10 to 100 nm, I_{on} increases from 0.12 to 0.23 $\mu\text{A}/\mu\text{m}$. It should be noted that I_{on} is ~ 0.11 $\mu\text{A}/\mu\text{m}$ even if H_t is zero. It is due to the corner effect of the source region. The details about corner effect will be mentioned in Section 2.3. To sum up, L-shaped TFETs can boost I_{on} by increasing H_t without area penalty [21].



(a)



(b)

Fig. 2.7. (a) Transfer curves with the variation of H_t . The inset shows the relationship between $V_{\text{turn-on}}$ and H_t . (b) I_{on} as a function of H_t . Simulation tool: Silvaco AtlasTM.

Figure 2.8 shows the simulated transfer characteristic of an L-shaped TFET compared with that of a conventional TFET. For both kinds of TFETs, the detailed simulation parameters are the same as summarized in Table 2.1. Especially, in the case of L-shaped TFET, L_t and H_t of the tunneling region are 4 and 40 nm according to the previous results. As expected and demonstrated in Fig. 2.8, L-shaped TFETs have two main advantages over conventional ones. First, L-shaped TFETs show more abrupt on/off transition, which means that the S_{avg} is smaller than that of conventional TFETs. Second, at the same V_{ov} , L-shaped TFETs show 1000 times higher I_{on} than conventional TFETs thanks to the low S_{avg} and large A_t .

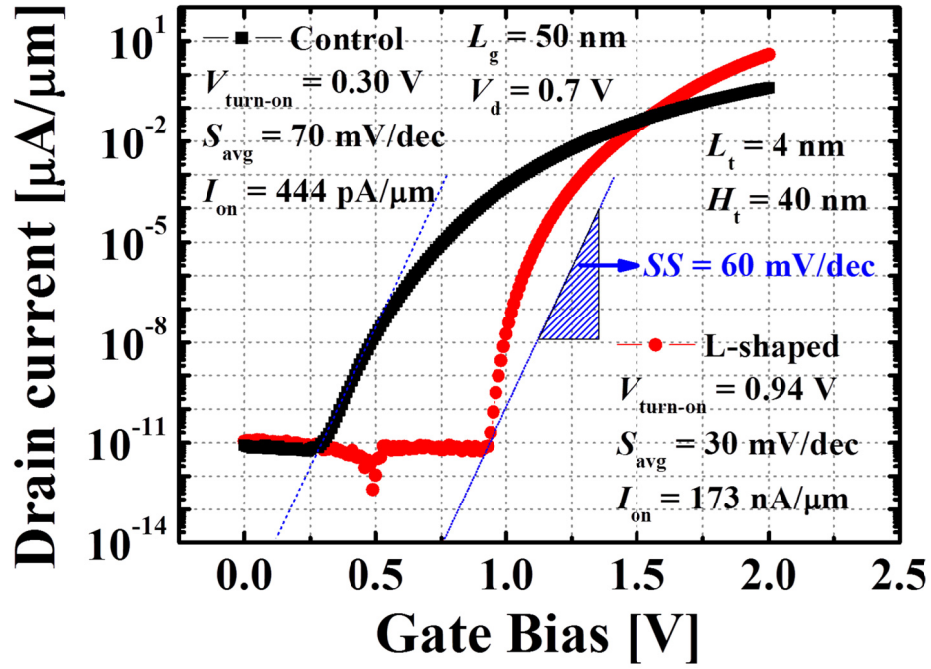
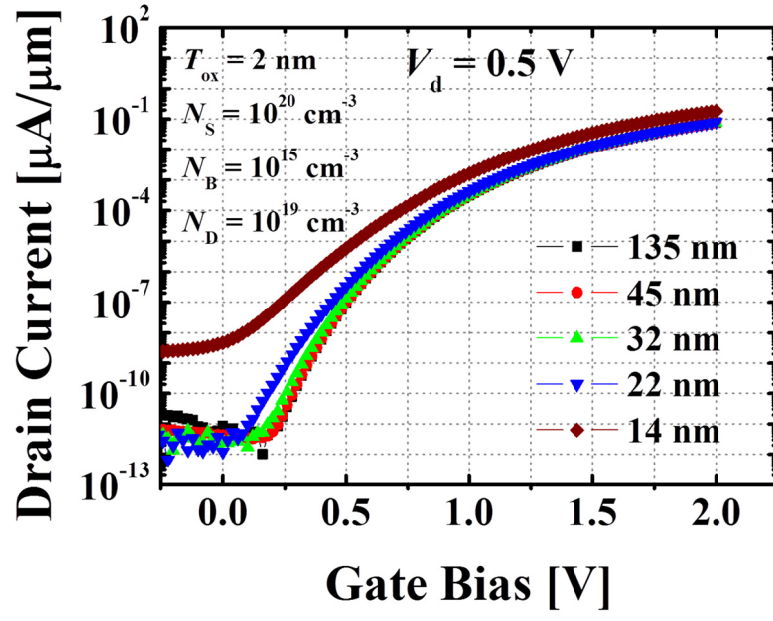


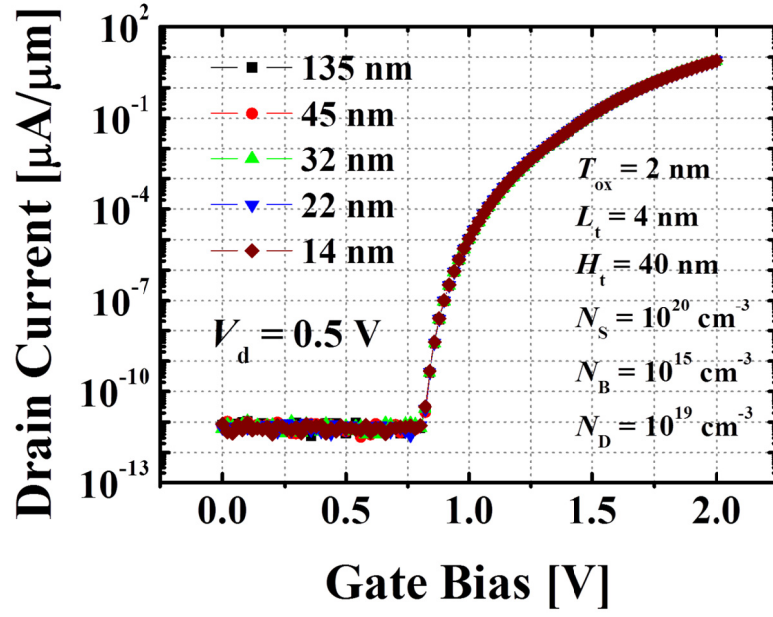
Fig. 2.8. Transfer curves of conventional and L-shaped TFETs. Simulation tool: Silvaco AtlasTM.

Lastly, the L-shaped TFETs' scale-down limit is compared with conventional TFETs. In the case of MOSFETs, reduction of L_g induces severe SCE such as drain-induced barrier lowering (DIBL) or punch through current that leads to a large increase of I_{off} and S . On the other hand, the characteristics of TFETs rarely change until L_g down to 22 nm, even though there exists a slight increase of I_{off} due to DICE or DIBT, as shown in Fig. 2.9(a). The results imply that TFETs are superior to MOSFETs in the aspect of L_g scaling. The reason of that is well established by previous studies of [34-39]. Because I_d of TFETs is dominated by tunneling resistance (R_{tun}) which is generally much larger than channel resistance (R_{ch}), change of L_g or channel mobility (μ) seldom effect on the I_{on} [38], [39].

However, the conventional planar TFETs show an obvious scaling limit of sub-22-nm L_g , due to the significant I_{off} increase. If the L_g reaches to ~ 10 nm, valence electrons at source could tunnel to the conduction band edge of drain directly because W_t is thin enough, i.e. almost the same as L_g . On the other hand, as shown in Fig. 2.9(b), the L-shaped TFETs do not suffer from SCE since its vertical channel is little affected by the V_d . In addition, a large area of source compared to drain region results in electric field dispersion. Consequently, DIBT will be reduced drastically and L-shaped TFETs show high scalability beyond the 14-nm technology node.



(a)



(b)

Fig. 2.9. Transfer curves with the variation of L_g . (a) Planar and (b) L-shaped TFETs. Simulation tool: Silvaco AtlasTM.

2.3 Corner Effect

As shown in the previous section, L-shaped TFETs show better performance than conventional TFETs in terms of I_{on} and S_{avg} . However, the previous work performed by Silvaco AtlasTM had a limitation in that it calculates only perpendicular non-local tunneling current components in device structures. In this section, for more accurate modeling and determination of fabrication flow, L-shaped TFETs have been simulated by Synopsys SentaurusTM using dynamic non-local path band-to band model [30, p. 395]. The model determines tunneling paths dynamically based on the energy band profile and includes non-local tunneling current components in all directions. The simulated device structure is the same as in Fig. 2.8.

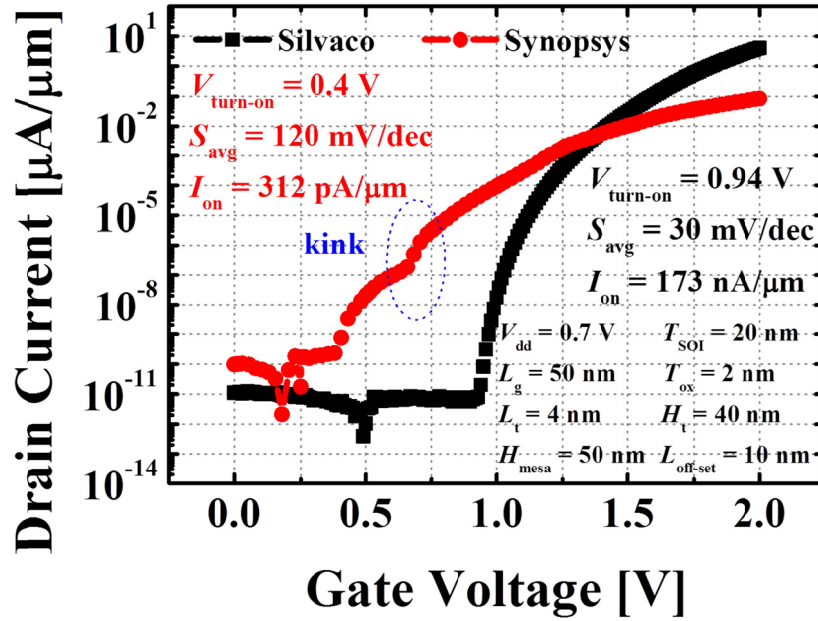


Fig. 2.10. Transfer curves simulated by Synopsys SentaurusTM and Silvaco AtlasTM. Due to a kink, S_{avg} and I_{on} properties are degraded.

The transfer curves illustrated in Fig. 2.10 show a kink when V_g is ~ 0.7 V. The kink should be suppressed to maximize the advantages of L-shaped TFETs: low S_{avg} and high I_{on} . In order to investigate the origin of the kink phenomenon, BTBT rates are examined by 2-D contour plots under various V_g 's. As shown in Fig. 2.11, BTBT occurs at source corner ahead of flat source region. In detail, tunneling phenomena start at the source corner at V_g of ~ 0.5 V which corresponds to $V_{turn-on}$ shown in Fig. 2.10. It is contrary to our expectation that tunneling occurs uniformly all over the Si tunneling region for high current drivability and low S_{avg} .

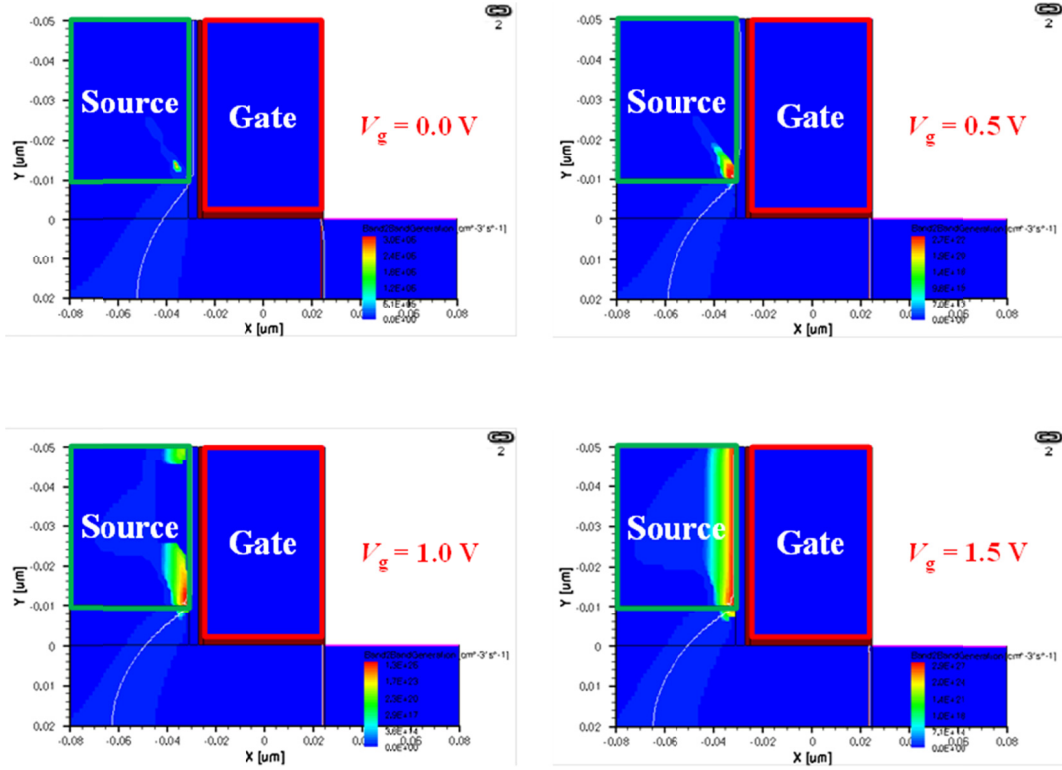
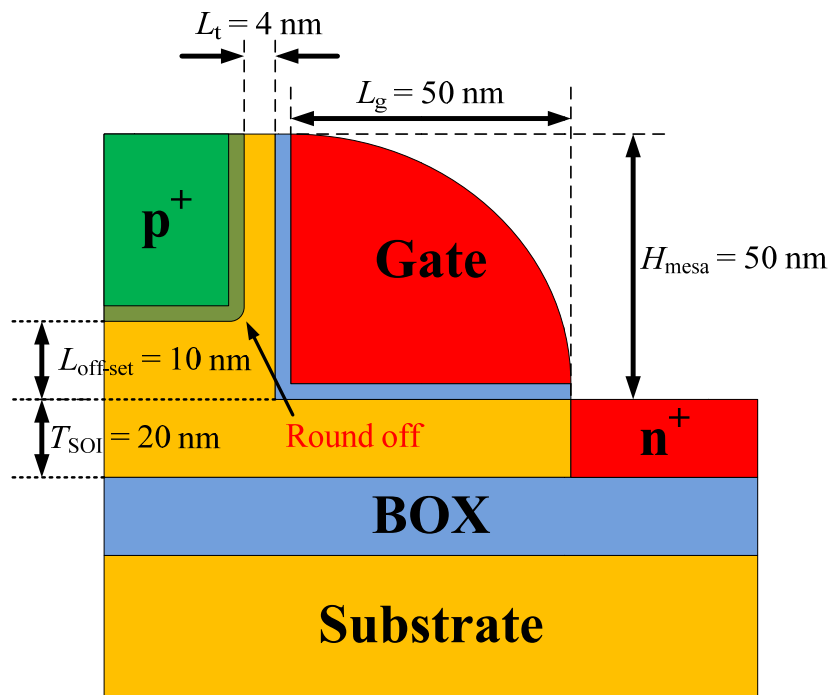


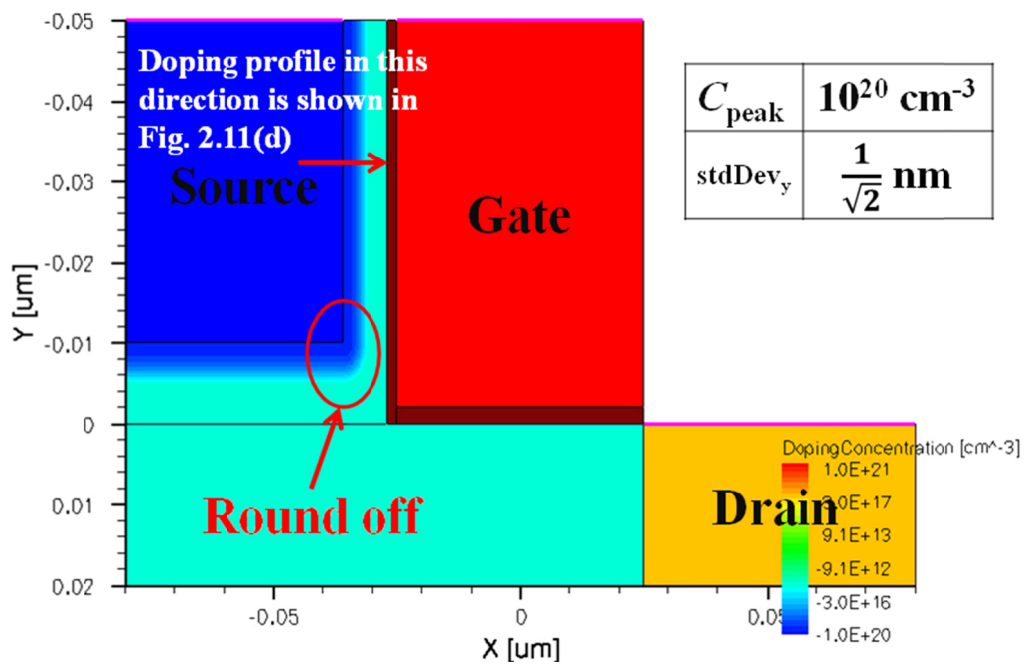
Fig. 2.11. 2-D contour plots of BTBT rates with various V_g 's. Simulation tool: Synopsys SentaurusTM.

It has been inferred that the kink is induced by electric field crowding around the sharp source corner edge [22], [40]. In order to confirm this assumption, the source corner is rounded off as shown in Fig. 2.12. The radius of the rounded region is ~ 4 nm. In order to investigate the effect of rounded corner, Gaussian doping profile is used at the junction between p^+ -source and tunneling region with peak concentration (C_{peak}) of 10^{20} cm^{-3} and standard deviation (stdDev_y) of ~ 0.71 nm, respectively. The other simulated parameters are fixed at the same values as control samples for fair comparison. From the simulation result, it is observed that the fully depleted rounded corner with gradual doping profile (Fig. 2.12(c)) is helpful to suppress kinks (Fig. 2.13). As a result, S_{avg} is reduced down to 85 mV/dec and I_{on} is doubled compared with that in Fig. 2.8.

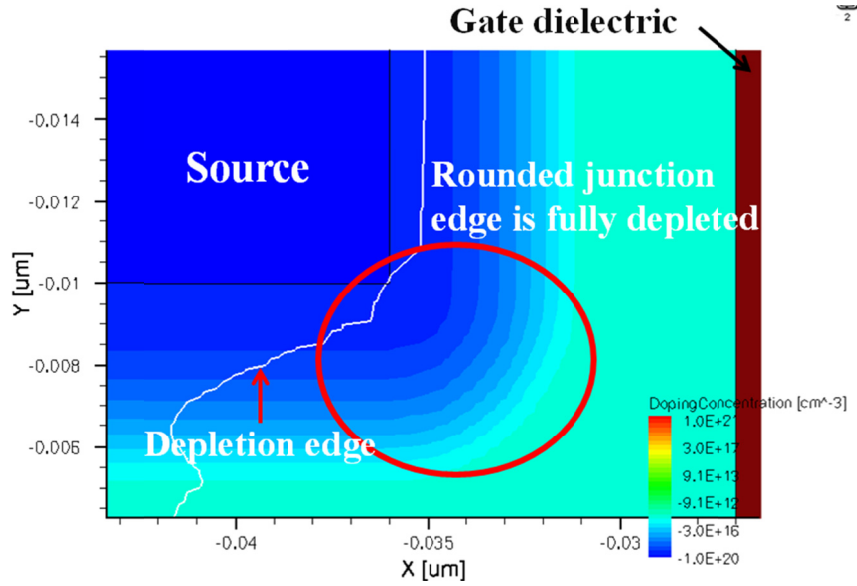
The results show that the kink phenomenon comes from the electric field crowding which can be alleviated by rounding off sharp source corner edges. However, S_{avg} is still larger than 60 mV/dec. According to previous work, abrupt doping profile is necessary for narrow W_t which determines the S_{avg} characteristics of TFETs. In other words, in terms of doping profile, there is trade-off between the kink phenomenon and the S .



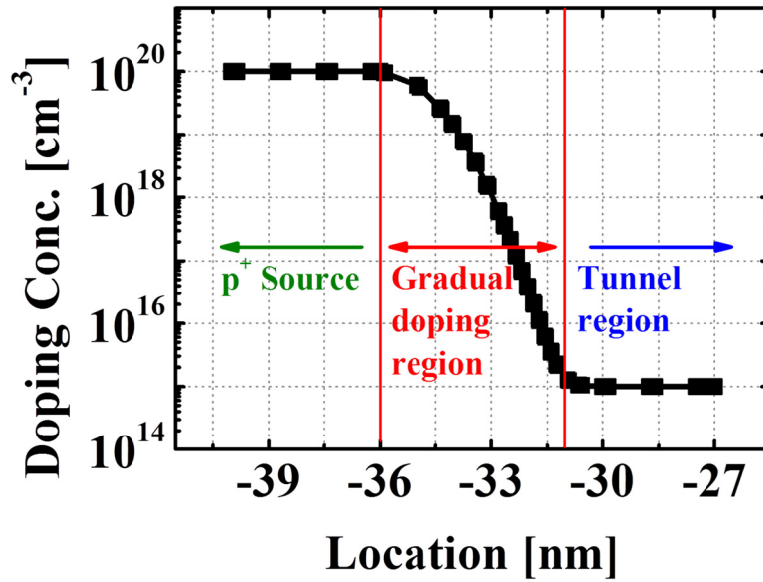
(a)



(b)



(c)



(d)

Fig. 2.12. (a) Schematic diagram of an L-shaped TFET with rounded source corner and several device parameters. (b) 2-D contour plot of dopant concentration based on device simulation. (c) 2-D contour plot of doping concentration and depletion region. (d) Extracted doping profile at source and channel junction indicated in Fig. 2.12(b). Simulation tool: Synopsys SentaurusTM.

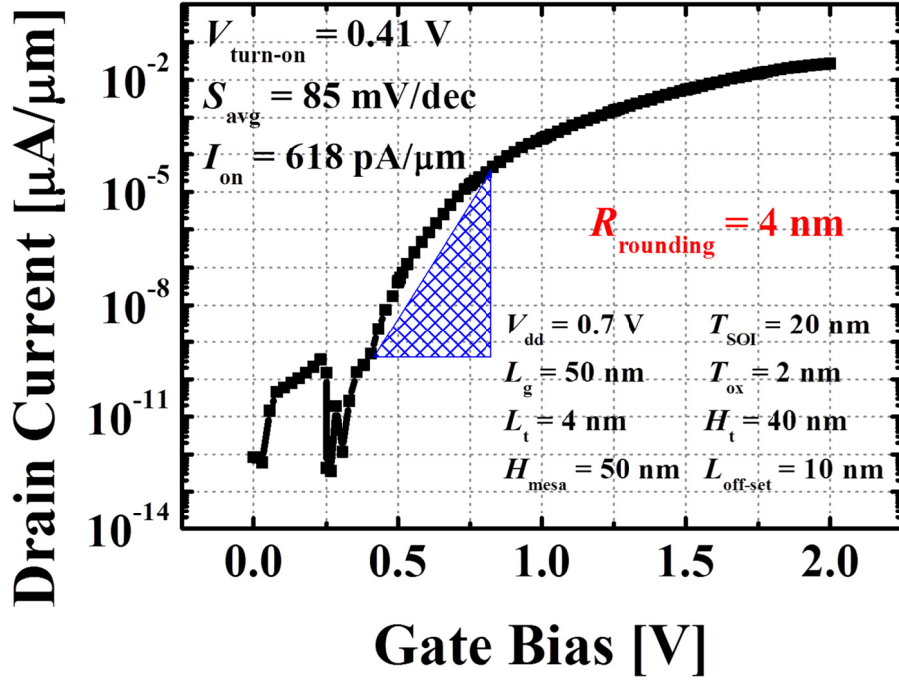


Fig. 2.13. Transfer curves with the structure shown in Fig. 2.12(b). Simulation tool: Synopsys SentaurusTM.

In order to suppress kinks and improve S_{avg} characteristics, a novel fabrication flow has been proposed. The main idea is that dopant diffusion in lateral direction is suppressed to make W_{t} narrow, whereas gradual doping profile is preferred in vertical direction for the reduction of kink effects. Figure 2.14 summarizes key process steps to achieve abovementioned goals. For the reduction of bulk leakage current, a SOI wafer is used as a substrate (a). First, a Si epitaxial layer is grown on the SOI wafer to form uniformly doped source region (b). The dopants can be easily injected during the epitaxial growth step by in-situ doping technique. Then, mesa-shaped source regions are

patterned by anisotropic Si etch with hard mask of plasma-enhanced chemical vapor deposition (PECVD) oxide (c, d). In order to prevent stress induced by lattice mismatch between the Si and silicon-nitride (Si_3N_4), buffer layer is deposited by high-density plasma CVD (HDPCVD) oxide (e). The Si_3N_4 sidewall spacer is formed by etch-back process followed by deposition using low-pressure CVD (LPCVD) with dichlorosilane (DCS, SiH_2Cl_2) and ammonia (NH_3) gas. The sidewall spacer is used as a masking layer from ion implantation to form drain regions (f), and as a stopper of chemical-mechanical polishing (CMP) after oxide deposition with HDPCVD (g). For the convenient progress of following steps, the polished thickness should be sufficient to expose a Si_3N_4 layer. Then, the Si_3N_4 sidewall spacer and SiO_2 buffer layer are stripped step by step with phosphoric acid (H_3PO_4) and diluted hydrofluoric acid (DHF), respectively (h, i). The L-shaped intrinsic Si layer is deposited by selective epitaxial growth (SEG) at $\sim 670^\circ\text{C}$ to suppress lateral diffusion of dopants in the source region (j). After SEG, gate dielectric and gate regions are formed by well-established replacement gate technology of high- κ /metal gate stack (k, l). Back-end process is the same as that of the conventional CMOS process.

In order to confirm the feasibility of the proposed fabrication steps, process simulation has been carried out. Because source-first and low-temperature SEG process are adopted, dopants are rarely diffused in lateral direction and abrupt junction profile is maintained between the source and the tunneling region as presented in Fig. 2.15(a). On the other hand, the diffusion of dopants in vertical direction is not negligible due to

thermal process steps including LPCVD step. The abrupt junction profile in lateral direction leads to narrower W_t and lower S_{avg} , whereas gradual doping profile in vertical direction results in the decrease of kink phenomenon. As a result, the contradictory issue between the elimination of kink and the narrow W_t can be addressed simultaneously. Figure 2.15(b) shows that S_{avg} characteristic is further improved with the value of 45 mV/dec in accompany with the reduction of kink.

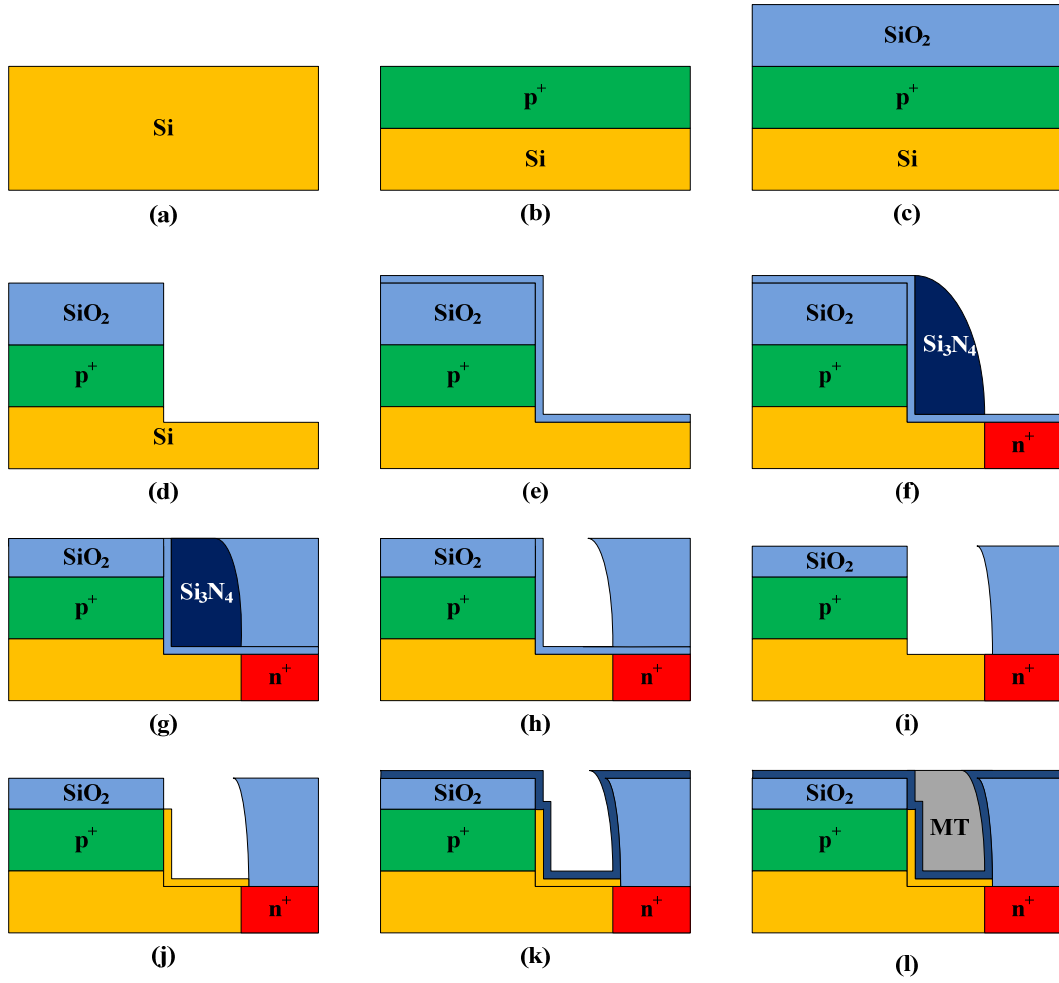
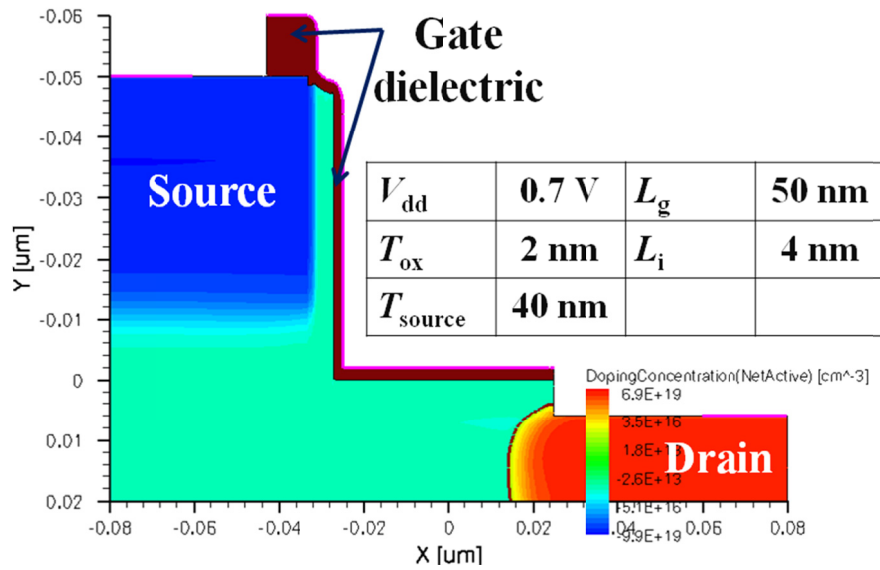
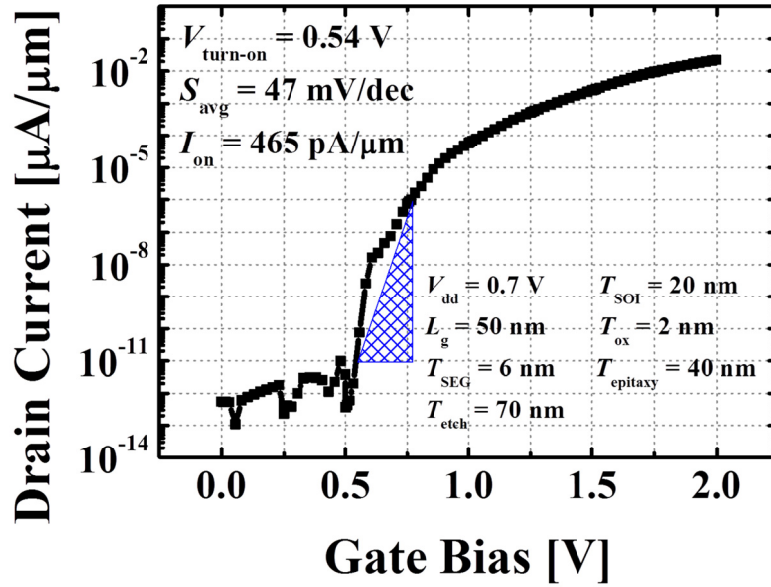


Fig. 2.14. Key fabrication steps.



(a)



(b)

Fig. 2.15. (a) Device structure obtained by process simulation. The critical process conditions are listed in the inset. Shortly, the thickness of epitaxially grown Si for source (T_{source}) is 40 nm and the amounts of Si etch for mesa (T_{mesa}) is 70 nm. (b) Transfer curves simulated with the device in Fig. 2.15(a). Simulation tool: Synopsys SentaurusTM.

2.4 Further Improvement and Circuit Application

For further optimization of L-shaped TFETs and its complementary logic application, 2-nm hafnium dioxide (HfO_2) is used as gate dielectric rather than SiO_2 to improve gate controllability over the channel. In addition, in the case of p-channel L-shaped TFETs, p^+ -doped poly-Si is used as gate material for $V_{\text{turn-on}}$ adjustment.

Figure 2.17 shows the transfer and output curves of optimized n- and p-channel L-shaped TFETs. For both types of TFETs, L_t is set to be 4 nm following the simulation results and H_t is set by 40 nm to alleviate convergence issues in device simulation. They show better performance than those with SiO_2 gate dielectric, in terms of $V_{\text{turn-on}}$, S_{avg} and I_{on} as shown in Fig. 2.17(a). One noteworthy thing is that n- and p-channel TFETs have almost the same I_{on} unlike MOSFETs. It is described well in Fig. 2.17(b). Output curves are symmetric with respect to the origin although electrons have different mobility values than holes. It is because I_{on} is determined by BTBT rather than carrier drift in the case of TFETs. The other interesting point is small channel conductance (g_d) when V_d is small. This is due to large tunneling resistance R_{tun} and it is a common phenomenon of TFETs. The saturation characteristics of L-shaped TFETs along with high I_{on} promise their low-power applications with high operation speed.

Finally, in order to evaluate operation speed, an inverter has been designed by adopting the optimized n- and p-channel TFETs. Figure 2.16 shows simulation conditions. The load capacitance (C_L) is set to be 6 fF referring 0.13 μm technology nodes and it is not much different from simulated device. The mixed-mode simulation

of Silvaco AtlasTM is used for transient simulation. Figure 2.18 presents the effect of high- κ gate dielectric on its operation speed. As dielectric constant increases from 10 to 25, delay time decreases from 29.1 ns to 356 ps. In the case of L-shaped TFET inverters with the SiO₂ gate dielectric, $V_{\text{turn-on}}$ is too high and I_{on} is too small to show static inverter operation and it is not shown in here. On the other hand, using the high- κ gate dielectric, it shows high operation speed up to GHz which is ~ 1000 times faster than conventional ones even though V_d is scaled to 0.5 V. The voltage overshoot comes from Miller capacitance which entirely depends on gate-to-drain capacitance [17], [41-43].

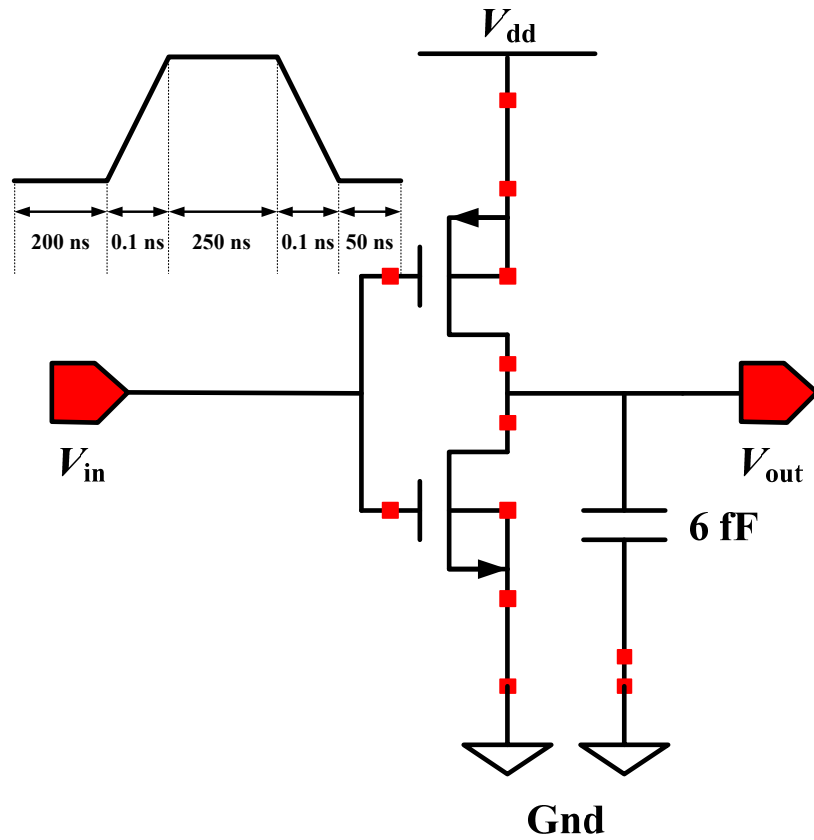
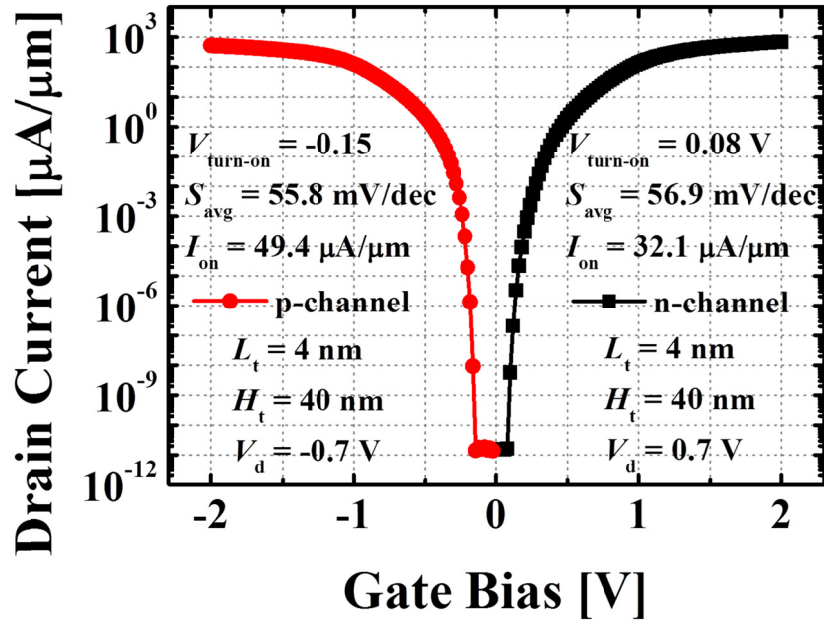
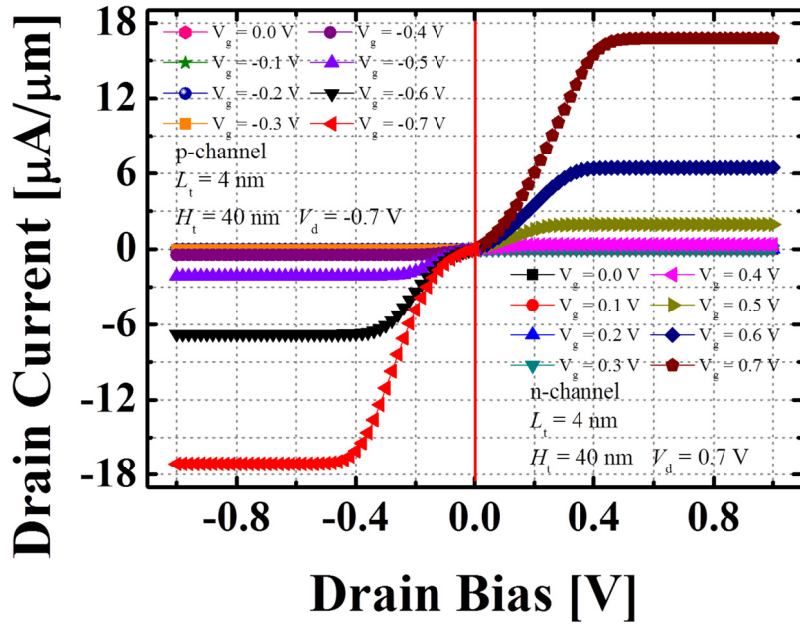


Fig. 2.16. Schematic of an inverter and its input pulse.

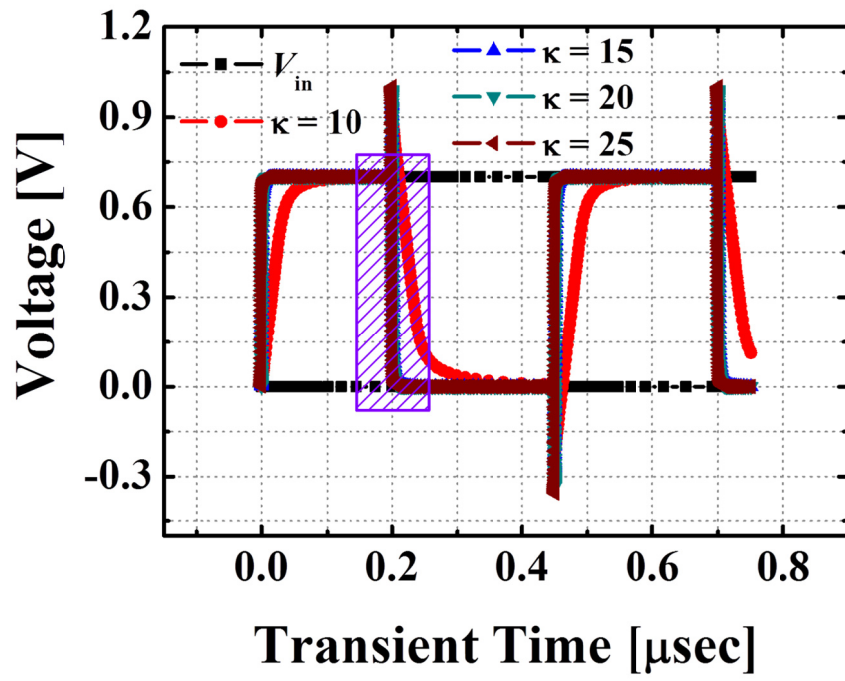


(a)

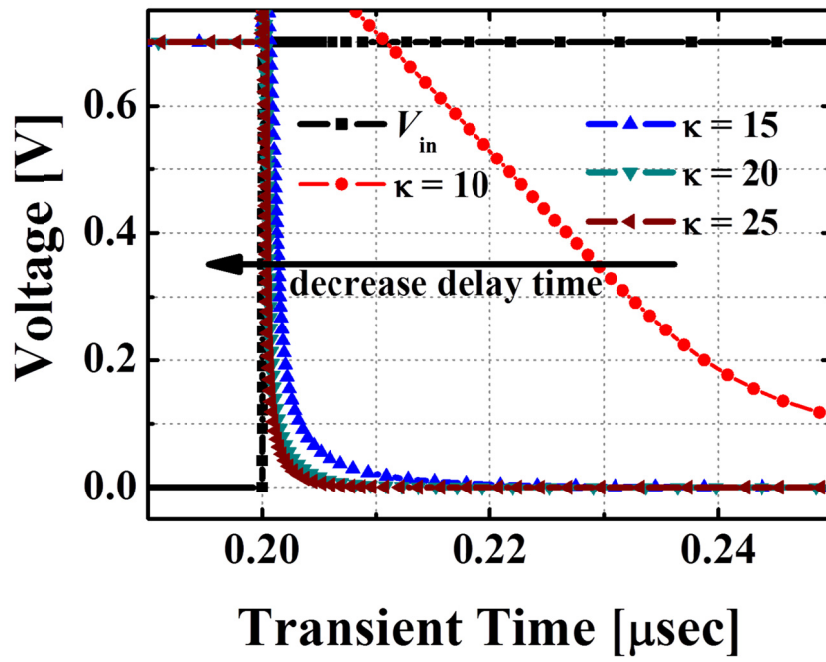


(b)

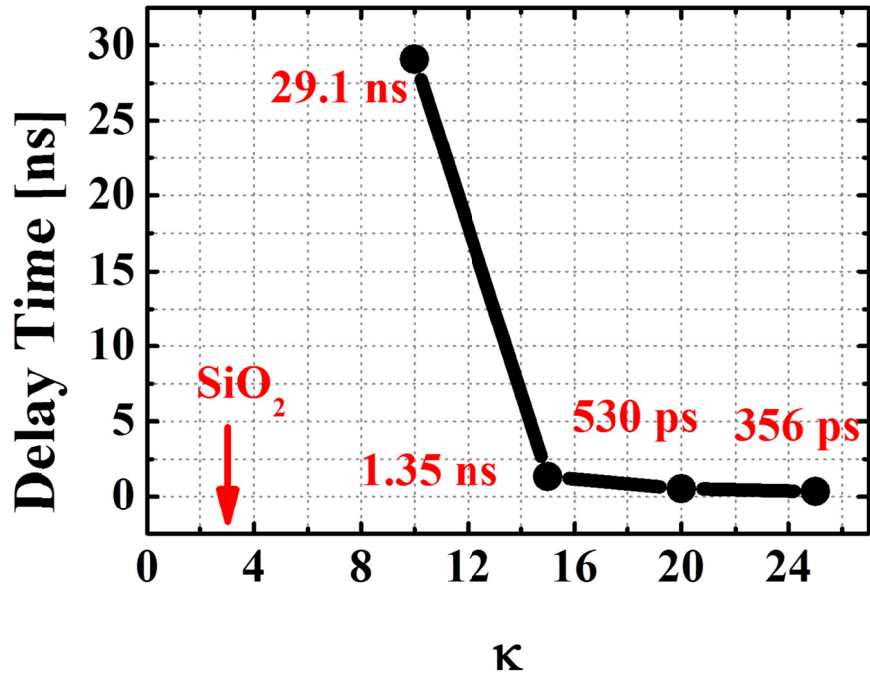
Fig. 2.17. (a) Transfer and (b) output curves of n- and p-channel L-shaped TFETs. Simulation tool: Silvaco AtlasTM.



(a)



(b)



(c)

Fig. 2.18. Transient simulation results of L-shaped TFETs inverters with various gate dielectric. (a) Transient simulation results, (b) an enlarged image of indicated region in (a), and (c) extracted delay time. Simulation tool: Silvaco AtlasTM.

2.5 Summary of Target Device

Based on the simulation results, the target device parameters are determined as follows. First, an adaptation of sub-3-nm gate dielectric is inevitable to increase gate controllability with high electric field from gate capacitor. Unfortunately, there doesn't exist well established sub-3-nm gate dielectric technique with a reasonable gate leakage current yet, in Inter-university of Semiconductor Research Center (ISRC) of Seoul

National University (SNU). Therefore, high- κ /metal gate stack process should be set up and introduced in the process.

For abrupt doping profile between the source and the tunneling region, the intrinsic layer beside the source is grown by low temperature SEG process. In addition, thermal process with high temperature is performed prior to the SEG step. For example, an annealing process for activating the dopants in drain is performed before the SEG. The use of high- κ /metal gate stack rather than SiO_2 /poly-Si also has the advantage of low thermal budget.

According to the simulation results regarding thermal diffusion, the optimum L_t is set by ~ 6 nm and H_t is determined by 50 nm. Considering the measurable base current limit is usually dozens of fA, active width more than 80 μm is included in the layout. For the simple process flow, self-aligned process is excluded and the minimum L_g is 0.5 μm . Because the L-shaped TFETs are rarely affected by L_g , it is sufficient to verify the ideas.

Chapter 3

Device Fabrication

3.1 Fabrication of Control TFETs

In order to prepare control samples, planar TFETs have been fabricated following the process sequence as shown in Fig. 3.1. First, active region is defined on 30-nm SOI substrate using i-line photolithography followed by reactive ion etch (RIE). The gate stack consists of 30-Å thermal SiO₂ with dry oxidation process and 2500 Å poly-Si with LPCVD process by the use of silane (SiH₄) gas. In order to make highly doped n⁺-poly-Si gate, arsenic (As) ions are injected by ion-implantation process while dose and energy are set by $3 \times 10^{15} \text{ cm}^{-2}$ and 70 keV. And then, gate is patterned by anisotropic RIE process followed by photolithography with L_g from 0.5 μm to 7 μm. Since there exists just a 30-Å gate dielectric for etch-stop layer, the RIE process should be performed very carefully. Fig. 3.2 shows microtrenching effects that are usually caused

by specular reflection of high energy ions due to angles of mask and trench [44]. As a result, there exist up to 38-nm differences of etch thickness between the nearby gate region and the source/drain side. Regarding the SOI substrate is much thinner than gate thickness and it is ~30 nm, a slight over-etch and microtrenching effects influence on substrate thickness and, in the worst case, the active region can be disappeared. The problem is solved by two-tiered RIE process with different recipe and the latter is adjusted for high selectivity with moderated etch rate. After gate patterning, source/drain implantation is performed by the use of PSD and NSD mask, respectively. In order to suppress dopant diffusion, rapid thermal annealing (RTA) process of 850 °C, 30sec is used for dopant activation. Finally, inter-layer dielectric (ILD) is formed by tetra-ethyl-ortho-silicate (TEOS) oxide with PECVD process and metal layers are deposited by physical vapor deposition (PVD) process using Ti/TiN/Al/TiN stacks.

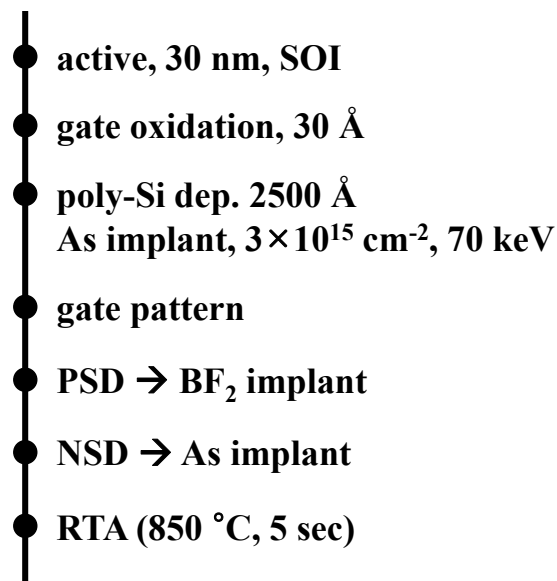


Fig. 3.1. Device fabrication flow for conventional planar TFETs.

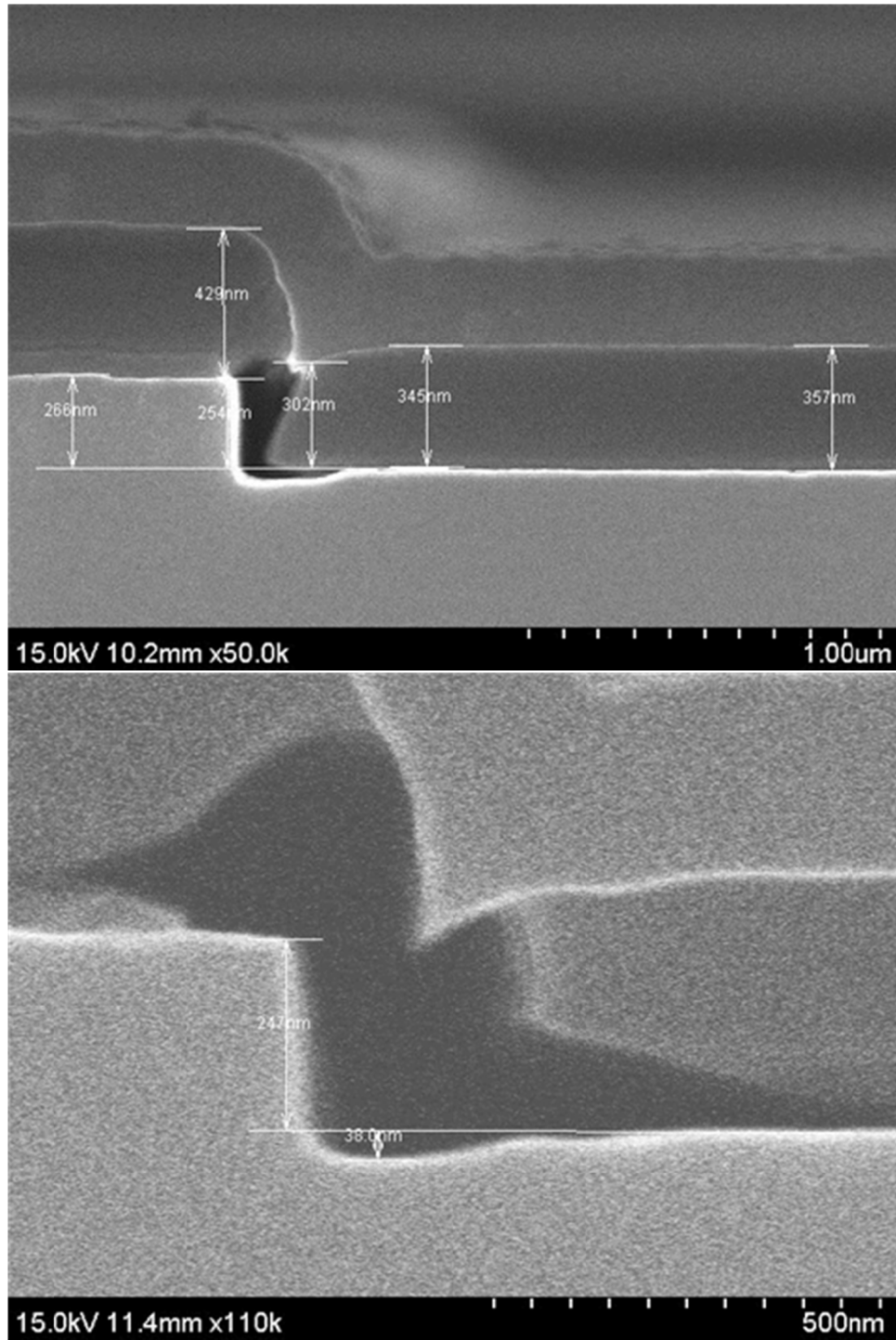


Fig. 3.2. Microtrenching effect.

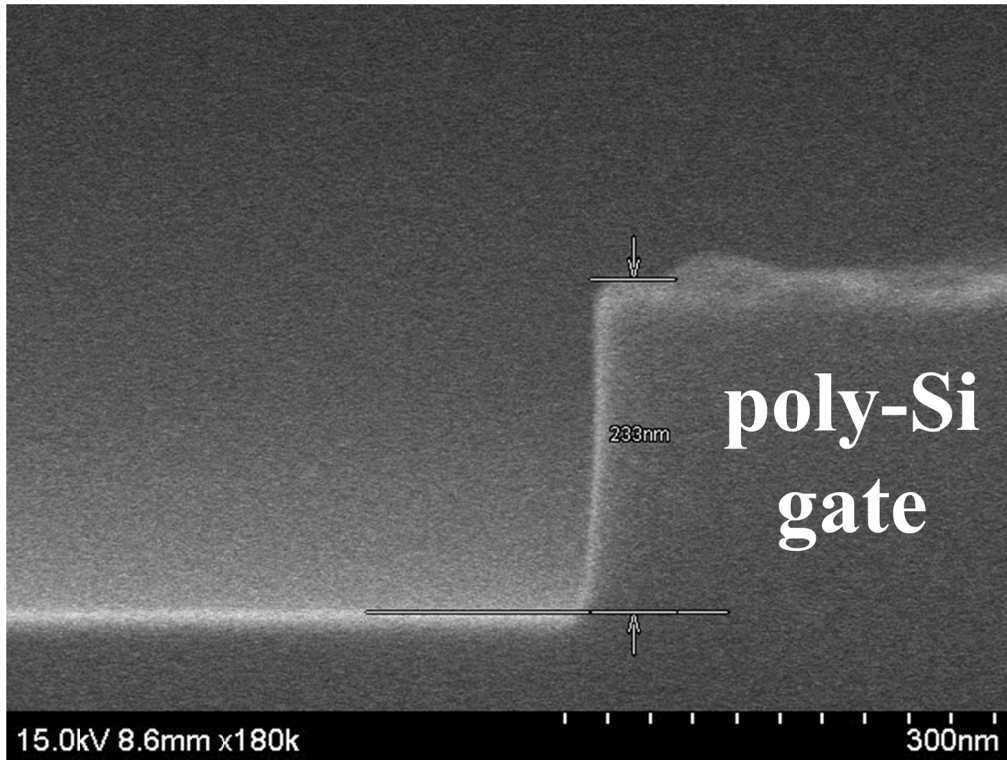


Fig. 3.3. Gate patterning with two-tiered RIE process.

3.2 Key Process Designs for L-shaped TFETs

In order to verify the idea of L-shaped TFET, the self-aligned process flow presented in Fig. 2.14 is slightly modified as shown in Fig. 3.4. After p^+ -doped source formation, it is patterned for mesa-shape by RIE processes (a, b). Next, as shown in Fig. 3.4(c), ion implantation process is performed to form n^+ -doped drain while the other regions are masked by photo resist (PR) rather than sidewall spacer hard mask, as depicted in Fig. 2.14(f). After SEG process, high- κ /metal gate stack is deposited directly on the substrate instead of damascene gate process of Fig. 2.14(g-l).

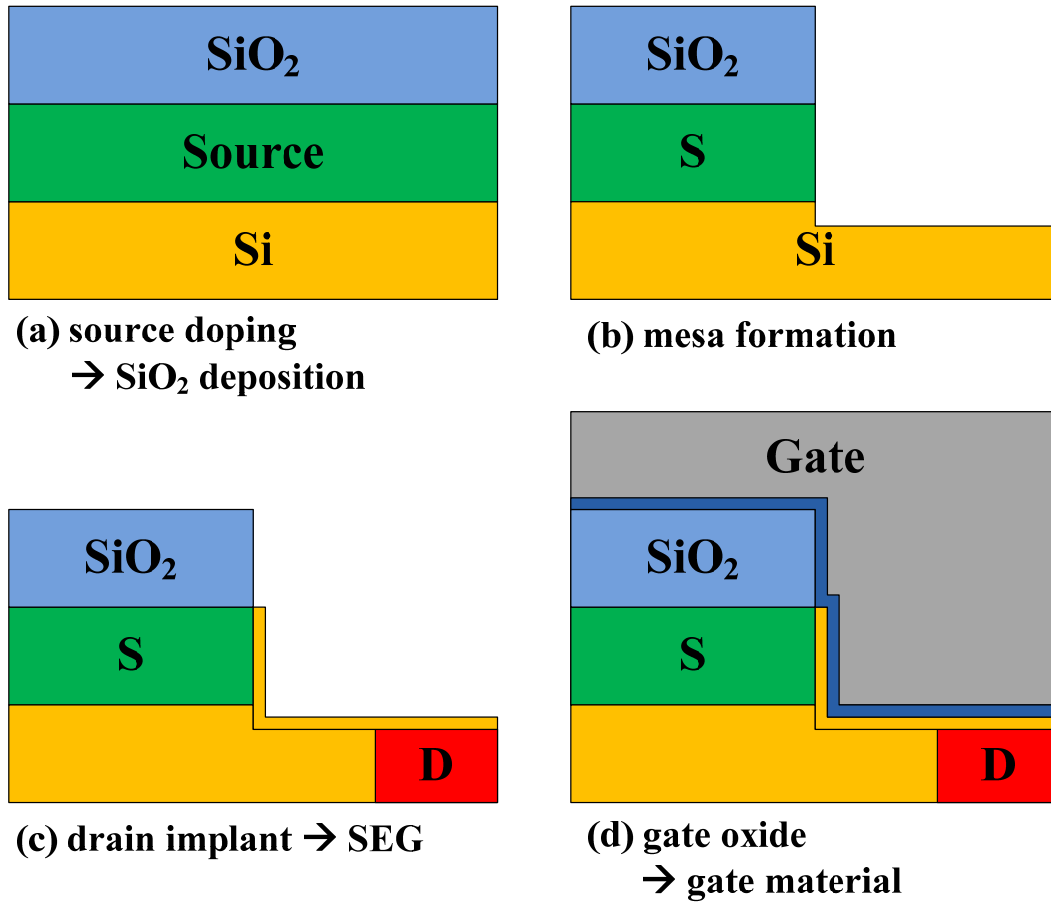


Fig. 3.4. Modified fabrication flow.

Figure 3.5 shows transmission electron microscope (TEM) images just after SEG process. In this experiment, source is doped by BF₂ ion implantation with the amount of 10^{15} cm^{-2} doses and 30 keV accelerating energy. After that, RTA process is performed at 1000 °C, 10sec to activate the dopants and moderate an implant damage. However, in spite of these efforts, there exist several dislocations and they result in non-uniform growth rates in SEG process, as shown in Fig. 3.5. Furthermore, from the other point of view, BTBT phenomena should occur simultaneously with the same amount over the

entire tunneling region for maximizing the merits of L-shaped TFETs with small I_{off} and S_{avg} . Therefore, it is necessary to make uniformly doped source region without any lattice mismatch. An in-situ doping technique during the epitaxial layer growth of Si is suitable for both perspectives. Figure 3.6(a) shows source region is well grown as a single crystalline Si layer without any dislocation problem. In addition, the dopants are injected uniformly and abruptly as depicted by secondary ion mass spectrometry (SIMS) profile of Fig. 3.6(b).

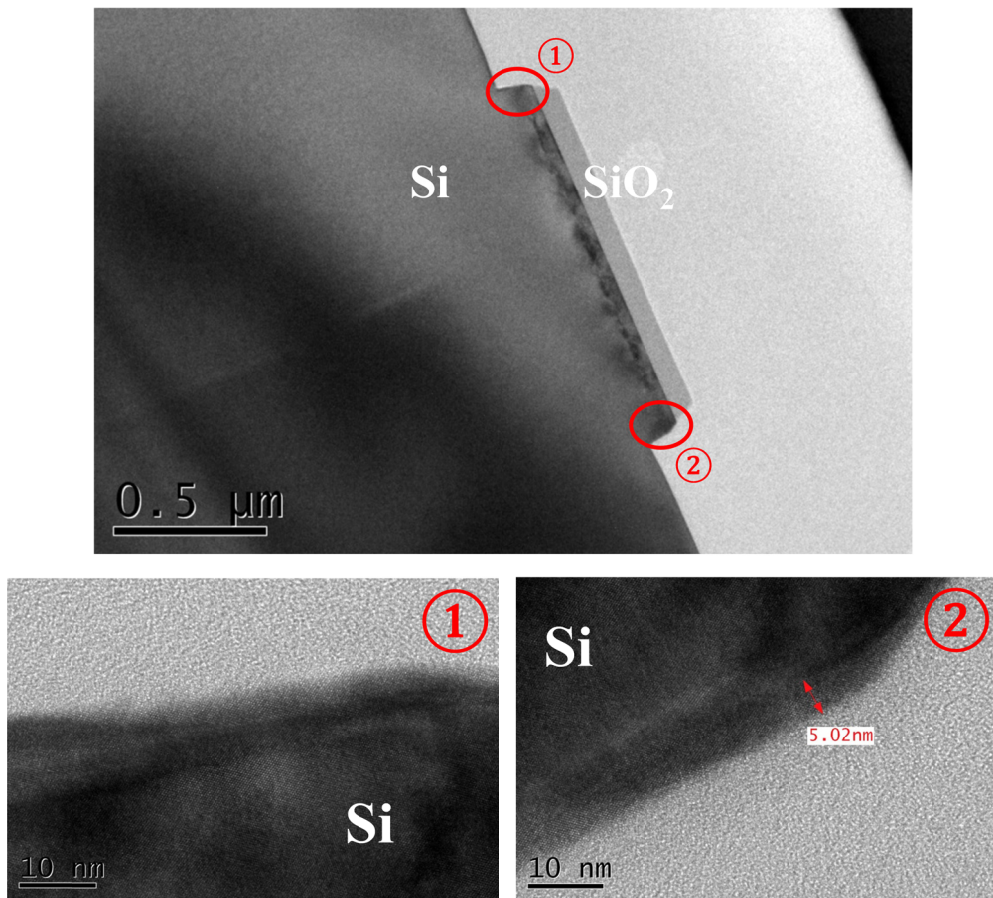
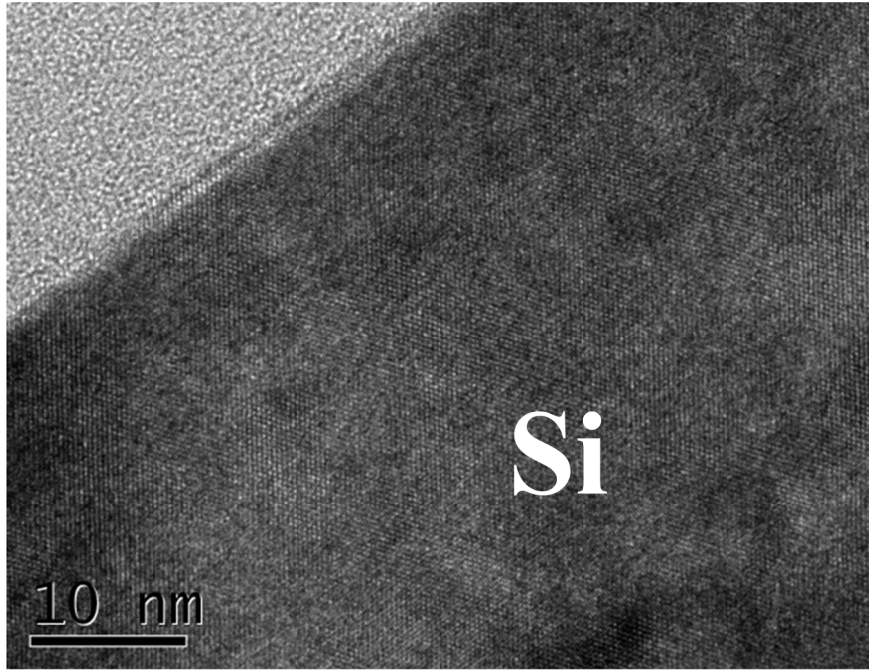
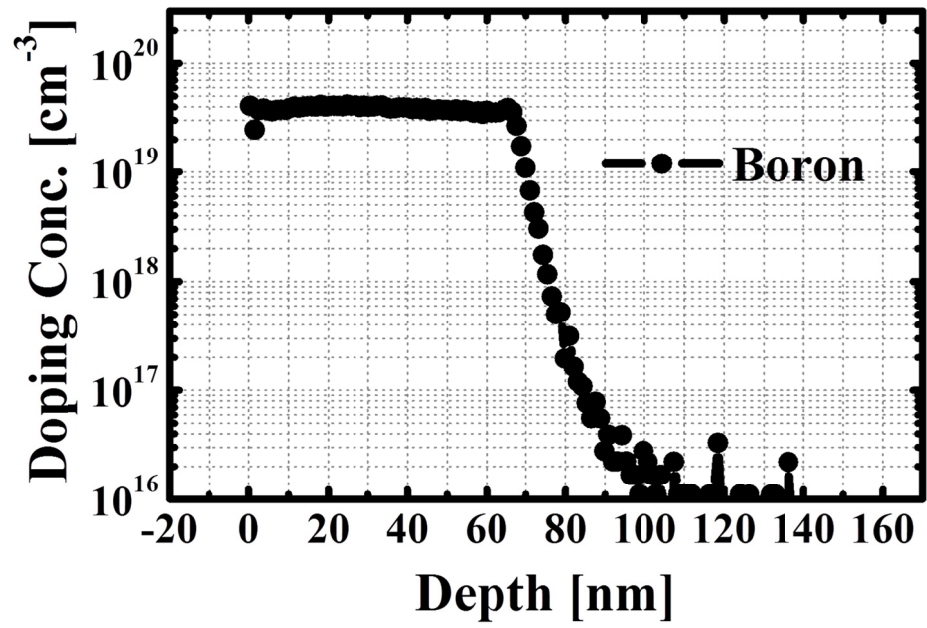


Fig. 3.5. TEM images about SEG process with source formed by ion implantaion.



(a)



(b)

Fig. 3.6. (a) TEM image and (b) SIMS profile of epitaxially grown source region.

The other key process for realization of high performance L-shaped TFET is SEG process for tunneling region because it determines tunnel junction energy band profile as well as maximum W_t . In order to form abrupt tunnel junction, dopant diffusion from p^+ -source should be under strict constraints. Accordingly, SEG process is performed at $\sim 670^\circ\text{C}$ with the help of AUK Corporation to suppress dopant diffusion, especially in lateral direction. Figure 3.7 shows SIMS profile of SEG region and source, where depth of 0 nm corresponds to the interface of SEG/atmosphere and 20 nm represents the boundary of source. The abruptness of doping profile is $\sim 10\text{ nm/dec}$. Figure 3.8 shows TEM images after SEG process at sidewall of mesa-patterned SOI substrate. It is certain that $\sim 10\text{ nm}$ of single crystalline Si is just grown on the Si substrate with high selectivity.

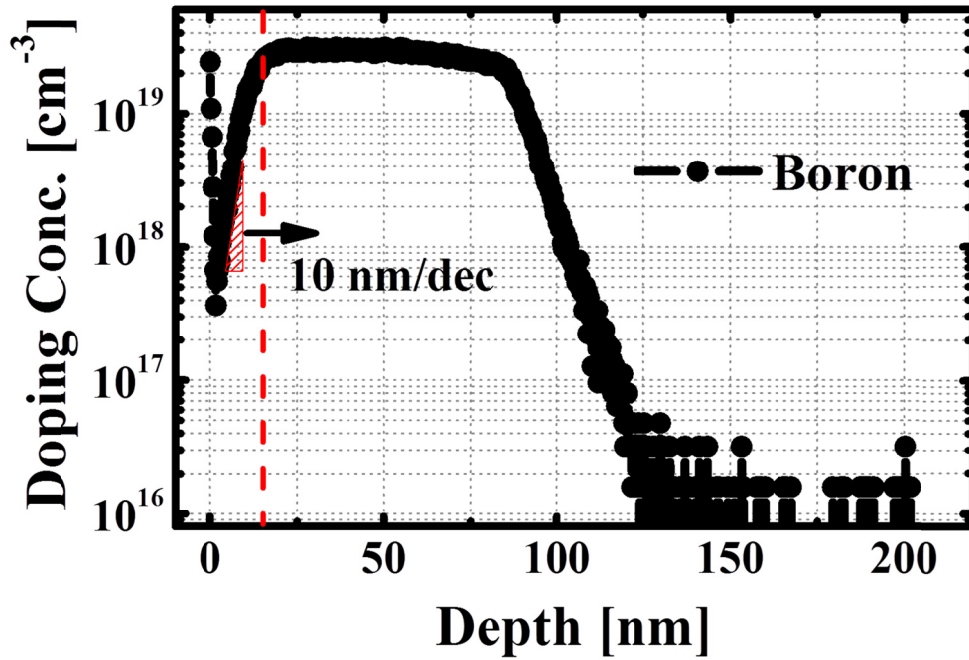
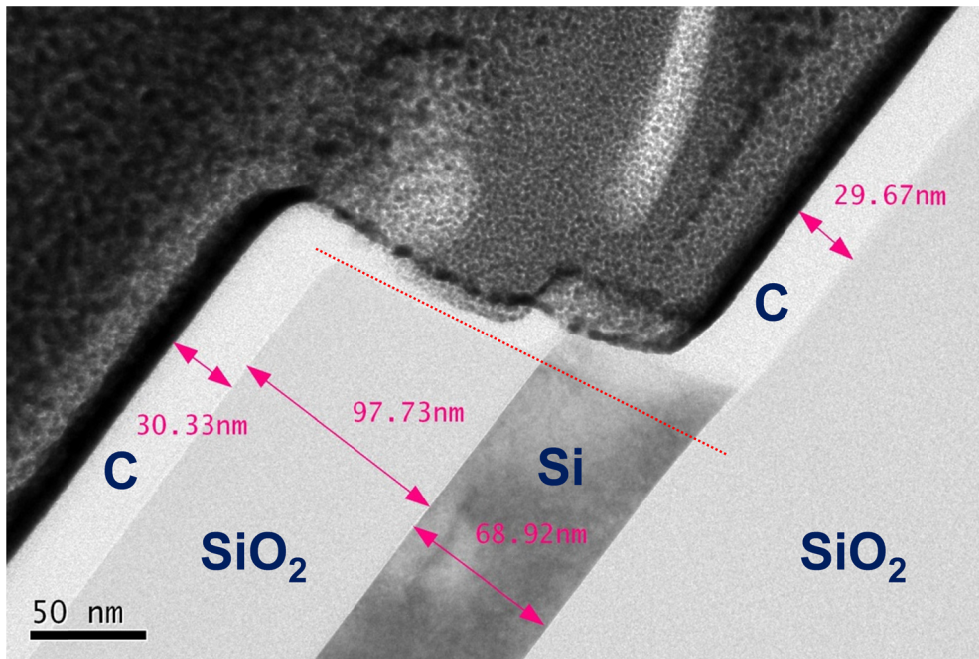
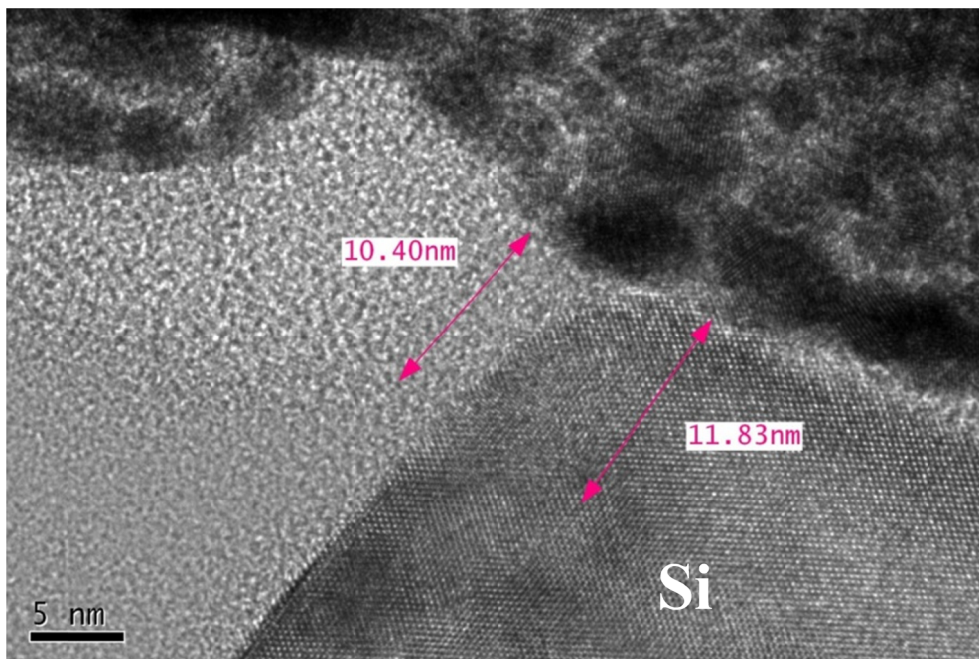


Fig. 3.7. SIMS profile from SEG region to source.



(a)



(b)

Fig. 3.8. TEM images of tunneling region, *i.e.* SEG region.

3.3 Fabrication of L-shaped TFET

On the basis of previous experiments, n-channel L-shaped TFET is fabricated as follows. After Si epitaxial layer growth on the ~100-nm SOI substrate, mesa-shaped source is patterned by RIE process with HDP oxide hard mask of ~200-nm thick. Figure 3.9 shows scanning electron microscope (SEM) images at (a) source and (b) drain after mesa patterning. The inset of Fig. 3.9(a) indicates the thickness of epitaxially grown source is about 45 nm. Furthermore, all of highly doped p⁺-region is removed at drain side as well as at mesa boundary although etch thickness differs from each other ~10 nm due to the microtrenching effect.

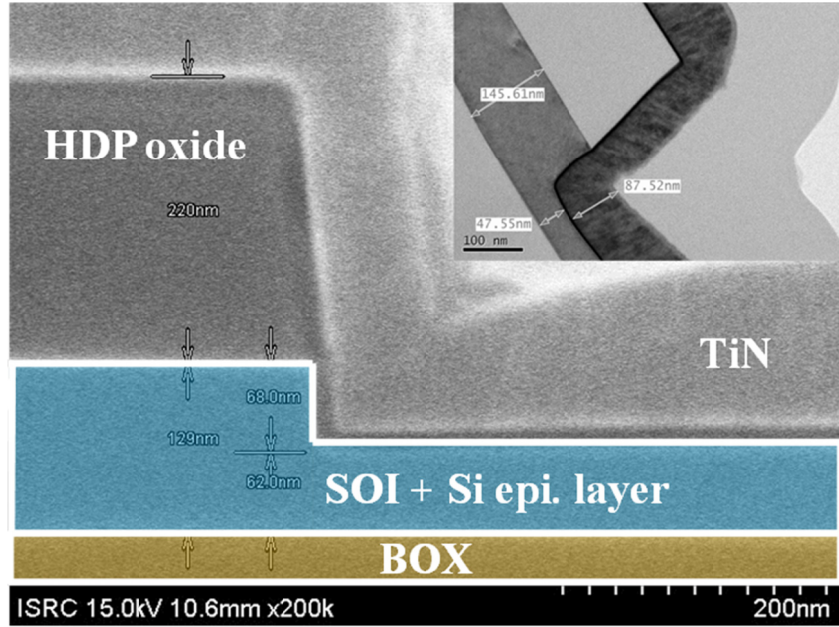
After the mesa-shaped source formation, As ions are implanted on the drain side with PR mask. A PLY mask layer is used for this process based on active region as a reference layer. The same layer of PLY mask is also used for gate patterning. In order to make up for weak point of non-self-aligned process flow, mis-aligned length between the two processes is checked and minimized by in-line SEM as shown in Fig. 3.10. In order to suppress thermal diffusion, dopant activation is performed by RTA process of 850 °C, 30 sec which is equivalent to the control groups as mentioned in Section 3.1.

As mentioned in Chapter 2, the gate stack is composed of high- κ gate dielectric of HfO₂ and metal gate of TiN. As shown in Fig. 3.11, a 5.1-nm HfO₂ layer is deposited by atomic layer deposition (ALD) process, followed by SEG process and interfacial oxidation. In order to enhance the stability and electrical property at Si/HfO₂ interface, ~1.3-nm interfacial oxide is grown with the help of chemical oxidation. The process is

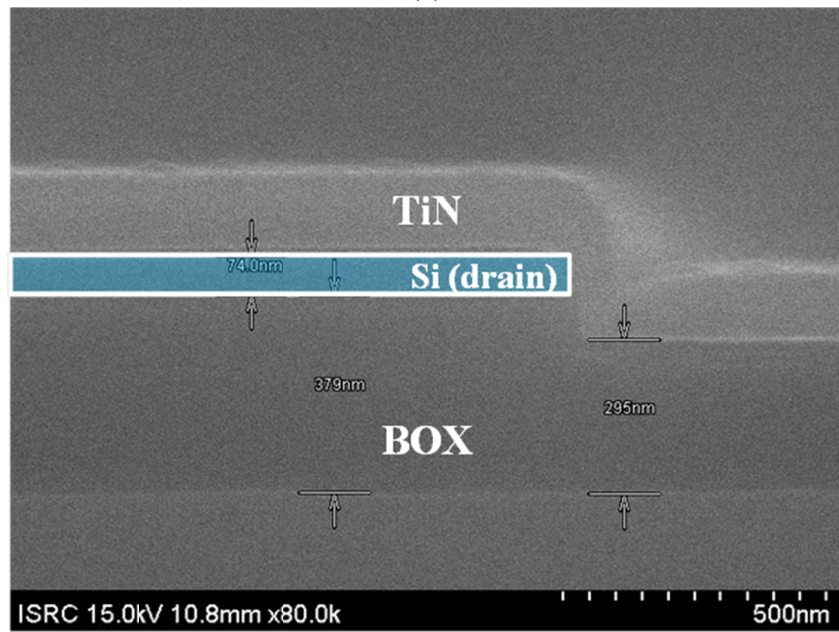
performed by the use of hydrogen peroxide (H_2O_2) at 120 °C, 3 min. Its electrical characteristics will be examined in Chapter 4.

The TiN gate is patterned by RIE etch process with Cl_2 and BCl_3 gases. Although the etchants have poor selectivity among the TiN gate, HfO_2 gate dielectric, and Si substrate, the source region is out of concern since there exist sufficient amount of etching stop layer of HDP oxide as shown in Fig. 3.12(a). On the other hand, it is necessary to approach more carefully at the drain side. Several tests have been performed, and TiN on the main wafers are well patterned by almost just etch (Fig. 3.12(b)). The residual HfO_2 has been removed by 50 : 1 diluted hydrofluoric acid (DHF) at room temperature, 1 min.

For the first step of back-end process, in order to have moderate level difference between the source and the drain, the HDP oxide located on the source region is removed by the use of PSD mask layer that could selectively open at the source side. After that, ~3000 Å of TEOS oxide is deposited by PEVCD process for ILD. Finally, metal layers are deposited and patterned, followed by contact hole formation. A TEM image of fabricated L-shaped TFET is shown in Fig. 3.13.



(a)



(b)

Fig. 3.9. SEM images after mesa patterning. (a) Source and channel. (b) Drain. The inset of Fig. 3.9(a) is TEM image at the same point after all the process is finished.

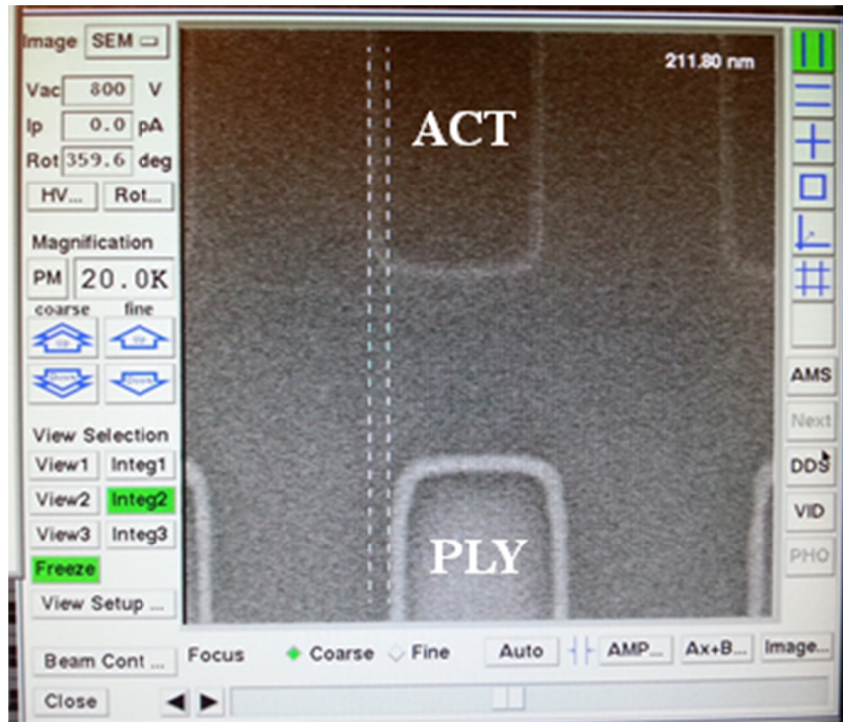


Fig. 3.10. In-line SEM image after photolithography of POLY layer.

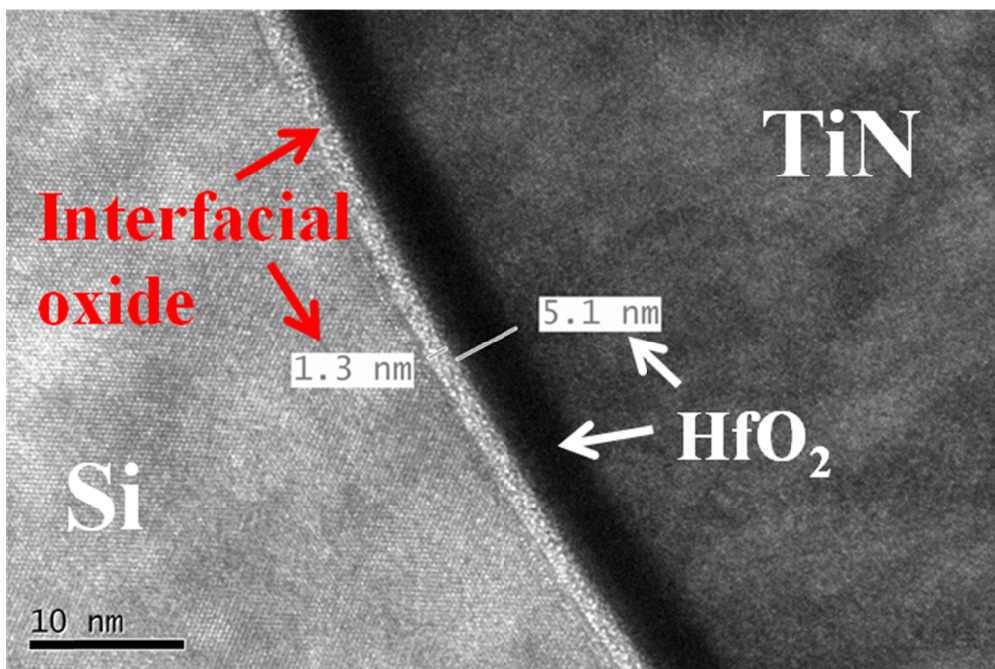
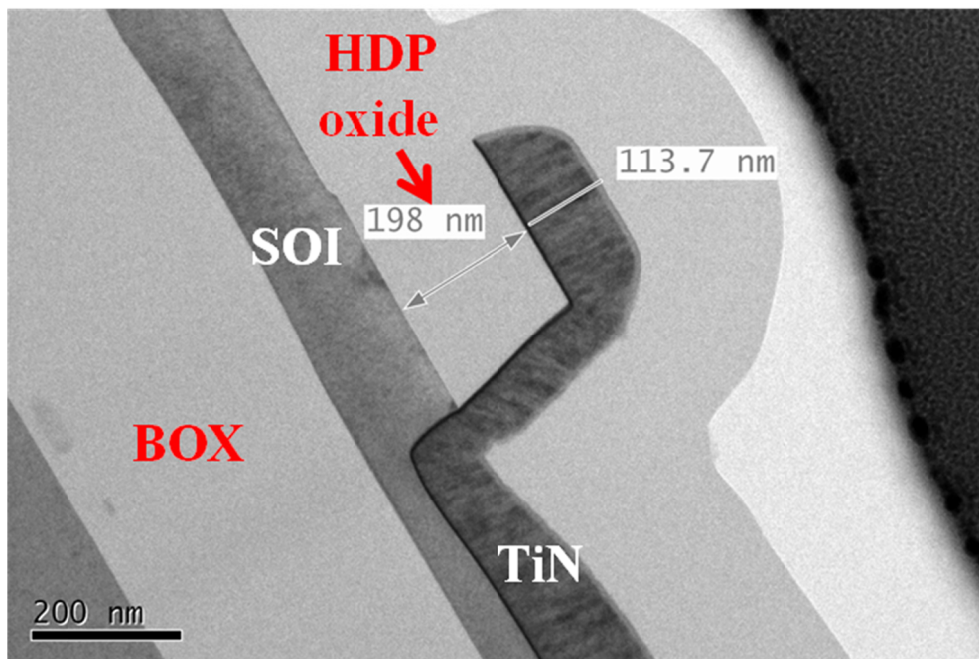
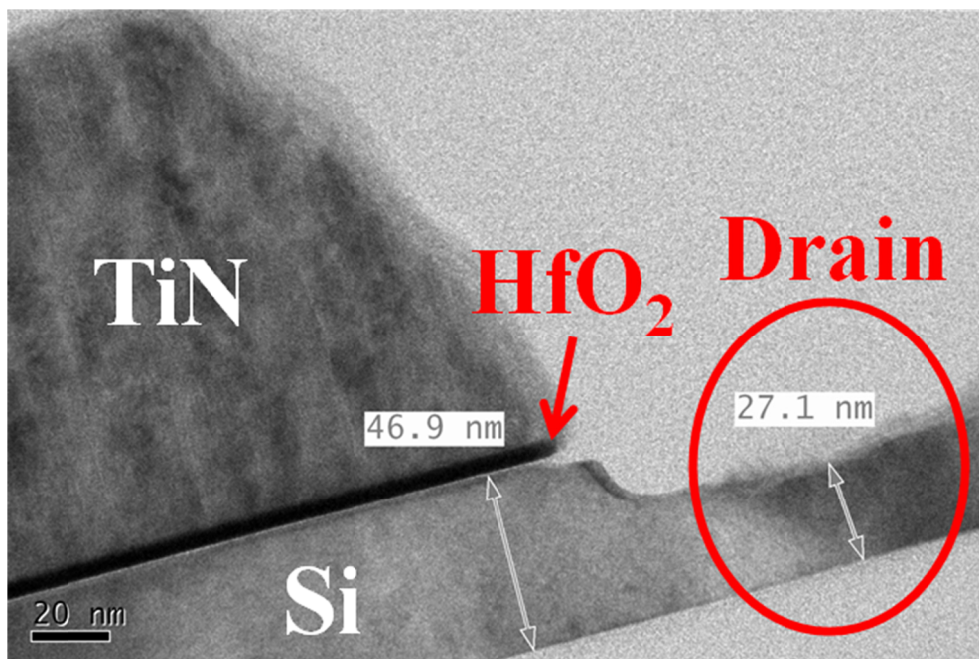


Fig. 3.11. TEM image of High- κ /metal gate stack.



(a)



(b)

Fig. 3.12. TEM images after TiN gate patterning. (a) Source and (b) drain side.

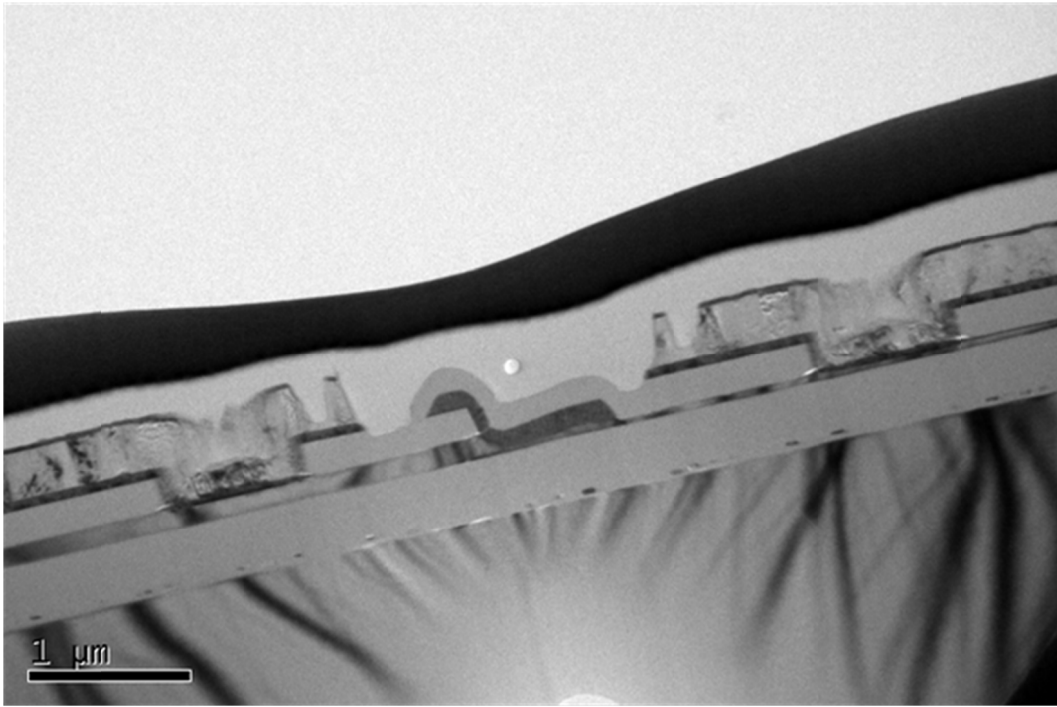
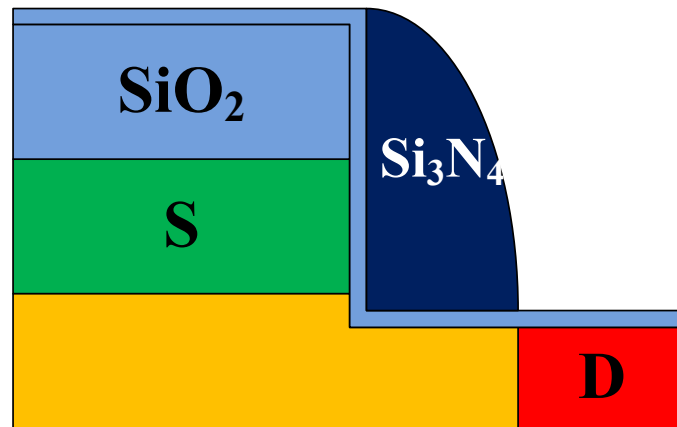


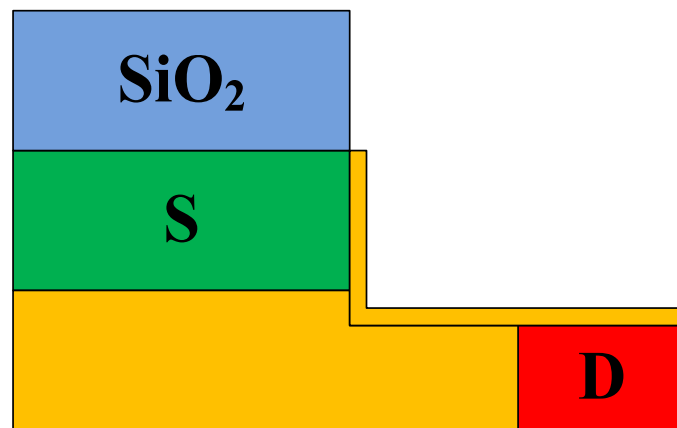
Fig. 3.13. TEM images of fabricated L-shaped TFET.

3.4 Sidewall Spacer for Minimization of Mis-alignment

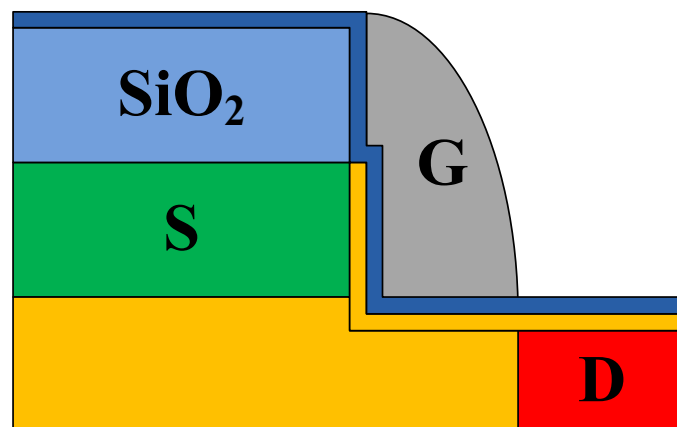
Using a sidewall spacer technique twice rather than damascene gate process proposed in Section 2.3, sub-100-nm L-shaped TFET could be fabricated even simpler minimizing mis-alignment. Modified process flow is shown in Fig. 3.14. The process up to drain formation using Si_3N_4 sidewall spacer (a) is the same as previous flow of Fig. 2.14. And then, SEG process is performed after the removal of Si_3N_4 spacer and SiO_2 buffer layer (b). For the gate stack, after HfO_2 ALD process, TiN gate is formed by RIE process followed by metal organic CVD (MOCVD) process for high step coverage (c). Figure 3.15 shows TiN sidewall spacer can be controlled sub-100-nm range.



(a)



(b)



(c)

Fig. 3.14. Modified process flow to minimize mis-alignment.

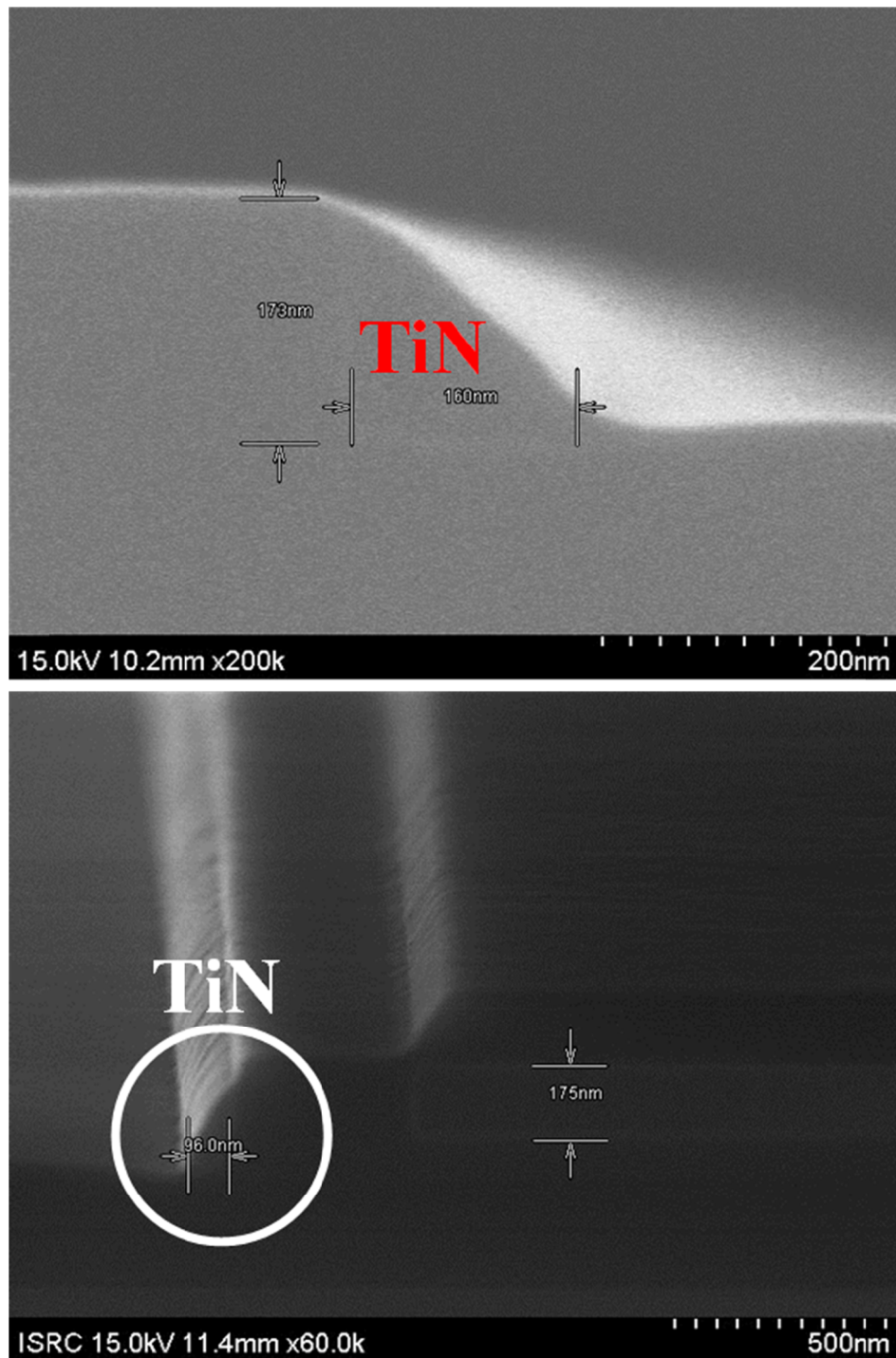


Fig. 3.15. SEM images of TiN sidewall spacer.

Chapter 4

Device Characteristics

4.1 Metal-Oxide-Semiconductor (MOS) Capacitor

As mentioned in Sections 1.3 and 2.4, the EOT of gate dielectric influences on the S_{avg} and I_{on} properties. Because sub-3-nm gate dielectric technology is not established at ISRC, the quality of gate dielectric is characterized with MOS capacitor on bulk wafers. It is used for monitoring the gate stack of L-shaped TFETs and composed by high- κ /metal gate stack for low temperature process flow.

Figure 4.1 shows the capacitance-voltage (C - V) characteristics of 5.8-nm HfO_2 gate dielectric with TiN gate, measured by Agilent HP4284 precision LCR meter. They show frequency dispersion behavior due to parasitic series resistance (R_s). In order to remove dispersion component for exact capacitance value, two-frequency method has been used [45], [46] (Fig. 4.2).

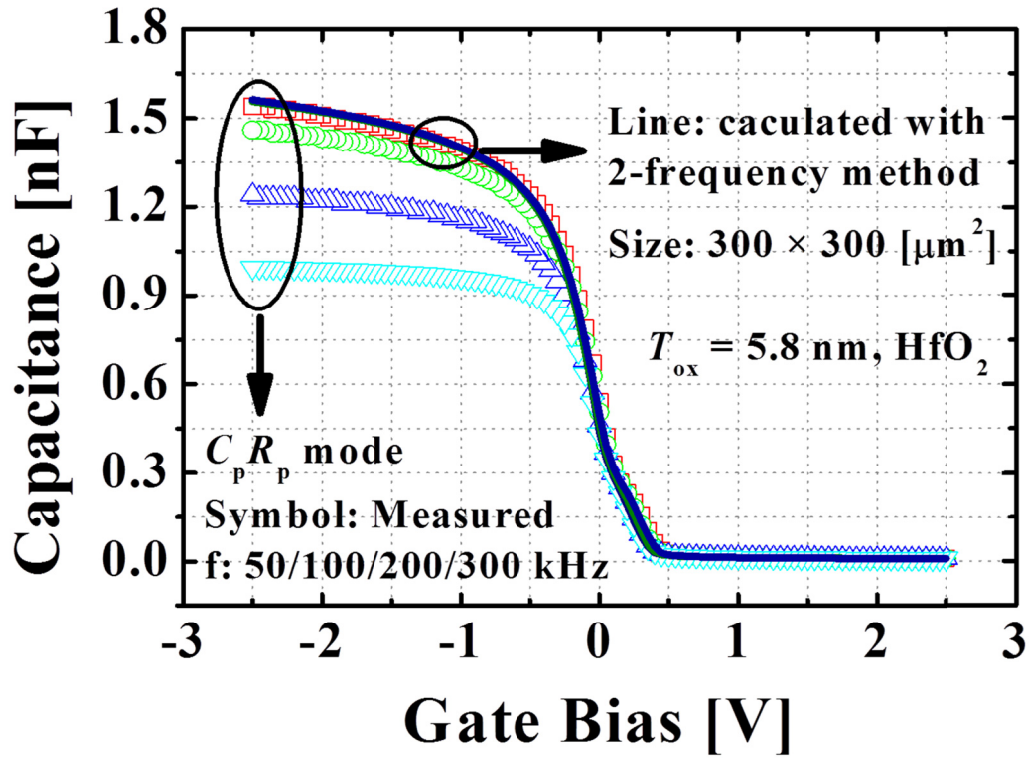


Fig. 4.1. C - V curves of MOSCAP using high- κ /metal gate stack. The symbols represent measured results with four different frequencies of 50, 100, 200, 300 kHz and the solid lines denote compensated C - V curves using two-frequency method with different six combinations of four frequencies (${}_4C_2 = 6$). They are converged on one curve and EOT is calculated from that.

Figure 4.3 presents (a) extracted EOTs and (b) V_{fb} as a function of HfO_2 thickness. The fitting of both curves are well established by linear functions. From Eq. 4.1 and 4.2, the slope of linear fitting curve in Fig. 4.3(a) is the ratio of dielectric constant between SiO_2 and HfO_2 . Since the relative permittivity of SiO_2 is 3.9, that of HfO_2 is calculated by 17.3. On the other hand, if all of oxide charges are located at Si/HfO_2 interface, the V_{fb} of MOS capacitor is expressed as Eq. 4.3 [47]. As a result, y-intercept of linear

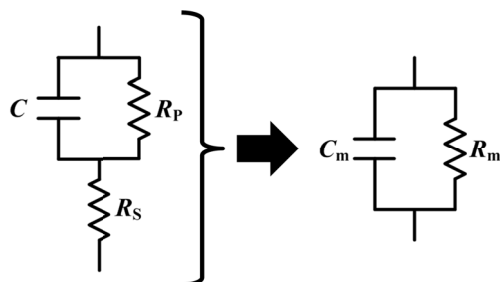
fitting curve in Fig. 4.3(b) represents the W_{fn} difference between the TiN and the Si substrate. Because the Si substrate is doped by 10^{15} cm^{-3} boron, its Fermi-level is located $\sim 0.29 \text{ eV}$ below the mid-gap as shown in Eq. 4.4. As a result, the W_{fn} of TiN gate is examined as 4.58 eV which is almost the midgap of Si.

$$C_{\text{ox}} = A \frac{\epsilon_{\text{ox}}}{\text{EOT}} = A \frac{\epsilon_{\text{HfO}_2}}{T_{\text{ox}}} \quad (4.1)$$

$$\frac{\text{EOT}}{T_{\text{ox}}} = \frac{\epsilon_{\text{ox}}}{\epsilon_{\text{HfO}_2}} = \frac{\kappa_{\text{ox}}}{\kappa_{\text{HfO}_2}} \quad (4.2)$$

$$V_{\text{fb}} = \phi_{\text{ms}} - \frac{Q_{\text{ox}}}{C_{\text{ox}}} = \phi_{\text{ms}} - \frac{Q_{\text{ox}}}{A \epsilon_{\text{HfO}_2}} T_{\text{ox}} \quad (4.3)$$

$$\phi_{\text{B}} = \frac{k_{\text{B}} T}{q} \ln \left(\frac{N_{\text{B}}}{n_{\text{i}}} \right) \approx 0.29 \text{ eV} \quad (4.4)$$



$$Z = R_s + [(j\omega C)^{-1} \parallel R_p] \quad \left| \quad Z = [(j\omega C_m)^{-1} \parallel R_m] \right.$$

$$Z = \frac{R_p(1 - j\omega C R_p)}{1 + \omega^2 C^2 R_p^2} \quad \left| \quad Z = \frac{D - j}{\omega C_m(1 + D^2)} \right.$$

$$\text{Im}(Z) = \frac{-\omega C R_p^2}{1 + \omega^2 C^2 R_p^2} \quad \left| \quad D = (\omega R_m C_m)^{-1} \right.$$

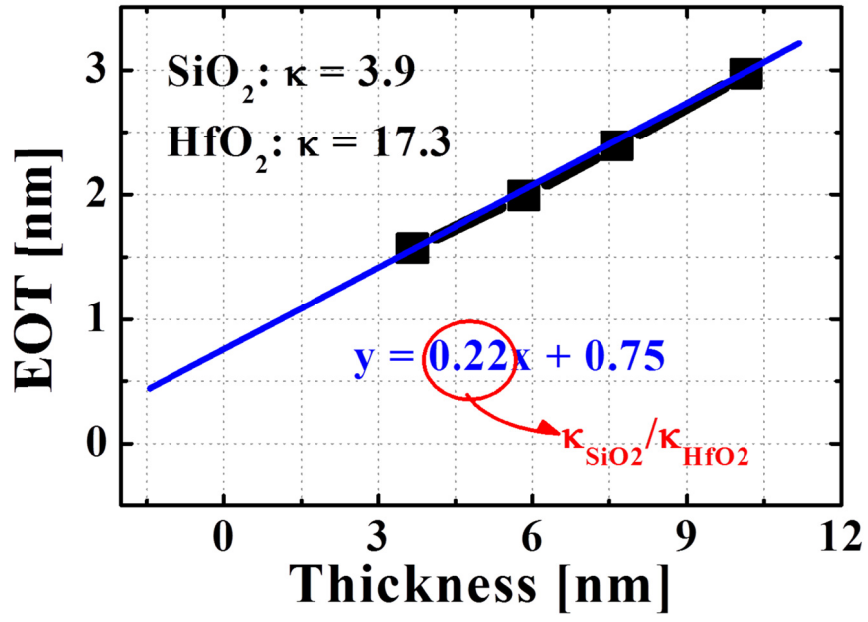
$$\quad \quad \quad \text{Im}(Z) = \frac{-1}{\omega C_m(1 + D^2)}$$

$$\frac{1 + \omega^2 C^2 R_p^2}{C R_p^2} = \omega^2 C_m(1 + D^2)$$

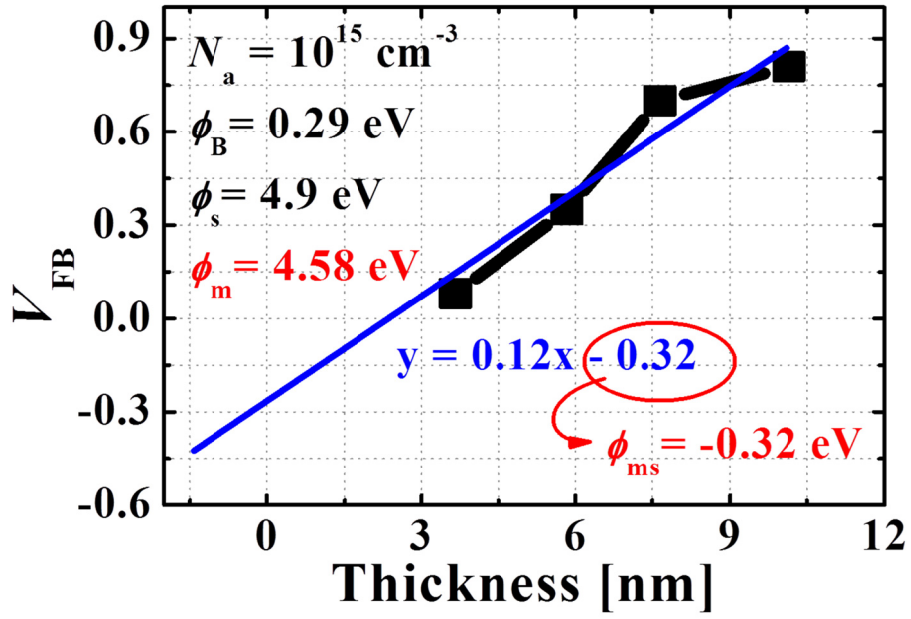
$$\therefore C = \frac{f_1^2 C_{m,1}(1 + D_1^2) - f_2^2 C_{m,2}(1 + D_2^2)}{f_1^2 - f_2^2}$$

$$, \text{ where } D_i = \frac{1}{\omega_i C_i R_i}$$

Fig. 4.2. Two-frequency method to remove frequency dispersion components.



(a)



(b)

Fig. 4.3. (a) Extracted EOTs and (b) V_{fb} as a function of HfO₂ thickness.

4.2 Control Samples of Conventional Planar TFETs

For the control samples, n- and p-channel planar TFETs are fabricated by following the process flow depicted in Section 3.1. For the measurement system, Agilent 4156C and B1500 have been used to obtain the current-voltage (I - V) characteristics.

Figure 4.4 shows transfer and output curves of n-channel TFET and detailed doping condition for source is BF_2 , $3 \times 10^{13} \text{ cm}^{-2}$ and that for drain is As , $3 \times 10^{13} \text{ cm}^{-2}$. The device shows minimum S of 102 mV/dec and I_{on} of $\sim 3 \text{ nA}/\mu\text{m}$ when the V_g and V_d is equal to 1.5 V.

On the other hand, Fig. 4.5 presents electrical performance when the device under the p-channel operation condition. Also, the doping condition for source is As , $3 \times 10^{14} \text{ cm}^{-2}$ and that for drain is BF_2 , $3 \times 10^{13} \text{ cm}^{-2}$. Because both devices have used n^+ -poly-Si gate, a $V_{\text{turn-on}}$ of p-channel TFET is higher than that of n-channel device even though doping concentration of source is higher than its counterpart. The device shows minimum S of 78 mV/dec and I_{on} of $\sim 0.8 \text{ nA}/\mu\text{m}$ when the V_g and V_d is equal to -1.5 V. The lower level of I_{on} than n-channel TFET is caused by high $V_{\text{turn-on}}$.

In summary, conventional planar TFETs suffer from higher S_{avg} and lower I_{on} than theoretical expectation. The differences of output characteristics, especially in the linear region, are suspected by coming from different junction profile and abruptness as well as doping conditions.

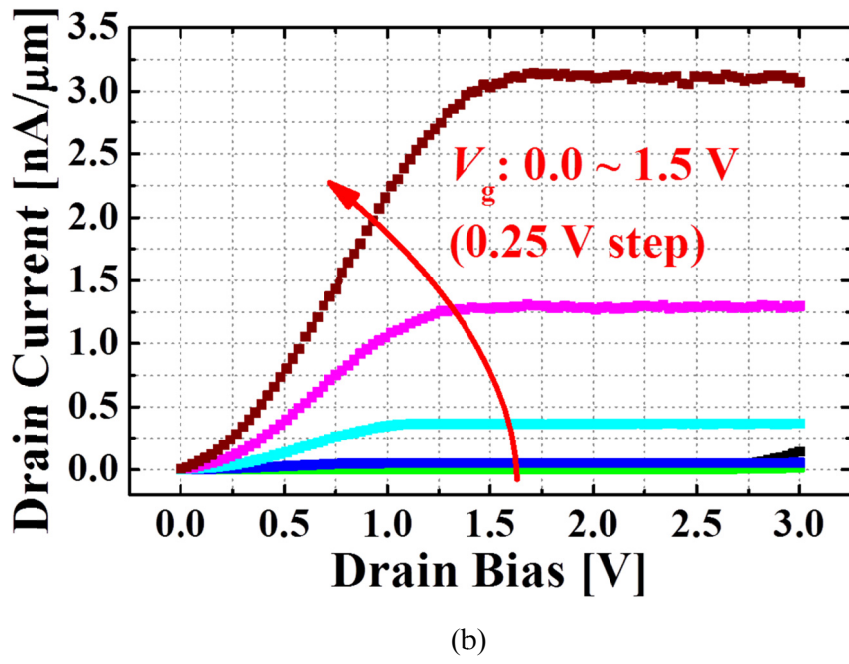
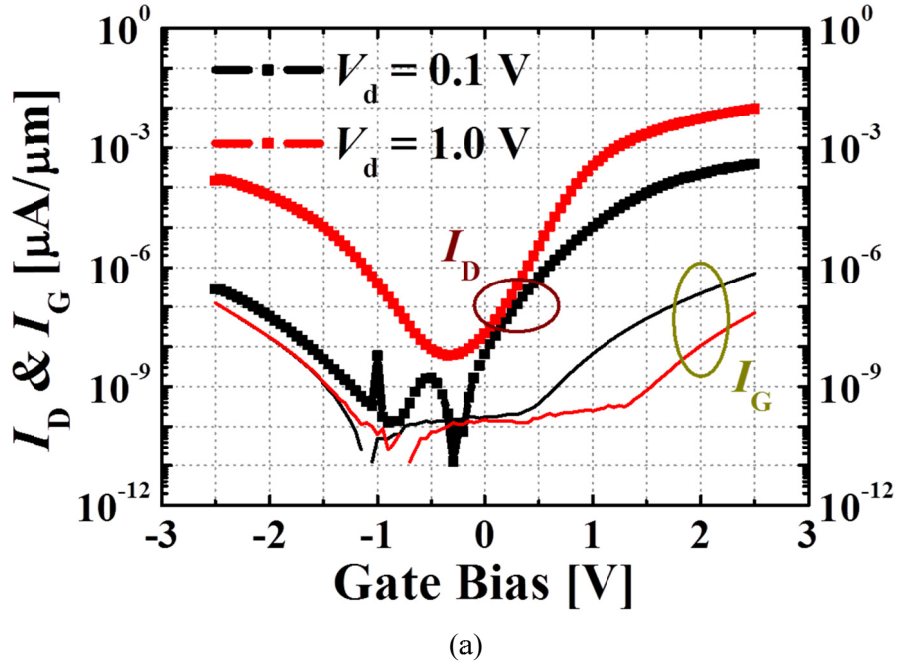


Fig. 4.4. (a) Transfer and (b) output curves of n-channel TFET.

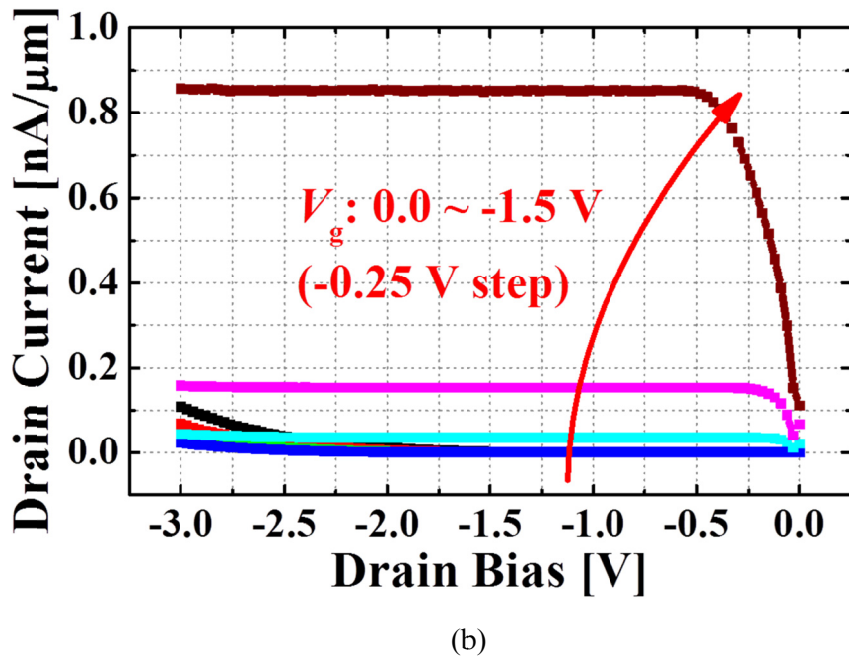
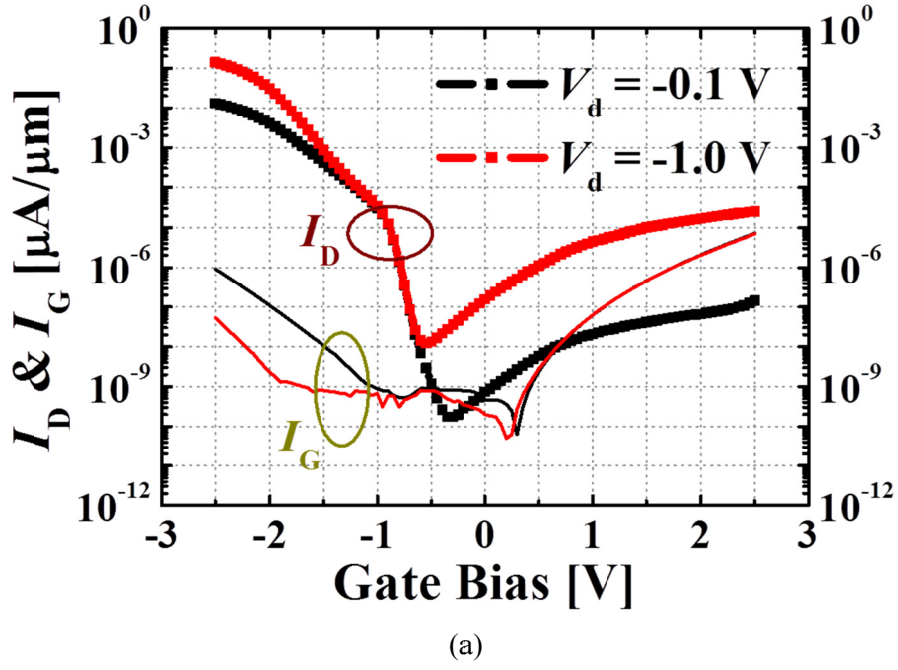


Fig. 4.5. (a) Transfer and (b) output curves of p-channel TFET.

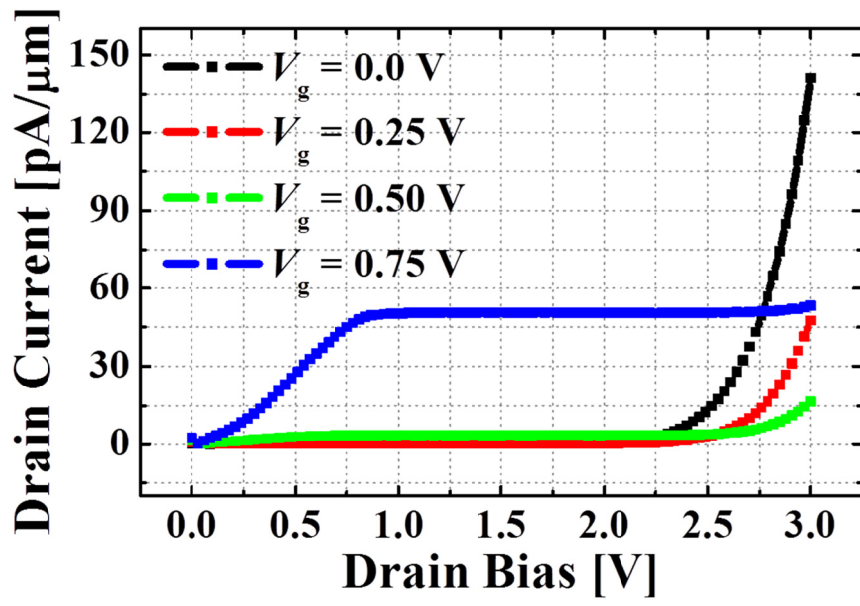
Figure 4.6 shows abnormal behaviors in TFETs' output curves. In the aspect of further increase of I_d beyond current saturation, it is similar to the MOSFET breakdown or SCE including channel length modulation. However, it is obvious that physics behind the phenomena are fundamentally different. For example, if the V_g is small, I_d increases more severely with low V_d and it is contrast trend compared with the abovementioned phenomena of MOSFETs. In order to verify these results, a 2-D device simulation has been performed with the help of Synopsis SentaurusTM. The geometrical parameters of simulated device are the same as fabricated n-channel TFETs except the L_g is 0.1 μm . As shown in Fig. 4.7, simulation results are well corresponded to the experimental data of Fig. 4.4(b) and 4.6(a).

Figure 4.8(a) shows energy band diagrams with various V_d 's while V_g is fixed at 0.5 V. It suggests that the output characteristics of TFETs can be classified by three different operating regions. First, if the V_d is increased approximately from 0 to 1 V, most of V_d appear across source/channel tunnel junction due to large R_{tun} . Because W_t is decreased with large \mathcal{E} , I_d is increased rapidly in this region, as shown in Fig. 4.4-4.7. Secondly, if the V_d is in the range of 1 to 2 V, depletion region at source/channel junction is expanded all over the channel and only the potential near the drain side is affected by V_d [48]. Because electric field from the drain cannot effect on the tunnel junction, I_d is saturated. Last of all, if V_d is higher than 2.0 V, valence electrons at channel can tunnel to the drain side as depicted in Fig. 4.8(b), *i.e.* ambipolar behavior is induced by V_d .

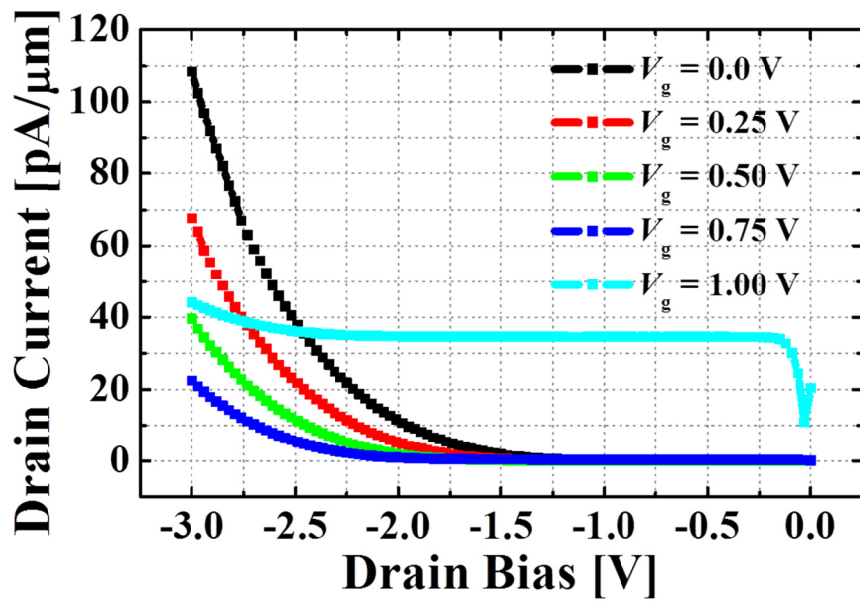
Until now, most of researches have concerned about I_{amb} in the aspect of I_{off}

increase as a function of V_g . However, these results imply that I_{amb} also induced by V_d . If the V_g is small, channel potential is much lower than drain potential. As a result, valence band maximum of channel ($E_{V\text{-ch,max}}$) and conduction band minimum of drain ($E_{C\text{-d,min}}$) can be aligned even though V_d is low, *i.e.* occurrence of ambipolar behavior. Because the main application field of TFETs is LOP device, these phenomena are problematic severely and should be suppressed for its applications with large amount of operating voltage window.

There exist many solutions to reduce I_{amb} and first of all, the uses of gate material with appropriate W_{fn} . As mentioned at the beginning of this section, n^+ -poly Si is used for both kinds of control TFETs. As a result, the potential difference between channel and drain of p-channel TFET is larger than that of n-channel TFET. It is consistent with Fig. 4.6, which shows the ambipolar behavior is much severer in the case of p-channel operation. Consequently, gate material with appropriate W_{fn} should be selected for small $V_{\text{fb}} \approx \phi_{\text{ms}}$ and for constraint of I_{amb} . In addition to the W_{fn} engineering, gate-drain underlap region and moderated drain doping is also helpful to decrease I_{amb} , since they can effectively reduce the \mathcal{E} at channel/drain tunnel junction [14-16]. Last of all, using hetero gate dielectric to make large EOT localized at drain side is also one of well-known methods to suppress I_{amb} [18].

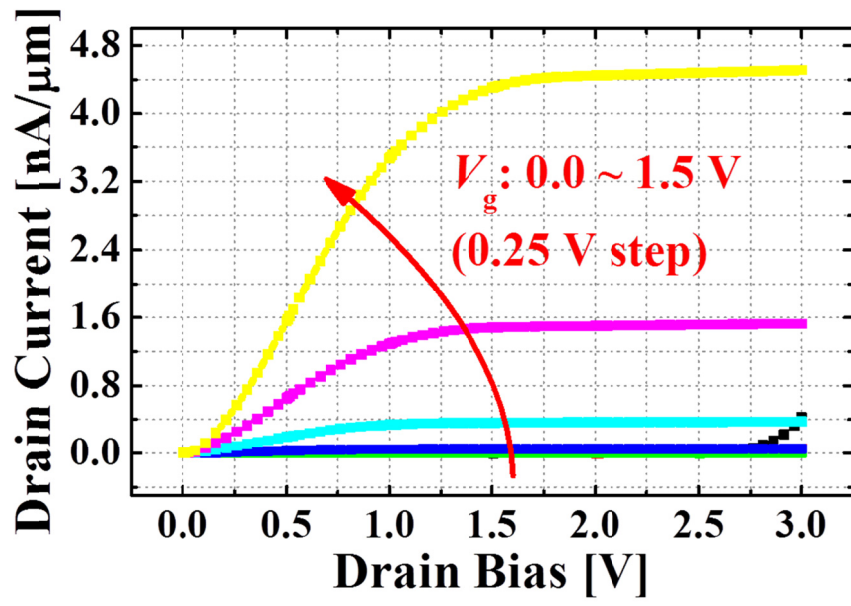


(a)

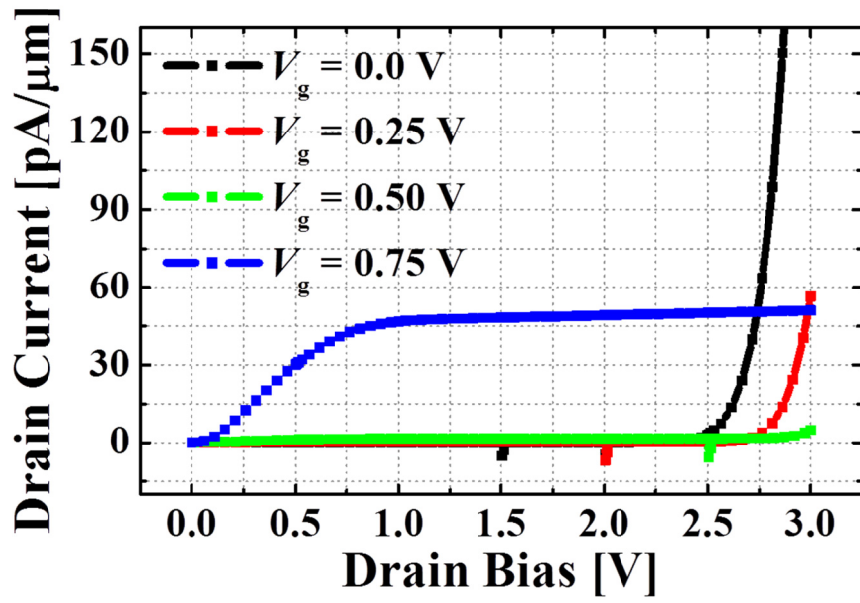


(b)

Fig. 4.6. Output characteristics of (a) n- and (b) p-channel TFET.

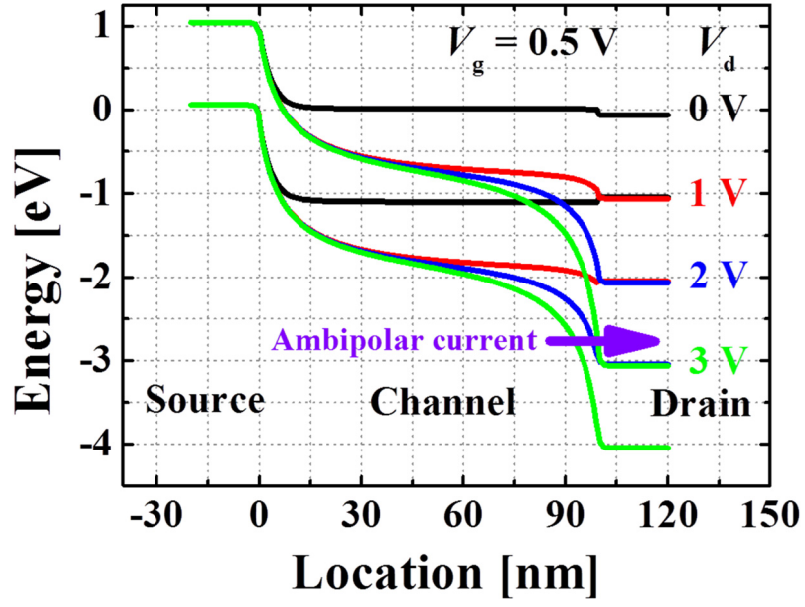


(a)

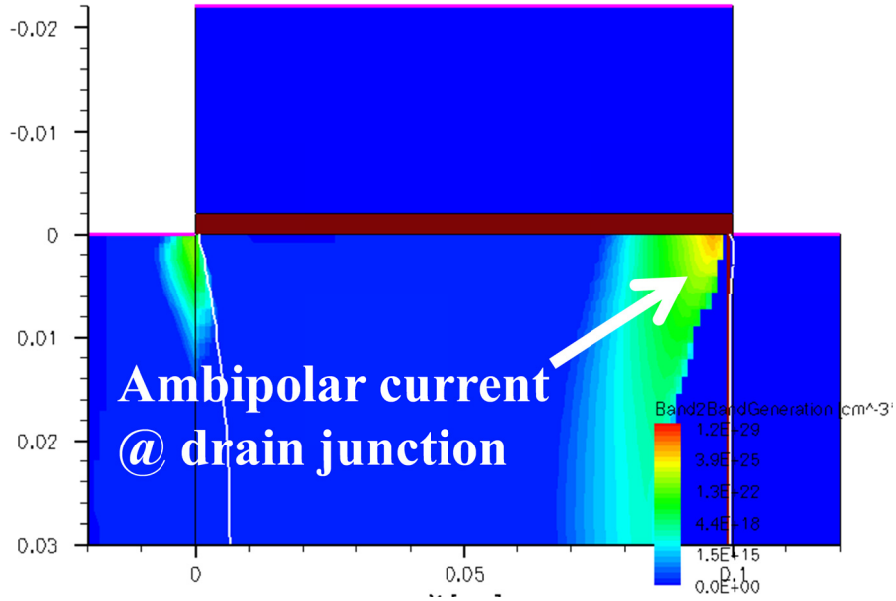


(b)

Fig. 4.7. Simulated output characteristics of n-channel TFET. Simulation tool: Synopsys Sentaurus™.



(a)



(b)

Fig. 4.8. Ambipolar behavior caused by V_d . (a) Energy band diagrams. (b) 2-D contour plot of BTBT rates. Simulation tool: Synopsys SentaurusTM.

4.3 L-shaped TFETs

The electrical characteristic of p-i-n junction is carefully examined prior to the measurement of L-shaped TFET. For that purpose, L-shaped TFET with 1- μm L_g and 80- μm active width has been used while gate is floated. As shown in Fig. 4.9, the junction of L-shaped TFET is well operated as a p-i-n diode depending on V_d .

Figure 4.10(a) presents the transfer characteristics of n-channel L-shaped TFET with the V_d of 0.05, 0.5 and 0.95 V, respectively. First of all, a $V_{\text{turn-on}}$ is ~ 0.43 V and it is ~ 0.63 V higher than planar TFETs as shown in Fig. 4.4(a). It is in part attributed to difference of W_{fn} and in part attributed to increase of depletion capacitance and body coefficient as mentioned in Section 2.2. From Fig. 4.10(a), minimum S is extracted as 7, 34, 59 and 68 mV/dec and S_{avg} is calculated by ~ 120 mV/dec.

Figure 4.11 shows the comparison of transfer characteristics between planar TFET, L-shaped TFET without (w/o) SEG region and L-shaped TFET with (w/) SEG region while V_d is biased by 0.1 V. If there doesn't exist SEG region in L-shaped TFETs, its transfer characteristic becomes similar to the gate-induced drain leakage (GLDL) of MOSFETs. Because source potential as well as channel potential is affected by V_g , $V_{\text{turn-on}}$ becomes higher and I_{on} gets lower. It is consistent with the simulation results of Fig. 2.5 and 2.6 that predict the reduction of L_t results in increase of $V_{\text{turn-on}}$ and larger S_{avg} .

In order to compensate $V_{\text{turn-on}}$ effects due to the difference of W_{fn} and depletion capacitance, transfer curves are shifted with the reference of 0.1 pA. As a result, it is clear that I_{on} of L-shaped TFET is more than 10 times higher than that of conventional

planar TFET. As mentioned in Chapter 2, it is in part attributed to the scaling of S_{avg} and in part related to the larger A_t .

The weak point of L-shaped TFET in this experiment is the large I_{amb} which increases depending on V_g as well as V_d very sensitively. In the fabrication process of L-shaped TFET, non-self-aligned process flow has been adopted for convenient verification of ideas. Although the device has received a careful attention to minimize mis-alignment length between the drain and the gate, it is impossible to make it zero. Therefore, relatively large amount gate-drain overlap is suspected for the reason of larger I_{amb} . Furthermore, SEG region is formed not only at tunneling region, but also at drain side. It also contributes to the current enhancement.

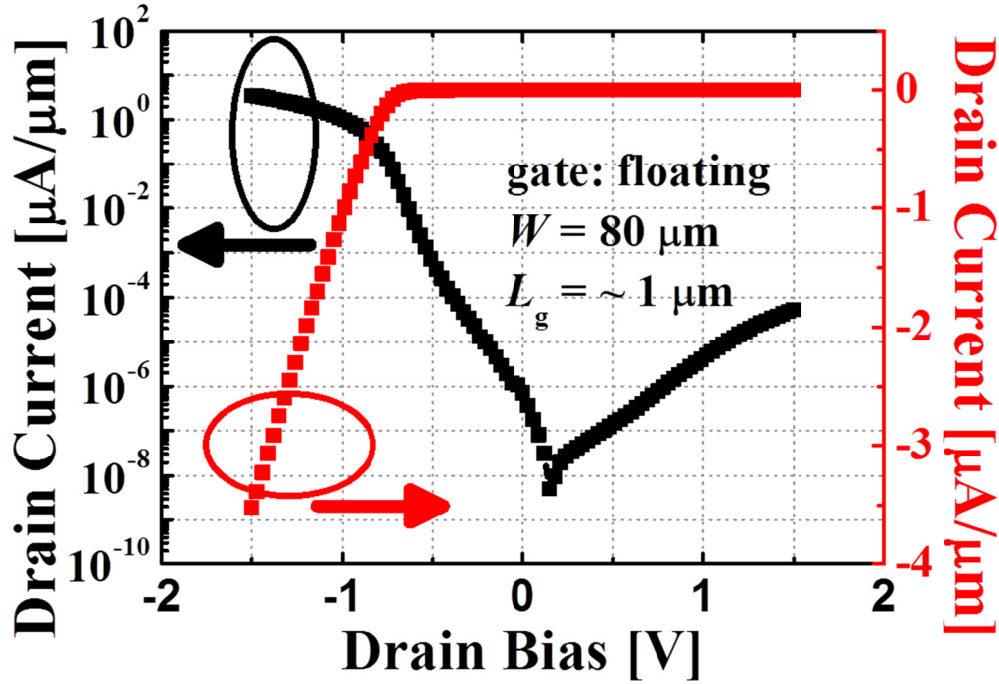
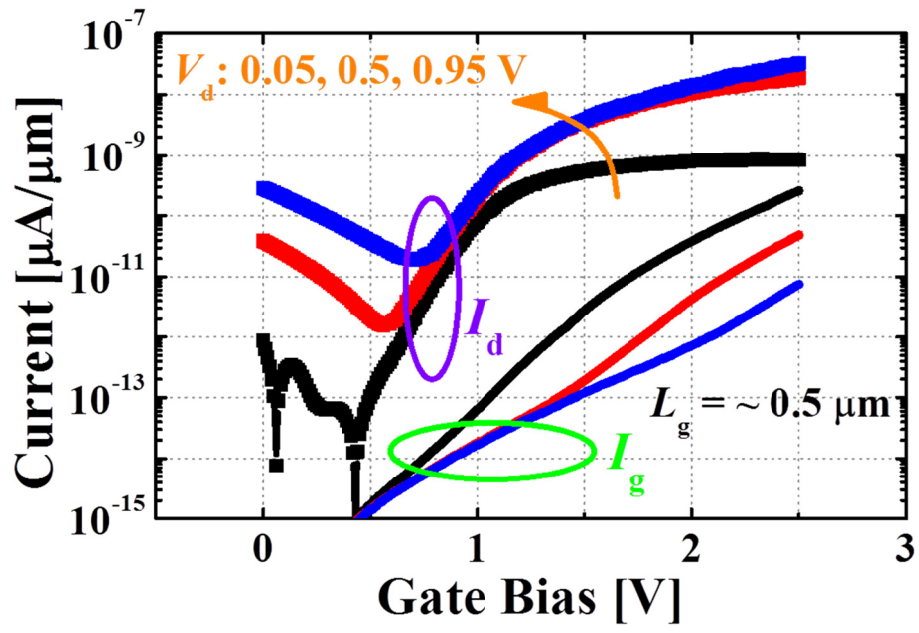
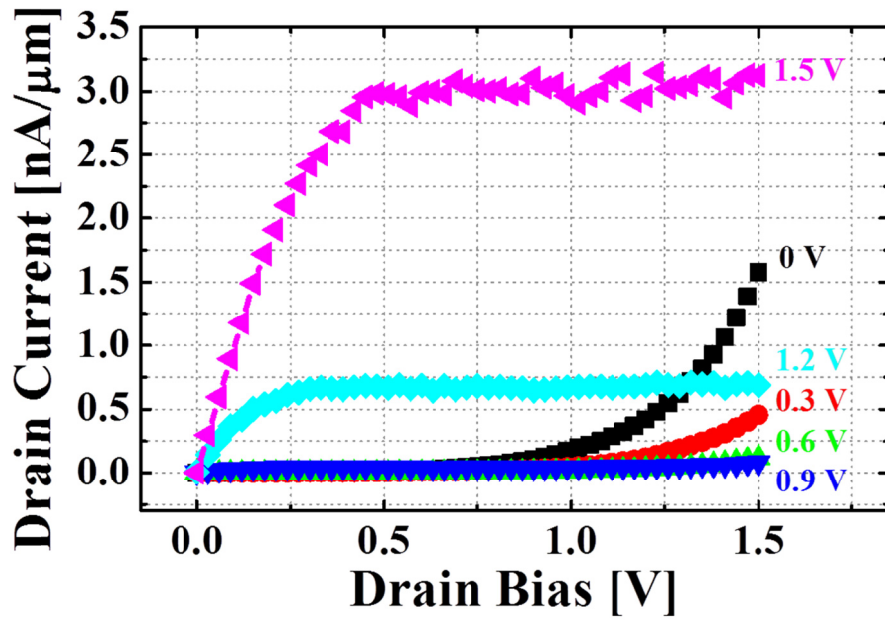


Fig. 4.9. A p-i-n junction characteristic depending on V_d .

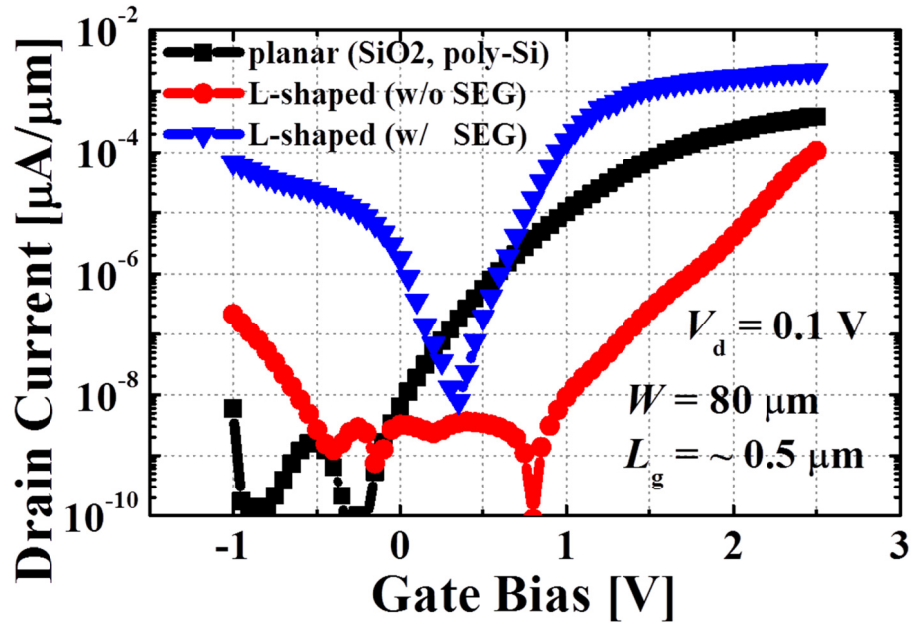


(a)

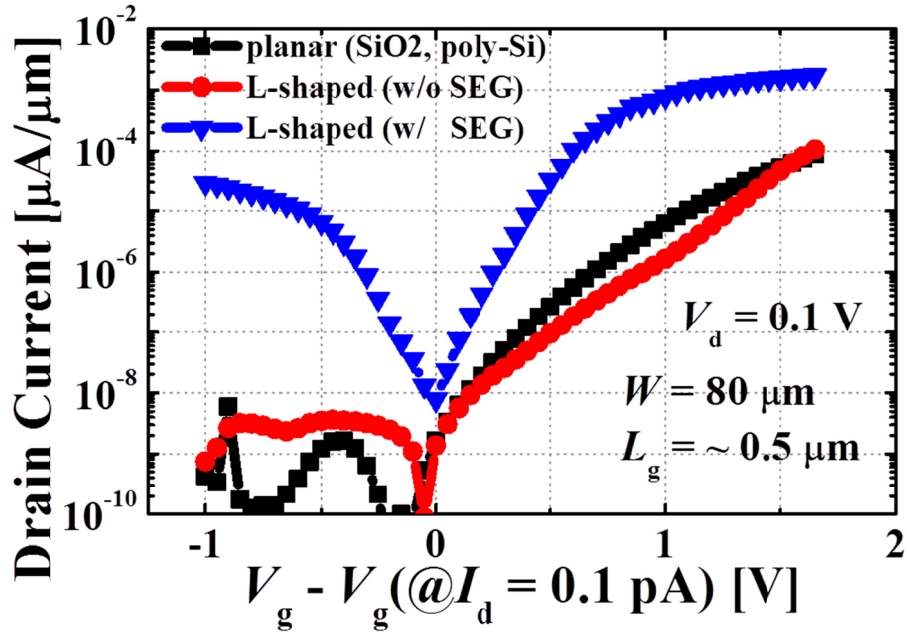


(b)

Fig. 4.10. (a) Transfer and (b) output curves of n-channel L-shaped TFET.



(a)



(b)

Fig. 4.11. Comparisons of fabricated TFETs.

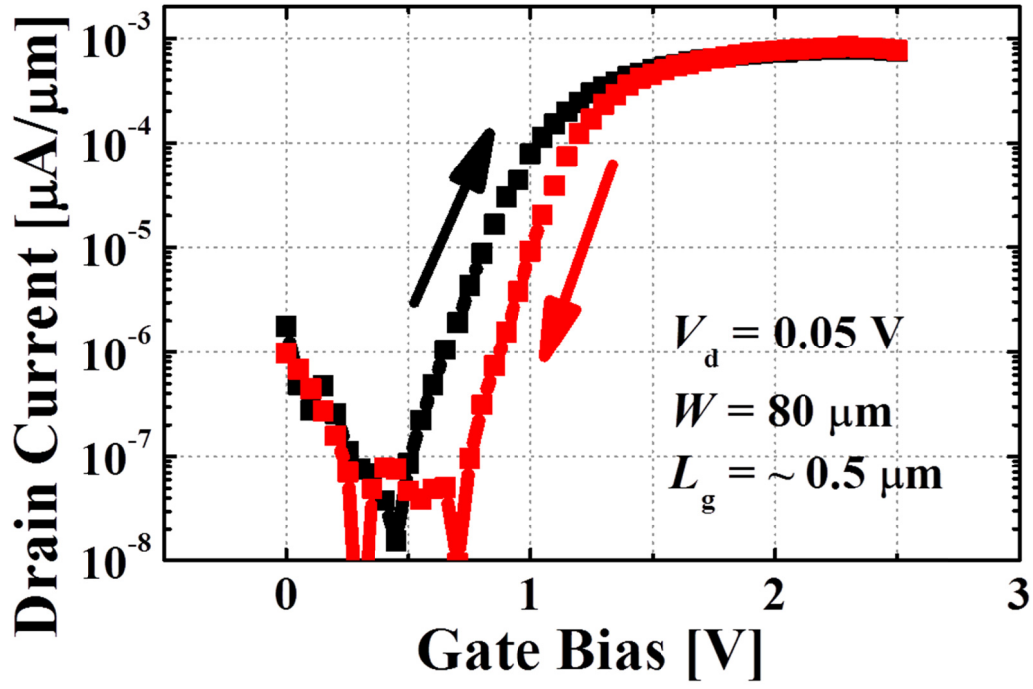


Fig. 4.12. Hysteresis in transfer characteristics.

For further improvement of L-shaped TFETs' performance, gate dielectric should be optimized. Although there exists $\sim 1.3\text{-nm}$ interfacial oxide formed by chemical oxidation as shown in Fig. 3.11, the L-shaped TFET suffers from severe hysteresis and results in degradation of S_{avg} characteristics due to the parasitic capacitance (Fig. 4.12). The quality of high- κ gate dielectric could be improved with the help of thermal annealing or plasma treatment with nitrogen gas (N_2) and alloy with hydrogen gas (H_2) [49]-[51].

4.4 Extraction of Several Electrical Parameters

For the analysis of TFETs' operation, several device parameters are extracted with the help of co-integrated MOSFETs. First of all, effective channel length (L_{eff}) excluding gate overlap and source/drain resistance (R_{sd}) are extracted by Terada-Muta method as shown in Fig. 4.13. In detail, p-type source resistance (R_{s}) and n-type drain resistance (R_{d}) refer to half of R_{sd} in p- and n-channel MOSFETs, respectively. In order to increase the accuracy of experiments, physical gate (L_{mask}) lengths are examined by in-line SEM as depicted in the inset of Fig. 4.13.

Figure 4.14 presents extracted effective channel mobility (μ_{eff}) as a function of V_{g} and effective normal electric field (\mathcal{E}_{eff}) which is calculated using Eq. 4.5. Comparing the universal mobility curves of [52], the extracted μ_{eff} has reasonable as shown in Fig. 4.14 (b). Because the SOI thickness is just about 30 nm, the μ_{eff} is much smaller than that of [52] with same doping concentration of 10^{15} cm^{-3} .

$$\mathcal{E}_{\text{eff}} = \frac{V_{\text{th}} - V_{\text{fb}} - 2\phi_{\text{B}}}{3t_{\text{ox}}} + \frac{V_{\text{g}} - V_{\text{th}}}{6t_{\text{ox}}} \quad (4.5)$$

Finally, assuming R_{ch} of L-shaped TFET is not much different from that of planar MOSFETs and all of resistors are connected in series, the R_{ch} and R_{tun} could be extracted as shown in Fig. 4.15. From the results, it is verified that L-shaped TFETs show much smaller R_{tun} , thanks to the novel structure. In addition, in spite of large amount of R_{tun} scaling, it still plays a role of dominant factor to determine I_{d} .

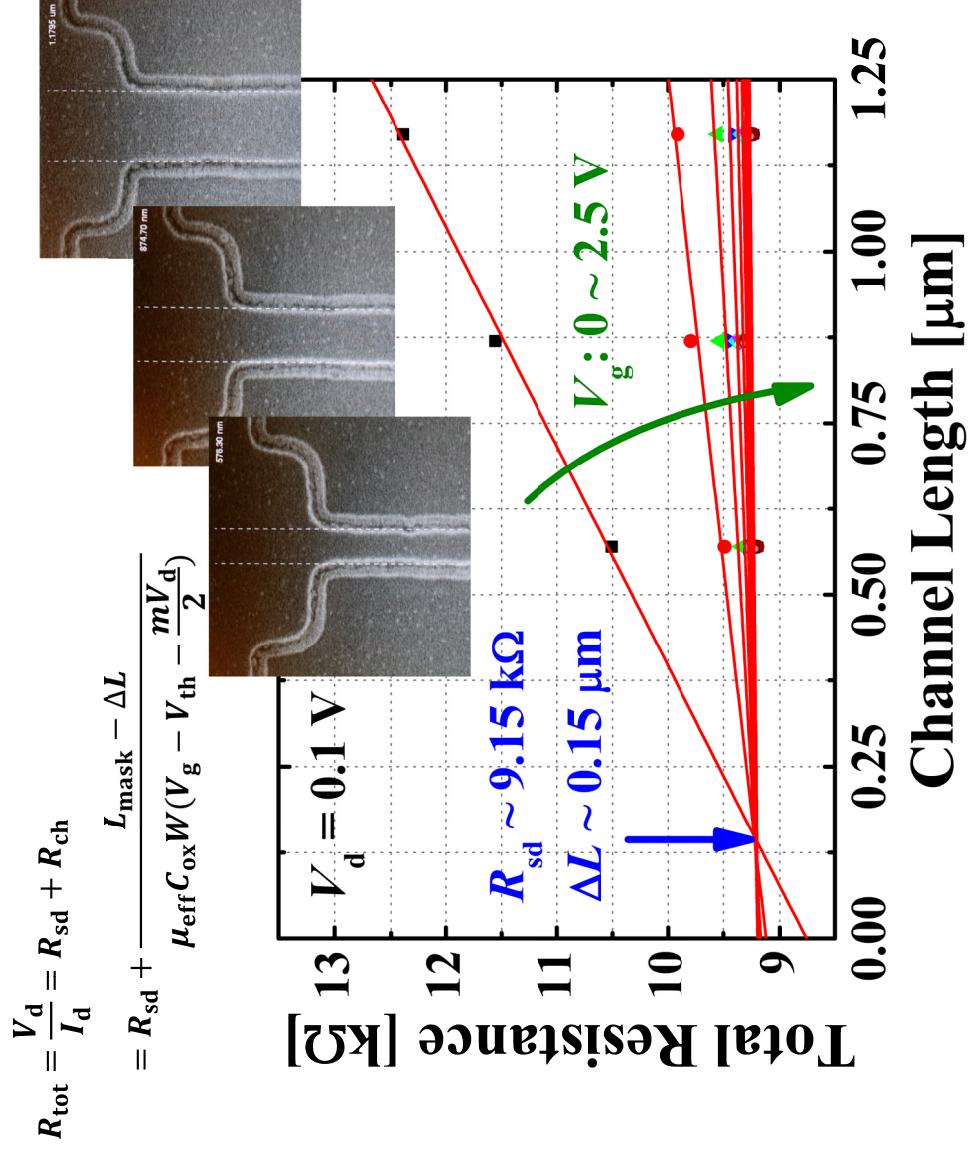
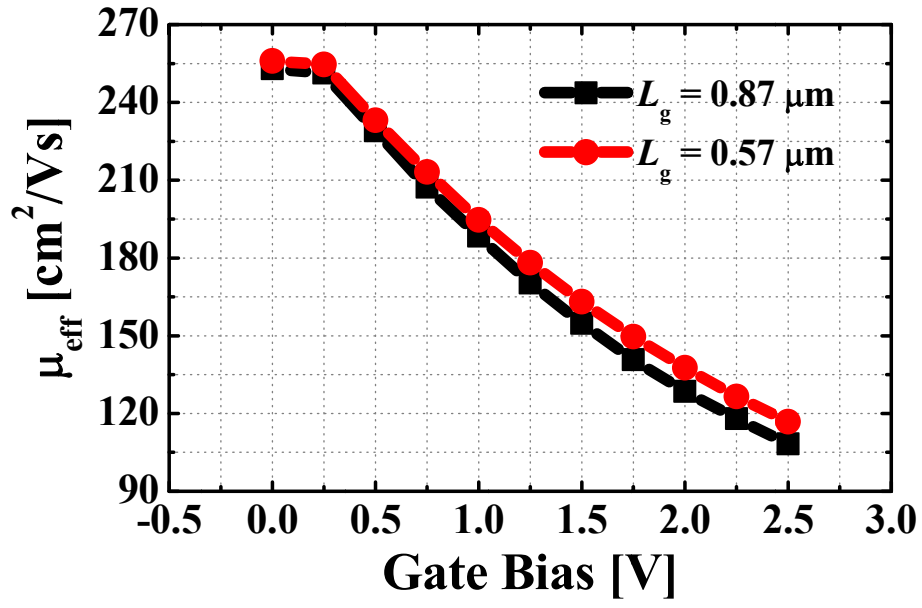
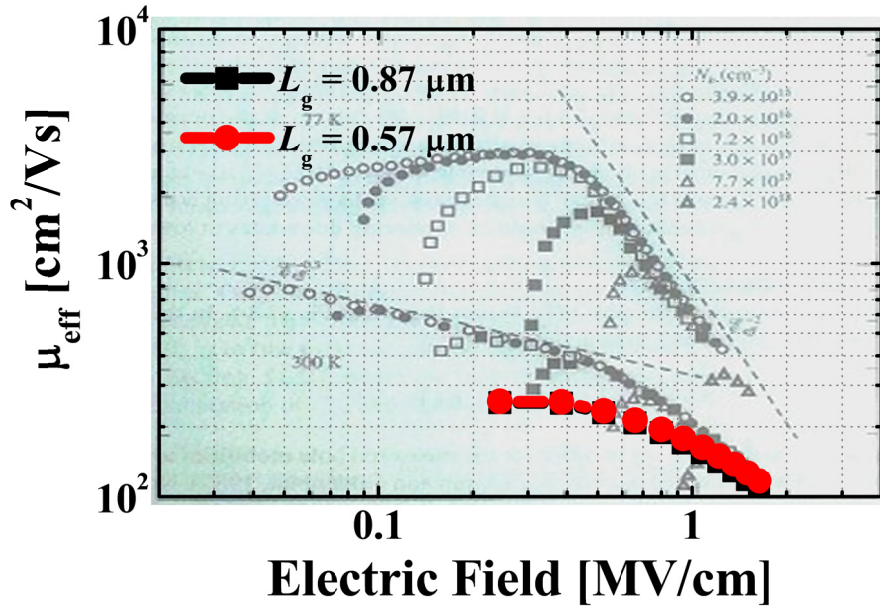


Fig. 4.13. R_{sd} extraction with Terada-Muta method.

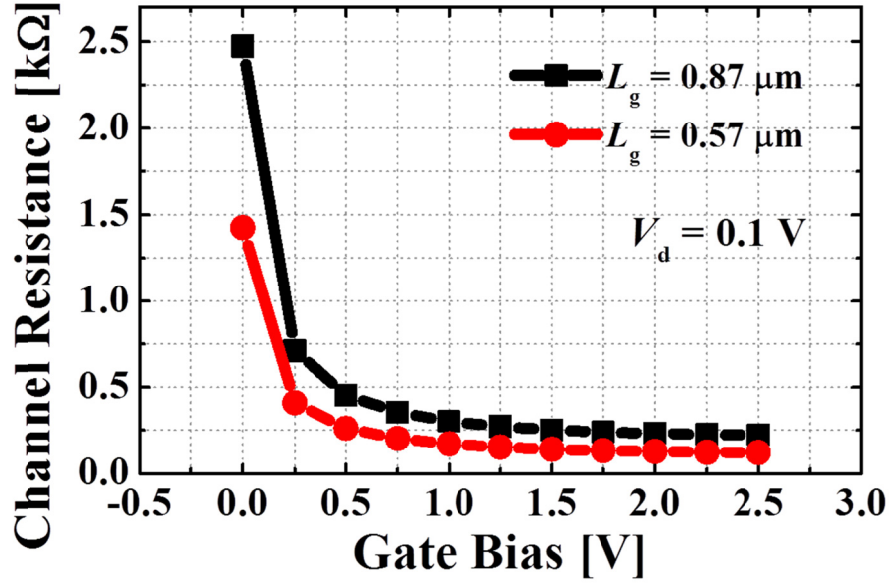


(a)

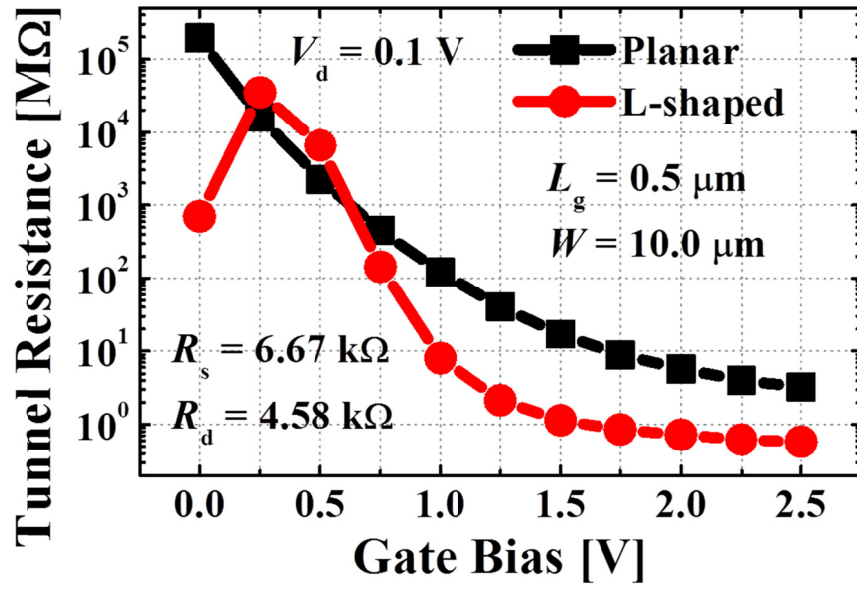


(b)

Fig. 4.14. μ_{eff} as a function of (a) V_g and (b) E_{eff} .



(a)



(b)

Fig. 4.15. Extraction of (a) R_{ch} from MOSFETs and (b) R_{tun} from TFETs.

Chapter 5

Conclusions

In this dissertation, a novel L-shaped TFET has been proposed which features BTBT direction perpendicular to the channel. Because W_t and A_t area are determined by L_t and H_t , respectively, L-shaped TFETs are expected to show better performance than conventional ones in terms of S_{avg} and I_{on} characteristics. The effects of several device parameters on the performance of L-shaped TFETs have been investigated and a design optimization is performed by TCAD simulation.

In order to fabricate L-shaped TFETs with improved performance, reduction of thermal budget is essential to restrict dopant diffusion to the tunneling region. For low temperature process flow and reduction of EOT below 3 nm, high- κ /metal gate stack process is adopted. In addition, abrupt doping profile is implemented with the help of in-situ doped epitaxial layer growth technique for source and Si SEG process for tunneling region. Finally, in order to minimize mis-alignment between the gate and the drain, sidewall spacer technique using twice is demonstrated for sub-100-nm L_g .

Device characteristics are examined through the electrical measurement test.

Fabricated MOS capacitor shows reasonable leakage current level while EOT is scaled down to ~ 1.8 nm. In addition, thanks to the novel structure, L-shaped TFETs show better performance than conventional ones, in terms of subthreshold characteristic as well as current drivability. However, I_{on} and S_{avg} properties should be further improved to utilize the strengths of TFETs and its real applications. The reduction of EOT below 2 nm without any parasitic capacitance such as trap sites will induce large band-bending and results in high I_{on} and low S_{avg} . In addition, the use of narrow E_g materials for source is also helpful to enhance TFETs performance. As shown in Fig. 5.1, combination of both ideas boosts the I_{on} up to dozens of μA and scales the S_{avg} to ~ 16 mV/dec.

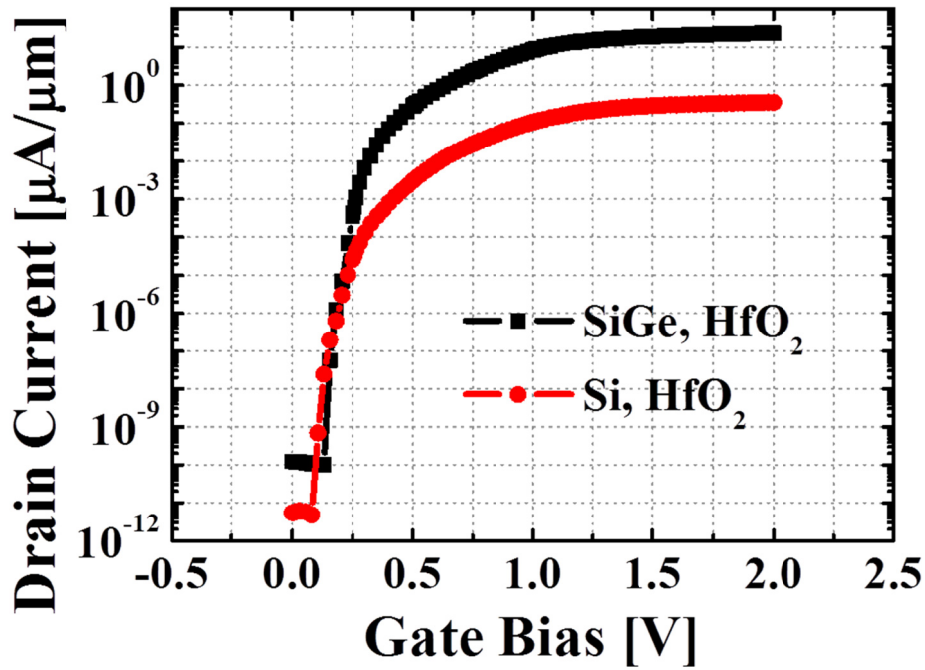


Fig. 5.1. Transfer curves of L-shaped TFETs using Si and SiGe source with HfO₂ gate dielectric. Simulation tool: Synopsys SentaurusTM.

Bibliography

- [1] W. Shockley, “The path to the conception of junction transistor,” *IEEE Trans. Electron Devices*, vol. 23, no. 7, pp. 597-620, Jul. 1976.
- [2] J. S. Kilby, “Turning potential into realities: The invention of the integrated circuit,” Nobel Lecture, pp. 474-485, Dec. 2000.
- [3] M. Bohr, “The new era of scaling in an SoC world,” in *IEEE International Solid-State Circuits Conference (ISSCC 2009)*, 2009, pp. 23-28.
- [4] C.-H. Jan, *et al.*, “A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications,” in *IEDM Tech. Dig.*, 2012, pp.3.1.1-3.1.4.
- [5] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, “I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q ,” in *IEDM Tech. Dig.*, 2002, pp. 289-292.
- [6] H. Kam, D. T. Lee, R. T. Howe, and T.-J. K. Liu, “A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics,” in *IEDM Tech.*

Dig., 2005, pp. 463-466.

- [7] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405-410, Feb. 2008.
- [8] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743-745, Aug. 2007.
- [9] S. M. SZE, and K. K. Ng, *Physics of semiconductor devices 3rd ed.*, Hoboken, NJ: Wiley, 2006, p.422.
- [10] P.-F. Wang, *et al.*, "Complementary tunneling transistor for low power application," *Solid-State Electron.*, vol. 48, no. 12, pp. 2281-2286, Dec. 2004.
- [11] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297-300, Apr. 2006.
- [12] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high- κ gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725-1733, Jul. 2007.
- [13] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: a novel high performance transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013-1019, Apr. 2008.
- [14] A. Chattopadhyay and A. Mallik, "Impact of a spacer dielectric and gate overlap/underlap on the device performance of a tunnel field-effect transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 677-683, Mar. 2011.

- [15] R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Assessment of ambipolar behavior of a tunnel FET and influence of structural modifications," *J. Semicond. Tech. Sci.*, vol. 12, no. 4, pp. 482-291, Dec. 2012.
- [16] H.-Y. Chang, B. Adams, P.-Y. Chien, J. Li, and J. C. S. Woo, "Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing," *IEEE Electron Device Lett.*, vol. 60, no. 1, pp. 92-96, Jan. 2013.
- [17] S. Mookerjee, R. Krishnan, S. Datta, and V. Narayana, "Effective capacitance and drive current for tunnel FET (TFET) CV/I estimation," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2092-2098, Sep. 2009.
- [18] G. Lee, and W. Y. Choi, "Low-power circuit applicability of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs)," *IEICE Trans. on Electron.*, vol. E95-C, no. 5, May, 2012.
- [19] R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Device and circuit level performance comparison of tunnel FET architectures and impact of heterogeneous gate dielectric," *J. Semicond. Tech. Sci.*, vol. 13, no. 3, pp. 224-236, Jun. 2013.
- [20] S. W. Kim, *et al.*, "L-Shaped tunneling field-effect transistors for complementary logic applications," *IEICE Trans. on Electron.*, vol. E96-C, no. 5, pp. 634-638, May. 2013.
- [21] S. W. Kim, W. Y. Choi, M.-C. Sun, H. W. Kim, and B.-G. Park, "Design guideline of Si-based L-shaped tunneling field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 51,

- no. 6, pp. 06FE09-1-06FE09-4, Jun. 2012.
- [22] S. W. Kim, W. Y. Choi, M.-C. Sun, and B.-G. Park, "Investigation on the corner effect of L-shaped tunneling field-effect transistors and their fabrication method," *Journal of Nanoscience and Nanotechnology*, vol. 13, no. 9, pp. 6376-6381, Sep. 2013.
- [23] A. Bowonder, *et al.*, "Low-voltage green transistor using ultra shallow junction and hetero-tunneling," in *Proc. 8th Int. Workshop on Junction Technology (IWJT)*, 2008, pp. 93-96.
- [24] C. Hu, *et al.*, "Prospect of tunneling green transistor for 0.1V CMOS," in *IEDM Tech. Dig.*, 2010, pp. 387-390.
- [25] G. Han, *et al.*, "Source engineering for tunnel field-effect transistor: elevated source with vertical silicon-germanium/germanium heterostructure," *Jpn. J. Appl. Phys.*, vol. 50, pp. 04DJ07-1-04DJ07-2, Apr. 2011.
- [26] R. Asra, K. V. R. M. Murali, and V. R. Rao, "A binary tunnel field effect transistor with a steep sub-threshold swing and increased ON current," *Jpn. J. Appl. Phys.*, vol. 49, pp. 120203-1-120203-3, Dec. 2010.
- [27] Q. Huang, *et al.*, "A novel tunnel FET with 36mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration," in *IEDM Tech. Dig.*, 2012, pp. 187-190.
- [28] Y. Morita, *et al.*, "Synthetic electric field tunnel FETs: drain current multiplication demonstrated by wrapped gate electrode around ultrathin epitaxial channel," in

VLSI Tech. Dig., 2013, pp. T236-T237.

- [29] I. A. Fischer, *et al.*, “Silicon tunneling field-effect transistors with tunneling in line with the gate field,” *IEEE Electron Device Lett.*, vol. 34, no. 2, Feb. 2013.
- [30] Sentaurus Device User Guide, ver. G-2012.06, Synopsys Inc.
- [31] Sentaurus Device User Guide, ver. H-2013.03, Synopsys Inc.
- [32] *Atlas User’s Manual-Device Simulation Software*, SILVACO Inc., Santa Clara, CA, Jul. 2013.
- [33] M.-C. Sun, *et al.*, “Novel tunneling field-effect transistor with sigma-shape embedded SiGe sources and recessed channel,” in *Proc. AWAD*, 2012, pp. 281-282.
- [34] L. Liu, D. Mohata, and S. Datta, “Scaling length theory of double-gate interband tunnel field-effect transistors,” *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902-908, Apr. 2012.
- [35] Th. Nirschl, *et al.*, “Scaling properties of the tunneling field effect transistor (TFET): device and circuit,” *Solid-State Electron.*, vol. 50, no. 1, pp. 44-51, Jan. 2006.
- [36] K. Boucart, and A. M. Ionescu, “Length scaling of the double gate tunnel FET with a high-K gate dielectric,” *Solid-State Electron.*, vol. 51, no. 11-12, pp. 1500-1507, Nov.-Dec. 2007.
- [37] A. C. Seabaugh, and Q. Zhang, “Low-voltage tunnel transistors for beyond CMOS logic,” *Proceedings of The IEEE*, vol. 98, no. 12, pp. 2095-2110, Dec. 2010.
- [38] S. Cho, *et al.*, “Simulation study on scaling limit of silicon tunneling field-effect

- transistor under tunneling-predominance,” *IEICE Electron. Express*, vol. 9, no. 9, pp. 828-833, May 2012.
- [39] M. J. Lee, and W. Y. Choi, “Dependency of tunneling field-effect transistor (TFET) characteristics on operating regions,” *Journal of Semiconductor Technology and Science*, vol. 11, no. 4, pp. 287-294, Dec. 2011.
- [40] J. G. Fossum, J.-W. Yang, and V. P. Trivedi, “Suppression of corner effects in triple-gate MOSFETs,” vol. 24, no. 12, pp. 745-747, Dec. 2003.
- [41] U. E. Avci, R. Rios, K. Kuhn, and I. A. Young, “Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic,” in *VLSI Tech. Dig.*, 2011, pp. 124-125.
- [42] Y. Yang, *et al.*, “Tunneling field-effect transistor: capacitance components and modeling,” *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 752-754, Jul. 2010.
- [43] S. Mookerjea, *et al.*, “On enhanced Miller capacitance effect in interband tunnel transistors,” *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1102-1104, Oct. 2009.
- [44] R. J. Hoekstra, *et al.*, “Microtrenching resulting from specular reflection during chlorine etching of silicon,” *J. Vac. Sci. Technol. B*, vol. 16, no. 4, pp. 2102-2104, Jul.-Aug. 1998.
- [45] K. J. Yang, and C. Hu, “MOS capacitance measurements for high-leakage thin dielectric,” *IEEE Trans. Electron Devices*, vol. 46, no. 7, pp. 1500-1501, Jul. 1999.
- [46] A. Nara, N. Yasuda, H. Satake, and A. Toriumi, “Applicability limits of the two-frequency capacitance measurement technique for the thickness extraction of

- ultrathin gate oxide,” *IEEE Trans. Semi. Manuf.*, vol. 15, no. 2, pp. 209-213, May 2002.
- [47] B.-G. Park, S. W. Hwang, and Y. J. Park, *Nanoelectronic devices*, Singapore: Pan Stanford Publishing, 2012, p. 143.
- [48] A. Mallik, and A. Chattopadhyay, “Drain-dependence of tunnel field-effect transistor characteristics: the role of the channel,” *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4250-4257, Dec. 2011.
- [49] P. L. Castro, and B. E. Deal, “Low-temperature reduction of fast surface states associate with thermally oxidized silicon,” *J. Electrochem. Soc.*, vol. 118, no. 2, pp. 280-286, Feb. 1971.
- [50] V. Singh, S. K. Sharma, D. Kumar, and R. K. Nahar, “Study of rapid thermal annealing on ultra thin high- κ HfO₂ films properties for nano scaled MOSFET technology,” *Microelectronic Engineering*, vol. 91, pp. 137-143, Mar. 2012.
- [51] J. Robertson, “High dielectric constant oxides,” *Eur. Phys. J. Appl. Phys.*, vol. 28, pp. 265-291, Dec. 2004.
- [52] Y. Taur, and T. H. Ning, *Fundamentals of modern VLSI devices 1st ed.*, New York, NY: Cambridge University Press, 1998, p.133.

초 록

상보형 금속-산화물-반도체(CMOS) 축소화 기술의 발달과 늘어나는 단위면적당 전력 소비 문제를 해결하기 위해 L자 형태의 터널링 전계효과 트랜지스터(L-shaped tunnel field-effect transistor, L-shaped TFET)를 제안, 제작하고 그 전기적 특성을 검증해 보았다. 제안한 소자는 밴드간 터널링(band-to-band tunneling)이 게이트(gate)에 의해 형성된 수직방향 전기장과 평행하게 발생한다. 반송자(carrier)가 채널의 방향과 수직으로 주입되기 때문에 터널링 접합의 단면적과 장벽의 폭을 구조적 변수들로 정의할 수 있다.

상용 TCAD 시뮬레이션 연구를 통하여 전기적 특성을 살펴보고 최적화 하였다. 시뮬레이션 결과, L자 형태의 TFET은 문턱전압 이하 기울기의 역수(subthreshold swing, S), 구동 전류, 짧은 채널 효과 측면에서 기존 TFET에 비해 우수한 성능을 보일 것으로 예상되었다. 뿐만 아니라, 기존 TFET과 L자 형태의 TFET으로 구성된 인버터들의 특성을 비교해 보았다.

주요 공정기술을 확보한 이후, 대조군과 비교군을 위한 소자들을 서울대학교 반도체 공동연구소에서 제작하였다. 주요 공정기술은 균일한 도핑 농도를 가지는 소스 영역 형성을 위한 실리콘 에피막 성장과 동시에 불순물 주입을 하는 기술, 터널링 영역을 형성하기 위해 실리콘 에피막을 선택적으로 저온에서 성장하는 기술, 3 nm 이하의 게이트 산화막 확보하는

기술 등을 포함한다.

전기적 측정을 통하여 얻은 전달 특성과 출력 특성에서, 102 mV/dec에 불과하였던 기존 TFET의 최소 S 값이 7, 34, 59 mV/dec으로 향상되는 것을 검증하였다. 뿐만 아니라, 구동 전류 또한 10배 이상 향상 되었다. 소스/드레인 저항, 채널 저항, 이동도, 터널링 저항등 TFET의 주요 파라미터들을 추출하여 성능 향상이 터널링 저항의 감소에 의한 것임을 명백히 확인할 수 있었다.

본 연구를 통해 L자 형태의 TFET이 차세대 저전력 소자의 강력한 후보가 될 수 있음을 검증했다.

주요어: 밴드간 터널링, 터널링 전계효과 트랜지스터, 저전력 소자, L자 형태의 TFET, 문턱전압 이하 기울기, 전류 구동 능력

학 번: 2008-30869

Curriculum Vitae

Personal

Department of Electrical and Computer Engineering,
Bldg. #301, Rm. #1017, Seoul National University,
1 Gwanak-ro, Gwanak-gu,
Seoul 151-744, Korea

Tel.: +82-2-880-7279
Mobile: +82-10-9372-0774
Email: swkim83@snu.ac.kr
Homepage : <http://smdl.snu.ac.kr>
Nationality: Republic of Korea

Education

Ph.D. in Department of Electrical and Computer Engineering

Seoul National University (Seoul, Korea)

Sep. 2008 – Feb. 2014

Research Advisor: Prof. Byung-Gook Park

Thesis: L-shaped Tunnel Field-Effect Transistors (L-shaped TFETs) with High Current Drivability and Low Subthreshold Swing

M.S. in Department of Electrical Engineering and Computer Science

Seoul National University (Seoul, Korea)

Mar. 2006 – Feb. 2008

Research Advisor: Prof. Byung-Gook Park

Thesis: “Investigation of Resistive Probe Used for Writing/Reading in Ferroelectric Material”

B.S. in Electrical Engineering

Seoul National University (Seoul, Korea)

Mar. 2001 – Feb. 2006

Career History and Work Experience

Inter-university Semiconductor Research Center, Seoul National University

(Seoul, Korea)

Research Assistant of Process Integration	Mar. 2010 – present
Research Worker	Mar. 2010 – Aug. 2011
Assistant Teacher of Oxidation & Diffusion	Jul. 2008 – present
Research Worker	Mar. 2008 – Aug. 2008
Assistant Teacher of Nanoscale CMOS Simulation	Jul. 2006 – present

Department of Electronics Engineering, Ewha Womans University

(Seoul, Korea)

Instructor in “Semiconductor Engineering”	Sep. 2010 – Dec. 2010
---	-----------------------

Semiconductor Materials and Devices Lab., Seoul National University

(Seoul, Korea)

Research Assistant,	Prof. Byung-Gook Park’s group	Mar. 2006 – present
---------------------	-------------------------------	---------------------

•Researched on “Ultra Low-Power/Small Nano Device and Reconfigurable 3D Integration System”

- Supported by Ministry of Science, ICT and Future Planning (MSIP) of Korea

Sep. 2013 – present

- Supported by Ministry of Education and Science Technology (MEST) of Korea

Sep. 2011 – Aug. 2013

•Researched on “Technology Development of Post-CMOS Future Semiconductor Devices for Sub-0.7-V Operation Voltage”

- Supported by Ministry of Trade, Industry and Energy (MOTIE) of Korea

Jun. 2013 – present

•Researched on “Tunneling Transistor Technology with Low Power and High Performance”

•Researched on “Low Power Memory and Logic Application Technology Using Tunneling Transistor”

- Researched on “Modeling, Compact Model, and Reliability Technology about Tunneling Transistor”
 - Supported by Consortium of Semiconductor Advanced Research (COSAR) of Korea
Jun. 2013 – present
- Researched on “Tunneling Device Using Schottky Barrier”
 - Supported by Samsung Electronics Co., Ltd. Jun. 2012 – Jun. 2013
 - Supported by Samsung LED Co., Ltd. Jun. 2010 – Jun. 2012
- Researched on “Tunneling Device Using Schottky Barrier”
 - Supported by SK Hynix Co., Ltd. Apr. 2010 – Jun. 2012
- Researched on “Research on a Property of Cutting-Edge Oxide Materials”
 - Supported by Samsung Electronics Co., Ltd. Aug. 2009 – Jul. 2010
- Researched on “Investigation on Novel 1T-Dram Cell”
 - Supported by Samsung Advanced Institute of Technology Jun. 2008 – Dec. 2008
- Researched on “Development of Asymmetric CMOS Device for High Speed/Low Power”
 - Supported by SK Hynix Co., Ltd. Apr. 2008 – Mar. 2010
- Researched on “Fabrication of NMOS Transistor for Realization of FeHDD Read Head”
 - Supported by Samsung Advanced Institute of Technology Mar. 2008 – Jun. 2008
- Researched on “Development of High Performance/Low Power CMOS Device with 3D-Structure”
 - Supported by Ministry of Knowledge Economy Sep. 2008 – Aug. 2009
 - Supported by Ministry of Commerce, Industry and Energy Sep. 2007 – Aug. 2008
- Researched on “Fabrication of 50 nm NMOS Transistor for Realization of FeHDD head”
 - Supported by Samsung Advanced Institute of Technology Apr. 2007 – Jul. 2007
- Researched on “Design a Novel Structure Transistor to Improve the Performance of Resistive Probe”
 - Supported by Samsung Advanced Institute of Technology Mar. 2006 – Oct. 2006
- Researched on “Si-based Electronic Device below 10 nm”
 - Supported by Ministry of Education and Science Technology(MEST) Mar. 2006 – Aug. 2007

Major Achievements

- Development of Nanoscale Tunnel TFETs
- Development of Resistive RAM Technology
- Development of Planar and 3D Non-Volatile Memory Technology
- Development of Thin Film Transistor (TFT) Technology
- Development of Capacitor less 1T DRAM Cell Technology
- Development of Carbon Nano Tube (CNT) based FETs
- Development of Nanoscale SiNW GAA MOSFETs
- Development of Nanoscale FinFETs
- Development of Nanoscale Planar and 3D MOSFETs
- Development of Nanoscale Asymmetric MOSFETs for High Performance CMOS Device
- Development of Resistive Probe Sensor for FeHDD Head with Ferroelectric Materials

Awards and Honors

- Best Paper Award
 - SMDL, Seoul National Univ., supported by Silvaco Korea Feb. 2012
- Scholarship for Outstanding User in Process Equipment
 - Inter-university Semiconductor Research Center, Seoul National Univ. Sep. 2013

Research Interests

Design, fabrication, characterization and theoretical analysis of nanoscale CMOS and novel devices (including TFETs), SiGe (strained Si) technology, Ge MOSFETs, multiple-gate MOSFETs, 3-D stack technology, high-k dielectric technology, non-volatile memory (NVM) such as RRAM, charge trap flash (CTF), thin film transistor (TFT), light emitting diode (LED), neuromorphic system

List of Publications

International Journal

- [1] Min-Chul Sun, Garam Kim, Jung Han Lee, Hyungjin Kim, **Sang Wan Kim**, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Patterning of Si nanowire array with electron beam lithography for sub-22 nm Si nanoelectronics technology," *Microelectronic Engineering*, Vol. 110, No. , pp. 141-146, Oct. 2013. [SCI]
- [2] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, and Byung-Gook Park, "Investigation on the corner effect of L-shaped tunneling field-effect transistors and their fabrication method," *Journal of Nanoscience and Nanotechnology*, Vol. 13, No. 9, pp. 6376-6381, Sep. 2013. [SCI]
- [3] Min-Chul Sun, **Sang Wan Kim**, Hyun Woo Kim, Hyungjin Kim, and Byung-Gook Park, "Complementary-metal-oxide-semiconductor technology-compatible tunneling field-effect transistors with 14nm gate, sigma-shape source, and recessed channel," *Japanese Journal of Applied Physics: Regular Papers*, Vol. 52, No. 6, pp. 06GE06-1-06GE06-5, Jun. 2013. [SCI]
- [4] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "L-Shaped tunneling field-effect transistors for complementary logic applications," *IEICE Transactions on Electronics*, Vol. E96-C, No. 5, pp. 634-638, May. 2013. [SCIE]
- [5] Min-Chul Sun, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Hyungjin Kim, and Byung-Gook Park, "Novel tunneling field-effect transistor with sigma-shape embedded SiGe sources and recessed channel," *IEICE Transactions on Electronics*, Vol. E96-C, No. 5, pp. 639-643, May. 2013. [SCIE]
- [6] Hyun Woo Kim, Jang Hyun Kim, **Sang Wan Kim**, Min-Chul Sun, Garam Kim, Euyhwan Park, Hyungjin Kim, Kyung Wan Kim, and Byung-Gook Park, "A novel fabrication method for the nanoscale tunneling field effect transistor," *Journal of Nanoscience and Nanotechnology*, Vol. 12, No. 5, pp. 5592-5597, Jul. 2012. [SCI]
- [7] Min-Chul Sun, Garam Kim, **Sang Wan Kim**, Hyun Woo Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Co-Integration of nano-scale vertical- and horizontal-channel metal-oxide-semiconductor field-effect transistors for low power CMOS technology," *Journal of Nanoscience and Nanotechnology*, Vol. 12, No. 7, pp. 5313-5317, Jul. 2012. [SCI]
- [8] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Design guideline of Si-based L-shaped tunneling field-effect transistors," *Japanese Journal of Applied Physics: Regular Papers*, Vol. 51, No. 6, pp. 06FE09-1-06FE09-4, Jun. 2012. [SCI]
- [9] Min-Chul Sun, Hyun Woo Kim, **Sang Wan Kim**, Garam Kim, Hyungjin Kim, and Byung-Gook Park, "Comparative study on top- and bottom-source vertical-channel tunnel field-effect transistors," *IEICE Transactions on Electronics*, Vol. E95-C, No. 5, pp. 826-830, May. 2012. [SCIE]
- [10] Hyungjin Kim, Min-Chul Sun, Hyun Woo Kim, **Sang Wan Kim**, Garam Kim, and Byung-Gook Park, "Study on threshold voltage control of tunnel field-effect transistors using V_T -control doping region," *IEICE Transactions on Electronics*, Vol. E95-C, No. 5, pp. 820-825, May. 2012. [SCIE]
- [11] Min-Chul Sun, **Sang Wan Kim**, Hyun Woo Kim, Garam Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Design of thin-body double-gated vertical-channel tunneling field-effect transistors for ultralow-power logic circuits," *Japanese Journal of Applied Physics: Regular Papers*, Vol. 51, No. 4, pp. 04DC03-1-04DC03-5, Apr. 2012. [SCI]
- [12] Garam Kim, **Sang Wan Kim**, Kyung-Chang Ryoo, Jeong-Hoon Oh, Min-Chul Sun, Hyun Woo Kim, Dae Woong Kwon, Jisoo Chang, Sunghun Jung, and Byung-Gook Park, "Split-gate-structure 1T1R1C DRAM for retention characteristic improvement," *Journal of Nanoscience*

- and Nanotechnology, Vol. 11, No. 7, pp. 5603-5607, Jul. 2011. [SCI]
- [13] Jang Hyun Kim, Dae Woong Kwon, Jisoo Chang, **Sang Wan Kim**, Jae Chul Park, Chang Jung Kim, and Byung-Gook Park, "Investigation on the characteristics of stress-induced hump in amorphous oxide thin film transistors," *Applied Physics Letters*, Vol. 99, No. 7, pp. 043502-1-043502-3, Jul. 2011. [SCI]
 - [14] Dae Woong Kwon, Jang Hyun Kim, Jisoo Chang, **Sang Wan Kim**, Wandong Kim, Jae Chul Park, Chang Jung Kim, and Byung-Gook Park, "Light effect on negative bias-induced instability of HfInZnO amorphous oxide thin-film transistor," *IEEE Transactions on Electron Devices*, Vol. 58, No. 4, pp. 1127-1133, Apr. 2011. [SCI]
 - [15] Dae Woong Kwon, Jang Hyun Kim, Jisoo Chang, **Sang Wan Kim**, Wandong Kim, Jae Chul Park, Ihun Song, Chang Jung Kim, U In Jung, and Byung-Gook Park, "Temperature effect on negative bias-induced instability of HfInZnO amorphous oxide thin film transistor," *Applied Physics Letters*, Vol. 98, No. 6, pp. 635021-635023, Feb. 2011. [SCI]
 - [16] Seongjae Cho, Shinichi O'uchi, Kazuhiko Endo, **Sang Wan Kim**, Younghwan Son, In Man Kang, Meishoku Masahara, James S. Harris Jr., and Byung-Gook Park, "Rigorous design of 22-nm node 4-terminal SOI FinFETs for reliable low standby power operation with semi-empirical parameters," *Journal of Semiconductor Technology and Science*, Vol. 10, No. 4, pp. 265-275, Dec. 2010. [SCIE]
 - [17] Dae Woong Kwon, Jang Hyun Kim, Jisoo Chang, **Sang Wan Kim**, Min-Chul Sun, Garam Kim, Hyun Woo Kim, Jae Chul Park, Ihun Song, Chang Jung Kim, U In Jung, and Byung-Gook Park, "Charge injection from gate electrode by simultaneous stress of optical and electrical biases in HfInZnO amorphous oxide thin film transistor," *Applied Physics Letters*, Vol. 97, No. 19, pp. 1935041-1935043, Nov. 2010. [SCI]
 - [18] Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jeong-Hoon Oh, Kyung-Chang Ryoo, Min-Chul Sun, Garam Kim, Jang-Gn Yun, Hyungcheol Shin, and Byung-Gook Park, "Fin and recess-channel metal oxide semiconductor field effect transistor for sub-50nm dynamic random access memory cell," *Japanese Journal of Applied Physics: Regular Papers*, Vol. 49, No. 10, pp. 1042021-1042025, Oct. 2010. [SCI]
 - [19] Jae Hyun Park, Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jang-Gn Yun, and Byung-Gook Park, "Fabrication of highly scaled silicon nanowire gate-all-around metal-oxide-semiconductor field effect transistors by using self-aligned local-channel V-gate by optical lithography process," *Japanese Journal of Applied Physics: Regular Papers*, Vol. 49, No. 8, pp. 842031-842035, Aug. 2010. [SCI]
 - [20] Jong Pil Kim, Jae Young Song, **Sang Wan Kim**, Jae Hyun Park, Woo Young Choi, Jong Duk Lee, Hyungcheol Shin, and Byung-Gook Park, "Self-aligned asymmetric metal-oxide-semiconductor field effect transistors fabricated on silicon-on-insulator," *Japanese Journal of Applied Physics*, vol. 48, no. 9, pp. 091201, Sep. 24, 2009. [SCI]
 - [21] Jong Pil Kim, Woo Young Choi, Jae Young Song, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Design and fabrication of asymmetric MOSFETs using a novel self-aligned structure," *IEEE Transactions on Electron Devices*, vol. 54, no. 11, pp. 2969-2974, November 2007. [SCI]
 - [22] Jong Pil Kim, Woo Young Choi, Jae Young Song, Seongjae Cho, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Design and simulation of asymmetric MOSFETs," *IEICE Trans. Electron.*, vol. E90-C, pp. 978-982, May 2007. [SCI]
 - [23] Jae Young Song, Woo Young Choi, Jong Pil Kim, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Novel gate-all-around metal-oxide-semiconductor field effect transistors with self-aligned structure," *Japanese Journal of Applied Physics*, vol. 46, no. 4B, pp. 2046-2049, April 2007. [SCI]

Domestic Journal

- [1] **Sang Wan Kim**, Chang-Su Seo, Yu-Kyung Park, Sang-Yeop Jee, Yun-Bin Kim, Suk-Jin Jung, Min-Kyu Jeong, Jong-Ho Lee, Hyungcheol Shin, Byung-Gook Park, and Cheol Seong Hwang, "The optimization of 0.5 μm SONOS flash memory with polycrystalline silicon thin film transistor," *Journal of The Institute of Electronics Engineers of Korea*, Vol. 49, No. 10, pp. 496-506, Oct. 2012.

International Conference

- [1] Hyun Woo Kim, **Sang Wan Kim**, Min-Chul Sun, Jang Hyun Kim, Euyhwan Park, and Byung-Gook Park, "Tunneling field-effect transistor with Si/SiGe material for high current drivability," *International Microprocesses and Nanotechnology Conference (MNC)*, Sapporo, Japan, p. 8P-11-37, Nov. 5-8, 2013.
- [2] Byung-Gook Park, Min-Chul Sun, and **Sang Wan Kim**, "Silicon-based tunneling field effect transistors for ultra-low power applications," *Asia Pacific Physics Conference*, Chiba, Japan, p. A2-2-I2, Jul. 14-19, 2013.
- [3] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Threshold voltage adjustment method of tunneling field-effect transistors," *International Conference on Electronics, Information and Communication (ICEIC)*, Bali, Indonesia, pp. 247-248, Jan. 30-Feb. 2, 2013.
- [4] Hyun Woo Kim, Min-Chul Sun, **Sang Wan Kim**, and Byung-Gook Park, "Hump phenomenon in transfer characteristics of double-gated thin-body tunneling field-effect transistor (TFET) with Gate/Source overlap," *IEEE International NanoElectronics Conference (INEC)*, Singapore, pp. 386-388, Jan. 2-4, 2013.
- [5] Min-Chul Sun, Hyun Woo Kim, **Sang Wan Kim**, Jung Han Lee, Hyungjin Kim, and Byung-Gook Park, "Threshold voltage of nanoscale Si gate-all-around MOSFET: short-channel, quantum, and volume effects," *IEEE International NanoElectronics Conference (INEC)*, Singapore, pp. 27-29, Jan. 2-4, 2013.
- [6] Min-Chul Sun, **Sang Wan Kim**, Hyun Woo Kim, Hyungjin Kim, and Byung-Gook Park, "CMOS-compatible tunnel FETs with 14 nm gate, sigma-shape source, and recessed channel," *International Microprocesses and Nanotechnology Conference (MNC)*, Sapporo, Japan, pp. 1P-7-34-, Nov. 4-7, 2012.
- [7] Hyun Woo Kim, Min-Chul Sun, **Sang Wan Kim**, Joo Yun Seo, Garam Kim, Jang Hyun Kim, and Byung-Gook Park, "Investigation on effects of changing body doping concentration in short-channel junctionless transistor," *International Microprocesses and Nanotechnology Conference (MNC)*, Sapporo, Japan, pp. 1P-7-41-, Nov. 4-7, 2012.
- [8] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Design improvement of L-shaped tunneling field-effect transistors," *IEEE International SOI Conference*, Napa, CA, USA, pp. 4.1-, Oct. 1-4, 2012.
- [9] Min-Chul Sun, Garam Kim, Jung Han Lee, Hyungjin Kim, **Sang Wan Kim**, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Patterning of Si nanowire array with electron beam lithography for sub-22nm Si nanoelectronics technology," *International Conference on Micro- and Nano-Engineering (MNE)*, Toulouse, France, pp. 281-282, Sep. 16-20, 2012.
- [10] **Sang Wan Kim**, Woo Young Choi, Won Bo Shim, Hyungjin Kim, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Study on the ambipolar behavior depending on the length of gate-drain overlap," *International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC)*, Sapporo, Japan, pp. P-T3-09-, Jul. 15-18, 2012.

- [11] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Investigation and optimization of the n-channel and p-channel L-shaped tunneling field-effect transistors," *Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD)*, Okinawa, Japan, pp. 36-37, Jun. 27-29, 2012.
- [12] Min-Chul Sun, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Novel tunneling field-effect transistor with sigma-shape embedded SiGe sources and recessed channel," *Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD)*, Okinawa, Japan, pp. 281-282, Jun. 27-29, 2012.
- [13] **Sang Wan Kim**, Woo Young Choi, Hyungjin Kim, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Investigation on hump effects of L-shaped tunneling field-effect transistors," *Silicon Nanoelectronics Workshop (SNW)*, Honolulu, HI, USA, pp. 169-170, Jun. 10-11, 2012.
- [14] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Ambipolar behavior of L-shaped tunneling field-effect transistors," *International Conference on Electronics, Information and Communication (ICEIC)*, Jeongseon, Korea, pp. 285-286, Feb. 1-3, 2012.
- [15] Hyungjin Kim, **Sang Wan Kim**, Min-Chul Sun, Hyun Woo Kim, Garam Kim, Jang Hyun Kim, Euyhwan Park, and Byung-Gook Park, "Enhanced ambipolar characteristic of tunneling field-effect transistors using doped region," *International Conference on Electronics, Information and Communication (ICEIC)*, Jeongseon, Korea, pp. 279-280, Feb. 1-3, 2012.
- [16] Min-Chul Sun, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Modulation of transfer characteristics of Si nanowire tunnel FET on ultra-thin-body and BOX (UTBB) SOI substrate using back-gate bias," *International Semiconductor Device Research Symposium (ISDRS)*, College Park, MD, USA, pp. 1-2, Dec. 7-9, 2011.
- [17] Garam Kim, Min-Chul Sun, **Sang Wan Kim**, Hyun Woo Kim, Jang Hyun Kim, Euyhwan Park, Hyungjin Kim, and Byung-Gook Park, "Novel MOSFET structure using p-n junction gate for ultra-low subthreshold-swing," *International Semiconductor Device Research Symposium (ISDRS)*, College Park, MD, USA, pp. 1-2, Dec. 7-9, 2011.
- [18] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "L-Shaped tunneling field-effect transistors (TFETs) for low subthreshold swing and high current drivability," *International Microprocesses and Nanotechnology Conference (MNC)*, Kyoto, Japan, pp. 26C-4-5L-26C-4-5L, Oct. 24-27, 2011.
- [19] Min-Chul Sun, **Sang Wan Kim**, Hyun Woo Kim, Garam Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Design of thin-body double-gated vertical-channel tunneling field-effect transistors for ultra-low power logic circuits," *International Conference on Solid State Devices and Materials (SSDM)*, Nagoya, Japan, pp. 845-846, Sep. 28-30, 2011.
- [20] Garam Kim, **Sang Wan Kim**, Min-Chul Sun, Hyun Woo Kim, Hyungjin Kim, and Byung-Gook Park, "Tunneling field effect transistor with sidewall floating gate for ultra-low subthreshold swing," *International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC)*, Gyeongju, Korea, pp. 306-307, Jun. 19-22, 2011.
- [21] Min-Chul Sun, Hyun Woo Kim, **Sang Wan Kim**, Garam Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Comparative study on top- and bottom-source vertical-channel tunnel field-effect transistors," *Asia-Pacific Workshop on Fundamental and Application of Advanced Semiconductor Devices (AWAD)*, Daejeon, Korea, pp. 87-89, Jun. 29-Jul. 1, 2011.
- [22] Hyungjin Kim, Min-Chul Sun, Hyun Woo Kim, **Sang Wan Kim**, Garam Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Threshold voltage control of tunnel field-effect transistors using V_T -control doping region," *Asia-Pacific Workshop on Fundamental and Application of Advanced Semiconductor Devices (AWAD)*, Daejeon, Korea, pp. 90-92, Jun. 29-Jul. 1, 2011.
- [23] Min-Chul Sun, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol

- Shin, and Byung-Gook Park, "Scalable embedded Ge-junction vertical-channel tunneling field-effect transistor for low-voltage operation," *IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Monterey, CA, USA, pp. 286-290, Oct. 12-15, 2010.
- [24] Jisoo Chang, **Sang Wan Kim**, Dae Woong Kwon, Jang Hyun Kim, Jae Chul Park, Ihun Song, U-In Jung, Chang Jung Kim, and Byung-Gook Park, "Investigation of bias temperature instability in HfInZnO thin film transistor," *International Conference on Solid State Devices and Materials (SSDM)*, Tokyo, Japan, pp. 379-380, Sep. 22-24, 2010.
- [25] Min-Chul Sun, Wandong Kim, Jeong-Hoon Oh, Kyung-Chang Ryoo, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Sunghun Jung, Dae Woong Kwon, Jisoo Chang, Jang Hyun Kim, and Byung-Gook Park, "Influence of sidewall thickness variation on transfer characteristics of L-shaped impact-ionization MOS transistor," *IEEE NANO*, Seoul, Korea, pp. 250-253, Aug. 17-20, 2010.
- [26] **Sang Wan Kim**, Garam Kim, Won Bo Shim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Simulation of retention characteristics in a double-gate and recessed-channel 1T DRAM cell with high reliability," *International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC)*, Pattaya, Thailand, pp. 905-906, Jul. 4-7, 2010.
- [27] Jang-Gn Yun, Dae Woong Kwon, **Sang Wan Kim**, Jong-Ho Lee, Hyungcheol Shin, Jong Duk Lee, and Byung-Gook Park, "Dumbbell-shaped nanowire with body contact region for three dimensional (3D) NAND flash memory application," *International Conference on Electronics, Information and Communication (ICEIC)*, Cebu, Philippines, pp. 5-7, Jun. 30-Jul. 2, 2010.
- [28] Kyung-Chang Ryoo, Jeong-Hoon Oh, Sunghun Jung, **Sang Wan Kim**, Min-Chul Sun, Garam Kim, Hyun Woo Kim, Dae Woong Kwon, Jisoo Chang, Jang Hyun Kim, Hongsik Jeong, and Byung-Gook Park, "Relationships of resistive switching parameters of resistive random access memory (RRAM) for high density and low power application," *International Conference on Electronics, Information and Communication (ICEIC)*, Cebu, Philippines, pp. 11-13, Jun. 30-Jul. 2, 2010.
- [29] **Sang Wan Kim**, Garam Kim, Wonjoo Kim, Hyoungsoo Ko, and Byung-Gook Park, "Investigation of 1T DRAM cell with non-overlap structure and recessed channel," *Silicon Nanoelectronics Workshop (SNW)*, Honolulu, HI, USA, pp. 139-140, Jun. 13-14, 2010.
- [30] Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jeong-Hoon Oh, Kyung-Chang Ryoo, Min-Chul Sun, Garam Kim, Hyun Woo Kim, Jisoo Chang, Sunghun Jung, Hyungcheol Shin, and Byung-Gook Park, "Fabrication and characterization of buried-gate fin and recess channel MOSFET for high performance and low GIDL current," *International Semiconductor Device Research Symposium (ISDRS)*, College Park, MD, USA, Dec. 9-11, 2009.
- [31] Seongjae Cho, **Sang Wan Kim**, Kazuhiko Endo, Shinichi O'uchi, Takashi Matsukawa, Younghwan Son, Jong Pil Kim, Kunihiro Sakamoto, Yongxun Liu, Byung-Gook Park and Meishoku Masahara, "Rigorous design of 20 nm level SOI 4-T FinFETs for low standby power by extracting parameters from the pre-stage 50 nm technology node devices," *Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials (SSDM)*, Sendai, Japan, pp. 380-381, Oct. 7-9, 2009.
- [32] Jae Hyun Park, Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jeong-Hoon Oh, Kyung-Chang Ryoo, Garam Kim, Hyun Woo Kim, and Byung-Gook Park, "Fabrication and analysis of the gate-all-around (GAA) structure silicon nanowire MOSFET," *IEEE Silicon Nanoelectronics Workshop (SNW)*, Kyoto, Japan, pp. 13-14, Jun. 13-14, 2009.
- [33] Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jeong-Hoon Oh, Kyung-Chang Ryoo, Jae Hyun Park, Garam Kim, Hyun Woo Kim, Atteq Ur Rehman, Jong Duk Lee, Hyungcheol Shin, and Byung-Gook Park, "Buried-gate fin and recess channel MOSFET for sub-30 nm DRAM cell transistors with high performance and low GIDL current," *IEEE Silicon Nanoelectronics Workshop (SNW)*, Kyoto, Japan, pp. 51-52, Jun. 13-14, 2009.
- [34] Garam Kim, **Sang Wan Kim**, Jae Young Song, Jong Pil Kim, Kyung-Chang Ryoo, Jeong-Hoon Oh, Jae Hyun Park, Hyun Woo Kim and Byung-Gook Park, "Body-raised double-gate structure for 1T DRAM," *IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Traverse City, MI, USA, pp. 259-263, Jun. 2-5, 2009.

- [35] Jae Young Song, Jong Pil Kim, Sang Wan Kim, Jae Hyun Park, Garam Kim, Jong Duk Lee and Byung-Gook Park, "Design consideration for source/drain and LDD junction of FiReFET," *The 2nd IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Kyoto, Japan, pp.150, Oct. 20-22, 2008.
- [36] Jong Pil Kim, Jae Young Song, **Sang Wan Kim**, Han Ki Chung, Jae Hyun Park, Hee Sauk Jhon, Garam Kim, Hyungcheol Shin, Jong Duk Lee and Byung-Gook Park, "High performance RF characteristics of asymmetric MOSFETs," *The 2nd IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Kyoto, Japan, p.56, Oct. 20-22, 2008.
- [37] Han Ki Chung, Hoon Jeong, Yeun Seung Lee, Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jae Hyun Park, Jong Duk Lee, Hyungcheol Shin, and Byung-Gook Park, "A capacitor-less 1T-DRAM cell with vertical surrounding gates using gate-induced drain-leakage (GIDL) current," *IEEE Silicon Nanoelectronics Workshop (SNW)*, Honolulu, HI, USA, M0345, Jun. 15-16, 2008.
- [38] **Sang Wan Kim**, Jae Young Song, Jong Pil Kim, Woo Young Choi, Han Ki Chung, Jae Hyun Park, Hyoungsoo Ko, Seungbum Hong, Hongsik Park, Chulmin Park, Jong Duk Lee, Hyungcheol Shin, and Byung-Gook Park, "Investigation of resistive probes with high sensitivity," *IEEE Silicon Nanoelectronics Workshop (SNW)*, Honolulu, HI, USA, P2-15, Jun. 15-16, 2008.
- [39] Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Han Ki Jung, Jae Hyun Park, Jong Duk Lee, and Byung-Gook Park, "Fin and recess channel MOSFET (FiReFET) for performance enhancement of sub-50 nm DRAM cell," *International Semiconductor Device Research Symposium (ISDRS)*, College Park, MD, USA, Dec. 12-14, 2007.
- [40] Jong Pil Kim, Jae Young Song, **Sang Wan Kim**, Woo Young Choi, Jong Duk Lee, and Byung-Gook Park, "30-nm asymmetric NMOSFET using a novel fabrication method," *IEEE Silicon Nanoelectronics Workshop (SNW)*, Kyoto, Japan, pp. 89-90, Jun. 10-11, 2007.
- [41] **Sang Wan Kim**, Woo Young Choi, Jae Young Song, Jong Pil Kim, Junsoo Kim, Hyoungsoo Ko, Hongsik Park, Chulmin Park, Seungbum Hong, Sung-Hoon Choa, Jong Duk Lee, Hyungcheol Shin and Byung-Gook Park, "Analysis and modeling of resistive probes," *IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Gyeongju, Korea, pp. 318-319, Oct. 22-25, 2006.
- [42] Woo Young Choi, Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Breakdown voltage reduction in I-MOS devices," *IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Gyeongju, Korea, pp. 380-381, Oct. 22-25, 2006.
- [43] Jong Pil Kim, Woo Young Choi, Jae Young Song, Seongjae Cho, Sangwoo Kang, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Design and simulation of asymmetric MOSFETs," *Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD)*, Sendai, Japan, pp. 175-178, Jul. 3-5, 2006.
- [44] Jae Young Song, Woo Young Choi, Jong Pil Kim, **Sang Wan Kim**, Doo-Hyun Kim, Jin Ho Kim, Dong-Wook Park, Jong Duk Lee, and Byung-Gook Park, "Effects on multi-fin on self-aligned gate-all-around MOSFETs," *International Conference on Electronics, Information and Communication (ICEIC)*, Ulaanbaatar, Mongolia, pp. 21-24, Jun. 27-28, 2006.

Domestic Conference

- [1] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, and Byung-Gook Park, "Study on the corner effect of L-shaped tunneling field-effect transistors," *NANO Korea*, Seoul, Korea, p. O1201_010, Aug. 16-18, 2012.
- [2] Euyhwan Park, Garam Kim, Jang Hyun Kim, **Sang Wan Kim**, Joong-Kon Son, Donghoon Kang, and Byung-Gook Park, "Analysis of cathodoluminescence image using ITO wet-etch process in GaN-based light-emitting diodes (LEDs)," *IEEK Summer Conference*, Jeju, Korea, pp. 77-78, Jun. 27-29, 2012.

- [3] **Sang Wan Kim**, Woo Young Choi, Min-Chul Sun, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Investigation on the effects of tunneling barrier width on tunneling field effect transistors (TFETs) performance," *IEEK Summer Conference*, Jeju, Korea, pp. 138-141, Jun. 27-29, 2012
- [4] Min-Chul Sun, Hyungjin Kim, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Ground-plane doping for V_T -modulation of planar tunnel field-effect transistors on ultra-thin-body and BOX (UTBB) SOI substrate," *Korean Conference on Semiconductors (KCS)*, Seoul, Korea, pp. 123-124, Feb. 15-17, 2012.
- [5] Hyun Woo Kim, Hyungjin Kim, **Sang Wan Kim**, Min-Chul Sun, Garam Kim, Euyhwan Park, Jang Hyun Kim, and Byung-Gook Park, "A novel fabrication method for nanoscale tunneling field-effect transistor," *NANO Korea*, Seoul, Korea, p. O1102_006, Aug. 24-26, 2011.
- [6] Min-Chul Sun, Garam Kim, **Sang Wan Kim**, Hyun Woo Kim, Hyungjin Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Co-integration of nano-scale vertical- and horizontal-channel MOSFETs for low power CMOS technology," *NANO Korea*, Seoul, Korea, p. O1101_010, Aug. 24-26, 2011.
- [7] Garam Kim, Jang Hyun Kim, Euyhwan Park, Joong-Kon Son, Daeyoung Woo, **Sang Wan Kim**, Min-Chul Sun, Hyun Woo Kim, and Byung-Gook Park, "Optical and electrical degradation of GaN LED by thermal stress," *NANO Korea*, Seoul, Korea, p. P1101_178, Aug. 24-26, 2011.
- [8] Euyhwan Park, Garam Kim, Jang Hyun Kim, **Sang Wan Kim**, Joong-Kon Son, Daeyoung Woo, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Analysis of current saturation delay in GaN-based light-emitting diodes (LEDs)," *IEEK Summer Conference*, Jeju, Korea, pp. 461-462, Jun. 22-24, 2011.
- [9] Hyun Woo Kim, **Sang Wan Kim**, Min-Chul Sun, Garam Kim, Dae Woong Kwon, Jisoo Chang, Jang Hyun Kim, Euyhwan Park, and Byung-Gook Park, "Fabrication method to reduce ambipolar effects in tunneling field-effect transistors," *IEEK Fall Conference*, Seoul, Korea, pp. 46-47, Nov. 23, 2010.
- [10] Garam Kim, **Sang Wan Kim**, Kyung-Chang Ryoo, Jeong-Hoon Oh, Min-Chul Sun, Hyun Woo Kim, Dae Woong Kwon, Jisoo Chang, Sunghun Jung, Jang Hyun Kim, and Byung-Gook Park, "Split gate structure 1T DRAM for improving retention characteristics," *NANO Korea*, Goyang, Korea, p. 1034, Aug. 17-20, 2010.
- [11] **Sang Wan Kim**, Garam Kim, Won Bo Shim, Min-Chul Sun, Hyun Woo Kim, Dae Woong Kwon, Jisoo Chang, Jang Hyun Kim, Euyhwan Park, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "1T DRAM cell with twin gates and recessed channel," *IEEK Summer Conference*, Jeju, Korea, pp. 723-724, Jun. 16-18, 2010.
- [12] Min-Chul Sun, **Sang Wan Kim**, Garam Kim, Hyun Woo Kim, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park, "Short-channel characteristics of tunneling field-effect transistor and operation of vertical-channel tunneling field-effect transistor," *IEEK Summer Conference*, Jeju, Korea, pp. 727-729, Jun. 16-18, 2010.
- [13] Seongjae Cho, **Sang Wan Kim**, Younghwan Son, Il Han Lark, Jong Pil Kim, Hyungcheol Shin, and Byung-Gook Park, "The extraction of effective junction area and carrier lifetimes of PN-junctions with unknown geometry from capacitance measurements," *IEEK Summer Conference*, Jeju, Korea, pp. 399-400, Jul. 8-10, 2009.
- [14] Garam Kim, **Sang Wan Kim**, Jae Young Song, Jong Pil Kim, Jeong-Hoon Oh, Kyung-Chang Ryoo, Hyun Woo Kim, Atteq-ur-Rehman, and Byung-Gook Park, "Optimization of block refresh (autonomous refresh) method for 1T DRAM," *IEEK Summer conference*, Jeju, Korea, pp. 385-386, Jul. 8-10, 2009.
- [15] Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Han Ki Jung, Jae Hyun Park, Hyungcheol Shin, Jong Duk Lee, and Byung-Gook Park, "Fin and recess channel MOSFET (FiReFET) for high performance DRAM cell," *Korean Conference on Semiconductors*, Pyeongchang, Korea, pp. 427-428, Feb. 20-22, 2008.
- [16] Jong Pil Kim, Jae Young Song, **Sang Wan Kim**, Han Ki Jung, Jae Hyun Park, Hee Sauk Jhon, Yeonam Yoon, Hyungcheol Shin, Jong Duk Lee, and Byung-Gook Park "RF performance of 50-nm self-aligned asymmetric MOSFET," *Korean Conference on*

- Semiconductors*, Pyeongchang, Korea, pp. 633-634, Feb. 20-22, 2008.
- [17] Woo Young Choi, Jae Young Song, Jong Pil Kim, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Reduction of breakdown voltage in I-MOS devices," *IEEK Summer conference*, Jeju, Korea pp. 593-594, Jun. 21-23, 2006.
 - [18] Jong Pil Kim, Jae Young Song, Woo Young Choi, **Sang Wan Kim**, Jong Duk Lee, and Byung-Gook Park, "Design and Simulation of Asymmetric MOSFETs," *IEEK Summer conference*, Jeju, Korea, pp. 577-578, Jun. 21-23, 2006.

Patents

- [1] Byung-Gook Park, Dae Woong Kwon, Jisoo Chang, Jang Hyun Kim, **Sang Wan Kim**, "Fabrication method of thin film transistor with rounded gate,"
Korean patent filed 10-2011-0015243, February 21, 2011
Korean patent No. 10-1195544, October 23, 2012
- [2] Byung-Gook Park and **Sang Wan Kim**, "1T DRAM device having two gates on recessed body and method of operating and fabricating the same,"
Korean patent filed 10-2010-0056615, June 15, 2010
Korean Patent No. 10-1163711, July 2, 2012
- [3] Byung-Gook Park and **Sang Wan Kim**, "Transistor using CNT for gate and fabrication method thereof,"
Korean patent filed 10-2010-0073924, July 30, 2010
Korean Patent No. 10-1160585, June 21, 2012
- [4] Byung-Gook Park, **Sang Wan Kim**, and Woo Young Choi, "Tunneling field effect transistor having FinFET structure of independent dual gates and fabrication method thereof,"
Korean patent filed 10-2012-0052537, May 17, 2012
Korean Patent No. 10-1286707, July 10, 2013
- [5] Byung-Gook Park, Dae Woong Kwon, Jang Hyun Kim, Jisoo Chang, **Sang Wan Kim**, "Two bit RRAM using inverted staggered thin transistor structure,"
Korean patent filed 10-2011-0015241, February 21, 2011
Korean Patent No. 10-1113885, February 1, 2012
- [6] Byung-Gook Park, Dae Woong Kwon, Jae Chul Park, **Sang Wan Kim**, Jang Hyun Kim, Jisoo Chang, "Transistors and electronic devices including the same,"
Korean patent filed 10-2010-0099542, October 12, 2010
United States patent filed 13/096314, April 28, 2011
- [7] Hyoung Soo Ko, Byung Gook Park, Seung Bum Hong, Chul Min Park, Woo Young Choi, Jong Pil Kim, Jae Young Song, **Sang Wan Kim**, "Semiconductor probe structure using impact-ionization metal oxide semiconductor device, information storing device therewith and manufacturing method thereof,"
Korean Patent filed 10-2007-0004973, January 16, 2007
Korean Patent No. 10-0804738-0000, February 12, 2008
United States Patent No. 7915109, Mar. 29, 2011
- [8] Hyoung Soo Ko, Byung-Gook Park, Seung Bum Hong, Chul Min Park, Woo Young Choi, Jong Pil Kim, Jae Young Song, **Sang Wan Kim**, "Method of manufacturing enhancement type semiconductor probe and information storage device having the semiconductor probe using the same,"
Korean Patent filed 10-2007-0022550, March 7, 2007
Korean Patent No. 10-0842923-0000, June 25, 2008
United States patent No. 7700393, April 20, 2010