PH.D. DISSERTATION

A PROCESS VARIATION TOLERANT ON-CHIP CMOS THERMOMETER FOR AUTO TEMPERATURE COMPENSATED SELF-REFRESH OF LOW-POWER MOBILE DRAM

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A Process-Variation-Tolerant On-Chip CMOS Thermometer for Auto Temperature Compensated Self-Refresh of Low-Power Mobile DRAM

By

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ABSTRACT

A PROCESS VARIATION TOLERANT ON-CHIP CMOS THERMOMETER FOR AUTO TEMPERATURE COMPENSATED SELF-REFRESH OF LOW-POWER MOBILE DRAM

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Smaller transistors mean that capacitors are charged less uniformly, which increases the self-refresh current in the DRAMs used in mobile devices. Adaptive self-refresh using an on-chip thermometer can solve this problem. In this thesis, a PVT tolerant on-chip CMOS thermometer specifically designed for controlling the refresh period of a DRAM will be proposed for low power mobile DRAM. Two types of on-chip CMOS thermometer including a novel temperature sensor is proposed, which is implemented in two different DRAM process technologies integrated into mobile LPDDR2 and LPDDR3 products. The on-chip thermometer incorporating in mobile LPDDR2 chip is fabricated in a 44nm DRAM process with a supply of 1.1V. The sensor has a temperature sensitivity of −3.2mV/°C, over a range of 0°C to 110°C. Its resolution is 1.94°C and is only limited by the 6.2mV step of the associated resistor ladder not by its own design. The high linearity

of the sensor permits one-point calibration, after which the errors in 61 sample circuits ranged between −1.42°C and +2.66°C. The sensor has an active area of 0.001725mm^2 and consumes less than 0.36μW on average with a supply of 1.1V.

To improve the overall performance including ultra-low operation voltage, temperature sensitivity, low power consumption, high linearity regardless of process skew variations and high productivity improved by one point calibration, the folded type on-chip thermometer incorporating in mobile LPDDR3 chip which fabricated in a 29nm DRAM process with a supply of 1.1V and 0.8V will be proposed. This folded type sensor exhibits further upgrading properties such as a temperature sensitivity of −3.2mV/°C@1.1V &−3.13mV/°C @0.8V, over wide range of -40°C to 110°C. Its resolution is 1.85°C@1.1V & 1.98°C@0.8V and is only limited by the 6.2mV step. The more linearity of folded type sensor permits one-point calibration, after which the errors in 494 sample circuits ranged between −1.94°C and +1.61°C. The folded type sensor has an active area of 0.001606mm^2 and consumes less than 0.19μW@1.1V & 0.14μW@0.8V on average slightly more than unfolded type sensor.

Index Terms—Mobile DRAM, thermometer, temperature sensor, self-refresh, low-power.
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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Recently, high-end smart-phones and large-screen tablet PCs equipped with dual-core or quad-core CPUs are leading rapid growth of the mobile DRAM usage. As there is a greater demand for higher power efficiency and higher density that guarantee longer battery life even in faster processing speed, the mobile double data rate (DDR) DRAM known as LPDDR2 (Low Power Double Data Rate 2) is being rapidly adopted in aforementioned applications. This type of memory consumes less power in standby mode, compared to typical PC DDR DRAM.

However, the increased DRAM density requirement such as 2GB in high-end smart-phones makes it difficult to satisfy the low-power specification as the self-refresh current of DRAM increases correspondingly. This current consists of operating current and stand-by current. The operating current for sensing and restoring data is inversely proportional to the internal refreshing period determined by data retention ability of memory cell. Theoretically, the maximum self-refresh period has to be limited by the retention capability at the highest operating temperature because the data retention time of DRAM cell decreases as the ambient temperature rises. In practice, an on-chip

thermometer can be used to reduce the operating current in self-refresh period by detecting the ambient temperature and setting the internal refresh period best suited to the temperature [1]-[3]. This type of temperature dependent self-refresh mode is called temperature compensated self-refresh (TCSR).

On-chip thermometer is an integrated circuit block that consists of a temperature sensor and peripheral circuit which change the temperature information to digital signal by using the bias circuitry and an analog-to-digital converter (ADC). On-chip thermometer must be compatible with the technology available in the process, must not consume a large area, and must be highly accurate with low power consumption under standard process and supply voltage variations.

On-chip thermometer manufactured by standard CMOS technology have a lot of advantages, such as low power, low-cost, small size etc., but also have a lot of disadvantages such as low productivity or incapable to incorporate the standard DRAM process due to the fact that it is too sensitive for process variation.

In this thesis, the new two types of on-chip thermometer architecture which satisfies all the considerations described above will be introduced. The two types of proposed thermometer features based on a novel CMOS temperature sensor which generates a CTAT voltage without using BJT(Bipolar Junction Transistor) based circuits or conventional CMOS circuits.

Since most of the materials of silicon are temperature dependent physical properties, the transistors and resistors can be used as temperature sensors. In this thesis, the proposed thermometer by utilizing only NMOS transistors and n+ active resistors will be

introduced for maximizing the temperature gain and minimizing the process sensitivity effects. Based on careful expectation of temperature dependency of NMOS transistor and n+ active resistor, the temperature sensor output can be easily estimated and controlled to process adjustment range by selecting resistor value and threshold voltage of NMOS transistor. This feature also enables the one-point calibration, which drastically improves the productivity of post-fabrication process. The proposed sensor techniques have been successfully demonstrated in commercial from 4xnm LPDDR2 to 2xnm mobile LPDDR3 products.

1.2 THESIS ORGANIZATION

This thesis consists of six chapters. Chapter 1 is an introductory chapter which introduces the usage and requirements of the on-chip thermometer in mobile DRAM. In chapter 2, the on-chip CMOS thermometer architecture in mobile DRAM will be introduced and the technique of generating a temperature information digital code which can be used for self-refresh period control will be presented. In this chapter, also the two types of thermometer architectures based on a novel temperature sensor are analyzed about the temperature sensitivity and linearity under PVT variations. In chapter 3, the operational principles and the method to enhance the temperature linearity and mass productivity over a wide temperature range of the proposed temperature sensor will be discussed. In Chapter 4, the design consideration of the peripheral circuits of on-chip

thermometer in mobile DRAM will be presented in detail. In chapter 5, experimental results are demonstrated. The characteristics and performance of the proposed on-chip CMOS thermometer and temperature sensor will be summarized in chapter 6.

CHAPTER 2

ARCHITECTURE OF ON-CHIP THERMOMETER

2.1 INTRODUCTION TO ON-CHIP THERMOMETER IN MOBILE DRAM

The TCSR scheme is an industry standard for low-power DRAMs after decided at the Joint Electron Device Engineering Council (JEDEC) from 2001[1], [2]. Due to the mobile system cannot provide the temperature information to the mobile DRAM directly, incorporating the on-chip thermometer scheme inside the mobile DRAM is mandatory but have a lot of difficulties such as productivity in post fabrication process, the low power consumption, good temperature measurement accuracy and small layout area.

The temperature sensor significantly suffers from process variations due to the small temperature coefficient of the sensing element which implemented in deep-submicron CMOS standard technology [1]-[5]. The various approaches about the on-chip thermometer have been reported but the heart of the thermometer is temperature sensor which is detecting the exactly on-chip temperature. The temperature sensor design which have a high temperature sensitivity and measurement accuracy over the wide temperature range with small layout area and low power consumption penalty in mobile DRAM is very challenging when the supply voltage and process technology are scaled down.

To overcome all those problems and meet the specification of low power mobile

DRAM, the key design issues of on-chip thermometer including temperature sensor are categorized by productivity, low power consumption, temperature sensitivity and accuracy, temperature linearity regardless of process variations and small layout area.

Productivity issues of on-chip thermometer when incorporating in standard CMOS technology mainly comes from the different temperature behavior with process variations. In other words, no more correctable to use or additional temperature test or trimming steps after the post fabrication process are very critical problems for mass production. Most of the mobile DRAM has a chip-by-chip test and trimming step to make up for yield loss by replacing a defect cell with good cell utilizing a resistive fuse. Because the temperature sensor significantly influenced by process variations, basically long time chip-by-chip test or many temperature trimming step are necessary to cover the whole temperature range and process skews perfectly. One step test and trimming process is desirable even if the temperature linearity or slope of temperature sensor output with temperature change is different. One step test and trimming process must to be done to reduce cost issue due to the temperature sensor itself as a non-critical part of the mobile DRAM chip. As mentioned above, a process variation tolerant on-chip temperature sensor design is important issue of on-chip thermometer scheme in terms of mass productivity of post fabrication process in mobile DRAM.

To overcome this issue, the temperature sensor adjustment scheme for eliminating the multi-temperature testing procedure was reported [1], [2]. The adaptive changing of self-refresh period using an on-chip thermometer scheme which equipped the temperature sensor adjustment method with single reference temperature is as shown in Fig.2.1.1 [1].

It was composed by thermometer block which generates digital representation of on-chip temperature information using an analog-to-digital converter (ADC), temperature comparator which acts as binary searching with reference temperature, fuse options to compensate for ±8°C of temperature offset due to errors in the sensor and adaptive changing of self-refresh period block [1].

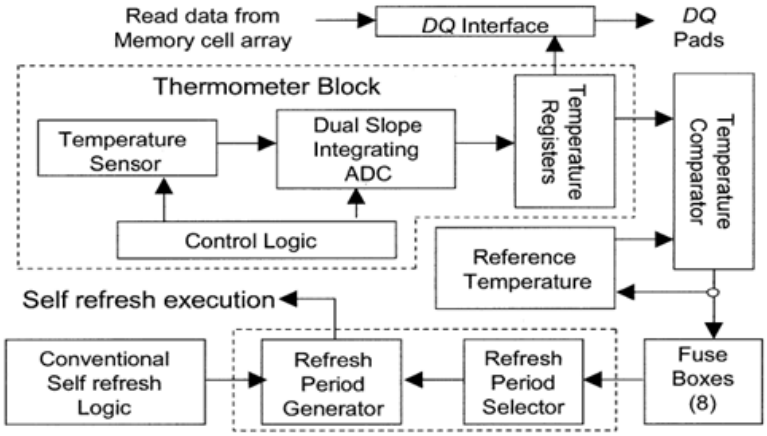

Fig. 2.1.1. Block diagram of a self-refresh scheme with on-chip thermometer [1]

The dual-referenced searching scheme was also reported to correct the trimming error caused by process variations [2]. Fig. 2.1.2 shows the searching sequence when the fabricated tuning resistance is 10% smaller than the target, using the dual-referenced searching scheme [2]. As illustrated in Fig. 2.1.2, x can be extracted for process skews which cause tuning error are related to x. With the nonlinearity compensation factor mentioned previously, tuning accuracy can be improved. Fig. 2.1.3 shows the implemented temperature sensor circuit with the dual-referenced searching scheme. AU0–AU5 are test mode input signals to raise the trip point at the 85 °C test, and they are

set to be low in normal operation. Similarly, AD0–AD5 are test mode input signals to lower the trip point at the -5°C test, and they are set to be high in normal operation [2].

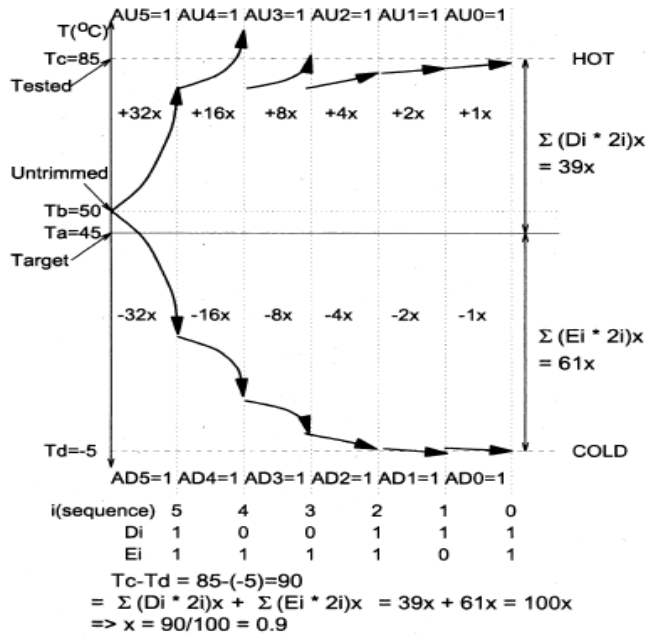

Fig. 2.1.2. Sequence of dual-referenced searching scheme when the fabricated tuning resistance is 10% smaller than target (x = 0:9) [2].

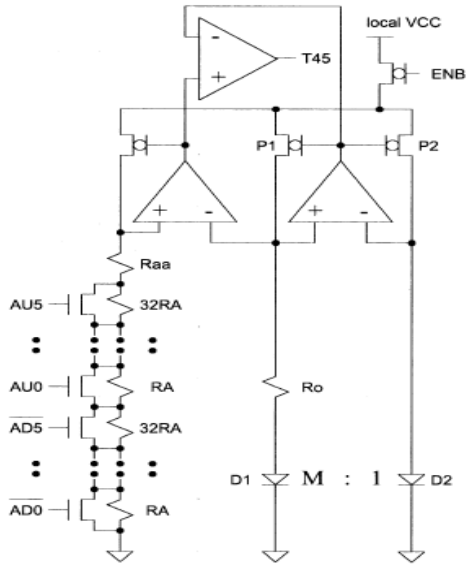

Fig. 2.1.3. Temperature sensor circuit with dual-referenced searching scheme [2]

Another major issue of the on-chip thermometer is power consumption, including dc current in the analog circuits. The current consumption of thermometer block is relatively small but could be affect to I_{DD6} (Self-refresh current) which related idle state power consumption in mobile DRAM. Since the on-chip thermometer in mobile DRAM is only used during the self-refresh operation period, it could be reduced by a proper control between normal and self-refresh operation [1]-[3].

As shown in Fig. 2.1.4 [1], when the burst refresh operation is finished, thermometer is turned on and measures a temperature. Then, the refresh operation is executed according to the refresh period determined by the measured temperature. The thermometer is turned on again when 8K refresh cycles are finished, and the process continues until the self-refresh mode is ended. Even though the current consumption of the thermometer during the temperature measurement period is as large as 2.4 mA, the

average current is less than 1uA since one measurement cycle with 32us (T_4) is executed during the entire 8K refresh cycles [1].

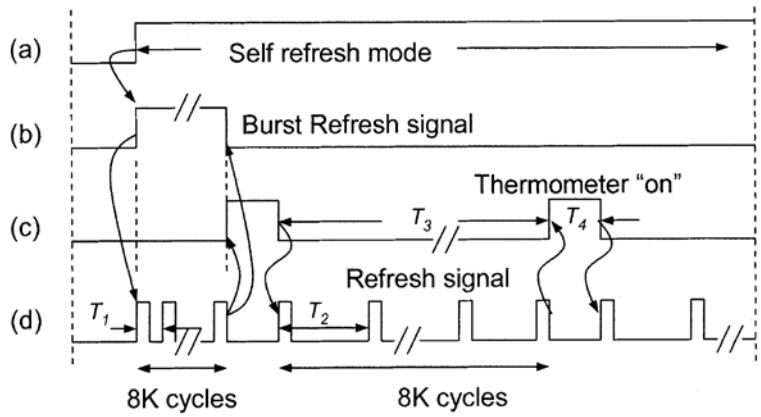

Fig. 2.1.4. Self-refresh and thermometer control scheme [1]

The different approach is reported to overcome this issue. To reduce the static current consumed by the temperature sensor, the sensor output is periodically latched and held during the self-refresh mode. Since the temperature does not change rapidly, occasional periodic sampling and adjustment will suffice. The period and the pulse-width of the sampling clock EN, as shown in Fig. 2.1.5 [2], are designed to be 5ms and 5us, respectively, for an average current of 0.1uA

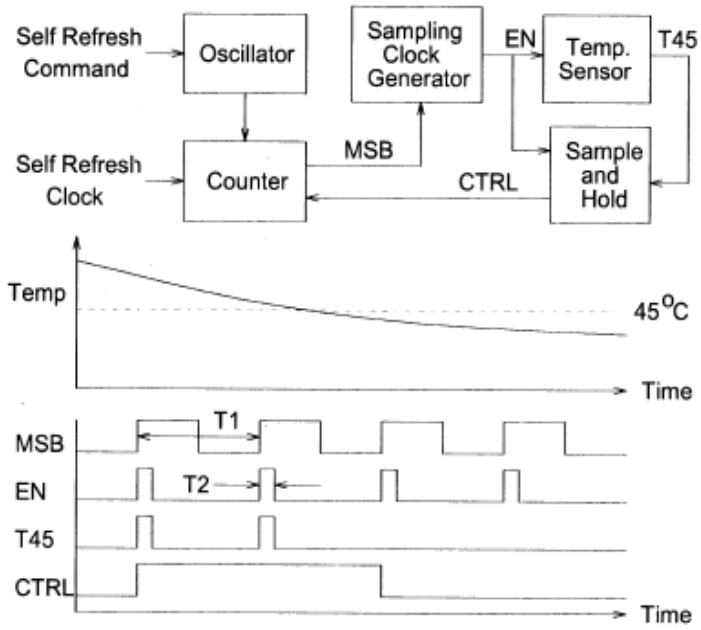

Fig. 2.1.5. Block diagram and timing diagram for the self-refresh period control with temperature sensor [2].

The third key essential issue of the on-chip thermometer is temperature sensitivity and accuracy, which should be the same temperature sensitivity and linearity with different process skews. As described before, productivity in mass production is directly related on these performance of on-chip thermometer as a small part of high density mobile DRAM. The on-chip thermometer itself do not affect the mass production yield of mobile DRAM but deviation from the normal characteristics sacrifice the productivity of the whole chip.

The process variation tolerant healthy design of CMOS temperature sensors is the key solution for productivity point of view. Most of the on-chip temperature sensors are based on the use of Bipolar Junction Transistors (BJTs), whose base-emitter voltage can be used to obtain the thermal voltage kT/q [2]. The implementation of this kind of

temperature sensors in standard CMOS processes can be done making use of lateral or vertical substrate transistors. However, these sensors require complicated calibration and their non-linear dependency with temperature of which demands complicated peripheral circuits that make the sensors occupy a large silicon layout area.

These kinds of temperature sensors are generally implemented by using a technique of comparing the difference in the base–emitter voltage of two bipolar junction transistors (BJTs) at different current densities as shown in Fig. 2.1.6. [1]. The temperature sensors mentioned above[1],[2] which based on conventional band-gap reference-based with NPN diode requires extra processing step in DRAM process and occupies a relatively large area so it costs high as the temperature sensor for mobile DRAM.

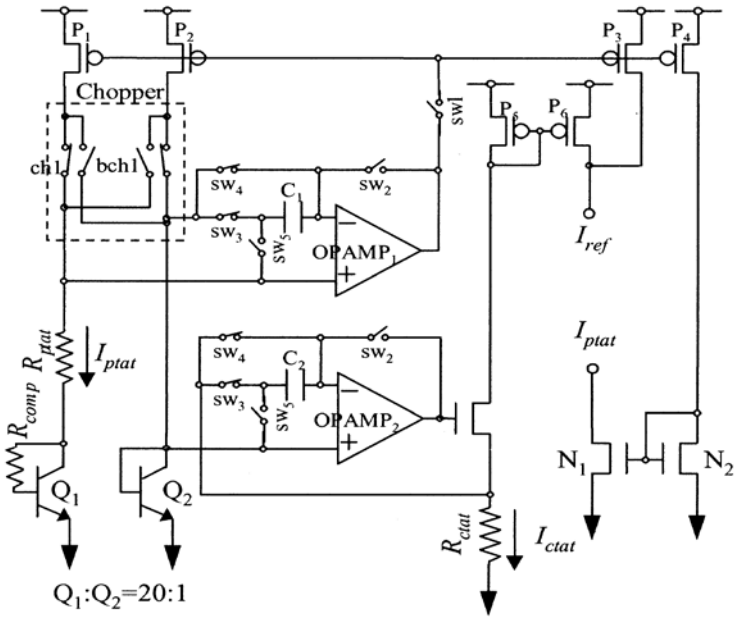

Fig. 2.1.6. Schematic of temperature sensor [1]

Temperature sensors are generally categorized into two major groups. The conventional type is based on proportional-to-absolute temperature (PTAT) principles by using bipolar junction transistor (BJT) [4] or CMOS transistor [1], while the alternative one is based on temperature dependent time delay of logic gates [5], [6]. Examples of the former are several high-resolution thermometers which were implemented using PTAT current generator and analog-to-digital converter (ADC) [7], [8]. They can typically achieve better than ±1°C accuracy with calibration. It was also reported that the enhanced accuracy of ±0.1°C with 75μW power consumption was achieved by combining with dynamic element matching, offset cancellation and calibration [9]. Even though the temperature sensor itself is simple and precise, it requires a high resolution ADC to achieve better accuracies with the penalties of increased circuit complexity and chip area. The power consumption of this type of thermometer is usually in tens to hundreds of μW range; therefore, they are not suitable for low power mobile DRAM. Examples of the latter are thermometers based on inverter delay cells and time-to-digital converter (TDC), in which the time it takes for the current to charge a capacitor to a fixed threshold voltage is measured [6], [10], [11].

After an initial batch calibration, a low-cost one-point calibration of individual samples is sufficient to achieve inaccuracies of a few degrees over from 40°C to 90°C [10]. By using two-point calibration, the inaccuracy can be improved to about ±1°C from -10°C to 30°C [11]. Temperature sensors based on the temperature-dependent propagation delay of a chain of inverters have also been proposed [5].

The minimization of the number of processing steps and the reduction of silicon area

in mobile DRAM production is very critical for cost minimization. The temperature measurement accuracy is concerned, the conventional BJT based temperature sensor reported in [1], [4] has a limited accuracy due to small number of current cross points, and is difficult to improve the resolution due to too large circuit overhead. In this situation, to improve the temperature accuracy by increasing the number of temperature trip points, the temperature sensor must use a number of additional current branches with different resistor values, op-amps and adjustable external signals, causing a significant area overhead.

Recently the newly developed method of monitoring the temperature by means of temperature-sensitive resistor and ring oscillator without extra processing step and with significantly less overhead on silicon area [3]. The newly reported temperature sensor, as shown in Fig. 2.1.7, based on present's novel low-cost CMOS temperature sensor [3], the temperature dependency of poly resistance is used to generate a temperature-dependent bias current, and a ring oscillator driven by this bias current is employed to obtain the digital code pertaining to on-chip temperature for controlling the self-refresh period of a mobile DRAM as illustrated in Fig. 2.1.8 and Fig. 2.1.9. This method is highly area-efficient, simple and easy for IC implementation as compared to traditional temperature sensors based on band-gap reference. The temperature sensor achieves the measured inaccuracy of −0.7 to +0.9°C after two point calibration.

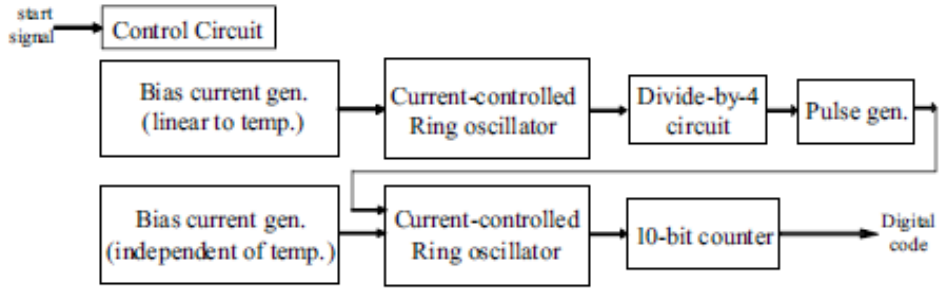

Fig. 2.1.7. Proposed temperature sensor [3]

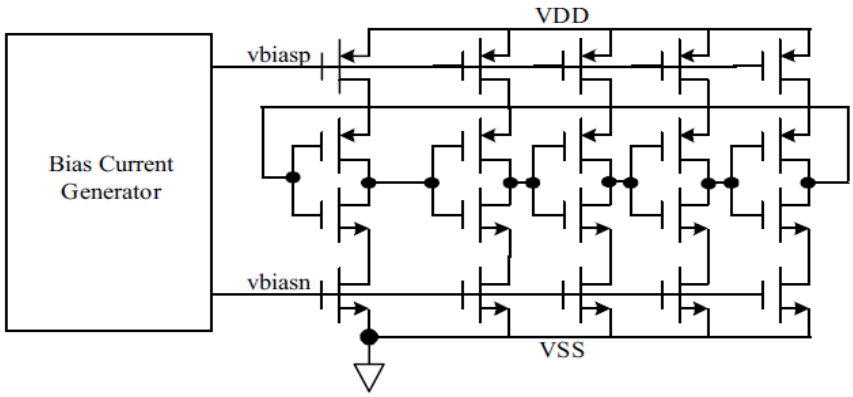

Fig. 2.1.8. Structure of CMOS ring oscillator with current starved inverter stages [3]

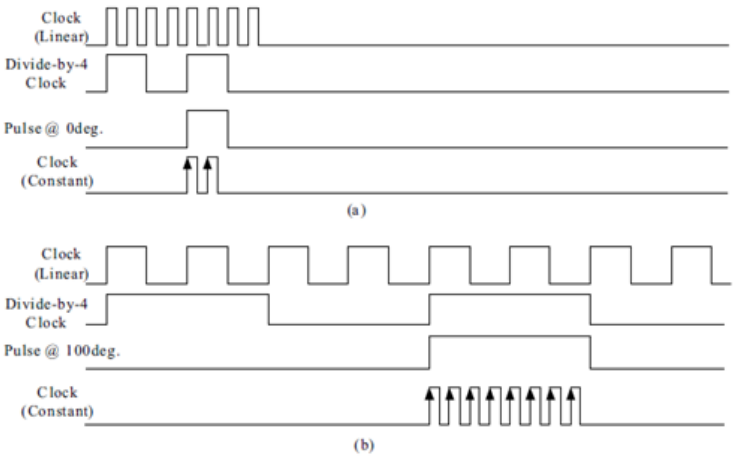

Fig.2.1.9. Timing diagram of temperature sensor operation: (a) for 0°C, (b) 100°C [3]

An all-digital CMOS temperature sensor based on dual-DLL has also been reported [5]. They are not only used to monitor the thermal profile of a microprocessor but also used in DRAM self-refresh control. However, self-refresh control does not have to cover the every temperature point of the operating range [13]. This feature suggests that TDC based thermometers are not good candidates because such thermometers occupy a considerable area and consume significant power [6]. Besides, their low immunity to the process variations inevitably requires calibration technique with hardware overhead.

Consequently, the temperature information on some specific points should be acquired instantly with minimal power and area consumption in DRAM self-refresh control. In addition, one-point calibration is preferred over two-point calibration to reduce the time and the complexity of the calibration process. These facts make the PTAT current or voltage generators and simple comparators more attractive over the inverter delay cells and complex ADCs, respectively.

2.2 PROPOSED ON-CHIP CMOS THERMOMETER ARCHITECTURE

The overall architecture of the proposed on-chip thermometer used for mobile LPDDR2 implemented in a 44nm DRAM process technology is shown in Fig. 2.2.1

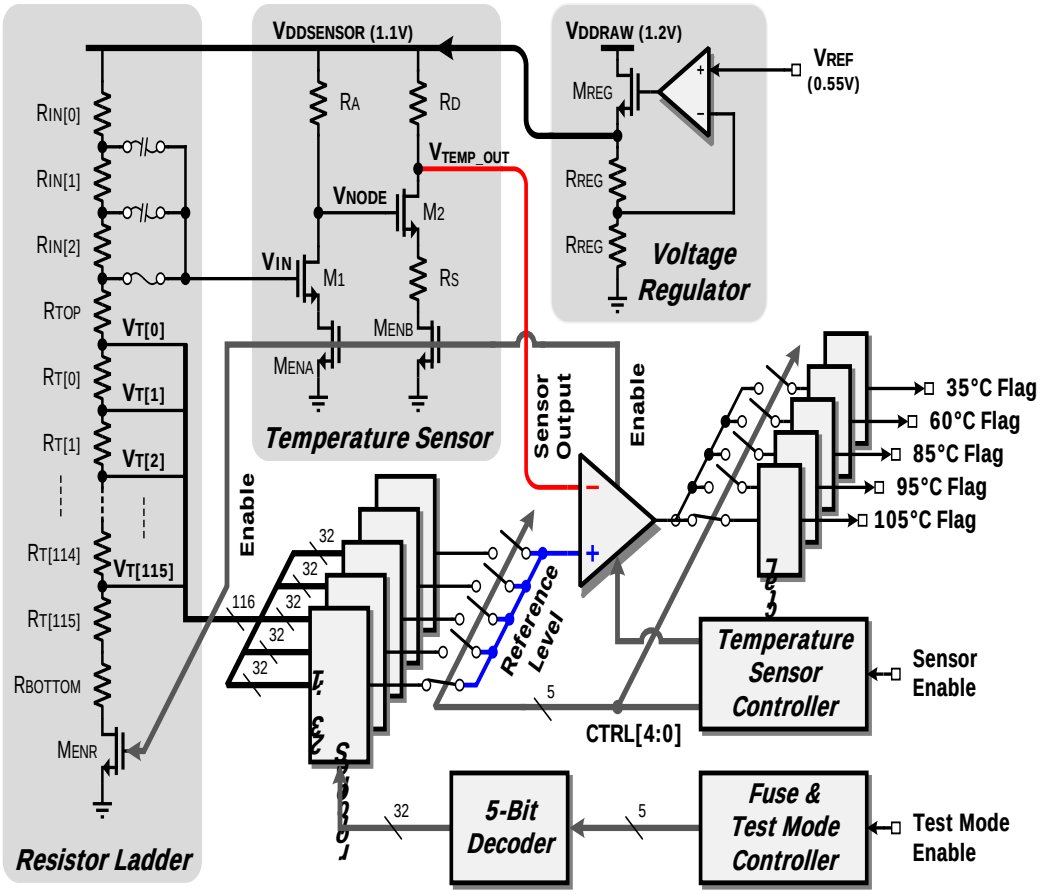

Fig. 2.2.1. Proposed on-chip CMOS thermometer including temperature sensor.

The proposed on-chip CMOS thermometer in mobile DRAM is composed of a temperature sensor, a resistor ladder which adjust to temperature sensor output target, five 32:1 selectors which used for reference level of each predetermined temperature, a voltage regulator which provide the temperature independent voltage source, a comparator which compares the real time on-chip temperature sensor output with designated reference temperature output, five latches which hold the temperature information, a temperature sensor controller which controls operation period of total thermometer block for power savings and a fuse & test mode controller to detect and adjust for trimming and calibration of reference level.

To increase the tolerance from the supply noise, the voltage regulator receives a temperature independent internal bias (V_{REF}=0.55V) from the reference generator which located on mobile DRAM and maintains the internal supply voltage $V_{DDSENSOR}$ (1.1V), which is required in every individual block of the thermometer. Thermometer block generates temperature information from comparator which acts as binary searching with five predetermined reference temperature, fuse options to compensate for ±1.6℃ of temperature offset due to errors in the sensor and adaptive changing of self-refresh period block

The temperature sensor generates the sensor output voltage V_{TEMP_OUT} which linearly tracks any temperature variation. The detailed operational principle of the sensor will be described in next chapter. At the same time, the resistor ladder generates various voltage levels, from which five reference levels are chosen to represent five reference temperatures (105℃, 95℃, 85℃, 60℃, 35℃). The temperature sensor controller

sequentially selects one of these reference levels as the single reference level to be compared with the sensor output voltage. The results of these comparisons are latched to generate five temperature indicating flags. These flags are sent to the main DRAM system to change the refresh period according to the retention time of DRAM cells at the current temperature.

To compensate process variations, one of some voltage levels from the resistor ladder is selected as the input V_{IN} of the temperature sensor and the other voltage levels V_T [115:0] are used as the levels to generate five reference levels. Each of the reference levels is adjustable among 32 consecutive levels with the step of 6.2mV. When test mode is enabled, each of the five levels is monitored to detect optimal reference levels. After trimming is completed, selected levels are permanently set with fuses. The fixed levels are robust to the temperature variation since they are generated from the temperature independent internal supply voltage $V_{DDSENSOR}$ as mentioned above.

Fig. 2.2.2 illustrates the temperature sensor output voltage behavior and the five predetermined reference levels. Assuming an ambient temperature of 70°C for example, the operational principle described above is visualized with two figures. Since each reference level of the five reference temperatures is set equal to the output voltage of the temperature sensor at the corresponding temperature, it is evident from the figure that the output voltage at 70°C lies between the reference level at 85°C and the reference level at 60°C.

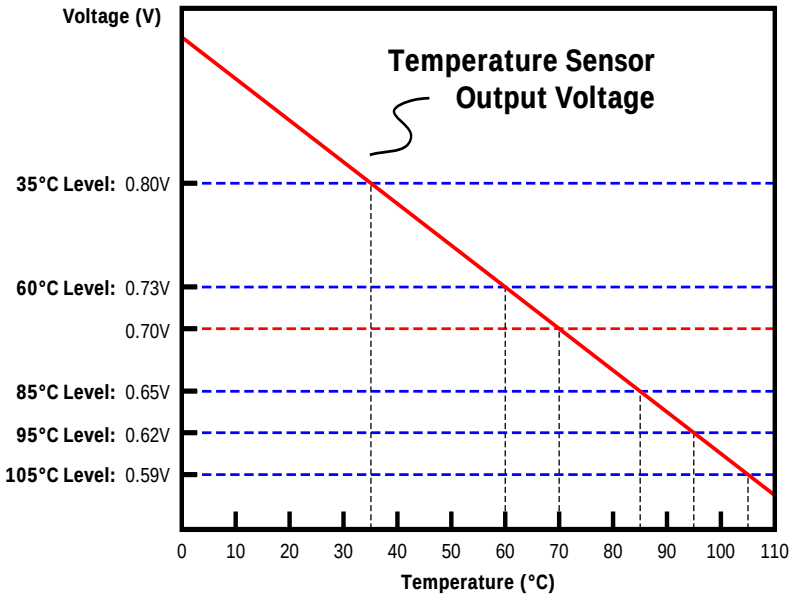

Fig. 2.2.2. Temperature dependency of the sensor output voltage and the reference levels

Fig. 2.2.3 depicts the timing diagram of all the major input and output signals of the thermometer, which is operating at the ambient temperature of 70°C. To minimize the power consumptions of on-chip thermometer, the temperature sensor controller generates the *Enable* signal to start and stop the operation of the temperature sensor, the resistor ladder, and the comparator during 128μs in every 8ms at the self-refresh mode of the mobile DRAM.

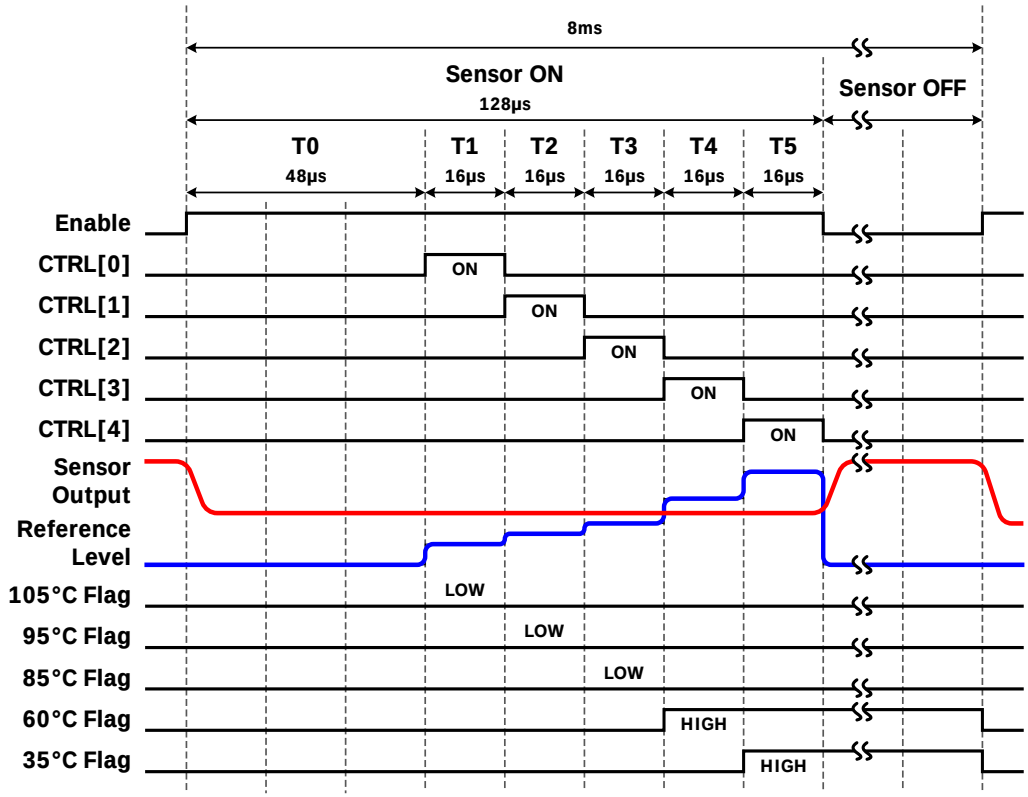

Fig. 2.2.3. Timing diagram of the input and output signals of the thermometer

When the self-refresh operation is started, thermometer is turned on and temperature sensor measures the real time on-chip temperature and generates sensor output level (V_{TEMP_OUT}) corresponding to ambient temperature. Then, the refresh operation is executed according to the refresh period determined by the measured temperature information digital code which generated by comparator output during 128µs in every 8ms at the self-refresh mode. Considering about power consumption, even though the current consumption for the thermometer during the temperature measurement period is as large as 2.4 mA, the average current is less than 1uA since one measurement cycle

with 128us is executed during the entire 8ms refresh cycles.

A new cycle to detect the temperature begins when the Enable signal goes high. During the period T0 which lasts for 48μsec, all the analog blocks including the temperature sensor are powered on and the sensor output voltage settles to the value which represents the current ambient temperature. Since the temperature does not change abruptly, the variation of the settled output voltage is negligible within the whole sensing time of one cycle, 128μs.

During the five periods from T1 to T5, each of which periods enabled during 16μs, the sensor output voltage is compared to the reference level, which is selected among the five reference levels by the switch control signals CTRL [4:0]. If the output voltage is lower than the selected reference level for each given period, the comparator output goes high and it is latched to generate the temperature indicating flag of the reference temperature being compared. In case of ambient temperature of 70°C, the output flags of 105°C, 95°C, and 85°C stay low during the periods of T1, T2, and T3, whereas the output flags of 60°C and 35°C go high during the periods of T4 and T5. These five temperature indicating flags will be used to reset the designated refresh period corresponding to this temperature in the main DRAM system. Since the temperature is not changed abruptly, the non-temperature-measurement period, which is less than one second in this design, could be enough to follow temperature variation with much smaller error than 1 °C.

2.3 TEMPERATURE READOUT PROCEDURE OF PROPOSED ON-CHIP CMOS THERMOMETER

The simulation result of overall temperature readout procedure of the proposed on-chip thermometer is as shown in Fig. 2.3.1.

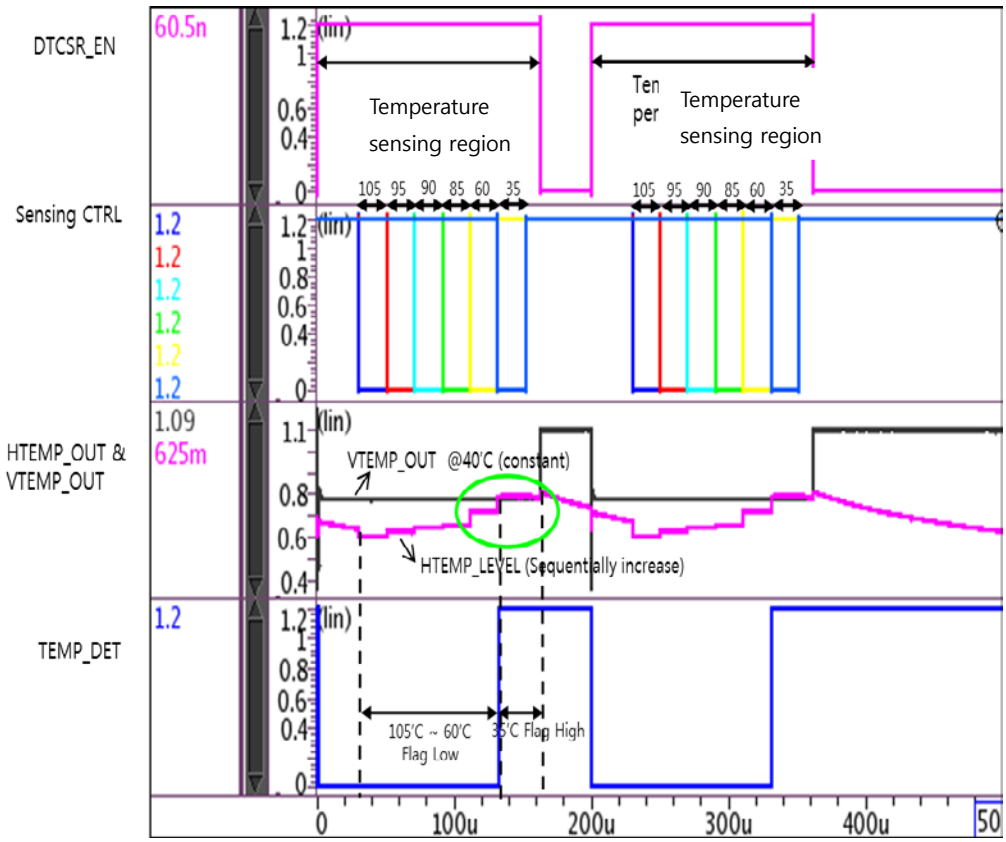

Fig. 2.3.1 Temperature readout procedure of the proposed on-chip thermometer

When the sensor Enable (DTCSR_EN) signal is high, the readout procedure of temperature sensor starts. Then, the temperature sensor generates the V_{TEMP_OUT} which

equals to the corresponding temperature (40℃). After initial settling period T0 (48usec), the sensing-CTRL-signal turned on sequentially by given pattern from high temperature to low temperature. According to these control signal, temperature sensor output (V_{TEMP_OUT}) compared with the predetermined reference voltage (H_{TEMP_OUT}) and generate the comparison results as temperature indication code for five temperatures (105℃, 95℃, 85℃, 60℃, 35℃) consecutively.

Comparator compares temperature sensor output (V_{TEMP_OUT}) with the reference voltage output (H_{TEMP_OUT}) sequentially from 105℃ to 10℃ in real time. If the reference voltage is smaller than the temperature sensor output generates low output (TEMP_DET). If the reference voltage is bigger than the temperature sensor output generates high output (TEMP_DET). Comparator outputs as a result of readout procedure performed for all temperatures are stored by five latches. The example of comparator performed at 40℃ is shown in Fig. 2.3.1, temperature comparing flags of each 105℃, 95℃ and 85℃ flag low values but flags high value at 60℃ and 35℃.

At the end of the comparing process, DTCSR_EN signal goes to low and checks the values of flags. So the information of the present temperature is in the section where the flag value changes into low to high, is obtained.

2.4 PROPOSED FOLDED TYPE ON-CHIP CMOS THERMOMETER ARCHITECTURE

The more advanced architecture of the proposed on-chip thermometer used for mobile LPDDR3 DRAM in 29nm CMOS process is shown in Fig. 2.4.1.

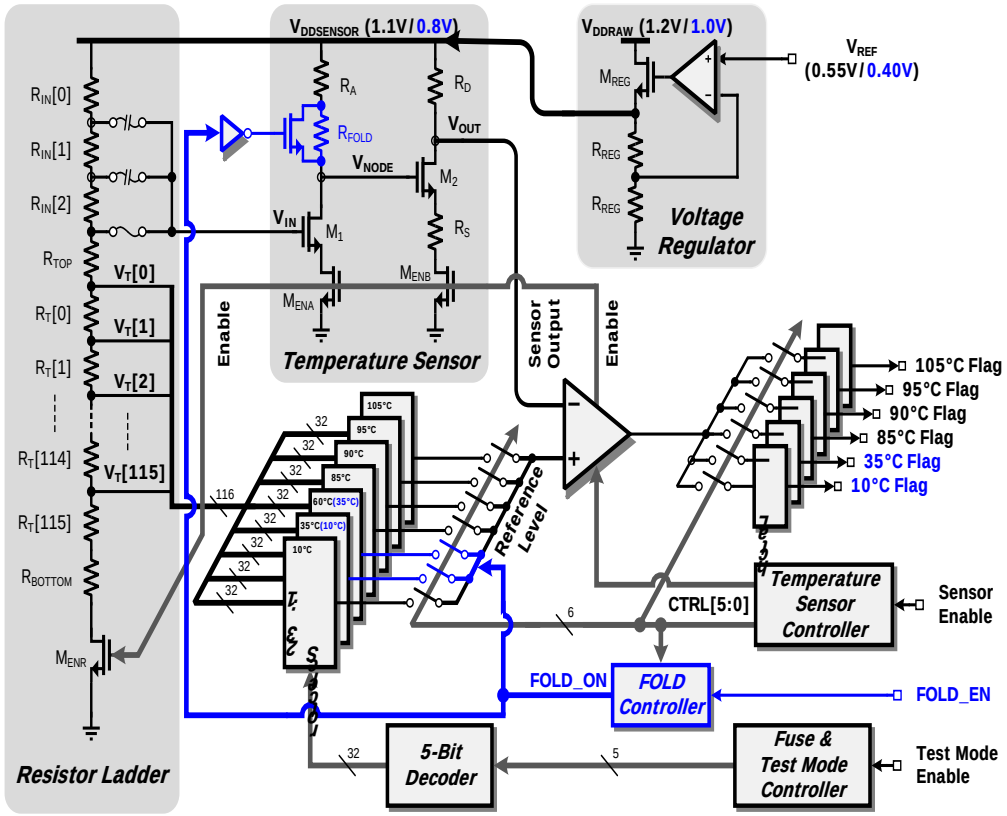

Fig. 2.4.1. Proposed folded type on-chip CMOS thermometer including folded type temperature sensor.

The *FOLD controller* is added to change the load resistor value of 1st stage temperature sensor below the certain temperature (<35°C), so called the folded type on-chip CMOS thermometer. The other parts of the remain circuits are almost the same as

shown in Fig. 2.2.1, except for adding 95°C and changing from 60°C to 10°C with respect to reference temperatures which reflects the temperature specification change of refresh control region in mobile LPDDR3.

In case of the folded type on-chip thermometer architecture incorporating in mobile LPDDR3, the thermometer is composed of temperature sensor, a resistor ladder which adjust to a temperature sensor output target level, six 32:1 selectors which preset the predetermined reference level of each designated temperature, a voltage regulator which provide the temperature independent voltage source, a comparator which compares the real time on-chip temperature sensor output with predetermined six reference temperature, six latches which hold the temperature indication digital code, a temperature sensor controller which controls the enabling period of thermometer block for power savings and a fuse & test mode controller to detect and adjust for trimming and calibration of reference level.

To compensate process variations, one of some voltage levels from the resistor ladder is selected by pre-trimmed fuse as the input (V_{IN}) of the 1st stage of temperature sensor and the other voltage levels V_T [115:0] are used for predetermined six reference temperature levels which tracks from the sensor output. Each of the reference levels is adjustable among 32 consecutive levels with the step of 6.2mV. When test mode is enabled, each of the six levels is trimmed to detect optimal reference levels using the fuse and test mode controller and the 32:1 selectors. After fuse trimming is completed, selected levels are permanently set with fuses. The fixed levels are robust to the temperature variation since they are generated from the temperature independent internal

supply voltage $V_{DDSENSOR}$.

Fig. 2.4.2 demonstrates the sensor output voltage and the six reference levels with respect to the temperature change. Assuming an ambient temperature of 15°C for example, the operational principle described above is visualized with two figures. Since each reference level of the six reference temperatures is set equal to the output voltage of the temperature sensor at the corresponding temperature, it is evident from the figure that the output voltage at 15°C lies between the reference level at 35°C and the reference level at 10°C.

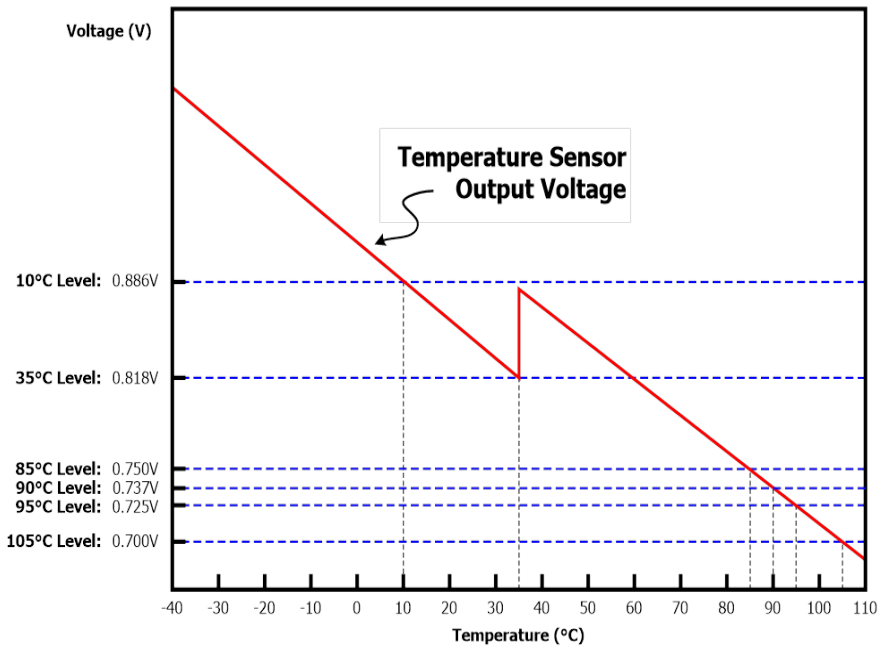

Fig. 2.4.2. Temperature dependency of the sensor output voltage and the reference levels

Fig. 2.4.3 illustrates the timing diagram of all the major input and output signals of

the thermometer, which is operating at the below 35°C to show the how the FOLD ON signal affect the operation.

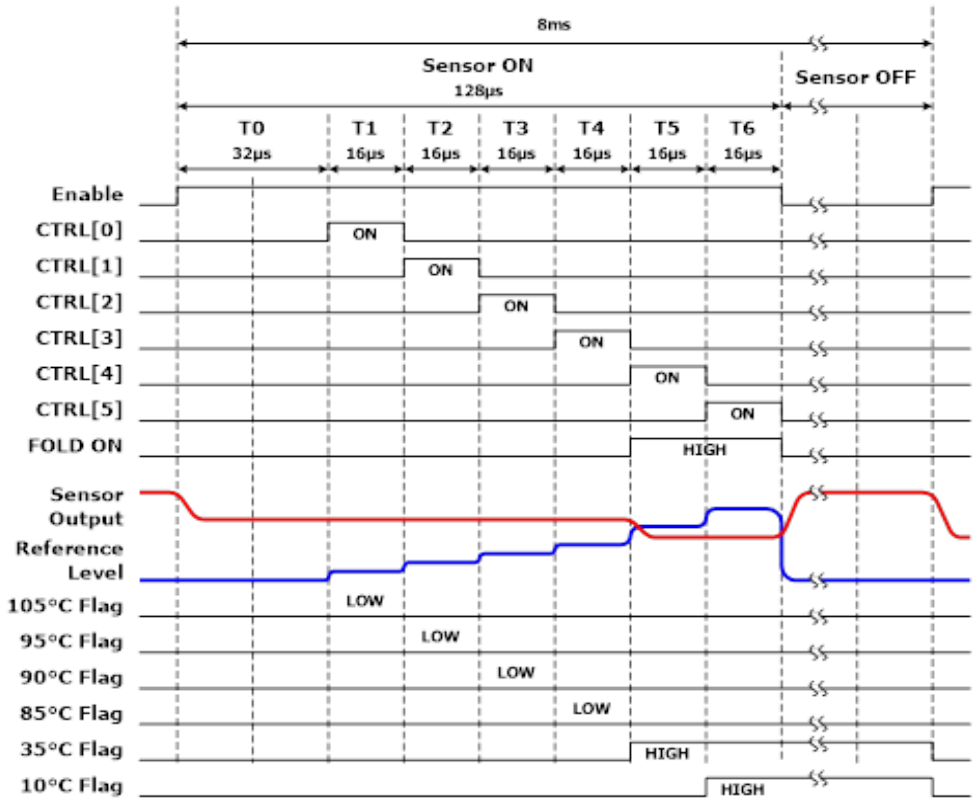

Fig. 2.4.3. Timing diagram of the input and output signals of the proposed folded type on-chip CMOS thermometer

Beginning with the Enable signal goes high, a temperature measurement starts after an initial period T0 as all the analog blocks are powered on and the sufficiently settled. Since the ambient temperature does not change abruptly, the output voltage variation and the existence of two state hysteresis problem near the 35°C is negligible within the whole 128µs sensing time of one cycle. The six periods from T1 to T6, the sensor output is compared to a reference voltage selected from the six pre-determined levels utilizing the

switch control signals CTRL [5:0]. The temperature sensor controller sequentially selects each of reference voltages for comparison with the sensor output. The results of these comparisons are latched to set one of six temperature flags. These flags are routed to the DRAM controller to set the appropriate refresh period.

The overall temperature decision sequence is same as previously described in chapter 2.2. To minimize the power consumptions of on-chip thermometer, it operates during 128μs in every 8ms at the self-refresh mode of the mobile DRAM.

From T1 to T6 which lasts for 16μs, the output voltage is compared to the six reference level which is determined by the switch control signals CTRL [5:0]. The different scheme from previous unfolded structure is the folded signal (FOLD ON) goes high when an ambient temperature is below the 35°C, automatically the temperature sensor output level decrease from the 35°C reference level.

In case of folded type temperature sensor, the sensor output level folded at the specific region near the 35°C do not concern about two corresponding temperature existing, since the temperature change from high to low or vice versa do not abruptly happened. If the output voltage is lower than the selected reference level for each given period, the comparator output goes high and it is latched to generate the temperature indicating flag of the reference temperature being compared. In this example, the output flags of 105°C, 95°C, 90°C ,and 85°C stay low during the periods of T1, T2, T3 and T4, whereas the output flags of 35°C and 10°C go high during the periods of T5 and T6, in case of an ambient temperature is assumed to be 15°C. These six temperature indicating flags will be used to change the refresh period in the main DRAM system.

2.5 TEMPERATURE READOUT PROCEDURE OF PROPOSED FOLDED TYPE ON-CHIP CMOS THERMOMETER

By incorporating a folding controller, the simulation results of temperature readout procedure for the proposed folded type thermometer shows different behavior at the specific temperature as illustrated in Fig. 2.5.1.

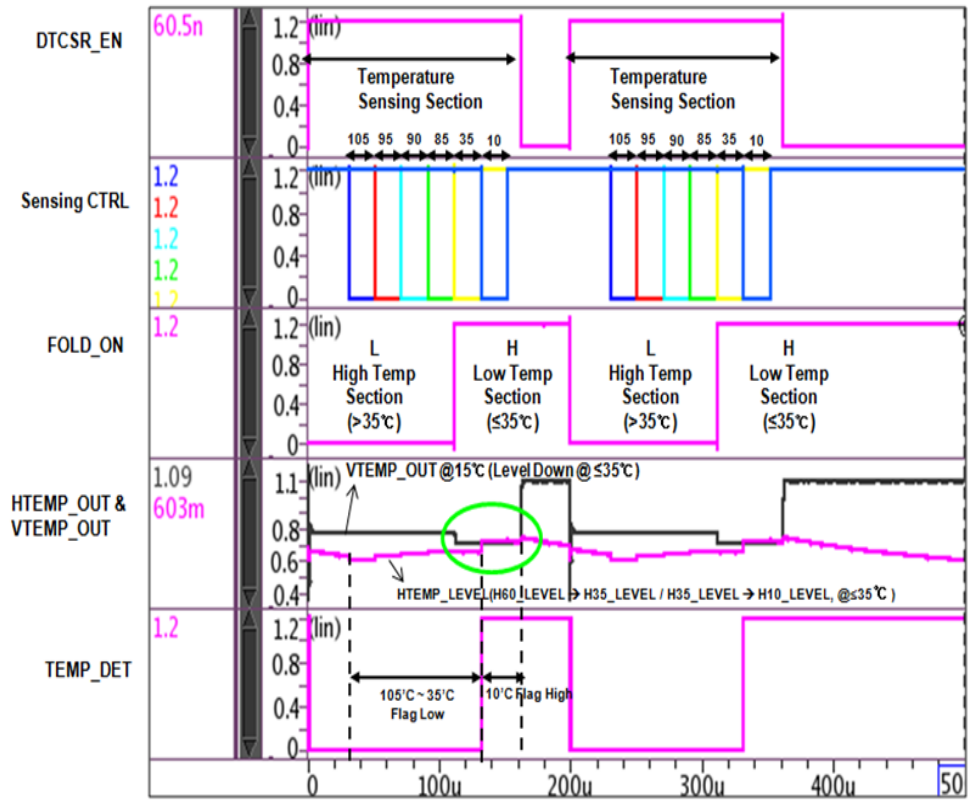

Fig. 2.5.1 Temperature readout procedure of the proposed folded type thermometer.

When the temperature sensor Enable (DTCSR_EN) signal is high, temperature sensor readout operation is activated, the sensing-CTRL-signal is turned on sequentially

by given pattern from high to low temperature. According to these control signal, temperature sensor output (V_{TEMP_OUT}) compared with the reference voltage (H_{TEMP_OUT}) and generate the comparison results as temperature indication code for six temperature (105℃, 95℃, 90℃, 85℃, 35℃, 10℃).

Comparator compares temperature sensor output and the reference voltage in real time. And generates low output (TEMP_DET) if the reference voltage is smaller than the temperature sensor's output. And generate high output (TEMP_DET) if the reference voltage is bigger than the temperature sensor's output.

Comparator compares temperature sensor output (V_{TEMP_OUT}) with the reference voltage output (H_{TEMP_OUT}) sequentially from 105℃ to 10℃ in real time. If the reference voltage is smaller than the temperature sensor output generates low output (TEMP_DET). If the reference voltage is bigger than the temperature sensor output generates high output (TEMP_DET). Comparator outputs as a result of readout procedure performed for all temperatures are stored by six latches. The example of comparator performed at 15℃ is shown in Fig. 2.5.1, the FOLD_ON signal is changed from low and high at the ambient temperature below 35℃, and then temperature sensor output voltage tracks the left side of the sensor output curve as demonstrated in Fig. 2.4.2. Temperature comparing results of each 105℃, 95℃, 85℃ and 35℃ generates low values and changes to high value at 10℃. The temperature sensor output behavior is divided by two part with respect to 35℃, according to the FOLD_ON signal is changed "LOW → HIGH", when moving at a high temperature to lower temperature region or vice versa.

2.6 ONE-POINT CALIBRATION METHOD

As mentioned in previous chapter, one-point calibration of individual chips is very effective to enhance the temperature accuracies of a few degrees over wide temperature range. The linearity and accuracy of temperature sensors can be improved by calibrating and trimming of them at one or more known temperatures. The wafer level fuse trimming process already is used for replacing the defect cells with good cells in mobile DRAM post fabrication process, on-point calibration by fuse trimming a resistor is not a serious problem of cost issue when it is constructed at the same temperature. The process variation effect of an accuracy and linearity of temperature sensor is unsystematic, so measurements on many chips are required to obtain reliable estimation of its inaccuracy and behaviors.

One-point calibration is the one of the good approaches to minimize the process variation effect. By adapting this method, if the every chip tracks the same V_{TEMP_OUT} behavior regardless of process skews tracks, the productivity issue of incorporating into mobile DRAM chips could be solved over the wide temperature range.

In case of mobile DRAM process, the process skew effect is more severe at higher temperature mainly due to the threshold voltage and the leakage current of transistor is higher than cold temperature.

Fig. 2.6.1 and Fig. 2.6.2 are simplified comparison graphs of the temperature sensor behavior with different process corner when performed before and after one-point calibration. After one-point calibration, error is decreasing drastically. Comparing graphs

before and after the one-point calibration, the maximum difference between the process corners is reduced from 28.4 mV to 10.8 mV. In other words, because of the one-point calibration, the accuracy and linearity of temperature sensor could be improved.

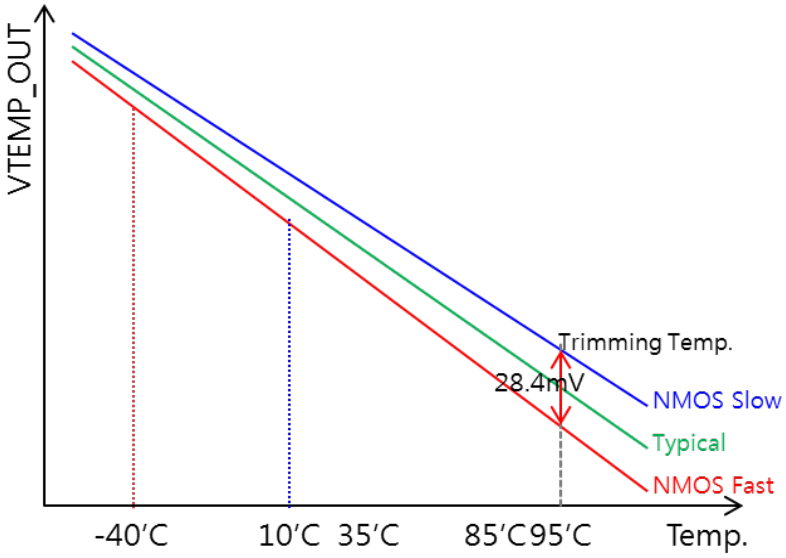

Fig. 2.6.1. Temperature sensor measured with various process corners before one-point calibration.

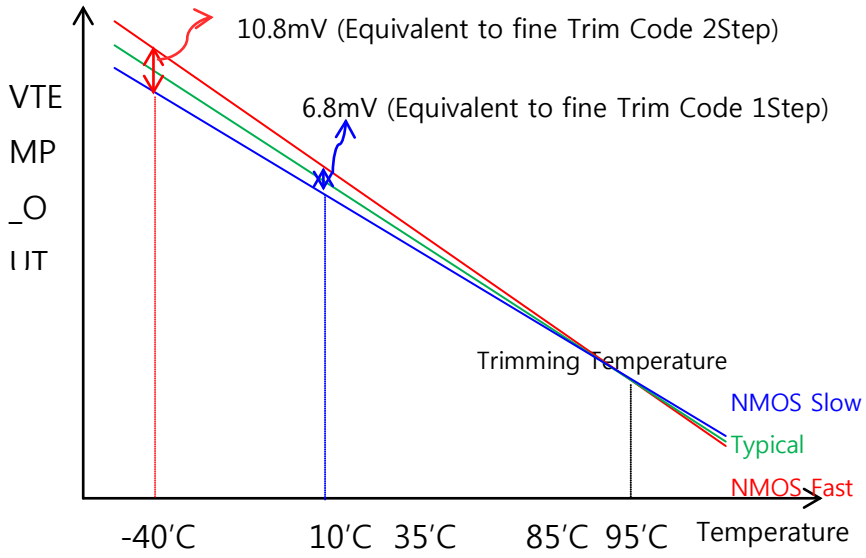

Fig. 2.6.2. Temperature sensor measured with various process corners after one-point calibration.

2.7 TEMPERATURE LINEARITY OF TEMPERATURE SENSOR

As mentioned before, one of the major productivity issues of on-chip temperature sensor when incorporating in mobile DRAM are the different temperature linearity or slope with each process skews. Fig. 2.7.1 shows the simulation results of adapting into 38nm DRAM process corner and the low supply voltage environment using 44nm circuit.

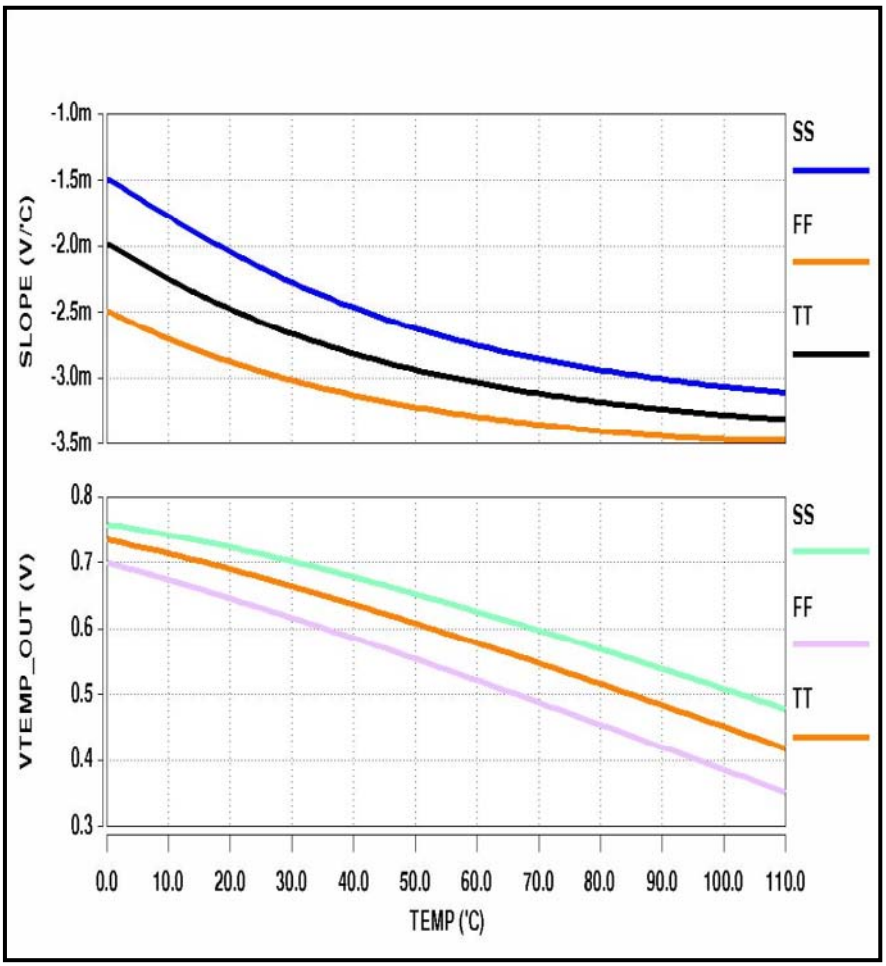

Fig. 2.7.1 Temperature sensor output sensitivity in the low supply voltage

As temperature changes, the sensitivity of temperature sensor also changes as much as maximum 1.5mV/℃. In other words, the linearity of temperature sensor is reduced according to the process variation at low temperature. Therefore, improved temperature sensor circuit is needed because existing temperature sensor cannot be used in the low supply voltage condition. Simulated results are divided into two sections, before the calibration and after the calibration, to compare the performance of temperature sensor. Simulations are performed under the FF (Fast PMOS and NMOS transistors), SS(Slow PMOS and NMOS transistors), TT(Typical PMOS and NMOS transistors) environment, using the existing 1.1V design.

Fig. 2.7.2 and Fig. 2.7.3 are the worst case simulation results of temperature sensor output with process corner before the one-point calibration.

Reference line is drawn by linear regression of three curve‘s average. Error values are defined as the difference between the reference line. The ±3σ error is 378 mV. Non-linearity is more severe as lower the temperature (0~35℃). The degradation of temperature sensor in 38nm mobile LPDDR2 can be explained compared to the measurement result of 44nm mobile LPDDR2.

One-point calibration is applied for the overall range of the temperature sensor outputs. Fig. 2.7.2 and Fig. 2.7.3 are output and error graphs of the temperature sensor before the calibration. Fig. 2.7.4 and Fig. 2.7.5 are output and error graphs of the temperature sensor after the calibration. 3σ error is reduced by 72 percent after the one-point calibration.

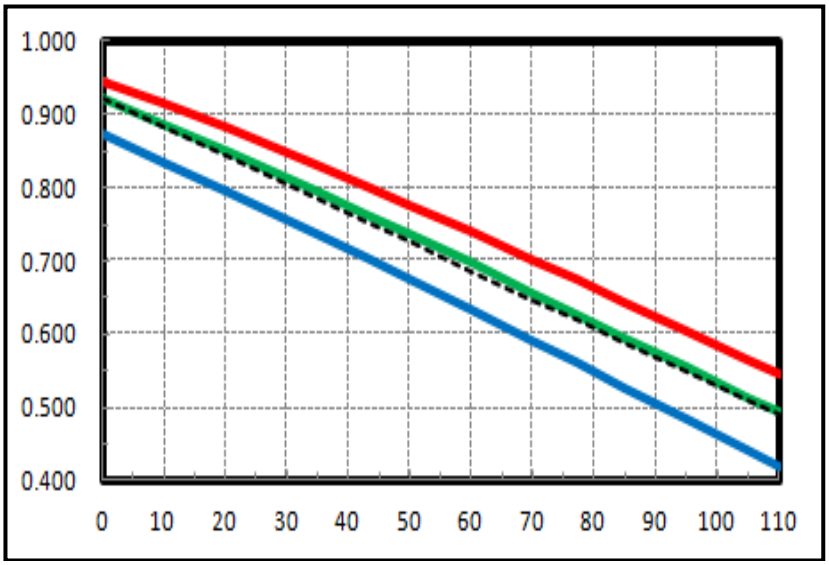

Fig. 2.7.2 V_{TEMP_OUT} TT(green), SS(red), FF(blue) simulated between 0~110℃ before one-point calibration.

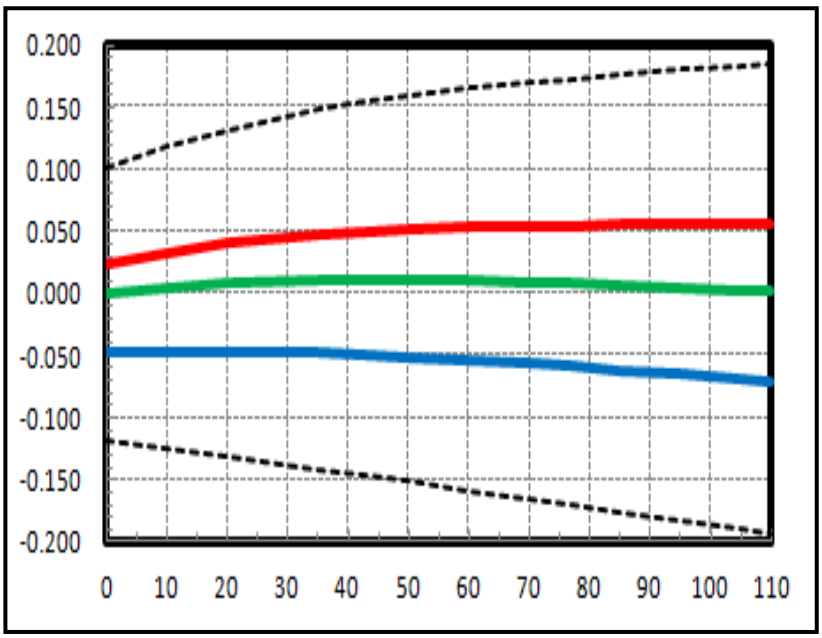

Fig. 2.7.3 V_{TEMP_OUT} 3σ error (378 mV) simulated between 0 ℃ and 110℃ before one-point calibration

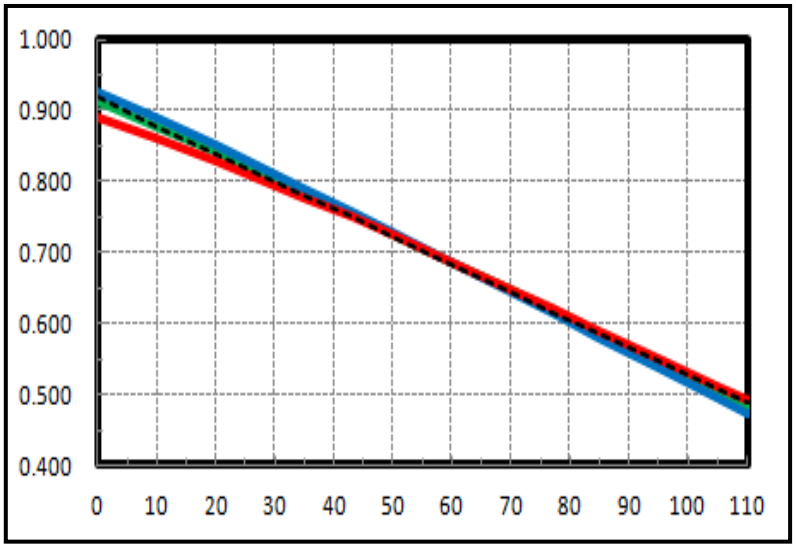

Fig. 2.7.4 V_{TEMP_OUT} with TT(green),SS(red),FF(blue)simulated between 0 ℃ and 110℃ after one-point calibration.

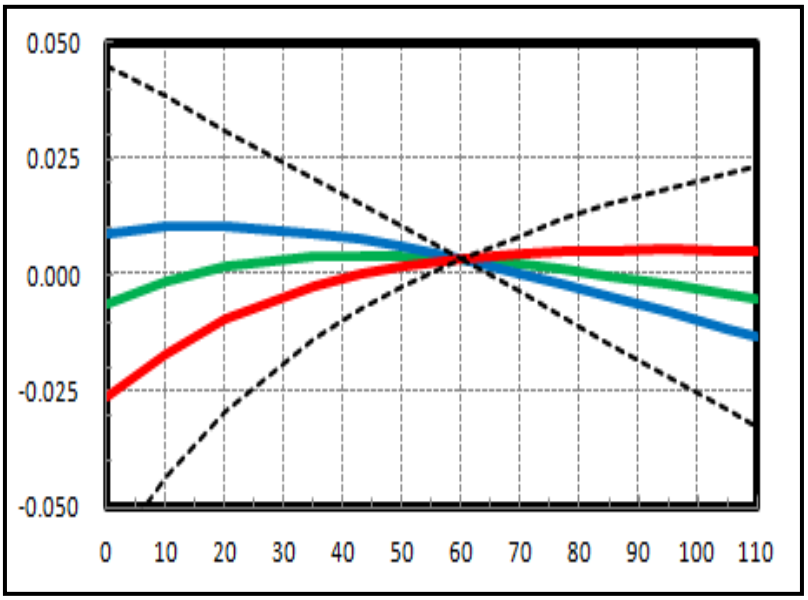

Fig. 2.7.5 V_{TEMP_OUT} 3σ error (106 mV) simulated between 0℃ and 110℃ after one-point calibration.

CHAPTER 3

OPERATIONAL PRINCIPLES OF CMOS TEMPERATURE SENSOR IN MOBILE DRAM

3.1 PRIOR WORKS OF ON-CHIP THERMOMETER IN MOBILE DRAM

As described in the previous sections, the Temperature sensor plays an important role in on-chip thermometer of mobile DRAM. In this thesis, the proposed thermometer employs the novel CTAT voltage generator as the temperature sensor and the simple comparators as the detectors to attain minimal power and area consumption in mobile DRAM self-refresh control. Considering the low power consumption and the low supply voltage of below 1.2V for LPDDR2 products, the BJT is not suitable for the precise control of process parameters and the reduction of active area [14], [15].

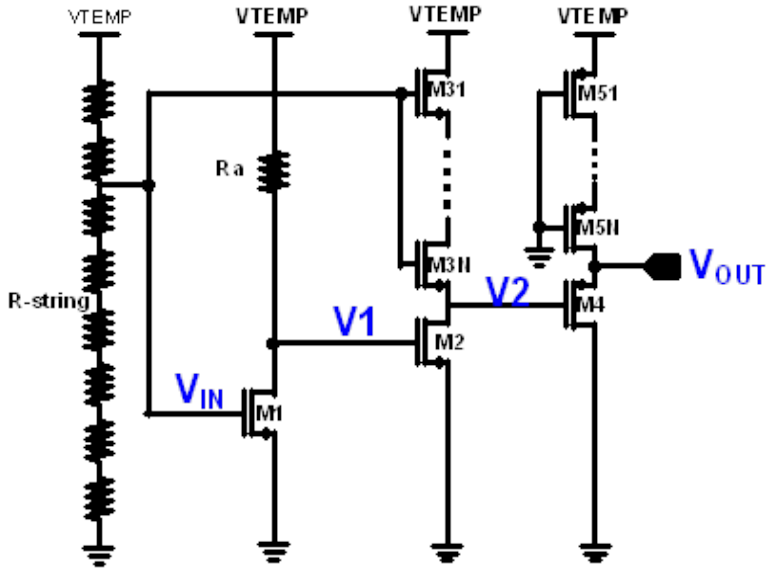

Fig. 3.1.1 Previous temperature sensor circuit

Fig. 3.1.1 shows the schematic of the previous CMOS temperature sensor used in 1.8V mobile DRAM, in which the footer transistors to turn on and off the temperature sensor are omitted for the simplicity. It consists of three stage, n+ active resistor (R_a) and the NMOS transistor (M_1) operating in the triode region for temperature sensing and feedback to next stage input, the common source amplifier composed of NMOS transistor (M_2) which operating in the saturation region with the load NMOS transistor (M_{31} ~M_{3N}) to enhance the output gain and level shifter for optimal V_{TEMP_OUT} which composed of source follower type PMOS (M_4) and the load PMOS transistor (M_{51} ~M_{5N}).

The main role of the first branch is sensing and generating a temperature dependent output level (V_1) which reflect the drain current change of NMOS transistor (M_1) and load resistance change by NMOS transistors (M_{31} ~M_{3N}) with temperature variation.

The main role of second branch is amplification from V_1 to V_2 for enhancement of the temperature gain which composed of the load NMOS transistor (M_{31} ~M_{3N}) and the NMOS transistor (M_2) operating in the saturation region forms the common source amplifier.

The main role of the third branch is generating an optimal output level for satisfying the suitable input offset of next stage comparator and making more linear output level which composed of the load PMOS transistor (M_{51} ~M_{5N}) and the PMOS transistor (M_4) as the source follower.

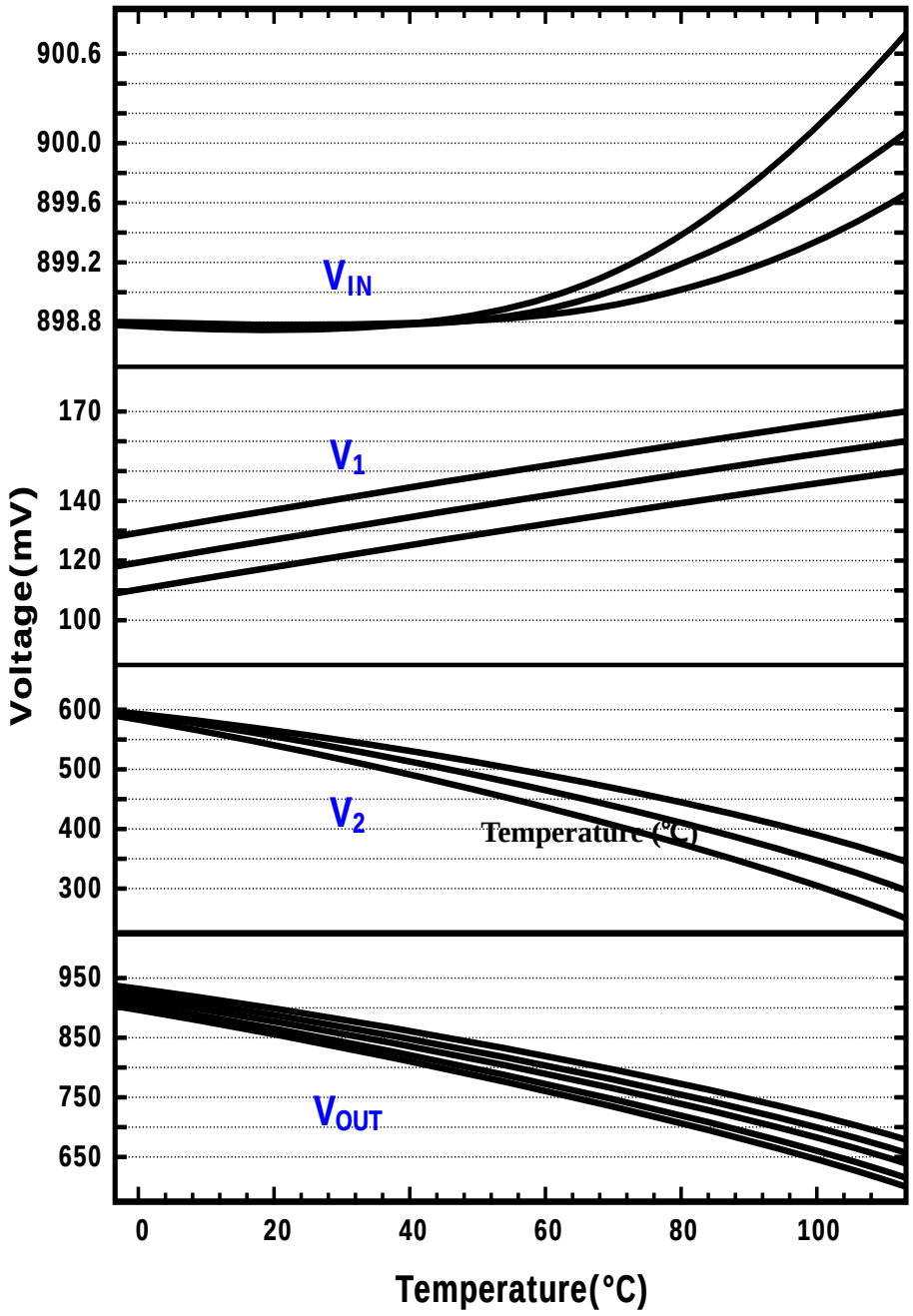

Fig. 3.1.2. Simulation results of temperature dependency of each node as shown in Fig. 3.1.1 with various process skews at supply VDD=1.2V

As shown in in Fig. 3.1.2, the previous temperature sensor can easily affected by process variations of NMOS, PMOS, resistor, results in poor linearity V_{TEMP_OUT} at low temperature and low supply (VDD=1.2V). The output of 1st stage branch (V_1) is relatively linear but 2nd stage & 3rd stage branch output severely deviates from the linearity. Based on further analysis of this type of temperature sensor, these effects can be originated from the fact that (1) the load NMOS transistor (M_{31} ~M_{3N}) is non-linear elements for temperature change, (2) no temperature compensation effect between temperature sensing NMOS transistor (M_1) and NMOS transistor (M_2), (3) the last stage input (V2) dropped by the load NMOS transistor (M_{31} ~M_{3N}) due to V_{GS}- V_{TH} (= V1-V_{TH}), (4) the final stage PMOS source follower is also the nonlinear elements and easily affected by process variation.

To enhance the temperature linearity of temperature sensor output over a wide temperature range and to keep the same linearity slope for all overall process skew corners, the temperature sensor should be composed of temperature linear elements such as resistor and NMOS transistor only. To support of lower supply voltage (VDD=1.2V) mobile LPDDR2 and also to minimize the sensitivity on process variation and maximize the temperature gain of the sensor, the device elements of temperature sensor should be replace with linear and more simple elements such as only NMOS transistors and n+ active resistors.

3.2 PROPOSED CMOS TEMPERATURE SENSOR IN MOBILE DRAM

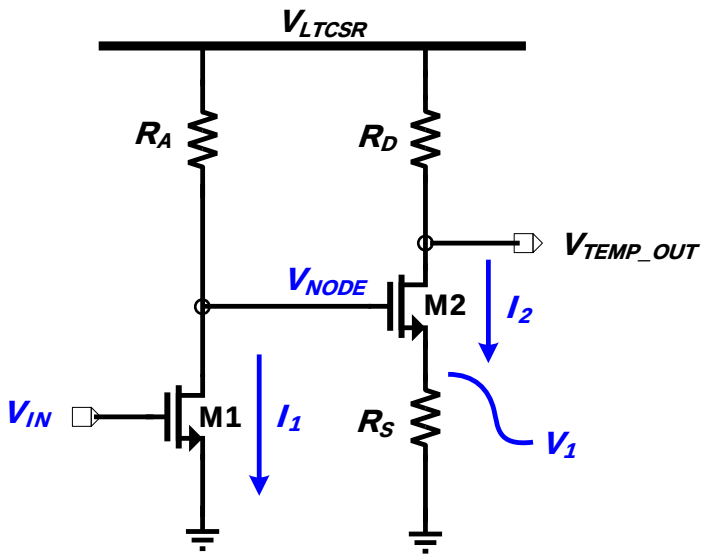

Fig. 3.2.1 Proposed CMOS temperature sensor circuit

Fig. 3.2.1 shows the schematic of the proposed CMOS temperature sensor, in which the footer transistors to turn on and off the sensor are omitted for the simplicity. It consists of the NMOS transistor M_1 operating in the triode region, the NMOS transistor M_2 operating in the saturation region, and the n+ active resistors R_A, R_S, and R_D. V_{LTCSR} is the temperature independent internal supply voltage, which is 1.1V and generated by the voltage regulator which made by bang-gap reference voltage in mobile DRAM. V_{IN} is the input bias voltage, which is properly selected from the resistor ladder for M_1 to operate in the triode region for all process corners and the temperature variation from -40°C to 110°C.

This simple type of CMOS temperature sensor have merits that behavioral model of the output voltage with temperature variation can be easily constructed to eliminate skew variations by adjusting of V_{IN} level by careful selection of resistor value and the threshold voltage (V_{TH}) of NMOS transistors. The proper adjustment by utilizing fuse trimming process also enables the one-point calibration which drastically improves the productivity of post fabrication process for mass production.

In this thesis, the temperature sensor consist only NMOS transistor and resistor which behaves like temperature linear element. By setting an optimal bias point of 1st stage and 2nd stage NMOS part mixed together, the final temperature sensor output became more linear curvature as temperature change.

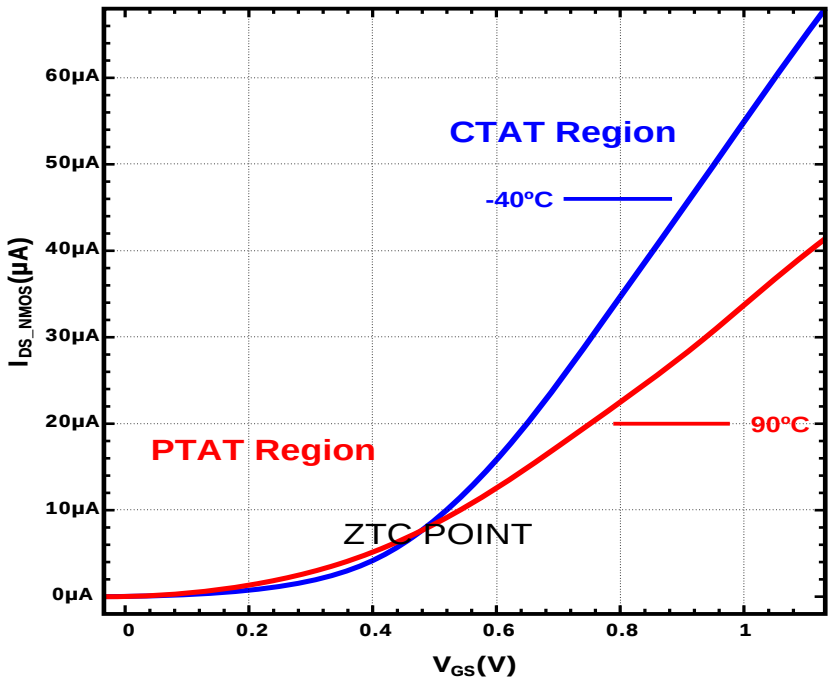

Fig. 3.2.2. Temperature dependent I_{DS_NMOS} with V_{GS}

Fig. 3.2.2 shows the temperature behavior of NMOS transistor for various V_{GS} condition. Since the threshold voltage (V_{TH}) and the mobility (μ_N) of the NMOS transistor are affected by temperature variation, the exact behavior of trans-conductance characteristics of bias point of transistor is important for the design of circuits which required operating in a wide temperature.

The mutual compensation of mobility and threshold voltage of temperature effects in field-effect transistors resulted in the so-called zero temperature coefficient (ZTC) point in MOS trans-conductance characteristics [16].

The combination of two stage NMOS transistors can be more effective when output voltage of each stage can be compensated with respect to all the given parameters, of which the temperature linearity effects on the output voltage could be more enhanced.

The drain output of NMOS transistor will be PTAT or CTAT whether V_{GS} level employed above or below with reference to ZTC point of this NMOS transistor.

V_{NODE} level is desirable as low as possible for considering about ICMR of comparator V_{OUT} over 0.45V. V_{NODE} Level is 0.3~0.4V and V_{NODE} Level is maintaining below the ZTC point at cold temperature

Temperature sensitivity of V_{TEMP_OUT} which means the slope of V_{TEMP_OUT} versus temperature should be high due to the high accuracy, can be obtained by 1st stage V_{IN} over the ZTC point. In design, $V_{IN} > 0.6V$ is desirable due to maximize temperature gain in CTAT point.

Key operation principles are summarized as

1. M1 operates at the above the ZTC point. This means the output of the first branch (V_{NODE}) becomes proportional to the temperature increase (PTAT).
2. M1 operates at linear region which the input level of M1 is properly selected from the resistor ladder for all process corners and the temperature from -40°C to 110°C. Based on implemented process parameters, V_{IN} is set to 0.95V and V_{NODE} is set to 0.17V ~ 0.31V.
3. M2 operates at saturation region (V_{NODE}=0.17V ~ 0.31V/ V_{OUT}=0.45~0.95V). The input of M2(=V_{NODE}) received PTAT effect , M2 Tr. shows negative amplification as temperature goes high. This means V_{OUT} of the sensor's 2nd branch becomes complimentary proportional to the temperature increase (CTAT). The 1^{ST} stage PTAT behavior and 2^{nd} stage CTAT behavior are compensated with each other so that temperature linearity will be more improved in addition to the output load replaced with linear elements such as resistors.
4. The input and output of temperature sensor and temperature slope of these are easily controlled and estimated by appropriate value of resistor components. This makes better productivity of temperature sensor and expected better PVT tolerant characteristics ever than before.

3.3 OPERATION PRINCIPLES OF PROPOSED TEMPERATURE SENSOR

First, we derive the equation of V_{NODE} at the output of the first branch as shown in Fig. 3.2.1. Since M_1 operates in the triode region, the drain current I_1 of M_1 can be expressed in equation (3.1.1).

$$I_1 = \mu_{N1} C_{OX} \left(\frac{W}{L}\right)_1 \left[(V_{IN} - V_{TH1}) V_{NODE} - \frac{V_{NODE}^{\ 2}}{2} \right] \tag{3.1.1}$$

where μ_{N1} is the mobility, $(W/L)_1$ is the aspect ratio, and V_{TH1} is the threshold voltage of M_1.

V_{NODE} is expressed as

$$V_{NODE} = V_{LTCSR} - I_1 R_A \qquad (3.1.2)$$

By substituting the equation (4.1.1) into (4.1.2), we get the closed form solution of V_{NODE} as below

$$V_{NODE} = V_{IN} - V_{TH1} + \frac{1}{\beta_1 R_A} - \sqrt{\left(V_{IN} - V_{TH1} + \frac{1}{\beta_1 R_A} \right)^2 - \frac{2V_{DD}}{\beta_1 R_A}} \tag{3.1.3}$$

where $\beta_1 = \mu_{N1} C_{OX} (W/L)_1$.

Now we consider the temperature dependency of the mobility μ_N, the threshold voltage V_{TH}, and the resistance R. They are expressed as below, where T_0 and T are the reference temperature and the current operating temperature, respectively.

$$\mu_N(T) = \mu_{N0}(T/T_0)^{-m} \tag{3.1.4}$$

$$\beta(T) = \beta_0(T/T_0)^{-m} \tag{3.1.5}$$

$$V_{TH}(T) = V_{TH0} - \alpha_{VTH}(T - T_0) \tag{3.1.6}$$

$$R(T) = R_0\left[1 + \alpha_R(T - T_0)\right] \tag{3.1.7}$$

For the mobility, m is a constant which ranges from 1.2 to 2, and one frequently used value is 2 for n-channel devices. With these relationship, β is also expressed as a function of T, where $\beta 0 = \mu_{N0}C_{OX}(W/L)$. For the threshold voltage, αV_{TH} is a constant which ranges from 1mV/°C to 4mV/°C, and one frequently used value is 2mV/°C [11]. For the resistance, αR is a constant which depends on the type of the resistor.

Substituting Equations (3.1.4) to (3.1.7) into (3.1.3), we can express V_{NODE} as the first term of a Taylor expansion:

$$V_{NODE}(T) \cong \boldsymbol{M} * (T - T_0) + \boldsymbol{N} \qquad (3.1.8)$$

$$\boldsymbol{M} = \alpha_{VTH1} + \frac{1}{\beta_{10} R_{A0} T_0} \left[m - \alpha_R T_0 + \frac{(m - \alpha_R T_0) V_{LTCSR}}{\sqrt{\left(V_{IN} - V_{TH10} + \frac{1}{\beta_{10} R_{A0}}\right)^2 - \frac{2V_{DD}}{\beta_{10} R_{A0}}}} \right.$$
$$\left. - \frac{(1 + \beta_{10} R_{A0} V_{IN} - \beta_{10} R_{A0} V_{TH10})(m - \alpha_R T_0 + \alpha_{VTH1} \beta_{10} R_{A0} T_0)}{\beta_{10} R_{A0} \sqrt{\left(V_{IN} - V_{TH} + \frac{1}{\beta_{10} R_{A0}}\right)^2 - \frac{2V_{DD}}{\beta_{10} R_{A0}}}} \right]$$

$$\boldsymbol{N} = V_{IN} - V_{TH10} + \frac{1}{\beta_{10} R_{A0}} - \sqrt{\left(V_{IN} - V_{TH} + \frac{1}{\beta_{10} R_{A0}}\right)^2 - \frac{2V_{DD}}{\beta_{10} R_{A0}}}$$

From this equation, we can see that V_{NODE} is proportional to the temperature, as long as M1 is operating in triode region. In this linear expression, the slope M of the V_{NODE} against temperature mainly depends on αV_{TH1}, which is not greatly affected by process variation. We can see that the offset N also depends mainly on $V_{IN} - V_{TH10}$, and V_{IN} can easily be adjusted using the resistor ladder shown in Fig. 3.2.1.

Next, we derive the equation of V_{TEMP_OUT} at the output of the second branch. 2nd stage NMOS operates in the saturation region. And its input is V_{NODE} voltage whose voltage is linearly increased by temperature. This NMOS is common source degeneration structure, which gain is small because of small g_m.

Current of 2nd stage NMOS (I_{D2}) and Source Node voltage (V_1) can be expressed as following equation.

Since M_2 operates in its saturation region, the drain current I_2 of M_2 is expressed as

$$I_2 = \frac{1}{2}\mu_{N2}C_{OX}\left(\frac{W}{L}\right)_2\left(V_{NODE} - V_1 - V_{TH2}\right)^2 \quad (3.1.9)$$

where $V_1 = I_2R_S$. V_{TEMP_OUT} is expressed as

$$V_{TEMP\_OUT} = V_{LTCSR} - I_2R_D \quad (3.1.10)$$

By substituting the equation (4.1.9) into (4.1.10), we get the closed form solution of V_{TEMP_OUT} as below

$$V_{TEMP\_OUT} = V_{LTCSR} - \frac{\boldsymbol{R_D}}{\boldsymbol{R_S}}\left[V_{NODE} - V_{TH2} + \frac{1}{\beta_2 R_S}\left\{1 - \sqrt{1 + 2\beta_2 R_S(V_{NODE} - V_{TH2})}\right\}\right] \quad (3.1.11)$$

where $\beta_2 = \mu_{N2}C_{OX}(W/L)_2$.

After substituting the equations (3.1.4) to (3.1.7) into (3.1.11) and applying the Taylor series expansion up to the first order, V_{TEMP_OUT} is expressed as

$$V_{TEMP\_OUT}(T) \cong V_{LTCSR} - \frac{\boldsymbol{R_{D0}}}{\boldsymbol{R_{S0}}}\left[V_{NODE} + \boldsymbol{P}(T - T_0) + \boldsymbol{Q}\right] \quad (3.1.12)$$

$$\mathbf{P} = \alpha_{VTH2} + \frac{1}{\beta_{20} R_{S0} T_0}\left[(m - \alpha_R T_0)\left\{1 - \sqrt{1 + 2\beta_{20} R_{S0}(V_{NODE} - V_{TH20})}\right\}\right.$$
$$\left. + \frac{\beta_{20} R_{S0}\{\alpha_{VTH2} T_0 + (m - \alpha_R T_0)(V_{NODE} - V_{TH20})\}}{\sqrt{1 + 2\beta_{20} R_{S0}(V_{NODE} - V_{TH20})}}\right]$$

$$\mathbf{Q} = -V_{TH20} + \frac{1}{\beta_{20} R_{S0}}\left[1 - \sqrt{1 + 2\beta_{20} R_{S0}(V_{NODE} - V_{TH20})}\right]$$

In this linear expression, P of the V_{TEMP_OUT} mainly depends on αV_{TH2}, which is not severely affected by the process variation. Q is mainly depends on $- V_{TH20}$. In both coefficients, the effect of nonlinearities including the temperature dependency of mobility is mitigated by the large value of R_{S0}. By substituting the equation (3.1.8) into (3.1.12), we finally get the linear expression of V_{TEMP_OUT}.

$$V_{TEMP\_OUT}(T) \cong V_{LTCSR} - \frac{R_{D0}}{R_{S0}}[\boldsymbol{M}(T - T_0) + \boldsymbol{N} + \boldsymbol{P}(T - T_0) + \boldsymbol{Q}] \qquad (3.1.13)$$
$$= V_{LTCSR} - \frac{R_{D0}}{R_{S0}}[(\boldsymbol{M} + \boldsymbol{P})(T - T_0) + \boldsymbol{N} + \boldsymbol{Q}]$$
$$\cong V_{LTCSR}$$
$$- \frac{R_{D0}}{R_{S0}}\left[\left(\alpha_{VTH1} + \alpha_{VTH2} + e_{slope}\right)(T - T_0)\right.$$
$$\left. + \left\{V_{IN} - (V_{TH10} + V_{TH20}) + e_{offset}\right\}\right]$$

Equation (3.1.13) dictates that V_{TEMP_OUT} is linearly decreasing with respect to temperature increasing. In this case, the slope of V_{TEMP_OUT} is mainly dependent on the value of αV_{TH1} plus αV_{TH2} and the ratio of R_{D0} and R_{S0}. Since these values are fairly

tolerant to the process variation, the slope of V_{TEMP_OUT} can be well controlled by the designed value.

The DC level of V_{TEMP_OUT} is adjustable by selecting a proper value of V_{IN}, of which the control can be easily applied after the fabrication. These features enable us to use one-point calibration, which greatly reduces the time and the complexity of the mass production issues. The simulation results from the temperature sensor circuit design parameter input, which compared to more easy and simple linear approximation with Taylor's series expansion as shown in Fig. 3.3.1. From the above the equations (3.1.8) to (3.1.12), in case of R_D and R_S using same type of resistors, V_{TEMP_OUT} is linearly decreasing because temperature coefficient of the resistor is equal. Finally, output voltage of thermometer is determined by k_{n1}, k_{n2}, V_{IN}, R_D, R_S, R_A.

The simulation results of the linear approximation, as shown in Fig. 3.3.2, coincide with calculation results from the exact equations of V_{NODE} and V_{TEMP_OUT} as shown in Fig. 3.3.1.

Initial design given by those equations relies on the square-law model of the transistor cannot be directly translated into the design with the modern deep submicron process. Final solution quickly by trimming the values of R_{D0} and R_{S0} to adjust the slope and the values of R_{S0} and V_{IN} to adjust the offset

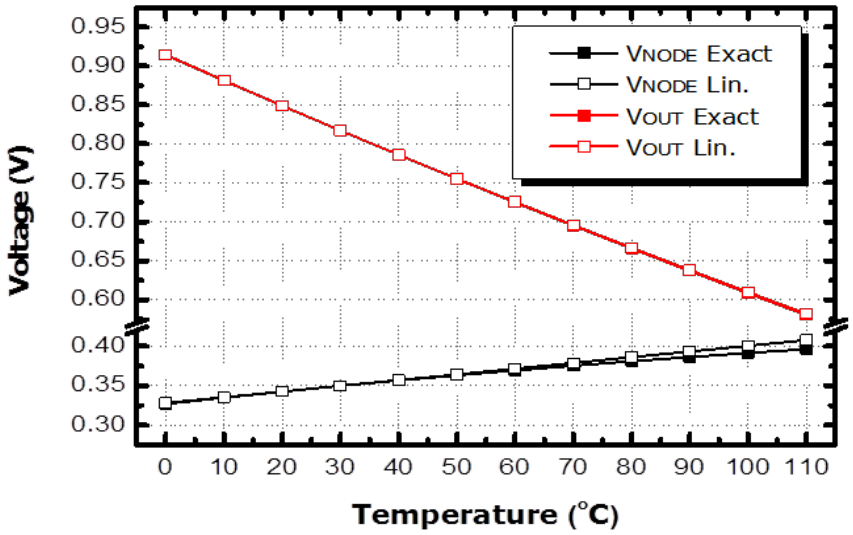

Fig. 3.3.1 Calculation results of the temperature sensor from exact equation comparing with linear approximation by Taylor's series expansion.

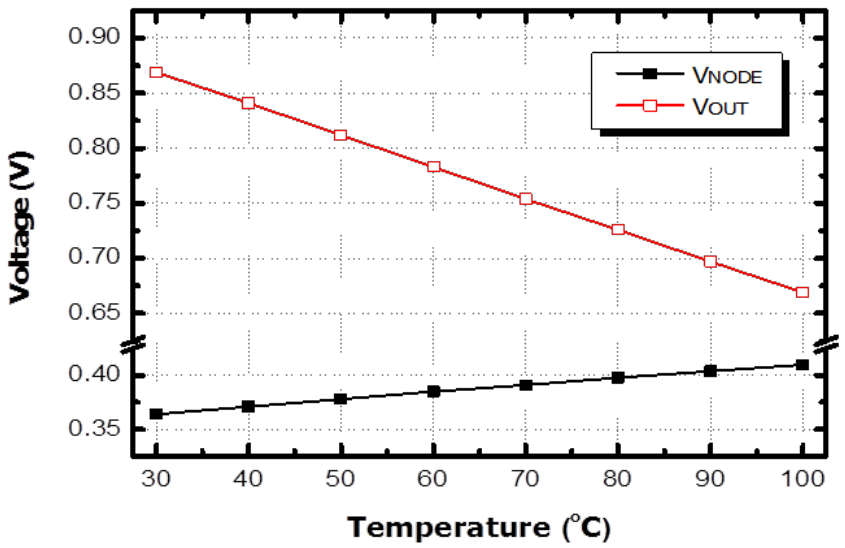

Fig. 3.3.2. Simulation results of the temperature sensor.

3.4 PROPOSED FOLDED TYPE TEMPERATURE SENSOR

As technology change from 44nm to 29nm DRAM process, the proposed temperature sensor also shows limited operation range due to the temperature dependency of the mobility μ_N, the threshold voltage V_{TH}, and the resistance of resistor (R) are changed by technology scaling down effect.

Main problem is the sensor output level is so high when implemented with design parameters of 29nm DRAM process. To support more wide temperature range and lower supply voltage operation, the maximum temperature sensor output level should be pulled down. For 1.0V supply voltage, the V_{LTCSR} level goes to 0.8V, then the maximum temperature sensor output level should be below the 0.8V at lowest operation temperature (-40℃).

For operating at lower supply voltage and enhancement of temperature sensor output linearity, the maximum temperature sensor output voltage is to be lowered enough. But the reduction of maximum temperature sensor output resulted in degrade of sensitivity.

In this thesis, the new proposed folded type temperature sensor which is very effective not only lowering the maximum sensor output level but also maintain the same temperature sensitivity when the boundary problem can be easily solved or non-critical at the vicinity of the folding temperature. The sensor output voltage level could be lowered when utilize the multiple folding, but inevitably adding a folding component cause the design complexity and consumes large area and power.

As mentioned previous section, the proposed temperature sensor circuit can be

expressed by mathematically, the NMOS transistors and resistor behavior should be analyzed for corresponding process technology. If the folded type temperature sensor with minor device element change is possible, the performance of temperature sensor can be easily reconfigurable without additional circuit block or device element.

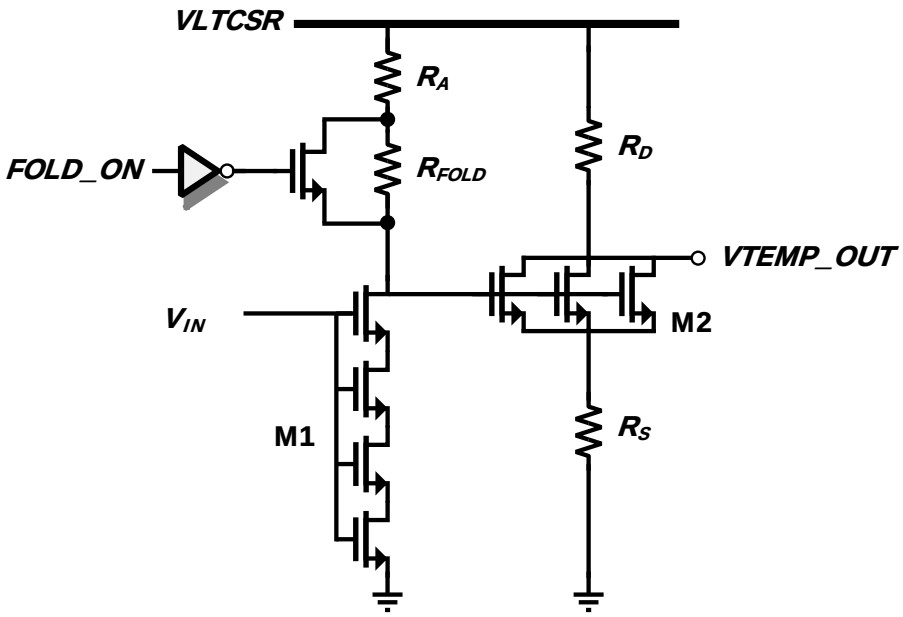

Fig.3.4.1. Proposed folded type temperature sensor

The simplified schematic of the newly proposed folded type temperature sensor is as shown in Fig.3.4.1. This folded type temperature sensor circuit is almost same as previous temperature sensor except for adding a NMOS switch transistor to change the load resistor value controlled by FOLD_ON signal at certain temperature below. As compared to Fig.3.1.1, the FOLD_ON signal which changes the load resistor value of 1st stage input NMOS transistor is added when temperature goes down below 35°C.

Prior to the circuit design of the folded type temperature sensor, the key design parameters should be define and executes the spice simulation based on the target of temperature range and operation V_{DD_SENSOR} under PVT variations. In this thesis, the target of operating temperature is from -40℃to 110℃ at the operation V_{DD_SENSOR} = 1.0 V and V_{LTCSR} = 0.8 V, but the temperature sensor sensitivity keep the same performance (~3.5mV/℃) as previously described temperature sensor type.

When the supply voltage condition is set to 1.0V, then V_{LTCSR} level is 0.8V. V_{REFLT0}, which is came from Resistor Deck, uses 0.4V voltage to generate 0.8V voltage. Even if V_{LTCSR} voltage is going down to 0.8V, circuit operation must to be compatible in case of the unfolded type temperature sensor at V_{LTCSR} =1.1V.

The input voltage of 1st stage NMOS transistor should be high for operating at deep triode region and 2nd stage NMOS transistor of source degeneration amplifier should be operate at saturation region for high temperature linearity. For considering about the source degeneration amplifier, increasing NMOS (W/L) and I_{DS} current can make increasing gm but decreasing the output level. To improve the linearity of temperature sensor output, the gain of 2nd stage source degeneration amplifier should be insensitive to gm. To satisfy the condition for $R_S \gg \frac{1}{g_m}$, R_S should be increase for the purpose of all considerations above.

But to improve the sensitivity or slope of temperature output with respect to temperature change, R_S should be decrease. So, there exists trade-off between the gain of 2nd stage and the sensitivity of temperature sensor in terms of R_S.

Considering about the temperature linearity, at first the W/L of NMOS transistor is fixed then finding the optimal R_A & R_D value to meet the overdrive voltage of 2nd stage NMOS in saturation region. Total area of resistor used in circuit linearly increases with the R_S value.

To adjust for same output inclination over the entire section, the number of folding and folding section is divided. In this thesis, the temperature output is divided into 2 parts: -40℃~35℃ (left) and 35℃~110℃ (right) as shown in Fig. 3.4.2.

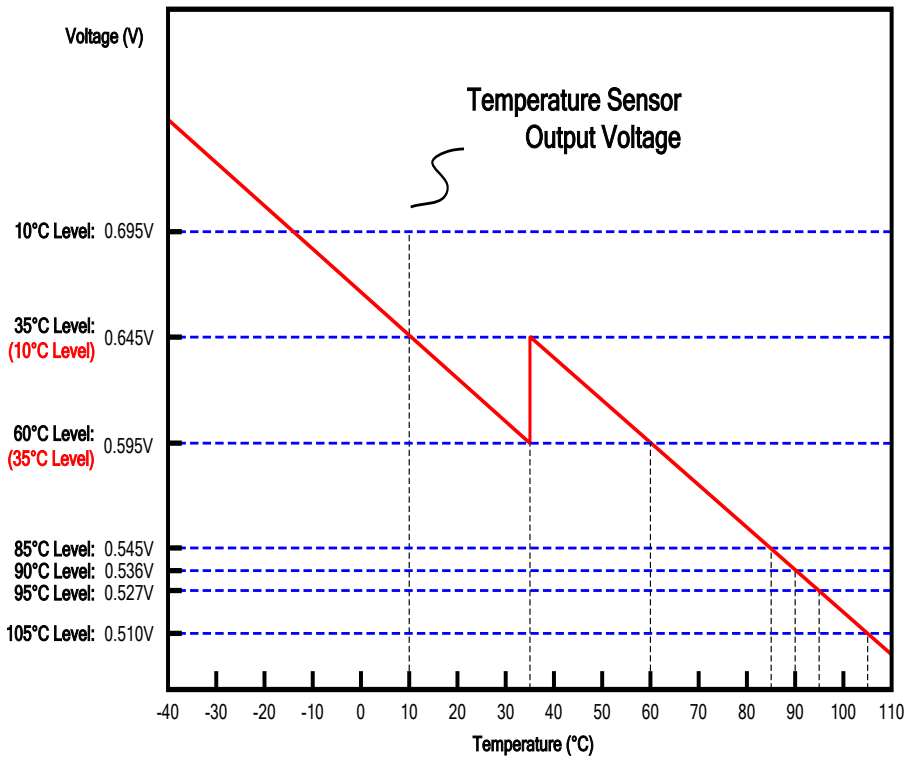

Fig. 3.4.2. Temperature dependence of the sensor output voltage and the reference levels with supply VDD=0.8V

Following simulation results as illustrated in Fig. 3.4.2 is performed by the top level, including core circuit and peripheral circuit in TT condition. Temperature sensor output and sensitivity are measured between -40℃ and 110℃. Temperature sensor has two output characteristics for each temperature region, the plot against the temperature shows 3.5mV/℃ which means temperature sensitivity and ±3% accuracy in overall temperature region. At 60℃, worst case ±3σ error after the one-point calibration is 0.0962 V.

There is large variation of characteristics, in accordance with the process and voltage variation. Performance of the temperature sensor can be improved if those variations are reduced. In case of the other corners, it has larger offset in TT basis. Moreover, because each section has different offset value, one-point calibration which calibrate only with the offset has a limitation in reducing the error. So, to reduce more ±3σ error, R_A and R_D use adjustable resistance to one-point trimming at the standard temperature.

CHAPTER 4

PERIPHERAL CIRCUITS OF THERMOMETER

In this section, the peripheral circuits of the temperature sensor will be described. To support the 1.0V below, the existing peripheral circuit can be optimized for low supply voltage condition. The peripheral circuits of the temperature sensor are composed of voltage regulator which providing from temperature independent supply voltage to the temperature sensor, resistor deck which providing input bias voltage of temperature sensor, comparator which comparing temperature sensor output voltage with reference temperature level, folding control block which change the load resistor value of 1st stage of temperature sensor.

4.1 REGULATOR FOR V_{LTCSR} SUPPLY

The simplified block diagram of regulator is shown in Fig. 4.1.1.

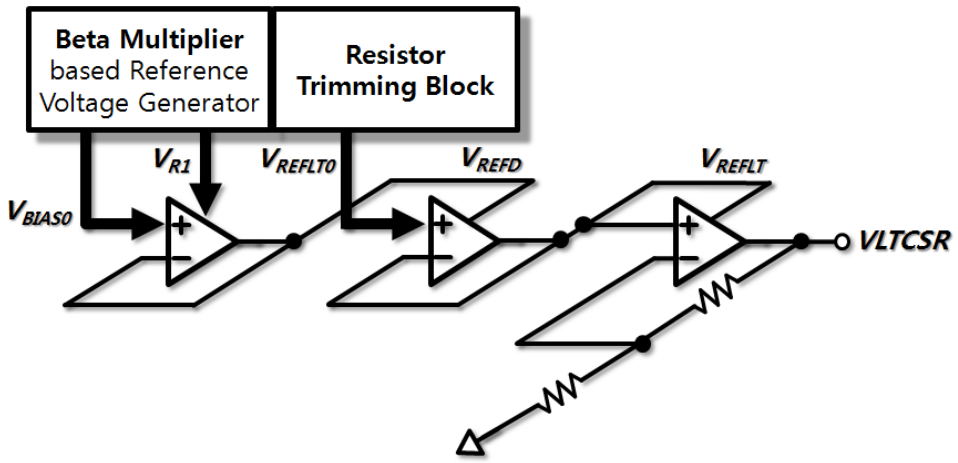

Fig. 4.1.1 Regulator for supplying voltage to the temperature sensor

V_{REFD} generated by input (V_{BIAS0}) and bias voltage (V_{R1}) which comes from the Beta Multiplier reference voltage through unit gain buffer. The output of this unit gain buffer (V_{REFD}) and V_{REFLT0} which provided by the Resistor Trimming Block generates V_{REFLT}. V_{LTCSR} voltage is generated from the voltage regulator with V_{REFLT} bias voltage. The target level of V_{LTCSR} is 0.8V in DC as V_{REFLT0} is changed from 0.55V into 0.4V.

As supply voltage changes from 1.2V to 1.0V, the peripheral circuits should be carefully checked for DC bias level of each circuit block from the DC analysis and gain (A_G) & band with (BW) changes of Unit Gain Amplifier and Regulator from AC analysis

4.1.1 DC ANALYSIS

The simulation results of main node voltages (V_{BIAS0}, V_{R1}, V_{REFD}, V_{REFLT}, V_{LTCSR}) at three temperatures (-40℃, 25℃, 90℃) from DC analysis are summarized under three different process and two operating voltage variations as shown in Table. 4.1.1.

Table. 4.1.1 DC level of peripheral circuit with process and supply voltage variations.

V_{DD2} (V)		1.0			1.2		
Temperature (℃)		-40	25	90	-40	25	130
V_{BIAS0}	FF	0.577	0.568	0.557	0.577	0.568	0.557
	TT	0.608	0.600	0.590	0.608	0.600	0.589
	SS	0.638	0.631	0.622	0.638	0.631	0.622
V_{R1}	FF	0.530	0.512	0.491	0.530	0.512	0.491
	TT	0.560	0.542	0.523	0.560	0.543	0.523
	SS	0.589	0.572	0.554	0.590	0.573	0.555
V_{REFD}	FF	0.577	0.568	0.557	0.577	0.568	0.557
	TT	0.608	0.600	0.590	0.608	0.600	0.590
	SS	0.638	0.631	0.622	0.638	0.632	0.623
V_{REFLT}	FF	0.400	0.400	0.400	0.550	0.550	0.550
	TT	0.400	0.400	0.400	0.550	0.550	0.550
	SS	0.400	0.400	0.400	0.550	0.550	0.550
V_{LTCSR}	FF	0.795	0.796	0.798	1.098	1.100	1.101
	TT	0.795	0.796	0.797	1.098	1.099	1.100
	SS	0.794	0.795	0.796	1.079	1.078	1.078

In case of supply voltage=1.0V, V_{REFLT0} = 0.4 V is optimal level for generating V_{LTCSR} = 0.8 V and V_{REFLT0} = 0.55 V is optimal level for generating V_{LTCSR} = 1.1V at supply voltage=1.2V. As shown in Table.5.1.1., V_{BIAS0}, V_{R1}, V_{REFD} has a same value regardless of the two supply voltage levels.

4.1.2 AC ANALYSIS

The gain and bandwidth of two unit gain buffers and regulator are simulated at three temperatures (-40℃, 25℃, 90℃) under three different process with two supply voltage conditions. As shown in Fig.4.1.2 and Fig.4.1.3, almost the same behavior resulted from before and after the trimming process based on AC analysis.

Gain and Bandwidth of each block is acceptable regardless of the supply voltage from 1.2V to 1.0V. The simulation results of AC output characteristics of peripheral circuit are summarized in Table.4.1.2.

Table. 4.1.2. Peripheral circuit's AC performance according to the PVT Variation and the supply voltage Level

Performance		Gain (dB)		3db BW (Hz)		Unit Gain BW (Hz)	
Supply voltage (V)		1.0	1.2	1.0	1.2	1.0	1.2
Regulator	TT	43.9	46.8	1.98E+04	9.59E+04	6.22E+05	3.94E+06
	FF	46.8	51.2	1.64E+04	9.95E+04	6.62E+05	5.79E+06
	SS	39.9	-65.7	2.14E+04	X	5.74E+05	X
1st Stage Unit Gain Buffer	TT	68.7	70.6	4.80E+03	4.03E+03	3.15E+06	3.23E+06
	FF	71.9	73.2	3.67E+03	3.23E+03	2.55E+06	2.60E+06
	SS	63.7	67.6	6.90E+03	5.06E+03	3.41E+06	3.55E+06
2nd Stage Unit Gain Buffer	TT	71.7	71.7	1.38E+04	6.93E+03	6.75E+06	7.04E+06
	FF	74.0	73.9	1.36E+04	6.10E+03	6.77E+06	6.80E+06
	SS	69.2	69.3	1.43E+04	7.87E+03	6.31E+06	6.85E+06

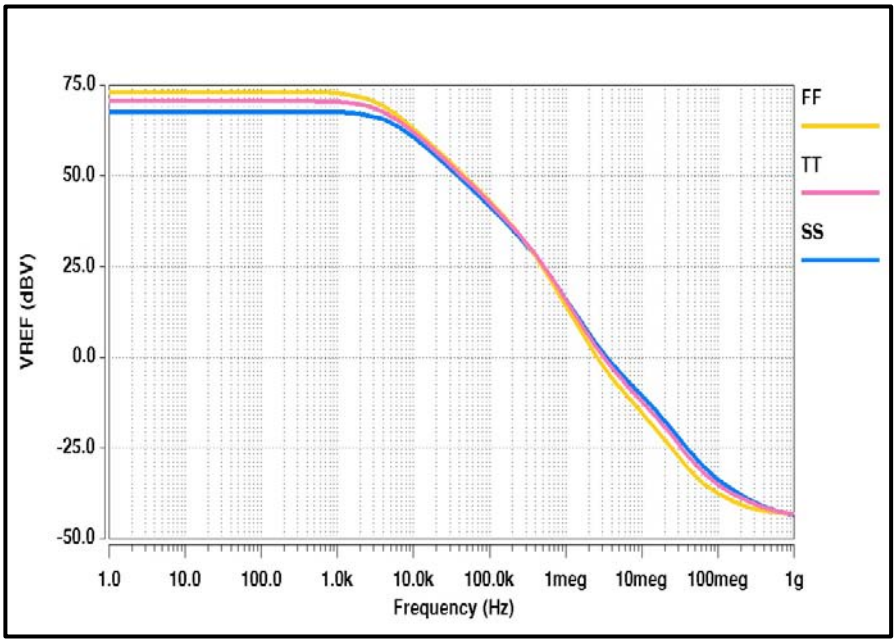

Fig. 4.1.2.1 AC analysis of 1st Stage Unit Gain Buffer Output (V_{DD2I} = 1.2 V)

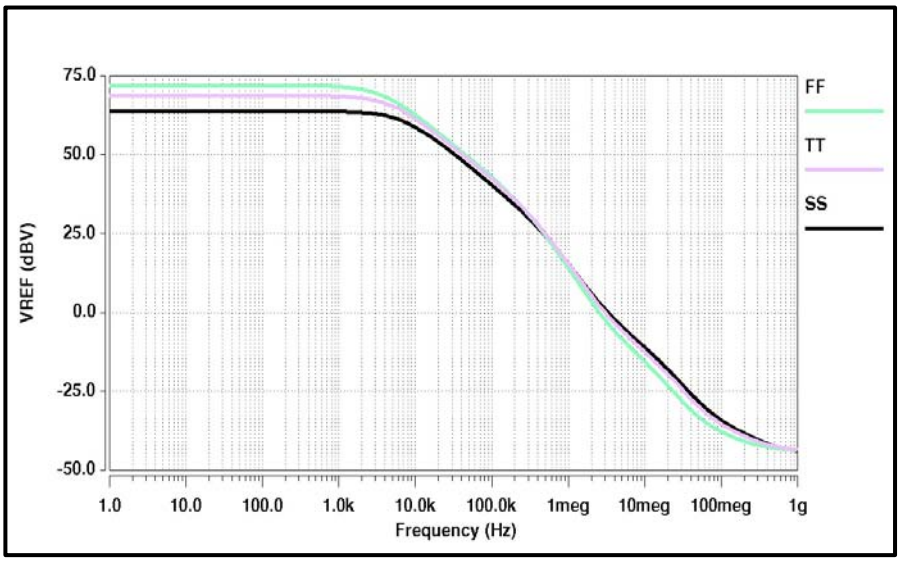

Fig. 4.1.2.2 AC analysis of 1st Stage Unit Gain Buffer Output (V_{DD2I} = 1.0 V)

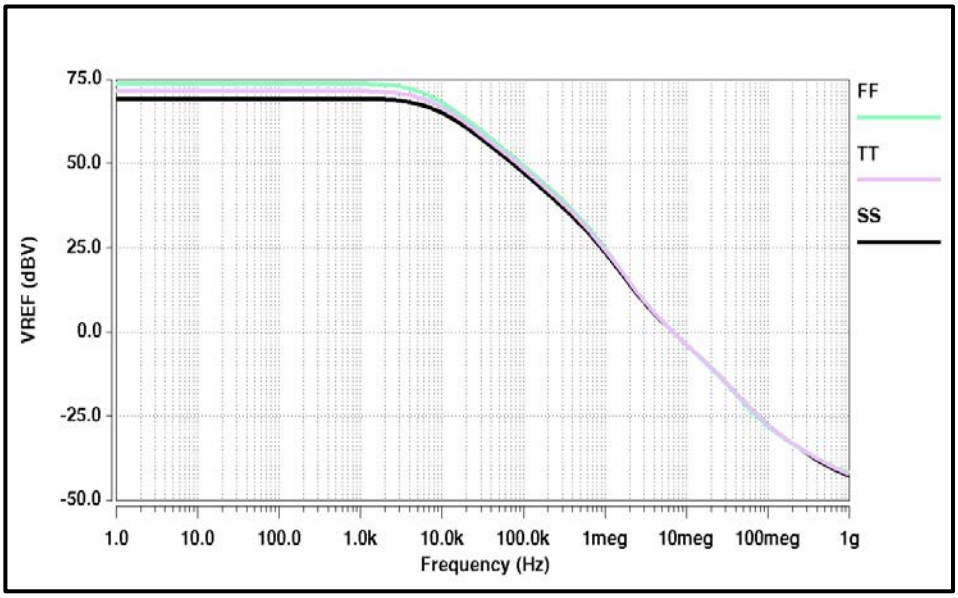

Fig. 4.1.2.3 AC analysis of 2nd Stage Unit Gain Buffer Output (V_{DD2I} = 1.2 V)

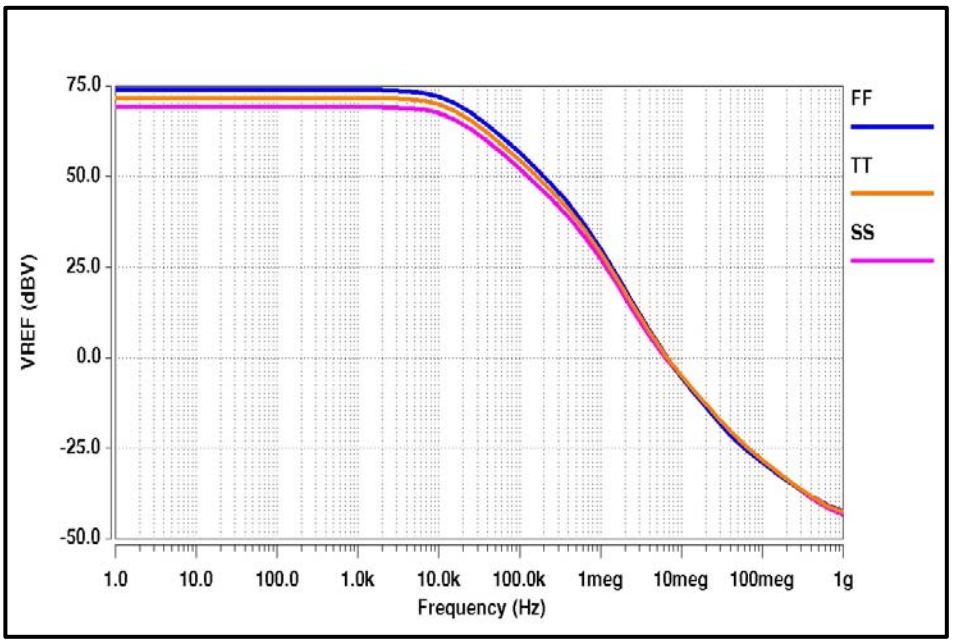

Fig. 4.1.2.4 AC analysis of 2nd Stage Unit Gain Buffer Output (V_{DD2I} = 1.0 V)

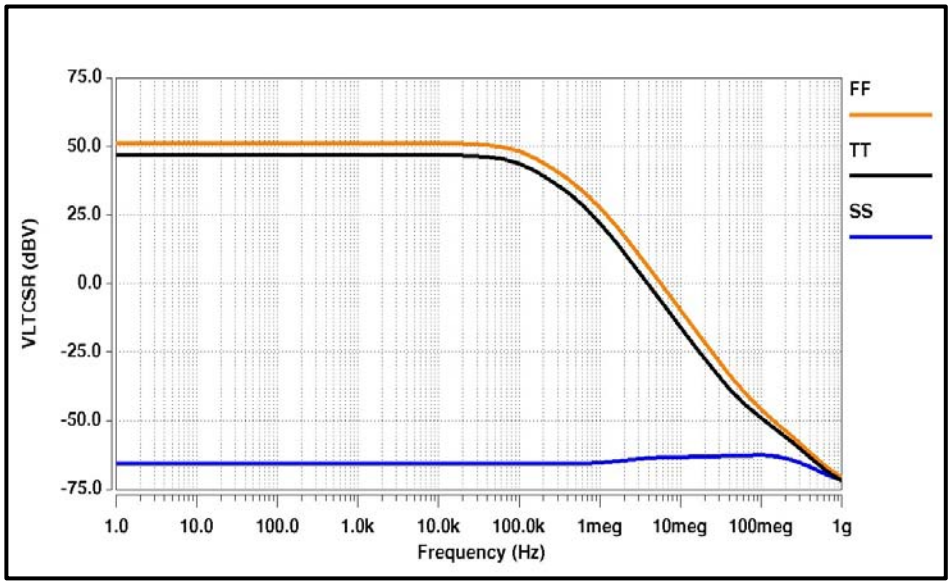

Fig. 4.1.2.5 AC analysis of voltage Regulator Output (V_{DD2III} = 1.2 V)

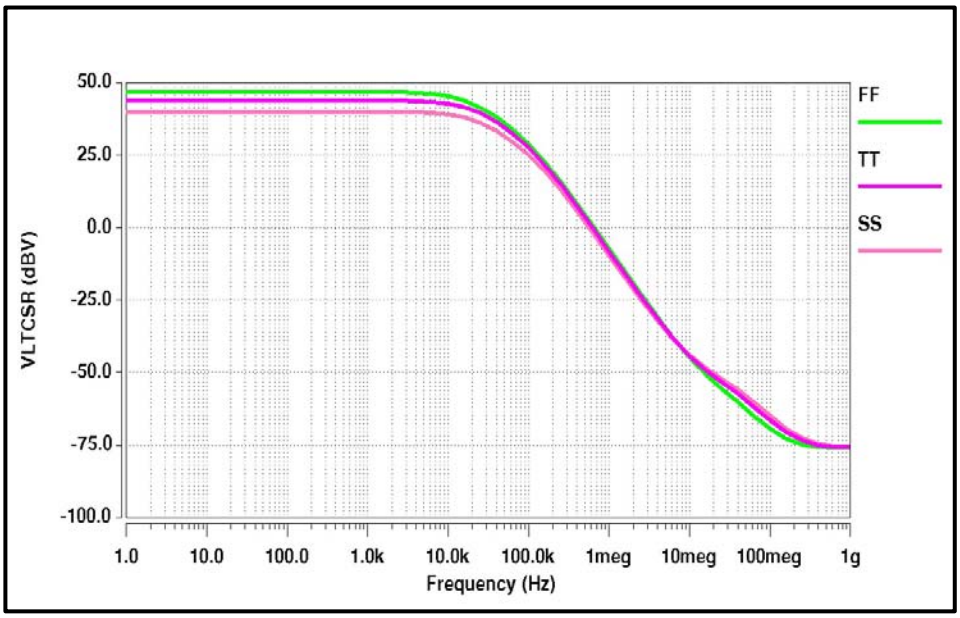

Fig. 4.1.2.6 AC analysis of voltage Regulator Output (V_{DD2I} = 1.0 V)

4.2 RESISTOR DECK

Resistor Deck provides the reference voltage of comparator at each designated temperature (35℃, 60℃, 85℃, 90℃, 95℃, 105℃). As supply voltage drops from 1.2V to 1.0V, more precise control of voltage is capable even if the voltage range is limited boundary. The one resistor trimming steps reduced from 6.2mV @1.2V to 4.5mV @1.0V due to the supply voltage pulled down, but the control resolution is increased as shown in Fig. 4.2.1 and Table. 4.2.1

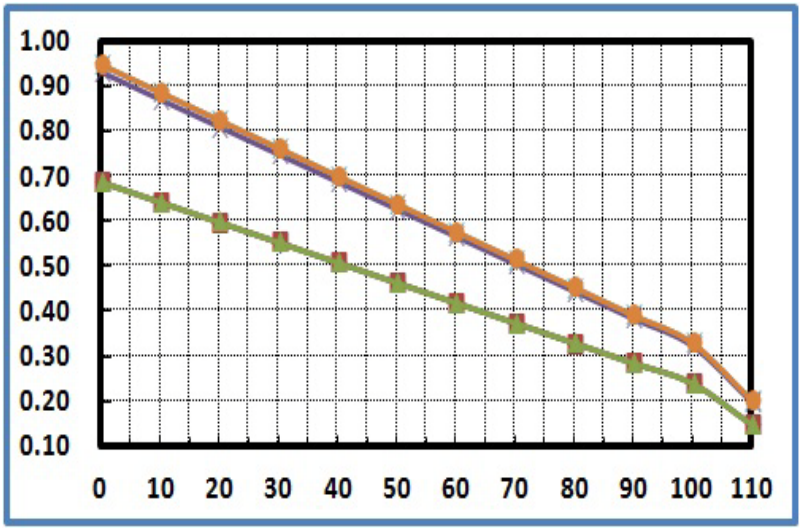

Fig. 4.2.1 Node number (horizontal) vs. Voltage level(vertical) graph
(∵ V_{DD2I} = 1.0 V(below), V_{DD2I} = 1.2 V(above))

Table. 4.2.1. Comparing Resistor Deck Spec.

Supply Voltage (V)	1.0	1.2
Minimum Voltage (V)	0.15	0.2
Maximum Voltage (V)	0.69	0.93
Voltage Step (mV)	4.5	6.2

4.3 COMPARATOR

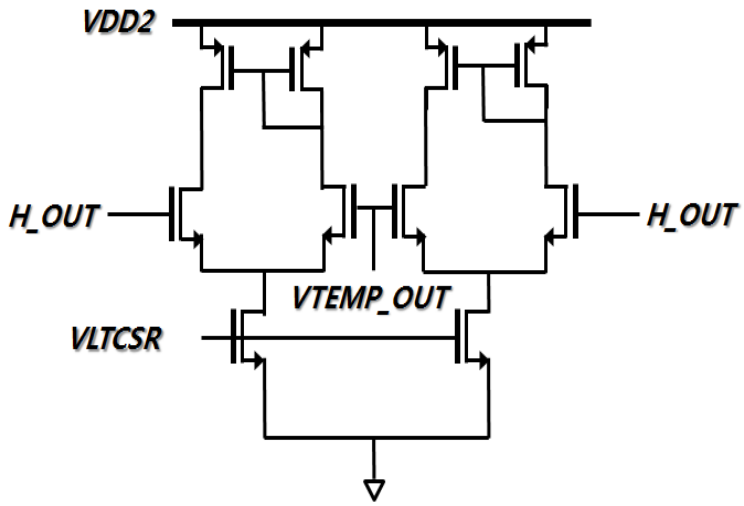

Fig. 4.3.1 Comparator circuit diagram of proposed on-chip thermometer.

Comparator as shown in Fig. 4.3.1 determines temperature range of the real time on-chip temperature by comparing temperature sensor output voltage with preset level of reference temperature. For operating at supply voltage =1.0V or below, resizing of two sink transistors whose input voltage is V_{LTCSR} have to be done. The offset of input differential pair of the comparator determines the critical for operating in low supply voltage condition. To confirm the offset margin of comparator, one terminal of the input differential pair is fixed and the other part input is sweeping.

The simulation result of comparing random input and core circuit of temperature sensor output voltage shows that the accurate temperature detection is accomplished through a comparator as shown in Fig. 4.3.2 and in Fig. 4.3.3.

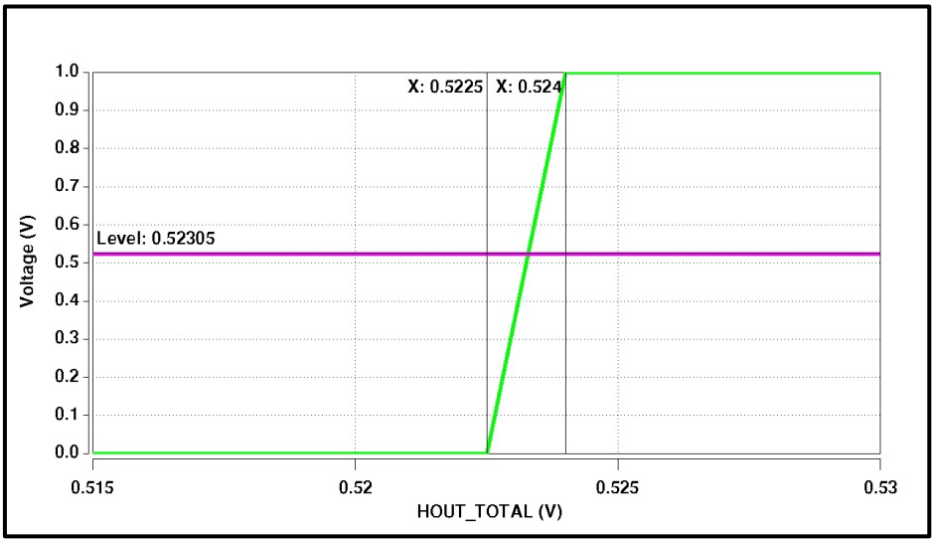

Fig 4.3.2 Comparator offset when temperature is lower than 60 degrees

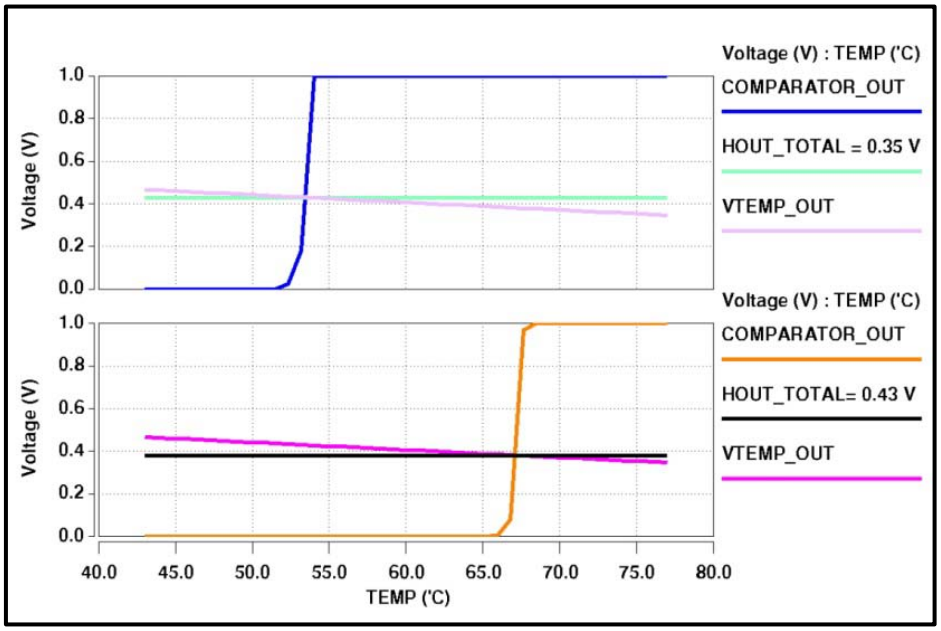

Fig. 4.3.3 Comparator offset when temperature is higher than 60 degrees

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 ON-CHIP CMOS THERMOMETER IN 44NM CMOS PROCESS FOR MOBILE LPDDR2

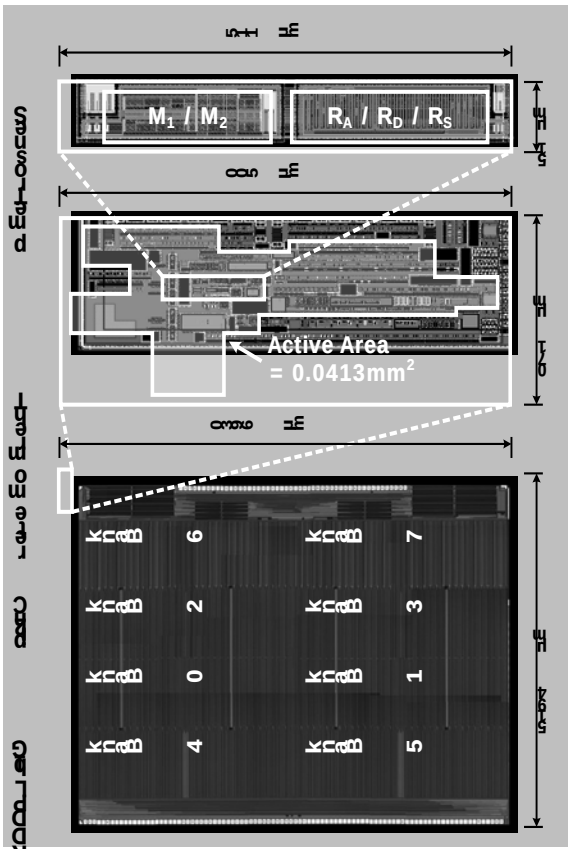

Fig. 5.1.1 The microphotograph of the4xm mobile LPDDR2 chip and the magnified layouts of the thermometer and the temperature sensor.

The proposed thermometer was designed and fabricated on a mobile LPDDR2 in a 44nm DRAM process. Fig. 5.1.1 shows a microphotograph of the fabricated chip, with its thermometer located at the upper left corner. The on-chip thermometer incorporating in mobile LPDDR2 chip is fabricated in a 44nm DRAM process with a supply of 1.1V. Temperature sensor incorporating in 44nm mobile LPDDR2 is shown in Fig. 5.1.2.

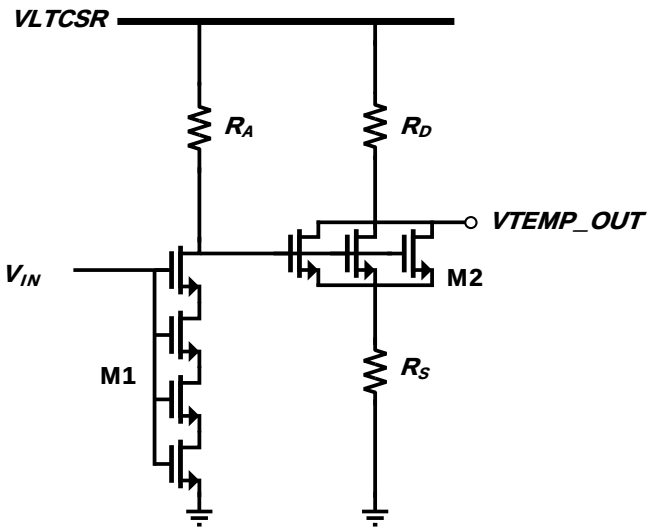

Fig. 5.1.2 Temperature sensor incorporating in 44nm mobile LPDDR2

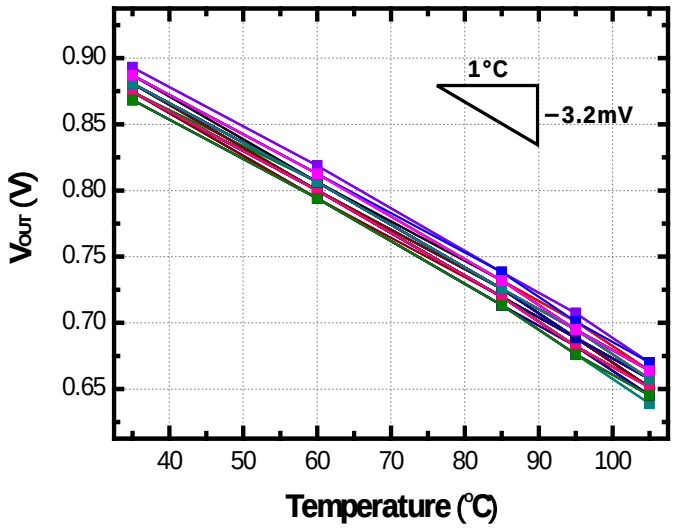

Fig. 5.1.3 Measured output voltages from 61 samples of the sensor circuit before one-point calibration, with their average slope.

The variation of output voltages against temperature for 61 samples of the sensor circuit is shown in Fig. 5.1.3. Between 35°C and 105°C, the sensors exhibit a temperature sensitivity of −3.2mV/°C on average, which is not affected by process variation. With this gain, the 6.2mV step of the resistor ladder provides a resolution of 1.94°C.

The output voltages of the 61 samples after the one-point calibration are shown in Fig. 5.1.4. The temperature sensitivity is unchanged since one-point calibration simply adjusts the DC level of each output. The uniformity of the temperature sensitivity, provided by the theoretical analysis, permits one-point calibration. Since the refresh rate needs to be precisely controlled at higher temperatures, the target temperature for the calibration is chosen to set to 85°C. The voltage error after calibration, which ranges between −8.5mV

and +4.53mV, corresponding to a temperature error between −1.42°C and +2.66°C as shown in Fig. 5.1.5.

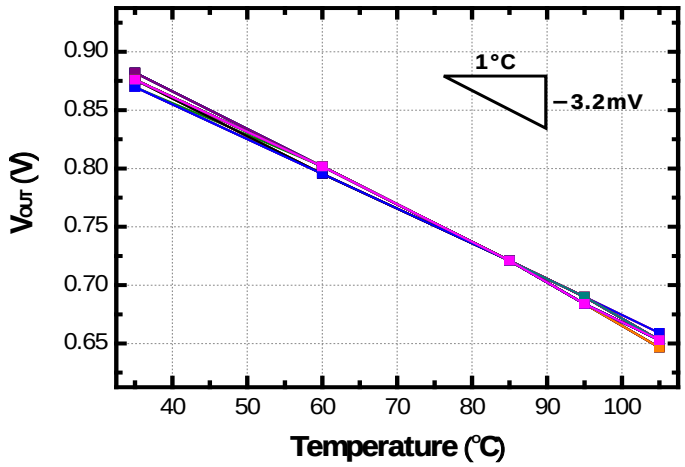

Fig. 5.1.4 Measured output voltages from 61 samples of the sensor circuit after one-point calibration, with their average slope.

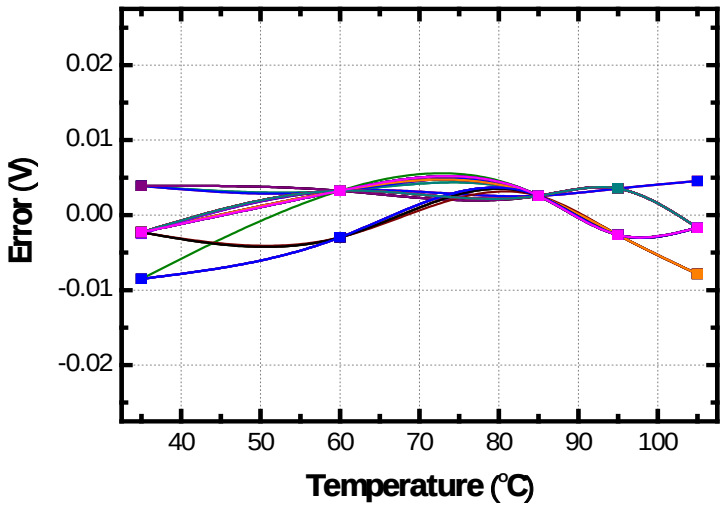

Fig. 5.1.5 Measured voltage error after the one-point calibration.

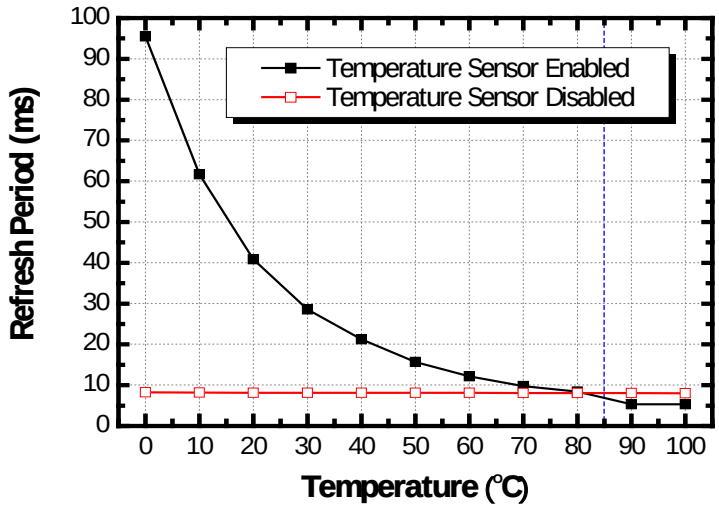

Fig. 5.1.6 Refresh period against temperature with and without refresh period control.

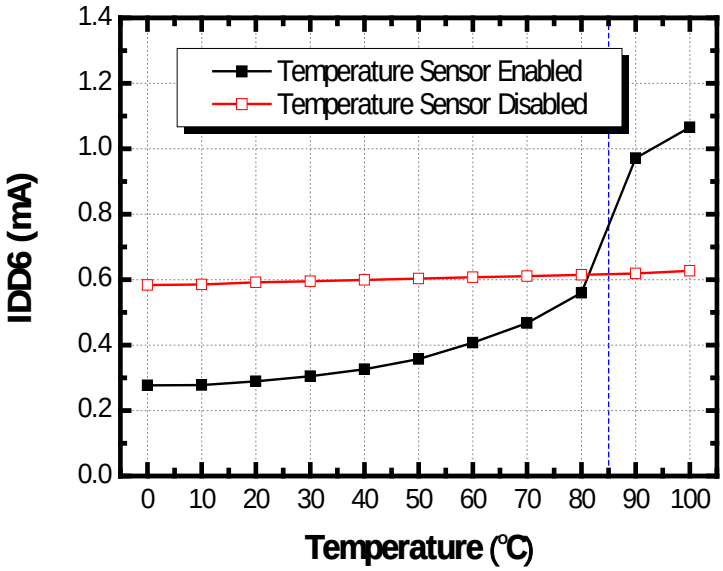

Fig. 5.1.7 IDD6 current against temperature with and without refresh period control

Fig. 5.1.6 shows how our thermometer changes the self-refresh period of the LPDDR2 chip. The self-refresh period is designed to be 8μs around 85°C. With the sensor disabled, it stays 8μs at this length; but with the sensor enabled, the period extends to 95μs as the temperature drops to 0°C. A longer refresh period reduces the temperature-dependent self-refresh current IDD6, as shown in Fig. 5.1.7. IDD6 stays around 0.6mA when there is no refresh control, but when self-refresh control is applied it drops to 0.33mA at 40°C and 0.28mA at 0°C. The self-refresh period should be shortened at high temperatures so that DRAM cells retain their data. With the sensor disabled, the period stays at 8μs, which has the risk of data loss at higher temperature. With the sensor enabled, the period is shortened to 4μs, which prevents data loss at the cost of increased IDD6. On chip Thermometer based Refresh period control circuit implemented in 44nm mobile LPDDR2.

The sensor has a temperature sensitivity of −3.2mV/°C, over a range of 0°C to 110° C. Its resolution is 1.94°C and is only limited by the 6.2mV step of the associated resistor ladder not by its own design. The high linearity of the sensor permits one-point calibration, after which the errors in 61 sample circuits ranged between −1.42°C and +2.66°C. The drain currents through M1 and M2 in the sensor are 19μA and 1.8μA respectively, since the sensor is only activated for 128μs in every 8ms cycle, it consumes 0.33μA on average. The sensor has an active area of 0.001725mm2 and consumes less than 0.36μW on average with a supply of 1.1V. The design summary of the temperature sensor is summarized in Table 5.1.1.

TABLE 5.1.1. DESIGN SUMMARY OF THE PROPOSED TEMPERATURE SENSOR

Temperature Sensor Type	Typical
Process	44nm CMOS
Operating Range	0°C ~ 110°C
Supply Voltage (VDDSENSOR)	1.1V
Temperature sensitivity (35°C ~ 105°C)	−3.2mV/°C
Resolution (with a 6.2mV step)	1.94°C
Calibration (35°C ~ 105°C)	One-Point (@ 85°C)
Inaccuracy (61 Samples)	−1.42°C ~ +2.66°C (after Calibration)
Area (Temperature sensor)	0.001725mm^2 (115µm x15µm)
Average Power Dissipation	0.36µW (0.33µA x 1.1V)

5.2 FOLDED ON-CHIP CMOS THERMOMETER IN 2XNM CMOS PROCESS FOR MOBILE LPDDR3

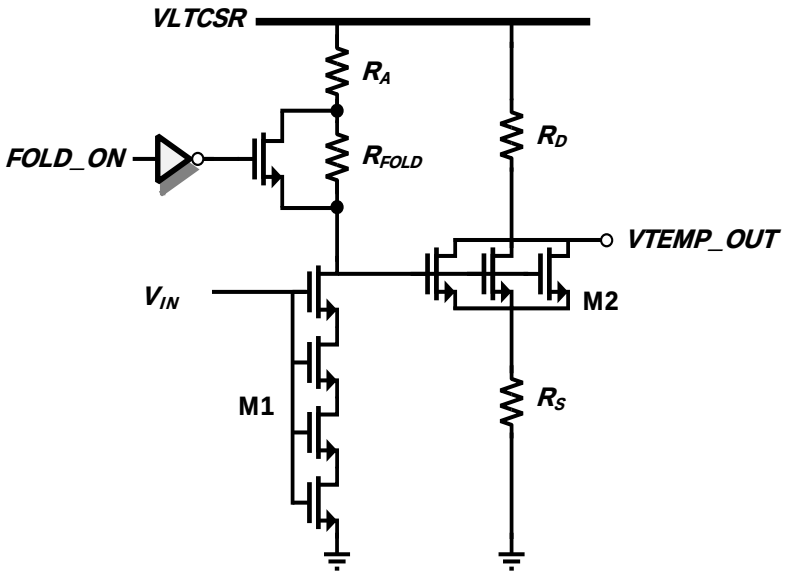

Fig. 5.2.1 Proposed folded type temperature sensor circuit

A prototype thermometer was designed and fabricated on a mobile LPDDR3 in a 29nm CMOS DRAM process. As supply voltage is lowered from 1.2V to 1.0V, the temperature sensor and several transistors size had to be changed for 44nm temperature sensor circuit. Structural difference between existing circuit and improved circuit are little, as already shown in Fig. 3.1.1.

As shown in Fig. 5.2.1, one signal line FOLD_ON is added to temperature sensor which was not in the 44nm temperature sensor circuit. Because the transistor is used as a switch, transistor turn on-resistance should also be carefully considered. Precisely obtain this transistor turn-on resistance value by simulation, and substitute the value from the resistor value.

The variation of output voltages with two types of temperature sensor against temperature for 494 samples of fabricated chips is shown in Fig. 5.2.2 and in Fig. 5.2.3. Between -40°C and 120°C with a supply voltage of 1.1V, the folded type exhibit a better a temperature sensitivity of −3.4mV/°C on average as compared to −2.9mV/°C on average from unfolded type.

In case of at a supply voltage of 0.8V, the variation of output voltages with two types of temperature sensor against temperature for 181 samples of fabricated chips is shown in Fig. 5.2.4 and in Fig. 5.2.5. As the supply voltage goes down, the temperature sensitivity and the resolution are decrease but the folded type exhibit a better performance with respect to temperature sensor without folding. The folded type exhibit a temperature sensitivity of −3.13mV/°C on average and resolution is about 1.98°C compared to −2.6mV/°C on average and 2.42°C as for the same temperature sensor without folding.

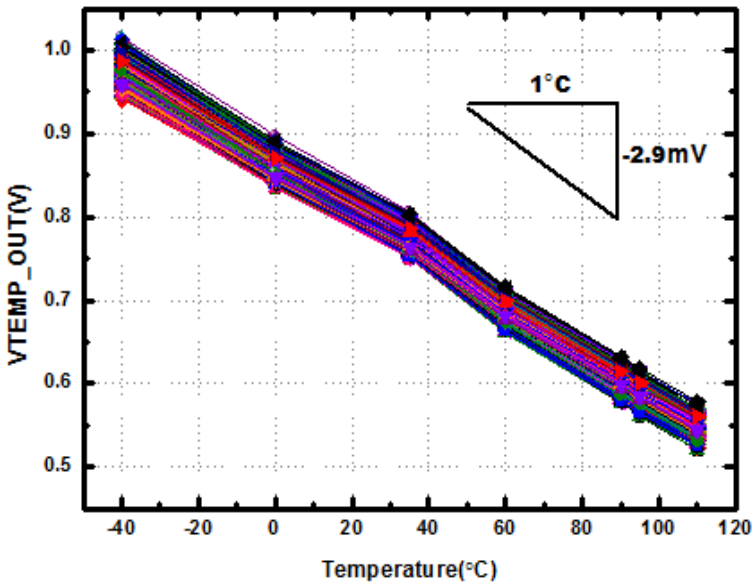

Fig. 5.2.2. Temperature sensor output voltages before one-point calibration measured from 494samples without folding @ VDD=1.1V.

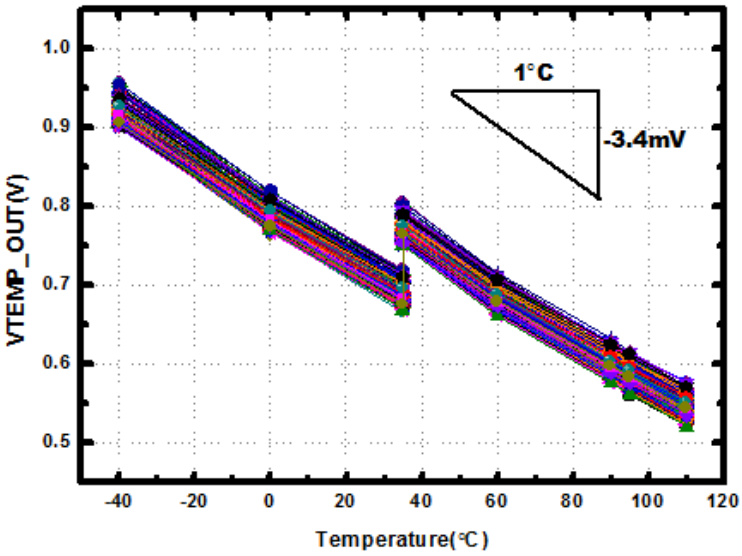

Fig. 5.2.3. Temperature sensor output voltages before one-point calibration measured from 494 samples with folding @ VDD=1.1V.

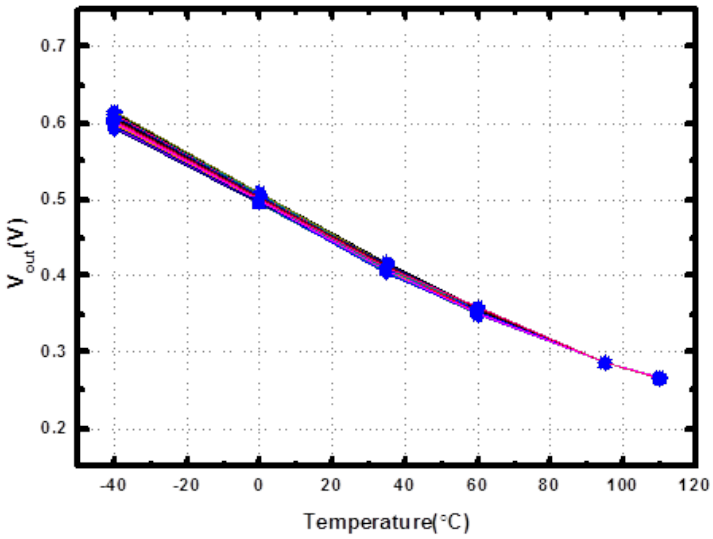

Fig. 5.2.4. Temperature sensor output voltages after one-point calibration measured from 181samples without folding @ supply VDD=0.8V.

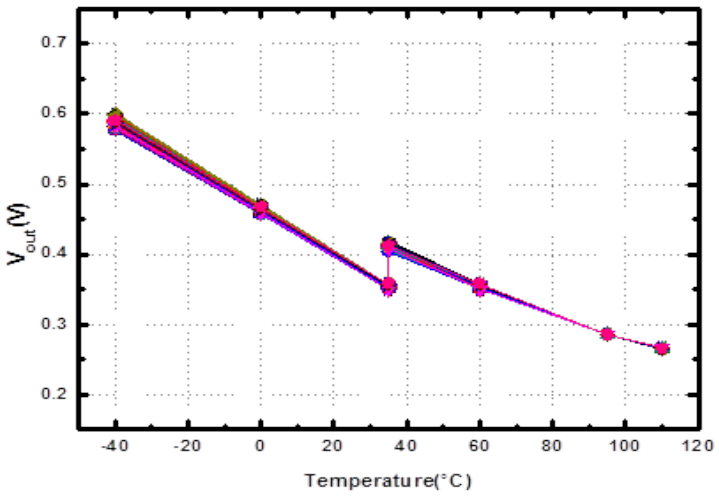

Fig. 5.2.5. Temperature sensor output voltages after one-point calibration measured from 181 samples with folding @ supply VDD=0.8V.

The overall performance comparison between the unfolded and folded type temperature sensor is summarized in Table 5.2.1 which including ultra-low operation voltage, temperature sensitivity, low power consumption, high linearity regardless of process skew variations and high productivity adapted by one point calibration.

The folded type on-chip thermometer incorporating in mobile LPDDR3 chip which fabricated in a 29nm DRAM process with a supply of 1.1V and 0.8V shows the better performance except for slightly increasing power consumption.

The folded type sensor exhibits more improvement of all those properties such as a temperature sensitivity of −3.2mV/°C@1.1V &−3.13mV/°C @0.8V, over more wide range of -40°C to 110°C. Its resolution is 1.85°C@1.1V & 1.98°C@0.8V and is only limited by the 6.2mV step. The more linearity of folded type sensor permits one-point calibration, after which the errors in 494 sample circuits ranged between −1.94°C and +1.61°C. The folded type sensor has an active area of 0.001606mm2 and consumes less than 0.198μW@1.1V &0.144μW@0.8V on average slightly more than unfolded type sensor.

Table 5.2.1 DESIGN SUMMARY OF THE TWO KINDS OF TEMPERATURE SENSOR AFTER FABRICATED IN 29NM DRAM PROCESS

Temperature Sensor Type	Unfolded		Folded	
Process	29nm CMOS		29nm CMOS	
Operating Range	-40°C ~ 110°C		-40°C ~ 110°C	
Supply Voltage ($V_{DDSENSOR}$)	1.1V	0.8V	1.1V	0.8V
Temperature Gain (-40°C ~ 35°C)	−2.9mV/°C	−2.6mV/°C	−3.4mV/°C	−3.13mV/°C
Resolution (with a 6.2mV step)	2.13°C	2.42°C	1.85°C	1.98°C
Calibration (-40°C ~ 110°C)	One-Point (@95°C)			
Inaccuracy (494 Samples)	−1.94°C ~ +1.61°C (after Calibration)			
Area (Temperature sensor)	0.001606mm^2 (73μm x 22μm)		0.001606mm^2 (73μm x 22μm)	
Average Power Dissipation	0.187 μW@1.1V 0.136 μW@0.8V		0.198 μW@1.1V 0.144 μW@0.8V	

CHAPTER 6

CONCLUSIONS

In this thesis, an on-chip CMOS thermometer, incorporating a novel temperature sensor, for adjusting the self-refresh period of LPDDR2 memory is presented. The sensor in the thermometer has a high temperature sensitivity and low sensitivity to the process variation because it only uses NMOS transistors and n+ active resistors. From derived a linearized expression for the sensor output voltage which showed that the temperature sensitivity is robust to process variation and the offset is easily tunable after manufacturing. This permits one-point calibration, which can significantly improve the productivity in mass production

Two types of on-chip CMOS thermometer including a novel temperature sensor is proposed, which is implemented in two different DRAM process technologies and integrated into mobile LPDDR2 and LPDDR3 products.

The on-chip thermometer incorporating in mobile LPDDR2 chip is fabricated in a 44nm DRAM process with a supply of 1.1V, which has a temperature sensitivity of −3.2mV/°C, over a range of 0°C to 110°C. Its resolution is 1.94°C and is only limited by the 6.2mV step of the associated resistor ladder not by its own design. The high linearity of the sensor permits one-point calibration, after which the errors in 61 sample circuits ranged between −1.42°C and +2.66°C. The sensor has an active area of 0.001725mm2

and consumes less than 0.36μW on average with a supply of 1.1V.

The newly proposed folded type on-chip thermometer incorporating in mobile LPDDR3 chip which fabricated in a 29nm DRAM process with a supply of 0.8V is proposed for supporting at sub-1V operation voltage and lower temperature extend to the -40°C. The folded type sensor exhibits more improvement of all those properties such as a temperature sensitivity of −3.2mV/°C@1.1V &−3.13mV/°C @0.8V, over more wide range of -40°C to 110°C. Its resolution is 1.85°C@1.1V & 1.98°C@0.8V and is only limited by the 6.2mV step. The more linearity of folded type sensor permits one-point calibration, after which the errors in 494 sample circuits are ranged between −1.94°C and +1.61°C. The folded type sensor has an active area of 0.001606mm2 and consumes less than 0.198μW@1.1V & 0.144μW@0.8V.

The overall performance comparisons with previously published works are summarized in Table 6.1.1 [3], [17]-[19]. The proposed on-chip thermometer have a good competence for ultra-low operation voltage, low power consumption, high linearity regardless of process skew variations and high productivity adapted by one point calibration.

Table 6.1.1 COMPARISON WITH PREVIOUSLY PUBLISHED WORKS

	This work (Folded)	This work (Unfolded)	Kim, CICC, 2009 [16]	Kim, ISCAS, 2008 [17]	Souri, ESSCIRC, 2011 [18]	Shalmany, ISSCC, 2013 [19]
Process	29nm DRAM	29nm DRAM	65nm CMOS	80nm DRAM	0.16μm CMOS	0.13μm CMOS
Temperature Range (°C)	-40~110	-40~110	−40 ~ +110	0 ~ +100	−55 ~ +125	−55 ~ +85
Supply Voltage (V)	1.1	1.1	1.2	N/A	1.8	1.5
Calibration	One-Point	One-Point	One-Point	One-Point	Two-Point	One-Point
Accuracy (°C) (# of samples)	−1.94~+1.61 (483)	−1.94+1.61 (483)	−2.899~+2.748 (15)	N/A	± 0.1 (20)	±0.15 (12)
Resolution (°C)	1.85	2.13	0.34	0.7	0.033	0.005
Conversion rate (S/s)	125	125	366k	1	5	50
Power Consumption (μW)	0.198	0.187	400	< 1	8.6	55
Area(mm^2) (Temperature sensor)	0.001606	0.001606	0.0013	0.016	0.12	1.1

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국 문 초 록

소자가 소형화되면 충전되는 전하의 양이 작아짐에 따라 모바일 기기에 사용되는 디램의 self-refresh 전류의 증가를 야기하고 있다. 이러한 문제의 해결을 위해 self-refresh 주기를 칩에 온도계를 내장하여 선택적으로 조절함으로써 전류증가의 문제를 해결할 수 있다. 본 논문에서는 공정변화에 둔감하면서 DRAM의 self-refresh 주기를 조절할 수 있는 온칩 CMOS 온도계를 제안하였다.

새로운 온도감지기를 기본으로 하는 두 가지 종류의 온칩 CMOS 온도계 설계가 모바일 LPDDR2 제품과 모바일 LPDDR3 제품에 각각 다른 디램 공정으로 구현되었다. 모바일 LPDDR2 제품에 내장된 온도계는 44nm 디램 공정을 통해 1.1V전원용으로 설계되었다. 이때 사용된 온도감지기는 0°C 에서 110°C 구간의 온도 구간에서 -3.2mV/°C 온도 구분능력을 가지고 있다. 또한 온도계 회로에 스텝당 6.2mV조절이 가능한 저항조절기를 구비하여 최대 1.94°C의 정밀도를 가지도록 하였다. 온도감지기의 높은 선형성으로 One-Point 보정이 가능하며 이를 통해 61개의 칩에 대한 온도 오차는 -1.42°C와 +2.66°C 내에 존재한다. 내장된 온도감지기는 0.001725mm^{2}의 면적을 차지하며 1.1V 전원동작조건에서 0.36mW 이하의 평균 전력을 소모한다.

매우 낮은 전원전압 하에서 다양한 공정 조건변화에도 높은 온도선형성을

유지하면서 온도센싱 능력을 향상시키고자 One-point 보정방법을 이용하여 Folded 타입의 온칩 온도계를 29nm 디램 공정을 이용하여 모바일용 LPDDR3 메모리칩에 1.1V와 0.8V 전원용으로 제작하였다. 제안한 Folded 타입의 온칩 온도계는 -40°C 에서 110°C 구간의 온도 구간에서 -3.2mV/°C@1.1V &-3.13mV/°C @0.8V의 온도 구분능력을 나타내고 있으며 0.8V의 저 전압 에서도 향상된 성능을 나타내었다. 온도계 회로내에 구비된 STEP당 6.2mV조절이 가능한 저항조절기를 통해 1.85°C@1.1V & 1.98°C@0.8V의 정밀도를 구현할 수 있다. Folded 타입의 온칩 온도계에 One-Point 보정방법을 적용하여 484개의 칩에서 온도 오차를 측정한 결과 -1.94°C와 +1.61°C 내에 존재하는 것으로 나타났다. 내장된 온도감지기는 0.001606mm^{2}의 면적을 차지하고 있으며 1.1V 전원동작 조건에서 0.19μW@1.1V & 0.14μW@0.8V의 평균 전력을 각각 소모하는 것으로 나타났다.

주요어 : 모바일 디램, 온도계, 온도감지기, 셀프-리프레쉬, 저전력.

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