저작자표시-비영리-변경금지 **2.0** 대한민국

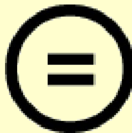
이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:

저작자표시. 귀하는 원저작자를 표시하여야 합니다.

비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.



변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 이용허락규약(Legal Code)을 이해하기 쉽게 요약한 것입니다.

Disclaimer

dCollection

공학박사 학위논문

Investigation of Hysteresis, Off-Current and Instability in In-Ga-Zn Oxide Thin Film Transistors Under UV Light Irradiation

자외선이 인듐갈륨징크 산화물 박막 트랜지스터의 전기적 특성 및 신뢰성에 미치는 영향 연구

2013년 8월

서울대학교 대학원

전기·컴퓨터 공학부

이 수 연

Investigation of Hysteresis, Off-Current and Instability in In-Ga-Zn Oxide Thin Film Transistors Under UV Light Irradiation

지도교수 한 민 구

이 논문을 공학박사학위논문으로 제출함

2013년 8월

서울대학교 대학원

전기·컴퓨터 공학부

이 수 연

이수연의 박사학위논문을 인준함

2013년 7월

위 원 장 ______________________ (인)

부위원장 ______________________ (인)

위 원 ______________________ (인)

위 원 ______________________ (인)

위 원 ______________________ (인)

Abstract

Investigation of Hysteresis, Off-Current and Instability in In-Ga-Zn Oxide Thin Film Transistors Under UV Light Irradiation

Soo-Yeon Lee
Department of Electrical Engineering and Computer Science
College of Engineering
Seoul National University

Amorphous oxide-based thin film transistors (TFTs), for instance, amorphous indium gallium zinc oxide (IGZO) TFTs, are expected to meet emerging technological demands where conventional silicon-based TFTs confront with the limitation of the electrical performance such as field-effect mobility, uniformity, and process temperature. However, the variation of characteristics and the stability in IGZO TFTs under light illumination still needs to be verified for further application. In this thesis, the characteristics and reliability of IGZO TFTs under light illumination were investigated. Furthermore, the effect of mechanical bending on flexible IGZO TFTs was analyzed for flexible displays.

First, the effects of light on initial characteristics of IGZO TFTs were studied. Under illuminated condition, significant hysteresis and off-current (I_{off}) were observed due to the creation of donor-like interface states near conduction band energy level arising from ionized oxygen vacancy (Vo^{2+}). From hysteresis, the response time (~10^0) of Vo^{2+} at the interface was obtained, which is important parameter for analyzing hysteresis. On the contrary to conventional mechanism of photo-current, the change in I_{off} increased with increasing light intensity. The increase of I_{off} occurs because Vo^{2+} at the interface prevents carrier depletion with Fermi-level pinning.

Second, the reliability of IGZO TFTs under the conditions combined with negative gate bias stress and light illumination were investigated. Under illumination, negative shift of threshold voltage (V_{th}) is accelerated by the photo-induced holes and Vo^{2+}. In TFTs featuring passivation layer, a long characteristic time (~10^2 s) for Vo^{2+} generation in IGZO bulk was extracted. It was also found that the charge trapping probability of single carrier did not change.

Finally, the reliability of flexible IGZO TFTs was analyzed when the bending radius was 10 mm, 4 mm, and 2 mm. The device characteristics were hardly changed under mechanical strain unless the gate bias stress was applied. However, V_{th} shift was increased by mechanical strain under the gate bias stress due to valence band energy level shift.

Keywords: thin film transistor, oxide semiconductor, light illumination,

gate bias stress, flexible display

Student Number: 2009-20860

Contents

Abstract i

Contents iv

List of Tables vii

List of Figures viii

Chapter 1 Introduction 1

1.1 Recent flat panel display 1

1.2 Dissertation Organization 8

Chapter 2 Review of IGZO TFTs 9

2.1 Oxide semiconductor for TFT application 10

2.2 Reliability of IGZO TFTs 17

2.2.1 Reliability under negative gate bias and illumination stress 17

2.2.2 Reliability under various environments 18

2.3 Passivation layer in IGZO TFTs 24

Chapter 3 Effect of light on initial characteristics of IGZO TFTs 27

3.1 Experiment 29

3.1.1 Fabrication of IGZO TFT 29

3.1.2 Experimental conditions 29

3.2 Electrical Characteristics of IGZO TFT under light

illumination 33

3.2.1 Photo-induced Hysteresis Phenomenon of IGZO TFT 38

3.2.2 Effect of Response time of Donor-like Interface States on IGZO TFT 45

3.2.3 Photo-induced Off-Current of IGZO TFT 51

3.3 Conclusion 58

Chapter 4 Effect of UV light on reliability of IGZO TFTs 61

4.1 Reliability of IGZO TFTs depending on gate insulator layer 63

4.2 IGZO TFT with SiO_2 gate insulator layer 67

4.2.1 Experiment 67

4.2.2 Reliability under negative gate bias stress combined with light illumination 68

4.2.3 Characteristics of fast recovery and time parameter 76

4.3 IGZO TFT with SiN_x gate insulator layer 81

4.3.1 Fabrication and Experimental Conditions 81

4.3.2 Reliability under negative gate bias stress combined with various intensities of light 84

4.3.3 Photo-induced carrier concentration vs. V_{th} shift 87

4.4 Conclusion 96

Chapter 5 Characteristics of IGZO TFT on Flexible Substrate 99

5.1 Overview of flexible TFT 100

5.2 Fabrication and Experiment of Flexible IGZO TFT107

5.3 The effect of mechanical bending on electrical

characteristics of Flexible IGZO TFT 112
5.4 The effect of mechanical bending on stability of Flexible IGZO TFT... 119
5.5 The effect of light on flexible IGZO TFTs............... 131
5.6 Conclusion 136

Chapter 6 Summary 139

Appendix A Design and Fabrication of Simultaneous Emission AMOLED Pixel Circuit143

Bibliography.. 165

초 록 177

List of Tables

Table 2.1 Comparison of TFTs with various channels 14

Table 3.1 Layer information of the fabricated IGZO TFTs 32

Table 4.1 Layer information of the fabricated IGZO TFTs 83

Table 5.1 The continuous use temperature and characteristics of the plastic substrates [119, 120]. 104

Table 5.2 Layer information of the fabricated flexible IGZO TFTs........ 110

Table 5.3 Extent of V_{th} change depending on length of TFTs under 4 mm bending radius when width was 25 μm. 117

Table 5.4 Extent of V_{th} change depending on width of TFTs under 4 mm bending radius when length was 10 μm. 118

Table 5.5 Fitting parameters of stretched exponential equations of V_{th} shift depending on various bending radius when bending axis was perpendicular to the channel direction........ 127

Table 5.6 Fitting parameters of stretched exponential equations of V_{th} shift depending on various bending radius when bending axis was parallel to the channel direction. 128

Table A.1 Panel specification........ 163

List of Figures

Figure 1.1 Evolution of display technology. 6

Figure 1.2 Next generation display...7

Figure 2.1 Schematic orbital structure of the conduction band minimum in Si and in an ionic oxide semiconductor [37]. 12

Figure 2.2 Atomic structure of IGZO (Ref. Displaybank)................................. 13

Figure 2.3 Progress of oxide TFT technology (Ref. Displaybank) 15

Figure 2.4 Prototype 70'' IGZO ultra definition LCD TV (Ref. DisplaySearch) 16

Figure 2.5 Evolution of transfer curves as a function of the applied -20 V negative gate bias stress time (a) in the dark and under green light exposure and (b) schematic of energy band diagram showing the sub-band gap states related to oxygen vacancy. [40] 19

Figure 2.6 Schematic energy band diagram to explain photo-induced hole trapping [49]. 20

Figure 2.7 Schematic energy band diagram showing the photo-desorption of oxygen molecules into the ambient atmosphere for the un-passivated device under the application of negative gate bias stress [78]. 21

Figure 2.8 Comparison of the transfer curves before and after the water exposure for the device with (a) 35 nm-thick and (b) 150 nm-thick

channels, respectively [85]. 22

Figure 2.9 Schematic showing the electric field-induced adsorption of oxygen molecules from the ambient atmosphere under the application of positive bias stress (left). Schematic showing the electric field-induced desorption of water molecules into the ambient atmosphere under positive bias stress (right) [86]. 23

Figure 2.10 Comparison of V_{th} shift depending on the passivation layer [86]. 25

Figure 3.1 Cross-section of the inverted-staggered etch stopper structure IGZO TFTs. 31

Figure 3.2 (a) Transfer characteristics of IGZO TFT in the dark when V_{DS} = 10 V. (b) Output characteristics of IGZO TFT when V_{GS} = 2, 4, and 6 V in the dark. 35

Figure 3.3 Transfer characteristics in the dark and under the 400 nm wave length light illumination. 36

Figure 3.4 Output characteristics when (b) V_{GS} = 2, 4, and 6 V, in the dark and under light illumination and (c)-10 V under light illumination. 37

Figure 3.5 C-V curve in the dark and under 400 nm wave length light illumination. 41

Figure 3.6 Conventional C-V characteristics when the interface states exist 42

Figure 3.7 Energy band diagram of IGZO TFTs when V_{GS} <0 or V_{GS} >0 under light illumination.. 43

Figure 3.8 Characteristics of the donor-like interface state (D_{GD}): (a) when the D_{GD} responds immediately to a change in the Fermi-level (E_F) (b) when the response time of D_{GD} (τ) is considered.......................... 44

Figure 3.9 Activation energy vs. gate-source bias extracted by Arrhenius plot. 48

Figure 3.10 Schematic of the numerical analysis flow.................................... 49

Figure 3.11 Result of the numerical analysis: the effect of the donor-like interface state on the transfer curve (a) when the states respond immediately with V_{GS} change (τ_f = τ_r =0) and (b) when the states cannot respond immediately with V_{GS} change (τ_f = 3 s and τ_r =1 s). 50

Figure 3.12 Experimental results (symbol) and ATLAS simulation results (line) of off-current under illumination according to the intensity of light. Off-current was extracted at V_{GS} = -10 V of the reverse sweep... 55

Figure 3.13 Comparison of the off-current (I_{off}) characteristics between the crystalline and amorphous material depending on the intensity of light. 56

Figure 3.14 Schematic of energy band diagram in IGZO TFTs...................... 57

Figure 3.15 Transfer characteristics under UV light illumination depending on the fabrication process... 60

Figure 4.1 Comparison of V_{th} shift (a) SiO_2 and (b) SiN_x gate insulator layer 66

Figure 4.2 Transfer curves of double sweep measurement before and after 1 hour negative gate bias (-30 V) and illumination stress..... 70

Figure 4.3 Time evolution of V_{th} shift of transfer curve at the forward and reverse sweep. 71

Figure 4.4 Transfer curves at the forward sweep before and after 1 hour negative gate bias (-30 V) and illumination stress, which is normalized by V_{th} shift. 72

Figure 4.5 Transfer curves at the reverse sweep before and after 1 hour negative gate bias (-30 V) and illumination stress, which is normalized by V_{th} shift. 73

Figure 4.6 Consecutively measured transfer curves after 1 h negative gate bias (-30 V) and illumination stress. 74

Figure 4.7 Transfer curves of double sweep measurement with various V_{GS} sweep range........ 75

Figure 4.8 Recovery characteristics (a) when the trapped positive charge at the gate insulator recovers and (b) when the created positive charge in IGZO bulk recover. 79

Figure 4.9 V_{th} shift and the extent of the fast recovery under negative gate bias (-30 V) and illumination stress when the stress time was 50 s, 100 s, 500 s, 1000 s, and 3600 s, respectively. 80

Figure 4.10 Cross-section of the inverted-staggered etch stopper structure IGZO TFTs. 82

Figure 4.11 Transfer characteristics in the dark and under the 400 nm wave length light illumination. 85

Figure 4.12 Transfer curves of IGZO TFTs subjected to negative gate bias (-20 V) stress with 400 nm wavelength light illumination (0.025 mW/cm^2). 86

Figure 4.13 ΔV_{th} versus stress time of IGZO TFTs under negative gate bias stress (-20 V) with light illumination. 91

Figure 4.14 ΔV_{th}/dt when the stress time is 0 s 92

Figure 4.15 Trapping process according to the hole concentration at the channel when the stress is just started. 93

Figure 4.16 Trapping process according to the hole concentration at the channel when the stress is progressed. 94

Figure 4.17 Comparison of ΔV_{th} at t = 7000 s from experimental result and calculated saturation value of ΔV_{th}. 95

Figure 5.1 A film-on-plastic structure bent to a cylindrical roll. 105

Figure 5.2 Summary of the response of a-Si TFTs to mechanical strain [134]. 106

Figure 5.3 Cross-section of the inverted-staggered etch stopper structure IGZO TFTs on flexible substrate. 109

Figure 5.4 (a) A photograph of bending measurement system. (b)

Schematic showing bending direction perpendicular to channel. 111

Figure 5.5 Transfer characteristics of flexible IGZO TFT under the bending of 4 mm radius... 114

Figure 5.6 Schematic of flexible IGZO TFTs on plastic substrate............... 115

Figure 5.7 Calculated strain of each layer 116

Figure 5.8 Time evolution of V_{th} shift under negative gate bias (-30 V) stress depending on bending radius. Bending axis was perpendicular to channel 122

Figure 5.9 Flexible IGZO TFT sample and 10 mm bending chuck............. 123

Figure 5.10 Time evolution of V_{th} shift under negative gate bias (-30 V) stress depending on bending radius. Bending direction was parallel to channel.. 124

Figure 5.11 Comparison of the trends of mechanical strain and $|\Delta V_{th}|$ when bending direction was parallel to channel.............................. 125

Figure 5.12 Calculated strain of each layer considering the built-in stress 126

Figure 5.13 Energy band structure when bending axis was perpendicular to channel direction... 129

Figure 5.14 Energy band structure when bending axis was parallel to channel direction... 130

Figure 5.15 Time evolution of ΔV_{th} of IGZO TFTs when the negative gate bias of -30 V was applied under visible light. 133

Figure 5.16 Time evolution of ΔV_{th} of IGZO TFTs when the negative gate bias of -30 V was applied under 400 nm and 450 nm wavelength light. 134

Figure 5.17 Absorption coefficient of IGZO semiconductor 135

Figure A.1 The progressive emission driving scheme for 3D display...... 146

Figure A.2 The simultaneous emission driving scheme for 3D display.. 147

Figure A.3 The progressive emission driving scheme for 2D display...... 148

Figure A.4 The simultaneous emission driving scheme for 2D display.. 149

Figure A.5 (a) Conventional pixel schematic and (b) the timing diagram for the progressive emission driving.. 151

Figure A.6 (a) Conventional pixel schematic and (b) the timing diagram for the progressive emission driving... 154

Figure A.7 OLED current variation according to V_{th} variation from -0.5 V to 0.5 V: (a) at the proposed pixel and the conventional 6T1C and (b) when OLED emission time is decreased....................................... 158

Figure A.8 Leakage current path at the gate node of the driving TFT at: (a) the conventional 6T1C and (b) the proposed pixel circuit............ 159

Figure A.9 Pixel layout. 161

Figure A.10 Panel demonstration.. 162

Figure A.11 (a) External circuit design for the proposed simultaneous emission driving pixel circuit and (b) the timing diagram............ 164

Chapter 1 Introduction

1.1 Recent flat panel display

Electronic displays are essential elements in communication, computing, and entertainment devices such as mobile phone, PDA, digital still camera (DSC), laptop computer, monitor, large area TV and so on. Flat panel displays (FPDs), which is light-weight and thin, have been main stream over the bulky cathode ray tube (CRT) in the display industry as shown in Figure 1.1 [1]. As active matrix liquid crystal displays (AMLCDs) employing the thin film transistors (TFTs) demonstrated large size and high image quality, AMLCDs have been widely used [2-4]. By incorporating TFTs as the switching elements at each pixel in a matrix display, the voltage signal for each pixel could be controlled independently so that AMLCDs could achieve a high image quality such as

high resolution and full-color display. Recently, active-matrix organic light-emitting diode (AMOLED) displays have attracted a considerable attention due to faster response-time (~several μsec) and more vivid color than AMLCD. Starting from the mobile devices, AMOLED displays are developed extensively for the large-sized display.

The electrical performance and reliability of TFTs are key issues for active matrix display because the mobility, off-current and stability of TFTs influence directly the voltage signal addressing on each pixel. When the switching TFT in AMLCD is turned on, the liquid crystal capacitor of each pixel is charged by the data voltage. The mobility of switching TFTs should be increased at the same time when the displays increase in size, resolution and refresh rate. In AMOLED display, pixels require not only the switching devices but also the current driving device for OLED emission because the OLED luminance is emitted by a constant current source with a desired image data at each pixel. Thus, a small variation of the TFT characteristics such as mobility and threshold voltage (V_{th}) causes non-uniform luminance in the display panel, so that the uniformity of TFT characteristics is also important in AMOLED display. TFT characteristics vary with the device structure and the types of materials. Usually, silicon-based TFTs such as hydrogenated amorphous silicon (a-Si:H) TFTs and low temperature polycrystalline silicon TFTs have been widely used for AMLCD and AMOLED display.

a-Si:H TFTs are suitable for large area applications due to their productivity on a large area glass substrate by low temperature process

below 300°C [3-5]. However, the device performance is limited by low mobility of the channel materials (< 1 $cm^2/V \cdot s$) and instabilities under bias stress [6] and exposure of light [7]. In crystalline silicon, there are the band of bonding states (valence band) and the antibonding band (conduction band). There is the energy gap between the valance and conduction band edge. In amorphous phase, semiconductor has tails of the conduction and valance band states because of disorder of the bond lengths and angles in the silicon matrix causing significantly low mobility [8]. Under gate bias stress, the threshold voltage (V_{th}) is easily changed and sometimes subthreshold slope (SS) is increased at the same time. When only V_{th} is changed and transfer curve shape was not changed, the charge trapping at the SiN_x gate insulator is responsible for V_{th} instability of a-Si:H TFT [9]. On the other hand, the defect creation is the main cause of the instability of a-Si:H TFT when V_{th} change is accompanied by SS increase [10-13]. The defect creation originates from the weak-bond breaking by hydrogen diffusion in a-Si:H.

The limitation of a-Si:H TFT capability could be overcome by employing the polycrystalline silicon (poly-Si) film as an active layer [14-16]. As producing of low temperature poy-Si (LTPS) TFTs was succeeded, LTPS TFTs have attracted considerable attentions due to its high electron mobility (30~500 cm^2/Vsec) and current driving capability [17]. Excimer laser annealing (ELA) has been extensively studied to produce poly-Si thin film on a large area glass substrate [18-23]. A rapid heating is induced to a-Si film by the pulsed laser in the ELA process. Because more

than 90% of the excimer laser energy is absorbed within a shallow depth (~20 nm) from the a-Si film surface during laser pulse duration (tens of nanoseconds) the low temperature (< 400°C) crystallization of a-Si film on a glass can be obtained without any thermal damage to the glass [22, 23]. The electrical characteristics of LTPS TFT is superior to a-Si:H TFTs allowing a fast charging capability with the reduced device size for high-resolution display. However, there is a non-uniformity issue of grain-boundary induced by the fluctuation of ELA energy. The non-uniformity of grain-boundary causes the non-uniformity of device characteristics so that it is difficult to demonstrate the luminance uniformity in the AMOLED display panel [24, 25]. Therefore, to compensate the TFT characteristic variation, the compensate pixel circuits are required for the uniform luminance in the display panel [26-28].

Recently, amorphous oxide-base semiconductors, for instance, amorphous indium gallium zinc oxide (IGZO), have attracted much attention as a candidate for advanced TFTs [29-36]. Oxide-based TFT can be fabricated under low temperature less than 300 °C and the active layer can be fabricated at room temperature. Because IGZO is an amorphous phase in general, TFTs show uniform electrical properties with a large-area substrate. At the same time, IGZO TFTs have high filed-effect mobility (> 10 $cm^2/V{\cdot}s$) even though it is amorphous. In IGZO semiconductor, electron conduction is insensitive to variation of chemical bond structure[37]. Thus, the carrier mobility is preserved in amorphous phase which is completely different from a-Si:H. In the aspect of TFT stability,

IGZO TFT exhibits rather good electrical characteristics and stability in the dark state [38]. However, when light is illuminated, V_{th} decreases considerably without SS degradation under negative gate bias stress even though the light has a smaller photon energy than the optical bandgap (E_{opt}) of IGZO (~3.1 eV) [39, 40]. The instability mechanism is still under investigation. Even though the high performance display prototype has been demonstrated already adopting oxide-based TFT, sufficient physical background oxide-base TFT is required for the next generation display such as transparent and flexible display as shown in Figure 1.2.

Figure 1.1 Evolution of display technology.

Figure 1.2 Next generation display

1.2 Dissertation Organization

The purpose of this thesis is to investigate the effect of light illumination on the reliability of IGZO TFTs. Furthermore, the effect of mechanical bending on IGZO TFTs is also investigated.

Background of IGZO TFTs is given in Chapter 2. Reliability under various environments such as a combination of negative gate bias stress and illumination are reviewed.

In Chapter 3, the photo-induced hysteresis and I_{off} of IGZO TFT are investigated. When light is illuminated, significant hysteresis is observed. Sometimes, I_{off} is increased under light illumination. The origin and the characteristics of hysteresis phenomenon and I_{off} under various intensities of light were studied.

Chapter 4 focused on the mechanism of instability of IGZO TFT under negative gate bias and illumination stress. Under negative gate bias and illumination stress, V_{th} of IGZO TFTs shifts toward negative direction. In this study, Vo^{2+} generation in the IGZO bulk and a relationship between photogenerated holes and trapping at the gate insulator are studied.

The characteristics of IGZO TFT on plastic substrate were investigated in Chapter 5. IGZO TFTs are promising candidates for flexible display backplane due to high mobility, good uniformity, and low process temperature. The effects of mechanical bending and visible light illumination on reliability are investigated.

Finally, the summary of the thesis will be described in Chapter 6.

Chapter 2 Review of IGZO TFTs

Recently, amorphous IGZO TFTs have attracted considerable attentions for the various flat panel displays such as active-matrix liquid crystal displays and active-matrix organic light emitting diode displays due to the high filed-effect mobility and good uniformity. Because process temperature is less than 300 °C and the active layer can be fabricated at room temperature, IGZO TFTs is suitable for flexible display.

In this chapter, recent issues of of IGZO TFTs, such as the electrical characteristics and reliability, are reviewed.

2.1 Oxide semiconductor for TFT application

Polycrystalline oxide-based semiconductors such as In_2O_3, ZnO, and $SnO_2In_2O_3$, ZnO, and $SnO_2In_2O_3$, ZnO, and $SnO_2In_2O_3$, ZnO, and $SnO_2In_2O_3$, ZnO, and SnO_2, were introduced for the transparent conductive oxides (TCOs). TFT employing ZnO was reported in 1968. However, oxide-based TFT couldn't get much attention because silicon-based TFTs were widely used with their fast growth. As the display increases in resolution, size and refresh rate, mobility, stability, and uniformity becomes critical issues because of defects in a-Si:H TFTs or non-uniformity. From early 2000s, ZnO-based TFTs have been extensively studied due to the requirements for high-resolution, large size, and high frame rate operation. ZnO TFT exhibited high mobility near 20 $cm^2/V·s$ with room temperature deposition [41]. However, relatively high gate voltage was required. Electrical conductivity (10^{-2} Ω^{-1} cm^{-1} to 10^3 Ω^{-1} cm^{-1}) of oxide semiconductor higher than a-Si:H is attributed to the oxygen vacancies, cation interstitials, and substitutional/interstitial hydrogen, acting as shallow donors [42]. TCOs have a high carrier concentration (10^{18} cm^{-3} – 10^{21} cm^{-3}) due to these donors. However, polycrystalline structure, causing non-uniformity problem, and the difficulty of fabrication were drawbacks of ZnO TFTs.

In 2004, Nomura *et al*. reported a TFT adopting IGZO which is amorphous and deposited at room temperature[37] It demonstrated high-mobility (μ ~ 8.3 $cm^2/V·s$) and low off-current. On the contrary to silicon-based TFTs, IGZO TFTs have high filed-effect mobility even though it is amorphous.

This is because of the electronic orbital structure of IGZO. As shown in Figure 2.1, a conducting path for free electrons is formed by direct overlap between neighboring metal s orbitals. The conduction band of IGZO is mainly formed by the overlap of In 5s orbitals. Due to the spherical symmetry of the 5s orbitals as shown in Figure 2.1, the semiconductor is insensitive to structural deformation, so that IGZO has a high mobility even in amorphous phase. Table 2.1 compares features of various TFTs. IGZO TFTs have been considered as a promising material for display products due to its high performance and good uniformity. Thus, in the past decade, display prototype adopting the oxide-based TFT has been demonstrated as shown in Figure 2.3 and Figure 2.4.

Oxide-based semiconductor channel layers can be formed by widely used sputtering at a temperature of 300 ^{o}C or lower [43, 44]. One of the important parameters is the oxygen concentration because oxygen vacancies are the major source of free carriers. As oxygen partial pressure increases, transfer curve is positively shifted [45]. By optimizing oxygen content, very high mobility (46 $cm^2/V \cdot s$) and high performance (SS = 0.54 V/decade, $V_{th} \approx 0$ V) can be obtained [46]. Because TFTs are exposed to

visible light from the underlying backlight unit in a working AMLCD or AMOLED panel, the susceptibility of oxide TFTs with respect to illumination should be minimized. After device fabrication, annealing in oxygen ambient can affect the oxygen concentration within the active layer. Especially, wet O_2 annealing is more effective in reducing the density of electron traps, which helps to enhance TFT performance[47].

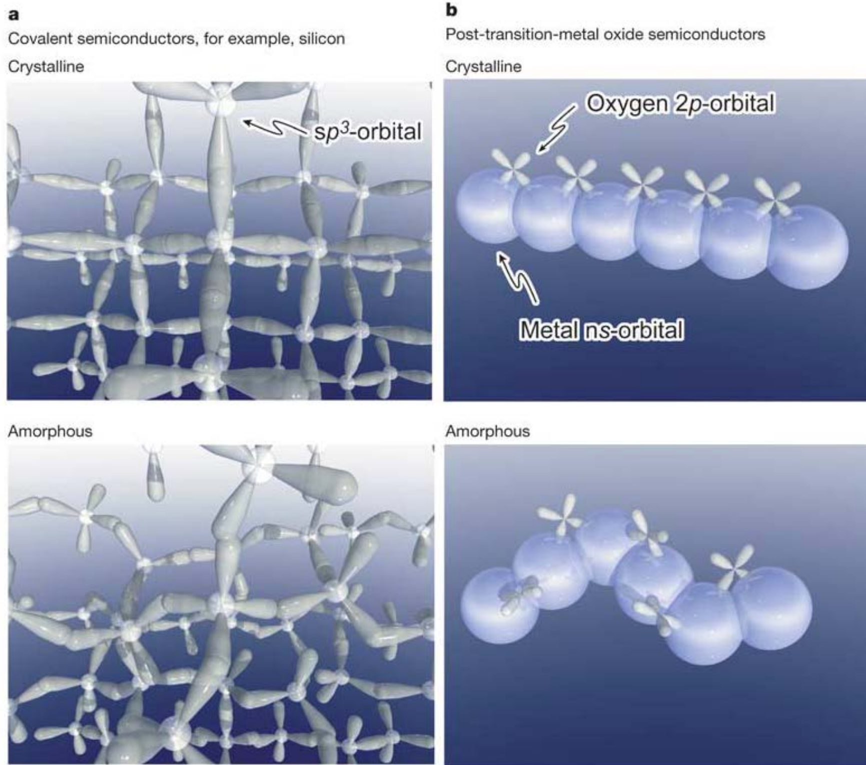
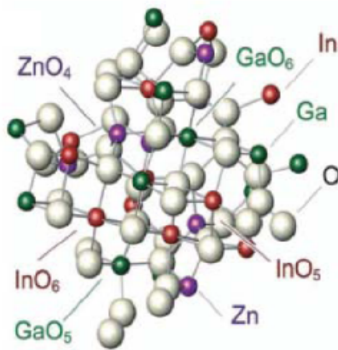


Figure 2.1 Schematic orbital structure of the conduction band minimum in Si and in an ionic oxide semiconductor [37].

- **Atomic structure**



High electron mobility

➡ **In^{3+}** as electron pathway former

$(4d)^{10}(5s)^0$

Stable amorphous structure

➡ **Zn^{2+}** as amorphous structure stabilizer

tetrahedral coordination

Excellent controllability of carrier density

➡ **Ga^{3+}** as carrier generation suppresser

high ionic field strength Z/r

Figure 2.2 Atomic structure of IGZO (Ref. Displaybank)

Table 2.1 Comparison of TFTs with various channels

	a-Si TFT	**Laser poly-Si TFT**	**nc-Si TFT**	**Oxide based TFT**
Mobility ($cm^2/V{\cdot}s$)	0.4~0.8	30~400	0.5~250	5~100
Uniformity	Good	Medium	Good	Med-Good
Stability	Bad	Good	Good	Good
TFT type	NMOS	CMOS	CMOS	NMOS
Technology maturity	High	High	Not yet	Medium

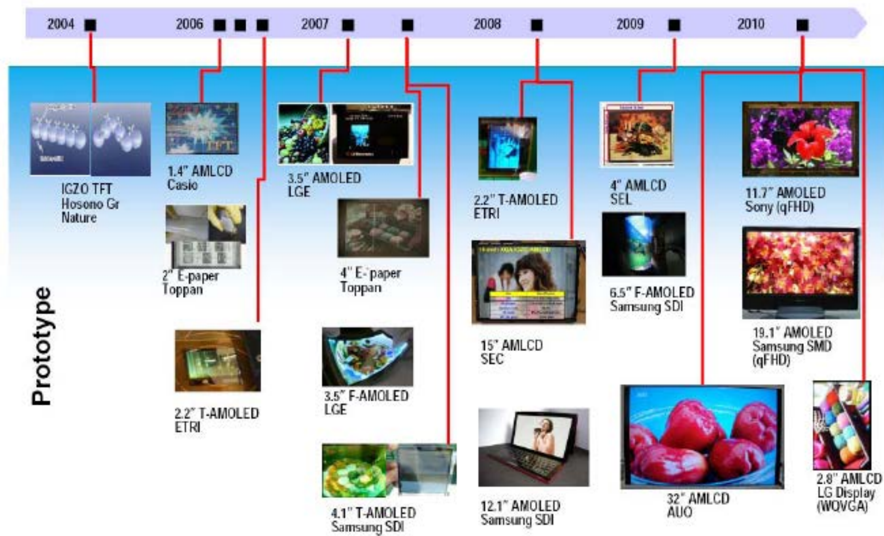


Figure 2.3 Progress of oxide TFT technology (Ref. Displaybank)

Figure 2.4 Prototype 70'' IGZO ultra definition LCD TV (Ref. DisplaySearch)

2.2 Reliability of IGZO TFTs

2.2.1 Reliability under negative gate bias and illumination stress

Good device performance and stability of IGZO TFT is exhibited in the dark state. Under the illumination and environmental stress, however, the reliability issues are still remained [48-72]. Because TFTs in display panel are mostly turned off during their operation and exposed to light, the stability under the negative bias illumination stress is one of the crucial issues. Under negative gate bias stress with light illumination, V_{th} decreases considerably. Figure 2.5 (a) shows transfer curves under negative bias stress when the device is illuminated by green light. Significant V_{th} shift without SS change was observed while V_{th} was barely changed in the dark. These negative shift of V_{th} is explained by the charge trapping of the photo-induced holes [39, 48, 49] and the creation and diffusion of the ionized oxygen vacancies (Vo^{2+}) [38, 40]. Vo^{2+} is created when the oxygen vacancies (Vo) capture photo-induced holes or lose two electrons by photon energy that is less than E_{opt} of IGZO. Figure 2.6 and Figure 2.5 (b) show the schematic of photo-induced hole trapping and Vo^{2+} creation, respectively.

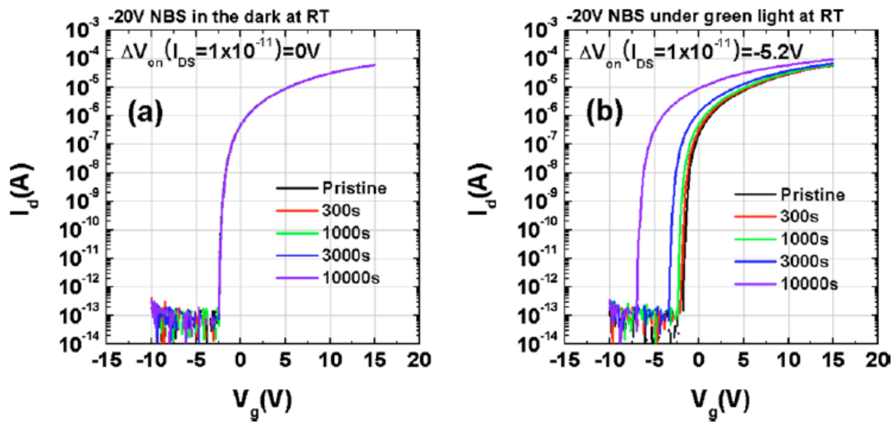
The transfer characteristic shows hysteresis and increase of off-current (I_{off}) under light illuminated condition without prolonged gate bias stress [73-77]. It has been reported that hysteresis phenomenon is caused by photo-generated Vo^{2+} at the interface between the gate insulator and the

active layer [73, 74]. The transfer curve was recovered immediately at the reverse sweep because Vo^{2+} can capture two electrons and be neutralized. The I_{off} increases when the photogenerated carriers are collected by the source/drain electrodes [75, 76] or the photo-generated carriers increase the doping level [77]. In the latter case, V_{th} is decreased at the same time without a change in SS.

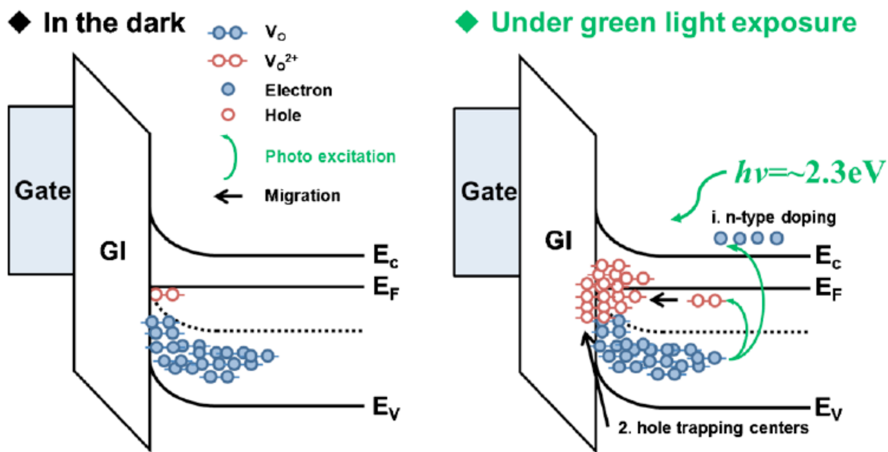
Without a passivation layer, the ambient effect on the device degradation should be considered. Figure 2.7 shows the schematic of energy band diagram explaining the photo-desorption of oxygen molecules into the ambient atmosphere [78].

2.2.2 Reliability under various environments

Oxide TFTs are sensitive to ambient atmosphere such as oxygen, hydrogen, or water molecules [79-86]. When oxide semiconductor was exposed to water, leakage current and SS was increased and V_{th} was decreased as shown in Figure 2.8 [85]. Figure 2.9 shows the schematic showing the electric field-induced adsorption of oxygen or desorption of water molecules depending on the gate bias stress [86]. The interaction between the backchannel of active layer and ambient atmosphere plays a critical role in the V_{th} shifts.



(a)



(b)

Figure 2.5 Evolution of transfer curves as a function of the applied -20 V negative gate bias stress time (a) in the dark and under green light exposure and (b) schematic of energy band diagram showing the sub-band gap states related to oxygen vacancy. [40]

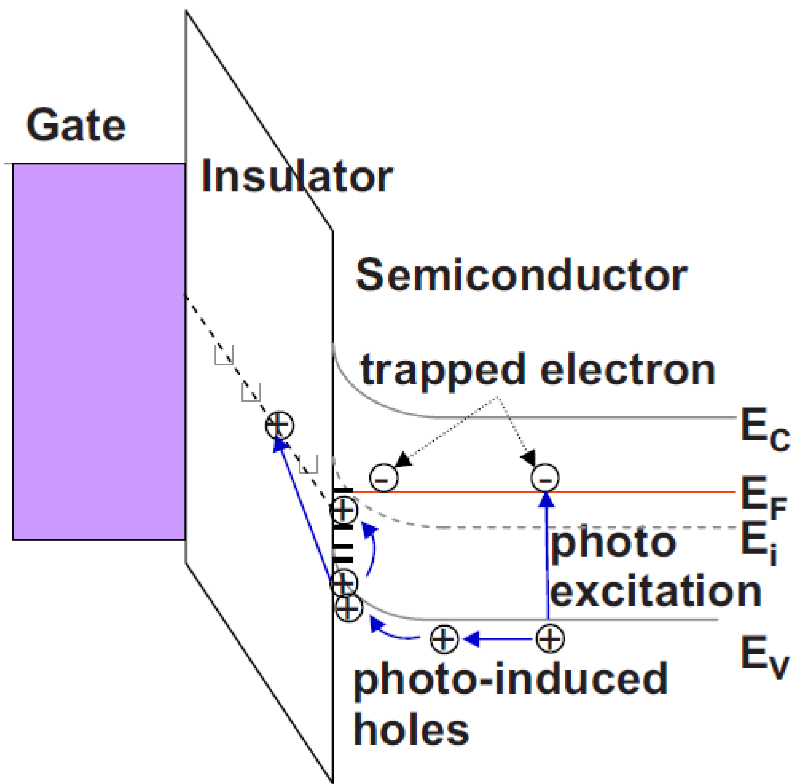


Figure 2.6 Schematic energy band diagram to explain photo-induced hole trapping [49].

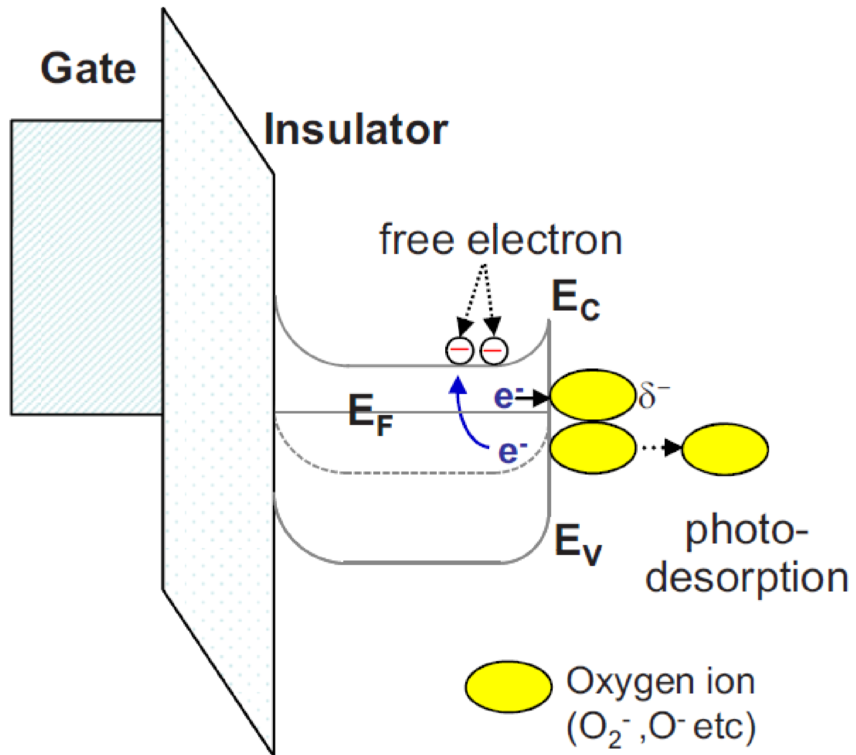


Figure 2.7 Schematic energy band diagram showing the photo-desorption of oxygen molecules into the ambient atmosphere for the un-passivated device under the application of negative gate bias stress [78].

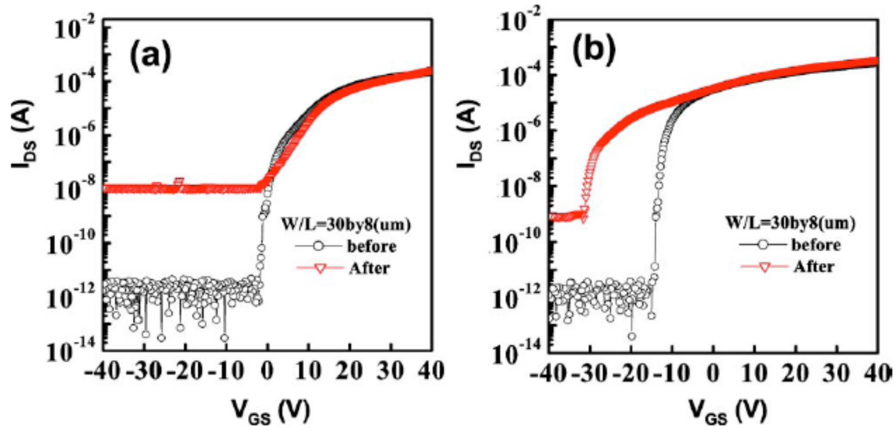


Figure 2.8 Comparison of the transfer curves before and after the water exposure for the device with (a) 35 nm-thick and (b) 150 nm-thick channels, respectively [85].

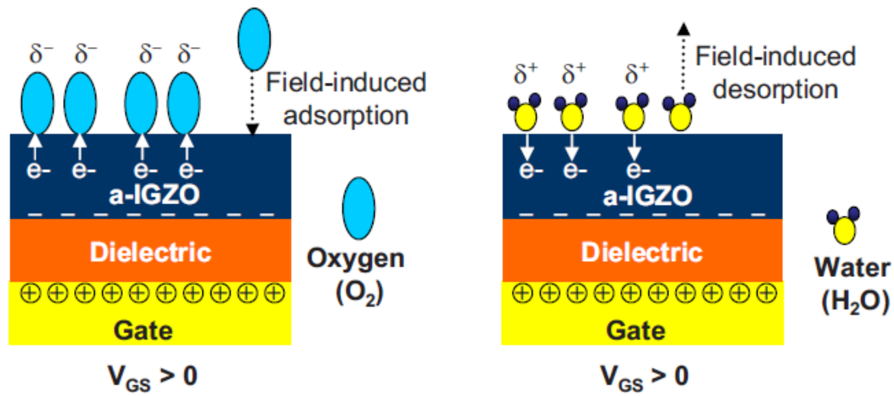


Figure 2.9 Schematic showing the electric field-induced adsorption of oxygen molecules from the ambient atmosphere under the application of positive bias stress (left). Schematic showing the electric field-induced desorption of water molecules into the ambient atmosphere under positive bias stress (right) [86].

2.3 Passivation layer in IGZO TFTs

Because oxide semiconductor is very sensitive to the ambient atmosphere, the passivation layer should be employed [64, 86-92]. Figure 2.10 shows the V_{th} stability of IGZO TFTs depending on the passivation layer. The device stability is improved by featuring passivation layer. The passivation layer is required in oxide TFTs not only for preventing the ambient effects but also for eliminating deep defects of back surface of oxide semiconductor [93]. Deep defects with high density are located in a depth of about 2 nm in the back surface of IGZO, which is one of the reasons in V_{th} shift under gate bias stress and illumination by light having photon energy less than E_{opt} of IGZO. However, it was found that the passivation layer eliminates the deep defect in the IGZO back surface so that the stability under light illumination is improved.

Without a passivation layer in IGZO TFTs, the effect of the photodesortion of oxygen molecules and subgap state at IGZO back surface cannot be excluded. To understand the effect of light on IGZO, the passivation layer is required to prevent the effect of ambient atmosphere and reduce the subgap state at the IGZO back surface.

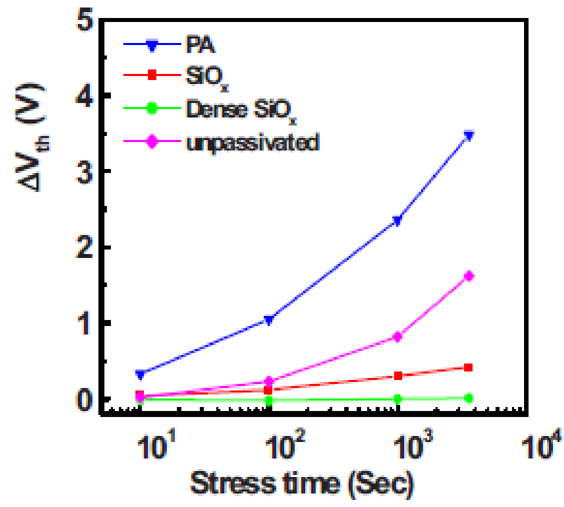


Figure 2.10 Comparison of V_{th} shift depending on the passivation layer [86].

Chapter 3 Effect of light on initial characteristics of IGZO TFTs

In IGZO TFT, hysteresis and increase off-current (I_{off}) are observed under light illumination without prolonged negative bias stress. Although there are many reports about the effect of light on IGZO TFTs, it cannot be clearly defined unless the effect of ambient atmosphere is excluded. Because IGZO is affected by both light illumination and ambient atmosphere, the passivation layer is required to understand the effect of light on IGZO. In this chapter, the effect of 400 nm light intensity on IGZO TFTs employing SiO_x passivation is investigated.

The hysteresis phenomenon was explained by Vo^{2+} created through photoexcitation at the interface between the gate insulator and the active layer. In this study, it was found that not only the creation of Vo^{2+} but also

the response time of Vo^{2+} should be considered when analyzing the hysteresis. From a numerical calculation, it was found that Vo^{2+} has rather long (~10^0 s) response time according to V_{GS} change.

In IGZO TFTs, I_{off} was also caused by Vo^{2+} at the interface. I_{off} of the result was much smaller than the estimated photocurrent. I_{off} showed a rapid non-linear increase with light intensity, while the photocurrent of a conventional crystalline semiconductor is expected to show a linear relationship. I_{off} of experimental results was not the photocurrent caused by the photogenerated carriers.

3.1 Experiment

3.1.1 Fabrication of IGZO TFT

IGZO TFTs with inverted-staggered etch stopper structures were fabricated. Molybdenum was deposited by DC sputtering on a glass substrate as the gate metal. 200 nm thick SiO_2 gate insulator layer was deposited by plasma enhanced chemical vapor deposition (PECVD) and the 40 nm thick active layer was deposited by sputtering. After the active island was patterned, the 50 nm thick SiO_2 etch-stopper layer was deposited by PECVD and patterned by dry etching. Then, the 250 nm thick source and drain electrodes (Mo) were deposited by sputtering. The channel length is defined with length of the etch stopper layer. The cross section of fabricated IGZO TFT is shown in Figure 3.1. The channel width and length of the device were 50 μm and 15 μm, respectively, and the active layer thickness was 400 Å. The thickness of each layer is shown in Table 3.1.

3.1.2 Experimental conditions

Monochromatic light was used with a band-pass filter from a Xenon lamp light source. Various wavelengths, such as 400, 450, 550, and 650 nm were illuminated from the top of the device. An Agilent B1500A semiconductor parameter analyzer was used for measuring the devices. The transfer curves were measured at V_{DS} = 10 V using double sweep which starts from the forward sweep (from V_{GS} = -20 V to 20 V) to the

reverse sweep (from V_{GS} = 20 V to -20 V). Those were scanned at 0.2 V intervals.

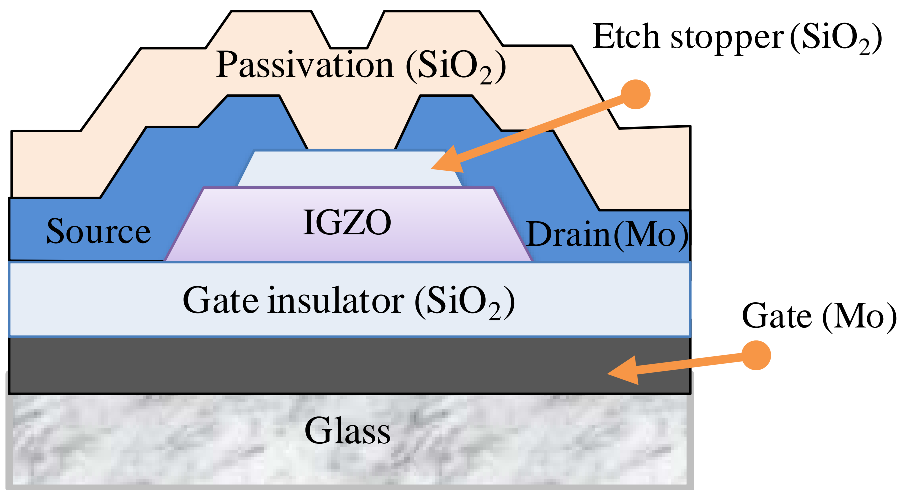


Figure 3.1 Cross-section of the inverted-staggered etch stopper structure IGZO TFTs.

Table 3.1 Layer information of the fabricated IGZO TFTs

Gate	Mo 250 nm
Gate Insulator	SiO_2 200 nm
Active	IGZO 40 nm
Source/Drain	Mo 250 nm
Passivation	SiO_2 100 nm + SiN_x 100 nm
Pad	IZO 90 nm

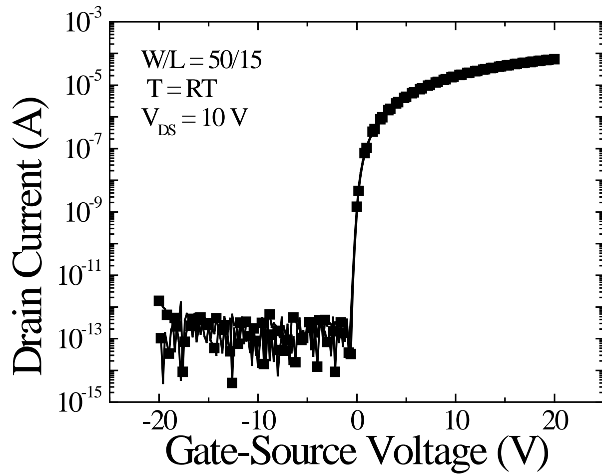
3.2 Electrical Characteristics of IGZO TFT under light illumination

Figure 3.2 shows IGZO TFT transfer curve and output curve in the dark state. The saturation mobility was 10.1 $cm^2/V \cdot s$ which is much higher than a-Si:H TFT (<1 $cm^2/V \cdot s$) even in amorphous phase. On-off ratio was larger than 1×10^8 and SS was 223 mV/dec. Off-current is quite small in IGZO TFTs because IGZO has a wide band gap (≈3.1 eV) and deep bulk state near E_V [47]. Due to deep bulk state, Fermi-level (E_F) cannot close to E_V. The energy barrier between the source electrode and E_V of IGZO is kept large even under the large negative V_{GS}. In the dark state, the device represents good performance such as high mobility, good SS and low I_{off}.

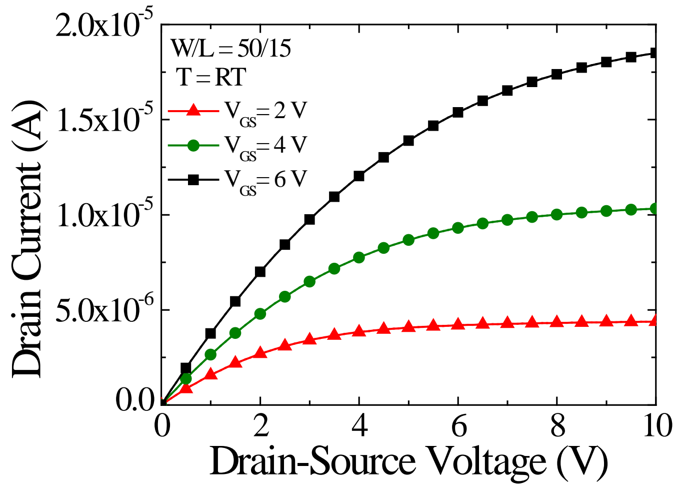
However, significant hysteresis and an increase of I_{off} were observed under light illumination as shown in Figure 3.3. The transfer curve change was observed when 400 nm wavelength light (>3.1 eV) was illuminated, while the electrical characteristics were not altered under 450, 550, and 650 nm wavelength light (1.91 eV ~ 2.76 eV). In IGZO TFTs, the devices responded to light even though light has smaller energy than E_{opt}, due to the photodesortion of oxygen molecules [78] and subgap state [93] at IGZO back surface. In this case, however, the transfer curve changed only when light had larger photon energy than E_{opt}. From these results, it was inferred that the passivation layer successfully suppresses the photodesorption of oxygen and subgap states.

Figure 3.3 shows the transfer characteristic of IGZO TFTs under various

light intensities. The output characteristics under light illumination are also shown in Figure 3.4 (a). Under light illumination two distinct phenomena were observed: hysteresis and an increase in I_{off}. For the hysteresis, V_{th} decreased and SS increased during the forward sweep, while V_{th} and SS hardly changed in the reverse sweep. The degree of hysteresis increased at higher light intensities and I_{off} also increased. As shown in Figure 3.4 (b), I_{off} increased linearly with V_{DS} with a negative gate bias. When the light was turned off, the device recovered immediately and the transfer curves recovered their initial characteristics before the illumination. In the following chapter, the hysteresis phenomenon will be discussed before the increase of I_{off}.



(a)



(b)

Figure 3.2 (a) Transfer characteristics of IGZO TFT in the dark when V_{DS} = 10 V. (b) Output characteristics of IGZO TFT when V_{GS} = 2, 4, and 6 V in the dark.

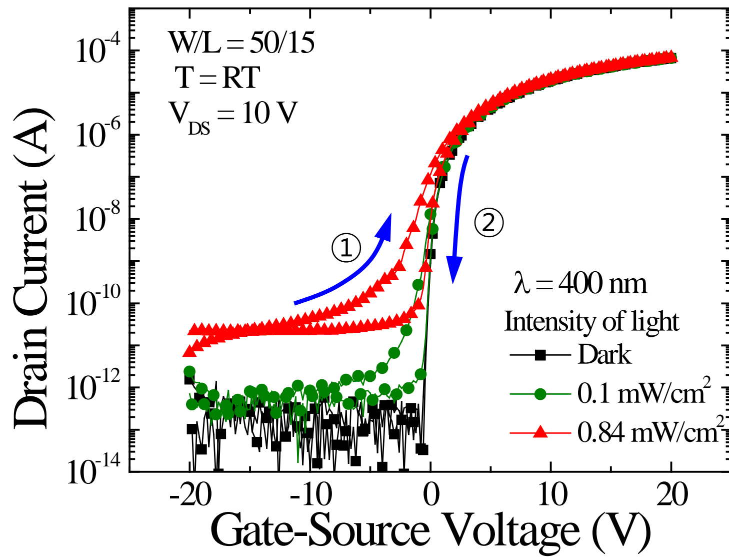
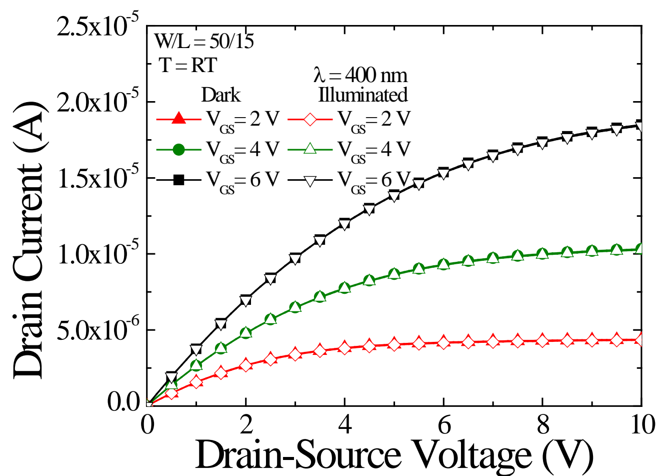
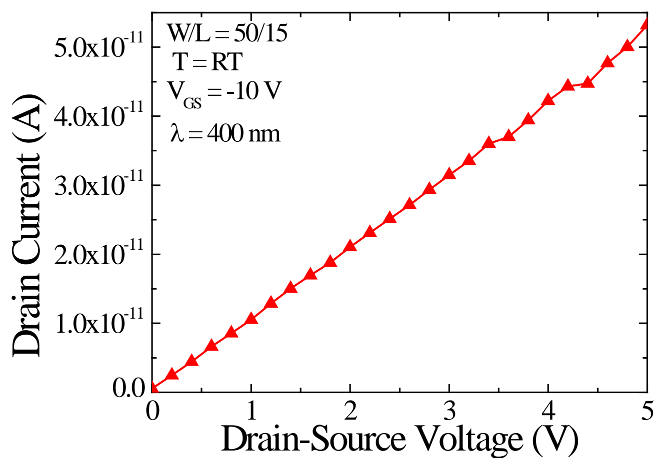


Figure 3.3 Transfer characteristics in the dark and under the 400 nm wave length light illumination.



(a)



(b)

Figure 3.4 Output characteristics when (b) V_{GS} = 2, 4, and 6 V, in the dark and under light illumination and (c)-10 V under light illumination.

3.2.1 Photo-induced Hysteresis Phenomenon of IGZO TFT

Under illumination, V_{th} decreased and SS increased during the forward sweep; however, these values returned to normal during the reverse sweep. During the forward sweep, the devices turned on at more negative gate bias and featured an extended subthreshold region. Figure 3.5 shows the Capacitance-Voltage (C-V) characteristics of forward and reverse sweeps conducted to investigate the interface of the devices. The C-V curves also shifted to negative voltages, extended during the forward sweep and remained unchanged from the dark measurement during the reverse sweep. When acceptor-like states are created, the states are negatively charged or neutral according to the trapping and de-trapping of the electrons. The transfer and C-V curves should stretch out toward positive direction compared to the ideal one (a in Figure 3.6). On the other hand, the donor-like states are positively charged or neutral. In this case, the transfer and C-V curves should stretch out toward negative direction (b in Figure 3.6). In the experimental results, both the transfer and C-V curves stretched out toward negative direction under the light illumination. Those indicate that donor-like states were created at the interface under light illumination. The presence and distribution of these donor-like states ($D_{GD}(E)$) alter the charge at the interface depending on the location of the Fermi level (E_F), which in turn affects the transfer curve. This can be expressed as,

$$V_{GS} = -\frac{Q_{IGZO}}{C_{ox}} + \varphi_S - \frac{Q_{it}}{C_{ox}}, \tag{3.1}$$

$$Q_{it} = q\int_{q\varphi_s}^{E_c} D_{GD}(E)dE, \tag{3.2}$$

Where Q_{IGZO}, C_{ox}, φ_s, Q_{it}, and E_C are the charge in IGZO, gate insulator capacitance, surface potential, interface charge, and conduction band energy level, respectively. For simplicity, the states above E_F were considered to be empty and those below E_F were filled by electrons. Figure 3.7 illustrates the energy band diagrams of the device under different gate bias conditions. When a negative gate bias was applied, E_F is shifted such that the separation between E_C is large and the interface is positively charged. Thus, the turn on voltage shifts negatively under light illumination. When the gate bias increases, the separation between E_F and E_C becomes smaller, and the donor-like interface states are filled by the electrons so that the interface states become neutral. This process is observed as a SS change.

Donor-like states may arise from Vo^{2+} in IGZO TFTs [40], produced by Vo hole capture [38, 73, 74]. In this case, the transfer characteristics were changed when illuminated by light having photon energy greater than E_{opt} of IGZO. This suggested that the hysteresis and the increase of I_{off} were caused by photoexcied electron-hole pairs. The resulting Vo^{2+} created by photo-induced holes caused hysteresis under light illumination. Immediate recovery occurred because IGZO is n-type and has high

electron concentration (10^{16}–10^{17} cm^{-3}) [94]. Depending on the gate bias, the carrier concentration of IGZO is changed; however, when no longer illuminated and no bias exists on the gate and source/drain electrodes, the IGZO active layer will revert to a high electron concentration (10^{16}–10^{17} cm^{-3}). Then, Vo^{2+} recovers to Vo with electron capture. This effect explains the temporary nature of the photo-induced hysteresis and off-currents.

During the forward sweep, we observed the effects of the donor-like interface states; however, in the reverse sweep no changes were seen in the subthreshold region even under illumination. This effect may be related to the response time (τ) of the donor-like interface states. When the donor-like interface states cannot respond immediately, $\tau > 0$, these empty interface states (D_{GD}^{+}) remain below E_F during the forward sweep as shown in Figure 3.8 (a). When E_F moves toward the valence band (E_V) during the reverse sweep, electrons will continue to occupy the interface states above E_F if $\tau > 0$ as shown in Figure 3.8 (b).

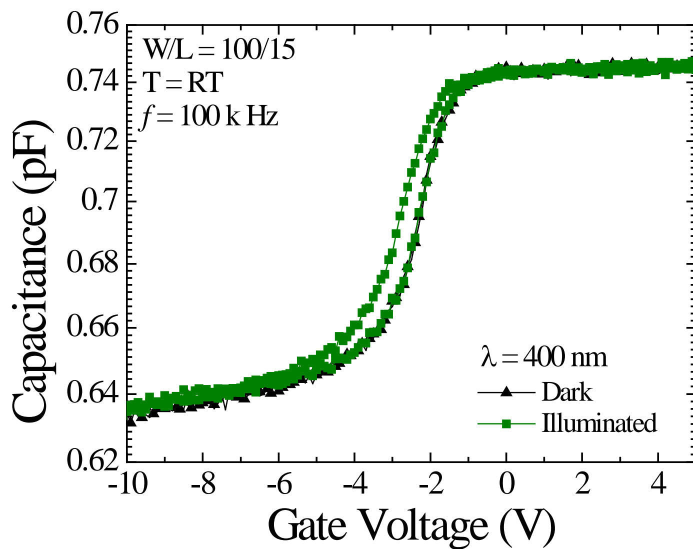


Figure 3.5 C-V curve in the dark and under 400 nm wave length light illumination.

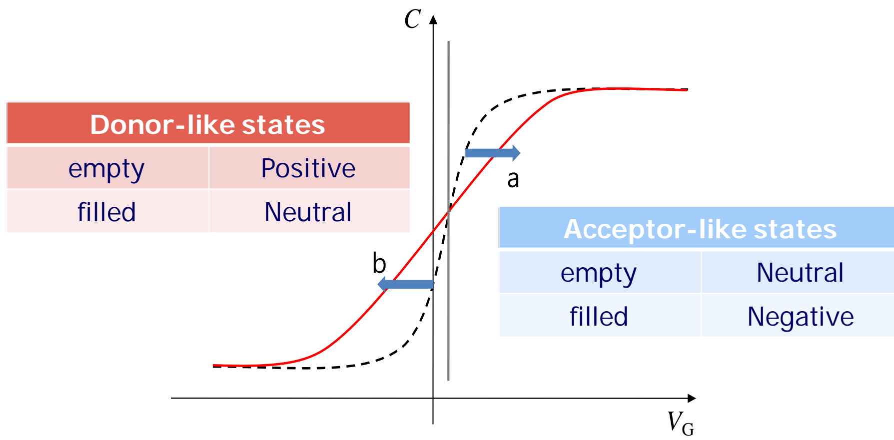


Figure 3.6 Conventional C-V characteristics when the interface states exist

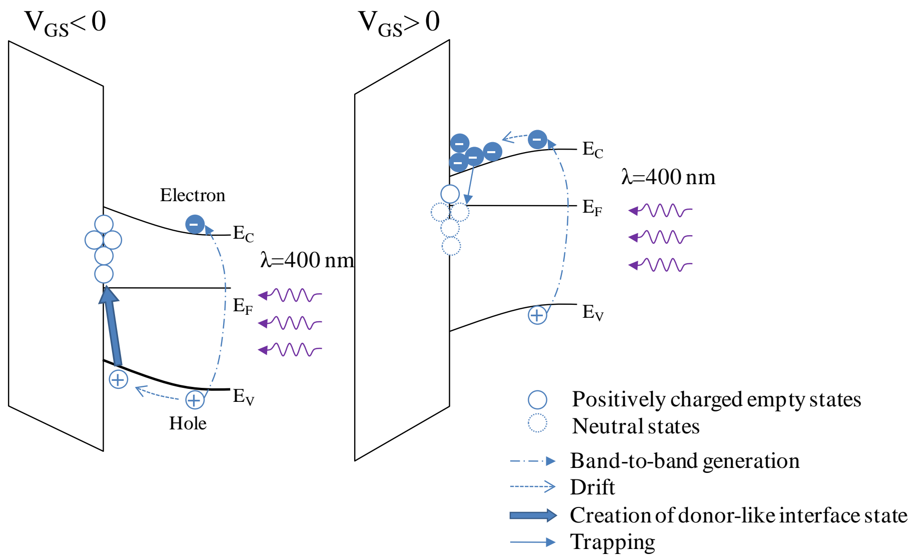
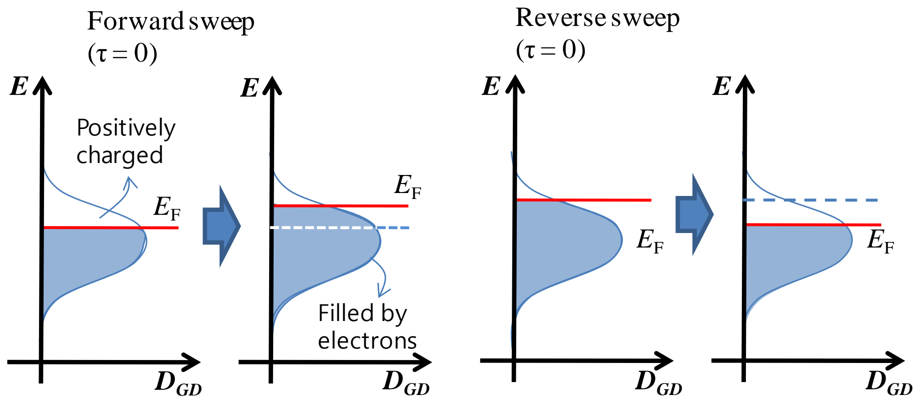
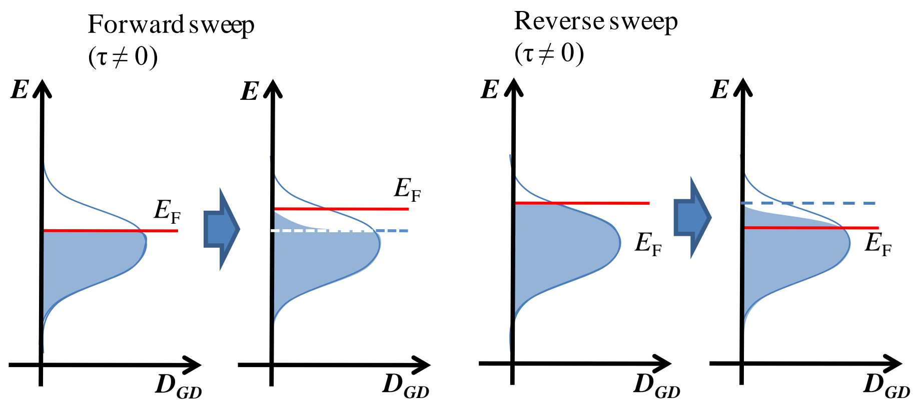


Figure 3.7 Energy band diagram of IGZO TFTs when V_{GS} <0 or V_{GS} >0 under light illumination.



(a)



(b)

Figure 3.8 Characteristics of the donor-like interface state (D_{GD}): (a) when the D_{GD} responds immediately to a change in the Fermi-level (E_F) (b) when the response time of D_{GD} (τ) is considered.

3.2.2 Effect of Response time of Donor-like Interface States on IGZO TFT

The effect of the response time of the donor-like interface state was investigated with a numerical analysis based on the following theory:

From V_{GS} equation (3.1), transfer curve shifts negatively as much as positive charge at the interface when light is illuminated.

$$\Delta V_{GS} = -\frac{Q_{it}}{C_{ox}}. \quad (3.3)$$

Q_{it} is changed according to the E_F location at the interface. As shown in Figure 3.8 (a) and expressed in (3.2), all $D_{GD}(E)$ above E_F contributes to Q_{it} when the response time of the donor-like state was not considered. However, $D_{GD}(E)$ below E_F also affect Q_{it} at the forward sweep and partial $D_{GD}(E)$ above E_F contributes to Q_{it} when the donor-like state cannot respond immediately to E_F change as shown in Figure 3.8 (b). Therefore, Q_{it} is expressed as below.

$$Q_{it} = q\int_{-\infty}^{\infty} D_{GD}{}^{+}(E)dE, \quad (3.4)$$

where $D_{GD}{}^{+}(E)$ is empty donor-like state. When donor-like interface states cannot respond immediately to a change in E_F, the $D_{GD}{}^{+}(E)$ will be occupied by electrons with the response time, τ_f, during the forward

sweep as

$$\frac{\partial D_{GD}^{+}(E)}{\partial t} = -\frac{D_{GD}^{+}(E)}{\tau_f}, \tag{3.5}$$

and the states will empty again during the reverse sweep with a response time τ_r given by

$$\frac{\partial D_{GD}^{+}(E)}{\partial t} = -\frac{D_{GD}(E) - D_{GD}^{+}(E)}{\tau_r}. \tag{3.6}$$

It was assumed that donor-like states near E_C were created at the interface with a Gaussian distribution,

$$D_{GD}(E) = N_{GD} \exp[-(E - E_{GD})^2 / W_{GD}{}^2], \tag{3.7}$$

where N_{GD} is the peak value of the Gaussian donor-like state, E_{GD} is the location below E_V, and W_{GD} is the variation. During sweep measurements, the scan rate of V_{GS} was constant and double sweep took around 72 s. It was assumed that the donor-like interface states were initially filled by electrons, as the electrodes were not under any applied bias. Under these conditions, the E_F was high and close to E_C so that the interface states were filled by the high electron concentration (10^{16}–10^{17} cm^{-3}).

In this study, the effect of additionally created interface state was investigated based on the experimental transfer curve in the dark state. Therefore, the density of state in IGZO bulk and any other physical parameters in IGZO TFT was not considered. E_C-E_F vs. V_{GS} was determined from an Arrhenius plot ($\ln(I_{DS})$ vs. $1/T$) [95] as shown in Figure 3.9. It allowed $\Delta V_{GS} = Q_{it}/C_{ox}$ at each V_{GS} in the dark to be determined by (3.3), (3.4), and (3.7). The detailed analysis flow is summarized in Figure 3.10.

The hysteresis phenomenon between the forward and reverse sweep was not observed if the response time was not considered, as shown in Figure 3.11 (a). However, Figure 3.11 (b) shows that hysteresis between the forward sweep and reverse sweep occurred when τ_f = 3 s and τ_r =1 s. This supports our suggestion that both the creation of the states and the response time based on V_{GS} change are the important factors in the hysteresis.

In this study, the response time was rather long (~10^0 s) compared with the carrier life time (~10^{-6} s). In the previous report, the long response time (~10^{-3} s) was observed because of the reaction with oxygen when the IGZO film was exposed to ambient atmosphere under light illumination [96]. However, TFT had the passivation layer so that the ambient effect could be excluded in this case. The response time, ~10^0 s, is Vo^{2+} generation time at the interface caused by the photo-induced hole capture of Vo in IGZO.

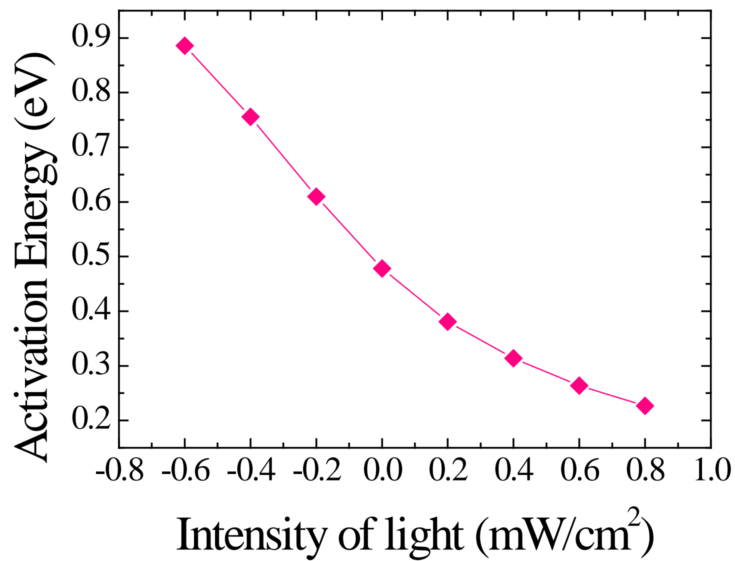


Figure 3.9 Activation energy vs. gate-source bias extracted by Arrhenius plot.

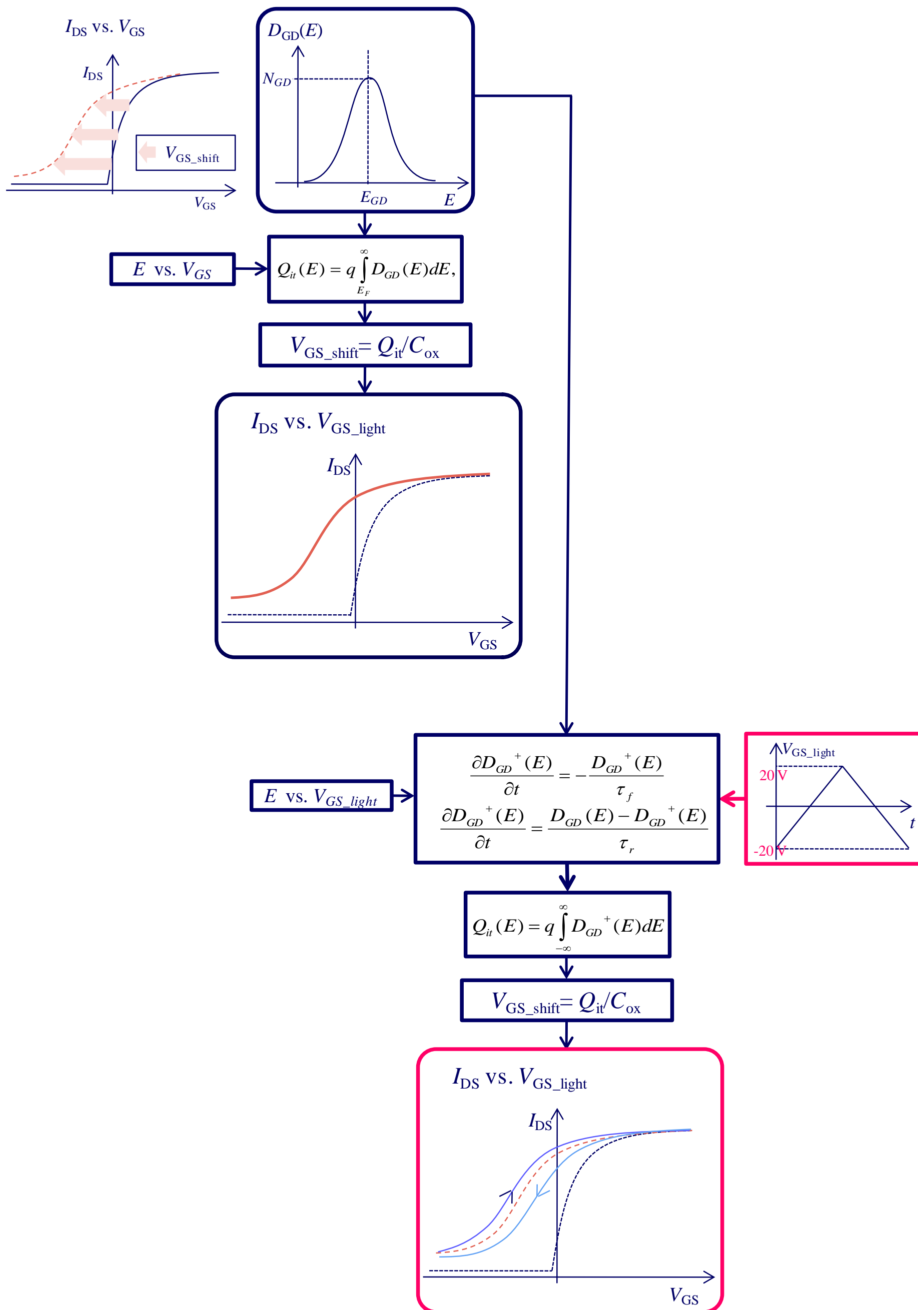
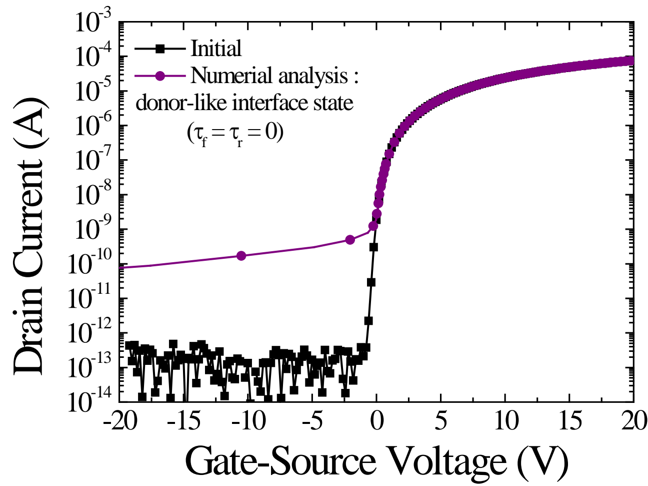
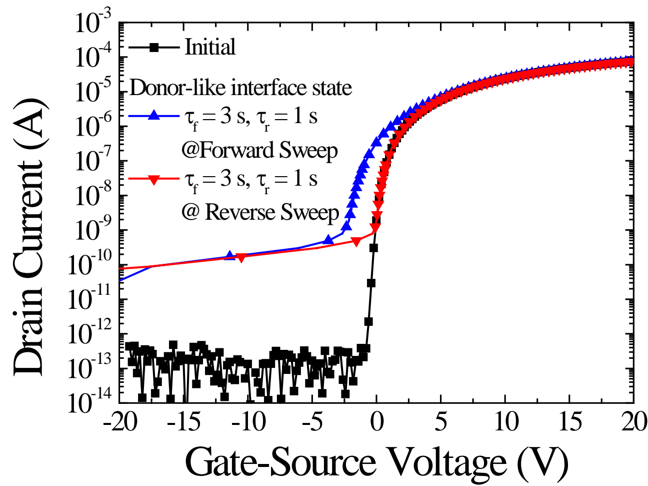


Figure 3.10 Schematic of the numerical analysis flow.



(a)



(b)

Figure 3.11 Result of the numerical analysis: the effect of the donor-like interface state on the transfer curve (a) when the states respond immediately with V_{GS} change (τ_f = τ_r =0) and (b) when the states cannot respond immediately with V_{GS} change (τ_f = 3 s and τ_r =1 s).

3.2.3 Photo-induced Off-Current of IGZO TFT

Considering the hysteresis and I_{off} phenomena in Figure 3.3, I_{off} increased linearly with V_{DS} as shown in Figure 3.4 (b), which suggested that it is attributed to drift current. Furthermore, I_{off} increased with light intensity as shown in Figure 3.12, where I_{off} was measured with V_{GS}=-10 V and V_{DS}=10 V during the reverse sweep. It is well known that I_{off} increases under light illumination because of photo-generated charge carriers that are collected by the source/drain electrodes [75, 76]. In IGZO, the photoexcitation increases both the doping level of IGZO and I_{off}. The increase of I_{off} is explained by the photo-generated carriers, I_{off}, which can be expressed as a drift current,

$$I_{off} = Aq\mu_n \tau_n G V_{DS} / L, \quad (3.8)$$

where A is a cross-sectional area of current flow, τ_{n} is the life time of charge carrier, and G is the carrier generation rate from the incident light. In the crystalline semiconductor, the photo-current increases linearly with light intensity as shown in Figure 3.13. As the intensity of light is increased, the photo-induced carrier density also increases, while others factors μ_{n} and τ_{n} remain constant. With a carrier lifetime of ~10^{-6} s [97] and absorption coefficient at 400 nm of ~1×10^{4} cm^{-1} [96], the photo-induced carrier density was estimated to be 10^{12} to 10^{13} cm^{-3}. The I_{off} was estimated at ~10^{-9} A at 0.84 mW/cm^{2}, which is much higher than the

experimental result, ~10^{-11} A. When both photo-induced holes and electrons are collected by the source/drain electrodes, I_{off} is increased. However, IGZO has a wide band gap (≈3.1 eV) and a deep bulk state near E_V [47] and the energy barrier between the source electrode and E_V of IGZO is large for the photo-induced holes even under at high negative gate bias as shown in Figure 3.14. Therefore, I_{off} is not significantly increased by the photo-induced carriers in IGZO TFTs. In a conventional amorphous semiconductor, the photocurrent cannot increase linearly with light intensity because of the formation of localized states [98]. The localized states behave as recombination centers for the photogenerated carriers, decreasing their lifetime. As light intensity is increased, the carrier generation rate increases linearly; however, the lifetime decreases at the same time. The change in I_{off} should therefore be expected to decrease with increasing light intensity as shown in Figure 3.13. However, experimental results showed that the change in I_{off} increased with increasing light intensity. This result also supports our suggestion that the measured I_{off} from our experimental results was not caused by photogenerated carriers. We can also exclude a change in doping level because the photo-induced carrier density was much lower than the IGZO doping level ($\gg 10^{17}$ cm^{-3}) and V_{th} was barely changed during the reverse sweep.

An increase of I_{off} is also observed when the electrons in the IGZO are not completely depleted in the off-region. When a large number of states exist at the interface or bulk, the energy band of IGZO is unchanged because E_F

hardly shifts towards E_V even under high negative V_{GS}. Under illumination, Vo^{2+} was created and caused the hysteresis in IGZO TFTs. Depletion of electrons in the IGZO is also prevented by the large amount of interface states Vo^{2+} even at high negative V_{GS}. Vo^{2+} causes not only the hysteresis, but also the increase of I_{off} under light illumination. To explore the effect of Vo^{2+} on the increase of I_{off}, simulations were performed using ATLAS (SILVACO). Parameters for the IGZO transistor models were based on previous reports [77]. An electron affinity of 4.3 eV, doping concentration of 5×10^{16} cm^{-3}, and band gap of 3.1 eV were used. The acceptor-like tail states at E_C were 3.5×10^{16} cm^{-3}, the decay energy for the tail distribution was 0.15 eV, and the peak value and variation of acceptor-like Gaussian states were 1.6×10^{16} cm^{-3}/eV and 0.21 eV, respectively. The peak for acceptor-like Gaussian state was located 1.34 eV below E_C. In the donor-like Gaussian states, the peak value and variation were 1×10^{21} cm^{-3}/eV and 0.3 eV, respectively. The energy location of the peak for donor-like Gaussian states was 0.7 eV above E_V. To express the effect of Vo^{2+}, donor-like Gaussian states were added at the interface between the active layer and the insulator layer. The total density of donor-like Gaussian interface states was ~10^{13} cm^{-2} and the Gaussian distribution peak was located at 2.42 eV above E_V of IGZO. The donor-like interface state density was assumed to increase linearly with the incident photon flux. I_{off} values were calculated at V_{GS}=-10 V with various densities of interface states. The results of these simulations are shown in Figure 3.12 and I_{off} values followed the same trend as the experimental results. I_{off} increased under illumination because of E_F pinning caused by Vo^{2+} at the interface. For the

SiO_2, the Gaussian distribution peak was located near the middle of the SiO_2 energy gap (~9 eV). There are various types of Vo states in SiO_2 [99] , and Vo near the E_V of SiO_2 may be related to the V_{th} shift under illumination by UV light and negative gate bias stress [38]. However, the changes under illumination by UV light without prolonged gate bias were more likely related to mid gap Vo of SiO_2.

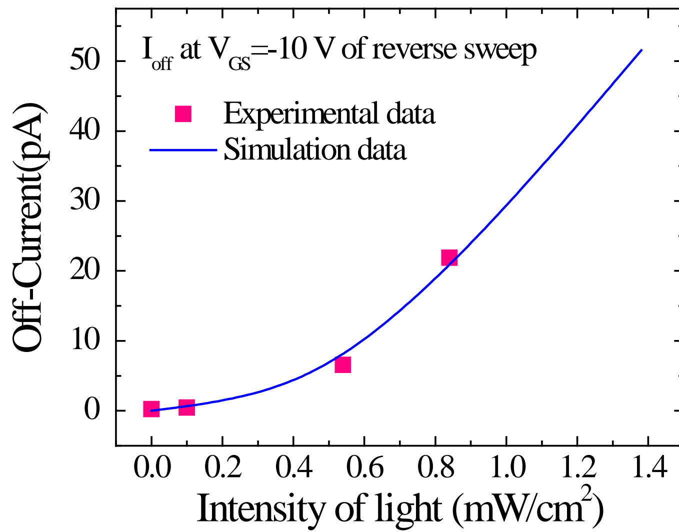


Figure 3.12 Experimental results (symbol) and ATLAS simulation results (line) of off-current under illumination according to the intensity of light. Off-current was extracted at V_{GS} = -10 V of the reverse sweep.

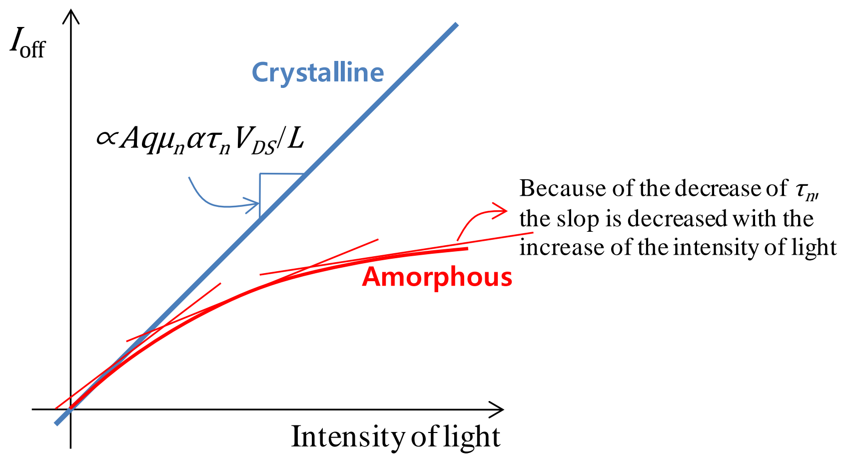


Figure 3.13 Comparison of the off-current (I_{off}) characteristics between the crystalline and amorphous material depending on the intensity of light.

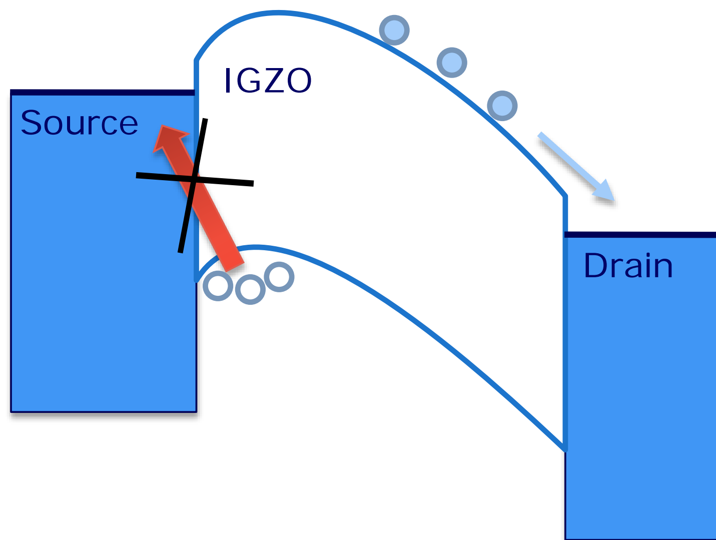


Figure 3.14 Schematic of energy band diagram in IGZO TFTs

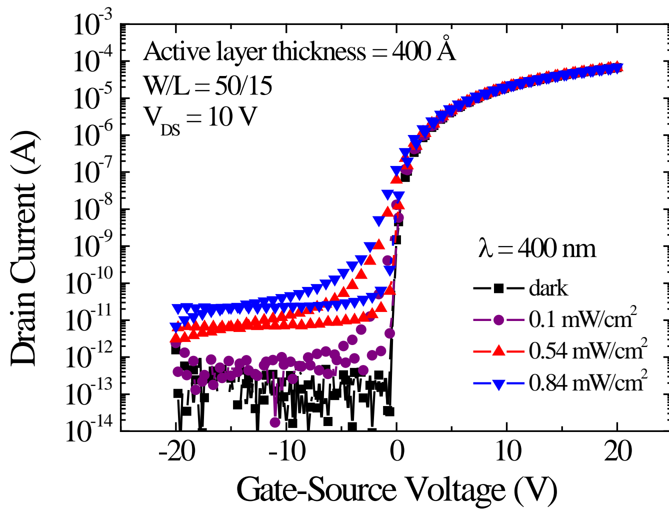
3.3 Conclusion

In this chapter, the photo-induced hysteresis and I_{off} of IGZO TFT under various light intensities were investigated. Vo^{2+} was created at the interface through capture of photo-induced holes by Vo. Under a negative gate bias, Vo was recovered from Vo^{2+} by electron capture. The decrease in V_{th} and increases in SS were explained by Vo^{2+} formation at the interface. However, the significant hysteresis could not be explained without considering the response time of Vo^{2+}. Because the creation and recovery of Vo^{2+} cannot occur immediately during V_{GS} potential sweep, hysteresis was observed under UV light. From the study, the response time, $\sim 10^0$ s, was obtained which related to Vo^{2+} generation at the interface.

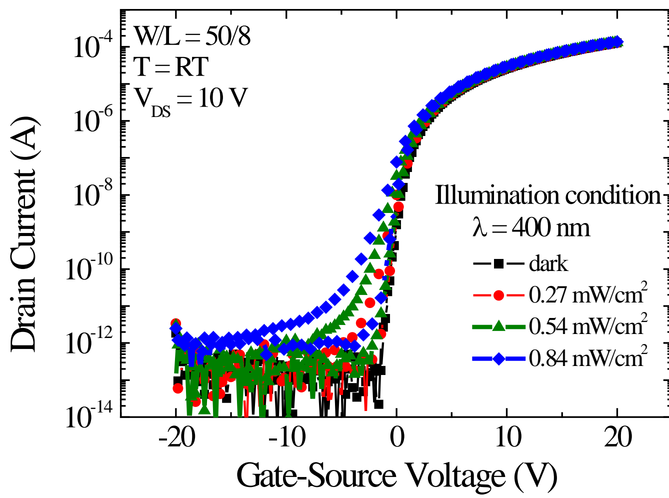
When I_{off} is considered as the drift current of the photo-generated carriers, the I_{off} of the experimental results was much lower than the calculated values. Furthermore, I_{off} showed a rapid non-linear increase with light intensity, whereas the photo-current should be expected to increase linearly with light intensity in crystalline semiconductors. In this case, the increase in I_{off} was attributed to formation of Vo^{2+} at the interface.

Interface is characterized by both SiO_2 and IGZO characteristics. When Vo in IGZO film is reduced, the transfer curve change under light illumination decreases [46]. Figure 3.15 shows that I_{off} increase can be suppressed depending on the process conditions. The midgap Vo of SiO_2 and the density of Vo in IGZO determine the behavior under UV light without

prolonged bias.



(a)



(b)

Figure 3.15 Transfer characteristics under UV light illumination depending on the fabrication process.

Chapter 4 Effect of UV light on reliability of IGZO TFTs

Two mechanisms have been proposed for the negative shift of V_{th} under a combination of negative gate bias stress and light illumination: charge trapping of the photo-induced holes and the creation and diffusion of ionized oxygen vacancies (Vo^{2+}). In this chapter, Vo^{2+} generation in the IGZO bulk and the relationship between photo-generated carriers and V_{th} shift are investigated.

In Chapter 3, hysteresis and increase of I_{off} were observed because Vo^{2+} was created at the interface under light illumination without prolonged gate bias. When light was turned off, the device recovers to the initial condition because Vo^{2+} was neutralized by electron capture. However, Vo^{2+} was also responsible to the negative shift of V_{th} under the negative

gate bias illumination stress, which cannot recover immediately. Since the transfer curve shape was hardly changed after the stress, the created Vo^{2+} at the interface was not affected by the prolonged negative gate bias. From the partial recovery characteristic of V_{th} shift, the relaxation time of Vo^{2+} generation in the IGZO bulk was extracted.

Quantitative analyses of the generation of holes by illumination and trapping process at the gate insulator are also presented. IGZO TFTs employing SiN_x gate insulator layer was used to investigate the relationship between hole concentration and the extent of V_{th} shift. When SiO_2 is employed as the gate insulator layer, Vo^{2+} in IGZO and gate insulator layer is important in TFT degradation. However, Vo does not exist in SiN_x gate insulator layer. Thus, the effect of carriers on the reliability of IGZO TFT has been investigated with SiN_x gate insulator layer. Light illumination caused a considerable V_{th} shift toward negative direction. However, the trapping probability of a single hole was not altered, which means that the accelerated V_{th} shift was because of the increase of hole concentration at the channel.

4.1 Reliability of IGZO TFTs depending on gate insulator layer

In IGZO TFTs, SiN_x or SiO_2 is usually adopted as gate insulator layer due to their large area scalability [100-103]. The stability of SiO_2 gate insulator is superior to that of SiN_x. Under gate bias or gate bias and illumination stress, the degree of V_{th} shift is much large with SiN_x gate insulator than SiO_x. This is because the trap density of SiN_x is much higher than that of SiO_2 [104-106]. Energy band structure of the gate insulator and IGZO is also key factor on the negative gate bias reliability. E_V difference between SiN_x gate insulator and IGZO is smaller than SiO_2 [63] so that V_{th} shifted more negatively with SiN_x gate insulator than SiO_2. In positive gate bias stress, it has been reported that the charge trapping mechanisms for SiN_x and SiO_2 gate insulator IGZO TFTs are different [107].

Depending on the charge trapping models, V_{th} shift follows the stretched-exponential equation [108] or logarithmic function [9] according to the stress time. When the trapped charge is redistributed in a deeper state of gate insulator layer, V_{th} shift can be described as

$$\Delta V_{th}(t) = A\{1 - \exp[-(\frac{t}{\tau})^{\beta}]\}, \quad (4.1)$$

where A is the V_{th} shift at infinite time. $\tau = \tau_0 \exp(E_a / kT)$ represents the characteristic trapping time of carriers, where the thermal activation

energy is given by $E_a = E_\tau \cdot \beta$ (in which β is the stretched-exponential exponent. E_τ is the average effective energy barrier that the electrons in the IGZO TFT channel need to overcome before they can enter the insulator). τ_0 is the thermal prefactor for emission over the barrier. When V_{th} shift follows the stretched exponential model, a function of log(ΔV_{th}) increases linearly with log(t).

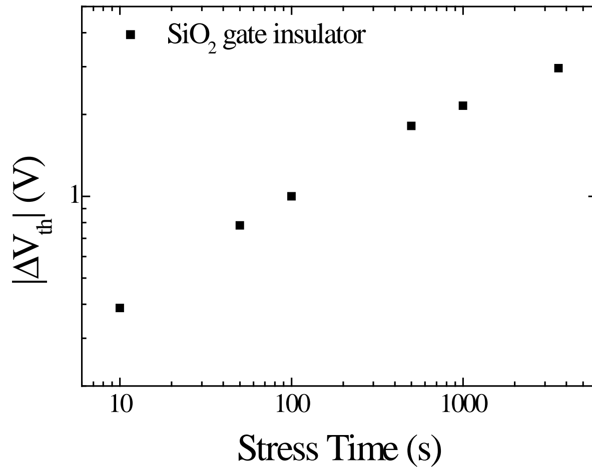
When the charge trapping at gate insulator is caused by direct tunneling of carriers and no further redistribution occur, V_{th} shift can be expressed as

$$\Delta V_{th}(t) = r_0 \log(\frac{t}{t_0} + 1), \tag{4.2}$$

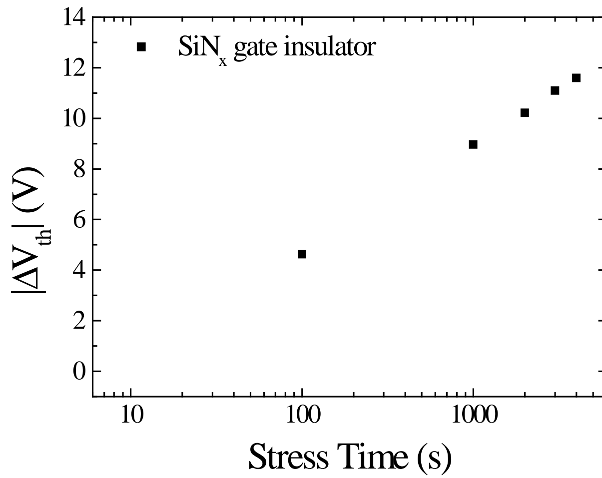
where r_0 is proportional to the gate insulator trap density and de Broglie wavelength and $1/t_0$ is the tunneling rate. In this case, ΔV_{th} and log(t) has a linear relationship. In SiO_2 gate insulator layer, V_{th} shift followed the stretched-exponential equation and logarithmic function in SiN_x under positive gate bias stress [107].

Under negative gate bias and illumination stress, it was found that V_{th} shift followed the same trend as the positive gate bias stress as shown in Figure 4.1. Figure 4.1 (a) is log(ΔV_{th}) vs. log(t) plot of SiO_2 gate insulator layer IGZO TFT and Figure 4.1 (b) is ΔV_{th} vs. log(t) of SiN_x. The results

suggested that the charge trapping at SiN_x gate insulator layer may arise from the direct tunneling of photo-induced holes from the channel.



(a)



(b)

Figure 4.1 Comparison of V_{th} shift (a) SiO_2 and (b) SiN_x gate insulator layer

4.2 IGZO TFT with SiO_2 gate insulator layer

4.2.1 Experiment

In this chapter, the inverted-staggered etch stopper structure IGZO TFTs with SiO_2 passivation layer was used. The detail of the fabrication process is mentioned in Chapter 3.1.1. The active layer thickness was 400 Å. 400 nm wavelength light was used and intensity was 0.2 mW/cm^2. An Agilent B1500A semiconductor parameter analyzer was used for measuring the devices. The stability characteristics of TFT were measured under negative gate bias stress of V_{GS} = -30 V and V_{DS} = 0 V for 1 hour under light illumination. The transfer curves were measured to monitor the degradation during the stress. Those were measured at V_{DS} = 10 V using double sweep which starts from the forward sweep (from V_{GS} = -20 V to 20 V) to the reverse sweep (from V_{GS} = 20 V to -20 V) and scanned at 0.2 V intervals. V_{th} was defined employing the constant current method.

4.2.2 Reliability under negative gate bias stress combined with light illumination

Figure 4.2 shows the transfer curve before and after 1 h negative gate bias illumination stress. The transfer curve was shifted negatively due to the positive charge trapping at the gate insulator layer. At the same time, the degree of hysteresis increased. When time evolution V_{th} was extracted at both forward and reverse sweeps, V_{th} difference between forward sweep and reverse sweep was increased as shown in Figure 4.3. Hysteresis is caused by donor-like interface states arising from Vo^{2+} as presented in Chapter 3.2. Transfer curve at the forward sweep is stretched out due to Vo^{2+}. Therefore, the shape of transfer curve is affected by the density and distribution profile of Vo^{2+}. However, the subthreshold region at both the forward and reverse sweep was hardly changed after the stress time as shown in Figure 4.4 and Figure 4.5. To compare the shape of subthreshold region, the transfer curve is normalized with the shifted V_{th} by the stress. It was found that the characteristics of Vo^{2+} at the interface was identical to that before the stress.

It was assumed that the hysteresis increased because negatively shifted V_{th} recovered due to the positive gate bias. To find out if the increase of hysteresis was recovery characteristics, the transfer curve was measured consecutively after the continuous 1 h negative gate bias illumination stress as shown in Figure 4.6. It was found that the increased hysteresis recovered immediately after 1st sweep measurement. When the positive gate bias was applied during the forward sweep, some instability factor

partially recovered so that the extent of V_{th} shift at the reverse sweep is smaller than that at the forward sweep. Figure 4.7 shows the effect of positive gate bias on the recovery characteristics. More positive gate bias was applied at the forward sweep, more recovery of V_{th} shift was observed.

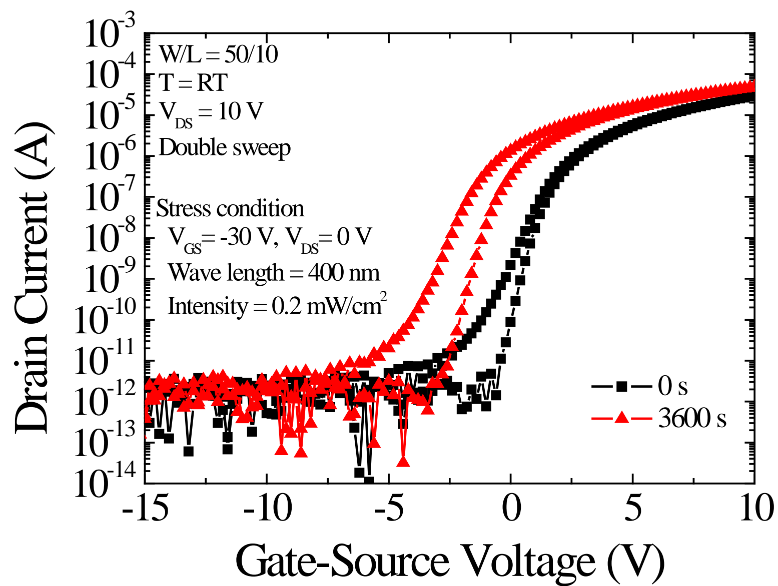


Figure 4.2 Transfer curves of double sweep measurement before and after 1 hour negative gate bias (-30 V) and illumination stress

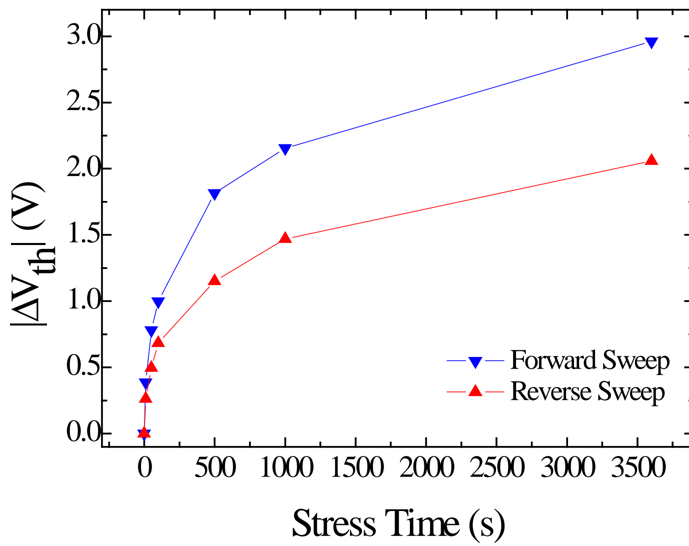


Figure 4.3 Time evolution of V_{th} shift of transfer curve at the forward and reverse sweep.

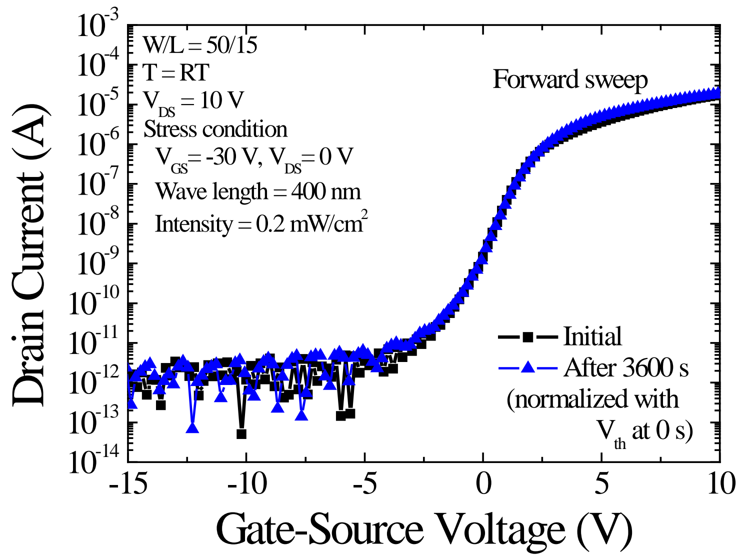


Figure 4.4 Transfer curves at the forward sweep before and after 1 hour negative gate bias (-30 V) and illumination stress, which is normalized by V_{th} shift.

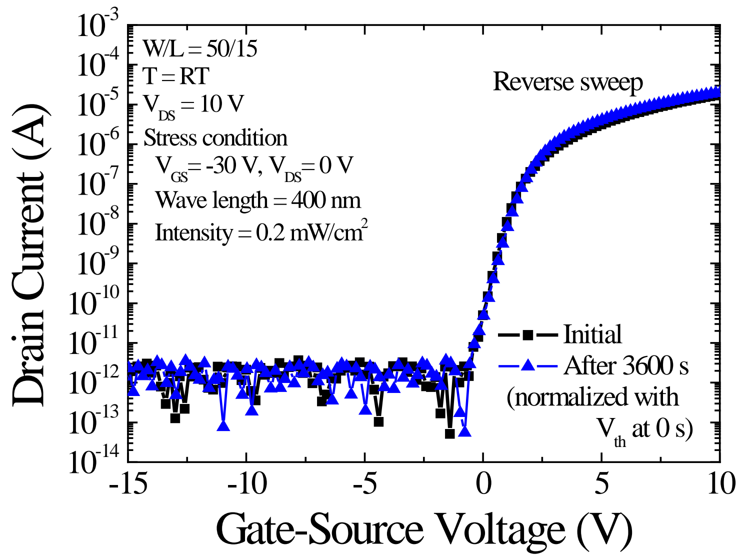


Figure 4.5 Transfer curves at the reverse sweep before and after 1 hour negative gate bias (-30 V) and illumination stress, which is normalized by V_{th} shift.

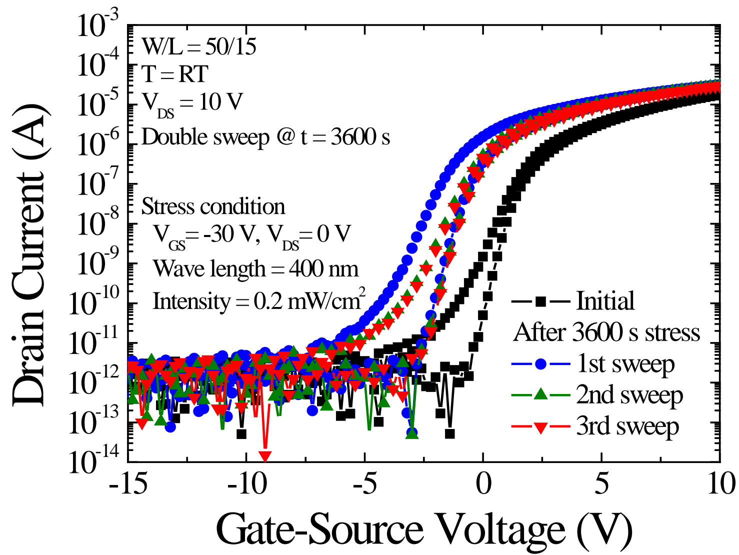


Figure 4.6 Consecutively measured transfer curves after 1 h negative gate bias (-30 V) and illumination stress.

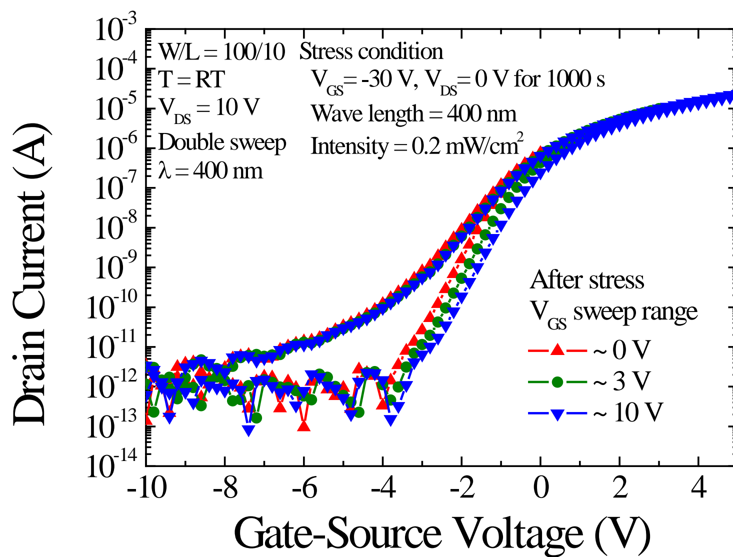


Figure 4.7 Transfer curves of double sweep measurement with various V_{GS} sweep range

4.2.3 Characteristics of fast recovery and time parameter

Negative V_{th} shift in IGZO TFTs are caused by photo-induced hole trapping [39] and Vo^{2+} accumulation at the gate insulator layer [38, 40]. When light is illuminated, Vo^{2+} is created and accumulates at the gate insulator layer due to the negative gate bias. Because of the positive charge at the gate insulator layer, transfer curve shifted negatively under negative gate bias illumination stress. Therefore, the recovery could occurr at the gate insulator layer or IGZO bulk as shown in Figure 4.8. The trapped charge at the gate insulator recovers due to the de-trapping of positive charge or recombination with electrons. Otherwise, created positive charge in IGZO bulk recovers with the recombination with electrons.

To investigate the recovery characteristic specifically, the stresses for 50 s, 100 s, 500 s, 1000 s, and 3600 s were performed individually. Because measuring the transfer curve enhances the fast recovery of V_{th} shift, the transfer curve measurements between the continuous stresses could disturb the instability process. Therefore, five different IGZO TFTs were used for 50 s, 100 s, 500 s, 1000 s, and 3600 s stress, respectively. The results are shown in Figure 4.9. The extent of recovery increased at the early stage of the stress and it was saturated from 500 s.

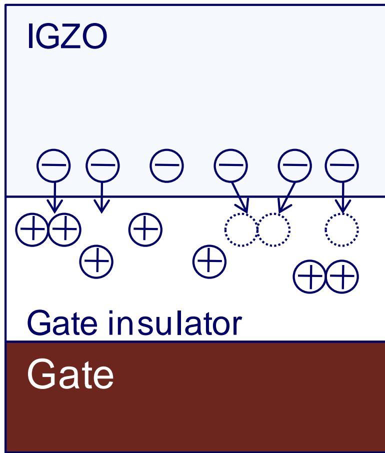
When the recovery occurred at the gate insulator layer, the recovering charge originated from the charge trapping of photo-induced holes or the accumulation of Vo^{2+}, which was diffused from IGZO bulk. The de-trapping of positive charge or recombination with electrons is possible mechanism of the fast recovery as shown in Figure 4.8 (a). In this case,

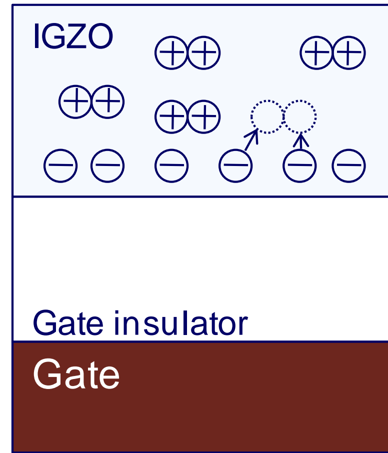
the positive charge will recover easily when it is close to the interface. When the stress is just started, the positive charges are trapped at gate insulator near the interface. However, the trapped charge is redistributed in the gate insulator layer as the stress is progressed [108]. Therefore, as the stress time is increased, the trapped charge will be located at deep sites in the gate insulator layer. It means that the large portion of V_{th} shift will recover at the early stage of the stress. Then, the recovery portion will decrease due to the charge redistribution as the stress is progressed. However, the recovery portion was increased at early stage of the stress (35 % at 50 s and 52 % at 100 s). The trapped charge at gate insulator was not main reason for the recovery characteristics.

Another possible source of the recovery is the created positive charge in IGZO bulk. When the recovery occurred in the IGZO bulk, the recovering charge could be Vo^{2+}. Vo^{2+} is generated by light illumination in IGZO bulk and it is accumulated at the gate insulator layer. The recovery might occur when Vo^{2+} combines with electrons as shown in Figure 4.8 (b). The amount of Vo^{2+} increases with time progressing and it is saturated when it reaches the steady state. This matches the recovery characteristic in Figure 4.9. Therefore, it is plausible that Vo^{2+} in IGZO bulk was responsible to the recovery. The generation process (G) can be expressed as time progress (t) as below.

$$G = A\exp(-t/\tau), \quad (4.3)$$

where A is a saturation value and τ relaxation time in generation of Vo^{2+}. By fitting the recovery characteristics in Figure 4.9, the relaxation time of 133.0 s was extracted. In this case, UV light was illuminated during the stress so that Vo^{2+} is created when oxygen vacancy (Vo) captures the photo-induced hole carriers [38, 73, 74]. It seems that a rather long time is required in Vo^{2+} creation in IGZO bulk when UV light is illuminated.





(a) (b)

Figure 4.8 Recovery characteristics (a) when the trapped positive charge at the gate insulator recovers and (b) when the created positive charge in IGZO bulk recover.

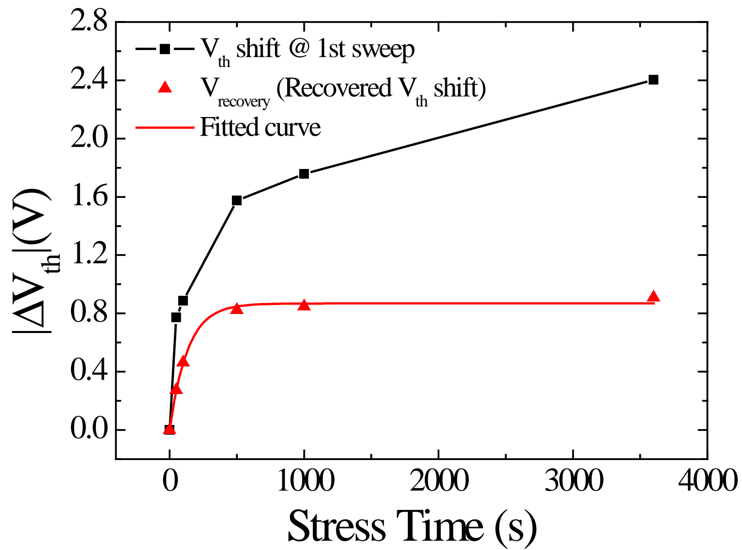


Figure 4.9 V_{th} shift and the extent of the fast recovery under negative gate bias (-30 V) and illumination stress when the stress time was 50 s, 100 s, 500 s, 1000 s, and 3600 s, respectively.

4.3 IGZO TFT with SiN_x gate insulator layer

4.3.1 Fabrication and Experimental Conditions

The inverted-staggered etch stopper structure IGZO TFTs with SiN_x gate insulator layer were fabricated. Molybdenum was deposited by DC sputtering on a glass substrate as the gate metal. 200 nm thick SiN_x gate insulator layer was deposited by plasma enhanced chemical vapor deposition (PECVD) and the 40 nm thick active layer was deposited by sputtering. After the active island was patterned, the 50 nm thick SiO_2 etch-stopper layer was deposited by PECVD and patterned by dry etching. Then, the 250 nm thick source and drain electrodes (Mo) were deposited by sputtering. The channel length is defined with the etch stopper layer length. The cross section of fabricated IGZO TFT is shown in Figure 4.10 and thickness of each layer is listed in Table 4.1.

An Agilent B1500A semiconductor parameter analyzer was used for measuring the devices. The transfer curves were measured with the double sweep from the forward sweep (from V_{GS} = -20 V to 20 V) to the reverse sweep (from V_{GS} = 20 V to -20 V). The stability characteristics of TFT were measured under negative gate bias stress of V_{GS} = -20 V and V_{DS} = 0 V under light illumination. 400 nm wavelength light was used with a band-pass filter from a Xenon lamp light source.

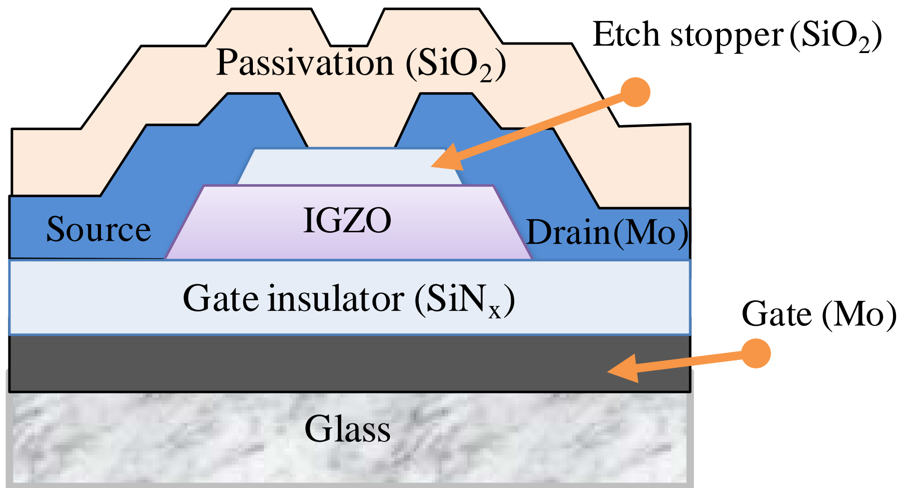


Figure 4.10 Cross-section of the inverted-staggered etch stopper structure IGZO TFTs.

Table 4.1 Layer information of the fabricated IGZO TFTs

Gate	Mo 250 nm
Gate Insulator	SiN_x 200 nm
Active	IGZO 40 nm
Source/Drain	Mo 250 nm
Passivation	SiO_2 100 nm + SiN_x 100 nm
Pad	IZO 90 nm

4.3.2 Reliability under negative gate bias stress combined with various intensities of light

Figure 4.11 shows IGZO TFT transfer curve in the dark state and under light illumination. The saturation mobility was 17.6 $cm^2/V \cdot s$ which is higher than that of SiO_2 gate insulator layer (10.1 $cm^2/V \cdot s$). On-off ratio was larger than 1×10^6 and SS was 246 mV/dec. When the negative gate bias stress was applied in the dark state for 7000 s, V_{th} was shifted negatively by less than 1 V. When 400 nm light whose intensity was 0.025 mW/cm^2 was combined with the negative bias stress, V_{th} decreased by about 8.7 V. Figure 4.12 shows the time evolution of the transfer curve. The SS was not changed significantly which implies that the main reason of the V_{th} shift is the charge trapping as reported in previous studies [39, 49]. Holes are generated in the active layer and drift to the interface between active layer and the gate insulator due to the effect of negative gate bias. Then, the accumulated holes at the channel are trapped to the interface/gate insulator. It was assumed that the charge trapping mechanism is based on the direct tunneling to gate insulator of holes [9].

In IGZO bulk, photo-induced holes might also contribute to increase of Vo^{2+}. However, Vo does not exist in SiN_x so that the trapped charge in gate insulator layer was hole carriers.

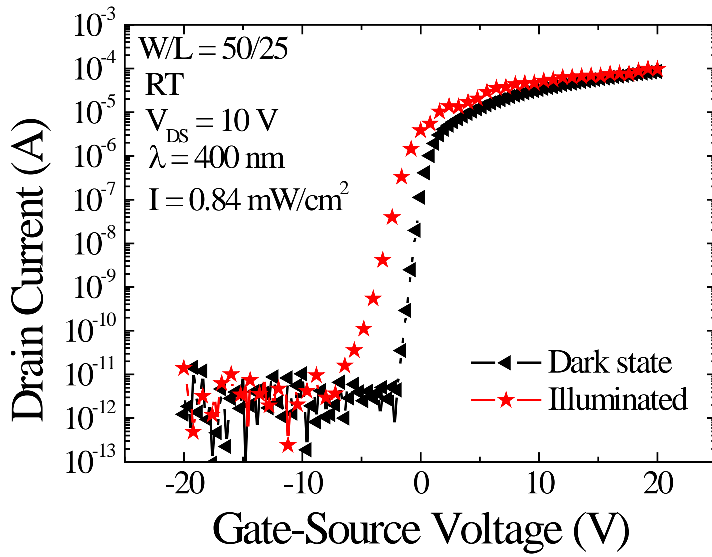


Figure 4.11 Transfer characteristics in the dark and under the 400 nm wave length light illumination.

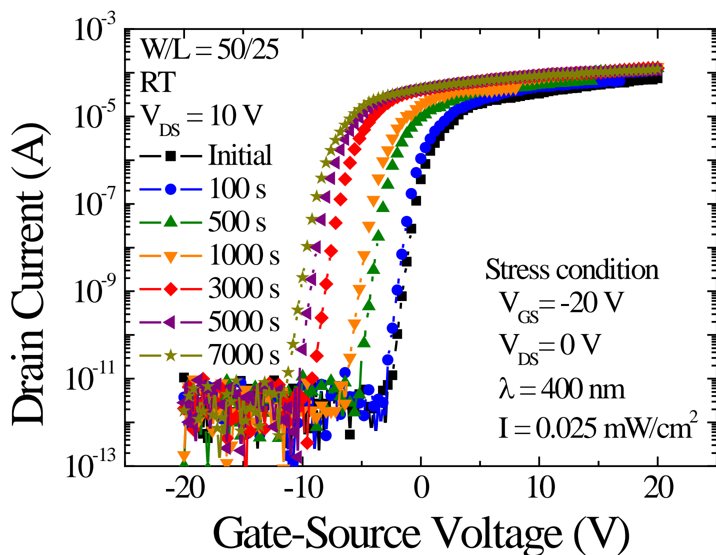


Figure 4.12 Transfer curves of IGZO TFTs subjected to negative gate bias (-20 V) stress with 400 nm wavelength light illumination (0.025 mW/cm^2).

4.3.3 Photo-induced carrier concentration vs. V_{th} shift

The negative bias stress under various intensities of light, such as 0.025, 0.05, 0.1, 0.27, 0.54, and 0.84 mW/cm^2 was performed and the resulting variation of the extent of the V_{th} shift (ΔV_{th}) according to the stress time is shown in Figure 4.13. As the intensity of light increased, ΔV_{th} was increased. Especially, ΔV_{th} increased rapidly when the stress was just started and it was intensified with the increase of the intensity of light. It was found that the significant difference under various intensities of light was determined at the early stage of the stress. It was tried to express numerically this phenomenon with $\mathrm{d}\Delta V_{th}/\mathrm{d}t$ at t = 0 s according to the intensity of light. As the intensity of light increased, $\mathrm{d}\Delta V_{th}/\mathrm{d}t$ at t = 0 s increased, having a linear relationship with the intensity of light as shown in Figure 4.13. $\mathrm{d}\Delta V_{th}/\mathrm{d}t$ was calculated with the V_{th} data of t = 0 s and t = 10 s.

The amount of photo-induced holes is proportional to the intensity of light and $\mathrm{d}\Delta V_{th}/\mathrm{d}t$ is proportional to the hole trapping rate. Thus, it can be inferred that the hole trapping rate increases with the increase of photo-induced holes at the channel. The charge trapping is a combination of holes and traps just like the recombination of the electron and hole in semiconductor. In semiconductor, the minority carrier is the determinant factor of the recombination rate. When 0.84 mW/cm^2 is illuminated, the incident photon flux is 1.69×10^{15} cm^{-2}s^{-1} and when the photons are absorbed in the whole active layer (4×10^{-6} cm), the generated hole concentration might be $\sim10^{14}$ cm^{-3} because the carrier lifetime is $\sim10^{-6}$ s

[97]. However, it has been reported that the trap density of SiN_x is about 10^{20} cm^{-3} [109]. The trap density is much larger than the hole concentration, so that the hole concentration is the determinant factor in the charge trapping. Therefore, the trapping rate of holes should be proportional to the hole concentration.

From the result of Figure 4.14, the variation of the trapping rate of holes can be determined according to the incident photon flux. At first, using the $d\Delta V_{th}/dt$ value of the y axis of Figure 4.14, the trapping rate of holes [#/cm^2-s] can be expressed as $C_n(d\Delta V_{th}/dt)/q$, where C_n is the SiN_x gate insulator capacitance. Then, the intensity of light of the x-axis of Figure 4.14 can be converted to the photon flux [#/cm^2-s]. The result is also listed in Figure 4.14. When the gradient is extracted, the ratio of the incident photon to the trapped holes is extracted and it was 1.53×10^{-3} %. It can be deduced that the tunneling probability from the channel to the gate insulator of a single hole is not altered even though the intensity of light is increased. The ratio of the incident photon to the trapped holes will be dependent on the properties of the gate insulator and charge transfer between the active layer and gate insulator. When the gate insulator has larger trap density than the photo-induced hole and the trapping rate increases, ΔV_{th} increases significantly with the increase of intensity of light.

However, the linear relationship between the trapping rate and the hole concentration at the channel is observed only when the stress is just started. This is because of the tunneling probability according to the

location of the traps of the gate insulator. The charge trapping is the combination of the trap site and holes with the tunneling probability. The tunneling probability of holes according to the trap location [110] as follows:

$$\text{tunneling probability} = t_0^{-1} \exp(-x/\lambda), \tag{4.4}$$

where λ is de Broglie wavelength, $1/t_0$ is the tunneling rate, and x is the location of the trap. The tunneling probability decays exponentially as the distance from the trap sites to the interface between the active layer and gate insulator layer increases. The trap density of SiN_x (N_0) is uniformly distributed in the bulk at a single energy level [111]. When the stress is started, all of the trap sites are empty, so that it can be observed that the trapping rate increases linearly with the intensity of light. The trap sites located near the interface can be filled with high probability, while far from the interface the trap sites remain largely unfilled. That is why $\mathrm{d}\Delta V_{\mathrm{th}}/\mathrm{d}t$ is large at the early stage of the stress and decrease as the stress is progressed. This mechanism is illustrated in Figure 4.15 and Figure 4.16.

Because it is considered that the charge trapping is caused by the direct tunneling of the holes, the detrapping of trapped charge during the stress is excluded. In this case, the saturation of ΔV_{th} might be reached by filling all of the available trap sites. When the hole concentration at the channel

increases, the trapping probability for the deeper trap sites increases. However, because the tunneling probability is exponential function of the tunneling distance of holes, it can be found that the maximum tunneling distance might be a logarithmic function of the intensity of light. The saturation value of ΔV_{th} might increase with the logarithmic function of the intensity of light.

Figure 4.17 shows the comparison of calculated saturation value of ΔV_{th} (ΔV_{th_sat}) with arbitrary units and the experimental value of ΔV_{th} at t = 7000 s. It was found that the calculated ΔV_{th_sat} is close to the empirical result. For a specific value of ΔV_{th_sat}, further investigation of the physical parameters of the gate insulator and oxide semiconductor, such as the trap density, effective mass of carriers and quantum efficiency, needs to be conducted.

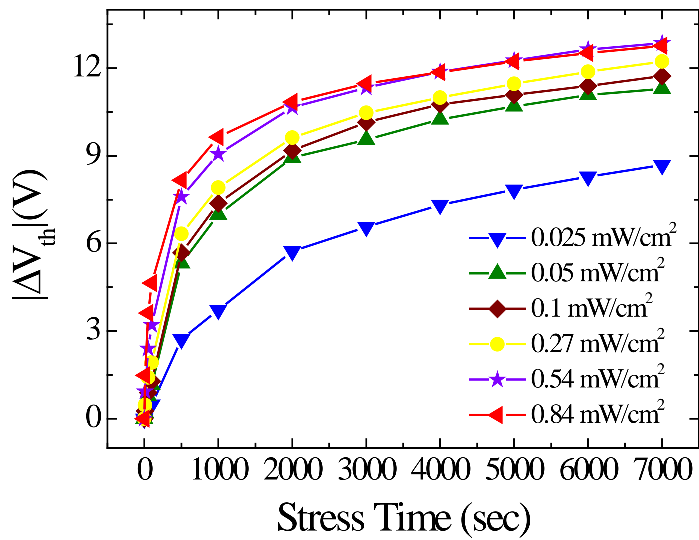


Figure 4.13 ΔV_{th} versus stress time of IGZO TFTs under negative gate bias stress (-20 V) with light illumination.

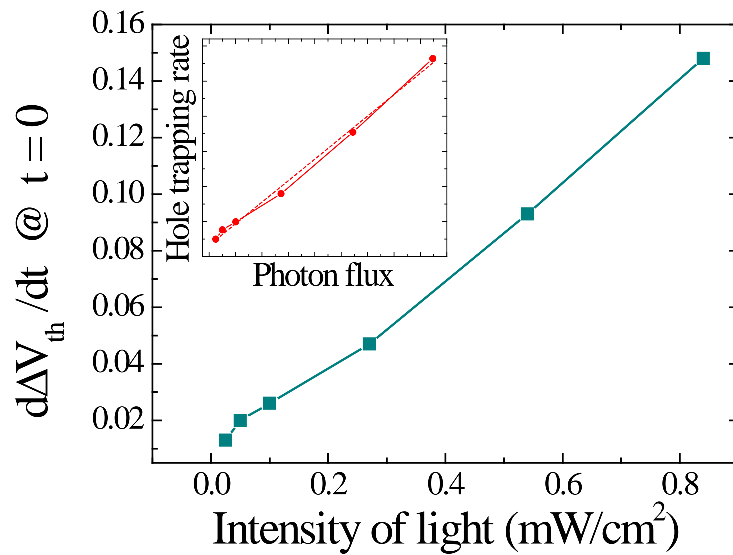


Figure 4.14 $\Delta V_{\mathrm{th}}/\mathrm{dt}$ when the stress time is 0 s.

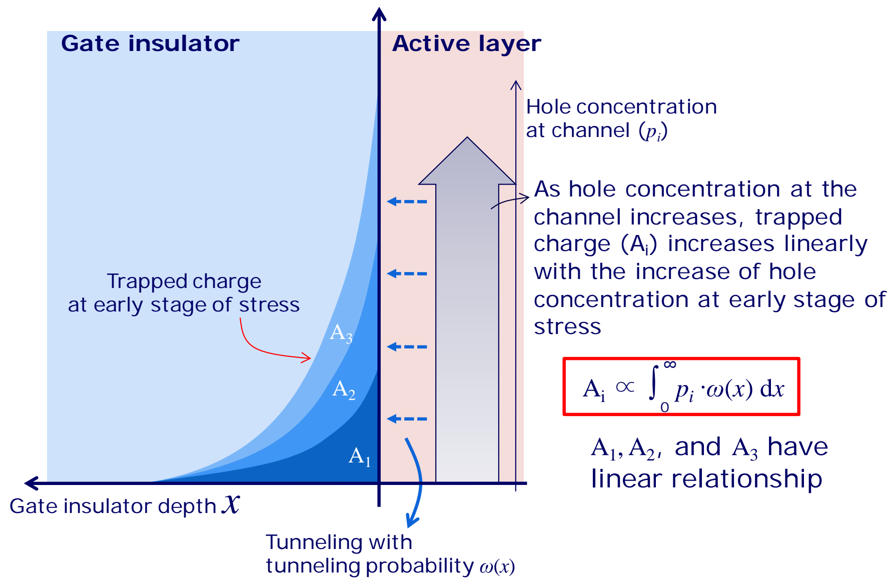


Figure 4.15 Trapping process according to the hole concentration at the channel when the stress is just started.

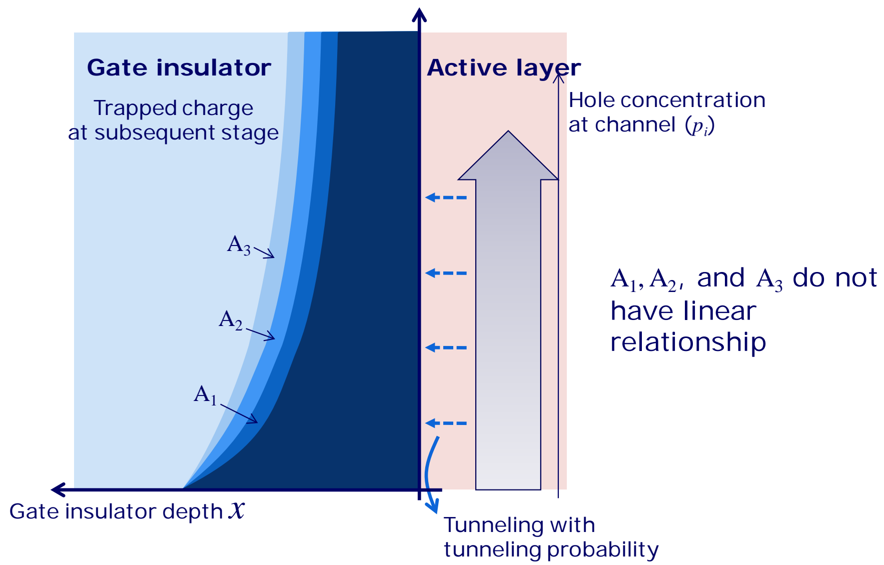


Figure 4.16 Trapping process according to the hole concentration at the channel when the stress is progressed.

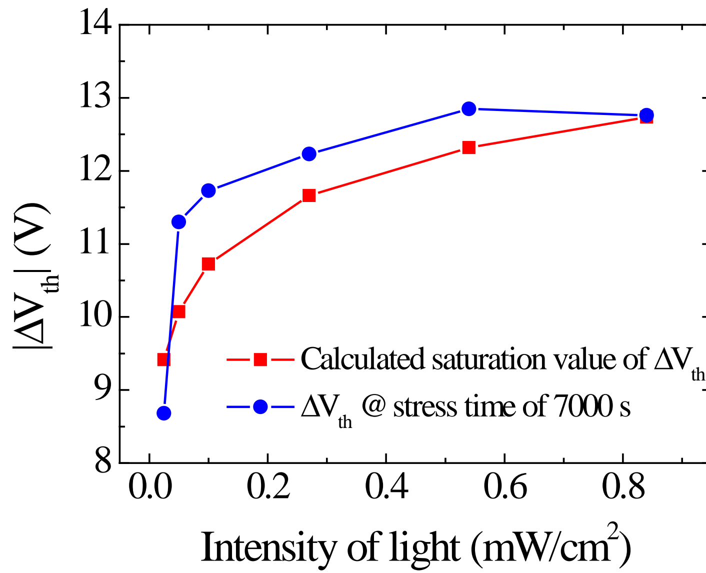


Figure 4.17 Comparison of ΔV_{th} at t = 7000 s from experimental result and calculated saturation value of ΔV_{th}.

4.4 Conclusion

In this chapter, the mechanism of instability of IGZO TFTs under negative gate bias UV illumination stress was investigated using different gate insulator material. When SiO_2 gate insulator is employed, the positive charge at the gate insulator caused by both photo-induced holes and Vo^{2+} contributes to V_{th} shift. However, Vo^{2+} does not exist in SiN_x such that only the charge trapping of photo-induced holes can be considered.

Using IGZO TFTs with SiO_2 gate insulator, Vo^{2+} generation process in IGZO bulk was observed. It was found that the relaxation time of Vo^{2+} generation in the IGZO bulk was 133.0 s. Both the Vo^{2+} generation at the interface and IGZO bulk depend on Vo density in IGZO film. Vo^{2+} at the interface caused hysteresis which was observed temporarily under illumination. Since the transfer curve shape was hardly changed after the stress, the created Vo^{2+} at the interface was not affected by the prolonged negative gate bias.

The reliability of IGZO TFTs under negative gate bias stress combined with various intensities of 400 nm wavelength light was studied with SiN_x gate insulator layer. The degradation of V_{th} was increased when the intensity of light increases. V_{th} was shifted faster as the intensity of light increased when the stress was just started. However, the trapping probability of a single hole was not changed. When the hole concentration at the channel increases due to the light illumination, the tunneling change to the deeper trap sites of gate insulator increases. Finally, the $\Delta V_{\mathrm{th_sat}}$, which is close to the empirical result, could be estimated. In IGZO

TFTs, the hole concentration at the channel and the characteristics of the gate insulator are the determinant factors.

Chapter 5 Characteristics of IGZO TFT on Flexible Substrate

In this chapter, the electrical characteristics and reliability of IGZO TFTs on flexible substrate are studied when TFTs was bent with 10 mm, 4mm, and 2mm bending radius. The IGZO TFTs were fabricated on a polyimide (PI) substrate with an inverted staggered structure. SiO_2 and SiN_x multi-buffer layer was deposited on the substrate to prevent the environmental effect, such as water or oxygen molecules.

5.1 Overview of flexible TFT

Flexible displays have attracted attention as a next generation flat panel display. Flexible plastic substrates have many advantages such as flexibility, ruggedness, light-weight and low cost compared to glass substrate. However, plastic substrate has a much lower thermal budget, so that the process temperature of the TFT fabrication should be sufficiently low. The most of commercially developed plastic substrates can stand low temperature below 250 °C, and the critical temperature of plastic substrates is determined by the inherent characteristics of plastics [112]. Limited process temperature affects the deposition of films and the physical properties of the films tend to be deteriorated with the decrease of the process temperature. Due to the lack of thermal treatment, characteristics of the TFTs on plastic may be degraded much compared with those of the TFTs on glass.

Polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polyether sulfone (PES), polycarbonate (PC), polyimide (PI), stainless steel, and thin glass were used as flexible substrate materials [113-120].

PI exhibits 275 °C of the continuous use temperature, orange color, high coefficient of thermal expansion (CTE), good chemical resistance, expensive cost, and high moisture absorption. PES exhibits 230 °C of the continuous use temperature, clear, good dimensional stability, poor solvent resistance, expensive cost, and moderate moisture absorption. PC exhibits 155 °C of the continuous use temperature, clear, poor CTE, inexpensive cost, moderate moisture absorption. PEN exhibits 150 °C of

the continuous use temperature, clear, moderate CTE, good chemical resistance, inexpensive cost, moderate moisture absorption. PET exhibits 120 °C of the continuous use temperature, clear, moderate CTE, good chemical resistance, inexpensive cost, moderate moisture absorption. Table 5.1 summarizes the continuous use temperature and characteristics of the plastic substrates [119, 120].

Flexible displays are demonstrated with various active materials such as amorphous silicon, low temperature poly silicon, single crystalline silicon, and oxide semiconductor on various flexible substrates [37, 113-118, 121-133]. In the aspect of mechanical flexibility, organic TFTs are quite suitable for flexible display. However, their low field-effect mobility and instability should be improved for flexible display backplane. For the low temperature process and high device performance, oxide TFTs are considered as a promising candidates for flexible displays. Because of the high mobility, good uniformity, and robust stability, it is a powerful alternative to the organic-based TFTs or a-Si:H TFTs.

For the success of flexible displays, it is very important to understand the effect of mechanical bending on TFT characteristics. When a film on a flexible substrate is bent with radius R as shown in Figure 5.1, the top surface is in tension and the bottom is in compression. There is the neutral surface inside the sheet having no strain. The strain of the device changes according to R.

The response of a-Si:H TFTs to mechanical strain is summarized as illustrated in Figure 5.2 [134]. In tension, TFTs fail due to crack caused by

pre-existing defects. On the other hand, they fail because the film delaminated from the substrate under compressive stress. There are transition regimes where the TFTs are metastable. Mobility of a-Si:H TFTs increases depending on strain (ε) as $\mu = \mu 0 \ (1+26\times\varepsilon)$, where tensile strain is positive and compressive is negative [135]. In crystalline silicon, the mobility increases in tension because interaction of carriers with atom decreases. In a-Si:H, the slope change of the conduction-band tail might cause the mobility change in strained condition. However, physical origin has not been clearly defined.

In flexible IGZO TFTs, there are a few reports about the electrical performance depending on mechanical strain. It was reported that critical strain values about device failure are similar to a-Si:H TFTs [116]. Device performance was stable in the range of ~0.2%–0.4% of tensile strain and more than ~0.8%–0.9% of compressive strain. From these, it was deduced that inorganic layers except for IGZO semiconductor might limit the bending performance. For bending strains -0.3%–0.3% (compressive to tensile stress), decrease of Vth and increase of μ and SS were observed in IGZO TFTs [117]. Mobility change was explained by the distance change between the atoms of the semiconductors which influence the current flow. The increase of distance between the atoms decreases the energy level splitting (ΔE) so that more electrons are excited at the same condition. The electron concentration increase explains the decrease of Vth. To guarantee the stability of IGZO TFTs implemented in flexible displays, the stability under the mechanical strain should be investigated.

However, it has been reported scarcely.

Table 5.1 The continuous use temperature and characteristics of the plastic substrates [119, 120].

Continuous use temperature	Material	Characteristics
275 °C	Polyimide (PI)	Orange color, high CTE, good chemical resistance, expensive, high moisture absorption
230 °C	Polyether Sulfone (PES)	Clear, good dimensional stability, poor solvent resistance, expensive, moderate moisture absorption
155 °C	Polycarbonate (PC)	Clear, poor CTE, inexpensive, moderate moisture absorption
150 °C	Polyethylene naphthalate (PEN)	Clear, moderate CTE, good chemical resistance, inexpensive, moderate moisture absorption
120 °C	Polyethylene terephthalate (PET)	Clear, moderate CTE, good chemical resistance, inexpensive, moderate moisture absorption

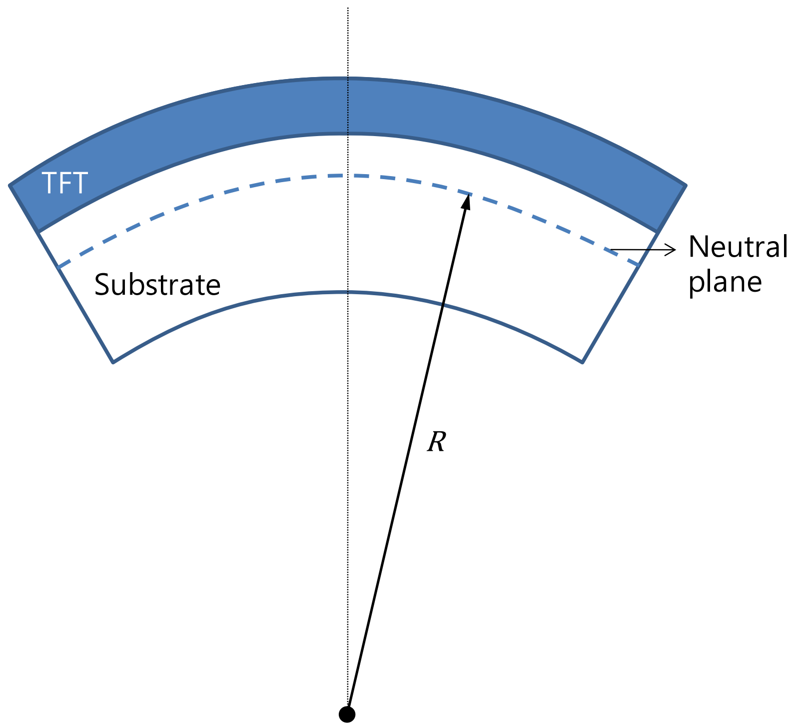


Figure 5.1 A film-on-plastic structure bent to a cylindrical roll.

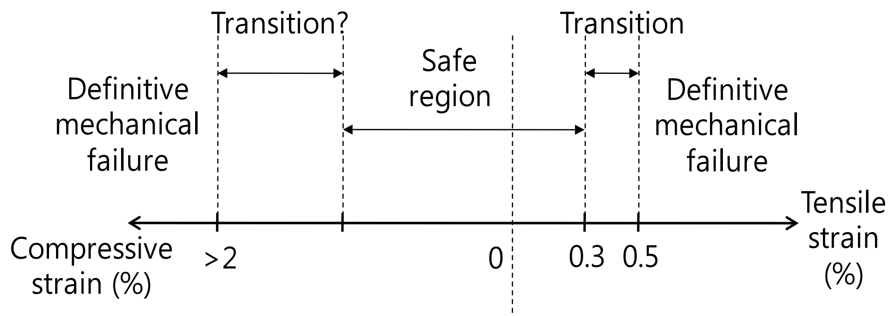


Figure 5.2 Summary of the response of a-Si TFTs to mechanical strain [134].

5.2 Fabrication and Experiment of Flexible IGZO TFT

The IGZO TFTs were fabricated on a PI substrate with an inverted staggered structure. Figure 5.3 shows the cross sectional view of the fabricated IGZO TFTs. PI is spin-coated onto glass substrate, in order to overcome difficulties in handling flexible freestanding plastic substrates, eliminating the problem of plastic shrinkage with high temperature processing and allowing the use of standard semiconductor equipment. Thickness of PI was about 18 μm.

An inorganic buffer layer, composed of SiO_2 and SiN_x multi-layer, was deposited over the entire substrate area by plasma enhanced chemical vapor deposition (PECVD). Multiple barrier layers provide a long-term stability. Vapor diffusion is delayed by multilayer because of a long effective diffusion path length [134]. Mo were deposited and patterned as the gate electrode. SiO_2 of 2,000 Å thickness was then deposited by PECVD and served as the gate dielectric layer. The IGZO (In:Ga:Zn = 1:1:1) layer with a thickness of 500 Å was deposited by sputtering. The SiO_2 etch stop layer was deposited by PECVD. The source and drain were formed by depositing a layer of Mo and were patterned by dry etching. The SiO_2 layer was used as a passivation layer. After device fabrication, the PI substrates were released by laser irradiation process. Table 5.2 summaries the layers information of the fabricated flexible IGZO TFTs.

Figure 5.4 (a) shows a photograph of bending measurement system. The electrical characteristics and reliability of IGZO TFTs were measured

under 2 mm, 4 mm, and 10 mm bend radius conditions. Bending direction was perpendicular to channel as illustrated in Figure 5.4 (b). When TFT was bent perpendicular to channel direction, the current flow might be directly affect by the mechanical strain.

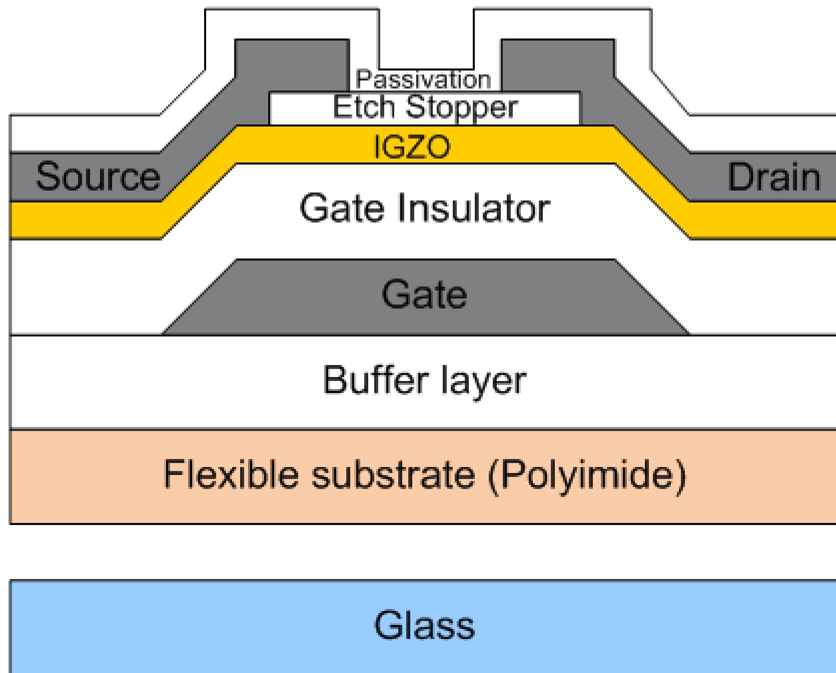
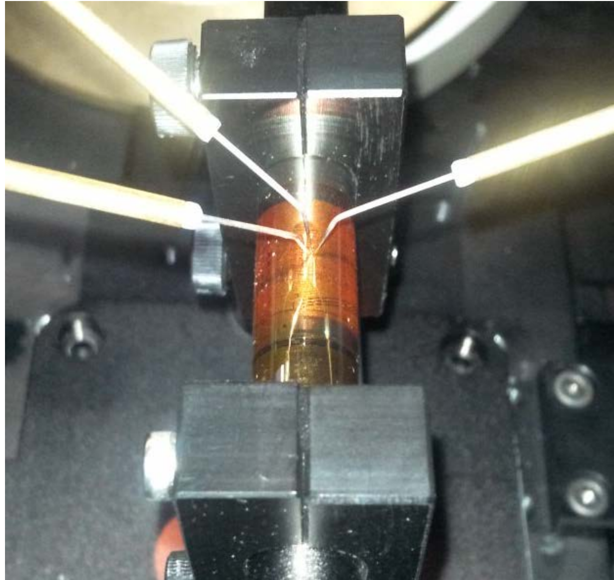


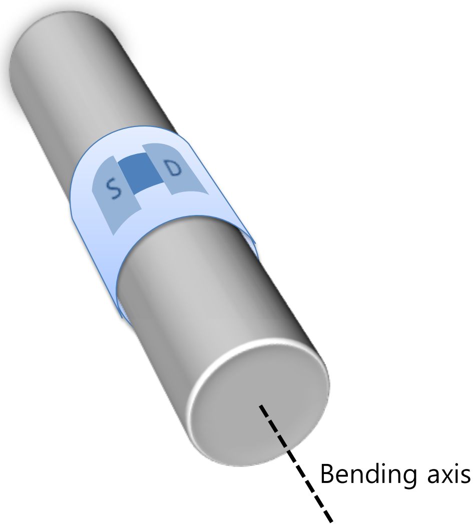
Figure 5.3 Cross-section of the inverted-staggered etch stopper structure IGZO TFTs on flexible substrate.

Table 5.2 Layer information of the fabricated flexible IGZO TFTs

Layer	Material	Equipment
Buffer layer	SiO_2 / SiN_x multi-layer	PECVD
Gate	Mo	DC sputter
Gate Insulator	SiO_2 200 nm	PECVD
Active	IGZO 50nm	DC sputter
Etch stopper	SiO_2 50 nm	PECVD
Source/Drain	Mo	DC sputter
Passivation	SiO_2 200 nm	PECVD



(a)



(b)

Figure 5.4 (a) A photograph of bending measurement system. (b) Schematic showing bending direction perpendicular to channel.

5.3 The effect of mechanical bending on electrical characteristics of Flexible IGZO TFT

Transfer curve of flexible IGZO TFT is shown in Figure 5.5. The saturation mobility and SS were 10.8 cm^2/V·s and 351 mV/dec, respectively. It was found that the device performance is comparable to IGZO TFTs on the glass substrate. Even under 4 mm bending radius, the electrical characteristics such as V_{th}, mobility, and SS were hardly changed with mechanical bending in the dark when the electrodes were applied by no bias. In the previous experiment, the maximum strain was about 0.3 % with 9 mm [117] or ~0.8–0.9 % with 5 mm bending radius [116] and the device failure or the characteristic change was observed.

To find out the mechanical strain on the fabricated devices, the position of the neutral axis (y_0) and the bending strain of the each layer were calculated by following equation.

$$y_0 = \frac{\sum_i y_i E_i d_i}{\sum_i E_i d_i}, \quad (5.1)$$

$$\varepsilon_i = \frac{y_i - y_0}{R}, \quad (5.2)$$

where y_i, is centroidal position of each layer based on Figure 5.6 and E_i,

and d_i are Young's modulus and thickness of the film and R are the bending radius. The neutral plane was placed in PI near the buffer layer. Figure 5.7 shows the calculated strain of each layer. Even under 2 mm bending radius, the strain on TFT region was less than 0.1 %. That is why the TFT are more stable than the previous report although it is bent with 2 mm radius. Because the substrate thickness (18 μm) was much smaller than the previous reports (~50 μm) the strain on TFT can be reduced.

When the device was kept flat or bending state for 1 day, V_{th} was shifted negatively. As listed in Table 5.3 and Table 5.4, the amount of V_{th} shift was insignificant and it was not affected by the physical size of the device and mechanical bending.

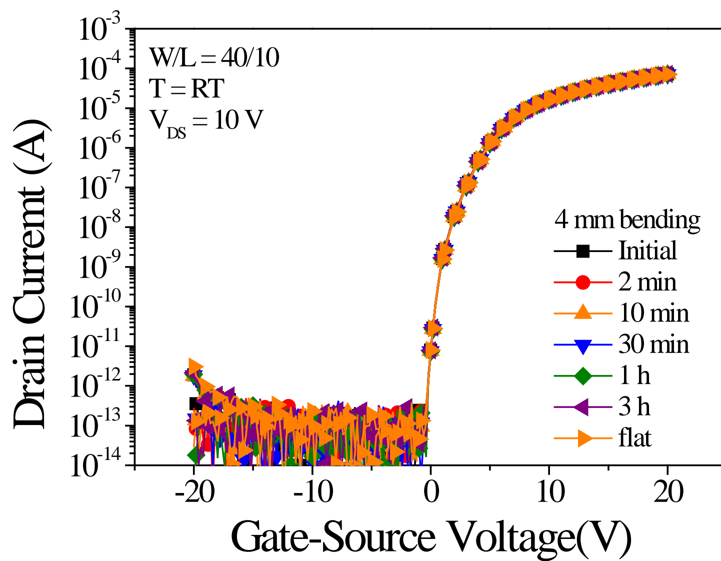


Figure 5.5 Transfer characteristics of flexible IGZO TFT under the bending of 4 mm radius.

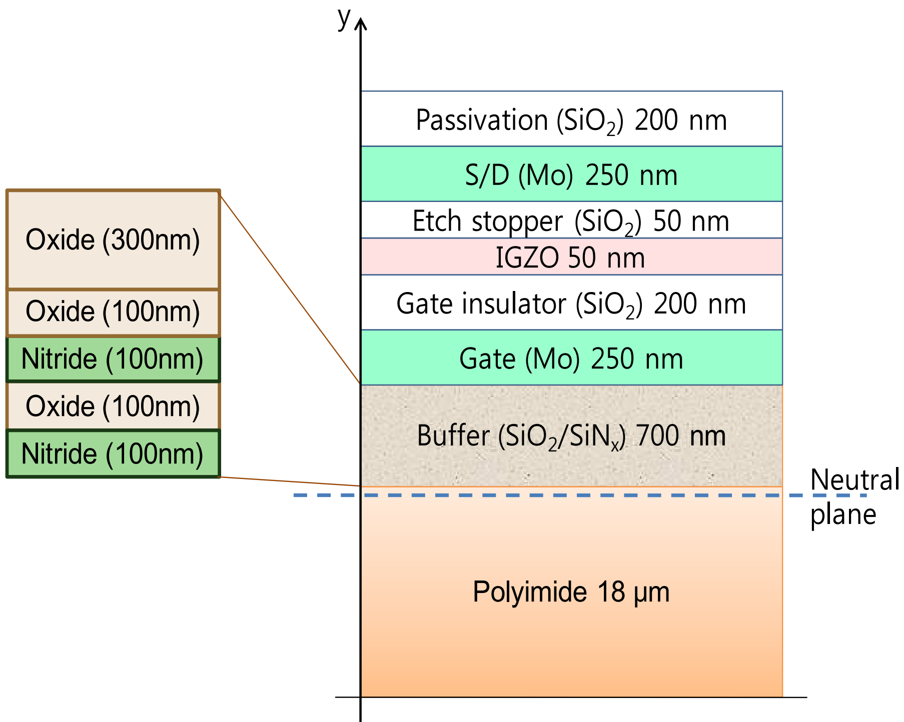


Figure 5.6 Schematic of flexible IGZO TFTs on plastic substrate.

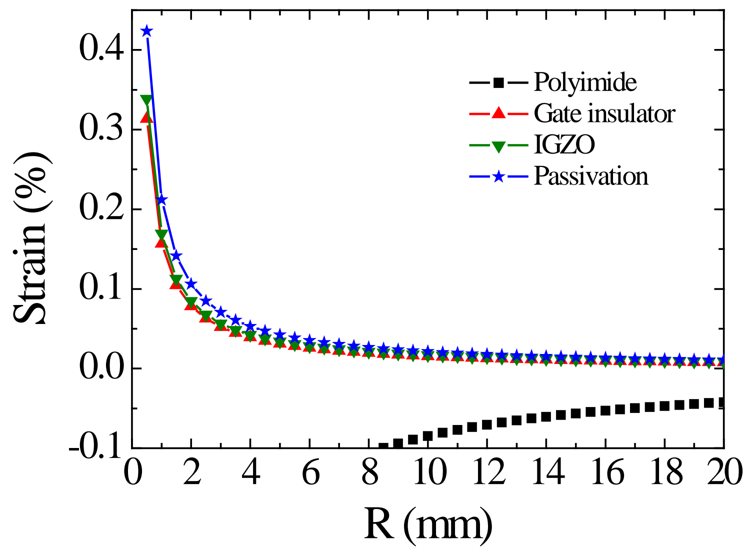


Figure 5.7 Calculated strain of each layer

Table 5.3 Extent of V_{th} change depending on length of TFTs under 4 mm bending radius when width was 25 μm.

L (μm)	$\|\Delta V_{th}\|$ (V)	State
10	0.04	Flat
6	0.04	Bending R = 4 mm Perpendicular to channel direction
7	0.03	
8	0.05	
10	0.05	
12	0.06	
14	0.05	
16	0.06	

Table 5.4 Extent of V_{th} change depending on width of TFTs under 4 mm bending radius when length was 10 μm.

W (μm)	$\|\Delta V_{th}\|$ (V)	State
25	0.04	Flat
25	0.05	Bending R = 4 mm Perpendicular to channel direction
30	0.04	
40	0.07	
50	0.03	
60	0.04	

5.4 The effect of mechanical bending on stability of Flexible IGZO TFT

The stability under -30 V gate bias was examined with various bending radius. The results are shown in Figure 5.8. When the bending radius was 2 mm, V_{th} was shifted more negatively than 4 mm, 10 mm, or flat state. Tensile strain on TFTs accelerated the device degradation. Under 10 mm bending radius, however, the extent of V_{th} shift was smaller than that under 4mm and flat state. In Chapter 5.3, the tensile strain in IGZO TFTs increases when the bending radius increases. However, the trend of V_{th} shift did not follow the strain.

When PI substrate was released by laser annealing, the film bended itself. Figure 5.9 shows the released sample and 10 mm bending chuck. It was found that the curvature of the released sample was about 10 mm. Because TFTs are built on substrates layer by layer, the built-in stress arises from a mismatch strain. This mismatch causes the substrate to bend with curvature R_0. However, during the TFT fabrication, PI substrate is flat, so that the film is in strain.

To find out the effect of the built-in strain on TFTs, negative gate bias stress was performed when the bending direction was parallel to the channel. As shown in Figure 5.10, the trend of V_{th} shift depending on bending radius changed when the bending direction changed. The degree of V_{th} shift was similar in 10 mm bending and flat state. When the bending radius was decreased to 4 mm and 2 mm, V_{th} shift was increased. The

built-in strain was probably biaxial in the sample. However, when the built-in strain parallel to channel direction was stronger than perpendicular, the sample might bend with the axis perpendicular to channel. When TFT is bent in parallel to channel, the strain in IGZO TFT will follow Figure 5.7. In Figure 5.11, the trends of mechanical strain and $|\Delta V_{th}|$ are compared. When bending direction was parallel to channel, V_{th} shift was increased with mechanical strain.

Usually, the built-in stress is not considered when the external strain is analyzed. However, the results suggested that the built-in stress cannot be ignored when the direction of strain is same with the built-in strain. Considering the curvature produced by build-in stress, the effective bending radius $1/R' = 1/R - 1/R_0$ should substitute in (5.2) [134]. As shown in Figure 5.12, the TFT is in tension with 2 mm and 4 mm bending radius and compression when it is flat. It was found that both tensile and compressive strain accelerated the V_{th} shift under gate bias stress.

Depending on the strain, the atomic distance of semiconductor is changed, which in turn affects the energy band structure. In crystalline Si, the energy gap is decreased by tensile or increased by compressive strain due to both E_V and E_C shift [136]. E_C shift is closely related to electron transport while E_V shift changes hole transport. In IGZO TFTs, energy band structure might be affected by mechanical strain. V_{th} or mobility which is determined by electron transport was hardly changed by strain unless negative gate bias stress was applied. However, V_{th} shift under negative gate bias stress, is a function of hole carrier concentration

(Chapter 4.3) and band structure of E_V [63]. This suggested that E_V shift might be caused by the mechanical strain in IGZO TFTs. Because the stretched exponential equation, (4.1), includes the effective energy barrier of the carriers, the effect of stain on energy band of IGZO TFTs was analyzed by fitting the time evolution of V_{th} shift. The solid lines in Figure 5.8 and Figure 5.10 are the fitted lines by stretched exponential and the parameters A, τ, and β are listed in Table 5.5 and Table 5.6. A is the V_{th} shift at infinite time, and $\tau = \tau_0 \exp(E_a/kT)$ represents the characteristic trapping time of carriers, where the thermal activation energy is given by $E_a=E_\tau \cdot\beta$. β is the stretched-exponential exponent and E_τ is the average effective energy barrier that the electrons in the IGZO TFT channel. When bending axis was perpendicular to channel, A and τ were increased with both compressive and tensile strain while β kept about 0.51. The increase in τ indicated that E_V shifted toward E_C as shown in Figure 5.13. Because E_V difference between the gate insulator and IGZO was increased, energy barrier for charge trapping was increased. At the same time, the hole concentration might be increased by E_V shift toward E_F, which is closely related to the increase in A. On the other hand, when bending axis was parallel to channel, both A and τ were decreased with tensile strain. This can be explained by E_V shift away from E_C as shown in Figure 5.14. Due to the decrease in E_V difference between the gate insulator and IGZO, the energy barrier for charge trapping decreases. The decrease in A might be caused by the decrease of hole concentration.

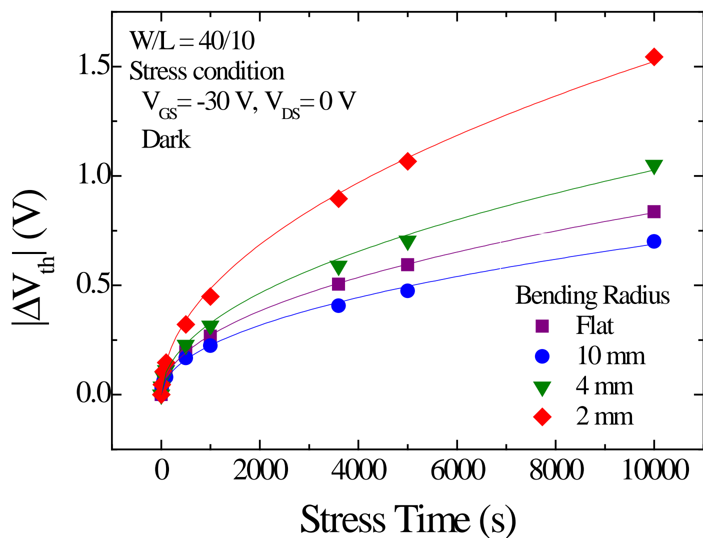


Figure 5.8 Time evolution of V_{th} shift under negative gate bias (-30 V) stress depending on bending radius. Bending axis was perpendicular to channel

Figure 5.9 Flexible IGZO TFT sample and 10 mm bending chuck.

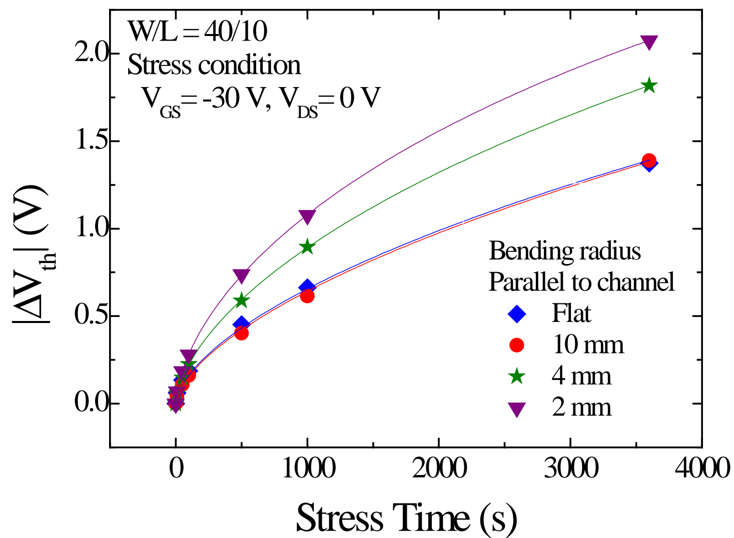


Figure 5.10 Time evolution of V_{th} shift under negative gate bias (-30 V) stress depending on bending radius. Bending direction was parallel to channel

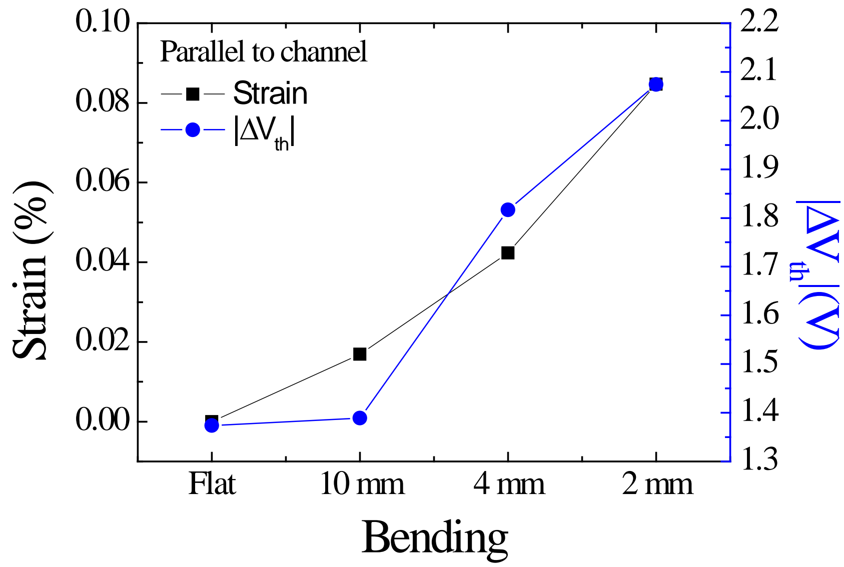


Figure 5.11 Comparison of the trends of mechanical strain and $|\Delta V_{th}|$ when bending direction was parallel to channel.

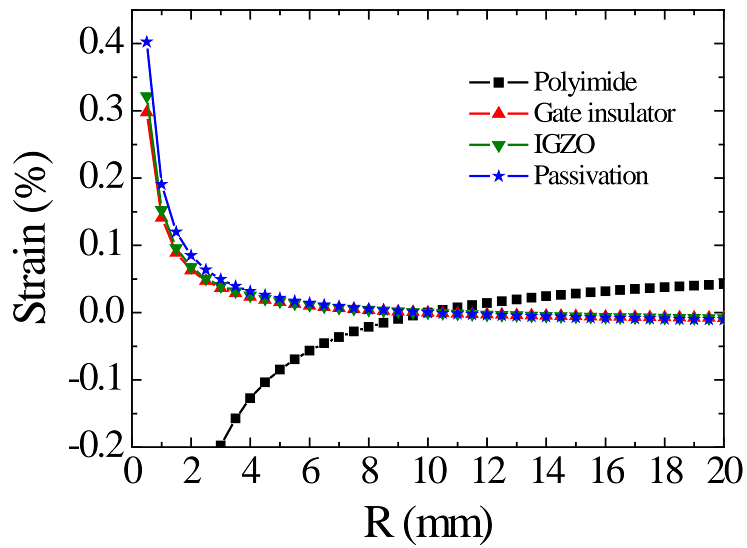


Figure 5.12 Calculated strain of each layer considering the built-in stress

Table 5.5 Fitting parameters of stretched exponential equations of V_{th} shift depending on various bending radius when bending axis was perpendicular to the channel direction.

R	A	τ	β	Strain (%)
Flat	7.7	7.5×10^5	0.51	-0.017
10 mm	5	4.3×10^5	0.51	-
4 mm	11.2	1.0×10^6	0.51	0.025
2 mm	19.3	1.3×10^6	0.51	0.068

Table 5.6 Fitting parameters of stretched exponential equations of V_{th} shift depending on various bending radius when bending axis was parallel to the channel direction.

R	A	τ	β	Strain (%)
Flat	10.8	9×10^4	0.62	-
10 mm	12.0	1.0×10^5	0.62	0.017
4 mm	6.8	2.4×10^4	0.62	0.042
2 mm	4.9	1.0×10^4	0.62	0.085

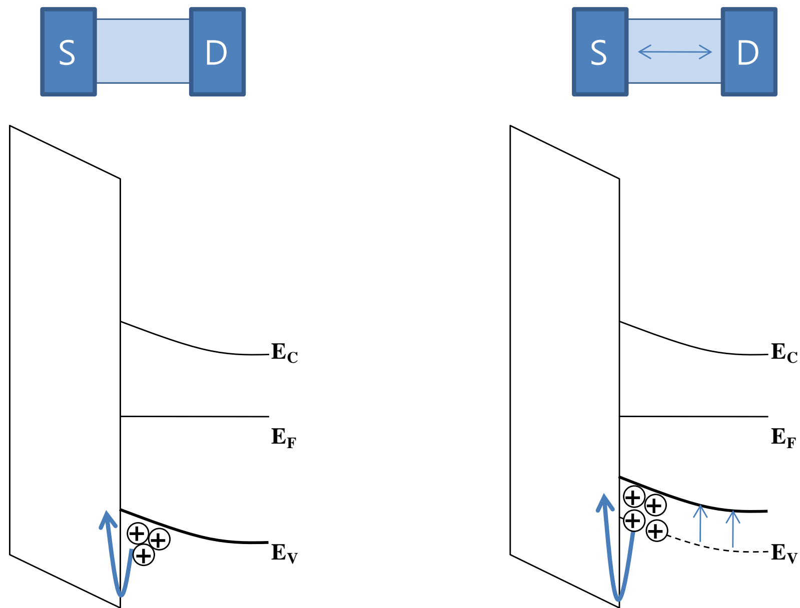


Figure 5.13 Energy band structure when bending axis was perpendicular to channel direction.

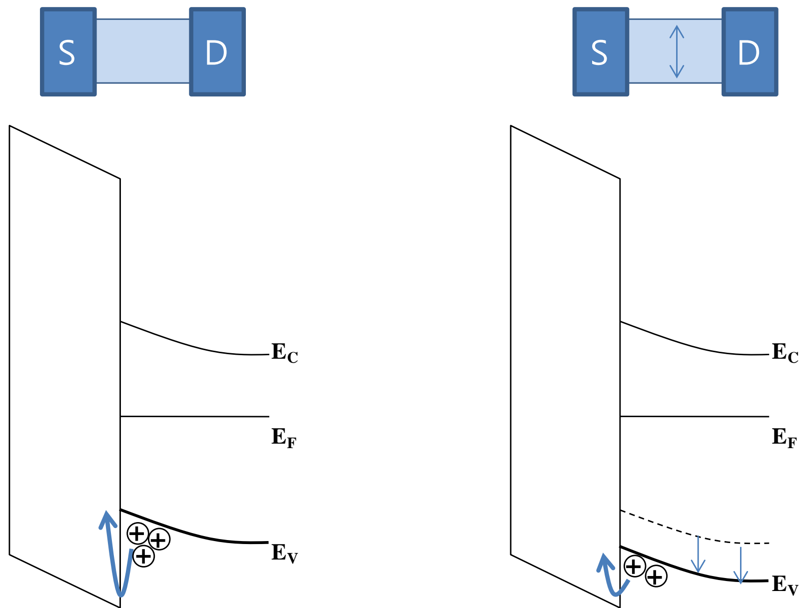


Figure 5.14 Energy band structure when bending axis was parallel to channel direction.

5.5 The effect of light on flexible IGZO TFTs

In flexible displays, TFTs are also exposed to visible light due to the backlight. Therefore, it is important to examine the effect of light on reliability of flexible IGZO TFTs. In this chapter, the negative gate bias stress of -30 V was performed for 10000 s when 450, 550, and 650 nm wavelength light was illuminated. The light intensity of 450, 550, and 650 nm light were about 0.4, 0.39 and 0.21 mW/cm^2, respectively. IGZO TFTs were bent with 4 mm bending radius. From the results listed in Figure 5.15, it was found that the light having photon energy less than E_{otp} of IGZO did not affect the degree of V_{th} shift. When 550 nm and 650 nm wavelength light was illuminated, V_{th} was shifted as much as that in the dark. However, V_{th} shifted more negatively under 450 nm illumination. Because IGZO semiconductor has tail state near E_C and E_V the absorption of photon is inevitable. Figure 5.16 show the time evolution of ΔV_{th} of IGZO TFTs when the negative gate bias of -30 V was applied under 400 nm and 450 nm wavelength light. Under 400 nm wavelength light, V_{th} shift is increased due to the photo-induced hole carriers. In this experiment, the intensity of 400 nm light was 0.2 mW/cm^2. Based on the absorption coefficient in Figure 5.17 which was obtained from transmittance of IGZO thin film, the absorption coefficient of 400 nm and 450 nm was around 1×10^4 cm^{-1} and 5×10^3 cm^{-1}, respectively. When the photo-induced hole carrier concentration was calculated, it was 1.6×10^{13} cm^{-3} under 400 nm and 1.8×10^{13} cm^{-3} under 450 nm. The photo-induced hole carrier concentration under 450 nm wavelength light was almost

same with 400 nm. The negative shift of V_{th} under 450 nm was caused by the photo-induced hole carrier in IGZO. From the results, it was suggested that the passivation layer on the top of the device and buffer layer on the substrate successfully prevent the ambient oxygen and moisture.

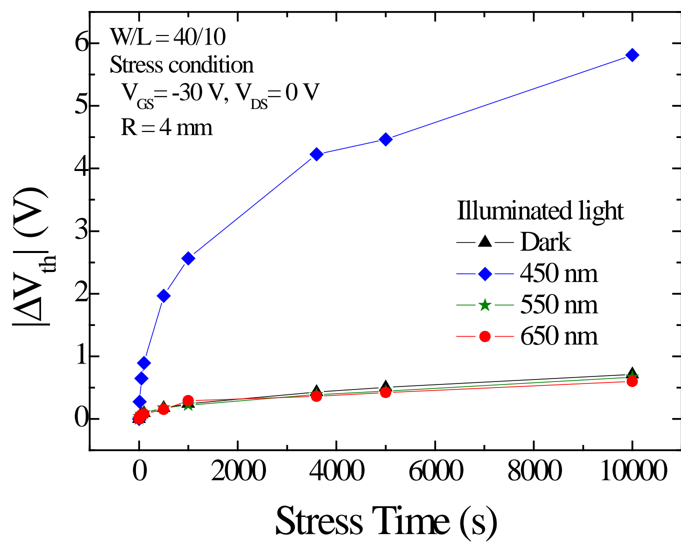


Figure 5.15 Time evolution of ΔV_{th} of IGZO TFTs when the negative gate bias of -30 V was applied under visible light.

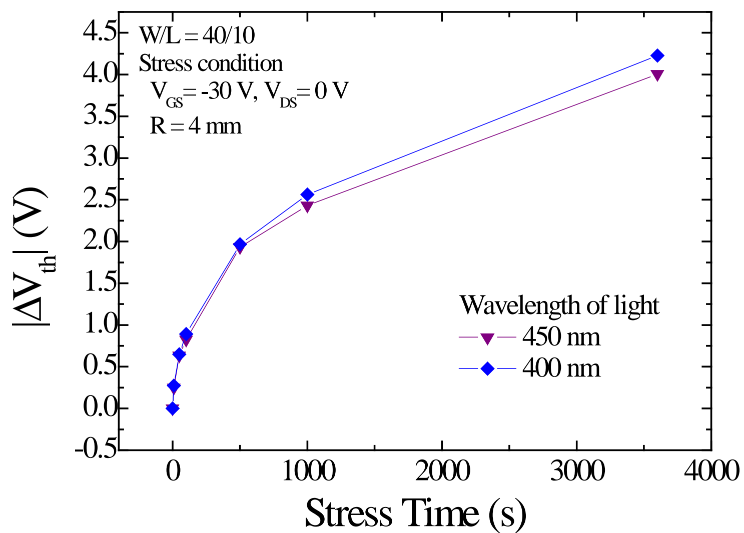


Figure 5.16 Time evolution of ΔV_{th} of IGZO TFTs when the negative gate bias of -30 V was applied under 400 nm and 450 nm wavelength light.

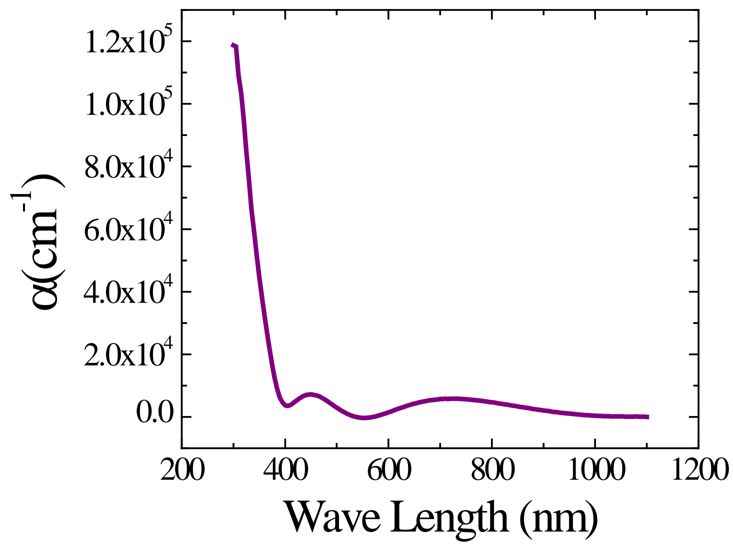


Figure 5.17 Absorption coefficient of IGZO semiconductor

5.6 Conclusion

With spin-coated thin PI substrate, IGZO TFTs showed very stable characteristics in 2 mm bending radius. The mechanical strain in TFTs was less than 0.1 % even under 2 mm bending. However, V_{th} shift was increased with tensile or compressive strain under negative gate bias stress. Stretched-exponential fitting of V_{th} shift showed that charge trapping energy barrier increased with strain when bending axis was perpendicular to channel. On the contrary, it decreases under the bending parallel to channel. This suggested that E_V might shift toward E_C under mechanical bending perpendicular to channel and it shift away from E_V when bending axis was parallel to channel.

To reduce the mechanical strain in TFTs, the neutral plane should be placed in TFT with a suitable encapsulation layer. The effect of mechanical bending on TFTs can be minimized when

$$E_s d_s^2 = E_e d_e^2, \quad (5.3)$$

where E_s and E_e are Yong's modulus and d_s and d_e are thickness of the substrate and encapsulation layer [134].

The effect of visible light on flexible IGZO TFTs was also examined. Under 550 and 650 nm light, the V_{th} degradation was almost same with that in the dark state. Due to the tail state near E_C and E_V, the light was absorbed

in IGZO under 450 nm light so that V_{th} shift was increased. Although the light intensity used in this experiment was much stronger than display application, the further improvement is required under light illumination. However, from the result it was confirmed that the passivation layer buffer layer prevent the ambient oxygen and moisture successfully.

Chapter 6 Summary

In this thesis, the effect of UV light on the initial and reliability characteristics of IGZO TFTs were intensively investigated.

Firstly, the photo-induced hysteresis and I_{off} of IGZO TFT in various intensities of light was investigated. Vo^{2+} is created at the interface when Vo captures the photo-induced holes. When the electrons are induced by gate bias, Vo^{2+} can recover to Vo with capturing electrons. The decrease in V_{th} and increases in SS could be explained by Vo^{2+} at the interface. However, significant hysteresis could not be explained without considering the response time of Vo^{2+}. Because the creation and recovery of Vo^{2+} could not occur immediately with V_{GS} change, the hysteresis was observed under the UV light. In this study, a long response time ($\sim 10^{0}$ s) was extracted by calculation. The ambient effect was prevented by the

passivation layer so that the response time might express the generation of Vo^{2+} at the interface between IGZO and SiO_2 gate insulator. When I_{off} was considered to be the drift current of the photo-generated carriers, the I_{off} of the experimental results was much lower than the calculated values. Furthermore, I_{off} showed a rapid non-linear increase with light intensity, whereas the photo-current should be expected to increase linearly with light intensity in crystalline semiconductors. In this case, I_{off} increased because of Vo^{2+} at the interface. Interface will be characterized by IGZO and SiO_2. In the aspect of SiO_2, Vo near E_V of SiO_x was related to the V_{th} shift under the UV light with the negative gate bias stress. However, Vo in the middle of the SiO_2 energy gap could be the main reason under UV light without any prolonged bias. In IGZO film, I_{off} could be suppressed when Vo density was decreased.

The instability of IGZO TFTs under the combination of negative gate bias stress and light illumination was also studied. In IGZO TFTs, photo-induced hole trapping and Vo^{2+} accumulation at the gate insulator layer are responsible for the negative shift of V_{th}. It was found that Vo^{2+} at the interface causing hysteresis was not affected by the prolonged negative gate bias stress. Form the experimental results, a relaxation time of Vo^{2+} generation in the IGZO bulk was extracted ($\sim 10^2$ s). When IGZO TFTs featured a passivation layer to prevent the ambient effect, the relaxation time for Vo^{2+} generation in IGZO bulk was larger than conventional carriers. It was more likely the relaxation time for the defect state creation.

With various intensities of 400 nm light, the relationship between hole concentration and the extent of V_{th} shift was investigated. The results suggested that the trapping probability of a single hole was not altered by light intensity. The accelerated V_{th} shift was because of the increase of hole concentration at the channel. In IGZO TFTs, the hole concentration at the channel was the determinant factor. Based on this, the ΔV_{th_sat}, which was close to the empirical result, could be estimated.

Finally, the characteristics of IGZO TFT on plastic substrate were investigated. When IGZO TFT was fabricated on thin PI substrate, the device was quite stable even under 2 mm bending radius. However, the mechanical bending increased the V_{th} shift under electrical gate bias stress due to E_V shift. The mechanical strain in TFTs can be minimized when the additionally deposited layers such as an encapsulation layer and OLED having suitable thickness and Young's modulus. Under the negative gate bias and illumination stress, it was found that the passivation layer and buffer layer prevent the ambient effect on IGZO TFTs successfully.

Appendix A Design and Fabrication of Simultaneous Emission AMOLED Pixel Circuit

A.1 Introduction

Recently, active organic light emitting diode display (AMOLED) employing Low temperature polycrystalline silicon (LTPS) thin film transistor (TFT) have attracted a considerable attention due to high brightness, wide viewing angle and low power consumption [A.1, A.2]. LTPS TFTs employing excimer laser annealing (ELA) are widely used in AMOLED displays [A.3-A.5]. However, the excimer laser annealed poly-Si TFTs suffer from a threshold voltage (V_{th}) variation in the pixel which causes non-uniform OLED current. Various compensation circuits have been reported [A.6-A.8]. Usually, 5–6 TFTs and 1–2 capacitors are required for V_{th} compensation.

However, as displays increase in resolution, the pixel size decreases due to the increase of pixel number on the display. For the high resolution AMOLED display, the compensation pixel circuit should be simplified.

The simultaneous emission diving has advantages for the stereoscopic 3D display [A.9]. Most of AMOLED display employs the progressive emission driving scheme, which increases the pixel area due to the compensation of V_{th} variation and decreases the emission time in the stereoscopic 3D display. In the progressive emission driving, the reset, V_{th} storage, data scan and emission steps progress line-by-line as shown in Figure A.1. On the other hand, the simultaneous emission can simplify the pixel structure and increase the emission time in the 3D display. The panel is turned off at the reset, V_{th} storage and data scan steps and it is turned on

simultaneously at the emission step as shown in Figure A.2.

For 2D display, the simultaneous emission driving method has shorter emission time than the progressive emission, because the progressive emission has almost 100 % emission ratio on one frame. However, in the aspect of the pixel circuit, the simultaneous emission is more suitable for high-resolution AMOLED display because the circuit can be simplified with the simultaneous emission driving. The detail driving scheme for 2D display is shown in Figure A.3 and Figure A.4.

In this chapter, a new p-type poly-Si pixel circuit for simultaneous emission method, which is suitable for high resolution AMOLED, is presented. The 1280 × 720 pixels 2D AMOLED panel was fabricated employing the simultaneous emission driving method for the first time.

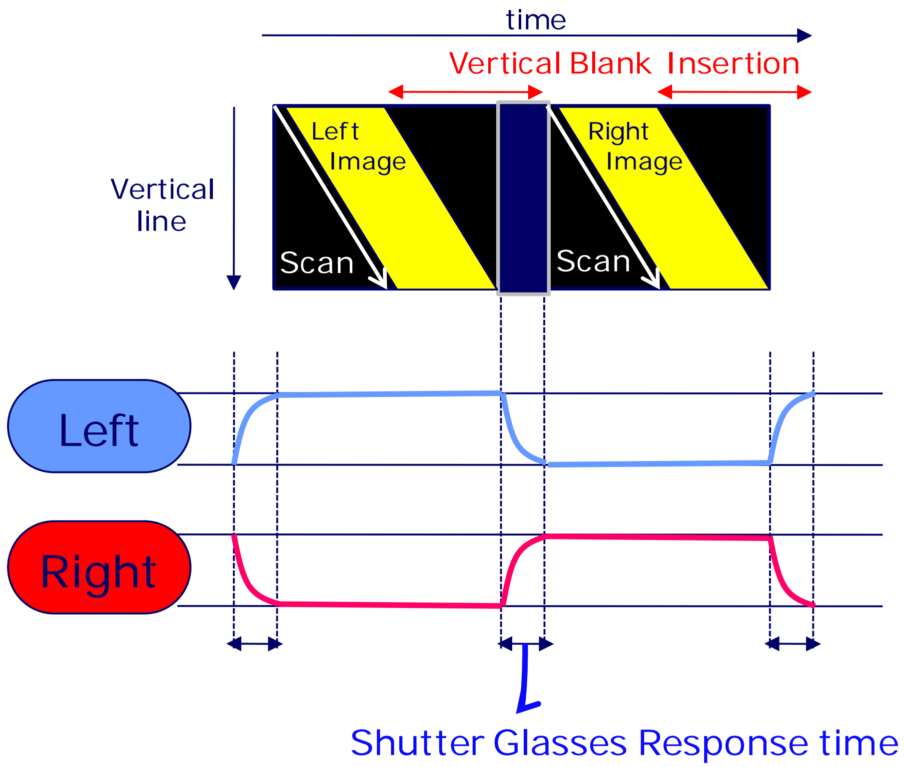


Figure A.1 The progressive emission driving scheme for 3D display

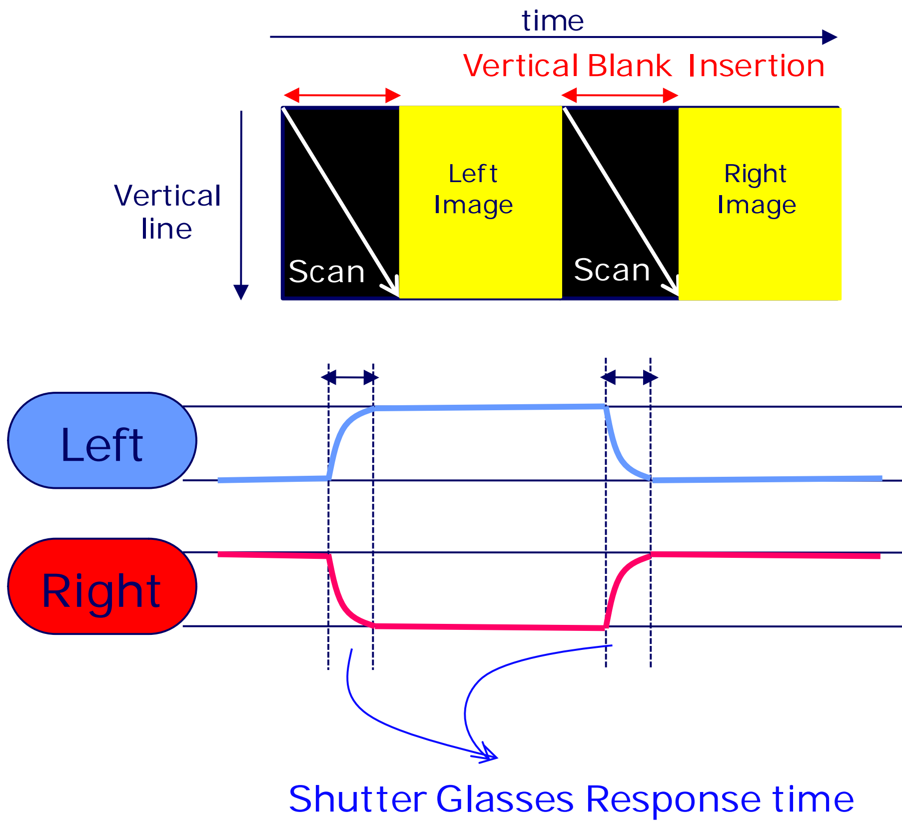


Figure A.2 The simultaneous emission driving scheme for 3D display

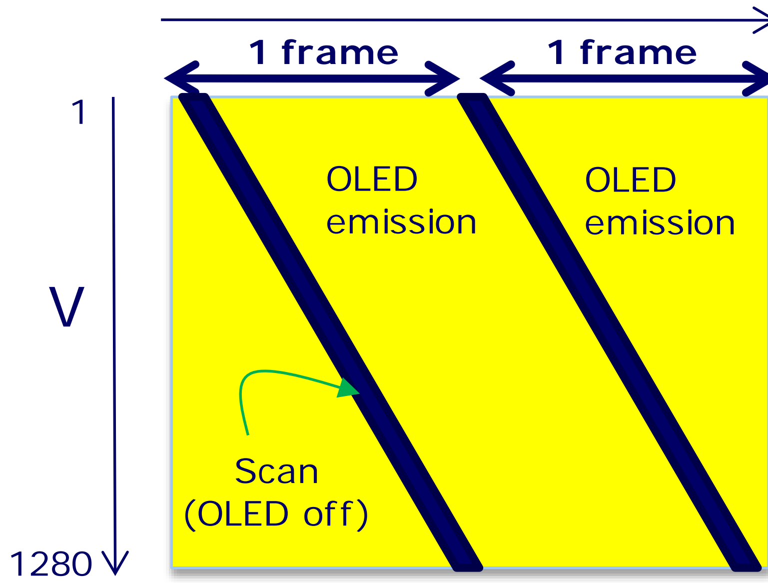


Figure A.3 The progressive emission driving scheme for 2D display

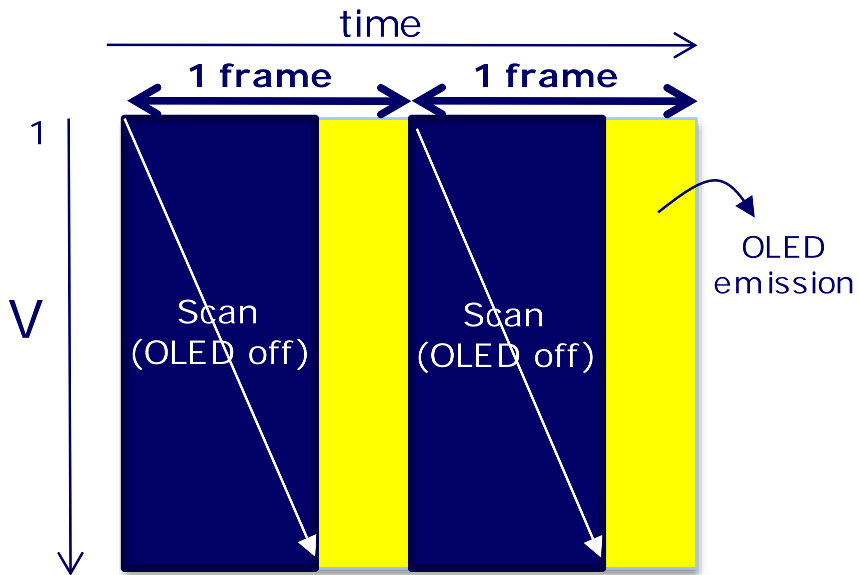


Figure A.4 The simultaneous emission driving scheme for 2D display

A.2 Conventional pixel circuit for progressive emission driving

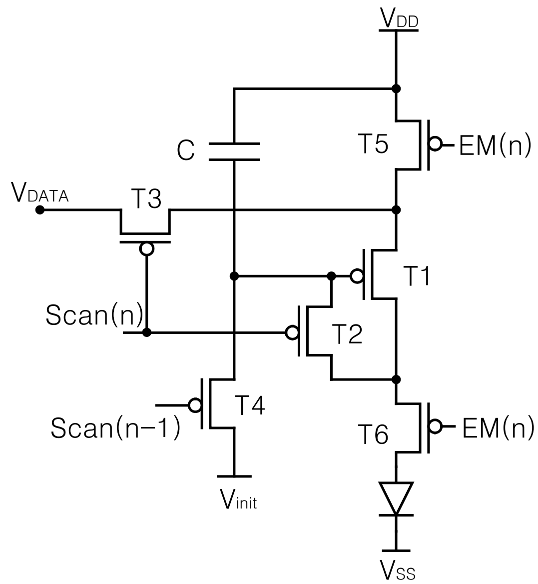
Figure A.5 shows the pixel schematic and the timing diagram of the reported 6-TFT and 1-capacitor pixel circuit for progressive emission [141]. When scan (n-1) is low, the gate voltage of the driving TFT (T1) is initialized as the initial voltage (V_{init}). When scan (n) is low, a data voltage (V_{DATA}) is memorized as V_{DATA}-|V_{th}| at the gate of T1. Because the drain current of T1 is the function of (|V_{GS}|-|V_{th}|), V_{th} term can be cancelled in the emission time as below.

$$I_{DS} = \frac{\beta}{2}(|V_{GS}| - |V_{th}|)^2$$

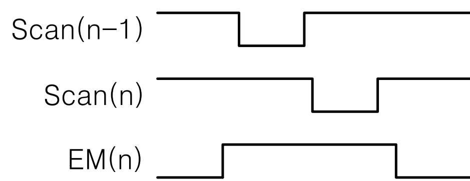
$$= \frac{\beta}{2}\{V_{DD} - (V_{DATA} - |V_{th}|) - |V_{th}|\}^2 \qquad (1)$$

$$= \frac{\beta}{2}(V_{DD} - V_{DATA})^2$$

These steps progress line-by-line as shown in Figure A.4, so that the emission time is almost 100% during one frame. The pixel consists of 6-TFT, 1-capacitor, 2-control signal and 4-power line.



(a)



(b)

Figure A.5 (a) Conventional pixel schematic and (b) the timing diagram for the progressive emission driving.

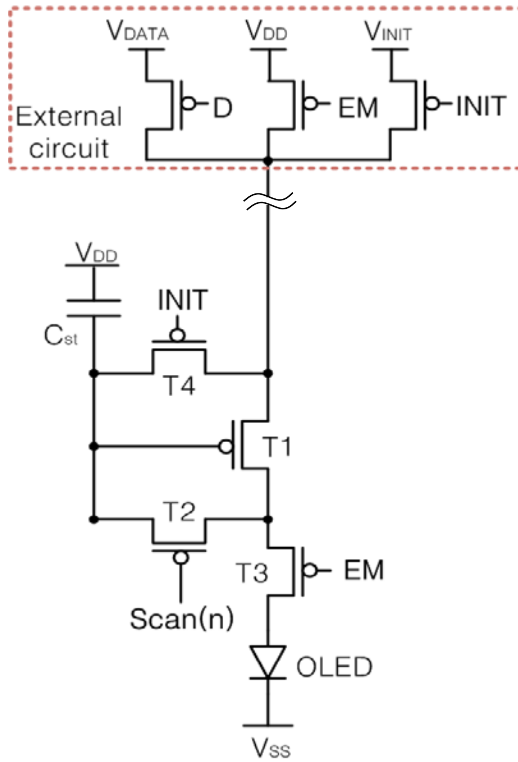
A.3 Proposed pixel circuit for simultaneous emission driving

Proposed V_{th} compensation pixel circuit for the simultaneous emission driving is shown in Figure A.6 (a). The pixel consists of 4-TFT and 1-capacitor. At first, T4 is turned on and the gate node of the driving TFT is initialized with connecting pixel to V_{INIT} at the external circuit. Then, the pixels are connected to data voltage line during the line by line scanning. During the scanning period, the panel is turned off. Finally, the light is emitted simultaneously with connecting the pixels to V_{DD}.

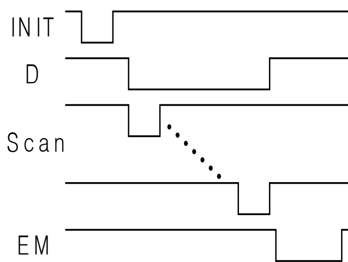
In the conventional progressive emission driving, OLEDs emit the light after line by line scanning. When one line is in the scanning time, the others are in the emission period. It means that each pixel requires the data voltage line and the initialization line in addition to V_{DD} line because it has to memorize the data voltage regardless of the other lines. At the same time, the switching devices for connecting the pixel to data line, initialization line and V_{DD} line are required. However, in the simultaneous emission driving, data line, initialization line and V_{DD} line can be shared because all OLEDs of the panel are turned off. In the simultaneous emission driving, the compensation pixel circuit can be simplified compared to the conventional progressive emission driving.

Instead of simplification of pixel structure, the external circuit, which is for controlling the connection of data voltage line, initialization line and V_{DD} line to pixel, is added in the simultaneous emission driving. The detail

of the external circuit will be explained at A.4 Panel design.



(a)



(b)

Figure A.6 (a) Conventional pixel schematic and (b) the timing diagram for the progressive emission driving.

A.4 Simulation results & discussion

The performance of the proposed pixel circuit was verified using smart SPICE circuit simulation. OLED current variation according to V_{th} variation (ΔV_{th}) of LTPS TFTs was examined. The results of the proposed pixel circuit were compared with that of the conventional progressive emission driving 6T1C because the pixel operation of 6T1C is very similar to the proposed pixel circuit. In 6T1C pixel circuit, the gate node of the driving TFT is initialized with the scan[n-1] signal. When scan[n] signal turns on the switch for the diode-connection of the driving TFT, V_{th} is detected and data voltage is memorized at the same time. Then, light is emitted during 1 frame.

Figure A.7 (a) shows the simulation results of OLED current variation according to ΔV_{th}, ±0.5 V. OLED current of Figure A.7 is the average current of 1 frame. The proposed simultaneous emission driving pixel circuit shows the better V_{th} compensation performance than the conventional progressive emission 6T1C.

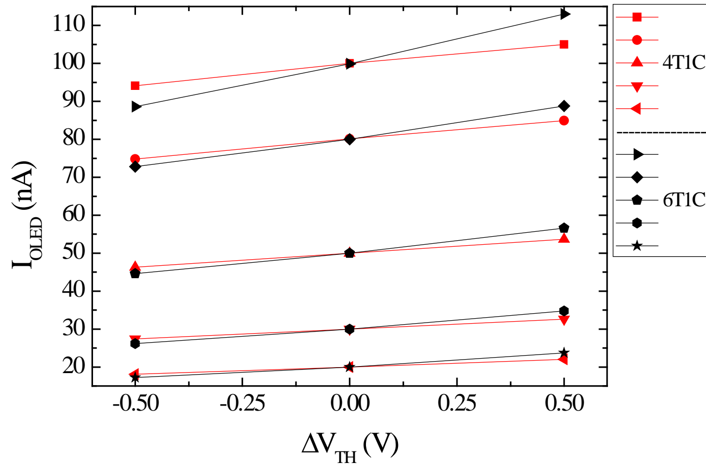
In the proposed pixel circuit, the initializing time and scanning time was 21 μs and 8 μs, so that the emission time was 38 % of 1 frame. The scanning time of 6T1C was also 8 μs. The storage capacitance was 0.5 pF for both pixel circuits. Even though the compensation method, the scanning time and capacitor size was same, it is found the proposed pixel circuit shows the better compensation performance than the conventional 6T1C.

Even though the compensation circuit reduces OLED current variation caused by V_{th} variation, OLED current variation still exists. This is because of the leakage current though the switching TFTs. In the conventional 6T1C, the gate voltage of the driving TFT is changed during the emission time, almost 100 % of 1 frame, while it is changed during 38 % of 1 frame in the proposed simultaneous emission driving pixel circuit. It is assumed that OLED current variation is reduced in the proposed pixel circuit due to the shorter emission time than the conventional 6T1C. To verify the effect of the emission time on OLED current variation, the emission time of the conventional 6T1C to 38 % of 1 frame was decreased. Figure 2(c) shows that OLED current variation is decreased when the emission time of 6T1C is decreased. However, OLED current variation of the proposed pixel circuit is much smaller than 6T1C.

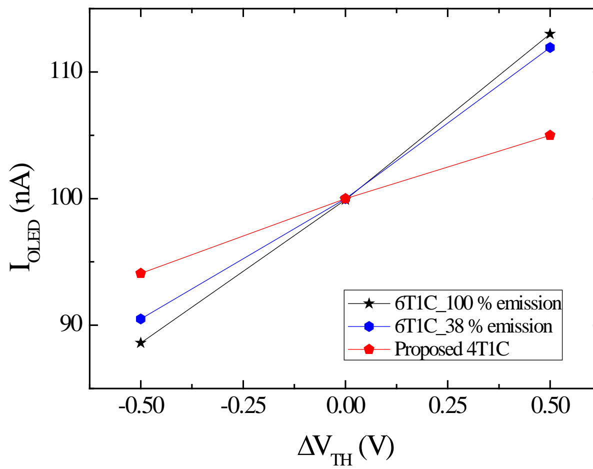
Figure A.8 shows the pixel structure and the leakage current path of the conventional 6T1C and the proposed pixel circuit. In the conventional 6T1C, the gate node always has higher voltage than the opposite side of switching TFTs, Vinit and the drain of driving TFT. Because the amount and direction of leakage current is significantly related to V_{DS} gate node of the driving TFTs always lose the memorized voltage. On the other hand, the gate node of the driving TFT is connected to source and drain of the driving TFT. The leakage current through the switch for the diode-connection is almost same at both proposed pixel circuit and conventional 6T1C. However, the source node of the driving TFT is the data voltage for next scan line. In this case, the leakage current flows from

the source to the gate of the driving TFT through T2. Therefore, the data voltage loss due to the leakage current is suppressed in the proposed pixel circuit.

From the simulation results, it is supported that V_{th} compensation circuit will show good performance in the simultaneous emission driving due to the shorter emission time than the conventional progressive emission driving. Furthermore, the proposed pixel shows improved compensation performance, compared to the conventional pixel circuit, because the proposed pixel structure can suppress the effect of the leakage current on V_{th} compensation.

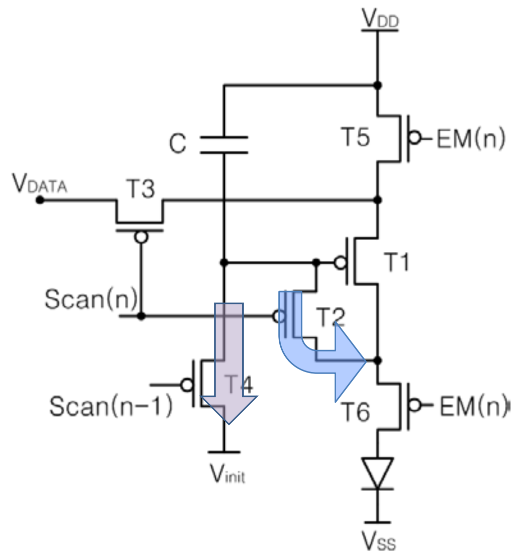


(a)

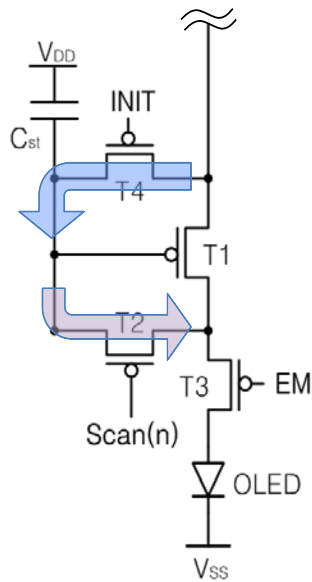


(b)

Figure A.7 OLED current variation according to V_{th} variation from -0.5 V to 0.5 V: (a) at the proposed pixel and the conventional 6T1C and (b) when OLED emission time is decreased.



(a)



(b)

Figure A.8 Leakage current path at the gate node of the driving TFT at: (a) the conventional 6T1C and (b) the proposed pixel circuit.

A.5 Panel design

Employing the simultaneous emission driving, 4.0-inch 1280x720 pixels monocolor AMOLED panel was fabricated. Figure A.9, Figure A.10 and Table A.1 show the pixel layout, display image and the specification of 4.0-inch AMOLED panel. A good image quality was realized with simultaneous emission driving employing the proposed pixel circuit.

From the result, it is confirmed that the proposed pixel circuit successfully compensates V_{th} variation of PMOS LTPS TFTs. In this case, V_{th} was -2 ± 0.2 V. The sizes of the driving TFT and switching TFTs are 20 μm/5 μm and 4 μm /4 μm. To reduce the number of current driver ICs, 1:2 deMUX was used. However, when 1:2 deMUX was used, data writing time is required between line by line scanning, causing out of time for the emission. Thus, two data lines were used. One was for odd scan lines and the other was for even scan line. The external circuit for the proposed pixel circuit is shown in Figure A.11. The circuit is for half current driver ICs and two data lines.

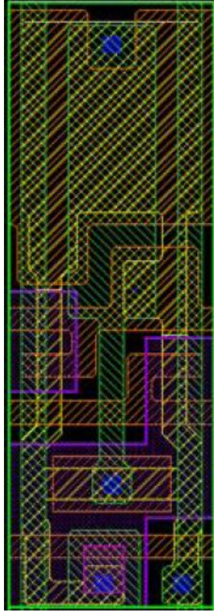
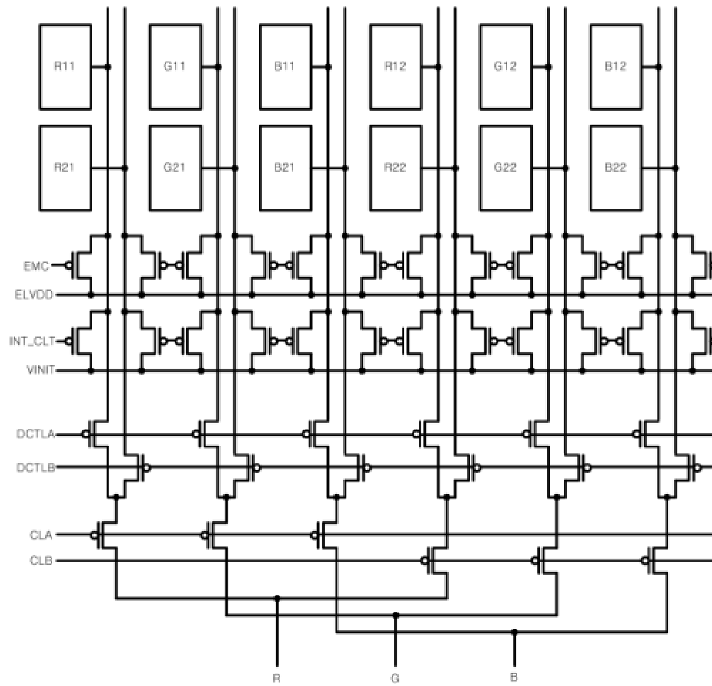


Figure A.9 Pixel layout.

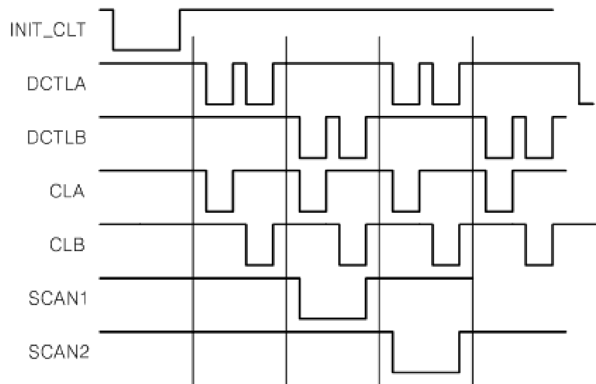
Figure A.10 Panel demonstration.

Table A.1 Panel specification

PARAMETER	**SPECIFICATION**
DRIVING SCHEME	Simultaneous emission
DISPLAY SIZE	4.0 inch
NUMBER OF PIXEL	1280×720
PIXEL PITCH	26×78 μm
TFT TYPE	PMOS only
PIXEL STRUCTURE	4 TFTs and 1 capacitor



(a)



(b)

Figure A.11 (a) External circuit design for the proposed simultaneous emission driving pixel circuit and (b) the timing diagram.

Bibliography

[1] W. Den Boer, *Active matrix liquid crystal displays: fundamentals and applications*: Newnes, 2011.

[2] T. Scheffer and B. Clifton, "Active addressing method for high-contrast video-rate STN displays," in *SID*, 1992, pp. 228-231.

[3] T. Sunata, T. Yukawa, K. Miyake, Y. Matsushita, Y. Murakami, Y. Ugai*, et al.*, "A large-area high-resolution active-matrix color LCD addressed by a-Si TFT's," *IEEE Transactions on Electron Devices,* vol. 33, pp. 1212-1217, Aug. 1986.

[4] K. Ichikawa, S. Suzuki, H. Matino, T. Aoki, T. Higuchi, and Y. Oana, "14.3-in.-Diagonal 16-Color TFT-LCD Panel Using a-Si: H TFTs," in *Digest of Technical Papers, 1989 SID International Symposium*, 1989, p. 226.

[5] P. Le Comber, W. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electronics Letters,* vol. 15, pp. 179-181, Mar. 1979.

[6] M. Powell, C. Van Berkel, I. French, and D. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," *Applied physics letters,* vol. 51, pp. 1242-1244, Oct. 1987.

[7] D. Staebler and C. Wronski, "Reversible conductivity changes in discharge-produced amorphous Si," *Applied physics letters,* vol. 31, pp. 292-294, Aug. 1977.

[8] J. Kanicki, *Amorphous and Microcrystalline Semiconductor Devices: Materials and Device Physics*: Artech House, Incorporated, 1992.

[9] M. Powell, "Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors," *Applied physics letters,* vol. 43, pp. 597-599,

Sept. 1983.
[10] M. J. Powell, I. D. French, and J. R. Hughes, "Evidence for the defect pool concept for Si dangling bond states in a-Si:H from experiments with thin film transistors," *Journal of Non-Crystalline Solids,* vol. 114, Part 2, pp. 642-644, Dec. 1989.
[11] A. Merticaru and A. Mouthaan, "Dynamics of metastable defects in a-Si:H/SiN TFTs," *Thin Solid Films,* vol. 383, pp. 122-124, Feb. 2001.
[12] W. Jackson, J. Marshall, and M. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," *Physical Review B,* vol. 39, pp. 1164-1179, Jan. 1989.
[13] R. Schropp and J. Verwey, "Instability mechanism in hydrogenated amorphous silicon thin-film transistors," *Applied physics letters,* vol. 50, pp. 185-187, Jan. 1987.
[14] W. G. Hawkins, "Polycrystalline-silicon device technology for large-area electronics," *IEEE Transactions on Electron Devices,* vol. 33, pp. 477-481, Apr. 1986.
[15] W. Czubatyj, D. Beglau, R. Himmler, G. Wicker, D. Jablonski, and S. Guha, "Low-temperature polycrystalline-silicon TFT on 7059 glass," *IEEE Electron Device Letters,* vol. 10, pp. 349-351, Aug. 1989.
[16] M. Mohri, H. Kakinuma, and T. Tsuruoka, "Fabrication of TFTs using plasma CVD poly-Si at very low temperature," in *International Electron Devices Meeting 1992, IEDM'92. Technical Digest.*, San Francisco, CA, USA, 1992, pp. 673-676.
[17] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," *IEEE Transactions on Electron Devices,* vol. 36, pp. 2868-2872, Dec. 1989.
[18] D. P. Gosain, J. Westwater, and S. Usui, "High performance bottom gate TFTs by excimer laser crystallization and post hydrogenation," *Japanese Journal of Applied Physics,* vol. 34, part 1, pp. 937-941, Feb. 1995.
[19] T. Sameshima, S. Usui, and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," *IEEE Electron Device Letters,* vol. 7, pp. 276-278, May 1986.
[20] K. Shimizu, O. Sugiura, and M. Matsumura, "High-mobility poly-Si thin-film transistors fabricated by a novel excimer laser crystallization method," *IEEE Transactions on Electron Devices,* vol. 40, pp. 112-117, Jan. 1993.
[21] C.-H. Kim, I.-H. Song, W.-J. Nam, and M.-K. Han, "A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure," *IEEE Electron Device Letters,* vol. 23, pp. 315-317, Jun. 2002.
[22] H. Kim and J. S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors," *Applied physics letters,* vol. 68, pp. 1513-1515, Mar. 1996.
[23] C.-H. Oh, M. Ozawa, and M. Matsumura, "A novel phase-modulated excimer-laser crystallization method of silicon thin films," *Japanese*

Journal of Applied Physics, vol. 37, pp. L492-L495, May 1998.

[24] T. Shimoda, M. Kimura, S. Seki, H. Kobayashi, S. Kanbe, S. Miyashita*, et al.*, "Technology for active matrix light emitting polymer displays," in *International Electron Devices Meeting 1999, IEDM'99. Technical Digest.*, Washington, DC, USA, 1999, pp. 107-110.

[25] R. Dawson, Z. Shen, D. Furst, S. Connor, J. Hsu, M. Kane*, et al.*, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," in *International Electron Devices Meeting 1998, IEDM'98. Technical Digest.*, San Francisco, CA, USA, 1998, pp. 875-878.

[26] G. Rajeswaran, M. Itoh, M. Boroson, S. Barry, T. Hatwar, K. Kahen*, et al.*, "40.1: Invited Paper: Active Matrix Low Temperature Poly-Si TFT/OLED Full Color Displays: Development Status," in *SID Symposium Digest of Technical Papers*, 2000, pp. 974-977.

[27] T. Sasaoka, M. Sekiya, A. Yumoto, J. Yamada, T. Hirano, Y. Iwase*, et al.*, "24.4 L: Late-News Paper: A 13.0-inch AM-OLED Display with Top Emitting Structure and Adaptive Current Mode Programmed Pixel Circuit (TAC)," in *SID Symposium Digest of Technical Papers*, 2001, pp. 384-387.

[28] T. Shirasaki, T. Ozaki, T. Toyama, M. Takei, M. Kumagai, K. Sato*, et al.*, "Solution for Large-Area Full-Color OLED Television-Light Emitting Polymer and a-Si TFT Technologies," in *Proceeding ot International Display Workshops*, 2004, pp. 275-278.

[29] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi*, et al.*, "High-mobility thin-film transistor with amorphous InGaZnO channel fabricated by room temperature rf-magnetron sputtering," *Applied physics letters,* vol. 89, pp. 112123-1 - 112123-3, Sept. 2006.

[30] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park*, et al.*, "Bottom-gate gallium indium zinc oxide thin-film transistor array for high-resolution AMOLED display," *IEEE Electron Device Letters,* vol. 29, pp. 1309-1311, Dec. 2008.

[31] J. F. Wager, "15.1: Invited Paper: Amorphous Oxide Semiconductor Thin-Film Transistors: Performance & Manufacturability for Display Applications," *SID Symposium Digest of Technical Papers,* vol. 40, pp. 181-183, Jun. 2009.

[32] J. K. Jeong, J. H. Jeong, H. W. Yang, J.-S. Park, Y.-G. Mo, and H. D. Kim, "High performance thin film transistors with cosputtered amorphous indium gallium zinc oxide channel," *Applied physics letters,* vol. 91, pp. 113505-1 - 113505-3, Sept. 2007.

[33] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Japanese Journal of Applied Physics,* vol. 45, pp. 4303-4308, May 2006.

[34] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J.-S. Park*, et al.*, "High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper," *Applied physics letters,* vol. 90, pp. 212114-1 - 212114-3, May

2007.

[35] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor," *Science,* vol. 300, pp. 1269-1272, May 23 2003.

[36] E. Fortunato, P. Barquinha, A. Pimentel, A. M. F. Gonçalves, A. J. S. Marques, L. Pereira*, et al.*, "Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature," *Advanced Materials,* vol. 17, pp. 590-594, Mar. 2005.

[37] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, pp. 488-492, 25 Nov. 2004.

[38] B. Ryu, H.-K. Noh, E.-A. Choi, and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors," *Applied physics letters,* vol. 97, pp. 022108-1 - 022108-3, Jul. 2010.

[39] J. S. Park, T. S. Kim, K. S. Son, J. S. Jung, K. H. Lee, J. Y. Kwon*, et al.*, "Influence of illumination on the negative-bias stability of transparent Hafnium–Indium–Zinc Oxide thin-film transistors," *IEEE Electron Device Letters,* vol. 31, pp. 440-442, May 2010.

[40] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang, and S.-H. K. Park, "Photon-accelerated negative bias instability involving subgap states creation in amorphous In–Ga–Zn–O thin film transistor," *Applied physics letters,* vol. 97, pp. 183502-1 - 183502-3, Nov. 2010.

[41] E. Fortunato, P. Barquinha, A. C. Pimentel, A. M. Gonçalves, A. J. Marques, R. F. Martins*, et al.*, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature," *Applied physics letters,* vol. 85, pp. 2541-2543, Sept. 2004.

[42] A. Janotti and C. G. Van de Walle, "Oxygen vacancies in ZnO," *Applied physics letters,* vol. 87, pp. 122102-1 -122102-3, Sep. 2005.

[43] T. Aoi, N. Oka, Y. Sato, R. Hayashi, H. Kumomi, and Y. Shigesato, "DC sputter deposition of amorphous indium–gallium–zinc–oxide (a-IGZO) films with H2O introduction," *Thin Solid Films,* vol. 518, pp. 3004-3007, Mar. 2010.

[44] S.-J. Kim, S.-Y. Lee, Y.-W. Lee, W.-G. Lee, K.-S. Yoon, J.-Y. Kwon*, et al.*, "Effect of Channel Layer Thickness on Characteristics and Stability of Amorphous Hafnium–Indium–Zinc Oxide Thin Film Transistors," *Japanese Journal of Applied Physics,* vol. 50, p. 024104, Feb. 2011.

[45] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park*, et al.*, "Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules," *Applied Physics Letters,* vol. 90, pp. 192101-1 - 192101-3, May 2007.

[46] K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim*, et al.*, "Effect of high-pressure oxygen annealing on negative bias illumination stress-induced instability of InGaZnO thin film transistors," *Applied physics letters,* vol. 98, pp. 103509-1 - 103509-3, Mar. 2011.

[47] K. Nomura, T. Kamiya, E. Ikenaga, H. Yanagi, K. Kobayashi, and H. Hosono,

"Depth analysis of subgap electronic states in amorphous oxide semiconductor, a-In-Ga-Zn-O, studied by hard x-ray photoelectron spectroscopy," *Journal of applied physics,* vol. 109, pp. 073726-1 - 073726-8, Apr. 2011.

[48] J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H. K. Park, W.-S. Cheong, M. Ryu*, et al.*, "Light effects on the bias stability of transparent ZnO thin film transistors," *Etri Journal,* vol. 31, pp. 62-64, Feb. 2009.

[49] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi*, et al.*, "The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors," *Applied physics letters,* vol. 95, pp. 232106-1 - 232106-3, Dec. 2009.

[50] M. Fujii, H. Yano, T. Hatayama, Y. Uraoka, T. Fuyuki, J. S. Jung*, et al.*, "Thermal Analysis of Degradation in Ga2O3–In2O3–ZnO Thin-Film Transistors," *Japanese Journal of Applied Physics,* vol. 47, pp. 6236-6240, Aug. 2008.

[51] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Applied Physics Letters,* vol. 93, pp. 093504-1 - 093504-3, Sept. 2008.

[52] A. Suresh and J. F. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors," *Applied Physics Letters,* vol. 92, pp. 033502-1 - 033502-3, Jan. 2008.

[53] J. Lee, J.-S. Park, Y. S. Pyo, D. B. Lee, E. H. Kim, D. Stryakhilev*, et al.*, "The influence of the gate dielectrics on threshold voltage instability in amorphous indium-gallium-zinc oxide thin film transistors," *Applied Physics Letters,* vol. 95, pp. 123502-1 - 123502-3, Sept. 2009.

[54] J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang, and H.-I. Kwon, "Comparative study of electrical instabilities in top-gate InGaZnO thin film transistors with Al2O3 and Al2O3/SiNx gate dielectrics," *Applied Physics Letters,* vol. 94, pp. 222112-1 - 222112-3, Jun. 2009.

[55] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato*, et al.*, "Gate-bias stress in amorphous oxide semiconductors thin-film transistors," *Applied Physics Letters,* vol. 95, pp. 063502-1 - 063502-3, Aug. 2009.

[56] Y.-K. Moon, S. Lee, W.-S. Kim, B.-W. Kang, C.-O. Jeong, D.-H. Lee*, et al.*, "Improvement in the bias stability of amorphous indium gallium zinc oxide thin-film transistors using an O2 plasma-treated insulator," *Applied Physics Letters,* vol. 95, pp. 013507-1 - 013507-3, Jul. 2009.

[57] C.-T. Tsai, T.-C. Chang, S.-C. Chen, I. Lo, S.-W. Tsao, M.-C. Hung*, et al.*, "Influence of positive bias stress on N2O plasma improved InGaZnO thin film transistor," *Applied Physics Letters,* vol. 96, pp. 242105-1 - 242105-3, Jun. 2010.

[58] M. D. H. Chowdhury, P. Migliorato, and J. Jang, "Time-temperature dependence of positive gate bias stress and recovery in amorphous indium-gallium-zinc-oxide thin-film-transistors," *Applied Physics Letters,* vol. 98, p. 153511, 2011.

[59] C. Geng-Wei, C. Ting-Chang, J. Jhe-Ciou, T. Tsung-Ming, S. Yong-En, C. Kuan-Chang, *et al.*, "Abnormal Subthreshold Leakage Current at High Temperature in InGaZnO Thin-Film Transistors," *IEEE Electron Device Letters,* vol. 33, pp. 540-542, Apr. 2012.

[60] T.-C. Chen, T.-C. Chang, C.-T. Tsai, T.-Y. Hsieh, S.-C. Chen, C.-S. Lin, *et al.*, "Behaviors of InGaZnO thin film transistor under illuminated positive gate-bias stress," *Applied Physics Letters,* vol. 97, pp. 112104-1 - 112104-3, Sept. 2010.

[61] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, *et al.*, "Instability in threshold voltage and subthreshold behavior in Hf-In-Zn-O thin film transistors induced by bias-and light-stress," *Applied Physics Letters,* vol. 97, pp. 113504-1 - 113504-3, Sept. 2010.

[62] D. W. Kwon, J. H. Kim, J. S. Chang, S. W. Kim, M.-C. Sun, G. Kim, *et al.*, "Charge injection from gate electrode by simultaneous stress of optical and electrical biases in HfInZnO amorphous oxide thin film transistor," *Applied Physics Letters,* vol. 97, pp. 193504-1 - 193504-3, Nov. 2010.

[63] J.-Y. Kwon, J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, *et al.*, "The impact of gate dielectric materials on the light-induced bias instability in Hf–In–Zn–O thin film transistor," *Applied physics letters,* vol. 97, pp. 183503-1 - 183503-3, Nov. 2010.

[64] J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, *et al.*, "The influence of SiO_x and SiN_x passivation on the negative bias stability of Hf–In–Zn–O thin film transistors under illumination," *Applied physics letters,* vol. 96, pp. 262109-1 - 262109-3, Jun. 2010.

[65] K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, Y. G. Mo, *et al.*, "Comprehensive studies of the degradation mechanism in amorphous InGaZnO transistors by the negative bias illumination stress," *Microelectronic Engineering,* vol. 88, pp. 1412-1416, Jul. 2011.

[66] B. Kim, E. Chong, D. Hyung Kim, Y. Woo Jeon, D. Hwan Kim, and S. Yeol Lee, "Origin of threshold voltage shift by interfacial trap density in amorphous InGaZnO thin film transistor under temperature induced stress," *Applied physics letters,* vol. 99, pp. 062108-1 - 062108-3, Aug. 2011.

[67] J. H. Kim, U. K. Kim, Y. J. Chung, J. S. Jung, S. H. Ra, H. S. Jung, *et al.*, "The effects of device geometry on the negative bias temperature instability of Hf-In-Zn-O thin film transistors under light illumination," *Applied physics letters,* vol. 98, pp. 023507-1 - 023507-3, Jan. 2011.

[68] S. Kim, S. Kim, C. Kim, J. Park, I. Song, S. Jeon, *et al.*, "The influence of visible light on the gate bias instability of In–Ga–Zn–O thin film transistors," *Solid-State Electronics,* vol. 62, pp. 77-81, Aug. 2011.

[69] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang, and S.-H. K. Park, "Transition of dominant instability mechanism depending on negative gate bias under illumination in amorphous In-Ga-Zn-O thin film transistor," *Applied physics letters,* vol. 98, pp. 033504-1 - 033504-3, Jan. 2011.

[70] S. Yang, K. Hwan Ji, U. Ki Kim, C. Seong Hwang, S.-H. Ko Park, C.-S. Hwang,

et al., "Suppression in the negative bias illumination instability of Zn-Sn-O transistor using oxygen plasma treatment," *Applied Physics Letters,* vol. 99, pp. 102103-1 - 102103-3, Sept. 2011.

[71] S. Y. Lee, S. J. Kim, Y. W. Lee, W. G. Lee, K. S. Yoon, J. Y. Kwon*, et al.*, "The Effect of the Photo-Induced Carriers on the Reliability of Oxide TFTs Under Various Intensities of Light," *IEEE Electron Device Letters,* vol. 33, pp. 218-220, Feb. 2012.

[72] T. Y. Luo, M. Laughery, G. A. Brown, H. N. Al-Shareef, V. H. C. Watt, A. Karamcheti*, et al.*, "Effect of H2 content on reliability of ultrathin in-situ steam generated (ISSG) SiO2," *IEEE Electron Device Letters,* vol. 21, pp. 430-432, Sept. 2000.

[73] S.-H. Kuk, S.-Y. Lee, S.-J. Kim, B. Kim, S.-J. Park, J.-Y. Kwon*, et al.*, "Light-Induced Hysteresis of In-Ga-Zn-O Thin-Film Transistors With Various Temperatures," *IEEE Electron Device Letters,* vol. 33, pp. 1279-1281, Sept. 2012.

[74] J. H. Kim, U. K. Kim, Y. J. Chung, and C. S. Hwang, "Correlation of the change in transfer characteristics with the interfacial trap densities of amorphous In–Ga–Zn–O thin film transistors under light illumination," *Applied physics letters,* vol. 98, pp. 232102-1 - 232102-3, Jun. 2011.

[75] T. C. Fung, C. S. Chuang, K. Nomura, H. P. D. Shieh, H. Hosono, and J. Kanicki, "Photofield-effect in amorphous In-Ga-Zn-O (a-IGZO) thin-film transistors," *Journal of Information Display,* vol. 9, pp. 21-29, 2008.

[76] M. Kimura, Y. Kamada, S. Fujita, T. Hiramatsu, T. Matsuda, M. Furuta*, et al.*, "Mechanism analysis of photoleakage current in ZnO thin-film transistors using device simulation," *Applied physics letters,* vol. 97, pp. 163503-1 - 163503-3, Oct. 2010.

[77] J. Jeong and Y. Hong, "Debye Length and Active Layer Thickness-Dependent Performance Variations of Amorphous Oxide-Based TFTs," *IEEE Transactions on Electron Devices,* vol. 59, pp. 710-714, Mar 2012.

[78] S. Yang, D.-H. Cho, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, J. Jang*, et al.*, "Improvement in the photon-induced bias stability of Al–Sn–Zn–In–O thin film transistors by adopting AlO_x passivation layer," *Applied physics letters,* vol. 96, pp. 213511-1 - 213511-3, May 2010.

[79] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, and L. M. Irving, "Stable ZnO thin film transistors by fast open air atomic layer deposition," *Applied Physics Letters,* vol. 92, pp. 192101-1 - 192101-3, May 2008.

[80] P.-T. Liu, Y.-T. Chou, and L.-F. Teng, "Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress," *Applied Physics Letters,* vol. 95, pp. 233504-1 - 233504-3, Dec. 2009.

[81] S.-Y. Sung, J. H. Choi, U. B. Han, K. C. Lee, J.-H. Lee, J.-J. Kim*, et al.*, "Effects of ambient atmosphere on the transfer characteristics and gate-bias stress stability of amorphous indium-gallium-zinc oxide thin-film transistors," *Applied Physics Letters,* vol. 96, pp. 102107-1 - 102107-3, Mar. 2010.

[82] W.-F. Chung, T.-C. Chang, H.-W. Li, C.-W. Chen, Y.-C. Chen, S.-C. Chen*, et al.*, "Influence of H_2O Dipole on Subthreshold Swing of Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors," *Electrochemical and Solid-State Letters,* vol. 14, pp. H114-H116, Dec. 2011.

[83] C.-S. Fuh, S. M. Sze, P.-T. Liu, L.-F. Teng, and Y.-T. Chou, "Role of environmental and annealing conditions on the passivation-free in-Ga–Zn–O TFT," *Thin Solid Films,* vol. 520, pp. 1489-1494, Dec. 2011.

[84] S.-Y. Huang, T.-C. Chang, M.-C. Chen, S.-C. Chen, C.-T. Tsai, M.-C. Hung*, et al.*, "Effects of Ambient Atmosphere on Electrical Characteristics of Al2O3 Passivated InGaZnO Thin Film Transistors during Positive-Bias-Temperature-Stress Operation," *Electrochemical and Solid-State Letters,* vol. 14, pp. H177-H179, Feb. 2011.

[85] J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water," *Applied physics letters,* vol. 92, pp. 072104-1 - 072104-3, Feb. 2008.

[86] J. K. Jeong, H. Won Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Applied Physics Letters,* vol. 93, pp. 123508-1 - 123508-3, Sept. 2008.

[87] S.-H. Choi and M.-K. Han, "Effect of Deposition Temperature of SiOx Passivation Layer on the Electrical Performance of a-IGZO TFTs," *IEEE Electron Device Letters,* vol. 33, pp. 396-398, Mar. 2012.

[88] S.-H. Choi, J.-H. Jang, J.-J. Kim, and M.-K. Han, "Low-Temperature Organic (CYTOP) Passivation for Improvement of Electric Characteristics and Reliability in IGZO TFTs," *IEEE Electron Device Letters,* vol. 33, pp. 381-383, Mar. 2012.

[89] W. B. Jackson, R. Hoffman, B. Yeh, T. Emery, T. Koch, C. McConica*, et al.*, "Metastability in multicomponent oxide transistors," *physica status solidi (a),* vol. 207, pp. 695-699, Mar. 2010.

[90] J. S. Jung, K.-H. Lee, K. S. Son, J. S. Park, T. S. Kim, J. H. Seo*, et al.*, "The Effect of Passivation Layers on the Negative Bias Instability of Ga-In-Zn-O Thin Film Transistors under Illumination," *Electrochemical and Solid-State Letters,* vol. 13, pp. H376-H378, Aug. 2010.

[91] S.-I. Kim, S. W. Kim, C. J. Kim, and J.-S. Park, "The Impact of Passivation Layers on the Negative Bias Temperature Illumination Instability of Ha-In-Zn-O TFT," *Journal of The Electrochemical Society,* vol. 158, pp. H115-H118, 2011.

[92] L. Shou-En, Y. Ming-Jiue, L. Chang-Yu, H. Geng-Tai, C. Chun-Cheng, L. Chih-Ming*, et al.*, "Influence of Passivation Layers on Characteristics of a-InGaZnO Thin-Film Transistors," *IEEE Electron Device Letters,* vol. 32, pp. 161-163, Feb. 2011.

[93] K. Nomura, T. Kamiya, and H. Hosono, "Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects," *Applied physics letters,* vol. 99, pp. 053505-1 - 053505-3, Aug. 2011.

[94] J.-S. Park, J. K. Jeong, Y.-G. Mo, H. D. Kim, and C.-J. Kim, "Control of

threshold voltage in ZnO-based oxide thin film transistors," *Applied physics letters,* vol. 93, pp. 033513-1 - 033513-3, Jul. 2008.

[95] J. Jeong, J. K. Jeong, J. S. Park, Y. G. Mo, and Y. Hong, "Meyer–Neldel rule and extraction of density of states in amorphous indium–gallium–zinc-oxide thin-film transistor by considering surface band bending," *Jpn J Appl Phys,* vol. 49, pp. 03CB02-03CB02-6, Mar. 2010.

[96] D. H. Lee, K. Kawamura, K. Nomura, T. Kamiya, and H. Hosono, "Large Photoresponse in Amorphous In–Ga–Zn–O and Origin of Reversible and Slow Decay," *Electrochemical and Solid-State Letters,* vol. 13, pp. H324-H327, 2010.

[97] S. Yasuno, T. Kugimiya, S. Morita, A. Miki, F. Ojima, and S. Sumie, "Correlation of photoconductivity response of amorphous In–Ga–Zn–O films with transistor performance using microwave photoconductivity decay method," *Applied physics letters,* vol. 98, pp. 102107-1 - 102107-3, Mar. 2011.

[98] E. Arene and J. Baixeras, "Steady-state photoconductivity and recombination process in sputtered hydrogenated amorphous silicon," *Physical Review B,* vol. 30, pp. 2016-2025, Aug. 1984.

[99] Z.-Y. Lu, C. J. Nicklaw, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Structure, Properties, and Dynamics of Oxygen Vacancies in Amorphous SiO_{2}," *Physical Review Letters,* vol. 89, pp. 285505-1 - 285505-4, Dec. 2002.

[100] H. N. Lee, J. Kyung, M. C. Sung, D. Y. Kim, S. K. Kang, S. J. Kim*, et al.*, "Oxide TFT with multilayer gate insulator for backplane of AMOLED device," *Journal of the Society for Information Display,* vol. 16, pp. 265-272, Feb. 2008.

[101] J. K. Jeong, J. H. Jeong, H. W. Yang, T. K. Ahn, M. Kim, K. S. Kim*, et al.*, "12.1-in. WXGA AMOLED display driven by InGaZnO thin-film transistors," *Journal of the Society for Information Display,* vol. 17, pp. 95-100, Feb. 2009.

[102] J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, J.-Y. Kwon*, et al.*, "The impact of SiN_x gate insulators on amorphous indium-gallium-zinc oxide thin film transistors under bias-temperature-illumination stress," *Applied physics letters,* vol. 96, pp. 193506-1 - 193506-3, May 2010.

[103] J. K. Jeong, "The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays," *Semiconductor Science and Technology,* vol. 26, p. 034008, Mar. 2011.

[104] A. Stewart and D. Jones, "Optical absorption and defects in amorphous SiNx and SiOx," *Philosophical Magazine B,* vol. 57, pp. 431-440, Aug. 1988.

[105] K. H. Ji, J.-I. Kim, Y.-G. Mo, J. H. Jeong, S. Yang, C.-S. Hwang*, et al.*, "Comparative Study on Light-Induced Bias Stress Instability of IGZO Transistors With SiNx and Si02 Gate Dielectrics," *IEEE Electron Device Letters,* vol. 31, pp. 1404-1406, Dec. 2010.

[106] K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, Y.-G. Mo, J. H. Jeong*, et al.*, "The effect of density-of-state on the temperature and gate bias-induced instability of InGaZnO thin film transistors," *Journal of The Electrochemical Society,*

vol. 157, pp. H983-H986, 2010.

[107] Y. Wook Lee, S.-J. Kim, S.-Y. Lee, W.-G. Lee, K.-S. Yoon, J.-W. Park*, et al.*, "An Investigation of the Different Charge Trapping Mechanisms for SiNx and SiO2 Gate Insulator in a-IGZO TFTs," *Electrochemical and Solid-State Letters,* vol. 15, pp. H84-H87, Jan. 2012.

[108] F. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Applied physics letters,* vol. 62, pp. 1286-1288, Mar. 1993.

[109] H. Aozasa, I. Fujiwara, and Y. Kamigaki, "Analysis of carrier traps in silicon nitride film with discharge current transient spectroscopy, photoluminescence, and electron spin resonance," *Japanese Journal of Applied Physics,* vol. 46, pp. 5762-5766, Sept. 2007.

[110] A. V. Ferris-Prabhu, "Charge transfer by direct tunneling in thin-oxide memory transistors," *IEEE Transactions on Electron Devices,* vol. 24, pp. 524-530, May 1977.

[111] D. T. Krick, P. Lenahan, and J. Kanicki, "Nature of the dominant deep trap in amorphous silicon nitride," *Physical Review B,* vol. 38, pp. 8226-8229, Oct. 1988.

[112] N. Young, I. French, M. Trainor, D. Murley, D. McCulloch, and R. Wilks, "LTPS for AMLCD on glass and polymer substrates," in *Proceedings of the sixth international display workshop*, 1999, pp. 219-222.

[113] Y. Juhn-Suk, J. Sang-Hoon, K. Yong-Chul, B. Seung-Chan, K. Jong-Moo, C. Nack-Bong*, et al.*, "Highly Flexible AM-OLED Display With Integrated Gate Driver Using Amorphous Silicon TFT on Ultrathin Metal Foil," *Journal of Display Technology,* vol. 6, pp. 565-570, Nov. 2010.

[114] B. Hekmatshoar, A. Z. Kattamis, K. H. Cherenack, L. Ke, C. Jian-Zhang, S. Wagner*, et al.*, "Reliability of Active-Matrix Organic Light-Emitting-Diode Arrays With Amorphous Silicon Thin-Film Transistor Backplanes on Clear Plastic," *IEEE Electron Device Letters,* vol. 29, pp. 63-66, Jan. 2008.

[115] G. Fortunato, A. Pecora, L. Maiolo, M. Cuscuna, D. Simeone, A. Minotti*, et al.*, "Excimer Laser Annealing for Low-Temperature Polysilicon Thin Film Transistor Fabrication on Plastic Substrates," in *Advanced Thermal Processing of Semiconductors, 2007. RTP 2007. 15th International Conference on*, 2007, pp. 301-305.

[116] J.-S. Park, T.-W. Kim, D. Stryakhilev, J.-S. Lee, S.-G. An, Y.-S. Pyo*, et al.*, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," *Applied physics letters,* vol. 95, pp. 013503-1 - 013503-3, Jul. 2009.

[117] N. Munzenrieder, K. H. Cherenack, and G. Troster, "The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs," *IEEE Transactions on Electron Devices,* vol. 58, pp. 2041-2048, Jul. 2011.

[118] S. Yang, J. Y. Bak, S.-M. Yoon, M. K. Ryu, H. Oh, C.-S. Hwang*, et al.*, "Low-Temperature Processed Flexible In-Ga-Zn-O Thin-Film Transistors Exhibiting High Electrical Performance," *IEEE Electron Device Letters,* vol.

32, pp. 1692-1694, Dec. 2011.

[119] G. Fortunato, A. Pecora, and L. Maiolo, "Polysilicon thin-film transistors on polymer substrates," *Materials Science in Semiconductor Processing,* vol. 15, pp. 627-641, Dec. 2012.

[120] N. D. Young, M. J. Trainor, S. Y. Yoon, D. J. McCulloch, R. W. Wilks, A. Pearson*, et al.*, "Low Temperature Poly-Si on Flexible Polymer Substrates for Active Matrix Displays and Other Applications," in *Materials Research Society Symposium Proceedings*, 2003, pp. 17-28.

[121] S. D. Theiss and S. Wagner, "Amorphous silicon thin-film transistors on steel foil substrates," *IEEE Electron Device Letters,* vol. 17, pp. 578-580, Dec. 1996.

[122] S. H. Won, J. K. Chung, C. B. Lee, H. C. Nam, J. H. Hur, and J. Jang, "Effect of Mechanical and Electrical Stresses on the Performance of an a-Si:H TFT on Plastic Substrate," *Journal of The Electrochemical Society,* vol. 151, pp. G167-G170, 2004.

[123] K. Shih-Chin, Z. Hsiao-Wen, H. Jung-Jie, and K. Bo-Cheng, "Self-Heating Effect on Bias-Stressed Reliability for Low-Temperature a-Si:H TFT on Flexible Substrate," *IEEE Transactions on Electron Devices,* vol. 57, pp. 588-593, Mar. 2010.

[124] S. Maikap, C. Y. Yu, S. R. Jan, M. H. Lee, and C. W. Liu, "Mechanically strained strained-Si NMOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 40-42, Jan. 2004.

[125] A. Jong-Hyun, K. Hoon-Sik, L. Keon Jae, Z. Zhengtao, E. Menard, R. G. Nuzzo*, et al.*, "High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates," *IEEE Electron Device Letters,* vol. 27, pp. 460-462, Jun. 2006.

[126] Y. J. Yang, W. S. Ho, C. F. Huang, S. T. Chang, and C. W. Liu, "Electron mobility enhancement in strained-germanium n-channel metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 91, pp. 102103-1 - 102103-3, Sept. 2007.

[127] T. Afentakis, M. Hatalis, A. T. Voutsas, and J. Hartzell, "Design and fabrication of high-performance polycrystalline silicon thin-film transistor circuits on flexible steel foils," *IEEE Transactions on Electron Devices,* vol. 53, pp. 815-822, Apr. 2006.

[128] P.-C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis, "Effect of mechanical strain on mobility of polycrystalline silicon thin-film transistors fabricated on stainless steel foil," *Applied Physics Letters,* vol. 91, pp. 243507-1 - 243507-3, Dec. 2007.

[129] F. Templier, B. Aventurier, P. Demars, J.-L. Botrel, and P. Martin, "Fabrication of high performance low temperature poly-silicon backplanes on metal foil for flexible active-matrix organic light emission diode displays," *Thin Solid Films,* vol. 515, pp. 7428-7432, Jul. 2007.

[130] I.-H. Peng, P.-T. Liu, and T.-B. Wu, "Effect of bias stress on mechanically strained low temperature polycrystalline silicon thin film transistor on stainless steel substrate," *Applied Physics Letters,* vol. 95, pp. 041909-1 - 041909-3, Jul. 2009.

[131] S. Nai-Chao, W. Shui-Jinn, H. Chin-Chuan, C. Yu-Han, H. Hao-Yuan, C. Chen-Kuo, *et al.*, "Low-Voltage-Driven Flexible InGaZnO Thin-Film Transistor With Small Subthreshold Swing," *IEEE Electron Device Letters,* vol. 31, pp. 680-682, Jul. 2010.
[132] M. J. Gadre and T. L. Alford, "Highest transmittance and high-mobility amorphous indium gallium zinc oxide films on flexible substrate by room-temperature deposition and post-deposition anneals," *Applied Physics Letters,* vol. 99, pp. 051901-1 - 051901-3, Aug. 2011.
[133] D. H. Lee, K. Nomura, T. Kamiya, and H. Hosono, "Diffusion-Limited a-IGZO/Pt Schottky Junction Fabricated at 200 ◦C on a Flexible Substrate," *IEEE Electron Device Letters,* vol. 32, pp. 1695-1697, Dec. 2011.
[134] G. Crawford, *Flexible flat panel displays*: Wiley, 2005.
[135] H. Gleskova, S. Wagner, W. Soboyejo, and Z. Suo, "Electrical response of amorphous silicon thin-film transistors under mechanical strain," *Journal of applied physics,* vol. 92, pp. 6224-6229, Nov. 2002.
[136] Y. Sun, S. E. Thompson, and T. Nishida, *Strain Effect in Semiconductors: Theory and Device Applications*: Springer, 2009.
[A.1] C. Tang and S. VanSlyke, "Organic electroluminescent diodes," *Applied physics letters,* vol. 51, pp. 913-915, 1987.
[A.2] R. Dawson, Z. Shen, D. Furst, S. Connor, J. Hsu, M. Kane, *et al.*, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," in *International Electron Devices Meeting 1998*, 1998, pp. 875-878.
[A.3] T. Scheffer and B. Clifton, "Active addressing method for high-contrast video-rate STN displays," in *SID*, 1992, pp. 228-231.
[A.4] T. Sunata, T. Yukawa, K. Miyake, Y. Matsushita, Y. Murakami, Y. Ugai, *et al.*, "A large-area high-resolution active-matrix color LCD addressed by a-Si TFT's," *IEEE Transactions on Electron Devices,* vol. 33, pp. 1212-1217, Aug. 1986.
[A.5] K. Ichikawa, S. Suzuki, H. Matino, T. Aoki, T. Higuchi, and Y. Oana, "14.3-in.-Diagonal 16-Color TFT-LCD Panel Using a-Si: H TFTs," in *Digest of Technical Papers, 1989 SID International Symposium*, 1989, p. 226.
[A.6] S. H. Jung, W. J. Nam, and M. K. Han, "A new voltage-modulated AMOLED pixel design compensating for threshold voltage variation in poly-Si TFTs," *IEEE Electron Device Letters,* vol. 25, pp. 690-692, 2004.
[A.7] S. M. Choi, O. K. Kwon, and H. K. Chung, "An Improved Voltage Programmed Pixel Structure for Large Size and High Resolution AM-OLED Displays," in *SID Symposium Digest of Technical Papers*, 2004, pp. 260-263.
[A.8] S. Choi, O. Kwon, N. Komiya, and H. Chung, "A self-compensated voltage programming pixel structure for active-matrix organic light emitting diodes," in *IDW Tech Dig.*, 2003, pp. 535-8.
[A.9] B.-W. Lee, I.-H. Ji, S.-M. Han, S.-D. Sung, K.-S. Shin, J. D. Lee, *et al.*, "51.1: Novel Simultaneous Emission Driving Scheme for Crosstalk-free 3D AMOLED TV," *SID Symposium Digest of Technical Papers,* vol. 41, pp. 758-761, 2010.

초록

능동 액정 디스플레이나 능동 유기발광 다이오드 디스플레이 등과 같은 평판 디스플레이는 대면적화, 고해상도화, 빠른 구동속도가 요구되고 있는 가운데 차세대 디스플레이로서는 플렉서블 디스플레이 연구가 활발히 이루어지고 있다. 그러나 널리 사용되어 온 비정질 실리콘 박막 트랜지스터의 이동도와 같은 전기적 특성은 이러한 요구사항을 만족시킬 수 없기 때문에 인듐갈륨징크 산화물 (IGZO) 박막 트랜지스터와 같이 이동도, 균일도, 공정 온도 면에서 우수한 특성을 갖는 비정질 산화물 박막 트랜지스터가 차세대 디스플레이 기술로서 각광을 받고 있다. 그러나 산화물 박막 트랜지스터를 다양한 기술에 적용 및 응용하기 위해서는 빛을 비추었을 때의 전기적 소자 특성 변화 및 신뢰성 문제를 해결해야 한다.

본 학위 논문에서는 IGZO 박막 트랜지스터에 빛을 비추었을 때의 전기적 소자 특성 및 신뢰성 문제에 대해 연구하였고, 플렉서블 기판에 제작했을 때의 신뢰성에 대해 연구하였다.

먼저 빛이 비추어졌을 때 IGZO 박막 트랜지스터의 전기적 특성변화에 대해 분석하였다. 자외선을 비추었을 때 I-V 특성 측정 시 이력현상 (hysteresis)과 함께 누설전류가 관찰되었다. 이는 인듐갈륨징크 산화물 반도체의 전도대 근처에 생성된 유사 도너 상태에 의한 것으로 설명할 수 있고 이온화된 oxygen vacancy

(Vo^{2+}) 생성이 원인인 것으로 볼 수 있다. 이력현상은 Vo^{2+}가 게이트 전압 변화에 따라서 ~10^0 초의 반응속도를 갖기 때문에 관찰되는 현상임을 알 수 있었다. 또한 누설전류는 빛에 의해 생성된 캐리어의 광전류 메커니즘을 따르지 않았고, 계면에 생성된 유사 도너 상태에 의한 현상임을 시뮬레이션을 통해 검증하였다.

자외선을 비춘 상태에서 음의 게이트 전압 스트레스를 가했을 때의 문턱전압 열화에 대해 연구하였다. 문턱전압은 빛에 의해 생성된 홀(hole)이나 Vo^{2+}가 게이트 절연막에 트랩되기 때문에 감소하는 것으로, 특히 IGZO 내부에서 ~10^2 초의 비교적 큰 반응 속도를 가지고 Vo^{2+}가 생성된다고 볼 수 있었다. 또한 빛의 세기에 따라 생성된 홀의 게이트 절연막으로의 트랩 확률이 일정하다는 것을 알 수 있었다.

마지막으로 플렉서블 플라스틱 기판에 제작된 IGZO 박막 트랜지스터의 신뢰성 연구를 진행하였다. 기판을 10 mm, 4mm, 2 mm의 곡률반경으로 구부렸을 때 평판 상태 대비 소자의 전기적 특성 변화는 관찰되지 않았고, 음의 게이트 전압 스트레스를 가했을 때 문턱전압 이동이 가속되는 것을 확인할 수 있었다. 이를 통해 소자의 물리적 변형율이 전기적 스트레스를 가속시킨다는 것을 알 수 있었고, IGZO의 가전자대의 이동을 원인으로 볼 수 있었다.

주요어: 박막 트랜지스터, 산화물 반도체, 광조사, 게이트 전압

스트레스, 플렉서블 디스플레이

학 번: 2009-20860