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하이브리드 전력 저장 시스템의 설계 및 운용 최적화

Design and Runtime Optimizations of Hybrid Electrical Energy Storage Systems

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전기컴퓨터공학부

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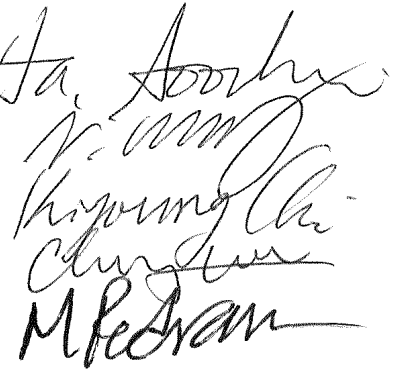이 논문을 공학박사학위논문으로 제출함

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Abstract

Electrical energy storages (EES) systems provides various benefits of high energy efficiency, high reliability, low cost, and so on, by storing and retrieving energy on demand. The applications of the EES systems are wide, covering contingency service, load leveling, peak shaving, energy buffer for renewable power sources, and so on. Current EES systems mainly rely on a single type of energy storage technology, but no single type of EES element can fulfill all the desirable characteristics of an ideal electrical energy storage, such as high power/energy density, low cost, high cycle efficiency, and long cycle life. A hybrid electrical energy storages (HEES) system is composed of multiple, heterogeneous energy storage elements, aiming at exploiting the strengths of each energy storage element while hiding its weaknesses, which is a practical approach to improve the performance of EES systems. A HEES system may achieve the a combination of performance metrics that are superior to those for any of its individual energy storage elements with elaborated system design and control schemes.

This dissertation proposes high-level optimization approaches for HEES systems in order to maximize their energy efficiency. We propose new architectures for the HEES systems and systematic design optimization methods. The proposed networked charge transfer interconnect (CTI) architecture and bank reconfiguration architecture minimizes the power

conversion loss and thus maximizes the charge transfer efficiency of the HEES system. We also point out the limitation of the conventional control schemes and propose a joint optimization design and control considering the power sources. The proposed maximum power transfer tracking (MPTT) operation and MPTT-aware design method effectively increases energy harvesting efficiency and actual available energy. We finally introduce a prototype of a HEES system implementation that physically proves the feasibility of the proposed HEES system.

Keywords: energy storage system, hybrid electrical energy storage system

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Chapter 1

Introduction

Electrical energy is a high quality form of energy [1], which can be easily and efficiently converted to other forms of energy and used to control other lower quality forms of energy. Transformity of energy, which is the amount of one type of energy required to produce a heat equivalent of another type of energy, is an important factor of the quality of energy. Energy with higher transformities require larger amounts of sunlight for their production, and therefore are more economically useful [2]. Electrical energy can be efficiently transformed into other forms of energy, with a transformity of 1.59×10^5 seJ/J (solar emjoules per joule), which is 2–4 times higher than that of fossil fuel energy [3].

Electrical energy consumption in a system changes over time due to changes in the power requirements of load devices and user behaviors. The level of power generation of fossil fuel power plants and nuclear power plants cannot be adjusted immediately, and so they are not capable of dealing with the rapid change in the power consumption. Therefore, we should always generate larger amount of electricity than actually needed to prevent power unreliability, which is unused and wasted.

Renewable power sources also have unreliable power generation characteristics. The

level of power generation of the renewable power sources, such as solar cells and windmills, is heavily dependent on environmental factors (e.g., the solar irradiance level or climate conditions) that are not controllable. Furthermore, power generation from such renewable power sources and the power consumption are typically not balanced with each other in terms of time.

Storage of excess energy mitigates over-investment in power generation facilities and avoids energy waste. An electrical energy storages (EES) system is an energy reservoir which can store energy electrically for future use. EES systems increase availability of electrical energy, mitigate supply-demand mismatches, and reduce the generation capacity required to meet the peak-power demand.

Nevertheless, EES system technologies are still short for wide deployment. So far, development of a better energy storage element technology has been focused as a key to success of high-performance EES systems. However, despite active research on the new energy storage element technologies, it is not likely for us to have an ultimate high-efficiency, high-power/energy capacity, low-cost, light-weight, and long-cycle life energy storage elements in the near future. In other words, there is no single type of energy storage element that can fulfill all the desired requirements as of toady. Current EES systems that are composed of heterogeneous energy storage elements are subject to the limitation of the energy storage elements that are used.

It is a practically promising solution to develop system-level design methodology that enhances storage system performance and lifetime through efficient use of the current energy storage technologies. Hybrid electrical energy storages (HEES) systems consist of multiple heterogeneous EES elements in order to exploit the advantages of the EES elements while hiding their shortcomings with aid of system-level managements such as architecture and control policy designs [4, 5]. This approach aims to achieve the a combi-

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nation of performance metrics that are superior to that for any of its individual EES components from the heterogeneity. However, such improvements can be achieved only by HEES systems that are well designed and well controlled by elaborated design and control techniques. Hence, development of design and control techniques for HEES systems is the goal of this dissertation.

1.1   Motivations

Let us discuss the motivation of the hybrid approach for the EES systems from the issues in designing memory subsystem of computers. Table 1.1 shows some representative computer memory devices. Static random access memory (SRAM) has the lowest latency and highest throughput but expensive and has low capacity. On the other hand, dynamic random access memory (DRAM) is inferior to the SRAM in terms of latency and throughput, but cheap and has a high capacity. Mass storage devices such as a hard disk drive (HDD) and flash memory have even lower cost, higher capacity, non-volatility, but are subject to limited random access capability and write count. Composing the required memory space with the SRAM only is infeasible due to its high cost except for supercomputers where cost is not a primary issue. On the other hand, using HDD or flash memory only cannot meet the latency and throughput requirements of the central processing unit (CPU) core and suffers from poor random access capability and limited write count. Computer architects, therefore, have remedied this problem by building a hierarchy of different types of memory devices. A typical memory hierarchy example is illustrated in Figure 1.1(a). L1 (level 1) SRAM cache provides the best latency and throughput but smallest capacity, and L2 (level 2) SRAM cache has a bit poor latency and throughput but is larger than the L1 cache. They both generally reside on chip to provide a fast access speed. The DRAM main memory is

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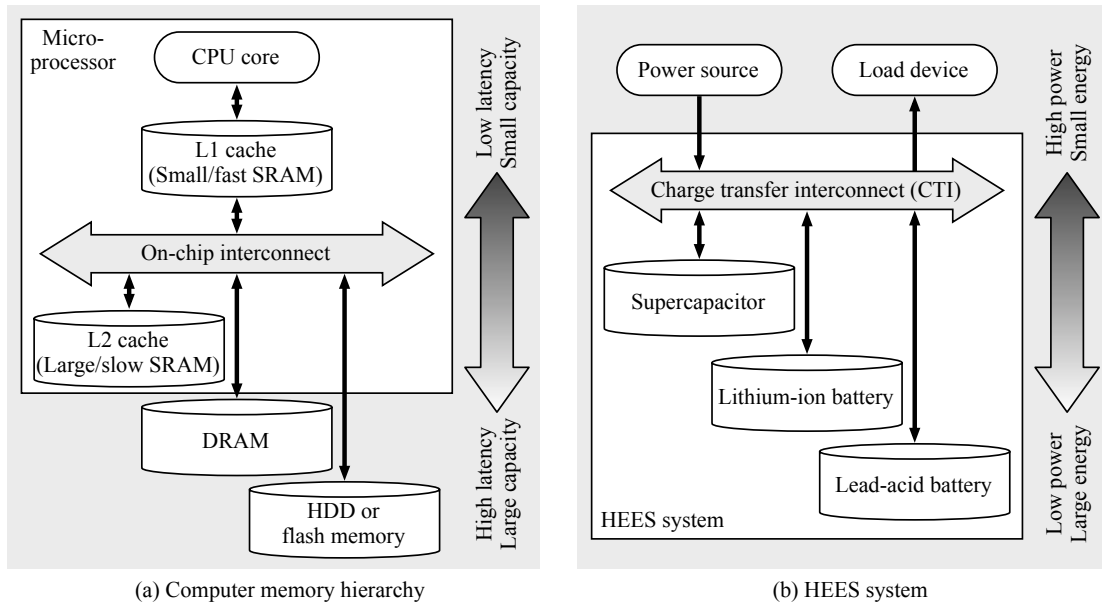
Figure 1.1: Comparison of computer memory hierarchy and HEES system architecture.

placed off chip, or sometime on chip for better latency, provides a much larger capacity with a higher latency and lower throughput than the L1/L2 SRAM caches. Finally, the slowest HDD and flash memory are used to provide the largest storage space. There are many policies to utilize this memory hierarchy efficiently, but generally speaking, we use a faster memory to store frequently accessed data to take advantages of its high speed, and overcome its capacity limitation by moving less frequently accessed data down to a slower memory. As a result, this memory hierarchy enables the CPU to exploit the low latency of the L1 SRAM cache as well as the large capacity of the HDD at the same time.

The HEES systems aim at similar benefits by using multiple heterogeneous EES elements. Instead of relying on a single type of EES element, the HEES systems exploit distinct advantages of multiple heterogeneous EES elements and hide their drawbacks. For instance, electrical vehicle (EV) and hybrid electrical vehicle (HEV) exhibit frequent charge/discharge cycles with a short period and a large amount of current. Conventional

Table 1.1: Comparison of memory devices [6].

| | Cost | Current (mA) | | Random access time (16 bit) | | | |
| | ($/Gb) | Idle | Active | Read | Write | Erase | Non-volatile |
Density							
Fast SRAM	Low	614	5	65	10 ns	10 ns	10 ns	No
Low power SRAM	Low	320	0.005	3	55 ns	55 ns	55 ns	No
Mobile synch. DRAM	High	48	0.5	75	90 ns	90 ns	90 ns	No
NOR flash	High	96	0.03	32	200 ns	210.5 μs	1.2 s	Yes
NAND flash	Very high	21	0.01	10	10.1 μs	200.5 μs	2 ms	Yes

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batteries make it difficult to maintain a high efficiency and a longer cycle life in such an operational environment. Use of supercapacitors may be huge upgrade in terms of efficiency and cycle life. However, the current supercapacitor technologies have serious disadvantages in energy density and cost, which makes it hard to completely replace the battery in EV with supercapacitors despite of a testbed supercapacitor-only EV [7]. Use of supercapacitors in a complementary manner reinforces the drawback of the battery through high power density, long life cycles, and high efficiency [8, 9, 10, 11].

A conceptual drawing of the HEES system is shown in Figure 1.1(b). An HEES system is comprised of a number of EES banks, and is connected to external power sources and load devices. The HEES system in Figure 1.1(b) is composed of a supercapacitor, lithium-ion battery, and lead-acid battery. Similar to the computer memory hierarchy, the HEES system exploits different superiorities of these three energy storages: the high power density and long cycle life of the supercapacitor and the relatively low cost and high energy density of lithium-ion battery and lead-acid battery. The charge transfer interconnect (CTI) internally connects the energy storages, external power sources, and external load devices though appropriate power converters.

Employing the HEES system concept comes with additional design considerations. Deployment of an HEES system does not always guarantee better performance unless proper design consideration is elaborated. Designer should carefully determine selection of EES elements, proportion of each energy storage elements, system architecture, management policy, etc, in order to maximize the benefits of the HEES system over the conventional homogeneous EES systems.

1.2 Contribution and Significance

This dissertation is to leverage the advantages of the HEES systems with elaborated architecture design and control policies mainly focusing on the energy efficiency improvement. There are different levels of approaches, from material development for energy storage elements to high-level system management, that maximize the benefits of the HEES systems. Among them, we focus on high-level approaches. More specifically, we consider the following questions throughout this dissertation.

- How to leverage the advantages of different energy storage elements?

- What factors and components affect the energy efficiency of the HEES systems?

- How to maximize the benefits of the HEES systems through architecture-level and system-level design methodologies?

- How to achieve the joint optimization of the HEES systems together with the power sources and load devices?

Contributions of this dissertation can be summarized as follows.

- We propose new architecture designs for the HEES systems to maximize the energy efficiency. We introduce the optimization issues involves in the new architecture designs and their operations.

- We model the problems for the HEES systems as conventional electronic design automation (EDA) problems and utilize the solution methods for the EDA problems for the HEES systems. We show potential that the systematic optimization methods of EDA problems can be used for the HEES system optimizations.

- We study the limitations of conventional operating methods and suggests a new

method that maximizes the energy efficiency. We specially focus on maximizing solar energy harvesting considering the energy efficiency of the HEES systems.

- We implement a prototype of a HEES system to verify the proposed control methods.

1.3 Organization of Dissertation

Chapter 2 reviews the background study on the energy storage elements and related work in EES and HEES systems. Chapter 3 is a discussion on the architecture, components, and design considerations of the HEES systems. Chapter 4 introduces our system-level design optimization efforts for the HEES systems. Chapter 5 expands the optimization scope to include the power sources. Chapter 6 introduces some experimental results and HEES system prototype implementation. Chapter 7 concludes this dissertation and suggests future research directions.

Chapter 2

Background and Related Work

2.1 Electrical Energy Storage Elements

An *EES element* is a unit device or apparatus that is capable of storing electrical energy in the potential, kinetic, chemical, or another form of energy, and restoring the stored energy back to the electrical energy. An example of widely known EES elements is an alkaline battery. There are diverse kinds of EES elements developed and used so far. In this chapter, we overview the various EES elements and compare their characteristics in different aspects. We first discuss some important metrics that are used to evaluate EES elements in Section 2.1.1 in detail. We compare some representative EES elements in the aspects of discussed metrics in the following Section 2.1.2. We do not discuss internal principles of storing the energy, such as chemical reactions, in detail, but focus on evaluating their performances and prices as energy storages.

2.1.1 Performance Metrics

In this section, we discuss the performance metrics that we use to describe EES elements in Section 2.1.2. We focus on how a good EES element and a poor EES element should be combined in a view point of HEES system design.

2.1.1.1 Power and Energy Density

Power density is defined as the rated output power divided by volume (W/L) or mass (W/kg) of the EES element. Similarly, *energy density* is the stored energy divided by the volume (Wh/L) or mass (Wh/kg). Generally speaking, power density is related to the amount of instant power that the ESS element can handle; on the other hand, energy density is related to the time duration that the EES element can last with handling a certain amount of power.

Supercapacitor and flywheel have a high power density, batteries typically have a marginally high power density. High-power density EES elements are suitable for dealing with short-duration high-power temporary energy buffer. Metal-air batteries and fuel cells have a high energy density which is multiple orders of magnitude higher than typical batteries. High-energy density EES elements are suitable for a long-term steady energy storage. Super-capacitor is one of the EES elements that has the worst energy density, and so it is not beneficial to use supercapacitor alone as a large-scale energy storage.

A HEES system can take advantage of high-energy density EES elements for large-amount, long-term storage and compensate its power density with a relatively small amount of high-power density EES elements. Battery-supercapacitor hybrid is a representative application that exploits the high energy density of the battery and high power density of the supercapacitor [8, 12, 13, 14, 15, 10, 11, 16, 17, 18, 19, 20, 21, 9].

2.1.1.2 Capital Cost

Capital cost, which is one of the most important considerations in the design and implementation of an EES system, is typically represented in the forms of cost per unit of output power ($/W) or per unit of delivered energy ($/Wh). Capital cost determines how much money should be invested in order to build an EES system with certain amount of energy capacity or power capacity.

We should carefully determine the portion of expensive (but good) EES elements and inexpensive (but poor) EES elements with given constraint on the total amount of available money. In fact, the capital cost gap between EES elements is the fundamental motivation of hybrid approach because we cannot use unlimitedly large amount of good and expensive EES elements to meet the all requirements. For example, we may need a small amount of supercapacitors to meet a power requirement, but may need a very large amount of them to meet an energy requirement due to their poor energy density, which would lead to an impractically high capital cost.

Some previous research attempt to minimize the cost of HEES systems. A sizing optimization method for stand-alone photovoltaic power systems with a HEES system is presented to find the cost-optimal combinations of photovoltaic module, fuel cell, and battery [22]. Control strategies for a battery and fuel cell HEES system is studies for optimization of system performance and cost [23].

2.1.1.3 Cycle Efficiency

Cycle efficiency of an EES element is defined by the round-trip energy efficiency, i.e., ratio of the amount of energy output during discharging to the energy input during charging. In other words, the cycle efficiency is the product of charging efficiency and discharging

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efficiency. Here, the charging efficiency is the ratio of energy stored in an EES element after charging to the total energy supplied to that element during the entire charging process, and discharging efficiency is the ratio of energy extracted from an EES element during the discharging to the total energy before the discharging process begins.

Cycle efficiency is significantly affected by charging/discharging profiles, i.e., the amount and shape of the charging/discharging current. For example, due to the well-known rate capability issue, the total charge or energy delivered by a battery goes down with the increase in load current, resulting in lower discharging efficiency. At the same time, the recovery effect of battery which recovers the terminal voltage during idle periods between current pulses also affects the cycle efficiency of the battery [24].

Supercapacitor and flywheel have a very high cycle efficiency which is close to 100% and less affected by the charging/discharging profile. A high cycle efficiency means less energy loss during charging and discharging processes which leads to low operational cost per each cycle. Therefore, it is wise to use a high-cycle efficiency EES element such as supercapacitor for frequent charging/discharging applications.

2.1.1.4 State-of-Health and Cycle Life

State of health (SoH) of an EES element is a measure of its age. It reflects the general condition of the EES element and its ability to store and deliver energy compared to its initial state (i.e., compared to a fresh new EES element). During the lifetime of the EES element, its capacity or 'health' gradually deteriorates due to irreversible physical and chemical changes which take place along with usage. The cycle life is the maximum number of charging and discharging processes that an EES element can perform before its capacity drops to a specific percentage (60–80% typically) of its initial capacity. It is one of the key performance parameters and gives an indication of the expected working lifetime of the

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EES element. Obviously cycle life of an EES element is closely related to the replacement period and full cost of the element according to a lifecycle analysis.

The cycle life of an EES element heavily depends on the usage pattern of the element, especially to the depth of discharge (DoD) which is defined as ratio of used capacity to the initial full capacity. For lead-acid batteries, the number available charging/discharging cycles increases when lowering the DoD [25]. Similar conclusions hold for most electrochemical batteries.

Typically, EES elements whose operation principles are based on electrical, mechanical or thermal technologies, such as supercapacitor, flywheel, thermal energy storage (TES), cryogenic energy storage (CES), typically have long cycle lives. In contrast, cycle life of electrochemical batteries are not that high due to unavoidable chemical deterioration of the electrodes during their operation.

2.1.1.5 Self-Discharge Rate

Self-discharge rate is a measure of how quickly a storage element loses its energy when there is no charging and discharging current. It is heavily dependent on how the EES element stores the energy inside, as well as ambient conditions such as temperature and humidity. Supercapacitor and flywheel, which have a high cycle life, have highest self-discharge rate; they loss all the energy within couple of weeks or days, or even hours. On the other hand, electrochemical batteries store the energy with stable chemicals, and do not lose so much energy by themselves. The self-discharge rate is related to the operational energy cost. One should not store energy in a supercapacitor if it is expected that the energy will not be used for a long time.

2.1.1.6 Environmental Impacts

The importance of environmental friendliness of EES elements is being realized recently. Typically, electrochemical batteries have negative impacts on the environment due to their toxic metals such as lead and cadmium that may be harmful if not disposed of properly. They should be recycled properly for both reducing environmental impact and securing resources [26]. On the other hand, supercapacitor and flywheel have very small or almost negligible impacts on the environments, not only because they no not contain harmful materials, but also because of their long life cycle. The environmental impacts is closely related to the cycle life. We can reduce the negative impacts of using harmful EES elements by extending the life cycle of them.

2.1.2 Energy Storage Elements

The primary driving force of EES system research has been energy storage element technology such as advanced batteries and supercapacitors [27, 28]. This is because that performance of homogenous EES systems is largely determined by the energy storage element characteristics. There are numerous types of energy storage elements that stores energy in various forms of potential energy, kinetic energy, chemical energy, and so forth, but we limit the focus of energy storage elements that directly accept electrical energy: batteries and supercapacitors. The advantages of batteries and supercapacitors include higher cycle efficiency, lighter weight, no moving components in the power converter and energy storage, etc. We deal with only batteries and supercapacitors, leaving other types of energy storages out of our scope, but diverse types of energy storages such as kinetic, thermal and chemical energy storages are also available. Examples include flywheels [29], compressed air [30], hydropower using dams [31], thermal energy storage [32], hydrogen-based chem-

ical energy storage system [33], etc.

Energy storage elements have different characteristics. Desirable characteristics of an ideal EES element include a high power density, high energy density, low cost, high cycle efficiency, long cycle life, low self-discharge, high rate capability, and small environmental effect, and so on, as described in Section 2.1.1. These performance metrics are largely variable by the operating conditions. For example, cycle life has exponential dependency on the state of charge (SoC) swing and average SoC, and cycle efficiency is largely dependent on the rate capability. Temperature is an important factor that influences both the cycle life and cycle efficiency. Table 2.1 compares some important characteristics of several representative EES elements. We see that they have distinctive characteristics, and unfortunately, no single type of energy storage element can simultaneously fulfill all the desired characteristics of the ideal one.

2.1.2.1   Lead-Acid Batteries

As one of the oldest and most developed rechargeable battery technologies, lead-acid batteries have short cycle life and low energy density due to the inherent high density of lead as a metal. Besides, they also have a poor low temperature performance and thus a thermal management system is required. In spite of these disadvantages, their ability to supply high surge currents means that such lead-acid cells maintain relative high power density. These features, along with their low cost and high energy efficiency, make lead-acid batteries suitable in motor vehicles so as to provide the high current demand for automobile starter motors. Lead-acid batteries have also been used in a few large-scale commercial energy management systems. Figure 2.1(c) shows an example of a valve-regulated (sealed) lead-acid battery pack, Panasonic LC-R123R4P.

Lead-acid battery technology is considered quite mature now [34], but there are still

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efforts to find better materials for the current collectors, electrodes, electrolytes, etc [35, 36]. A new emerging technology to replace conventional lead-acid batteries is soluble lead-acid flow battery [37, 38, 39]. Though it is still a infancy technology, it has advantages over other types of flow batteries that it requires single electrolyte and no membrane separator. It is suitable for large-scale applications and uses more environmentally friendly electrolyte than the conventional lead-acid batteries, but its DoD-sensitive cycle life and low cycle efficiency should be overcome [37].

2.1.2.2 Lithium-Ion Batteries

Lithium-ion battery, first demonstrated in the 1970s, is a family of rechargeable batteries in which lithium ions move from negative electrode to positive electrode through discharging, and in opposite direction during charging. It is now the battery of choice in portable electronic devices and is growing in popularity in military, electric vehicle, and aerospace applications. The growing popularity of lithium-ion battery is mainly due to the following reasons: high energy density, high efficiency, long cycle life, no memory effect, and low self discharge rate.

While taking over 50% of the small portable devices market [34], there are some challenges to build large-scale lithium-ion based EES. The main hurdle is the high cost due to special packaging and internal overcharge protection circuits. Manufactures are working to reduce the manufacturing cost of lithium-ion batteries to capture large new energy markets, especially markets for the electrical vehicles. Figure 2.1(b) shows a 18650 size lithium-ion battery, ICR18650-22F from Samsung SDI. Multiple lithium-ion batteries of this size are combined in a pack and widely used for portable devices such as laptops.

Like supercapacitors, new materials such as graphene and silicon thin film are under development to improve energy density and cycle life of the lithium-ion batteries as shown

D size

62 mm

33 mm

Maxwell Technologies BCAP0310
Capacitance: 310 F
Rated voltage: 2.7 V
Rated capacity: 0.31 Wh

(c) Supercapacitor

18650 size

65.2 mm

18.6 mm
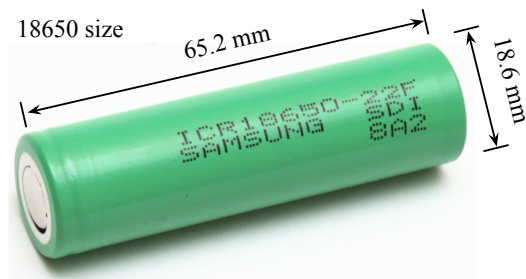
Samsung SDI ICR18650-22F
Nominal voltage: 3.7 V
Rated capacity: 2.2 Ah

(e) Li-ion battery

133 mm

67 mm

60 mm

Panasonic LC-R123R4P
Nominal voltage: 12 V
Rated capacity: 3.4 Ah (20 hour rate)

(a) Lead-acid battery

14 mm

AA size

50 mm
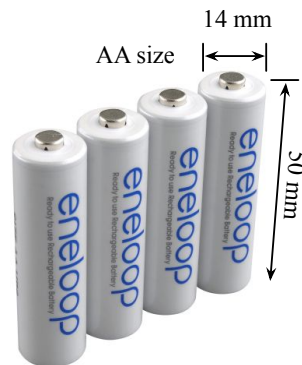
Sanyo HR-3UTGA
Nominal voltage: 1.2 V
Rated capacity: 2.0 Ah

(d) NiMH battery

Figure 2.1: Example products of supercapacitor and various batteries.
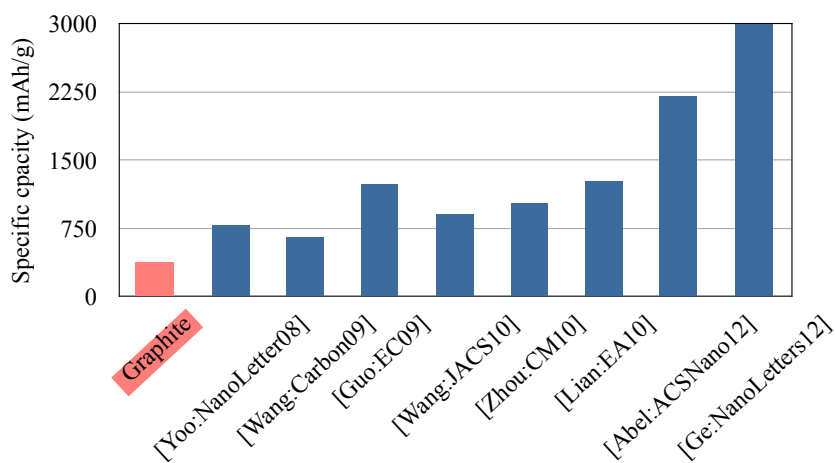
Figure 2.2: Specific capacity improvement with respect to the electrode weight of lithium-ion batteries with new electrode materials.

in Figure 2.2 [27, 28, 40, 41, 42, 43, 44, 45, 46, 47, 48].

2.1.2.3 Nickel-Metal Hydride Batteries

Nickel-metal hydride (NiMH) battery is a type of rechargeable battery similar to the nickel-cadmium (NiCd) cells. The only difference is that the former one uses a hydrogen-absorbing alloy for negative electrode instead of cadmium. The energy density of NiMH batteries is more than double that of lead-acid batteries and 40% higher than that of NiCd batteries. The NiMH battery relatively inexpensive to purchase. However, they suffer from the memory effect, although much less pronounced than that in the NiCd ones, and have a rather high self-discharge rate. Recently, low self-discharge (LSD) NiMH battery are commercialized for portable devices. Figure 2.1(d) is a commercial product of an AA size LSD NiMH battery from Sanyo. Toyota Prius HEV also uses NiMH batteries [49].

The most significant feature of NiMH batteries is the high power density, which is the

highest among existing battery types. Therefore these batteries are widely used in high current drain consumer electronics, such as digital cameras with liquid crystal displays (LCDs) and flashlights. Recently, they have been used in hybrid electric vehicles such as the Toyota Prius, Honda Insight, Ford Escape Hybrid, Chevrolet Malibu Hybrid, and Honda Civic Hybrid.

2.1.2.4 Supercapacitors

Electric double-layer capacitors, more commonly known as supercapacitors or ultracapacitors, are widely exploited to mitigate load current fluctuations in the batteries. Supercapacitors have a superior cycle efficiency which reaches almost 100%, and long cycle life [50]. Moreover, compared with batteries, supercapacitors exhibit significant higher volumetric power density but lower energy density [51]. Thus they are suitable for energy storage in situations with frequent charging/discharging cycles or periodic high current pulses. In a battery-supercapacitor hybrid system, the supercapacitor stores surplus energy from the battery during low demand periods, and provides extra energy during peak load current demand period.

However, a distinct disadvantage of a supercapacitor is its large self-discharge rate compared to that of ordinary batteries. A supercapacitor may lose more than 20% of its stored energy per day even if no load is connected to it. Another important concern of supercapacitors in HEES systems is the terminal voltage variation coming from the characteristics of a capacitor nature whereby the terminal voltage is linearly proportional to its SoC. The terminal voltage increases or decreases accordingly as the supercapacitor is charged or discharged. This terminal voltage variation is much higher than that observed in typical batteries. This effect results in a significant conversion efficiency variation in the power converters which are connected to the supercapacitors. The hybrid energy storage systems

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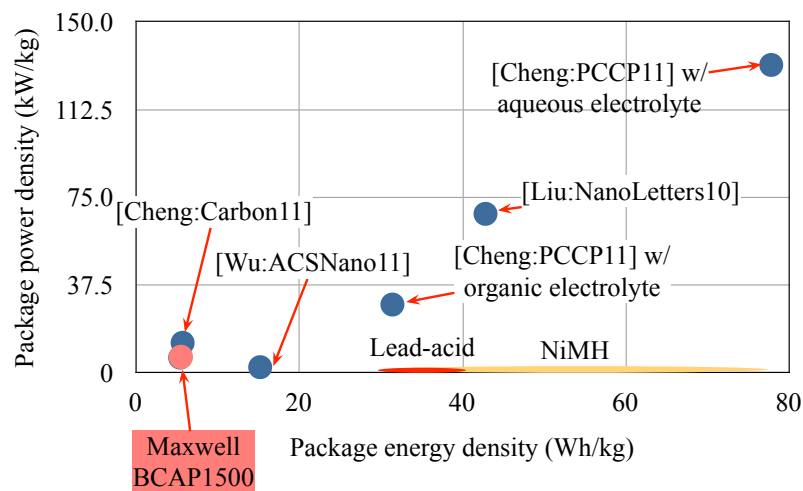
Figure 2.3: Power and energy density improvement of supercapacitors with new electrode materials. Package density is approximated to the half of the density with respect to the electrode weight [56].

including the supercapacitor should properly account for the above characteristics to be practical.

Figure 2.1(a) is a supercapacitor commercially available, BCAP0310 from Maxwell Technologies. Its size is same to the D size battery, and it has a 310 F capacity with the maximum voltage of 2.7 V, which results in 0.31 Wh energy capacity. A high energy density D size lithium primary battery has 68.4 Wh energy capacity.

Research efforts are being devoted to develop new materials that enhances the energy density of the supercapacitors as shown in Figure 2.3. Graphene and carbon nanotube (CNT) are actively studied for supercapacitor electrodes [40, 52, 53, 54, 55, 56, 57, 58, 59]. For example, graphene/CNT composite electrodes introduced in [55] achieves a very high energy density 155.6 Wh/kg which is compared to NiMH batteries.

2.1.2.5 Other Energy Storage Elements

There are also other types of EES elements such as NiCd battery, sodium-sulfur (NaS) battery, metal-air battery, and flywheel. We do not cover all the detail of those EES elements. Characteristics of those EES elements are summarized in Table 2.1 together with the EES elements we discussed above.

2.2 Homogeneous Electrical Energy Storage Systems

2.2.1 Energy Storage Systems

An *EES system* is an energy reservoir which stores electrical energy and supplies the energy when necessary [34]. The electric energy is stored in the EES system as potential energy, kinetic energy, chemical energy, or in some other form. EES systems perform many useful functions such as load leveling, contingency service, voltage stabilization, maximum power point tracking (MPPT) for renewable power sources, etc, for a wide range of applications including portable devices, household appliances, electrical vehicles, and even power grid. Storing energy connected to the power grid enables electricity to be produced when the demand is low or generation cost is low, and consumed when the demand is high or generation cost is high. It reduces the maximum power generation capacity requirement of the power generation infrastructure by reducing the peak demand. Another representative application is renewable power sources. The EES systems are considered mandatory for renewable power sources to enable MPPT that maximizes the power generation from the power source regardless the load demand.

A typical EES system consists of a single type of EES elements. A variety of EES elements is introduced and utilized these days, and they have different characteristics in many

aspects. Desirable characteristics of an ideal EES element include a high power density, high energy density, high cycle efficiency, low cost, long cycle life, small environmental effect, and so on. Table 2.1 compares some important characteristics of several representative EES elements. We see that they have distinctive characteristics, and unfortunately, no single type of EES element can simultaneously fulfill all the desired characteristics of an ideal EES element. For example, a lead-acid battery provides a high energy capacity, low self-discharge, relatively constant terminal voltage, and relatively low cost, but suffers from a lower rate capability and limited cycle life when compared with supercapacitors. In contrast, a supercapacitor is superior to the lithium-ion battery in cycle efficiency, cycle life, and capability of dealing with high peak power demands, but its energy density and self-discharge rate are poor. Therefore, an EES system made of a single type of EES element is bounded by the particular limitations of the EES element used.

A typical EES system consists of a single type of energy storage elements. This is natural since the homogeneity offers ease of implementation, control and maintenance. Figure 2.4 illustrates the architecture of a typical homogeneous EES system. It is composed of energy storage elements, input power converter, and output power converter. Multiple energy storage elements are typically combined together to provide high energy capacity and/or high power capacity. The input converter (e.g., air compressor, motor, and charger) performs energy transduction and/or power regulation from the power source to the energy storage element, and the output converter (e.g., turbine, generator, and DC–DC converter) performs the same from the energy storage element to the load device. Applications of the EES systems include a wide range of scales from portable devices (a few Wh or smaller); household appliances and electrical vehicles (a few kWh); and even power grid (hundreds of kWh or larger).

Significant research effort has focused on EES systems for decades because storing

Table 2.1: Comparison of energy storage elements [34, 60, 61, 62, 63, 64].

EES elements	Power density (W/kg)	Energy density (Wh/kg)	Capital cost ($/kWh)	Cycle efficiency	Cycle life	Self-discharge per day
Lead-acid battery	180	30–40	74–222	70–90%	500–800	0.1–0.3%
Lithium-ion battery	1,800	150–250	1,040–1,484	80–90%	1,200	0.1–0.3%
NiMH battery	250–1,000	30–80	450–1,000	66%	500–1,000	2%
NiCd battery	150	40–60	296–890	70–90%	1,50	0.2–0.6%
NaS battery	150–230	150	300–500	90%	2,500	˜20%
Metal-air battery	-	450–650	74–296	<50%	100+	Very small
Supercapacitor	1,000–2,000	2.5–15	2,000	>93%	10,000–100,000+	20–40%
Flywheel	1,000	100–130	5,000	90%	100,000+	100%

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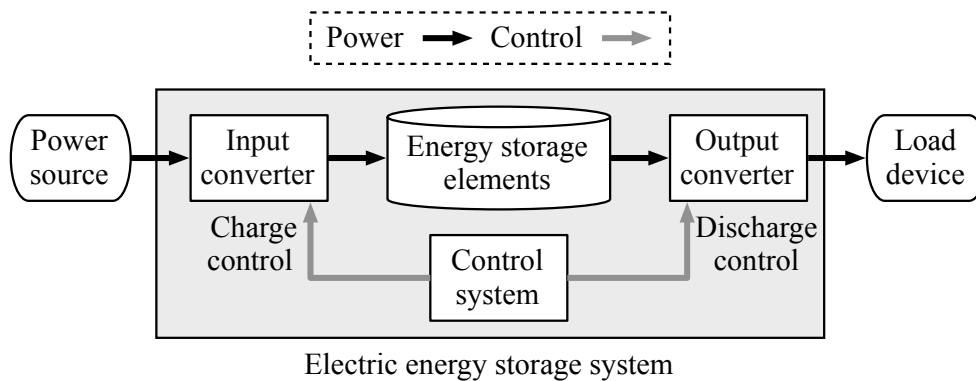
Figure 2.4: Architecture of a typical homogeneous EES system.

excess electrical energy is a natural need. Recent world-wide energy crisis is even more ac-
celerating the demands on practical deployment of EES systems. There are numerous EES
systems deployed over the world that are composed of lead-acid batteries, NiCd batteries,
lithium-ion batteries, or regenerative fuel cell [65]. EES systems are deployed for purposes
of power supply variation compensation and peak load shaving. The Department of Energy
introduces that a battery array incorporated with the solar cell in a house substantially en-
hances efficiency, and reduces overall energy cost despite the cost of the battery [66]. Some
testbed residential EES systems are equipped with lithium-ion batteries [67, 68].

Designing homogeneous EES systems involves numerous design considerations. First
of all, selection of the energy storage element is the most important decision of a homo-
geneous EES system design since the system performance is primarily determined by the
energy storage elements used. Power and energy capacity of a homogeneous EES sys-
tem is scaled by scaling the energy storage element array dimension, and the total capital
cost is determined accordingly. Cycle efficiency and cycle life is compromised with the
cost because they are related with the power capacity (maximum charge/discharge current
limitation to and from the energy storage elements) and energy capacity (SoC variation),

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respectively. The self-discharge rate is determined by what energy storage elements used, and is constrained by the EES system's application (short-term or long-term storage purpose). Both the cycle efficiency and self-discharge rate are closely related with energy cost during operation. The power converter design is crucial because its efficiency gives significant impact on the whole EES system efficiency. Input and output control and adaptation, such as consideration of power grid electricity price, MPPT of the input sources, etc., also should be taken into account.

2.2.2   Applications of EES Systems

The EES systems are widely utilized for diverse applications. A comprehensive review of the EES system applications is presented in [34]. The focus of this review is mainly on the large grid-scale applications, but we can expand those applications to the medium- and small-scale EES systems.

2.2.2.1   Grid Power Generation

The EES system can be used as a commodity storage for storing energy during off-peak period for use during peak period for arbitraging production price. Such systems may eliminate peak load demand to reduce maximum power generation capacity (peak shaving), or make the load demand uniform over time for generation, transmission, and distribution systems (load leveling).

Another application of the EES system is contingency service, which supplies power when the grid power generation plants fall off-line to provide power without interruption. An example for this application is an uninterruptible power supply (UPS) system shown in Figure 2.5(a) that supplies power to servers in data centers. Typical UPS systems for data centers are composed of lead-acid batteries or flywheels. It is also reported that a grid-

Photo from apc.com

(a) APC Smart-UPS 1500VA, a 980 W
lead-acid battery UPS for servers

Photo from gvea.com

(b) Golden Valley Electric Association EES system, Fairbanks,
AK, a 27 MW NiCd battery EES system for power grid

Figure 2.5: EES system applications for grid power generation.

scale NiCd battery-based EES systems shown in Figure 2.5(b), operated by Golden Valley
Electric Association (GVEA) Alaska, is designed to provide 15 minutes of community load
against the power failure [69].

The EES system aids the power generation also by preventing unplanned transfer of
power and maintaining a state of frequency equilibrium. In addition, it may start up on its
own and energize the power generation system after black-out.

2.2.2.2 Renewable Energy

Renewable power source such as solar cells and windmill generations almost always man-
date EES systems for various benefits. The EES systems for the renewable power sources
mitigates uncontrollable power generation due to environmental conditions (e.g., solar ir-
radiance, wind strength). It also enables MPPT that maximizes the power generation of
the use-it-or-waste-it power sources regardless the load variation. The EES system also
performs frequency stabilization against sudden load changes.

2.2.3 Previous Homogeneous EES Systems

2.2.3.1 Battery EES Systems

The EES systems are already being practically deployed for purposes of power supply variation compensation and peak load shaving. An overview gives some examples of such EES systems deployed over the world which are composed of lead-acid batteries, NiCd batteries, lithium-ion batteries, or regenerative fuel cell [65]. The reported EES systems in the overview are composed of homogeneous EES elements. A report from the Department of Energy indicates that a battery array incorporated with the solar cell in a house substantially enhances efficiency, and reduces overall energy cost despite the cost of the battery [66].

There are some high-level control methods developed for lithium-ion battery-based homogeneous EES system for residential purpose [67, 68] to reduce system capital cost and energy cost by peak shaving and load leveling when time-of-use charge is applied. Another management method introduced employs dynamic programming and expert knowledge base rules to reduce capital cost and energy cost for industrial purpose [70]. EES systems for renewable power sources such as solar cells and windmills are utilized to power generation maximization and voltage/frequency regulation. Those applications may be grid-tied [60, 68, 71], or off-gird (stand-alone) [72, 73, 74, 75]. Capital cost and energy cost reduction in a systematic way has been an important concern for such renewable power source applications [73, 74, 75]. EV/HEV shown in Figure 2.6 is another application are of battery-based EES systems [76, 77]. The research objectives include energy cost reduction and life cycle maximization [76] and energy capacity optimization with power management [77].

Implementation of an EES systems involves many issues including power circuit design and control method design. Some researches focus on developing system control methods

Figure 2.6: An example of battery-based EES system applications, Toyota plug-in hybrid vehicle with lithium-ion batteries.

such as SoC balancing between batteries [78] or power flow control of each battery [79]. System-level design and implementation of a grid-tied EES system prototype using lithium-ion batteries is introduced in [80].

2.2.3.2 Supercapacitor EES Systems

Supercapacitors are attracting more attentions for EES systems with their high power density, long life cycles, and high efficiency. An article introduces and categorizes applications of supercapacitor-based EES systems [81]. Energy management/conservation applications take advantages the high power capacity and high cycle life of the supercapacitors, and applications include heavy industrial machineries and heavy vehicles as shown in Figure 2.7(a). Power flow in those applications shows frequent charge/discharge cycles with a short period and a large amount of current, which makes the supercapacitors beneficial. Day-night storage, which is charged during daytime and discharged during nighttime, is an application that utilizes its high cycle efficiency. Its fast-charging advantage is utilized for home-use power tools such as a cordless screwdriver as shown in Figure 2.7(b).

(a) Regenerative energy storage for a seaport crane   (b) Coleman FlashCell cordless screwdriver

Figure 2.7: Examples of supercapacitor-based EES system applications [81].

Supercapacitor in EV/HEV are utilized as a high power and high efficiency energy buffer for acceleration and regenerative braking. A supercapacitor-only EV, which has no other power sources like combustion engine or battery, is introduced in [7]. A voltage equalization method for supercapacitor HEV is introduced in [82]. However, it is more common to use the supercapacitors with other high-energy capacity power sources due to the limitation on the energy capacity of the supercapacitors [8, 12, 13, 14, 15, 10, 11].

Not only for high-power applications such as HEV and power tools, low-power applications such as wireless sensor nodes exploits advantages of the supercapacitors. Energy harvesting is common for self-sustainability for the sensor nodes, and the supercapacitors provide a high cycle efficiency for the harvested energy in the sensor nodes. Examples in the literatures are solar energy harvesting with MPPT [50] and vibration energy harvesting [83].

2.2.3.3 Other EES Systems

We deal with only batteries and supercapacitors, leaving other types of energy storages out of our scope, but diverse types of energy storages such as kinetic, thermal and chemical en-

ergy storages are also available. Examples include flywheels [29], compressed air [30], hydropower using dams [31], thermal energy storage system [32], and hydrogen-based chemical energy storage system [33].

2.3 Hybrid Electrical Energy Storage Systems

2.3.1 Hybridization Architectures

The purpose of previous HEES architectures is to compensate primary drawbacks of the main energy storage element. For instance, as EV should handle a large amount of current during acceleration and deceleration, mitigation of the low rate capability of the primary battery, typically lithium-ion or NiMH batteries, with supercapacitors is beneficial [8, 9, 10, 11].

Figure 2.8 shows HEES architectures proposed in previous literature. Some HEES architectures are specialized for particular purposes such as lowering the effective internal resistance of the energy storage by parallel connection of the primary battery and supercapacitor (Figure 2.8(a)) [21] and buffering the battery current with supercapacitors (Figure 2.8(b)) [18, 19]. The cascaded converter architecture in Figure 2.8(b) has an explicit physical hierarchy and thus charging and discharging the battery should always be buffered by the supercapacitor. The shared bus architecture in Figure 2.8(c) is a more general architecture that all the energy storages are placed physically flat [8, 84, 20]. A typical control policy for this architecture is that one of the energy storages is used for maintain the shared bus voltage at a fixed voltage, and the other energy storages inject designated current into the shared bus. A control policy for this architecture regulates a fast-responding EES element's voltage with a slow-responding EES element in order [8, 84]. Another shared bus-based HEES system proposes a control method to increase the supercapacitor current as

(a) Passive parallel connection topology

(b) Cascade converters topology

(c) Shared bus topology
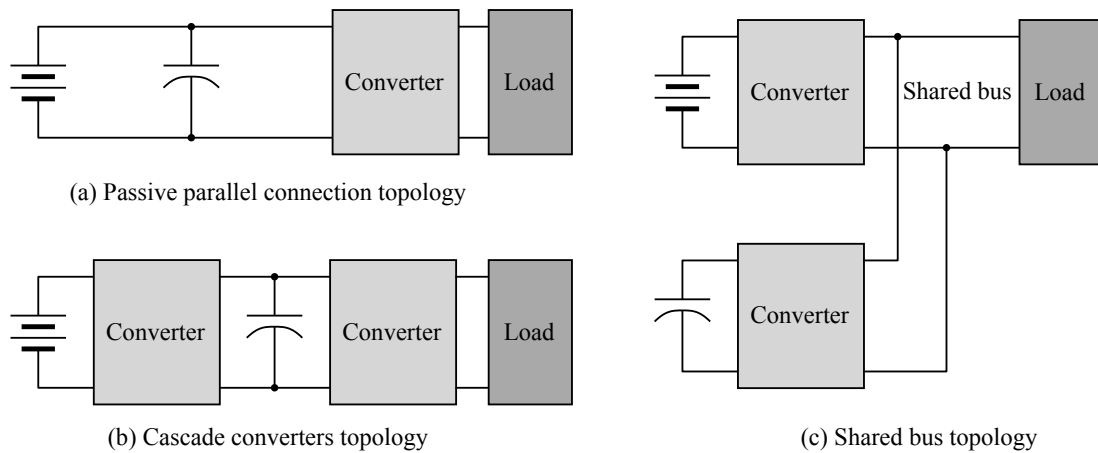
Figure 2.8: Battery-supercapacitor hybridization topologies.

the battery current increases [20].

However, the previous HEES systems cannot fully exploit the advantages of the HEES systems. The parallel connection and cascaded converter architectures have strict limitations on the type, number, and topology of the energy storage elements, and so lack of scalability and flexibility. In addition, the parallel connection architecture cannot fully utilize the energy capacity of the supercapacitor because its SoC-dependent voltage cannot deviate from the small battery terminal voltage variation. It does not allow independent current control of each energy storage element. The cascaded converter architecture is subject to a lower efficiency because the charging and discharging the battery must go through two conversion steps even if the current is low enough to be handled directly by the battery.

The previous HEES systems based on shared bus architecture are not optimized for energy efficiency as well. The energy control loops do not allow arbitrary current flow for each EES bank. Current distribution among the energy storage elements is determined by other storage element's voltage or current. Therefore, it is not possible to charge or discharge the each storage elements with the energy-optimal current considering rate capability, cycle

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efficiency, etc. Also, the energy control loop is for designed for a specific combination of HEES systems, and the control loop of each energy storage element is coupled with other energy storage element. The whole energy control loop is based on pre-characterization, and not scalable nor flexible. Furthermore, it is often neglected that the power converter is another significant contributor to the energy efficiency variation. Conversion efficiency in the shared bus architecture is not always maximum if the shared bus voltage is fixed, and this may result in sub-optimal energy efficiency. In short, the energy control loop of previous shared bus-based HEES systems does not consider the important factors related with the energy efficiency, such as rate capability, cycle efficiency, and power conversion efficiency. To the best of our knowledge, there is no prior work that presents a real implementation of an HEES system with a general architecture for scalability, flexibility, and energy-optimal control method. The HEES systems introduced in the previous literature are either based on an application-specific architecture or does not explicitly consider the energy efficiency for the system design.

2.3.2 Applications of HEES Systems

Fuzzy control method for battery-supercapacitor HEES system in micro-grid is introduced in [85]. More researches on the EV/HEV have adopted HEES system to improve energy efficiency of the EV/HEV [8, 12, 13, 14, 15, 10, 11]. A power control method proposed in [10] optimizes the supercapacitor current using neural network and achieves more than 20% of km/kWh improvement. A power control method introduced in [8] is for HEV with a shared bus, shown in Figure 2.8(c), composed of a fuel cell, battery, and supercapacitor. A simple passive parallel connection of battery and supercapacitor mitigates voltage ripple with limited volume and weight of the EV/HEV [11]. An optimization method in [86] solves the multi-objective optimization of minimizing energy loss and maximizing power
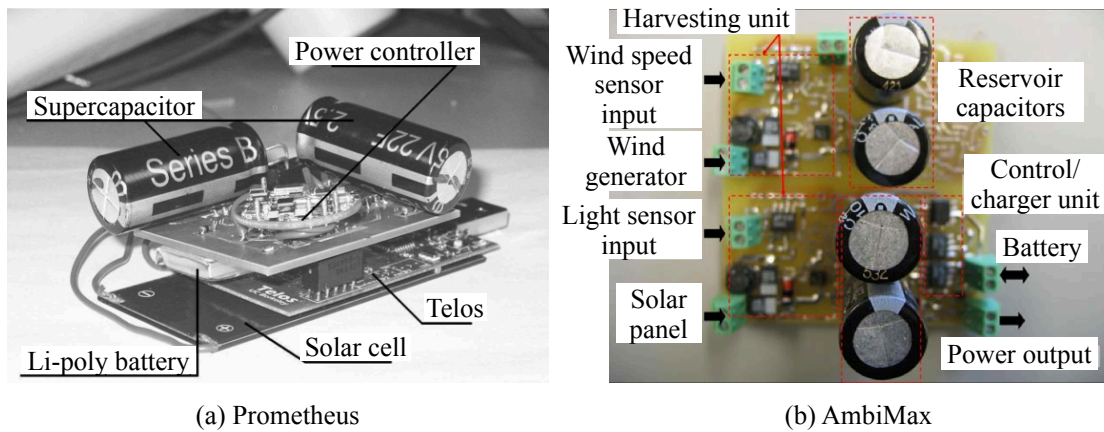
Figure 2.9: Battery-supercapacitor hybrid wireless sensor nodes. (a) Prometheus from UC Berkeley [89] and (b) AmbiMax from UC Irvine [90].

reserve) rated power reserve for HEV.

Some researches focus on the economic aspect of the HEES systems. Economic viability of using the HEES system for EV/HEV is analyzed in [87]. A genetic algorithm-based revenue maximization method for HEES systems used in energy and regulation markets is proposed in [88].

Low-power sensor nodes like [89, 90] employ a battery-supercapacitor hybrid as shown Figure 2.9. Due to very limited capability to produce power from energy harvesting devices such as solar cells, reducing power loss during charge/discharge cycles is important. They take advantages of the high cycle efficiency the supercapacitor while using the battery as a low-leakage long-term energy storage.

Recently, the HEES system has been attracting electronic design automation (EDA) society with its needs for systematical optimization [4, 17, 5, 91, 92]. For example, lifetime maximization for battery-supercapacitor HEES system is discussed in [17, 92] with systematic approaches utilized for the EDA problems. There more more examples of power
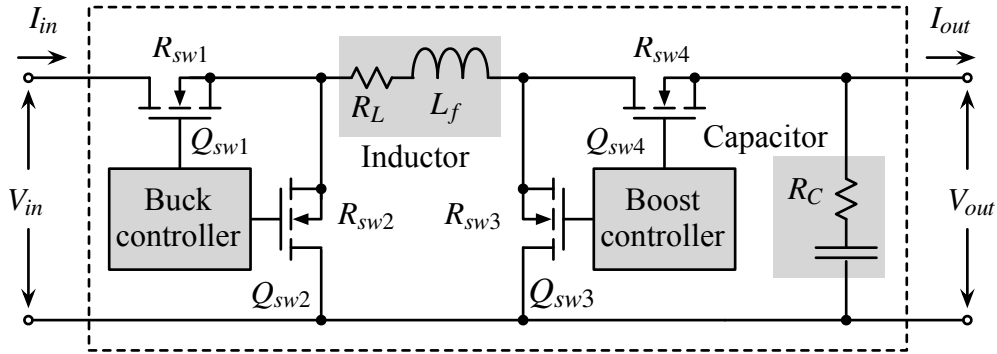
Figure 2.10: Buck-boost switching power converter model.

management of power sources and load devices when considering fuel cell-battery hybrid systems [93, 94, 95, 96, 97, 98, 99].

2.4 EES System Components Characteristics

2.4.1 Power Converter

A power converter is to deliver regulated voltage or current to the energy storage at a desired level regardless of variation in the input power source. The power converter is an essential component to resolve voltage or current mismatch between the input and output, and to provide controlled power delivery. A general schematic of a buck-boost switching power converter is shown in Figure 2.10. Depending on the relation between V_{in} and V_{out}, a power converter has two working modes: buck (step-down) mode and boost (step-up) mode. As the names imply, power converters operate in the buck mode if $V_{in} > V_{out}$, and otherwise in the boost mode.

An ideal power converter delivers the entire power from the source to the load without any loss, but the power conversion involves non-zero amount of power loss in practice. The

power converter efficiency η_c is defined as

$$\eta_c = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_c}{P_{in}} = \frac{V_{in} \cdot I_{in} - P_c}{V_{in} \cdot I_{in}}, \tag{2.1}$$

where P_{in} and P_{out} is input and output power of the power converter, respectively, and P_c is the power dissipation of the power converter. Therefore,

$$P_{out} = P_{in} - P_c = \eta_c \cdot P_{in}. \tag{2.2}$$

A pulse width modulation (PWM) switching power converter is a common type of switching power converter. The power loss of the PWM switching power converter consists of three components: conduction loss P_{cdct}, switching loss P_{sw} and controller loss P_{ctrl} [100]. That is,

$$P_c = P_{cdct} + P_{sw} + P_{ctrl}. \tag{2.3}$$

Those power loss components are strongly dependent on the input voltage V_{in}, output voltage V_{out}, output current I_{out}, and the circuit component properties.

In the buck mode, the power loss components is presented as

$$
\begin{aligned}
P_{cdct} =& I_{out}^2 \cdot (R_L + D \cdot R_{sw1} + (1 - D) \cdot R_{sw2} + R_{sw4}) \\
&+ \frac{(\Delta I)^2}{12} \cdot (R_L + D \cdot R_{sw1} + (1 - D) \cdot R_{sw2} + R_{sw4} + R_C), \\
P_{sw} =& V_{in} \cdot f_s \cdot (Q_{sw1} + Q_{sw2}), \\
P_{ctrl} =& V_{in} \cdot I_{ctrl}, \tag{2.4}
\end{aligned}
$$

where $D = \dfrac{V_{out}}{V_{in}}$ is the PWM duty ratio and $\Delta I = \dfrac{V_{out} \cdot (1 - D)}{L_f \cdot f_s}$ is the maximum current ripple; f_s is the switching frequency; I_{ctrl} is the current flowing into the controller; R_L and R_C are the equivalent series resistance (ESR) of inductor L and capacitor C, respectively; $R_{sw1,\dots,4}$ and $Q_{sw1,\dots,4}$ are the turn-on resistances and gate charges of the four switches in Figure 2.10, respectively.

In the boost mode, the power loss components is presented as

$$P_{cdct} = \left(\frac{I_{out}}{D}\right)^2 \cdot (R_L + (1-D) \cdot R_{sw3} + D \cdot R_{sw4} + R_{sw1} + D \cdot (1-D) \cdot R_C)$$
$$+ \frac{(\Delta I)^2}{12} \cdot (R_L + (1-D) \cdot R_{sw3} + D \cdot R_{sw4} + R_{sw1} + D \cdot R_C),$$

$$P_{sw} = V_{out} \cdot f_s \cdot (Q_{sw3} + Q_{sw4}),$$

$$P_{ctrl} = V_{in} \cdot I_{ctrl}, \tag{2.5}$$

where $D = \dfrac{V_{in}}{V_{out}}$ and $\Delta I = \dfrac{V_{in} \cdot (1-D)}{L_f \cdot f_s}$.

The gate width of the metal-oxide-semiconductor field-effect transistor (MOSFET) switches W_{sw} is the determining factor of R_{sw} and Q_{sw}. As W_{sw} gets smaller, R_{sw} increases and Q_{sw} decreases [101, 102]. More specifically,

$$R_{sw} = \frac{W_0}{W_{sw}} \cdot R_0, \tag{2.6}$$

$$Q_{sw} = \frac{W_{sw}}{W_0} \cdot Q_0, \tag{2.7}$$

where R_0 and Q_0 are the turn-on resistance and gate charge, respectively, of a MOSFET switch with a gate width of W_0.

Figure 2.11 shows the efficiency variation of the LTM4609 buck-boost converter from Linear Technology [103]. It shows a wide range of variation depending on V_{in}, V_{out}, and I_{out}. This wide variation may cause that the optimal operating point of the PV module does not match to the system-level optimal operating point.

2.4.2   Photovoltaic Cell

A PV cell converts light energy into electricity by the photovoltaic effect. This section briefly discusses the characteristics of the PV cell. It is the practice to compose PV modules with multiple, identical PV cells connected in series and/or parallel to obtain high
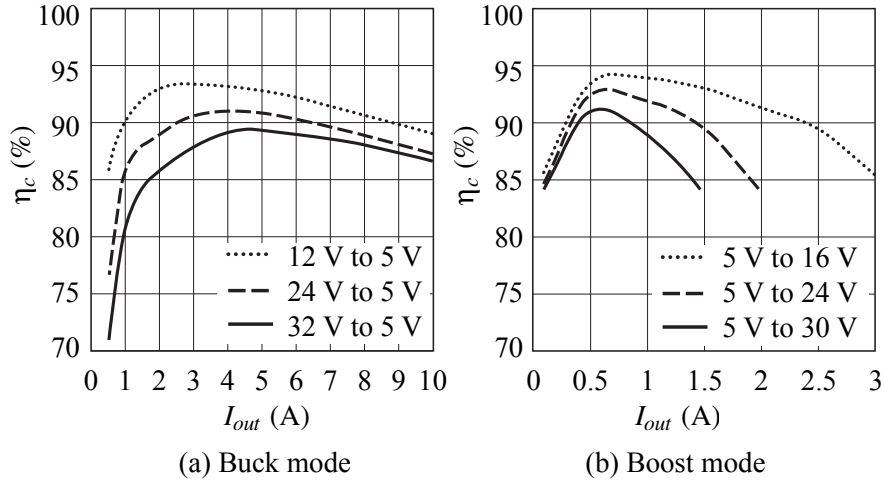
Figure 2.11: Power conversion efficiency of the Linear Technology LTM4609 buck-boost converter [103].

voltage and current level. The I-V characteristic of a PV module is heavily dependent on the solar irradiance level, and the maximum power point (MPP) also changes significantly. A typical equivalent circuit model of a PV module [104] is shown in Figure 2.12, with I-V characteristics given by:

$$I_{pv} = I_L - I_d - I_{sh} \tag{2.8}$$
$$= I_L(G) - I_0(T) \left(e^{(V_{pv} + I_{pv} \cdot R_s)(q/AnkT)} - 1 \right) - \frac{V_{pv} + I_{pv} \cdot R_s}{R_p},$$

where

$$I_L(G) = \frac{G}{G_{STC}} \cdot m \cdot I_{L,cell}(G_{STC}), \tag{2.9}$$

and

$$I_0(T) = m \cdot I_{0,cell}(T_{STC}) \left(\frac{T}{T_{STC}} \right)^3 e^{(qE_g/Ank)(1/T_{STC} - 1/T)}. \tag{2.10}$$

Here V_{pv} and I_{pv} are the voltage and current of the PV module, respectively. For the parameters, G is the irradiance level; T is the cell temperature; n and m are the number of
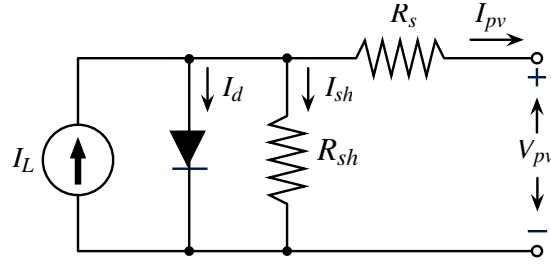
Figure 2.12: Equivalent circuit model of a PV module.

connected cells in series and parallel in the PV module, respectively; q is the charge of the electron; E_g is the energy bandgap and k is Boltzmann's constant. STC stands for standard test condition in which irradiance level is 1000 W/m^2 and temperature is 25 °C. The following five parameters determines the characteristics of the PV module.

- $I_{L,cell}(G_{STC})$: photo-generated current of a cell at standard test condition.

- $I_{0,cell}(T_{STC})$: dark saturation current of a cell at standard test condition.

- R_s: equivalent module series resistance.

- R_{sh}: equivalent module parallel (shunt) resistance.

- A: the diode ideality factor.

We use a method proposed in [105] to extract the above-mentioned five parameters from datasheet values in STC, which consist of the open circuit voltage V_{oc}, the short circuit current I_{sc}, voltage V_{mpp} and current I_{mpp} at the MPP, and temperature coefficients. Then a set of five parameters that determine V_{pv}–I_{pv} characteristic are derived from the measured G and T by (2.8), (2.9) and (2.10).

Figure 2.13 shows the variation of I_{pv} and P_{pv} by V_{pv} of a PV module with around 30 W power capacity at $G_{STC} = 1000$ W/m^2. It shows I_{pv}–V_{pv} curves and P_{pv}–V_{pv} curves at two different G of 500 W/m^2 and 1000 W/m^2. We see that the curves significantly change
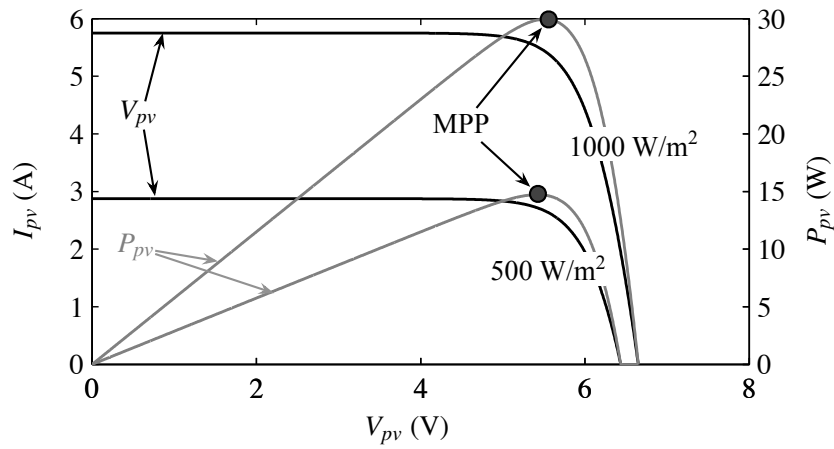
Figure 2.13: An example of I_{pv} and P_{pv} variation by V_{pv} when $G = 500$ W/m^2 and $G = 1000$ W/m^2.

depending on the solar irradiance levels. The MPPT methods adjust the operating point, which is defined as a pair of (V_{pv}, I_{pv}), to (V_{mpp}, I_{mpp}) against dynamically varying irradiance. Also, we see that both V_{pv} and P_{pv} change in a wide range depending on I_{pv} even with the same irradiance level.

Chapter 3

Hybrid Electrical Energy Storage Systems

3.1 Design Considerations of HEES Systems

Desirable performance metrics of the HEES systems naturally includes the general metrics as an energy storage such as energy density, power density, cycle efficiency, cycle life, cost, leakage, and other non-linear characteristics (rate capability, environmental effect, etc.) Improvement of these factors by hybridization in the HEES systems is heavily dependent on the energy efficiency. Every operation in the HEES systems, such as charging the EES element from power sources, discharging the EES element to supply power, transferring energy internally, and so on, affects the energy efficiency.

From the system-level point of view, we also emphasize the following aspects for designing and implementing the HEES system.

- Scalability: The proposed HEES system architecture is able to accommodate increased number of EES banks.

- Modularity: It is easy to remove or add EES banks from or to the HEES system, and change individual EES bank without significant modification to the system.

- Versatility: The proposed HEES system can adopt various types of EES elements, power sources, and load devices.

- Stability: The proposed HEES system stably responds to the rapid load demand variation.

These metrics are often neglected in conventional EES system design because the homogeneity makes the architecture design and control easy. However, they should not be overlooked when designing and implementing HEES systems, which adopt a sophisticated architecture and involve complicated system-level controls. We consider the these metrics when we discuss the proposed architectures and control schemes throughout this dissertation.

3.2   HEES System Architecture

We achieve the scalability, flexibility, and energy-optimality in the proposed HEES system by a general architecture and an energy-optimal control method and exploits all the benefits of HEES systems. Figure 3.1 show the proposed architecture of HEES system. The proposed HEES system is composed of multiple heterogeneous EES banks. Each EES bank consists of an EES array and a bidirectional charger that can charge and discharge the EES array. It also has unidirectional power converters to accommodate various kinds of alternating current (AC) or direct current (DC) power sources and load devices.

The CTI is an interconnection network for charge transfers among EES nodes such as EES banks, power sources, and load devices. The CTI connects the power converters of the EES banks, power sources, and load devices. We do not limit the topology of the CTI to a

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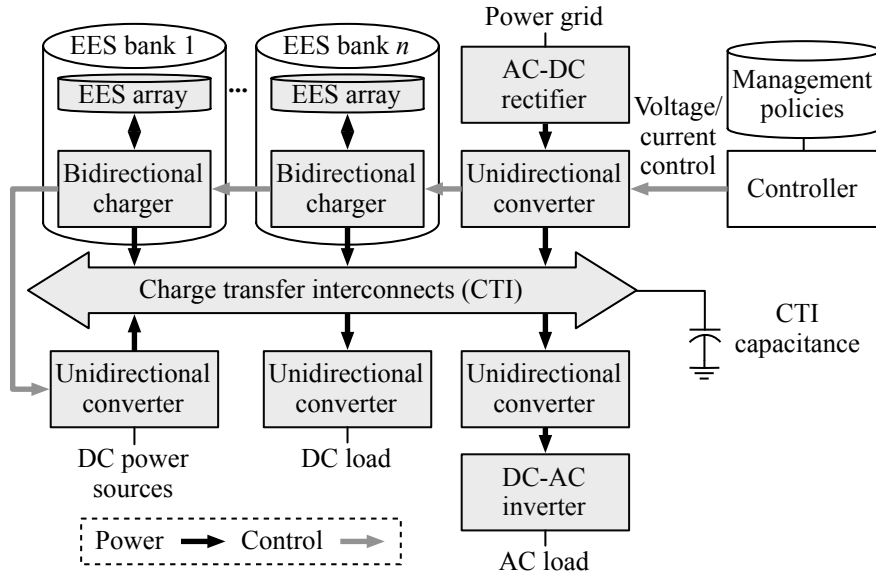
Figure 3.1: Architecture of the proposed HEES system.

single shared bus, which is similar to the shared bus architecture in Figure 2.8(c). The CTI can be multiple buses, segmented buses, mesh interconnect, crossbar interconnect, or any combinations of those.

We do not make a physical hierarchy among the EES banks. Of course, the charge management policies exploit range of logical hierarchy among EES banks. The primary reason that we have a physically flat architecture is to reduce energy loss involved in every charge and discharge operation between EES banks. This is different from computer memory hierarchy management where there is no data loss during data movement in the hierarchy. The physically flat architecture of the proposed HEES is more similar to a scratchpad memory rather than a cache memory [106].

The controller performs a high-level system control and management for reliable and energy-efficient operations. The controller is in charge of determining the CTI voltage and current of each EES banks and power sources based on the load current and EES bank

status such as SoC and SoH. While the controller makes such high-level decisions with a software control loop, the power converters maintain CTI voltage and input/output current determined by the controller with a hardware feedback control loop. The outer control loop continuously updates the set points to maximize the system efficiency by the use of high-level management policies. We are able to maintain a reasonable set point update frequency free from CTI stability control thanks to the cascaded feedback loops, which allows us to use standard microcontroller for the outer feedback loop.

3.3   Charge Transfer and Charge Management

The benefits of the HEES systems over the conventional EES systems rely on sophisticated charge management. Charge management is optimizing the charge transfer among the EES nodes. It includes determining the optimal time and amount of charge transfers to each EES nodes and finding the optimal operating conditions of the charge transfers. Compared with the homogeneous EES systems where the charge and discharge can be distributed uniformly across the all the homogeneous cells, charge management in the HEES systems is not trivial.

We proposed charge management policies to manage the energy flow recently. We need to select particular EES banks to charge or discharge among multiple possible selections and determine the CTI voltage and amount of current that maximize the energy efficiency. Also, we may need to internally move energy from one EES bank to another in order to mitigate self-discharge or to prepare for expected demand for energy/power capacity. Our charge management policies include i) charge allocation for charging EES banks [107], ii) charge replacement for discharging EES banks [108], and iii) charge migration for moving energy between EES banks [109, 110]. We consider the characteristics of the EES elements,

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power converter efficiency, input or output power variations, and time constraint, and find the EES banks and amount of current that achieves the energy-optimal charge transfers.

The charge management is resemble to memory management in a computer system. The charge allocation, replacement, and migration operations are similar to the cache allocation, replacement, and migration operations. The cache writing policy and victim selection policy affects the performance such as access latency, cache miss rate, and so on. In both charge management and memory management, finding a good allocation/replacement target and reducing unnecessary migration are key objectives to maximize the system performance.

Once the sources and destinations of the charge transfers are determined by the charge management policies, charge transfer scheduling follows. The charge transfer scheduling is determining duration of the CTI occupation of each charge transfer. This is similar to the task scheduling in a computer system that determines the computational resource occupation of the tasks. It derives the charge current that determines the time duration required to finish the charge transfer. The charge transfer current and time should be determined carefully not only to maximize the efficiency of a single charge transfer, but considering efficiency of other charge transfers. Table 3.1 summaries comparison between the charge transfer scheduling and task scheduling.

Table 3.1: Comparison of charge transfer scheduling and task scheduling.

	Charge transfer scheduling	Task scheduling
Resource	CTI links	Computing resources (e.g., CPU)
Task properties	Each charge transfer has an arrival time, deadline, and amount of charge transfer	Each task has an arrival time, deadline, and workload
Objectives	Maximizing the energy efficiency of charge transfers, EES element lifespan, etc.	Reducing total wall time of computation, power consumption, temperature, etc.
Scheduling parameters	Charge transfer current (charge transfer time)	Dynamic voltage/frequency scaling (computation time)

3.4 HEES System Components

3.4.1 Nodes

3.4.1.1 Energy Storage Banks

We apply the hybrid concept in bank level. Each bank consists of homogeneous EES elements. All the EES bank should meet standard interface specifications though the inside EES element array is heterogeneous. The standard specification is defined at the bank terminal such as terminal voltage range and the communication network protocol. The maximum charging and discharging current is generally different by EES bank to exploit the hybrid concept. The mandatory component in an EES bank includes a homogeneous EES element array, a bidirectional charger and a communication network.

The EES array is a set of multiple identical EES elements that are connected in series and/or parallel forming an $n \times m$ regular matrix, where n is the number of series connections and m is the number of parallel connections. The dimension of the EES element array is determined by the power and energy capacity, and the maximum voltage rating of the EES bank. We consider the regular array structure only so that we maintain the same SoC and SoH of all the elements in the array. We may also consider reconfigurable architecture of the EES array [111], but we do not consider the reconfiguration for the prototype implementation because the dimension of the EES array is not large enough for reconfiguration. Figure 3.2 shows an HEES bank architecture with a 3×3 array for an illustration purpose.

The charger regulates the current to and from the EES bank array and CTI. The bidirectional charger can also be set to a DC–DC converter when the direction is from the EES bank array to CTI. This allows easy CTI voltage control. The bidirectional charger is connected to the main controller through a communication network. When the power is
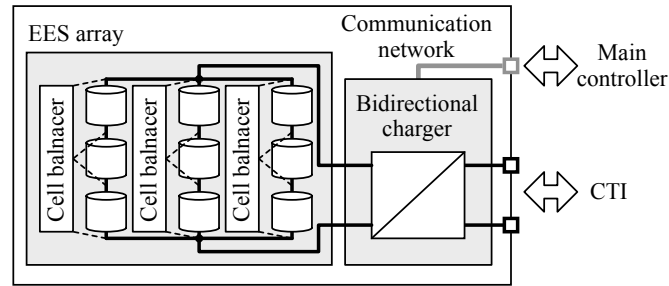
Figure 3.2: EES bank with a 3×3 EES array and charger.

on, the main controller identifies the bank characteristics such as the type of EES bank, the maximum charging/discharging current, the current SoC, the current SoH, the EES element array terminal voltage, temperature of the cells, etc. The main controller continues monitoring the current SoC, the EES element array terminal voltage, temperature of the cells, etc.

We optionally use cell balancers when the EES elements require external cell balancing. Even though all the EES elements are of the same type, manufacturing variation in practice may result in imbalance of characteristics such as capacity and internal resistance that causes imbalanced SoC during operation and even damage to the elements [112]. Supercapacitors and lithium-ion batteries require external cell balancing while lead-acid batteries may work without external cell balancing for example.

3.4.1.2 Power Sources and Load Devices

The power converters should be designed considering the power input and output requirements. The grid-connected HEES system receives AC power from the power grid and supply AC power to the load devices. Batteries and supercapacitors are DC energy storages. Therefore, AC–DC rectifier is required to perform AC-to-DC conversion for charging the EES bank from the power grid, and DC–AC inverter is required to perform DC-to-AC con-

version for discharging the EES bank to the load devices. These power converters for the power sources and load devices do not need to be bidirectional. They are connected to the CTI whose voltage is dynamically varying, and so they should be able to adapt to the voltage variation.

DC power sources such as fuel cells and solar cells require DC–DC conversion from the power sources to the CTI, and DC load devices such as portable appliances also require DC–DC conversion from the CTI to the load devices. Similar to the AC power converters, the DC–DC converters for the DC power sources and DC load devices are unidirectional, and they also need to be able to adapt to the CTI voltage variation.

3.4.2 Charge Transfer Interconnect

Similar to on-chip communication networks, the network topology of the CTI is one of the important design considerations for scalability and energy efficiency. The CTI architecture should be carefully determined for given type and number of EES banks. The parallel connection (Figures 2.8(a)) and cascaded architecture (Figures 2.8(b)) are not suitable for three or more EES banks. The shared bus architecture (Figures 2.8(c)) provides higher scalability. The energy efficiency of the charge transfers is significantly affected by the CTI voltage level because the CTI is the input or output port of the power converters of each charger and the power converter efficiency is dependent on the input/output voltage and output current. Each charge transfer has its own optimal CTI voltage level that maximizes the energy efficiency [107, 108, 109, 110]. Therefore, the CTI voltage needs to be dynamically adjustable.

As the number of EES banks increases, more number of simultaneous charge transfers take places among the EES banks. Higher energy efficiency may be achieved if the CTI network is able to provide more isolated paths to the simultaneous charge transfers for

the energy-optimal CTI voltage. The shared-bus architecture is the simplest design which is appropriate to accommodate a small number of EES nodes where there are not many simultaneous charge transfers. All the simultaneous charge transfers share the single CTI voltage level which may be energy-inefficient, but the single share bus offers easy implementation. We proposed more scalable architectures such as a mesh grid architecture [113] and multiple-bus architecture [114] for more number of EES banks. The mesh grid architecture uses routers like a communication network to dynamically reconfigure the CTI between the EES banks [113]. The routing algorithm merges charge transfers to increase routability and find the optimal CTI voltage to maximize the energy efficiency. EES banks in the multiple-bus architecture can be connected any of the multiple buses [114]. The charge transfers are merged into the same number of sets as the number of busses and each charge transfer set is assigned to one bus. Those architectures allow multiple simultaneous charge transfers at the energy-optimal CTI voltages levels, and therefore enhance the energy efficiency.

3.4.3   System Control and Communication Network

The HEES systems require sophisticated management policies than conventional EES systems do because of the heterogeneity of EES elements. Using multiple different EES elements doe not guarantee improved energy efficiency. Proper management policies are crucial for the HEES system to achieve energy efficiency improvement. It is mandatory to devices system-level policies in order for maximizing the benefits of the HEES system in energy efficiency, lifetime, etc, by exploiting its heterogeneity, which have been not considered for the conventional homogeneous EES systems.

In addition to the charge management policies introduced in Section 3.3, we proposed more HEES system optimization and management schemes that requires system-level controls. We also proposed bank reconfiguration to change the connection of EES elements

within an EES bank to adjust to the optimal terminal voltage considering the CTI voltage and the power converter efficiency [111]. We also introduced a management scheme to enhance the SoH of batteries using supercapacitors for high frequency power detected by applying a crossover filter to the power profile [115].

These sophisticated management schemes require a high-level controller, rather than a simple feedback control loop. For example, the current from each EES bank is directly determined by the voltage or current of another EES bank [8, 84, 20] or speed of the EV [10]. However, taking non-linear and time-varying characteristics such as rate capability and cycle life into account requires a more elaborate control system. Also, the control system involves a considerable amount of control data transfer through a communication network for collecting information from many EES banks, power sources, and load devices and sending commands to them. High speed communication network is required to enable the high-speed control. In addition, scalability issue arises in the communication network like in the CTI architecture to accommodate increased number of EES banks. Therefore, the communication network should be designed considering the high-speed and scalability requirements.

Chapter 4

System Level Design Optimization

4.1 Reconfigurable Storage Element Array

Memory hierarchy and organization has a significant impact on the computer system performance and power consumption. Objectives of memory system design include reducing access time, power consumption, cache miss rate, and so on. However, a memory design optimized for one application may not be optimal for all applications. Therefore, it is beneficial to adaptively change the organization of the memory design dynamically depending on the access pattern of the currently running applications [116, 117]. This is called memory reconfiguration.

A similar problem exists in the HEES system. One configuration of an EES bank may not be optimal always depending on the current cell voltage, CTI voltage, and amount of current. Therefore, we introduce EES bank reconfiguration that adaptively changes the series and parallel connection of the EES array. It aims to maximize the energy efficiency by reducing power loss in the power converter and EES element and maximize capacity utilization. This comparison is summarized in Table 4.1

Table 4.1: Comparison of EES bank reconfiguration and memory reconfiguration.

	EES bank reconfiguration	Memory reconfiguration
Configurable parameters	Series and parallel connections	Memory size, (DRAM) rank size, (cache) associativity
Dependency	Cell voltage, CTI voltage, amount of current	Applications access pattern (e.g., cache hit/miss rates)
Objectives	Reducing power loss in power converter and EES elements	Reducing access time, power consumption, (cache) miss rate

4.1.1 Cycle Efficiency and Capacity Utilization of EES Bank

Cost factors of HEES systems fall into two categories: operational cost and capital cost [4]. The operational cost is mainly the electricity cost, and thus it is directly related to the efficient use of energy. The capital cost includes expenses for purchasing and disposal of the EES elements, and therefore fully utilizing the EES bank capacity is a key for reducing the capital cost. Cycle efficiency and capacity utilization of EES banks are the major factors that motivate dynamic reconfiguration of EES banks for reducing the operational cost and capital cost of HEES systems.

The cycle efficiency is 'round-trip' energy efficiency generally defined as $\eta_{cyc} = \dfrac{E_{out}}{E_{in}}$ where E_{in} and E_{out} denote energy input and energy output, respectively. The cycle efficiency of supercapacitors is close to 100%, which means that almost all the energy consumed to charge a supercapacitor can be retrieved in the following discharging process. On the other hand, the cycle efficiency of batteries ranges 60–90% depending on the chemistry used for

the electrodes even under the optimal charge and discharge condition.

The cycle efficiency generally has been considered as a natural characteristics of an EES element [34]. However, the cycle efficiency is closely related to the charge and discharge rates, i.e., the magnitude of charge and discharge current with respect to the rated capacity of the storage element. The rate capacity effect of batteries results a low cycle efficiency for a high-current charge and discharge. In practice, from the system-level point of view, one should not disregard the power conversion process and its power loss when considering the cycle efficiency of an EES bank. In fact, the cycle efficiency is significantly affected by the power conversion efficiency, which is also a function of the charge and discharge rates as discussed in Section 2.4.1.

Therefore, it is beneficial to define constant-power charging efficiency η_c and constant-power discharging efficiency η_d for the cases that a storage element is charged and discharged at a constant CTI power and a constant CTI voltage:

$$\eta_c(P_{cti,c}, V_{cti}) = \frac{\max(E_{bank})}{P_{cti,c} \cdot t_c(P_{cti,c}, V_{cti})}, \tag{4.1}$$

$$\eta_d(P_{cti,d}, V_{cti}) = \frac{P_{cti,d} \cdot t_d(P_{cti,d}, V_{cti})}{\max(E_{bank})}, \tag{4.2}$$

where $t_c(P_{cti,c}, V_{cti})$ is the charging time, $t_d(P_{cti,d}, V_{cti})$ is the discharging time, $P_{cti,c}$ is the CTI power when charging, $P_{cti,d}$ is the CTI power when discharging, and V_{cti} is the CTI voltage. As a result, the *constant-power cycle efficiency* η_{cyc} when $P_{cti,c} = P_{cti,d} = P_{cti,cyc}$ is defined as

$$\eta_{cyc}(P_{cti,cyc}, V_{cti}) = \eta_c(P_{cti,cyc}, V_{cti}) \cdot \eta_d(P_{cti,cyc}, V_{cti}). \tag{4.3}$$

We define capacity utilization as one of the important performance metrics of an EES bank. A bank voltage cannot be arbitrarily low because the power converter cannot operate below a certain voltage [118], which we define as $V_{bank,min}$. The capacity utilization ρ is defined as the ratio between the usable energy capacity and the original energy capacity

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of the EES bank. The capacity utilization is equivalent to the ratio between the extracted energy and the stored energy in a fully charged bank. That is,

$$\rho = 1 - \frac{E_{bank,remain}}{E_{bank,lim}}, \tag{4.4}$$

where

$$E_{bank,remain} = \frac{1}{2} \cdot C_{bank} \cdot V_{bank,min}^{2} \tag{4.5}$$

is the remaining energy when the power converter can no longer extract energy, i.e., loss in the capacity. The capacity utilization of storage elements is smaller than 100% because the power converter requires the minimum bank voltage, $V_{bank,min}$, which is higher than 0 V.

Figure 4.1 illustrates the effect of the cycle efficiency and capacity utilization. The operational cost of HEES systems is affected mainly by the cycle efficiency. If the cycle efficiency is poor, we have to expense more for storing and retrieving the same amount of energy. As shown in Figure 4.1, the very first cycle requires additional energy of $E_{bank,remain}$ to increase the bank voltage from 0 V to $V_{bank,min}$. The operational cost for this additional energy is dependent on the capacity utilization, but this effect may be neglected for repeated cycles in long term. The capital cost is affected by the effective energy capacity of the EES banks. If the capacity utilization is 80%, we lose 20% of the expenses for the storage elements because this portion does not contribute to the energy capacity.

4.1.2 General Bank Reconfiguration Architecture

We introduce the *general balanced reconfiguration architecture (GBRA)* for the EES bank reconfiguration [111]. We define a balanced reconfiguration to satisfy the condition whereby all energy storage cells in a given EES bank have identical SoC and terminal voltages at all times i.e., they are balanced at all times, given that the cells are healthy and identical.

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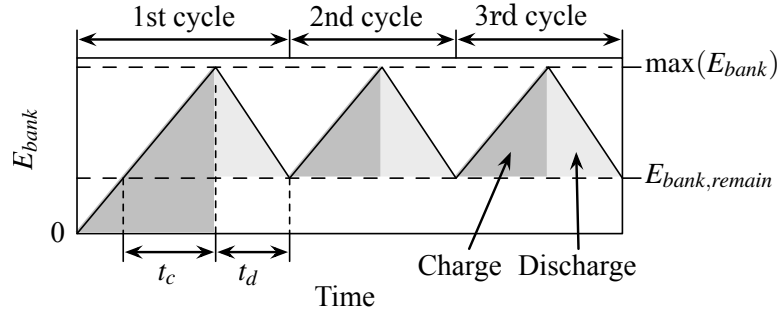
Figure 4.1: Cycle efficiency and capacity utilization in repeated charge-discharge cycles.

Unless active charge balancing circuits are used (which is not the case here), cell balancing can be achieved by regular arrangement of cells. We call such arrangements balanced configurations. The proposed architecture is 'general' in the sense that it can produce every balanced configuration that is possible with a given number of cells.

Let N denote the number of available cells. The N cells can be organized in various balanced configurations and the number of possible configurations equals the number of bi-factor decompositions of the natural number N (including $1 \times N$ and $N \times 1$.) We define a configuration $C(n,m)$ to be a configuration that has n cells in series and m cells in parallel. For example, the number of balanced configurations of a 10-cell bank (N is 10) is four: $C(1,10)$, $C(2,5)$, $C(5,2)$, and $C(10,1)$. Although $C(3,3)$, which is composed of nine cells, is also possible with 10 cells, we do not consider such a case as a balanced configuration because it leaves one cell imbalanced.

Figure 4.2 shows the proposed GBRA of a bank composed of N cells. Each of $N-1$ cells has three switches: one series switch (S-switch) and two parallel switches (P-switches) except for the last one. The P-switches connect cells in parallel into n-parallel sub-banks, whereas the S-switches connect those m sub-banks in series. A sub-bank is a set of cells connected only in parallel. For the i-th cell, its S-switch is denoted by $S_{S,i}$, while its two

55
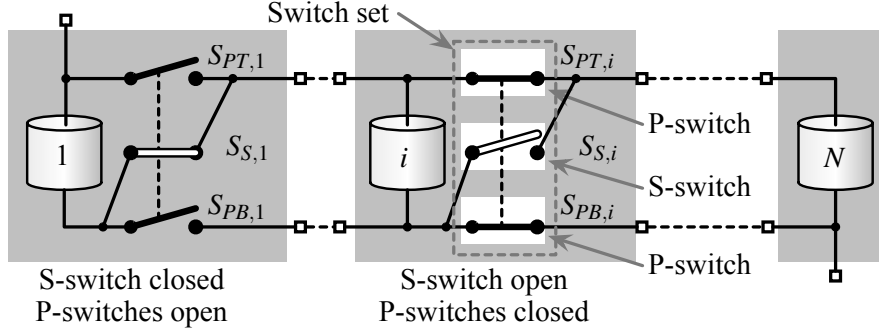
Figure 4.2: GBRA of an N-cell EES bank.

P-switches are denoted by $S_{PT,i}$ and $S_{PB,i}$, one on the top and the other in the bottom, respectively. We group the three switches of one cell as a switch set, which gives rise $N-1$ switch sets in the bank. For each cell, $S_{PT,i}$ and $S_{PB,i}$ are closed exactly if $S_{S,i}$ is open. There are no cases where one of $S_{PT,i}$ and $S_{PB,i}$ switches is open while the other is closed.

More formally, for $i = 1, 2, \ldots, N-1$,

$$x_{P,i} + x_{S,i} = 1, \tag{4.6}$$

where

$$x_{S,i} = \begin{cases} 0 & \text{if } S_{S,i} \text{ is open,} \\ 1 & \text{if } S_{S,i} \text{ is closed,} \end{cases} \tag{4.7}$$

$$x_{P,i} = \begin{cases} 0 & \text{if } S_{PT,i} \text{ and } S_{PB,i} \text{ are open,} \\ 1 & \text{if } S_{PT,i} \text{ and } S_{PB,i} \text{ are closed.} \end{cases} \tag{4.8}$$

Otherwise, the bank malfunctions; more precisely, the i-th cell is disconnected from the $(i+1)$-th cell if $x_{S,i} = x_{P,i} = 0$, or the i-th supercapacitor is short-circuited if $x_{S,i} = x_{P,1} = 1$.

A balanced configuration of GBRA is obtained by switching operations which obeys

the following rule; in the m-by-n balanced configuration $C(n,m)$,

$$
x_{S,i} = \begin{cases} 1 & \text{if } i = n \cdot k \text{ where } k = 1, 2, \ldots, m-1, \\ 0 & \text{otherwise,} \end{cases}
\tag{4.9}
$$

$$
x_{P,i} = 1 - x_{S,i}.
\tag{4.10}
$$

The total capacitance C_{bank}, voltage V_{bank}, internal resistance R_{bank}, and energy storage capacity E_{bank} of a bank of $C(n,m)$ are calculated as follows:

$$
C_{bank} = \frac{n}{m} \cdot C_{cell} = \frac{N}{m^2} \cdot C_{cell},
\tag{4.11}
$$

$$
V_{bank} = m \cdot V_{cell},
\tag{4.12}
$$

$$
E_{bank} = \frac{1}{2} \cdot C_{bank} \cdot V_{bank}^2 = N \cdot E_{cell},
\tag{4.13}
$$

$$
R_{bank} = \left(\frac{2}{3} \cdot n - 1 + \frac{1}{3 \cdot n} \right) \cdot m \cdot R_p + \frac{m}{n} \cdot R_c + (m-1) \cdot R_s,
\tag{4.14}
$$

where C_{cell}, V_{cell}, and E_{cell} denote the capacitance, voltage, and energy capacity of each cell, respectively; R_s and R_p denote the on-resistance of an S-switch and a P-switch, respectively; and R_c denotes the ESR of each cell. We assume that the charge or discharge current is equally distributed to every cell in a sub-bank when we derive (4.14). For a fixed N, the bank total capacitance C_{bank} is inversely proportional to m^2 whereas the bank terminal voltage V_{bank} is proportional to m. The total energy remains the same regardless of the configuration.

Each cell has its voltage limit $V_{cell,lim}$ that should not be exceeded, and corresponding energy capacity limit $E_{cell,lim}$. The voltage limit $V_{bank,lim}$ and energy capacity limit $E_{bank,lim}$ of a bank are defined similar to (4.12) and (4.13):

$$
V_{bank,lim} = m \cdot V_{cell,lim},
\tag{4.15}
$$

$$
E_{bank,lim} = N \cdot E_{cell,lim}.
\tag{4.16}
$$

$\mathcal{C}(4,1)$	$\mathcal{C}(2,2)$	$\mathcal{C}(1,4)$
$C_{bank} = (1/4) \cdot C_{cell}$	$C_{bank} = C_{cell}$	$C_{bank} = 4 \cdot C_{cell}$
$V_{bank} = 4 \cdot V_{cell}$	$V_{bank} = 2 \cdot V_{cell}$	$V_{bank} = V_{cell}$
$E_{bank} = 4 \cdot E_{cell}$	$E_{bank} = 4 \cdot E_{cell}$	$E_{bank} = 4 \cdot E_{cell}$
$R_{bank} = 4 \cdot R_c + 3 \cdot R_s$	$R_{bank} = R_p + R_c + R_s$	$R_{bank} = \frac{7}{4} \cdot R_p + \frac{1}{4} \cdot R_c$
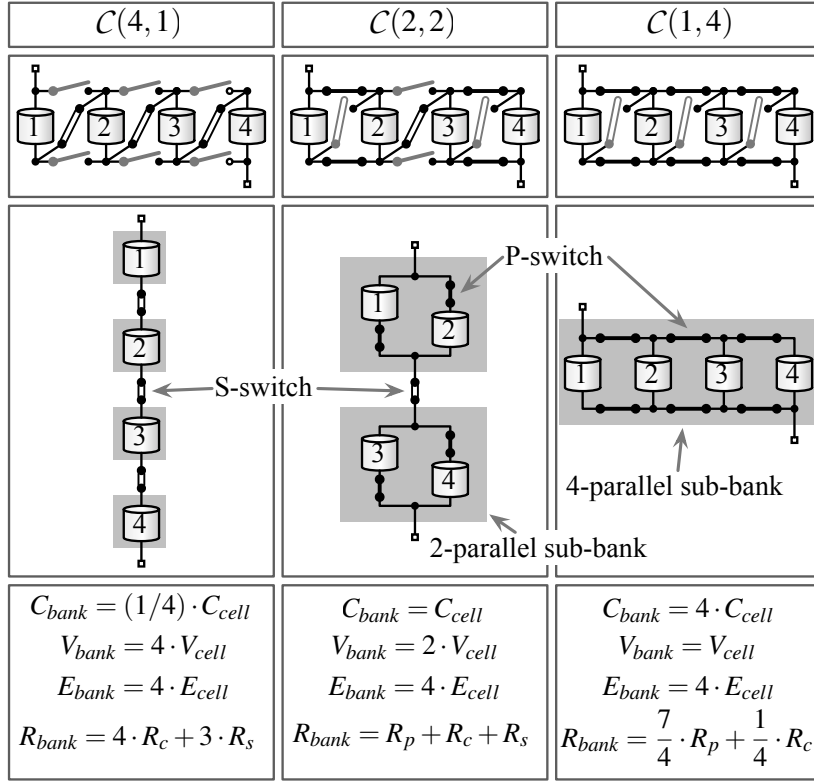
Figure 4.3: Reconfiguration examples of a four-cell EES bank ($N = 4$).

Figure 4.3 is an example of reconfiguration of a four-cell bank ($N = 4$) with the GBRA. With four cells, three balanced configurations are possible. One of them, for example, is $\mathcal{C}(2,2)$ which consists of two sub-banks connected in parallel with P-switches, and each sub-bank composed of two cells connected in series with S-switches.

Figure 4.4 shows the switch operations for each configuration when $N = 60$. Each row represents the configuration $\mathcal{C}(n,n)$, and each square represents which of the S-switch and P-switches are closed in the configuration. One can notice from the figure that each switch set has a different probability for closing the S-switch or P-switches. For example, $S_{S,30}$ is more likely to be closed than other S-switches in many configurations. On the other hand, switch sets that are annotated with dotted boxes always close P-switches except only for
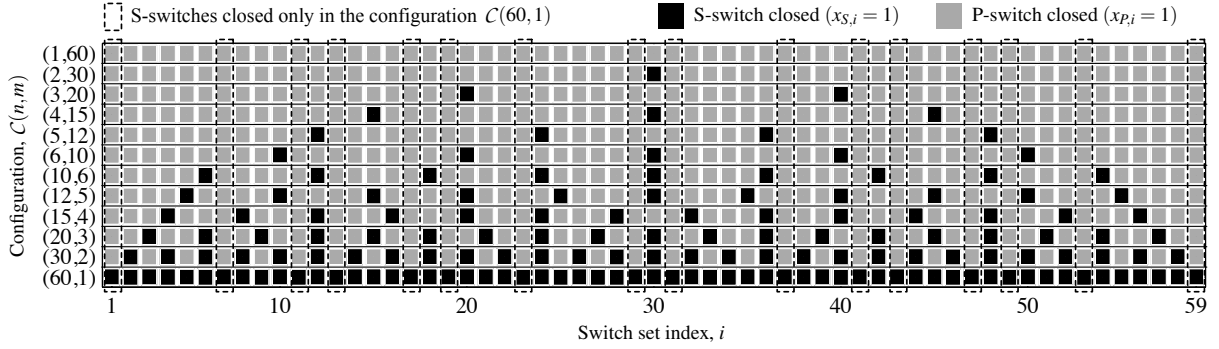
Figure 4.4: Operations of S-switches and P-switches of a 60-cell bank in different configurations.

one configuration $C(60,1)$. To generalize, $x_{S,i} = 1$ in $C(n,m)$ exactly if m is a common divisor of i and N, otherwise, $x_{P,i} = 1$ as shown in (4.9).

This observation provides the intuition for an optimization method to reduce the number of switches. A switch set can be removed if the switches in the set do not change their states, i.e., they remain always open or always closed. An always-open switch may be removed from the circuit, while an always-closed switch may be replaced by a wire. Eliminating unnecessary switch sets not only reduces the overall switch implementation cost, but also reduces the bank internal resistance and in turn, lowers the IR loss.

We can reduce the number of switches by restricting possible configurations. More precisely, $S_{S,i}$ may be short-circuited, and $S_{PT,i}$ and $S_{PB,i}$ may be open if we use only configurations where n and i are coprime. Conversely, $S_{S,i}$ may be open, and $S_{PT,i}$ and $S_{PB,i}$ may be short-circuited if we never use configurations where n and i are coprime. In the previous example, out of the 59 switch sets, 16 switch sets that are annotated with the dotted boxes can be removed if $C(60,1)$ is not used. However, we do not consider configuration selection, and assume all the configurations are possible with all the switch sets present.

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4.1.3 Dynamic Reconfiguration Algorithm

4.1.3.1 Cycle Efficiency

The primary objective of the dynamic EES bank reconfiguration is reducing energy loss by improving the power conversion efficiency. As discussed in Section 2.4.1, the power conversion efficiency of power converters depends on the input and output voltage and current values, that is V_{bank}, V_{cti}, I_{bank}, and I_{cti}. The purpose of dynamic EES bank reconfiguration is to maximize conversion efficiency η_{conv} by controlling V_{bank} at run time for given V_{cti} and I_{cti}. Meanwhile, the bank voltage should be within a range of $[V_{bank,min}, V_{bank,max}]$ as the power converter requires.

- Given: Number of cells N, CTI voltage V_{cti}, CTI current I_{cti}, and cell voltage V_{cell}.

- Find: Configuration $C(n, m)$ that minimizes the power loss of the EES bank.

- Subject to: Bank voltage limitation: $V_{bank,min} \leq V_{bank} \leq V_{bank,max}$.

The power loss of the EES bank has two components: power conversion loss which is discussed in Section 2.4.1, and IR loss induced by the internal resistance of the EES bank. Minimizing the power converter loss has different implications for charging and discharging: i) for charging, it means maximizing energy transferred from the CTI to the bank, and ii) for discharging, it means maximizing energy transferred from the bank to the CTI.

The dynamic reconfiguration is expressed as a mapping function

$$f : (V_{cti}, I_{cti}, V_{cell}) \rightarrow C(n, m), \tag{4.17}$$

where $V_{cti,min} \leq V_{cti} \leq V_{cti,max}$, $I_{cti,min} \leq I_{cti} \leq I_{cti,max}$, $0 \leq V_{cell} \leq V_{cell,lim}$, $n \in \hat{N}$, and $m = N/n$. Here, $[V_{cti,min}, V_{cti,max}]$ and $[I_{cti,min}, I_{cti,max}]$ denote the operational range of V_{cti} and I_{cti}, respectively, and $\hat{N}$ is a list of possible values of n in an ascending order. We can see that

exhaustive online search for the optimal *n* and *m* among numerous configurations is not practical. Therefore, we propose a two-phase reconfiguration method, which consists of an offline phase and an online phase. In the offline phase, we analyze the power converter efficiency η_{conv} and develop a function $f_{offline}$ to find the optimal bank voltage $V_{bank,opt}$ for given V_{cti} and I_{cti}. Next, in the online phase, we use a function f_{online} to find the optimal configuration $C(n,m)$ that minimized the power loss for given V_{cell}. That is,

$$f_{offline} : (V_{cti}, I_{cti}) \rightarrow V_{bank,opt}, \tag{4.18}$$

$$f_{online} : (V_{cti}, I_{cti}, V_{bank,opt}, V_{cell}) \rightarrow C(n,m). \tag{4.19}$$

It is not feasible to analytically find the optimal operating conditions that maximizes the power conversion efficiency η_{conv}. Therefore, it is reasonable to implement the offline function $f_{offline}$ as a lookup table since it is only two-dimensional and both of V_{cti} and I_{cti} have a limited range in practice because of the minimum and maximum ratings of peripheral circuitry. We build the lookup table by evaluating the conversion efficiency and finding the optimal condition. The lookup table is indexed with V_{cti} and I_{cti}, where each entry is the optimal bank voltage $V_{bank,opt}$ that maximizes η_{conv} for given V_{cti} and I_{cti}. Two lookup tables are built for charging and discharging in the same manner. The online algorithm can exploit these lookup tables and easily obtain $V_{bank,opt}$ at run time which greatly reduces the computation overhead.

The online function f_{online} is described in Algorithm 1. First, the optimal bank voltage is derived from $f_{offline}$ mapping function for current V_{cti} and I_{cti} (List 1). Since the lookup table is defined for discrete intervals, a two-dimensional interpolation may be used for intermediate values. Next, the ideal series-connection number n_{ideal} is derived (List 2). We redefine a possible set of configurations M' for the given condition, by excluding configurations that are not allowed due to bank voltage limitation (List 3). If n_{ideal} implies a possible

configuration (List 4), this is the optimal value for m. However, it is possible that n_{ideal} represents not a feasible configuration. If n_{ideal} is out of boundary of possible configurations, we set n_{opt} to the minimum or maximum (Lists 6 and 8). Otherwise, we find a consecutive n_i and n_{i+1} in $\hat{N}'$ that are near n_{ideal} (List 11). Between two configurations, we select the one whose sum of the power converter loss and IR loss due to the bank internal resistance is smaller (List 12). Finally, n_{opt} is derived (List 13), and the optimal configuration is returned. This algorithm has $O(\log |\hat{N}|)$ time complexity if $\hat{N}$ is in an ascending order, because finding elements in Lists 3 and 11 can be done with a binary search. Other operations are done in constant time; the lookup table indexing and the interpolating are done in constant time, and efficiency evaluation in List 12 is done only for two configurations regardless of the size of $\hat{N}$.

In a discrete-time reconfiguration scheme, bank reconfiguration is performed every decision epoch, assuming that the voltage and current condition is not significantly changed within a time interval. On the other hand, in a continuous-time reconfiguration scheme, we determine whether if a reconfiguration is needed when the voltage or current condition significantly changes.

Figure 4.6 shows two configuration transitions of a 120-cell bank when discharging. The figure shows transitions from $C(24,5)$ to $C(30,4)$, and from $C(30,4)$ to $C(40,3)$. The transitions occur at the points where the power loss (sum of power converter loss and internal resistance IR loss) of two consecutive configurations cross. This is different from a previous work [118] that the configuration transitions is triggered by the bank voltage variation constraint. Although limiting the bank voltage variation may improve the power conversion efficiency if the voltage range is chosen elaborately, but there is no explicit clue for setting the voltage range. Furthermore, the current which also affects the conversion efficiency is not considered for reconfiguration in the previous work. The proposed method
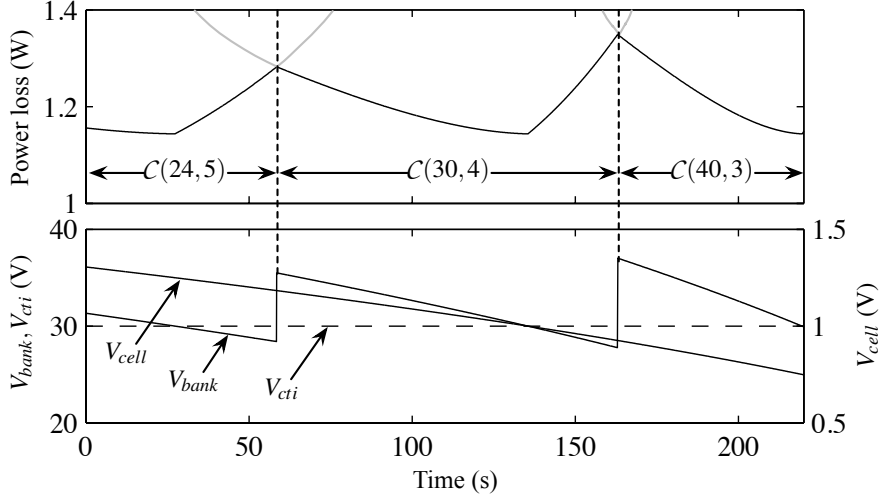
Figure 4.6: Two configuration transitions before and after the configuration $C(30,4)$ when discharging a 120-cell bank. CTI voltage (V_{cti}) is 30 V and CTI current (I_{cti}) is -1 A.

exhibits a better efficiency since it considers the conversion efficiency for the reconfiguration taking the voltage and current into account.

4.1.3.2 Capacity Utilization

We analyze the capacity utilization improvement by the proposed reconfiguration method. From (4.5) and (4.11), the remaining energy $E_{bank,remain}$ of a configuration $C(n,m)$ when $V_{bank} = V_{bank,min}$ is

$$E_{bank,remain} = \frac{1}{2} \cdot \frac{n}{m} \cdot C_{cell} \cdot V_{bank,min}^2. \tag{4.20}$$

From (4.4), (4.5), (4.16), and that $N = m \cdot n$,

$$\rho = 1 - \left(\frac{\min\left(V_{bank,min}, m \cdot V_{cell,lim}\right)}{m \cdot V_{cell,lim}} \right)^2. \tag{4.21}$$

This implies that a reconfiguration in a way that increases m improves the capacity utilization. Figure 4.7 is an example that graphically shows how the capacity utilization is im-

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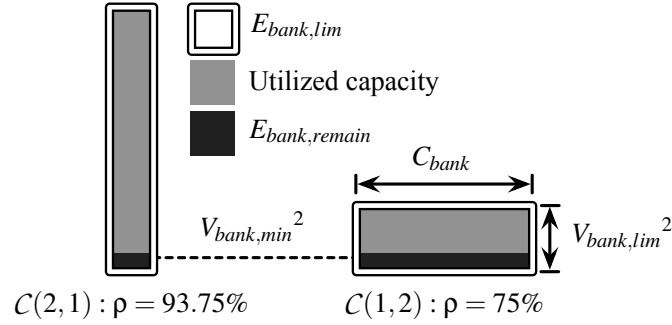
Figure 4.7: Capacity utilization (ρ) of two configurations of a two-cell bank when $V_{bank,min} = \dfrac{1}{2} \cdot V_{cell,lim}$. Note that the vertical length is proportional to the square of voltage so that the area is proportional to the energy capacity.

proved by the reconfiguration. Here, $N = 2$, and two configurations $C(2,1)$ and $C(1,2)$ are available. The horizontal and vertical lengths of the box are proportional to the capacitance and square of the voltage, respectively, and so the area is proportional to the energy. Reconfiguration changes the way to store the same amount of energy; either in higher voltage and smaller capacitance (switching to a more series configuration), or in lower voltage and larger capacitance (switching to a more parallel configuration). Therefore, when the bank is deeply depleted and V_{bank} is near $V_{bank,min}$, we can maximize the capacity utilization by reconfiguring the bank to a configuration with the maximum m, that is, N.

4.1.4 Cycle Efficiency and Capacity Utilization Improvement

In the experiments, we demonstrate that the proposed EES bank reconfiguration method improves the cycle efficiency and capacity utilization of an EES bank. Throughout this section, we use a supercapacitor bank consisting of capacitors with $C_{cell} = 100\,\text{F}$ and $V_{cell,lim} = 2.5\,\text{V}$.

First, we demonstrate the energy efficiency improvement of the proposed EES bank
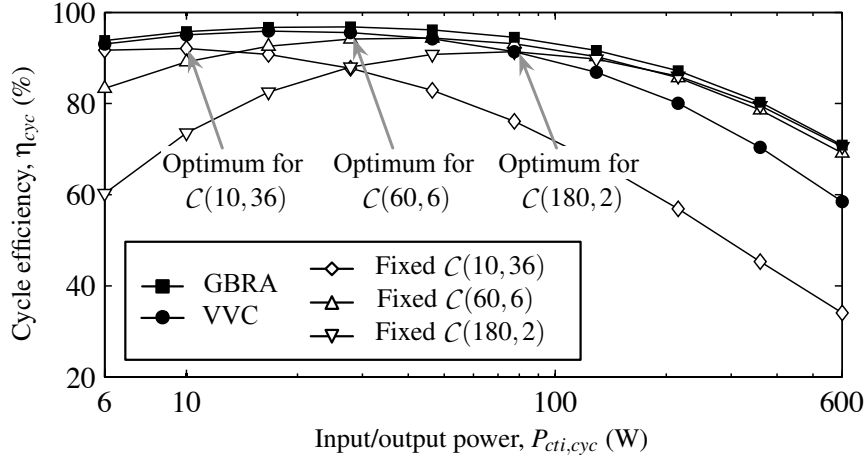
Figure 4.8: Constant-power cycle efficiency comparison for different input/output power values of a 360-cell bank. CTI voltage (V_{cti}) is 30 V.

reconfiguration method (GBRA) compared with two baselines: i) fixed EES bank configurations (Fixed), and ii) voltage variation-constraint (VVC) reconfiguration. The VVC reconfiguration method limits the bank voltage variation by switching the configuration when the bank voltage goes out of the given voltage range. We set the range of bank voltage to $\frac{1}{2} \cdot V_{cti} \leq V_{bank} \leq \frac{3}{2} \cdot V_{cti}$ for the VVC reconfiguration in the experiment. We assume a low minimum bank voltage constraint of $V_{bank,min} = 1.25$ V to minimize the effect of the capacity utilization limit.

We first demonstrate that the constant-power cycle efficiency η_{cyc} discussed in Section 4.1.1, is improved by the proposed reconfiguration method. Figure 4.8 shows the constant-power cycle efficiency of a 360-cell bank according to $P_{cti,cyc}$ ranging from 6 to 600 W, when $V_{cti} = 30$ V.

We can see that the proposed GBRA reconfiguration exhibits the best cycle efficiency for the all range by the timely efficiency-aware reconfiguration. On the other hand, the cycle efficiency of the VVC reconfiguration is lower than that of the GBRA reconfiguration,

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especially when the input/output power $P_{cti,cyc}$ is large. This is because the efficiency degradation due to the input and output voltage difference is escalated as the current increases. Figure 4.8 also shows the cycle efficiency of the three fixed configurations: $C(10, 36)$, $C(60, 6)$, and $C(180, 2)$. The cycle efficiencies of the fixed configurations are not as high as that of the proposed GBRA reconfiguration in the all range of $P_{cti,cyc}$. The cycle efficiency improvement is up to 21% compared with the VVC reconfiguration and up to 108% compared with the fixed configurations in the range of 6–600 W. We can see from Figure 4.8 that the cycle efficiency for larger $P_{cti,cyc}$ is optimal when the configuration has more cells in series. This is because a low bank voltage results in an excessively large current for larger $P_{cti,cyc}$, and induces a large P_{cdct} loss. In contrast, the P_{sw} loss becomes dominant for the high bank voltage cases. This clearly shows that finding the optimal configuration is not straightforward.

Next, we demonstrate the energy efficiency improvement with a varying power input and output, which is more realistic for practical HEES systems. We charge the bank with a low input power until it is fully charged, and then discharge it with a high output power until it is fully depleted. The discharge power P_d is 10 times higher than the charge power P_c, and therefore the maximum duty cycle, which is possible only when the cycle efficiency is 100%, is $\dfrac{1}{10+1} = 9.1\%$. Figure 4.9 shows the duty cycle of a 360-cell bank for P_c ranging from 6 to 600 W, when $V_{cti} = 30$ V. This result also shows that the proposed GBRA reconfiguration exhibits higher energy efficiency even for a realistic high-power pulsed load demand, compared with the VVC reconfiguration and fixed configurations. The duty cycle improvement is by up to 44% compared with the VVC reconfiguration and by up to 127% compared with the fixed configurations in the range of 6–600 W input power.

We demonstrate the capacity utilization for different n and $V_{bank,min}$ values in Figure 4.10. As seen in (4.21), the capacity utilization is dependent on n, but not on m. We

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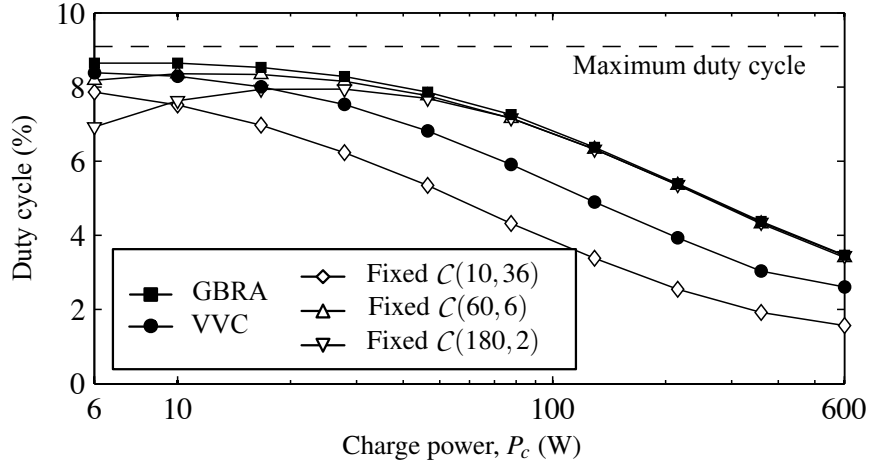
Figure 4.9: Duty cycle for a high-current pulsed load of a 360-cell bank when discharge power (P_d) is 10 times higher than charge power (P_c). CTI voltage (V_{cti}) is 30 V.

can see that the capacity utilization increases as n increases. This result clearly shows the motivation of dynamic reconfiguration to fully utilize the capacity. By dynamically increasing the number of series connections, n, when the bank is almost depleted, we can extract more energy from the bank. For example, when $V_{bank,min} = 10$ V, using a fixed configuration with $n = 10$ results in 84% of capacity utilization. These imply that 16% of the capital cost to purchase and dispose the EES elements is wasted without substantial capacity increase. The capital cost loss is reduced to less than 1% when the EES bank can be reconfigured to $n = 60$.

The energy and cost overhead of the proposed reconfiguration architecture is negligible. The energy overhead is caused by the conduction loss in the MOSFET switches due to their non-zero on-resistance. The resistance of power MOSFET switches are typically a few mΩ. The energy loss due to the resistance is only 1.0% of the total energy in the capacitor array per charge cycle when the charge current is 3 A and a 3 mΩ switch is used. This is negligible when considering the significant energy efficiency improvement. The cost

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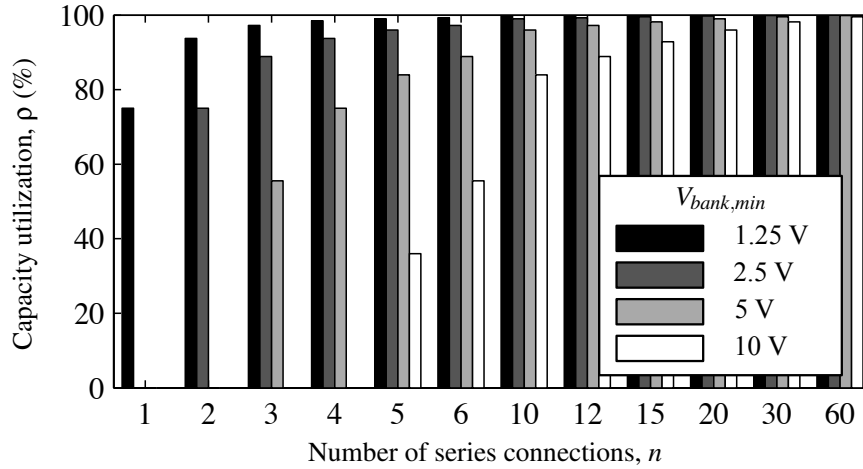
Figure 4.10: Capacity utilization (ρ) for different number of series connections (n) and the minimum bank voltage requirement ($V_{bank,min}$).

overhead is also insignificant. A switching circuit composed of three pairs of switches and gate drivers are required per cell. The cost of the switching circuit is only a few percent of the total cost including the supercapacitors. For instance, a switch circuit composed of ON Semiconductor NTD4904NT4G and one Maxim MAX15054AUT+T costs only $3. A supercapacitor Maxwell BCAP0650 is as expensive as $43. The payback period (PP), which is the time to recover the cost overhead, is dependent to the charge/discharge frequency and electricity cost. The higher charge/discharge frequency or electricity cost is, the shorter PP becomes.

4.2 Networked Charge Transfer Interconnect

4.2.1 Networked Charge Transfer Interconnect Architecture

A HEES system is composed of many EES nodes through a CTI, and so the CTI architecture is an important design factor. It has a significant impact on the charge transfer ef-

| (a) Shared bus | (b) Segmented bus | (c)Multiple bus | (d) Point-to-point |
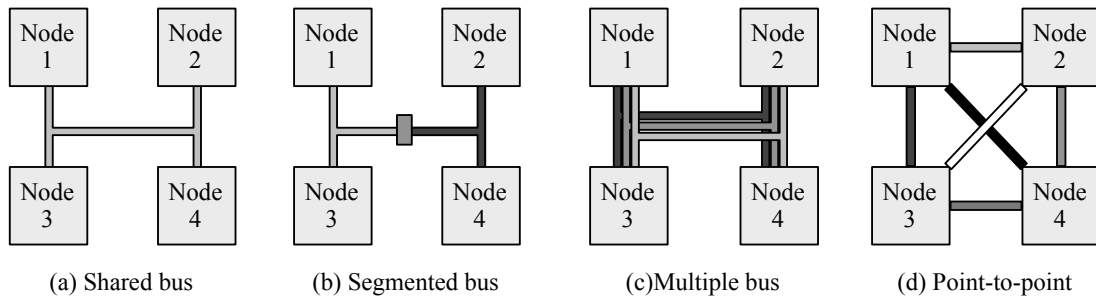
Figure 4.11: Various interconnect architectures for system-on-chip and HEES systems.

ficiency, and thus should be carefully designed in order to maximize the benefits of the HEES systems. A system-on-chip is subject to the similar problem of determining a proper interconnect architecture. The interconnect architecture on a system-on-chip affects communication latency, throughput, power consumption, and so on. For both HEES system and system-on-chip, the interconnect architecture should be selected to considering the scalability. As the number of nodes increases, the interconnect architecture becomes more critical.

Figure 4.11 shows four interconnect architectures. Figure 4.11(a) is a shared bus interconnect. It is simple to implement, but has a limited scalability. Variances of the shared bus CTI with higher scalability include segmented bus CTI in Figure 4.11(b) and multiple bus CTI in Figure 4.11(c). The point-to-point interconnect in Figure 4.11(d) provides independent paths between every pair of nodes, but its cost increases exponentially as the number of nodes increases. These architectures are well explored for the system-on-chips, but also applicable for the HEES systems as we shall discuss.

4.2.1.1 Charge Transfer Conflicts

Shared-bus CTI architectures (sometimes called DC bus) are commonly used when the number of EES banks is limited. Recent works on the HEES system management method-

ologies [107, 108, 109, 111] assume a general shared-bus CTI architecture. The shared-bus CTI is analogous to an on-chip shared bus on a system-on-chip and their advantages and disadvantages are similar. Another CTI architecture is a complete point-to-point connection among the nodes [17]. Both the shared-bus and point-to-point connection architectures are feasible as long as the number of EES banks is small, but they certainly lack scalability to accommodate a large-scale HEES system. The other architecture is a customized network architecture for a particular application and operation policy. For example, a supercapacitor buffer efficiently mitigates the rate-capacity effect of a lithium-ion battery especially for pulsed load demand [18]. As the control policy is to use the supercapacitor as a buffer of the battery, the path from the battery bank to the load device is not necessary. This architecture is similar to an network-on-chip (NoC) architecture with irregular connectivity which is fully dependent on the application. In short, none of the previously introduced CTI architectures can be used to accommodate a large number of EES banks for general applications.

The charge management of a HEES system is achieved by charge allocation, replacement, and migration operations [4]. The operations are basically charge transfers among EES banks using the CTI as charge transfer medium. The previous works on the charge management of HEES [107, 108, 109] assumed that the charge transfer path is always available for a given charge transfer task. They focused on maximizing the energy efficiency by setting a proper value for CTI voltage of the charge transfers. However, it is not always true that a charge transfer path is available whenever it is required. Two or more charge transfer tasks can have a conflict by competing for the shared-bus. Figure 4.12(a) demonstrates an example where the power supply charges the battery bank and the supercapacitor bank supplies power to the load at the same time. Two charge transfer tasks have different optimal CTI voltage values, which maximize the charge transfer energy efficiency
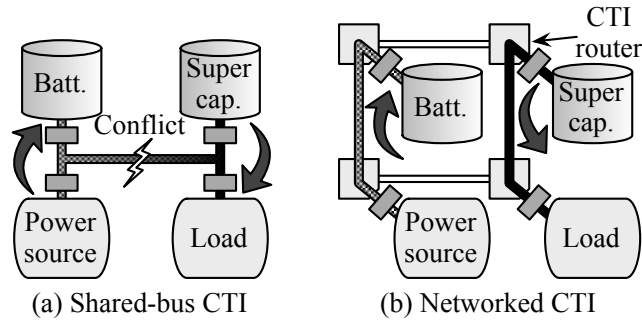
Figure 4.12: Shared-bus CTI and networked CTI of four nodes.

of each task, and there is only one CTI link.

We define that two or more charge transfers conflict when they try to occupy the same CTI link and have different optimal CTI voltage values. Such a conflict enforces the charge transfer tasks to use the same CTI voltage, and thus at least one of them has to suffer possibly severe degradation in energy efficiency.

4.2.1.2 Networked CTI Architecture

We introduce a *networked CTI architecture* as shown in Figure 4.12(b) to fundamentally solve the charge transfer conflict problem, which ensures scalability to a large number of EES banks [113]. Specifically, we use a mesh interconnect architecture to ensure flexibility and scalability of networked CTI architecture. One important component to realize the networked CTI architecture is the CTI router. We propose a CTI router that connects CTI links, an associated component (i.e., an EES bank, a power source, or a load device), and a power converter. Figure 4.13 shows the detailed architecture of the CTI router. Each CTI router is connected with the adjacent CTI routers through the CTI links. The CTI router consists of reconfigurable interconnects which are denoted as dashed lines in Figure 4.13. We dynamically connect or disconnect the reconfigurable interconnects inside the router to
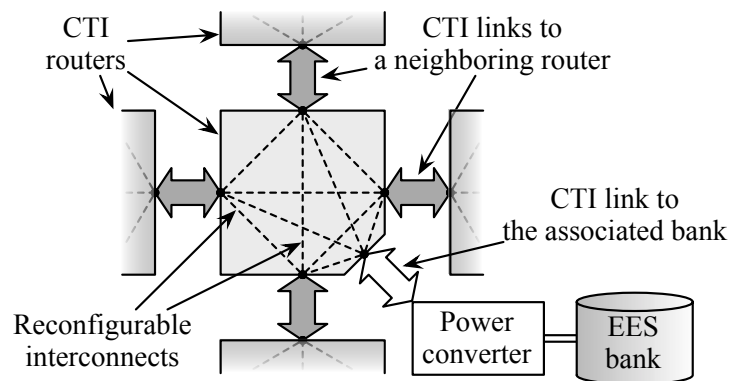
Figure 4.13: Architecture of a CTI router. An associated EES bank is connected via a power converter. The arrows denote the CTI links.

setup a path from one CTI link to another. The reconfigurable interconnects form a complete graph so that the signal can be routed in any direction. The CTI router in Figure 4.13 has five CTI links, and thus it has ten interconnects each of which is implemented as a pair of back-to-back MOSFET switches. We adopt the switching power converter efficiency model from [100].

The networked CTI architecture is comparable to a general NoC architecture. As the number of processing elements in an SoC increases, the single-level on-chip bus architecture is no longer able to handle increased data exchanges between the processing elements. Similar to the NoC which requires packet routing, a HEES system with a networked CTI architecture requires routing of the charge transfers. However, CTI routing on a networked CTI is not the same as the conventional NoC packet routing, conventional signal routing for field-programmable gate array (FPGA), nor application-specific integrated circuit (ASIC).

4.2.2 Conventional Placement and Routing Problems

Placement and routing is one of the challenging issues for electronic design automation, and many related papers are published for decades. A placement algorithm is given components such as circuit modules or logic cells as input and determines their locations on a printed circuit board (PCB) or very-large-scale integration (VLSI) circuit. Good placement is important to obtain a good routing result that minimizes wire length that affects area, latency, power consumption, and so on. Force-directed placement methods model connectivity of components as pulling and pushing force and place the components where the force is minimized [119, 120]. Partitioning-based methods iteratively divide components into two sets such that the number of nets connecting the two sets is minimized [121, 122]. Simulated annealing-based placement algorithms move components and evaluate the cost while reducing the movement range as the temperature decreases [123]. In spite of the diverse placement algorithms, the node placement problem for the HEES system is not introduced yet.

The CTI routing problem in a networked CTI has similarity to the conventional FPGA signal routing problem. In the problem of CTI routing, each task competes for routing resources such as converters and CTI links, whereas each signal competes for wires and connection points in FPGA routing. The FPGA routing is a highly complex combinatorial optimization problem, and thus it is usually done by iterative rip-up and reroute of signals. The success of routing is dependent not just on the choice of which nets to reroute, but also on the order in which rerouting is done as shown in traditional rip-up and reroute methods [124, 125]. The negotiation-based FPGA router successfully relieves the signal ordering problem and provides a systematic rip-up and reroute capability [126]. This routing algorithm allows initial sharing of the routing resources among signals, but subsequently

makes them negotiate for the shared resource with other signals until no resource is shared. The negotiation-based routing algorithm is further enhanced in terms of compilation time by incorporating delay-driven routing [127]. More recent works such as [128] focus on the new architecture or technology scaling, but the core of the routing algorithm is still based on [126]. Table 4.2 briefly compares the PCB/VLSI placement and routing problem and the CTI placement problem for the HEES system.

4.2.3 Placement and Routing Problems

We formally describe the node placement and CTI routing procedures of the networked CTI. We have a set of charge transfer tasks $\tau = \{T_i\}$ to perform. A charge transfer task is defined as a five-tuple $T_i = (\Sigma_i, \Delta_i, \varepsilon_i, R_i, D_i)$, where Σ_i is the source node, Δ_i is the destination node, ε_i is the amount of energy to be transferred to Δ_i, R_i is the task arrival time, and D_i is the duration. A task T_i and the participating nodes Σ_i and Δ_i are active during the time period of $[R_i, R_i + D_i]$. We assume that all the charge transfer tasks are single-source single-destination without loss of generality.

The CTI routing is a runtime procedure that finds independent routing paths that connects all the nodes in Σ_i and Δ_i for the period of D_i for each $T_i \in \tau^a$, where $\tau^a \subset \tau$ is the set of active charge transfer tasks. The CTI routing procedure assigns the CTI links, which corresponds to edges of E, to each T_i to make the path. The CTI routing procedure involves charge transfer optimization, which is to find the optimal CTI voltage V_{cti}^{opt} of the charge transfer task that maximizes the charge transfer efficiency. The networked CTI should periodically perform the CTI routing to maintain the best CTI configuration at all times for the given τ^a.

However, the number of CTI links is limited, and it may be impossible to assign independent paths to all the tasks if there are too many tasks that should take place simul-
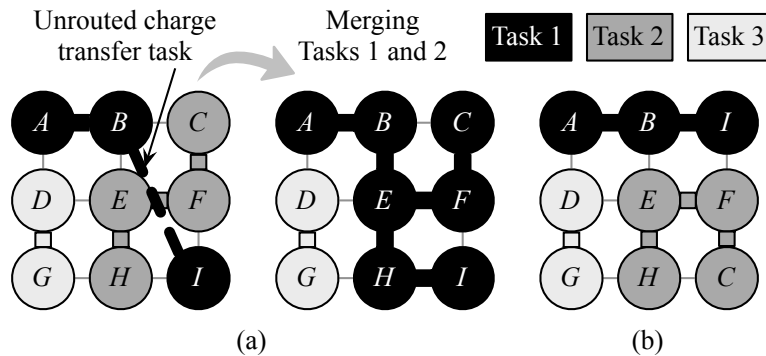
Figure 4.14: CTI routing examples of three charge transfers on two different node placement results. The poor placement (a) requires task merging to complete routing, but the good placement (b) does not.

taneously. The previous work introduces a unique feature of CTI routing such that some tasks may share the CTI link in such cases [113]. This is called task merging. It consolidates the tasks at the expense of charge transfer efficiency degradation because the merged tasks should share a sub-optimal CTI voltage like a shared-bus CTI. Therefore, reducing the number of task merging is the key to maximize the charge transfer efficiency [113].

We see that an elaborated node placement on a networked CTI dramatically enhances the routability and hence reduce the potential task merging occurrences. Figure 4.14 shows two node placements that lead to different CTI routing results. There are nine nodes and three charge transfer tasks to perform. Figure 4.14(a) shows a placement that fails in complete routing. Task 1 is not completely routed because there is no CTI link available to connect Node *I* to Node *A* or *B*. Merging Task 1 and Task 2 is a workaround to complete the routing at cost of degradation of the charge transfer efficiency. The merged task will suffer from low charge transfer efficiency if the V_{cti}^{opt} for Task 1 and Task 2 is different. Another placement shown in Figure 4.14(b), on the other hand, achieves complete routing without task merging. All three charge transfer tasks are performed with their own V_{cti}^{opt}.

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The node placement problem is more complicated than this example in practice. Each charge transfer task arrives and finishes at different time, and so τ^a is not a constant set. The sets of nodes to be connected through the routing change over time depending on τ^a. Therefore, the optimal placement of nodes is not fixed but continuously changes. For instance, placing Node I next to Node B in Figure 4.14 is good while Task 1 is active, but it is no longer beneficial once Task 1 is finished because the CTI configuration should be changed for the next τ^a.

We present a formal definition of the CTI routing problem in this section. We first define a *node* as a combination of a CTI router and either of an EES bank, a power source, or a load device associated with it. A CTI network is a graph $G = (V, E)$ where V is a set of vertices that corresponds to nodes, and E is a set of edges that corresponds to CTI links between two elements in V. It is an undirected graph as the CTI links are bidirectional electrical conductors. The link between the CTI router and the associated EES element (an EES bank, a power source or a load device) is a dedicated resource, and thus we do not consider this in the routing algorithm.

The CTI routing problem is to find routing paths for a given transfer task set τ, that connects all the nodes in Σ_i and Δ_i for each $T_i \in \tau$. A node of T_i participates in only one charge transfer, and it is either a source or a destination, not both. That is,

$$\bigcup_{T_i \in \tau} (\Sigma_i \cap \Delta_i) = \varnothing \quad \text{and} \quad \bigcap_{T_i \in \tau} (\Sigma_i \cup \Delta_i) = \varnothing. \tag{4.22}$$

As a result of the CTI routing, a disjoint subset of edges in E that forms an acyclic routing tree is assigned to each T_i. We set each CTI router configuration (make connections of the internal interconnects) according to the edges in the routing trees. An individual routed charge transfer is equivalent to a charge transfer on an independent shared-bus CTI. Therefore, it enables us to apply any previous HEES charge management methods that are based

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on a shared-bus CTI to each routed charge transfer task.

The routing process allocates limited resources to the nets (the set of charge transfer tasks or signals), and each net is allowed to use the resource for a designated period. Routing charge transfer tasks requires iterative execution of two steps; i) the CTI routing and ii) charge transfer optimization. The CTI routing operation is to determine a routing path of the charge transfer, and the charge transfer optimization operation is to determine the voltage level of the routing path and the amount of current through the routing path.

The CTI routing problem should tackle limitation in the routing resources (the CTI links) like the conventional FPGA routing problems. Signal routing of FPGA fails if there are unrouted nets which are not routable with remaining routing resources. The workaround is either increasing the resource, i.e., using a larger device or optimizing placement so that the congestion is reduced.

On the other hand, redoing placement is not an option for the CTI routing problem because the nodes are at a fixed location in the HEES system and cannot be moved. Instead, we perform *merging* in order to mitigate the routing congestion. This is a unique feature of the CTI routing for HEES systems. Merging is combining two charge transfer tasks into one to produce a new task set. Two or more migration tasks can be merged and share resources unlike signal routing.

If one task has a longer deadline than the other, the combined task uses the CTI links for whichever the shorter deadline. After the deadline expires, the task with a shorter deadline releases the CTI links and the task with a longer deadline solely occupies the CTI links after rerouting. Merging $T_i = (\Sigma_i, \Delta_i)$ and $T_j = (\Sigma_j, \Delta_j)$ results in a new task $T_{i,j} = (\Sigma_i \cup \Sigma_j, \Delta_i \cup \Delta_j)$. Then T_i and T_j are removed from τ and $T_{i,j}$ is added to τ. After T_i or T_j that has a shorter deadline is finished, the remaining task is added back to τ with the remaining deadline.
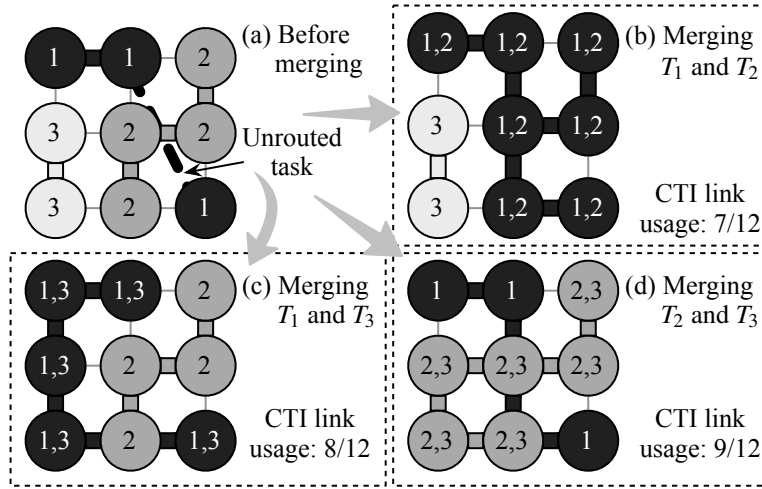
Figure 4.15: Example routing of three tasks after merging. T_1 is unrouted in (a), and routing after three possible merging combinations are presented in (b), (c), and (d).

Figure 4.15 is an example of the merging to improve routability of three tasks. In Figure 4.15(a), T_2 and T_3 are routed, but T_1 is not routed. There are three possible combinations to merge two tasks out of three as shown in Figures 4.15(b), (c), and (d). The CTI link usage out of 12 CTI links is different depending on the combinations. The number of unused CTI links directly affects the routability of the other charge transfer tasks.

Most importantly, merging is not free. A merged task suffers efficiency degradation due to single CTI voltage constraint. Therefore, we have to consider not only the routability but also the efficiency at same time.

4.2.4 Force-Directed Node Placement

We propose a force-directed node placement algorithm. The force-directed placement algorithm models interaction of nodes as attractive (pulling) force and repulsive (pushing) force. The attractive force between a pair of nodes becomes stronger as the distance increases, whereas the repulsive between a pair of nodes becomes stronger as the distance

decreases. The algorithm places the nodes where the net force is the minimum. The key for applying force-directed placement to the node placement problem is to define the coefficients of the force model so that they accurately reflect the routability and charge transfer efficiency depending on the location of the nodes. Specifically, the force vector $\mathbf{F}_i$ applied to node n_i is

$$\mathbf{F}_i = \mathbf{F}_i^a + \mathbf{F}_i^r, \tag{4.23}$$

where $\mathbf{F}_i^a$ is the attractive force vector and $\mathbf{F}_i^r$ is the repulsive force vector.

The attractive force $\mathbf{F}_i^a$ is defined as

$$\mathbf{F}_i^a = \sum_j \mathbf{F}_{i,j}^a = \sum_j c_{i,j} d_{i,j}^m \hat{\mathbf{d}}_{i,j}, \tag{4.24}$$

where $c_{i,j}$ is connectivity weight, $d_{i,j}^m$ is the manhattan distance between n_i and n_j such that $d_{i,j}^m = (x_j - x_i) + (y_j - y_i)$, and $\hat{\mathbf{d}}_{i,j}$ is the unit vector of the linear distance vector between n_i and n_j such that $\mathbf{d}_{i,j} = (x_j - x_i, y_j - y_i)$. We use the manhattan distance because it is a more accurate index of CTI link occupation than the euclidean distance. The connectivity weight $c_{i,j}$ indicates the significance of interaction of the nodes to the charge transfer efficiency. The significance is determined by two factors, which are amount of transferred energy ε and duration of the the charge transfer D of charge transfer tasks. We place two nodes close if the amount of charge transfers between them is large (high ε) because they have a significant impact to the total charge transfer efficiency. Also, we place two nodes close if they occupy CTI links for a long period (high D) so that they do not obstruct routing of the other tasks. Therefore, the connectivity weight $c_{i,j}$ is defined as

$$c_{i,j} = \alpha \sum_{T_k \in \tau[i,j]} \varepsilon_k D_k, \tag{4.25}$$

where α is a scaling constant and $\tau[i,j]$ is a set of all tasks such that n_i is the source and n_j is the destination or vice versa. A high $c_{i,j}$ implies that it is more beneficial to place n_i and

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n_j close. The connectivity weight is symmetric so that $c_{i,j} = c_{j,i}$.

The repulsive force $\mathbf{F}_i^r$ is defined as

$$\mathbf{F}_i^r = \sum \mathbf{F}_{i,j}^r = -\sum_j \frac{\Delta_{i,j}}{d_{i,j}^m} \hat{\mathbf{d}}_{i,j}, \tag{4.26}$$

where $\delta_{i,j}$ is the hindrance weight. The direction of $\mathbf{F}_{i,j}^r$ is opposite to $\mathbf{F}_{i,j}^a$. The hindrance weight $\delta_{i,j}$ indicates potential congestion on the CTI links between n_i and n_j during routing. The congestion occurs if both the nodes are active simultaneously. Its negative impact on the charge transfer efficiency gets worse if V_{cti}^{opt} difference between the charge transfers is large. Therefore, the hindrance weight $\delta_{i,j}$ is defined as

$$\delta_{i,j} = \beta \int a_{i,j}(t) \left| V_i^{opt}(t) - V_j^{opt}(t) \right| dt, \tag{4.27}$$

where β is a scaling constant and $a(t)$ is a binary variable such that

$$a_{i,j}(t) = \begin{cases} 1 & \text{if both } n_i \text{ and } n_j \text{ are active at time } t \\ 0 & \text{otherwise} \end{cases}, \tag{4.28}$$

and $V_i^{opt}(t)$ is V_{cti}^{opt} of the charge transfer that n_i performs at time t. A high $\delta_{i,j}$ implies that it is more beneficial to place n_i and n_j apart. Participating in the same charge transfer does not affect $\delta_{i,j}$ even they are both active because $V_i^{opt}(t) = V_j^{opt}(t)$. The repulsive force makes nodes that have similar V_{cti}^{opt} placed close and makes nodes that have different V_{cti}^{opt} placed apart. It minimizes the charge transfer efficiency degradation due to task merging because charge transfer efficiency of merged tasks with similar V_{cti}^{opt} is less affected by sharing the CTI links with the same CTI voltage.

We define the objective function ρ to evaluate the quality of the placement after each iteration as

$$\rho = \rho^a + \rho^r, \tag{4.29}$$

where

$$\rho^a = \sum_i \sum_j c_{i,j} d_{i,j}^m, \tag{4.30}$$

$$\rho^r = \sum_i \sum_j \frac{\delta_{i,j}}{d_{i,j}^m}, \tag{4.31}$$

which are equivalent to the sum of magnitude of attractive and repulsive force of all nodes, respectively. We iteratively select a node that has the highest magnitude of net force and move it toward the direction of the force. Figure 4.16 illustrates an example of force vectors of each nodes captured at the beginning of an iteration. We see $\mathbf{F}^a$ vectors (light gray arrow) point inward. Strong $\mathbf{F}^a$ applied to a node means that it is far from other nodes that actively perform charge transfers. On the other hand, $\mathbf{F}^r$ vectors (dark gray arrow) point outward. Strong $\mathbf{F}^r$ applied to a node means that it is close to other nodes that may incur congestion during routing. In this example, the force applied to Node A is the strongest as denoted with the longest black arrow. Therefore, moving Node A is most likely to reduce ρ. Contour lines in Figure 4.16 denotes the magnitude of $\mathbf{F}$ applied to Node A when it is placed at each point. The lines are curvy due to the repulsive force between Node A and other nodes. The cross in Figure 4.16 denotes the point where $\mathbf{F}$ applied to Node A is minimized. We map Node A to a vertex near the cross where $\mathbf{F}$ is the minimum and fix it. The victim node that was originally mapped to the vertex finds its new optimal vertex in turn. The iteration ends when the ripple moves finish or when there is no more node to move. The series of moves is accepted if ρ decreases, and the next iteration begins. Otherwise, we pick another node with the next-strongest $\mathbf{F}$ for the next iteration.

Algorithm 2 is the formal description of the proposed node placement procedure. We first do the charge transfer optimization to obtain V_i^{opt} for each task T_i assuming an ideal CTI that provides independent paths for all tasks (Line 2). We calculate $c_{i,j}$ and $\delta_{i,j}$ next (Line 3). We subsequently perform initialization. We find an initial placement (Line 4) and
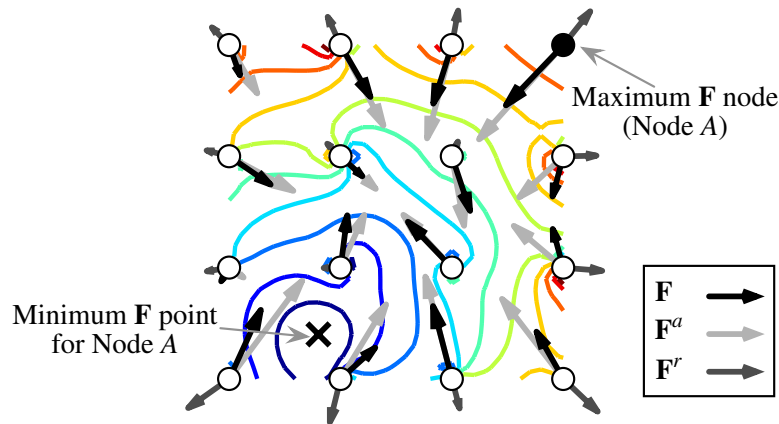
Figure 4.16: Arrows denote force vectors applied to each node. Contour lines denote the magnitude of **F** applied Node A is located at each point. The cross denotes the point where **F** applied to Node A is minimized.

evaluate it (Line 5). This may be a random placement or manual placement. The free node set N_f is set to N initially (Line 6).

We iterate trials to move one node at a time until no more free node exists (Line 7). We first update **F** at the beginning of each iteration for the current placement (Line 8). We select a node n_i among the free nodes N_f that has the highest magnitude of net force (Line 9). We map n_i to the vertex where $\mathbf{F}_i$ applied to n_i is minimized and get a new placement $f_{p,trial}$ (Line 10). This triggers ripple moves of other nodes in which the victim nodes recursively find a new vertex. We evaluate the new placement $f_{p,trial}$ triggered by moving n_i (Line 11). The new placement $f_{p,trial}$ is accepted and all the nodes are freed if ρ decreases compared with the previous placement f_p (Lines 12–15). Otherwise, n_i is fixed and not considered as a candidate in the subsequent trials (Line 17).

Formally speaking, the node placement finds an injective function (one-to-one function) f_p from N to V. Each n_i is mapped to one v_i. Each v_i has a fixed location (x_i, y_i). We call

that n_j is placed at (x_i, y_i) if n_j is mapped to v_i. The example in Figure 4.14 shows a HEES system where nine nodes are one-to-one mapped to nine vertices. Physical meaning of mapping a node to a vertex is that we attach the node to a CTI router that corresponds to the vertex. We assume a grid-like networked CTI like Figure 4.14. The vertices have a regular arrangement, and the edges connect neighboring vertex pairs.

An individual task that is assigned with an independent path is equivalent to a charge transfer on a shared-bus CTI. Therefore, we apply the previous optimization and management schemes that are based on a shared-bus CTI to each charge transfer task after routing. We limit the scope of interest to the node placement and employ the existing CTI routing scheme [113] and charge transfer optimization schemes [107, 108, 109] to focus on the node placement problem.

4.2.5 Networked Charge Transfer Interconnect Routing

We present the proposed networked CTI routing algorithm in Algorithm 3 [113]. The input of Algorithm 3 is the CTI network G and a set of charge transfer tasks τ. Algorithm 3 iteratively performs rip-up and rerouting the charge transfer tasks until all the tasks are routed. The kernel of the routing algorithm is based on the negotiated congestion (NC) routing algorithm in [126]. The cost of resources (CTI links) gradually increases over iterations, and each charge transfer task competes with others to occupy the resource. Only one charge transfer task that is willing to pay the cost occupies the resource, and the other tasks detour via other less-costly resources.

We first define the cost of resources taking into account the distinctive characteristics of the CTI routing problem. An edge $e = (u, v)$ is associated with a congestion cost $c[e]$ that is defined as

$$c[e] = (b[e] + h[e]) \cdot p[e], \tag{4.32}$$

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where $b[e]$ is the base cost of the edge e, $h[e]$ is the congestion history cost and $p[e]$ is the penalty due to the congestion at the current iteration. The base cost $b[e]$ is related with the unit cost of charge transfer from u to v, and we set the base cost to 1. The penalty $p[e]$ is defined as

$$p[e] = 1 + p_{gradient} \cdot u[e], \tag{4.33}$$

where $p_{gradient}$ is a constant, and $u[e]$ is the number of charge transfer tasks that share the edge e. The congestion history cost $h[e]$ increases gradually after each iteration to increase cost of congested edge and make the conflicting nets to avoid it. That is,

$$h[e] = \begin{cases} h[e]' & \text{if } u[e] = 0 \\ h[e]' + h_{gradient} \cdot (u[e] - 1) & \text{if } u[e] \geq 1 \end{cases}, \tag{4.34}$$

where $h[e]'$ is $h[e]$ of the previous iteration, $h_{gradient}$ is a constant, and $h[e]$ is initially 0.

Only the congestion history cost is dependent on the number of iterations by (4.34), and it is a non-decreasing function of the number of iterations. This is because the nets to be routed do not change over iterations in the signal routing, and so the congested resources are likely to be congested again in subsequent iterations. This is not the case for the CTI routing problem because we merge conflicting tasks into one, and then the shared resources are not congested any more. The cost of the previously shared edges are overestimated if we do not decrease $h[e]$ after they are merged. This leads to other charge transfers to avoid using the released edges and results in non-optimal routing results. Therefore, we reduce $h[e]$ of edges that have been congested by the merged tasks.

We define a conflict graph as $G^c = (V^c, E^c)$. There are $k = |\tau|$ nodes in $V^c = \{v_1^c, v_2^c, \ldots, v_k^c\}$, and each v_i^c is mapped to T_i. A conflict graph G^c is a complete graph, and each edge $e^c = (v_i^c, v_j^c) \in E^c$ is assigned with $d[e^c]$ which is *conflict count* between tasks T_i and T_j. Initially, $d[e^c]$ is set to zero, and we increase $d[e^c]$ by n if the tasks T_i and T_j share n CTI

links. We define the sum of the conflict counts of all the edges in a conflict graph G^c to be a *conflict degree* $D[G^c]$ such that

$$D[G^c] = \sum_{e^c \in E^c} d[e^c], \tag{4.35}$$

which is the metric of routability of a given task set.

We also use this conflict graph to prune away the task pairs that do not increase the routability after merging. This is important to efficiently find task pairs to merge by avoiding a situation of trying all the pairs in every iteration. We try merging a pair of tasks, and accept it if it increases the routability. We define that the routability is improved if the conflict degree is reduced after merging by the conflict count between merged transfer tasks or more. That is, we accept the merging of T_i and T_j if

$$D[G^{c\prime}] \leq D[G^c] - d[(v_i^c, v_j^c)], \tag{4.36}$$

or reject it otherwise. We mark an edge of rejected task pair with $r[e^c] = 1$ to indicate the task pair is previously rejected, and $r[e^c] = 0$ otherwise.

We merge a pair of tasks T_i and T_j that have the least difference in the optimal CTI voltage if they conflict ($d[(v_i^c, v_j^c)] > 0$) and have not been rejected previously ($r[(v_i^c, v_j^c)] = 0$). Merging the two tasks results in a new conflict graph because two tasks T_i and T_j is removed and a new task $T_{i,j}$ is added. The new task is marked not-to-be-merged ($r[e^c] = 1$) with existing tasks if both the merged tasks were marked not-to-be-merged with the tasks. The conflict count $d[e^c]$ is reset to zero after merging.

The algorithm starts from initialization of the cost of $e \in E$ based on (4.32), (4.33), and (4.34) in Line 1. Initially, $u[e] = 0$ for all e. It also initializes the conflict graph G^c in Line 2. We try routing and merging until all the CTI links are not shared by multiple charge transfer tasks in the loop through Lines 3–15. The loop in Lines 4–6 attempts to route the

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given task set with the NC-router. The NC-router repeats rip-up and rerouting for all the charge transfer tasks while updating the edge cost $c[e]$ in Line 5. We update the conflict graph after one trial for the rip-up and rerouting for all the charge transfer tasks in Line 6. These procedures are repeated until the current task set τ is fully routed. The algorithm is terminated and returns the routing results after the charge transfer optimization for each task in Line 7 if the routing is successful.

We perform merging through Lines 8–15 if the routing fails. We judge that the task set is not routable if routing attempt fails for a certain number of iterations or a certain amount of runtime. The previous merging is rejected in Line 10 if it fails to improve the routability. If the previous merging is rejected, we restore the previous states of τ, G^c, and edge costs of E. We mark rejected pairs of tasks at the edges ($r[e^c] = 1$) in Line 11 so that they are not explored in the future attempts for merging.

Merging tasks begins with saving the current states of τ, G^c, and edge costs of E so that we can restore them when the merging is rejected in Line 12. We utilize the conflict graph G^c to find candidate tasks to be merged. We update G^c and reset the conflict count $d[e^c]$ to zero after merging in Line 14. We also update the cost c of CTI links based on the new CTI link utilization after merging in Line 15.

4.2.6   Energy Efficiency Improvement

4.2.6.1   Experimental Setup

We demonstrate that the proposed node placement algorithm with network CTI examples and evaluate the charge transfer efficiency improvement. The size of CTI network is diverse from 3×3 ($|V| = 9$) to 6×6 ($|V| = 36$), and we have the same number of nodes ($|N| = |V|$). The terminal voltage of the nodes is between 15 V and 200 V. We assume that each node is

one of four types: source, load, and two types of storage banks. The source nodes perform discharging only, and the load nodes perform charging only. The storage banks perform both charging and discharging, but they do not perform charge transfers between the same type storage banks.

All the tasks in τ are single-source single-destination and may become multiple-source multiple-destination through task merging while we perform the CTI routing. The node utilization, which is proportion of active nodes to the total nodes, is around 85%. We adopt routing algorithm from [113] for the runtime CTI routing.

4.2.6.2   Experimental Results

We first show that the proposed node placement algorithm successfully enhances routability, which will reduce charge transfer task merging during routing. The example presented in Figures 4.17 is a 5×5 networked CTI. Figures 4.17(a) to 4.17(c) show $w_{i,j}$ between nodes (left hand side) and its spatial density (right hand side) of a random placement, a manual placement, and the optimal placement, respectively. We denote the scale of $w_{i,j}$ with the thickness of the lines between nodes. The spatial density of a certain area is accumulated $w_{i,j}$ of node connections that pass the area. High density indicates heavy congestion, and so charge transfer tasks that pass the specific area are more likely to be merged. We see that the density decreases and evenly distributed across the whole CTI network after the placement procedure by the proposed algorithm. It is shown that the distance between nodes with a high $w_{i,j}$ is shortened in Figure 4.17(c). Figure 4.18 shows normalized ρ and ρ_{trial} after each iteration. The initial placement is as shown Figure 4.17(a), and the final placement is as shown in Figure 4.17(c). Through 48 iterations, ρ decreases by 59.4%. A manual placement shown Figure 4.17(b) that puts power source, load device, and supercapacitors, which have more frequent charge transfers than the batteries, is slightly better than the random

placement, but still far worse than the optimal placement.

We next show that the optimized node placement leads to higher charge transfer efficiency. Figure 4.19 shows the results of the runtime routing procedure. Figure 4.19(a) shows variation of the number of charge transfer tasks due to task merging. The ideal CTI provides perfectly independent charge transfer path to all the tasks. There is no need to merge tasks on the ideal CTI, and so its charge transfer efficiency is the maximum upper bound. The number of tasks on the random placement is much smaller than that of the ideal CTI where no task merging occurs. Time-averaged number of tasks on the ideal CTI is 10.6, but it is only 3.5 on the random placement. In contrast, the optimal placement derived by the proposed placement algorithm requires only a few of task merging. Time-averaged number of tasks on the optimal placement is 9.1, which is much higher than that of the random placement. Less number of task merging leads to higher charge transfer efficiency as shown in Figure 4.19(b). The charge transfer efficiency on the optimal placement is very close to the maximum charge transfer efficiency that is possible on the ideal CTI only. We confirm the motivation of the node placement problem that the charge transfer efficiency is closely related to number of merged tasks. The charge transfer efficiency degradation becomes severe when more number of tasks are merged.

We perform the node placement and CTI routing to see the charge transfer efficiency improvement for several other cases with diverse size and number of tasks. Table 4.3 shows the results. We compare two metrics: charge transfer efficiency η and task independency μ. The task independency is the time-averaged ratio between numbers of tasks after merging and before merging, which is 100% for the ideal CTI. Case 2 is the result of the 5×5 example that we described above in this section. The improvement in charge transfer efficiency is up to 10%.

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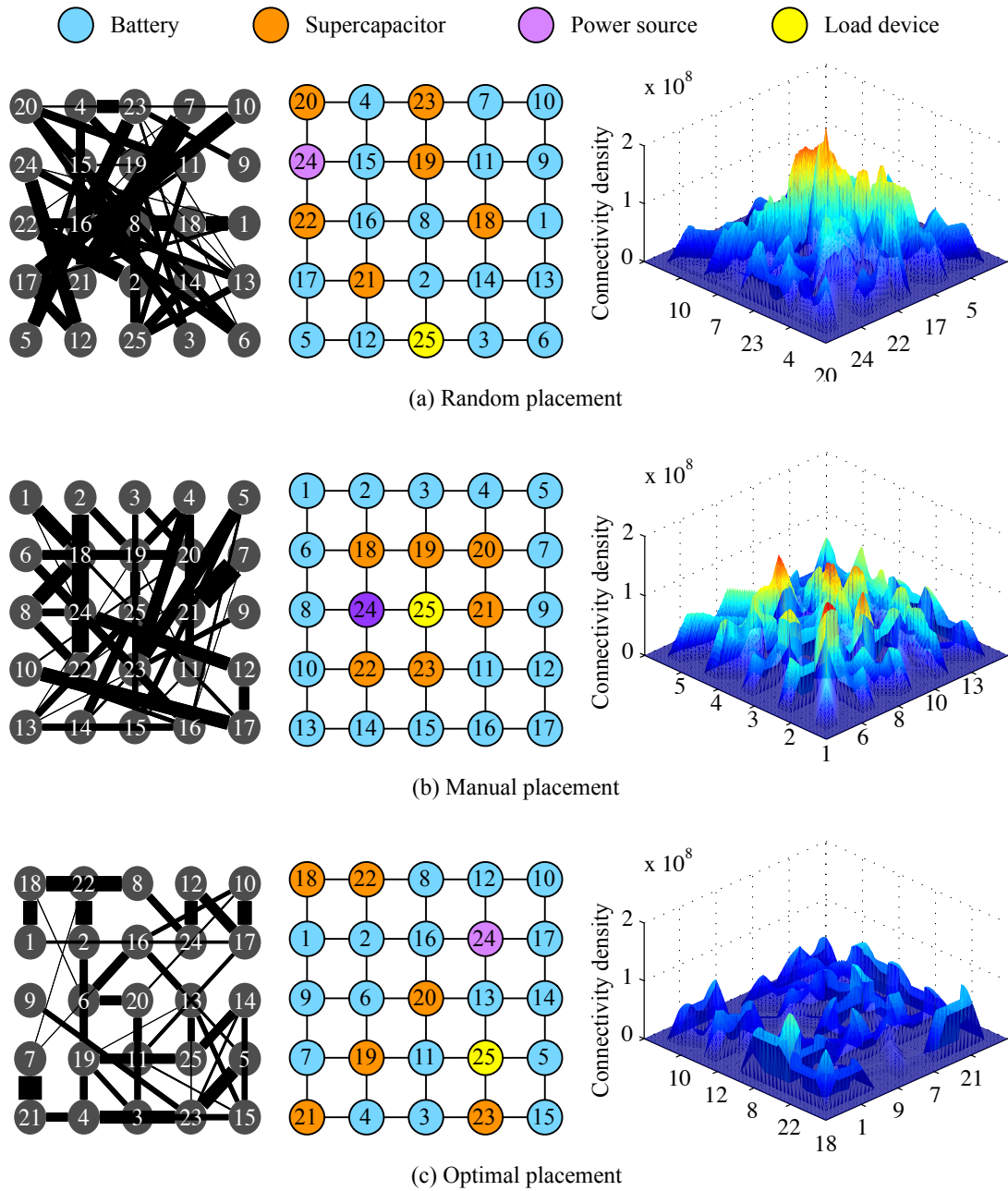
Figure 4.17: Connectivity weight $w_{i,j}$ between nodes and its spatial density of (a) random placement, (b) manual placement, and (c) optimal placement. Gaussian smoothing filter is applied to the density graph for clear view.
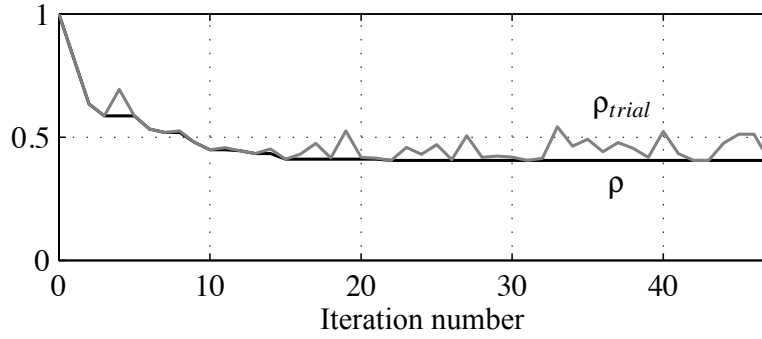
Figure 4.18: Normalized ρ and ρ_{trial} after each iteration.
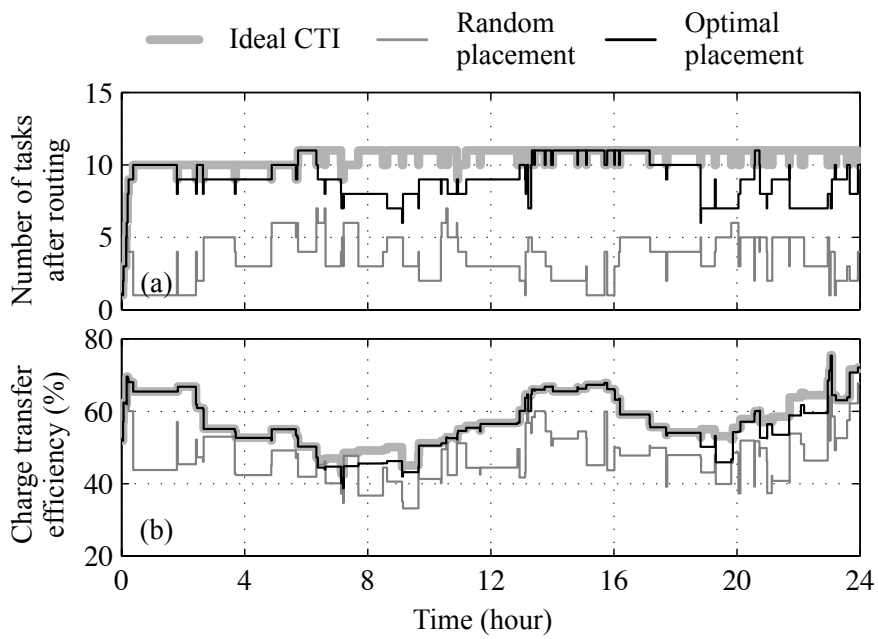
Figure 4.19: (a) Number of charge transfer tasks after merging and (b) charge transfer efficiency.

Algorithm 1: f_{online}: Online optimal configuration determination.

Input: V_{cti}: CTI voltage, I_{cti}: CTI current, and V_{cell}: cell voltage

Output: Optimal configuration (n_{opt}, m_{opt})

Global: N: number of cells, $\hat{N}$: list of possible values of m in an ascending order,

$f_{offline}$: optimal bank voltage mapping function, P_c: power converter loss

model, P_{int}: bank internal resistance IR loss model, $[V_{bank,min}, V_{bank,max}]$:

range of V_{bank}

1 $V_{bank,opt} = f_{offline}(V_{cti}, I_{cti})$

2 $n_{ideal} = \dfrac{V_{bank,opt}}{V_{cell}}$

3 $\hat{N}' = \left\{ m \in \hat{N} \,\middle|\, V_{bank,min} \leq m \cdot V_{cell} \leq V_{bank,max} \right\}$

4 **if** $n_{ideal} \in \hat{N}'$ **then**

5 $\quad\quad n_{opt} = n_{ideal}$

6 **else if** $n_{ideal} \leq \min(\hat{N}')$ **then**

7 $\quad\quad n_{opt} = \min(\hat{N}')$

8 **else if** $n_{ideal} \geq \max(\hat{N}')$ **then**

9 $\quad\quad n_{opt} = \max(\hat{N}')$

10 **else**

11 $\quad\quad$ Find i such that $n_i \leq n_{ideal} \leq n_{i+1}$, where $n_i, n_{i+1} \in \hat{N}'$

12 $\quad\quad n_{opt} = \underset{n}{\arg\min}\left(P_c(V_{cti}, I_{cti}, n \cdot V_{cell}) + P_{int}(n, I_{bank})\right)$ for $n \in \{n_i, n_{i+1}\}$

13 $m_{opt} = \dfrac{N}{n_{opt}}$

14 **return** (n_{opt}, m_{opt})

Table 4.2: Comparison of CTI placement and routing and FPGA/PCB placement and routing.

	CTI placement and routing	FPGA/PCB placement and routing
Nodes	EES banks, power sources, load devices	Lookup tables (LUT), ICs
Links	CTI links	Chanel segments, wires
Flows	Charge flows	Signal flows
Objective	High charge transfer efficiency	Low latency
Placement input	Charge transfer tasks	Netlist
Routing time	Dynamic (runtime)	Static (design time)
Routing output	Charge transfer routing trees	On-/Off-chip interconnect connections
Routing resource sharing	Not allowed	Allowed
Routability	Guaranteed w/ resource sharing	Not guaranteed

Algorithm 2: Node placement algorithm

Input: EES node set N, CTI graph G, charge transfer task set τ

Output: Mapping function f_p

1 **foreach** $T_i \in \tau$ **do**

2 $\quad$ Charge transfer optimization for T_i to get V_i^{opt}

3 Calculate $c_{i,j}$ and $\delta_{i,j}$

4 $f_p \leftarrow$ initial placement

5 $\rho \leftarrow \rho[f_p]$

6 $N_f \leftarrow N$

7 **while** $N_f \neq \varnothing$ **do**

8 $\quad$ Update $\mathbf{F_i}$ for all n_i

9 $\quad$ $n_i \leftarrow$ node in N_f with the strongest $\mathbf{F_i}$

10 $\quad$ $f_{p,trial} \leftarrow$ map n_i to the vertex where $\mathbf{F}_i$ is minimized

11 $\quad$ $\rho_{trial} \leftarrow \rho[f_{p,trial}]$

12 $\quad$ **if** $\rho_{trial} < \rho$ **then**

13 $\quad\quad$ $f_p \leftarrow f_{p,trial}$

14 $\quad\quad$ $\rho \leftarrow \rho_{trial}$

15 $\quad\quad$ $N_f \leftarrow N$

16 $\quad$ **else**

17 $\quad\quad$ $N_f \leftarrow N_f - \{n_i\}$

18 **return** f_p

Algorithm 3: Networked CTI routing algorithm

    Input: CTI graph G, Charge transfer task set τ

    Output: Routing tree for each task with the optimal voltage

1 Initialize cost c

2 Initialize conflict graph G^c

3 **while** shared resource exists **do**

4   **while** routing retry conditions hold **do**

5   NC-route τ on G_{cti} with cost c

6   Update conflict graph G^c

7   Solve the charge transfer optimization problem for each task

8   **if** routing failed **then**

9   **if** previous merging is not successful **then**

10   Reject the previous merging and restore τ, G^c, and costs of E

11   Mark rejected pair of tasks in G^c

12   Save the current τ, G^c, and costs of E

13   Merge the two tasks and update τ

14   Update conflict graph G^c

15   Update costs of E

Table 4.3: Charge transfer efficiency (η) and task independency (μ) on diverse networked CTI examples.

Case no.	CTI grid size	Node utilization	Metric	Ideal CTI	Random placement	Optimal placement
1	3×3 (9 nodes)	87.9%	η	66.1%	64.7%	66.1%
			μ	100%	86.0%	99.9%
2	4×4 (16 nodes)	86.2%	η	48.3%	40.8%	47.9%
			μ	100%	58.6%	96.7%
3	5×5 (25 nodes)	84.7%	η	58.3%	46.8%	56.9%
			μ	100%	33.1%	85.9%
4	6×6 (36 nodes)	84.4%	η	60.6%	49.5%	56.3%
			μ	100%	31.5%	69.1%

Chapter 5

Joint Optimization with Power Sources

5.1 Maximum Power Transfer Tracking

5.1.1 Maximum Power Transfer Point

5.1.1.1 Sub-Optimality of Maximum Power Point Tracking

Figure 5.1 shows the architecture of the solar energy harvesting system. The conventional MPPT techniques aim at maximizing P_{pv}. However, a solar energy harvesting system has a charger circuit which involves a non-zero amount of energy loss P_c, and so P_{charge} is not equal to P_{pv} as we have seen from (5.1). Furthermore, P_c is not constant as we discussed in Section 2.4.1. This results in maximizing P_{pv} does not necessarily guarantee the maximum P_{charge}, and thus the MPPT does not always achieve the maximum harvested energy.

Figure 5.2 shows an example of such a phenomenon. It shows variations of P_{pv}, P_{charge}, and η_c, whose relationship is shown in (5.1), depending on V_{pv}. Conventional MPPT simply
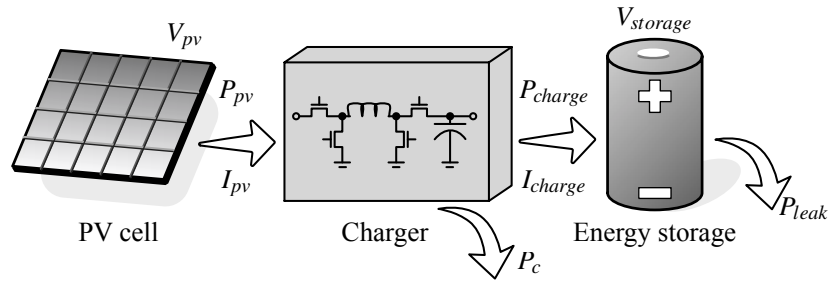
Figure 5.1: Power transfer and loss in a solar energy harvesting system.

finds the MPP (V_{mpp}, I_{mpp}) that results in $P_{pv} = P_{mpp}$ without consideration of the charger efficiency η_c at that point. In Figure 5.2, P_{pv} is maximized at ⓐ when $V_{pv} = V_a$. However, η_c is not high at the MPP, and this results in lower P_{charge} than when $V_{pv} = V_a$ where η_c is higher. Rather, P_{charge} at ⓑ is higher than P_{charge} at ⓐ thanks to higher η_c even though P_{pv} at this point is smaller than P_{mpp}. This is more desirable to operate at ⓑ in that we are interested in maximizing P_{charge} rather than P_{pv} in practice. Consequently, the MPPT and maximum efficiency tracking of the charger should be considered at the same time to overcome the sub-optimality of the MPPT. We have to take the dynamic status of the energy storage device into account when finding the optimal operating point that maximizes P_{charge} because η_c is affected by them. Therefore, we design the system to maximize the output of the charger P_{charge}, not the input of the charger P_{pv}, in order to achieve the system-level energy optimum.

5.1.1.2 Maximum Power Transfer Tracking

We first define the *maximum power transfer (MPT)* point, in contrast to the MPP, as the operating point where the P_{charge} is the maximum [129]. We name the voltage and current of the PV module at the MPT point V_{mpt} and I_{mpt}, respectively. We define P_{mpt} as the

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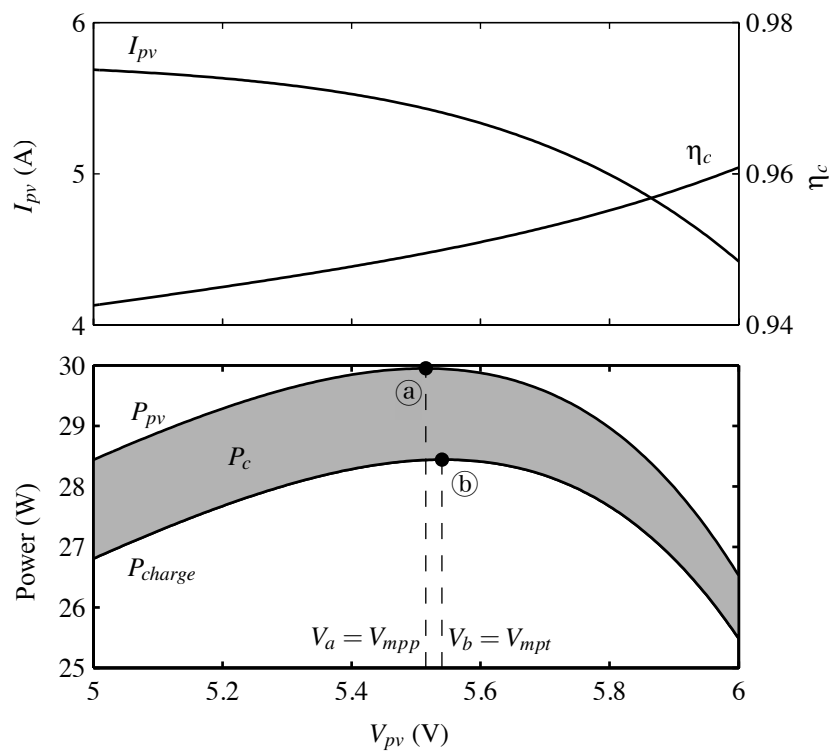
Figure 5.2: Different V_{pv} points that maximize P_{pv} and P_{charge} when efficiency varies. ($P_{charge} = \eta_c \cdot P_{pv}$.)

maximum P_{charge} that is available at the MPT point (V_{mpt}, I_{mpt}). That is,

$$P_{mpt} = V_{mpt} \cdot I_{mpt} - P_c. \tag{5.1}$$

For a given PV module, P_{mpt} is a function of G and $V_{storage}$ when the charger efficiency characteristics are given because P_{charge} is dependent on η_c, whereas P_{mpp} is solely dependent on G. The MPT point changes over time depending on the environmental conditions such as G and system condition such as $V_{storage}$ as mentioned above. The *maximum power transfer tracking (MPTT)* is a run-time operational method that dynamically adjusts the operating point to (V_{mpt}, I_{mpt}). We accomplish the MPTT by measuring P_{charge} and controlling the charger to maximize it. We may use the conventional tracking methods of the MPPT such as the perturb-and-observe or incremental conduction for the MPTT as well.

Figure 2.13(a) shows V_{pv} and P_{pv} variations according to I_{pv} with four different irradiance values. Even with the same irradiance, we can see a significant change in P_{pv}. The MPPT methods discussed in Section 5.1.1.1 can be used to find the maximum P_{pv} regardless of the irradiance.

However, if we take the charger efficiency into account, the *P-I* curve we have to consider is the P_{charge}-I_{charge} curve shown in Figure 2.13(b), rather than the P_{pv}-I_{pv} curve of Figure 2.13(a). Since the *x*-axis is I_{charge}, the *y*-axis P_{charge} is linearly proportional to the I_{charge} when V_{cap} is given. The maximum P_{charge} values, marked by squares, are the MPT points. Beyond this point, further increment of I_{charge} causes a rapid drop of V_{pv}. The V_{pv} values at the MPT points are not the same as the V_{pv} values at the MPP, and P_{charge} at the MPT point is slightly lower than P_{pv} at the MPP because $\eta < 1$.

Our proposed MPTT keeps tracking (V_{pv}, I_{pv}) which may be slightly different from that of conventional MPPT, to guarantee the maximum amount of power transferred to the load at all times rather than the maximum power extracted from the PV module. Note that

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the proposed MPTT always outperforms the conventional MPPT in terms of net energy delivery to the load regardless of environmental conditions.

P_{charge} at the MPT is determined not only by G, but also by the current value of V_{cap}. Figure 5.3(a) is the surface that consists of the maximum P_{charge} values of a 7×10 PV array in the $G - V_{cap}$ domain. We may draw a trace of $(V_{cap}(t), G(t))$ pairs on this surface with the solar irradiance set to a meaningful value in $t \in [t_{sunrise}, t_{sunset}]$. For instance, the white lines are the traces when C is 300 F, 3,000 F or 30,000 F. For illustration purpose, we set $G(t_{noon}) = 900$ W/m^2. Initially, $V_{cap}(t_{sunrise}) = 0$ V. From (5.6), the value of $P_{charge} - P_{leak}$ is the gradient of E_{cap}. Figure 5.3(b) shows the supercapacitor's energy, E_{cap} as t elapses. Right after the sun rises, G is low and P_{charge} is also low, and E_{cap} increases slowly. Generally, with a reasonable supercapacitor of C, P_{charge} has the maximum values during the day, and E_{charge} increases most rapidly at noon ($t = t_{noon}$). The sampling points in Figures 5.3(a) and (b) are matched with each other in terms of t. E_{cap} slightly decreases in the evening due to leakage of the supercapacitor such that $P_{leak} > P_{charge}$ in the evening.

5.1.2 MPTT-Aware Energy Harvesting System Design

5.1.2.1 Optimal System Design Problem

We harvest the solar energy during daytime and typically store some of the energy for use during the nighttime. To focus on energy storage efficiency and avoid divergence from the main context, we assume that there is no energy usage during the daytime. The amount of energy to be stored at the end of the day, E_{req} is given as a design requirement. The objective of the proposed design optimization is to derive a cost-effective and energy-efficient design of a solar energy generation and storage system to achieve this requirement.

Cost-effectiveness is defined as the minimum number of PV modules that meet the en-
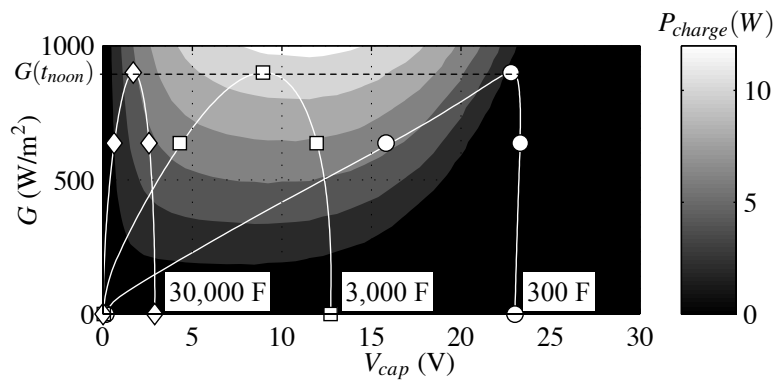
(a) P_{charge} and $(V_{cap}(t), G(t))$ trace line
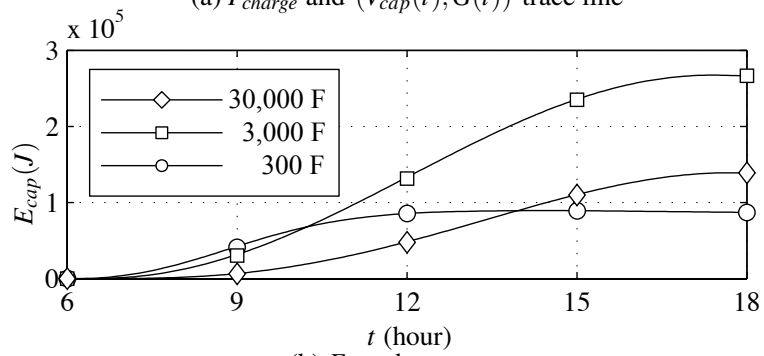
(b) E_{cap} change over t

Figure 5.3: Energy accumulation trace of a 7×10 PV array.

ergy storage requirement, E_{req}. Energy efficiency means maximizing the amount of energy that is eventually stored in the supercapacitor at the end of the day with the same number of PV modules. These two optimizations are coupled together; if we enhance the efficiency, we may use small number of PV modules while satisfying E_{req}.

The amount of energy stored during the daytime is given by

$$E_{cap}(t_{sunset}) = E_{cap}(t_{sunrise}) + \int_{t_{sunrise}}^{t_{sunset}} (P_{charge}(t) - P_{leak}(t)) \, dt. \tag{5.2}$$

We must consider another constraint, i.e., feasibility. Commercially available switching converters and chargers have the maximum voltage rating around 30 VDC, and we must thus limit the maximum voltage of the supercapacitor bank and the PV modules in series. We consider identical PV arrays with the configuration of n in series and m in parallel. Due to this regularity, we can operate all the PV cells at the identical operating condition and maintain uniform energy efficiency for all cells.

The maximum amount of energy that can be stored in a supercapacitor bank is proportional to $C \cdot V_{cap\_max}^2$, where V_{cap_max} is the maximum voltage rating of the supercapacitor bank. We can change C and V_{cap_max} by connecting more unit-sized supercapacitors in parallel and series, respectively. However, the total number of unit-sized supercapacitors necessary to store a certain amount of energy does not change no matter how we configure the series and parallel connections. Therefore the supercapacitor cost, which is proportional to the total number of unit-sized supercapacitors, is not the optimization objective that we consider. We first derive the amount C that results in maximum energy harvesting for the given E_{req}, and next, we determine V_{cap_max} from

$$V_{cap}(t) = \frac{Q(t)}{C} = \sqrt{\frac{2 \cdot E_{cap}(t)}{C}}. \tag{5.3}$$

To make a long story short, smaller voltage difference between the PV array and su-

percapacitor bank achieves better charger efficiency. Thus the key optimization method is to control the supercapacitor voltage by adjusting C, because the PV array voltage is determined by solar irradiance, which is not controllable. For example, if the supercapacitor bank capacitance is too small, the supercapacitor bank voltage rises quickly and goes way higher than the nominal PV array voltage. On the other hand if the supercapacitor bank capacitance is too big, the supercapacitor bank voltage does not rise much and remains far lower than the nominal PV array voltage. Determination of the supercapacitor bank capacitance is also coupled with the PV array configuration. We must jointly optimize how many series and parallel connections of PV cells within a PV array should be established given the supercapacitor capacitance.

We name the overall PV-supercapacitor system efficiency optimization as MPTT design. The MPTT design can be formally described as follows:

- Given: The energy requirement E_{req} and the maximum voltage rating V_{rating}.

- Prerequisite: PV module characteristics, charger efficiency model, and solar irradiance profile G.

- Objective: i) Find a $n \times m$ PV array configuration which minimizes $n \cdot m$ while meeting $E(t_{sunset}) \geq E_{req}$; and ii) given the $n \times m$ configuration, find a supercapacitor bank capacitance C that maximizes the energy efficiency while meeting $V_{cap}(t_{sunset}) \leq V_{rating}$.

It is possible to have $V_{cap}(t)$, for some t, higher than $V_{cap}(t_{sunset})$ due to the self-discharge. However, we assume this is negligible, as we will see in the following section for a half-day storage.

5.1.2.2 Design Optimization

PV Array and the P_{charge} Surface   The configuration of the PV array determines the shape and magnitude of the P_{charge} surface in the $G-V_{cap}$ domain. The total number of PV modules is $N = n \cdot m$, which determines the magnitude of the P_{charge} surface. Evidently the more PV modules are used, the higher power can be achieved. We define P_{peak} and V_{opt} of a P_{charge} surface as

$$P_{peak} = \max_{\forall V_{cap}} \left(P_{charge} \left(G(t_{noon}), V_{cap} \right) \right), \tag{5.4}$$

$$V_{opt} = \arg\max_{V_{cap}} \left(P_{charge} \left(G(t_{noon}), V_{cap} \right) \right), \tag{5.5}$$

which gives the maximum possible power that goes to the supercapacitor and its corresponding condition, with an $n \times m$ PV array. The values of n and m determine the location of P_{peak} and V_{opt}. As n increases, V_{opt} increases almost linearly. To achieve the maximum P_{charge} when G is the maximum ($t = t_{noon}$), $V_{cap}(t_{noon})$ should be equal to V_{opt} such that $P_{charge}(t_{noon}) = P_{peak}$.

Supercapacitor Size and Harvested Energy   It is shown in Figure 5.4 that V_{cap} is a critical factor for P_{charge}. From (5.3), V_{cap} is inversely proportional to C. Therefore the determination of C is very important for maximizing P_{charge}, and in turn, the accumulated energy, E_{cap}. Figure 5.5 shows the total amount of accumulated energy, $E_{cap}(t_{sunset})$, as a function of C. It turns out that neither a small nor a large C is energy efficient. This implies that an ad-hoc decision on C may result in a poor energy harvesting. Each curve in Figure 5.3(a) gives us more intuition about this result. A 3,000 F C is close to the energy optimal. If C is too small (300 F), V_{cap} increases too rapidly and V_{cap} is very different from V_{opt} when G is the maximum. Thus, the curve cannot arrive in the high P_{charge} region. On the other hand, if C is too large (30,000 F), V_{cap} increases too slowly and V_{cap} is again very different from V_{opt} when G is the maximum. Thus again the curve cannot arrive in the high
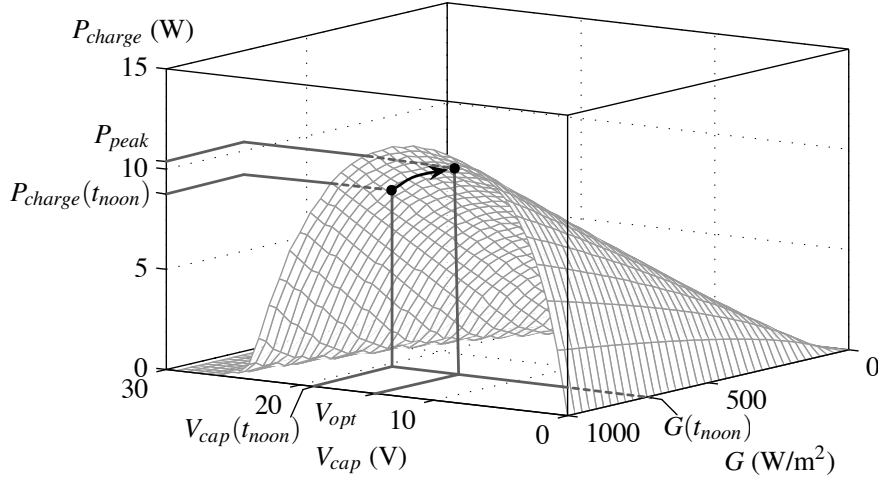
Figure 5.4: Maximum P_{charge} surface of a 7×10 PV array in GV_{cap} domain.

P_{charge} region.

Therefore it is important to determine C so that the system remains in the high-P_{charge} region for a longer period of time. For a symmetrical irradiation profile in a day, we make $P_{charge}(t_{noon}) = P_{peak}$ by adjusting C to guarantee $V_{cap}(t_{noon}) = V_{opt}$. Based on the fact that $V_{cap}(t_{noon}) = V_{opt}$ and using the estimated $E_{cap}(t_{noon})$, the energy-optimal C is calculated by (5.3).

5.1.2.3 Systematic Design Optimization

A naive brute force method to find the optimal design is that first we obtain P_{charge} surfaces for all $n\times m$ PV array configurations, and then evaluate E_{cap} for all C. However, obtaining P_{charge} surfaces as in Figure 5.4 is very time consuming because of the numerical iterations needed to reach the convergence point of the PV model and charger models. Furthermore, as can be seen in Figure 5.3(a), each curve passes only a part of the surface, which makes it pointless to calculate P_{charge} for all (V_{cap}, G) pairs.

Based on the observation that a switching converter exhibits a higher efficiency when

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Algorithm 4: MPTT-aware solar energy harvesting system design

Input: (energy requirement E_{req}, voltage rating V_{rating}, irradiance profile G,

theoretical maximum energy E_{mpp}, noon time t_{noon})

Output: (optimal PV module size n_{opt} and m_{opt}, optimal capacitance C_{opt}), or `null`

if given invalid parameters

1 $N \leftarrow \left\lceil E_{req}/E_{mpp}\left(G(t_{noon})\right)\right\rceil$; $n_{max} \leftarrow \infty$; $m_{max} \leftarrow \infty$

2 **repeat**

3   $\quad V_{opt}(1,N) \leftarrow$ `find_V_opt`$(1,N)$; $V_{opt}(N,1) \leftarrow$ `find_V_opt`$(N,1)$ $N_{next} \leftarrow \infty$

$\quad$ **foreach** $(n,m) \in S = \{(n,m)|(n < n_{max} \vee m < m_{max}) \wedge n \cdot m = N \wedge n, m \in \mathbb{N}\}$ **do**

4    $\quad\quad V_{opt}(n,m) \leftarrow$ `linear_approx`(V_{opt},n,m)

5    $\quad\quad P_{peak}(n,m) \leftarrow$ `maximum_P`$(V_{opt}(n,m),G)$

6    $\quad\quad E_{cap}(n,m) \leftarrow$ `estimate_E_cap`$(P_{peak}(n,m),G)$

7    $\quad\quad C(n,m) \leftarrow 2 \cdot (E_{cap}(n,m)/2)/V_{opt}(n,m)^2$

8    $\quad\quad V_{cap}(n,m) \leftarrow \sqrt{2 \cdot E_{cap}(n,m)/C(n,m)}$

9    $\quad\quad$ **if** $V_{cap}(n,m) > V_{rating}$ **then**

10     $\quad\quad\quad n_{max} \leftarrow \max(n_{max},n)$; $m_{max} \leftarrow \max(m_{max},m)$

11     $\quad\quad\quad$ **if** $m = N$ **then**

12      $\quad\quad\quad\quad$ **return** `null`

13    $\quad\quad$ **else if** $E_{cap}(n,m) < E_{req}$ **then**

14     $\quad\quad\quad N_{next} \leftarrow \min\left(N_{next},N+\left\lceil N \cdot (1 - E_{cap}(n,m)/E_{req})\right\rceil\right)$

15   $\quad N \leftarrow N_{next}$

16 **until** $\exists (n,m)$ *such that* $E_{cap}(n,m) \geq E_{req}$ *and* $V_{cap}(n,m) \leq V_{rating}$

17 $(n_{opt},m_{opt}) \leftarrow$ `maximum_E_cap`(E_{cap}) ; $C_{opt} = C(n_{opt},m_{opt})$

18 **return** $(n_{opt}, m_{opt}, C_{opt})$
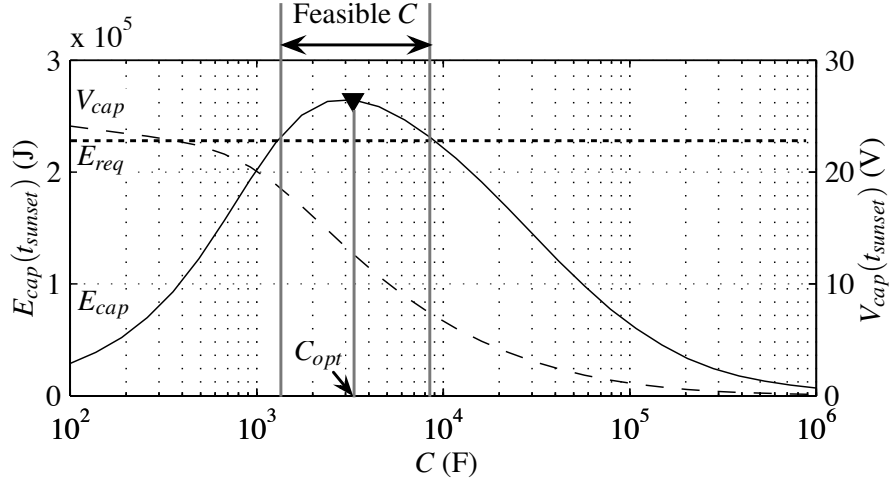
Figure 5.5: Accumulated energy $E_{cap}(t_{sunset})$ and corresponding $V_{cap}(t_{sunset})$ of a 7×10 PV array.

the input and output voltages are similar to each other, we develop Algorithm 4 that efficiently derives the near-optimal values of n, m, and C when E_{req}, V_{rating}, and G are given. The objective of this algorithm is to derive the minimum $n \times m$ and optimal C. Since the supercapacitor cost is determined by E_{req}, C is not to be minimized, but to be optimized for harvesting the largest amount of energy. This algorithm requires that the PV model and the charger efficiency model be characterized *a priori*.

We first calculate the minimum feasible number of PV modules by dividing E_{req} by E_{mpp}, which is the theoretical maximum energy that can be extracted by MPP with the maximum G (Line 1). And temporary variables are initialized subsequently. We find V_{opt} values for the two extreme cases such that all PV modules are connected in parallel or in series (Line 3).

Based on the observation in Section 5.1.2.2, we may linearly approximate V_{opt} for other $n \times m$ configurations from the two extreme cases (Line 4). We estimate the total harvested

energy using

$$E_{cap}(t + \Delta t) = E_{cap}(t) + \Delta t \cdot (P_{charge}(t) - P_{leak}(t)) \qquad (5.6)$$

and $P_{charge}(t) = P_{peak} \cdot G(t)/G(t_{noon})$ where P_{peak} corresponds to the approximated V_{opt}, considering leakage (Line 6). The corresponding C and the maximum V_{cap} are derived by equations on Lines 7 and 8. In each iteration, we prune a large portion of possible configurations that do not satisfy the voltage rating constraint from the current N and larger N (Lines 9). Even the all-parallel configuration may have V_{cap} that exceeds V_{rating} if the given V_{rating} is too low. We stop iteration in such a case (Line 11). If E_{cap} is less than E_{req}, we increase N by the ratio of insufficient energy (Line 14). This is repeated until we find a feasible configuration (Line 16). We choose the configuration that has the maximum E_{cap} among all feasible configurations (Line 17). This algorithm is scalable enough to accommodate large-scale applications due to judicious calculation of N as well as effective pruning.

5.1.2.4   Energy Harvesting Improvement

We use Linear Technology LTC3531 buck-boost converter as the charger model, and the Spectrolab GaAs/Ge single junction PV module of $A = 10$ cm^2, which has $V_{oc} = 1.025$ V, $I_{sc} = 0.305$ A, and $P_{mpp} = 0.257$ W at $G = 1353$ W/m^2 in the experiment. We assume that, without loss of generality, the sun rises at 6:00 and sets at 18:00, and $G(t_{noon}) = 900$ W/m^2. We assume 10% self-discharge rate per day for the supercapacitor, which is a typical value for commercially available supercapacitors.

First we show the energy efficiency of the proposed MPTT method compared with conventional MPPT method. Table 5.1 shows the accumulated energy E_{cap} at the end of the day for various PV array and supercapacitor configurations, which are operated by the

Table 5.1: Energy efficiency of the conventional MPPT and suggested MPTT methods.

$n{\times}m$	Tracking method	C (F)	V_{cap} (V)	E_{cap} (J)	Normalized E_{cap} (%)
5×5	MPTT	2,378	9.0	96,342	100.0
	MPPT	2,378	8.9	93,451	97.0
		23,780	2.2	59,170	61.4
		238	11.0	14,404	15.0
12×2	MPTT	874	15.2	101,545	100.0
	MPPT	874	14.8	95,795	94.3
		8,740	4.2	77,261	76.1
		87	19.1	15,823	15.6

MPPT and MPTT methods. The capacitance C of the MPTT case is the theoretical optimum for each given $n{\times}m$. Most importantly, conventional MPPT methods have no concept of the efficiency-optimal C and PV array configuration, and any C value and any PV array configuration are supposed to yield the same amount of harvested energy. Thus, it is not surprising to have a C value and a PV array configuration for conventional MPPT that yield very poor charging efficiency. We compare the proposed MPTT with conventional MPPT for different C values and PV array configurations. When using the optimal capacitance, MPTT shows more than 6x harvested energy over a poorly configured conventional MPPT as Table 5.1 shows. The results for poorly configured MPPTs are not embellished because conventional MPPT does not care about the charger loss caused by improper C value. More interesting result is that even the accidentally optimal configuration of conventional MPPT is up to 5.7% less efficient than the proposed MPTT. This is because MPTT finds the true optimal tracking point considering the charger loss while conventional MPPT draws

Table 5.2: Energy harvesting result of designs by the proposed method and exhaustive search (ES).

E_{req} (J)	V_{rating} (V)	Opt. method	$n \times m$	C_{opt} (F)	E_{cap} (J)	E_{cap} error (%)
50k	10	Alg. 4	6×2	1,159	49,507	-0.99
		ES	7×2	1,289	58,439	+16.88
50k	30	Alg. 4	12×1	415	50,970	+1.94
		ES	12×1	524	51,711	+3.42
100k	30	Alg. 4	12×2	648	100,011	+0.01
		ES	12×2	874	101,545	+1.55
200k	20	Alg. 4	10×5	2,691	197,713	-1.14
		ES	10×5	1,713	201,702	+0.85

more power from the PV array but loses even more power in the charger. The energy-efficient configuration of MPPT is coincidence and hard to achieve because conventional MPPT gives no clue for the optimal configuration. Note that the 5×5 configuration harvests less energy than the 12×2 configuration while using one more PV cell even the MPTT is applied, and therefore it is not an optimal design. Algorithm 4 can be used to effectively find the optimal design avoiding such a case.

We show the accuracy of Algorithm 4 in terms of actual cost and energy. Recall that Algorithm 4 tries to find the near-optimal value by a heuristic approach to make the computational complexity reasonable. Table 5.2 is the comparison between designs derived by the suggested algorithm and the optimal design found by exhaustive search for various E_{req} and V_{rating} values. For all cases, we notice that the negative error is less than 2%, which is quite reasonable in light of the typical device tolerance used in commercial circuits. This

error is mainly due to the fact that the estimation of E_{cap} is based on the observation that the trace on the P_{charge} curve may be approximated by a sinusoidal waveform. With this approximation, we cannot guarantee a positive or a negative bound on the error.

We confirm that the proposed MPTT design may have a slightly smaller E_{cap} than E_{req}. This is mainly because the curve on the P_{charge} surface is not an exact sine function. We can mitigate this error by a minor overdesign of E_{req}, which is anyway required due to the component tolerance in a real system.

5.2 Photovoltaic Emulation for MPTT

5.2.1 Model Parameter Extraction

We may extract five unknown parameters $I_L(G_0)$, $I_0(T_0)$, R_s, R_p and N from I_{sc}, V_{oc}, V_{mpp} and I_{mpp} for each I-V curve measured under a specific environmental condition (G_0, T_0) using a similar method as [105]. This conventional parameter extraction heuristic can be accelerated by Newton-Raphson iteration method. Although such method is quite stable and does not rely heavily on initial values for the iteration procedure, it does not utilize the whole I-V curve for parameter extraction, and therefore the overall average fitting error cannot be guaranteed to be minimized. Nevertheless, it is still necessary to collect the empirical data for the whole I-V curve in order to find out the MPP, unless we only can rely on the datasheet provided by the manufacturer. In fact, the fitting errors can be significant in some specific PV module I-V ranges. Hence, such method cannot fulfill the requirement of state-of-the-art researches [129, 130, 131] that the whole operating range should be accurately modeled for maximizing the energy efficiency. On the other hand, we adopt a nonlinear curve fitting algorithm here to overcome the shortcoming of the previous method that only some specific points of the whole I-V curve have been used. The parameter ex-

traction is performed only one time for each PV module at the characterization step, and so the computational overhead for the curve fitting is negligible.

The fitting parameters depend heavily on the initial values. If the initial values are not properly set, the fitting results obtained may be not optimal nor even feasible. This is because of the fact that nonlinear curve fitting is a highly non-convex optimization problem, and it is likely to be stuck at a local optimal point. Therefore, we propose to use the parameter extraction heuristic that uses specific points of each I-V curve, accelerated by Newton-Raphson method, in the initial phase. The derived five parameters, i.e., $I_L(G_0)$, $I_0(T_0)$, R_s, R_p and N, serve as the proper initial values in the subsequent least-squares nonlinear curve fitting method based on Levenberg-Marquardt algorithm. Furthermore, we have to also set an upper bound and a lower bound of the fitting parameters, since such bounds also play an important role in the nonlinear curve fitting for acceleration and convergence. One simple, yet effective set of bounds is given by $[\alpha\mathbf{P}, \beta\mathbf{P}]$, where $\mathbf{P} = (I_L(G_0), I_0(T_0), R_s, R_p, N)$ is the derived PV module parameters in the initial phase. With such properly set initial values and upper/lower bounds, nonlinear curve fitting algorithm can find the optimal PV module parameters effectively, taking into account the whole I-V operating range.

We apply the proposed combined parameter extraction method on the measured PV module I-V curves. Significant reduction in root mean square (RMS) fitting error is observed compared with the conventional method which only considers some specific points.

First, we show the model accuracy improvement by the proposed characterization method. Table 5.3 shows the equivalent circuit model parameters introduced in Section 2.4.2 extracted by the conventional method and the proposed method, respectively. We apply these parameters to the PV model and derive the I-V curves shown in Figure 5.6(a). It shows the I-V curves obtained from the measurement compared with the I-V curves derived by the conventional and proposed characterization methods, for three different G values: 840,

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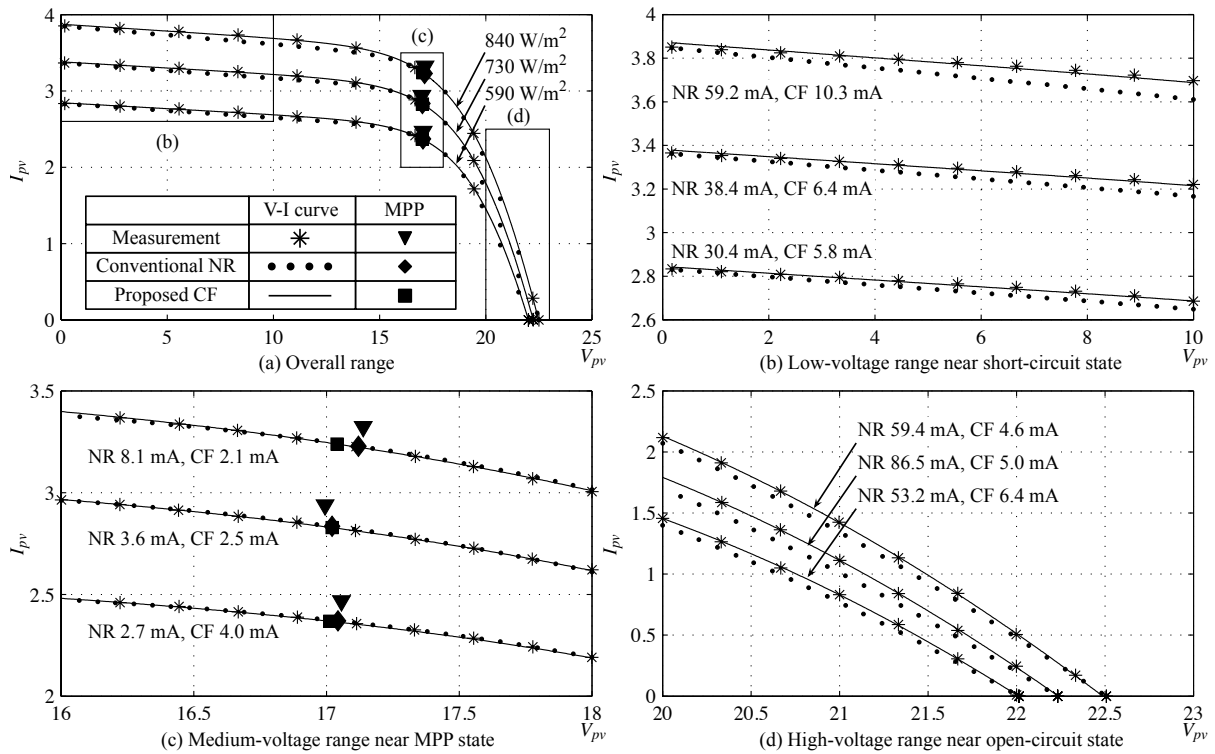
Figure 5.6: Model comparison with I-V curves in various irradiations. Numbers associated with curves denote the RMS error in each displayed voltage range. $T = 27\,^{\circ}$C.

730, and 590 W/m^2 at the same temperature $T = 27\,^{\circ}$C. We see that the proposed method extracts more accurate parameters than the conventional method does. Figs. 5.6(b), (c), and (d) provides a more detailed view of the curves, in a low-voltage range near short-circuit state, a medium-voltage range near the MPP state, and a high-voltage range near open-circuit state, respectively. The I-V curves derived by the proposed method are very close to the measured data, but the others derived by the conventional method have noticeable discrepancy.

Figure 5.6(c) shows an interesting result regarding the MPP. The MPPs derived by the conventional method are almost the same as the measured data. It is not surprising because

Table 5.3: Model parameters extracted by the conventional (NR) method and proposed (CF) method, and derived some V, I, and P compared with measured data (Meas.). $T_0 = 27\ ^\circ$C.

G_0	Parameters			Derived V (V), I (A), and P (W)			
	Value	NR	CF	Value	Meas.	NR	CF
	$I_L(G_0)$	4.66 mA	4.64 mA	V_{oc}	22.50	22.51	22.49
	$I_0(T_0)$	11.52 nA	11.52 μA	I_{sc}	3.85	3.85	3.87
840	R_s	689 mΩ	405 mΩ	V_{mpp}	17.14	17.12	17.04
	R_p	41.13 Ω	58.82 Ω	I_{mpp}	3.22	3.23	3.24
	N	37.00	57.08	P_{mpp}	55.25	55.25	55.19
	$I_L(G_0)$	4.68 mA	4.66 mA	V_{oc}	22.23	22.23	22.23
	$I_0(T_0)$	7.55 nA	6.98 μA	I_{sc}	3.37	3.36	3.38
730	R_s	761 mΩ	418 mΩ	V_{mpp}	16.99	17.02	17.02
	R_p	49.63 Ω	63.91 Ω	I_{mpp}	2.84	2.83	2.83
	N	36.00	54.86	P_{mpp}	48.24	48.25	48.14
	$I_L(G_0)$	4.87 mA	4.86 mA	V_{oc}	22.01	22.01	22.01
	$I_0(T_0)$	7.61 nA	2.03 μA	I_{sc}	2.83	2.83	2.84
590	R_s	776 mΩ	472 mΩ	V_{mpp}	17.06	17.04	17.01
	R_p	53.35 Ω	62.68 Ω	I_{mpp}	2.37	2.37	2.37
	N	36.00	50.28	P_{mpp}	40.38	40.39	40.29

what this method does is to fix V_{oc}, I_{sc}, V_{mpp}, and I_{mpp} as measured and find the parameters accordingly. This implies that the conventional method highly weights these points than other points. However, as mentioned earlier, not only the accuracy nearby the MPP, but overall accuracy across the whole I-V range should not be excluded when we explore the system in terms of energy efficiency. We do not weight any certain point or range of the I-V curve in the curve fitting, to enhance the overall accuracy. The MPP derived by the proposed method is slightly shifted from the measured data, but accuracy enhancement is observed in the entire range.

It is more clearly seen in Figure 5.7, which presents the relative and RMS errors of the derived I-V curves compared with the measured data. The curves show the relative error between the measured I_{pv} and modeled I_{pv} at $V_{pv} \in [0, V_{oc}]$ when $G_0 = 840$ W/m^2 and $T = 27$ °C. The bars indicate the RMS errors in ten uniform intervals of V_{pv}. The error rate of the proposed method is almost negligible when compared with the conventional method across the whole range of V_{pv}. It is noticeable that the error rate of the conventional method is small enough only nearby the MPP.

5.2.2 Dual-Mode Power Regulator with Power Hybridization

5.2.2.1 PV Module I-V Characteristics

Typical I-V characteristics of a PV module are shown in Figure 2.13. A PV module basically is a current source as shown in Figure 2.12, and forward biasing of the diode limits the output voltage which results in properties of a voltage source. An ideal PV module has a zero R_s and an infinite R_p, but a practical PV module has a non-zero R_s and a finite R_p. This non-ideal series and parallel resistances determine the gradients on the I-V curve. As mentioned above, the PV module exhibits dual behaviors which can be either a voltage source
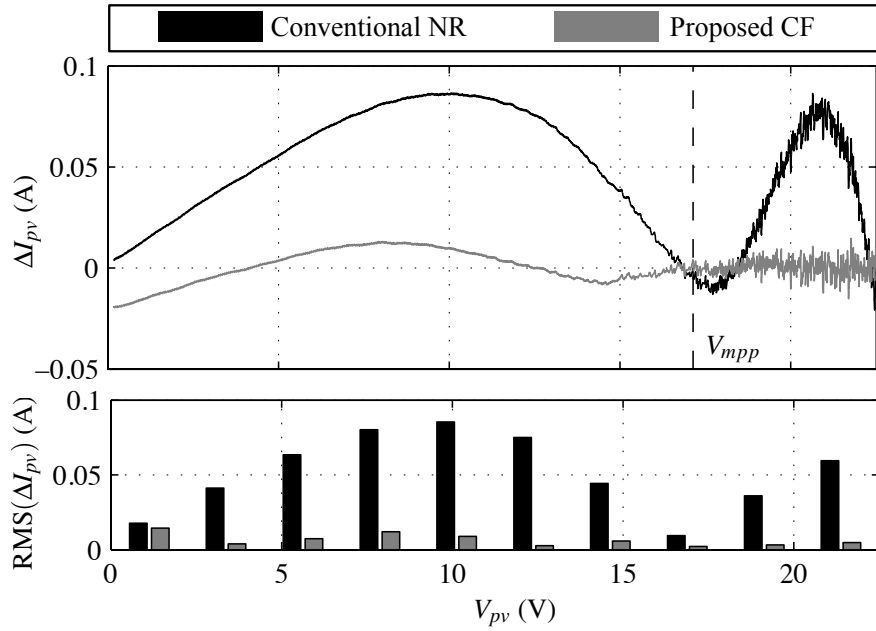
Figure 5.7: Model errors compared with the measured data. $G = 840$ W/m^2, and $T = 27$ °C.

or a current source depending on the operating range. More specifically, the PV module essentially behaves as a voltage source (i.e., it supplies a constant voltage regardless of the output current) when current is low and voltage is high, and behaves as a current source (i.e., it supplies a constant current regardless of the output voltage) when voltage is low and current is high. The boundary between the voltage source region (VSR) and current source region (CSR) is not very definitive, but reference [132, 133] defines it to be the MPP of the PV module.

Consequently, the PV module shows different output behavior even with the same amount of load power variation by its operation regions. Figure 5.8 illustrates how the load power variation affects the output of the PV emulator in the two different regions. The load power variation (①) results in a small voltage variation (②) and a large current variation (③) in the VSR. In contrast, the same amount of load power variation results in a small
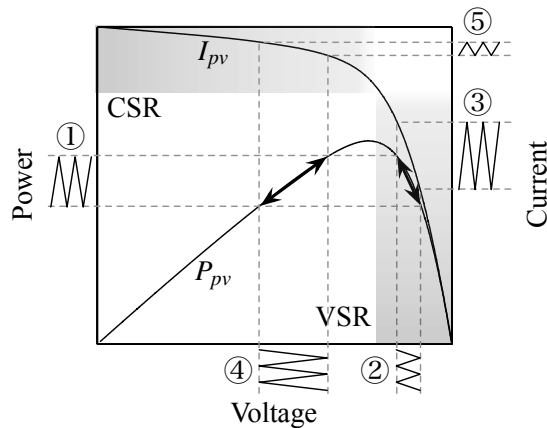
Figure 5.8: Voltage and current variations in the VSR and CSR.

current variation (⑤) and a large voltage variation (④) in the CSR. This implies that the PV emulators sorely based on a voltage regulator should be able to react to a small current change with a high feedback control gain in the CSR, which may result in instability in the VSR.

5.2.2.2 Modes of Operation

In spite of the dual characteristics of the PV module's output, previous PV emulators have relied on only a voltage regulator to reproduce the complete output I-V curve of the PV module. However, in the CSR, change in the output voltage of the PV module induced by the load impedance variation can be quite large. Under these conditions, current-based control provides a better control quality, and in turn, higher PV emulation accuracy in the CSR, in the same way that voltage-based control is preferred in the VSR. Nevertheless, we do not want to use a current regulator to reproduce the entire output I-V curve of the PV module because it may result in low accuracy in the VSR. Even if a nested feedback controller is used (e.g., an outer voltage control loop and an inner current control loop, or vice versa) [134, 135], the PV emulator will exhibit poor output controllability (and hence

poor emulation accuracy) in one or the other of the two regions of operation.

Therefore, in order to reproduce the original characteristics in both the VSR and CSR, we use two separate power sources [136]. In particular, we use a voltage regulator to generate a regulated voltage when the target PV module is operating in the VSR, and use a current regulator to generate regulated current in the CSR. We call the two operating modes of the dual-mode power regulator *voltage regulation mode (VRM)* and *current regulation mode (CRM)*. It is required to develop an elaborate power hybridization circuit which supports the VRM and CRM for the implementation of the PV emulator. A sophisticated control method also has to be designed in order to seamlessly switch between the two operating modes.

It is essential for a PV emulator to supply uninterrupted power to the load device, and so at least one of the voltage and current regulators should be turned on at all times. Instantaneously turning off the voltage regulator and turning on the current regulator, or vice versa, is not desirable because it tends to result in an instantaneous large current increase which causes current spikes. Furthermore, the power-on transient response is generally much worse than that of the set point change, and it is hard to realize seamless transition between two regulators. It is not practically feasible to turn on one regulator and turn off the other exactly at the same time, therefore we perform a make-before-break switching which has a period that both the regulators are turned on. However, different from ideal voltage and current sources, we should not simply tie up the outputs of the non-ideal voltage and current regulators because it may result in that current from the current source may flow into the voltage source. Practical voltage regulators do not allow reverse current which may cause hard failure in a power supply.
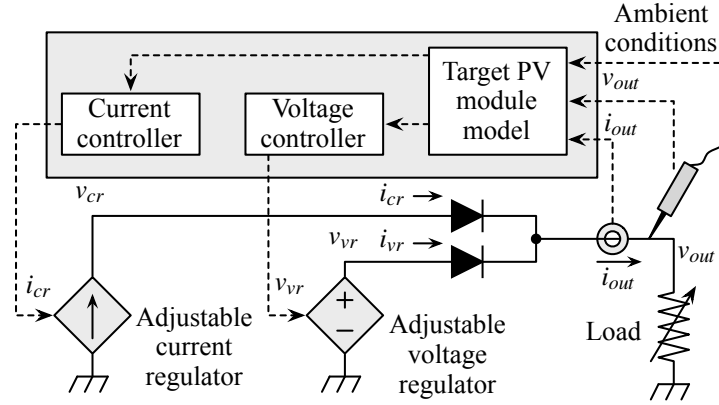
Figure 5.9: Architecture of the proposed dual-mode power regulator circuit for PV emulators.

5.2.2.3 Circuit Design Principle

We propose a dual-mode power regulator circuit for the model-based PV emulator as shown in Figure 5.9. It has adjustable voltage and current regulators whose outputs are tied together in parallel through two diodes. This parallel connection of diodes (or equivalently MOSFET-based lossless diodes) provides power hybridization preventing reverse current flow. This method has been used for power hot-swapping, and more recently, for hybridization of heterogeneous power sources [137], but has not yet been utilized for PV emulation.

The objective of the PV emulator is to make its output voltage V_{out} and output current I_{out} faithfully track V_{pv} and I_{pv}, which are derived from the PV module model. We switch the operation mode between the VRM and CRM near the boundary of the VSR and CSR. We first define a V-to-I mapping function and an I-to-V mapping function for the given I-V curve, based on (2.8) to (2.10). These functions translate V_{pv} to I_{pv} or vice versa, for given G and T.

Figure 5.10 shows three I-V curves of the target PV module model, the voltage regulator, and the current regulator. Here, the target PV module has a 17.5 V open-circuit voltage
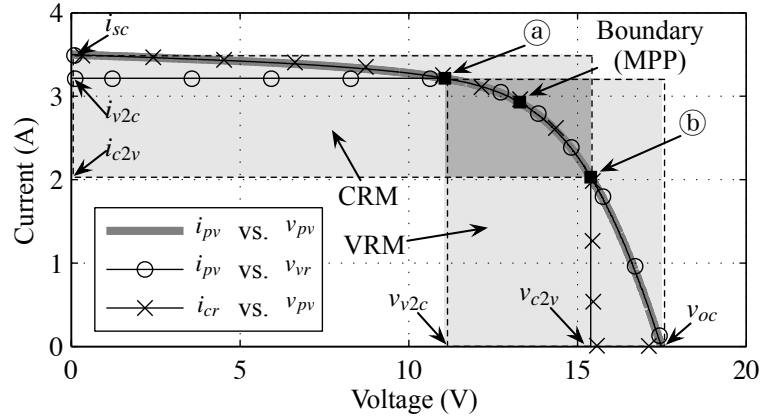
Figure 5.10: I-V characteristics of the dual-mode power regulators compared with the target PV module I-V curve.

(V_{oc}) and 3.5 A short-circuit current (I_{sc}). The voltage V_{mpp} and current I_{mpp} at the MPP are 13.3 V and 2.9 A, respectively. We define V_{v2c} and I_{v2c} to be the voltage and current when the operating mode changes from the VRM to CRM, respectively, and V_{c2v} and I_{c2v} to be the voltage and current when the operating mode changes from the CRM to VRM, respectively. Both the operating points (V_{v2c}, I_{v2c}) and (V_{c2v}, I_{c2v}) are on the I-V curve, for the given G and T. These values are considered as the voltage or current limits in each operating mode. That is, the PV emulator generates the maximum output current of I_{v2c} in the VRM, and generates the maximum output voltage of V_{c2v} in the CRM.

We make VRM and CRM overlap across the boundary as shown in Figure 5.10, and apply transition hysteresis. The transition hysteresis prevents frequent mode transitions between the VRM and CRM near the boundary. We make seamless transitions with the two-diode connection which allows make-before-break switching by blocking the reverse current. For example, when the operating mode switches from the VRM to CRM,

1. Keep the voltage regulator turned on and regulate output voltage V_{out} to V_{pv} while

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$I_{pv} < I_{v2c}$ (or equivalently, while $V_{pv} > V_{v2c}$).

2. If output current I_{out} increases and exceeds I_{v2c} (or equivalently, if V_{out} falls below V_{v2c}), turn on the current regulator (the transition point is annotated by ⓐ in Figure 5.10).

3. When the current from the current regulator I_{cr} reaches I_{out}, turn off the voltage regulator and regulate output current I_{out} to I_{pv}.

The opposite is done when the operating mode switches from the CRM to VRM at ⓑ in Figure 5.10; the voltage regulator is turned on first and current regulator is turned off later when the output current decreases. Both the voltage and current regulators maintain good controllability and thus high-quality output near the boundary, compared with the operating points far away from the boundary. Therefore, the proposed power hybridization and its control scheme guarantees smooth mode transition and guarantees superior output quality over the entire emulation range.

5.2.2.4 Dual-Mode Power Regulator Control

Figure 5.11 shows a control system block diagram of the proposed dual-mode power regulator circuit. It has two separate feedback control loops for the voltage and current regulators. The voltage and current regulators are coupled with each other such that their output V_{out} and I_{out} are located on the given I-V curve of the target PV module. The V-to-I and I-to-V mapping functions in Figure 5.11, which are derived from the PV module model, handle the dual-mode operation.

The output behavior of the two-diode connection is such that its output voltage is either of the higher one between the two input voltages, and only the one with the higher voltage supplies the current. If two voltages are the same, the output current is the sum of the

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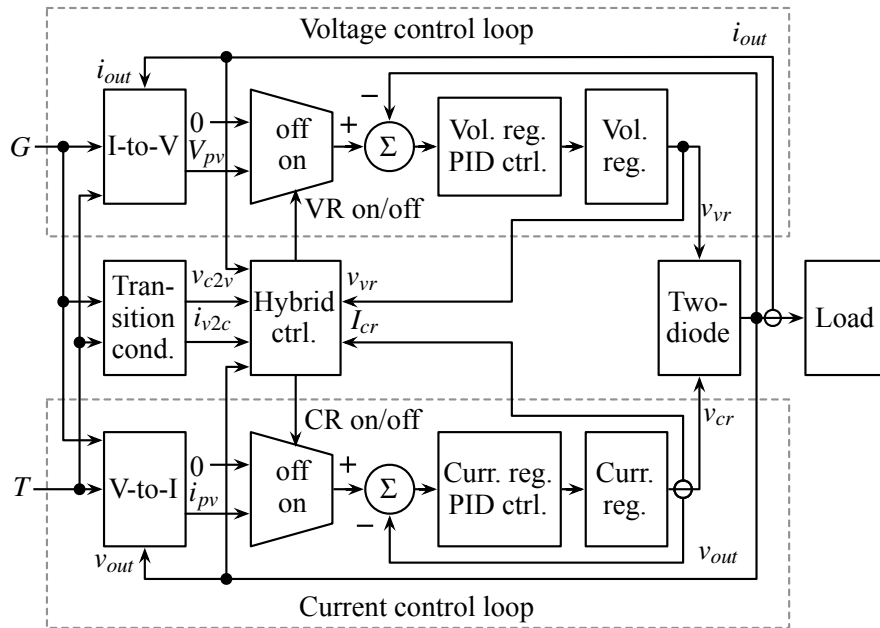
Figure 5.11: Dual-mode power regulator control system block diagram.

two input currents. The voltage and current control loop regulates voltage and current at different points. The current control loop regulates I_{cr}, and the voltage regulator control loop regulates V_{out} in order to compensate the voltage drop across the diode.

The hybridization controller ('Hybrid ctrl.' in Figure 5.11) is in charge of such seamless transition of the operating mode between the VRM and CRM by the load demand. The controller takes six inputs: V_{c2v}, I_{v2c}, V_{out}, I_{out}, V_{vr}, and I_{cr}, and it generates two outputs: on/off signals for the voltage and current regulators. The operating mode transition point, V_{c2v} and I_{v2c}, are derived by the transition condition block ('Transition cond.' in Figure 5.11). Figure 5.12 shows the functionality and behavior of the hybridization controller with a state machine. The state machine has four states: the VRM, CRM, and two intermediate states between them. The output current, I_{out}, exceeding the limit of I_{v2c} makes transition from the VRM state. This results in that the current regulator is turned on and supplies current.
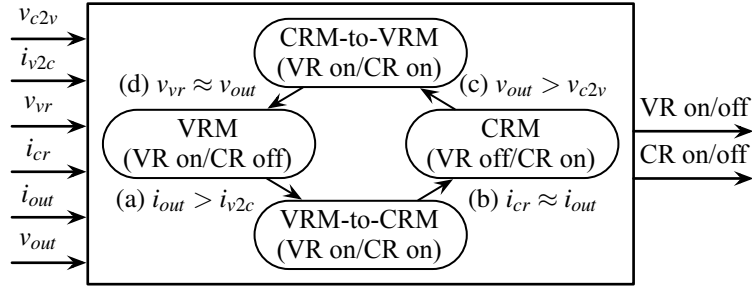
Figure 5.12: State transitions and conditions of the hybridization controller. (VR: voltage regulator, CR: current regulator)

If its output current I_{cr} becomes equal to I_{out}, that is, the voltage regulator does not supply current anymore, the state machine makes a transition to the CRM state and turns off the voltage regulator. The state machine makes transition from the CRM to VRM states in the same way. We consider the distance and position of the boundary between the VRM and CRM (ⓐ and ⓑ in Figure 5.10) and determine the voltage/current limit V_{c2v} and I_{v2c}. The PV emulator will switch the mode too frequently if the gap is too narrow. On the other hand, the benefit from using the dual-mode power regulator is diminished if we expand the overlapping region and the gap becomes too wide.

5.2.2.5 Implementation

Figure 5.13 shows the implemented dual-mode regulator-based PV emulator board. Figure 5.14 shows the circuit schematic diagram of the proposed PV emulator. We use a low dropout (LDO) linear regulator LT1083 from Linear Technology as the voltage regulator. Switching regulators have a higher efficiency in general, but they are inherently subject to switching noise and voltage ripples even the load is constant. Since a PV module does not create any noisy ripples on its voltage and current, we use a linear regulator for the voltage source to eliminate them.
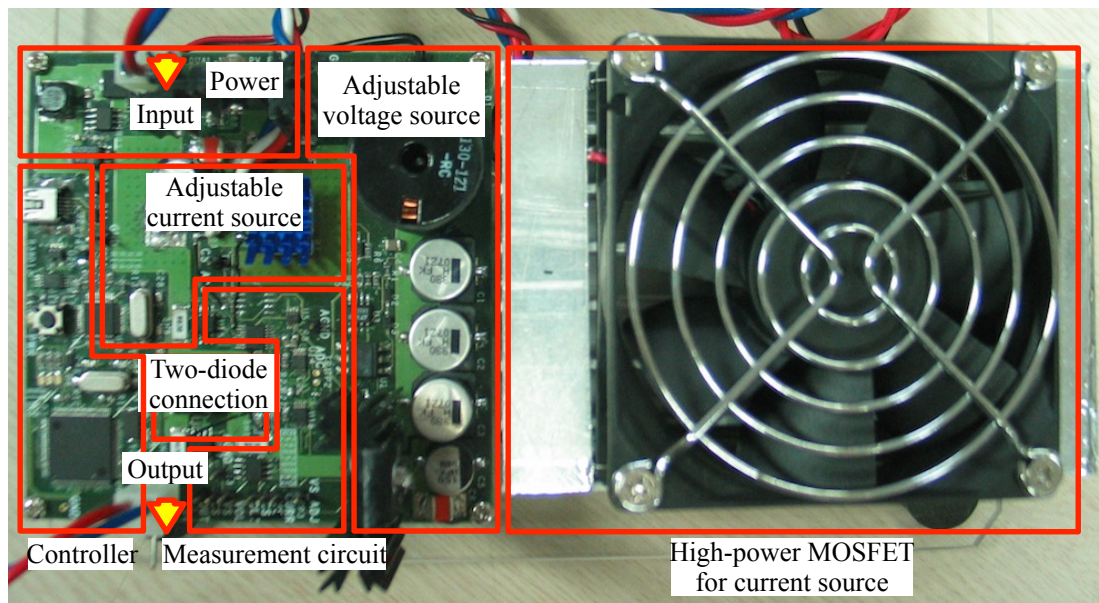
Figure 5.13: Implemented dual-mode regulator-based PV emulator board.
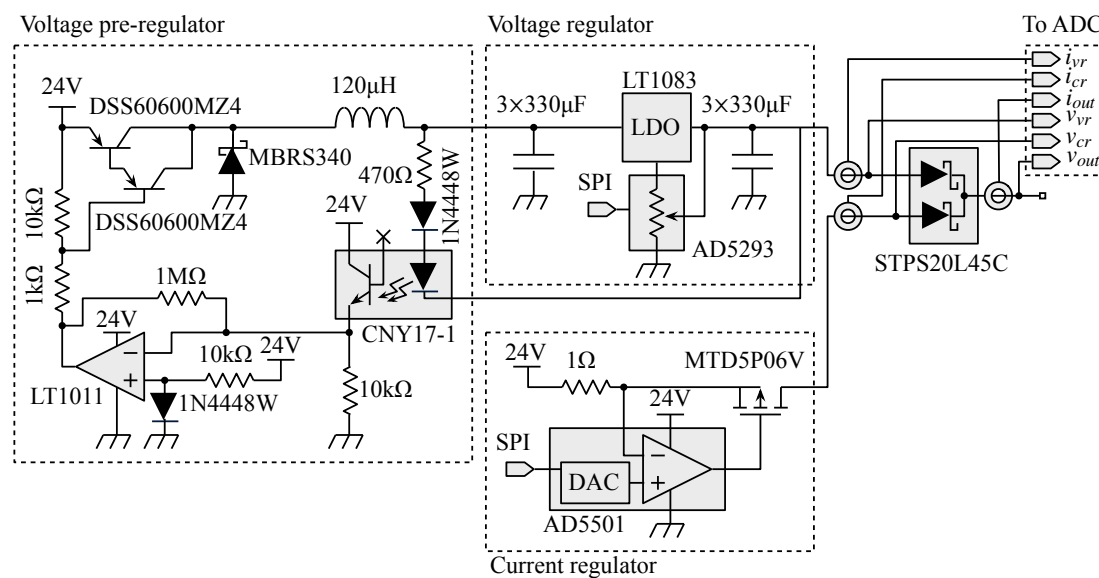
Figure 5.14: Circuit schematic diagram of the PV emulator design.

Power dissipated in a linear regulator is proportional to the dropout (voltage difference between the input and output). The dropout may be large in a wide output-adjustable regulator, and this results in a high heat dissipation. We implement a voltage pre-regulating circuit [138] for the input of the linear regulator to mitigate the heat dissipation. It automatically adjusts the input voltage to be higher that the output voltage by the required minimum dropout to minimize the heat dissipation, and allows a large amount of current from the linear regulator. The implemented voltage regulator is capable of supplying 1.2–21.8 V of output voltage with 12-bit resolution and up to 5.0 A of output current. However, the proposed dual-mode regulator architecture is not restricted to which type of regulator is used. We may use a high-efficiency switching regulator instead of the linear regulator as the voltage/current source to reduce its power dissipation for high-power PV emulation.

We implement a precision 10-bit resolution current regulator introduced in [139] for the current regulator also with the LT1083. The maximum available output current is 5.0 A up to 16.5 V, and it decreases as the output voltage increases up to 19.5 V. This does not limit the power capacity of the emulator since the current regulator generates a high current in the CRM where the voltage is low.

Due to the physical constraints of the components, the PV emulator's output voltage and current cannot span unlimitedly. Table 5.4 shows the voltage and current output ranges of the regulators. The range of operation of the regulators while performing the emulation is dependent not only on their physical capability, but also the I-V characteristic of emulating PV module. That is, the minimum output voltage that the voltage regulator generates is V_{v2c}, and the minimum output current that the current regulator generates is I_{c2v}, which vary depending on the target of emulation, as illustrated in Figure 5.10.

The two regulators are connected through a Schottky diode array STPS20L45C from STMicroelectronics. It has a forward voltage drop in a range of 0.4–0.6 V varying depend-

Table 5.4: Output specification of the implemented PV emulator. All values are measured at the output terminal.

Regulator	Output	Conditions	Min.	Max.	Unit
Voltage regulator	Voltage	$I_{out} = 2.0$ A	1.2	21.8	V
	Current	$V_{out} = 10.0$ V	-	5.0	A
	Power	$V_{out} = 21.8$ V $I_{out} = 5.0$ A	-	109.0	W
Current regulator	Voltage	$I_{out} = 2.0$ A	-	19.5	V
	Current	$V_{out} = 10.0$ V	0.0	5.0	A
	Power	$V_{out} = 16.5$ V $I_{out} = 5.0$ A	-	82.5	W

ing on the temperature and forward current. It is described in the datasheet that the diode will have around 0.3 W of conduction loss at 1 A forward current due to the on-resistance. Therefore, we compensate the voltage drop and resulting power loss through a feedback control as discussed in Section 5.2.2.4.

The controller is Stellaris LM3S3748 microprocessor with ARM Corex-M3 core running at 50 MHz. We use a real-time operating system μC-OS II to implement the controller described in Section 5.2.2.4. The control task performs proportional-integral-derivative (PID) control at 1 kHz frequency. PID parameters are critical for fast response and stable operation of the PID controller to disturbances. We carefully set the PID parameters so that the voltage and current regulators have a fast response to the load variation and generate stable voltage and current output. We perform PID parameter tuning through extensive experiments and apply gain scheduling to achieve the best performance for the voltage and
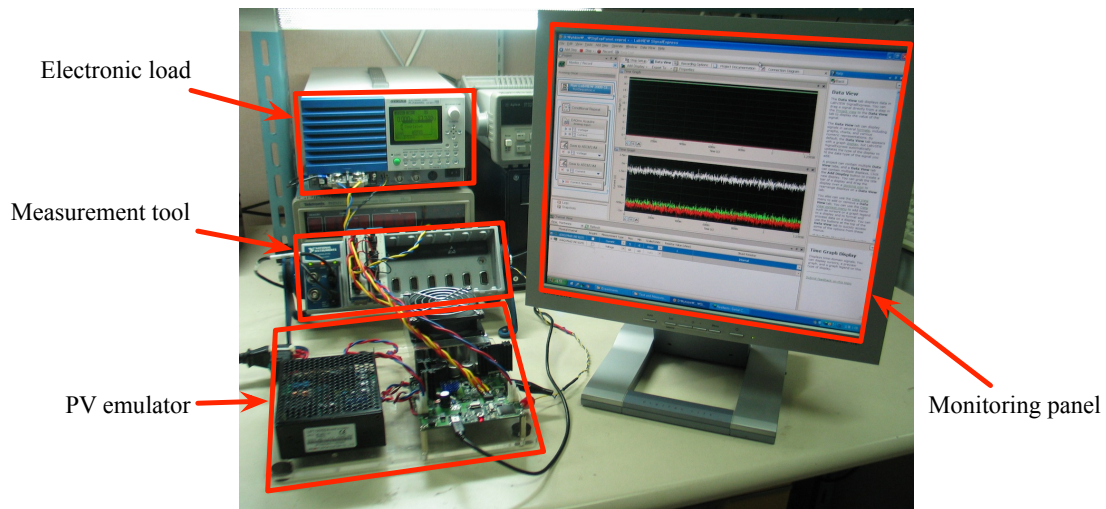
Figure 5.15: Experimental setup.

current regulators. The gain scheduling adjusts the PID parameters depending on the operation range in order to cope with the non-linear behavior. We divide the operation range into several subranges and tune the PID parameters for each subrange.

5.2.2.6 Experiments

We setup experimental environment as shown in Figure 5.15. The implemented PV emulator is connected to the adjustable electronic load Kikusui PLZ334WL which can consume up to 300 W of power. The currents and voltages of the regulators and output are measured with a DAQ from the National Instruments. All the system including the PV emulator, electronic load, and DAQ is controlled by a customized automated tool.

PV module I-V characteristics   We first measure the output of the target PV module to compare the voltage and current variations in the VRM and CRM. Table 5.5 is the voltage and current variations of the target PV module caused by load power variations in the VRM and CRM. Refer to Figure 5.8 which graphically illustrates the voltage and current

Table 5.5: Voltage and current variations by the load power variation of 40–60% of the maximum power at 1000 and 500 W/m^2.

G (W/m^2)	Region	Output	Marker in Figure 5.8	Range	Δ_{norm} (%)
1000	VSR	Voltage	②	16.2–16.7 V	2.9
		Current	③	0.93–1.44 A	14.6
	CSR	Voltage	④	4.5–6.9 V	13.7
		Current	⑤	3.38–3.43 A	1.4
500	VSR	Voltage	②	15.7–16.2 V	2.9
		Current	③	0.47–0.72 A	14.3
	CSR	Voltage	④	4.4–6.7 V	13.5
		Current	⑤	1.69–1.71 A	1.1

variations caused by the power variation. We measure the voltage variation (② and ④) and current variation (③ and ⑤) while changing the load power (①) in a range of 40–60% of the maximum power for the given irradiance. Table 5.5 presents the range of voltage and current variations in each region and the normalized value Δ_{norm} to the maximum voltage and maximum current, which are V_{oc} and I_{sc}, respectively. This definitely shows that using an appropriate power regulator results in only 1–3% output variations, otherwise it suffers from 13–15% output variations. This phenomenon becomes more clear when the operating point is near the maximum voltage (open-circuit) or maximum current (short-circuit). This confirms the dual characteristic of the PV module and shows the potential benefits of using two different regulators for PV emulation.

Matlab/Simulink simulation   We first validate the functionality of the proposed circuit and the control method with Matalb/Simulink simulation. Through the simulation, we show that the proposed circuit well performs the PV emulation, and present the resulting voltage, current, and power behavior. We use adjustable voltage and current regulator models, diode models, and resistive load models from the Matlab/Simulink Simscape library. Without loss of generality, we use a pre-measured PV module I-V curve at a given irradiance level and temperature for demonstration purpose.

First, we define the transition conditions in Figure 5.12. We define I_{v2c} in (a) and V_{c2v} in (c) as follows:

$$I_{v2c} = \quad (V_{mpp} + V_{oc})/2, \tag{5.7}$$

$$V_{c2v} = \quad (I_{mpp} + I_{sc})/2. \tag{5.8}$$

We consider that $V_{vr} \approx V_{out}$ in (b) and $I_{cr} \approx I_{out}$ in (d) when the error is less than 0.1%. These conditions are empirically determined based on the observation on the I-V curve of the target PV module.

Figure 5.16 shows the I-V curves, P-V curves, and P-I curves of the PV module model, voltage regulator, current regulator, and emulator output. Figures 5.16(a) and (b) show the two cases such that the operating point changes in two different directions, respectively, which are denoted by a gray arrow. It demonstrates the hybridization controller described in Section 5.2.2.4 is functioning as expected. The operating mode transition occurs when the output voltage reaches to V_{v2c} in the VRM in Figure 5.16(a) or when the output current reaches to I_{c2v} in the CRM in Figure 5.16(b). We see from the I-V curves that the voltage output of the voltage and current regulators is higher than V_{pv} (shifted to higher than V_{pv}) as a result of the feedback control to compensate the diode forward bias voltage drop of 0.6 V and the diode on-resistance of 0.3 Ω. In spite of the steep I-V curve at the transition, the

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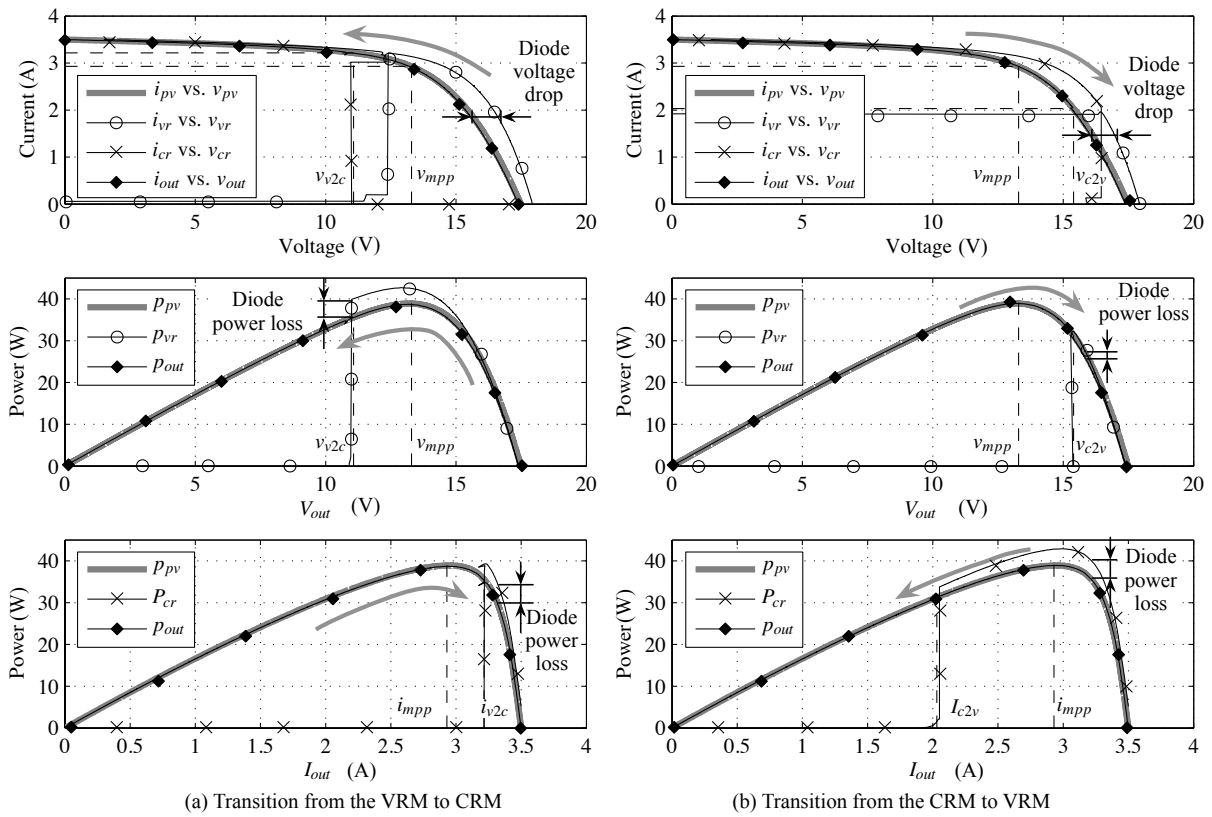
Figure 5.16: I-V, P-V, and P-I curves of the voltage regulator, current regulator, and emulator output, compare with the PV module model while transiting (a) from the VRM to CRM, and (b) from the CRM to VRM.

resultant PV emulator output I-V characteristic well matches with that of the PV module model thanks to the use of two-diode hybridization circuit and control.

I-V characteristics   Now that we have validated the functionality through simulation, we present the measurement results obtained from the physical experiments. We show the output quality of the proposed PV emulator compared with two conventional voltage or current regulator-based PV emulators. We turn off the current or voltage regulator to generate the output of voltage regulator-based PV emulator or current regulator-based emulator,

respectively.

Figures 5.17(a), (b), and (c) show the I-V curves measured from the three PV emulators based on the voltage regulator, current regulator, and dual-mode regulator, respectively. We measure the voltage and current while changing the load from the with period of 30 seconds. The load changes between zero (open circuit) to the value that makes the output 2 V, which is close to the minimum output voltage described in Table 5.4. In each figure, the solid line denotes the desired output I-V characteristic according to the PV module model, and the markers denote the measured points.

In Figure 5.17(a) and Figure 5.17(b), it is definite that the output of the regulators are not as expected in some operating range. More specifically, the voltage regulator fails to generate the desired voltage in the CSR as annotated by ⓐ. Similarly, the current regulator fails to generate the desired current in the VSR as annotated by ⓑ. This is not because the regulators are not capable of generating high power in those regions, but because the output voltage or current variation is too rapid for the regulator to follow the output change. The power output capability of the regulators is enough to generate the voltage and current on the target I-V curves as presented in Table 5.4. For example, the voltage regulator can stably supply up to 5 A at 10 V, but the I-V curve of 500 W/m^2 in Figure 5.17(a) shows unstable output at low current and low voltage range below 1.8 A and 7 V. In contrast, the output of the dual-mode regulator is in a good quality as shown in Figure 5.17(c). The output in the VSR is as good as that of the voltage regulator-based emulator, and the output in the CSR is as good as that of the current regulator-based emulator.

In practice, a load device connected to a PV module is not only a resistance-mode load, but may be a voltage-mode, current-mode, or combination of them. Therefore, we show that the proposed dual-mode PV emulator shows a good stability over all operating range not only for the resistance-mode load as shown in Figure 5.17(c), but also for voltage- and
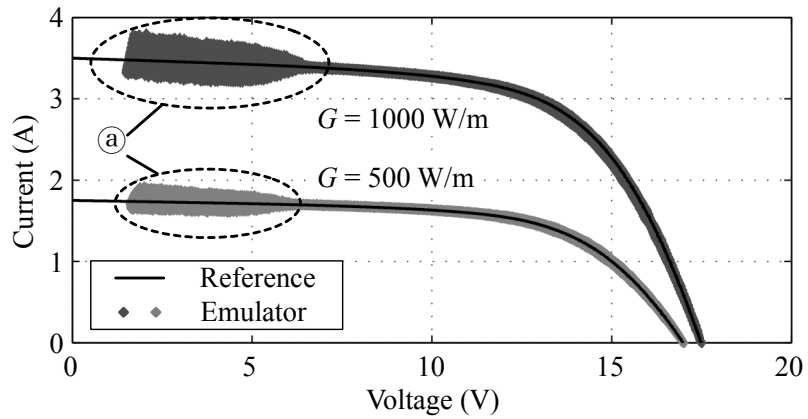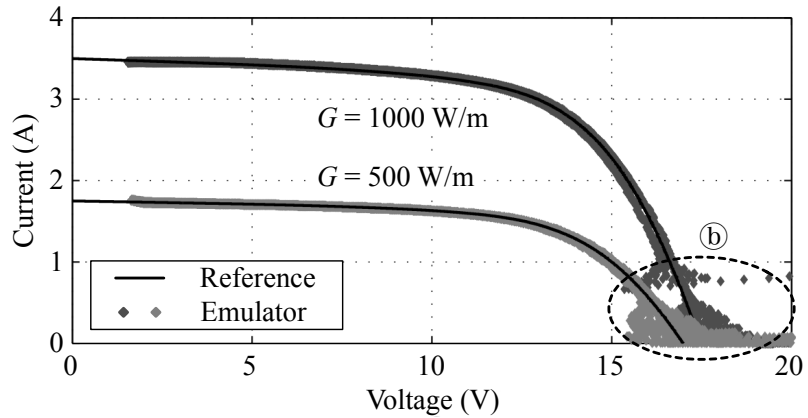
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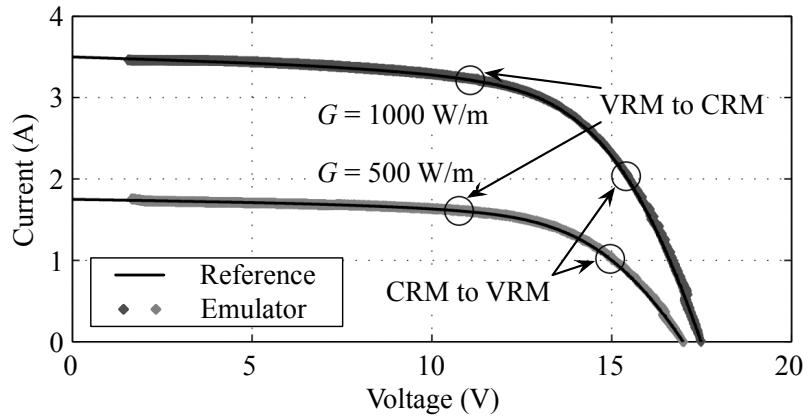
Figure 5.17: I-V curves of PV emulation based on three regulators: (a) voltage regulator, (b) current regulator, and (c) dual-mode regulator.
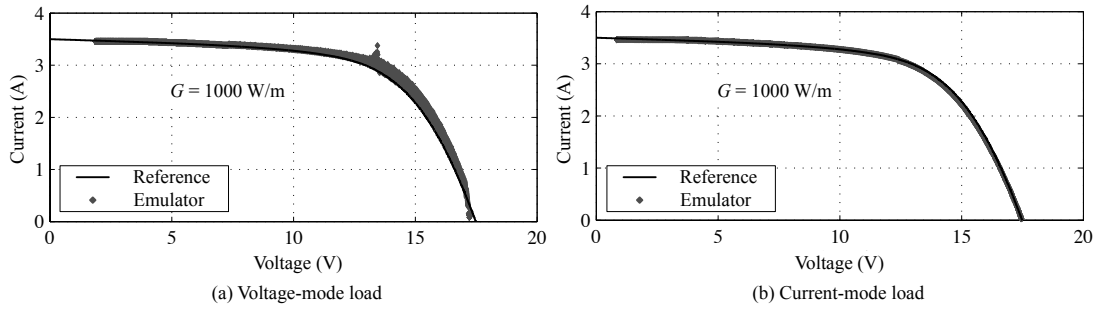
Figure 5.18: I-V curves of PV emulation for (a) a voltage-mode load, and (b) a current-mode load.

current-mode loads. Figures 5.18(a) and (b) show I-V curves when a voltage- and current-mode load is applied, respectively. We can see that both I-V curves for the voltage- and current-mode loads exhibit good consistency with the reference I-V curve.

Mode transitions Figure 5.19 shows the voltage and current output variations of the voltage regulator, current regulator, and emulator output when the load changes. This is a representation of the data in Figure 5.17(c) in a time axis. We apply a variable load starting from a zero load (open-circuit) to a very low resistance load (near short-circuit), and back to a zero load.

It starts in the VRM state because the load is zero. Current draw increases, and at t_1, the output current I_{out} reaches I_{v2c} which is the current limit of the voltage regulator. The operating mode changes from the VRM to VRM-to-CRM state, in which I_{cr} gradually increases, and I_{vr} gradually decreases. Finally, I_{cr} reaches to I_{out} at t_2, and the voltage regulator is turned off, by entering the CRM state. We see that the operating mode transition is seamlessly performed, and the output voltage V_{out} and current I_{out} are stably maintained during the transition. The hybrid controller performs the opposite when the operation mode changes from the CRM to VRM. The output voltage V_{out} increases and current I_{out} de-

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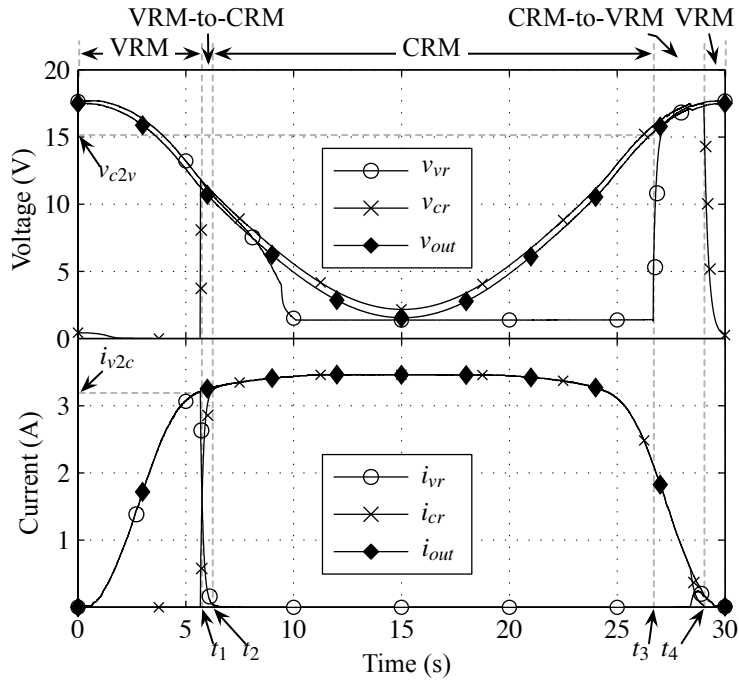
Figure 5.19: Output of the voltage and current regulators for varying load.

creases until it reaches V_{c2v} at t_3. The controller enters the CRM-to-VRM state and the voltage regulator is turned on. When the output voltage of the voltage regulator reaches V_{out} at t_4, the current regulator is turned off by entering the VRM state.

Next, we show the PV emulator's transient response to a step load change. A PV emulator should be able to change its operating point rapidly when the load changes. Due to the control hysteresis, the same operating point can be regulated by either voltage or current regulator, especially near the MPP. Therefore, we apply a step change of the load resistance and observe the voltage and current variations [133]. The step response of the voltage regulator and current regulator is shown in Figures 5.20(a) and (b), respectively. The MPP is at 2.9 A and 13.3 A, which corresponds to 4.5 Ω. The load resistance is first 8.3 Ω and the PV emulator output is 1.9 A at 15.6 V. We decrease the resistance to 4.0 Ω and the operating point changes to 3.1 A at 12.4 V. Both the voltage and current converters to the desired

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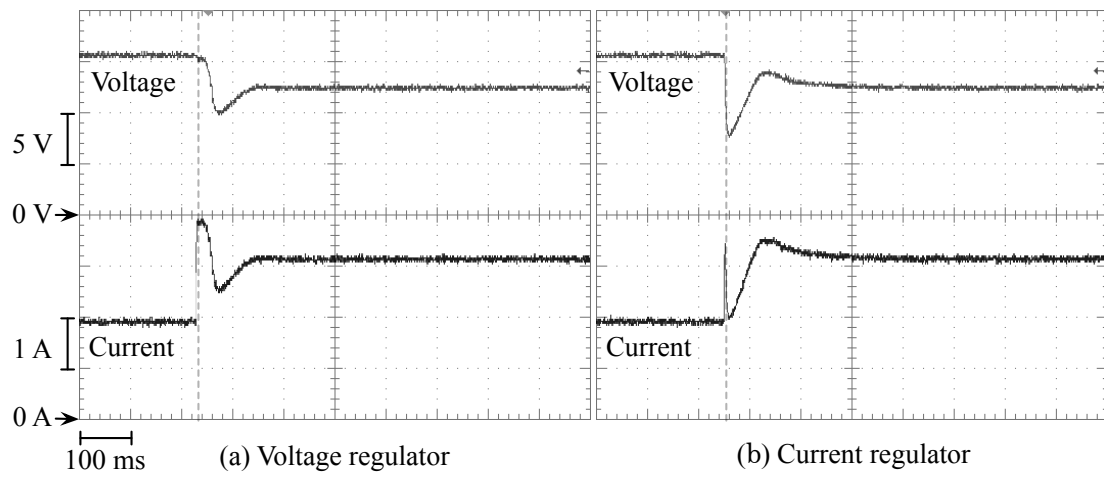
Figure 5.20: Voltage and current variance for step change of load resistance from 8.3 Ω to 4.0 Ω.

operating point within about 100 ms.

Chapter 6

Experiments

6.1 HEV Application

We present an example that the proposed HEES system design and operation optimization methods applied to a HEV. The HEES application is easy to see the benefit of the high energy efficiency by directly converting into fuel cost reduction. Figure 6.1 shows the components of a HEV. It is equipped with both a conventional combustion engine and an electrical traction motor. The regenerative brake produces electrical energy when braking. Photovoltaic (PV) modules installed on the roof and bonnet also produces energy from the solar irradiance. The energy generated by the regenerative brake and PV modules are stored in the energy storage, and used later to operate the traction motor for acceleration.

The baseline for comparison is a battery-only EES system without reconfiguration. The battery has 375 V output voltage and 53 kWh energy capacity. The PV modules generates 100 W maximum power in total and perform MPPT to generate maximum power from the PV modules. All the electrical devices, traction motor, regenerative brake, energy storage, and PV modules, are connected through a shared bus CTI. We improve the HEV by apply-
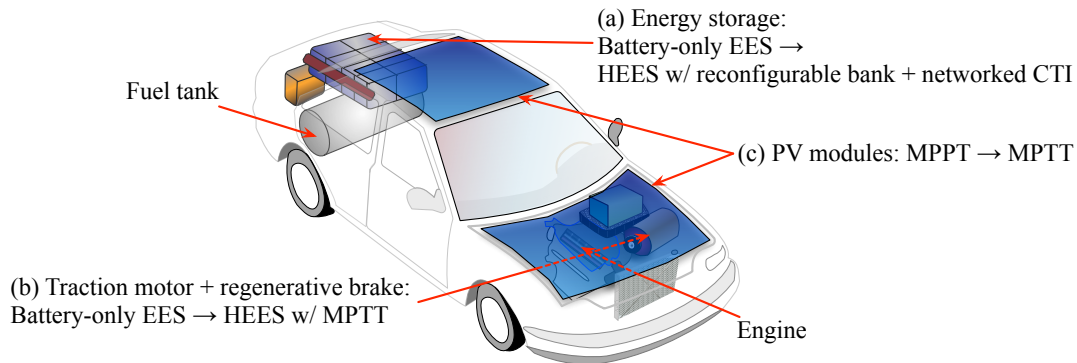
Figure 6.1: A HEV with PV modules. Energy storage, motor/brake, and solar modules are applied the proposed optimization methods.

ing the proposed HEES system design and operation methods. We make HEES system by adding a supercapacitor bank composed of 140 cells which has 1,200 F capacity each. Figure 6.2 illustrates the power flow among the components. The following sections introduce how the proposed optimization methods improves the energy efficiency in the HEV in each component by comparing with the baseline HEV.

6.1.1 Regenerative Brake

We increase energy recovery form the regenerative brake by hybrid use of the supercapacitor bank with the battery bank. We also apply the MPTT to further increase the energy efficiency. Power density of batteries are not so high that they are not suitable for handling intermittent high power demand. The regenerative brake produces a very large amount of power for a short duration, and so a battery-only EES system suffers from low energy efficiency due to the poor rate-capability. Hybrid use of supercapacitor bank greatly improves
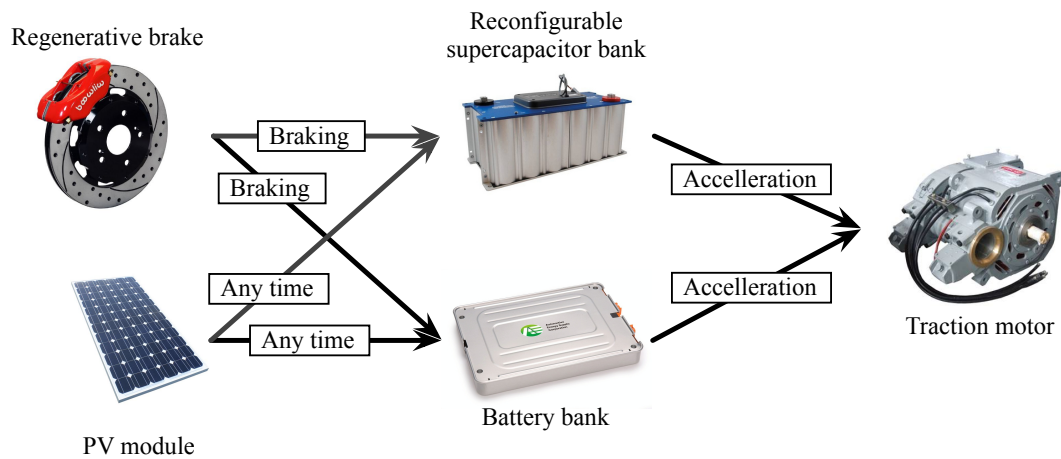
Figure 6.2: Power flow among components.

the energy efficiency, and thus recovers more energy. While the amount of current charged into the battery in a EES system is directly determined by the energy generation from the regenerative brake, having a battery-supercapacitor HEES system incurs charge allocation problem to determine the amount of current to each bank.

We determine the current distribution between the battery and supercapacitor based on the charge allocation policy proposed in [140]. This policy determines the current distribution so that the amount of total recovered energy is maximized. The energy is not evenly distributed between the battery and supercapacitor because they have different rate capability. Also, the current distribution changes over time depending on the input from the regenerative brake changes. We also apply the proposed MPTT operational method to the power converters in the battery bank and supercapacitor bank. Figure 6.3 shows the power output from the regenerative brake and power input to the battery and supercapacitor banks. The HEV reduces its velocity from 70 km/h to 0 km/h for about 4 seconds. The battery voltage is 375 V and initial supercapacitor voltage is 252 V. This is a case that the power conversion efficiency between the brake and supercapacitor is high thanks to similar
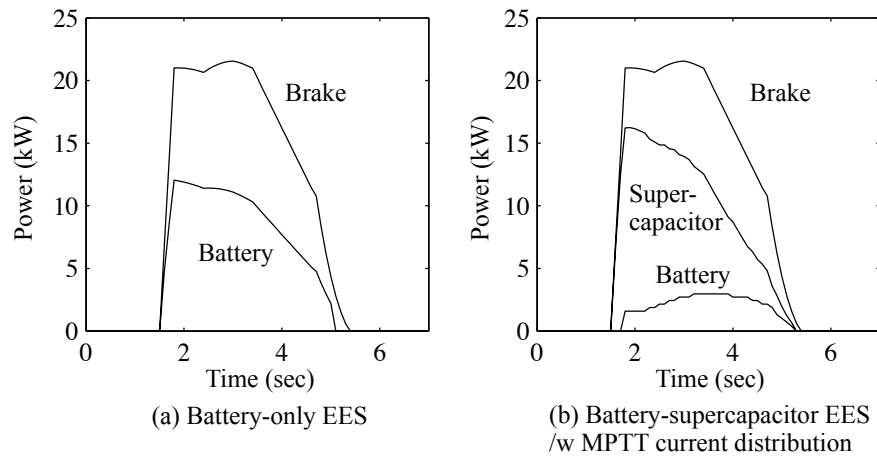
Figure 6.3: Power output from the brake and power input to the battery and supercapacitor banks while braking.

voltage levels. Amount of recovered energy with the battery-supercapacitor HEES system is 49% higher than the battery-only EES system. The improvement varies depending on the supercapacitor voltage. Assuming uniform probability of supercapacitor voltage, the additional energy recovery per one braking operation is about 3.1 Wh on average.

6.1.2 PV Modules

We increase power generation by applying the proposed MPTT method to the 100 W the PV modules. Figure 6.4 shows that energy harvesting increases by the proposed MPTT operation compared with the conventional MPPT operation. The MPTT operation maximizes the current output from the converter. Assuming uniform probability of supercapacitor voltage and irradiance level, the additional energy harvesting is 0.9 Wh per hour on average.
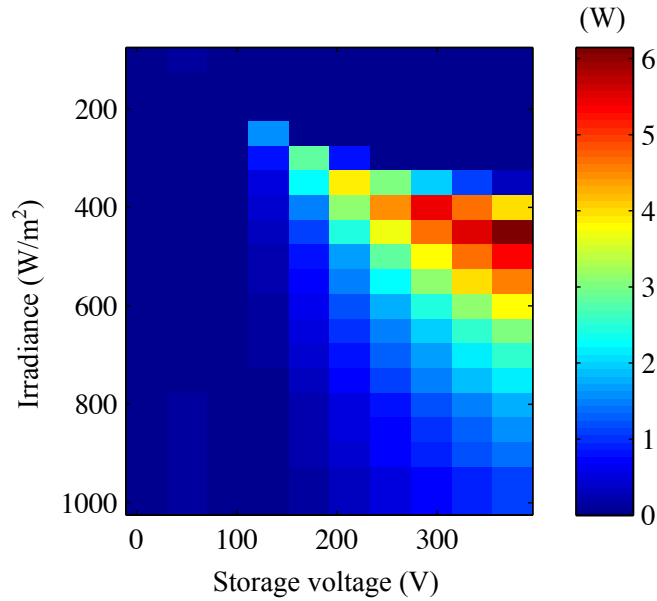
Figure 6.4: Additional energy harvesting by applying MPTT compared with MPPT.

6.1.3 EES Bank Reconfiguration and Networked CTI

We demonstrate energy efficiency improvement by the proposed EES bank reconfiguration and networked CTI architecture. We reconfigure the supercapacitor bank so that the power charged into the supercapacitor bank is maximized when it is charged by the regenerative brake and PV modules. We make a sequence of charge transfers tasks to the network CTI design problem based on the improvement described in Sections 6.1.1 and 6.1.2. The vehicle accelerates using the energy in the supercapacitor bank firstly. It uses energy in the battery bank if the energy is not enough. Both the acceleration and braking take 4 seconds each. Between the acceleration and braking, the vehicle cruises (maintains the constant velocity) for 1 minute using the combustion engine only. We assume that the solar irradiance level is 750 W/m^2.

Figure 6.5 shows the CTI architecture and connectivity of the baseline HEV and the proposed HEV. The baseline HEV uses a single shared-bus CTI as shown in Figure 6.5(a)

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(a) Battery-only homogeneous EES with shared bus CTI (baseline)

(b) Battery-supercapacitor HEES with networked CTI (connectivity as shown)
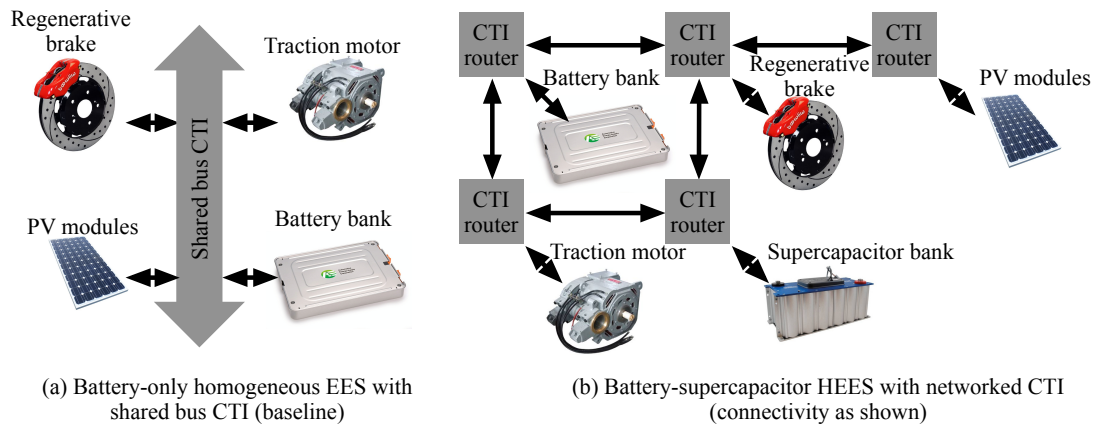
Figure 6.5: CTI architecture and connectivity of the baseline shared-bus CTI and proposed networked CTI.

to connect four nodes. The charge transfer efficiency in this shared-bus architecture is 46%. The proposed HEV has five nodes (a supercapacitor bank is added) and they are connected though a networked CTI. The node placement algorithm introduced in Section 4.2.4 derives the optimal connectivity as shown in Figure 6.5(b). The charge transfer efficiency in this networked CTI architecture is improved 51%. The charge transfer efficiency slightly further increases to 53% if we apply EES bank reconfiguration for the supercapacitor bank so that it maintains the best configuration for the PV and reintegrative brake.

6.1.4 Overall Improvement and Cost Analysis

Figure 6.6 shows contributions of each design and optimization methods to the energy efficiency improvement. The total energy gain per cycle is 3.7 Wh with the usage scenario described in Section 6.1.3. Majority of energy gain, which is as high as 82.1%, comes from the MPTT operation of the regenerative brake with the networked CTI battery-supercapacitor HEES system. Dynamic supercapacitor bank reconfiguration achieves additional 7.0% more energy gain from the regenerative brake. Energy gain from the PV
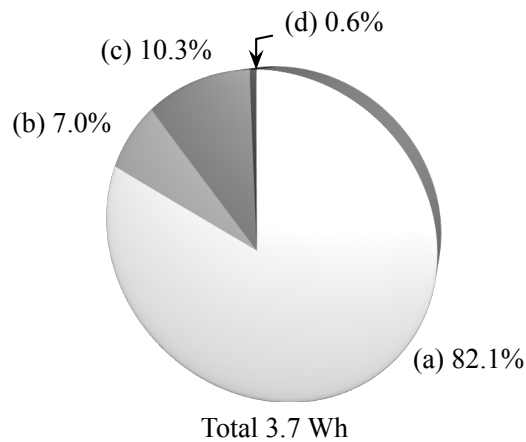
(a) MPTT regenerative braking with networked CTI
(b) MPTT regenerative braking with bank reconfiguration
(c) MPTT solar energy harvesting with networked CTI
(d) MPTT solar energy harvesting with bank reconfiguration

Figure 6.6: Energy recovery/harvesting gain per cycle.

modules is improved by 10.3% and 0.6% by the networked CTI and supercapacitor bank reconfiguration, respectively. The energy gain from the regenerative brake becomes significant as the acceleration and braking cycles become more frequent.

6.2 HEES Prototype Implementation

We discuss the HEES system prototype implementation in this section. The HEES prototype is aiming at household applications though the design framework is not bounded to a particular scale. The HEES system is connected to the power grid to store electrical energy during non-peak hours and becomes auxiliary power source to mitigate the peak power demand. There are five nodes which includes three heterogeneous EES banks, one power grid input, and one AC power outlet, which are connected through a shared-bus CTI. There are three EES banks such as 6.5 Wh supercapacitor, 115 Wh lithium-ion battery, and

163 Wh lead-acid battery banks. The HEES system provides a high degree of freedom to transfer energy between the nodes at a high efficiency by continuous update of the current and voltage of each EES bank and CTI.

The HEES system mandates elaborate management policies because the energy flow in the HEES is much more complicated than conventional heterogeneous type EES systems. It may suffer from a very low energy efficiency unless we perform intelligent management with consideration of characterizations of EES elements (IR loss, rate capacity effect, leakage, etc.). While most previous electric energy storage research focused on storage elements, we emphasize that power converters play an important role in the HEES system. HEES system energy efficiency is heavily dependent on the input and output voltage and current of power converters. It is crucial to maintain the power converter operating point close to the most efficient region. The charger board proposed this dissertation consists of a wide-range programmable bidirectional charger and a microcontroller with Control Area Network (CAN) interface. We have shown that proper determination of voltages and currents of each EES bank and CTI increases energy efficiency of the HEES system and introduced system-level management policies including charge allocation [107], charge replacement [108], and charge migration [109, 110]. We implement the management algorithms in the main controller that communicates with the charger boards through CAN.

6.2.1 Design Specifications

We describe the design specification of the HEES prototype implementation. We design a HEES system for load leveling and peak shaving of residential electricity usage. The specification of the HEES system in this section is for the proof-of-concept purpose. That is, the architecture and control method are highly scalable and flexible so that they can be applied to smaller and larger scale HEES systems with various types of EES elements,

power sources, and load devices.

6.2.1.1 Power Input and Output

The input to the HEES system is 120 V AC, and the output is 120 V AC. The proposed HEES system is transparent to both the power grid and load devices; it is seen as an ordinary AC-powered appliance to the power grid, while it is a AC power outlet to the load devices.

6.2.1.2 Power and Energy Capacity

We set the power capacity of the HEES system to 300 W. This is reasonable power capacity for load leveling and peak shaving purposes considering that the average residential electric usage ranges 0.4–1 kW over time [141]. All the EES banks are designed to meet this power capacity at least. We set the total energy capacity of the HEES system as small as 300 Wh for shorten time of charging and discharging the system for experimental purpose. Nevertheless, the energy capacity may be easily increased by extending the EES array or adding more EES banks.

6.2.1.3 Voltage and Current Ratings

Maximum power efficiency is available with proper operational range of voltage and current. Typically, power converters with hundreds of kW power capacity are designed with a DC voltage range of 12–48 V and and maximum current of 5–20 A. Commercial DC–DC converters with symmetric input and output voltage ranges have such voltage and current ratings typically. AC–DC rectifiers and DC–AC inverters have similar voltage and current ratings for the DC side. We set the maximum current to 10 A for each power converter. We design the power converters accordingly, and the voltage range covers a much wider range of 6–36 V for voltage variation of the supercapacitors and CTI.

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6.2.1.4 EES Elements

We use three types of EES elements in the proposed HEES system prototype: supercapacitor, lithium-ion battery and lead-acid battery. The supercapacitor has advantages in power capacity cycle life, and cycle efficiency, while the lead-acid battery has advantages in cost. The lithium-ion battery has moderately good characteristics all round, except for the cost. We do not consider other types of EES elements such as kinetic or thermal storages, but the proposed HEES system does not restrict types of EES elements fundamentally.

6.2.2 Implementation

We discuss the implementation of the HEES system prototype in this section. We especially focus on showing that the implementation satisfies the specifications of Section 6.2.1 with consideration on the design goals of Section 3.1. We achieve the goal of the high modularity of the HEES system by modular implementation of the HEES system. The modular design makes it easier to develop and modify EES bank individually and manipulate the system-level configurations. Figure 6.7 shows modules of the proposed HEES system composed of three EES bank modules, controller and converter module, and CTI capacitor module. The following subsections describe design and implementation of the modules and their subcomponents, justifying the design goals and specifications.

6.2.2.1 Bank Module

The proposed HEES system has three EES banks: a supercapacitor bank, a lithium-ion battery bank, and a lead-acid battery bank. Figure 6.8(a) shows the supercapacitor bank module viewed from the front and back assembled in a 19-inch rack case. There is an EES array composed of 18 supercapacitors inside the rack case, and a bidirectional charger is
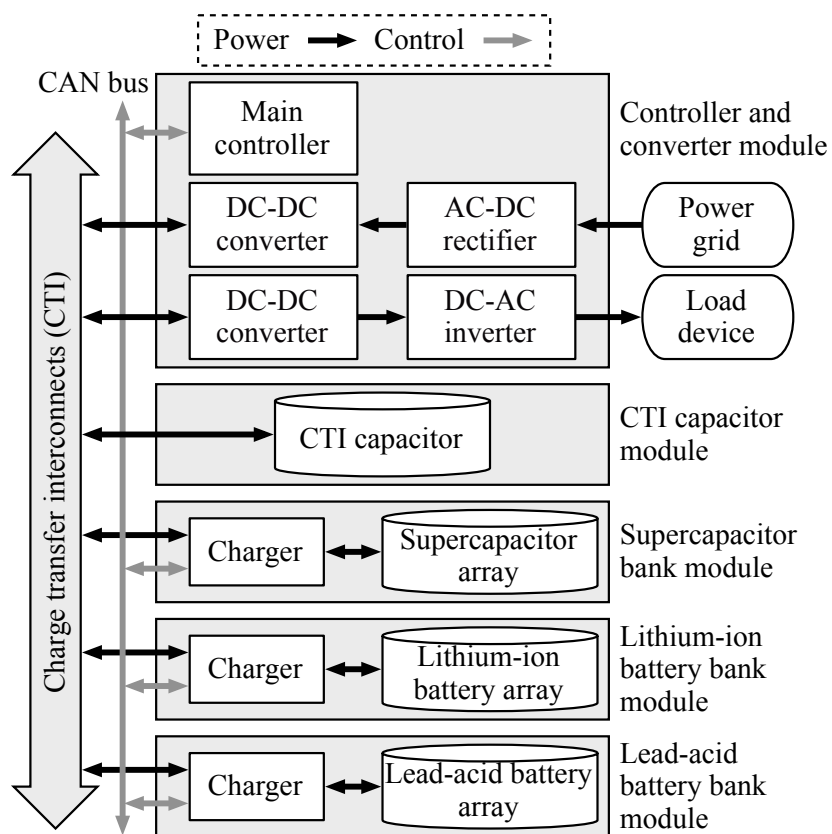
Figure 6.7: Architecture of the proposed HEES system.

(a) Supercapacitor bank (Front and back)

(b) Controller and converter module

(c) CTI capacitor module
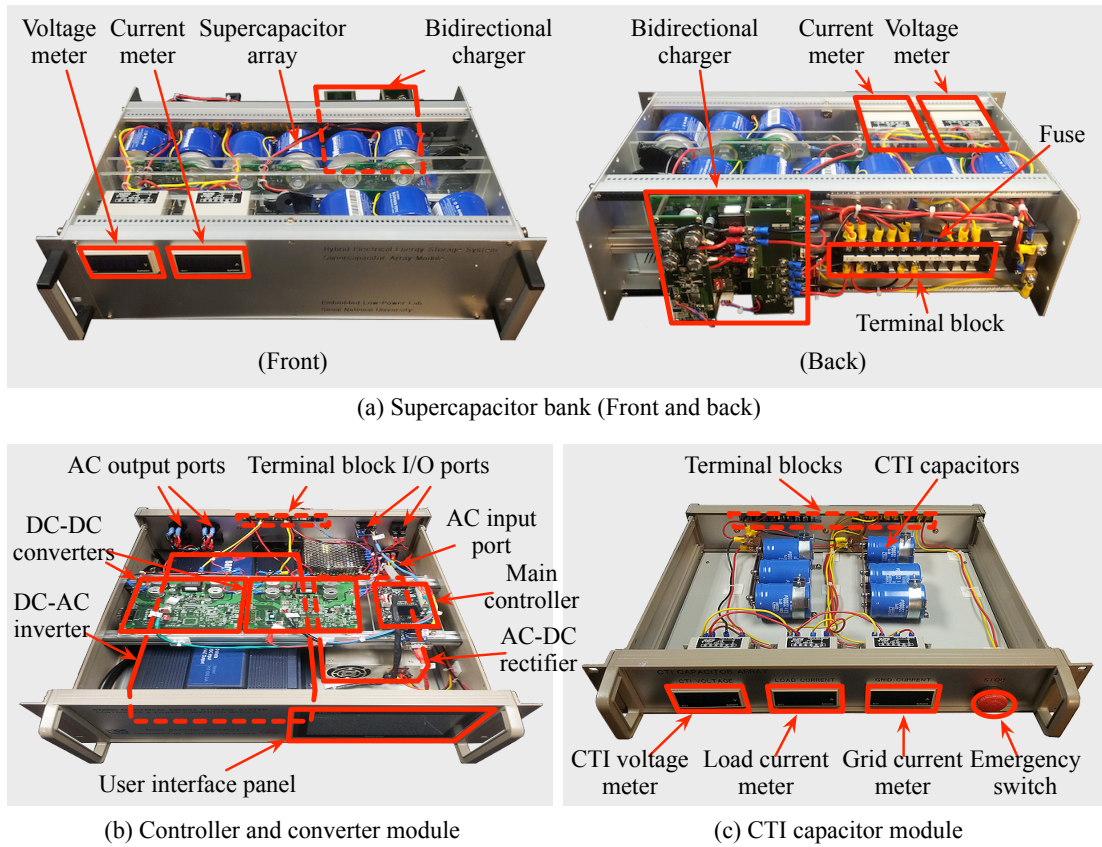
Figure 6.8: Modules of the proposed HEES system.

attached to the back of the module together with terminal blocks. The voltage and current meters on the front panel display the voltage and current of the EES array. We put a fuse to prevent excess current flow between the bank and CTI that may cause damage to the array or charger. The lithium-ion battery module bank and the lead-acid battery bank module also have a similar structure. Composition each EES bank module is summarized in Table 6.1.

The EES bank implementation in a 19-inch rack case as a module is for scalability and modularity of the system. Design of each EES bank is independent to each other. All the EES banks have the uniform interface regardless the EES elements. It has a DC power port to the CTI, a communication network port, and a power input port for the bidirectional

Table 6.1: Composition of EES banks.

Parameter		Supercapacitor	Lithium-ion battery	Lead-acid battery
	Cell	Maxwell BCAP0650	Samsung ICR18650-26F	Panasonic LC-R123R4P
Unit cell	Voltage	2.7 V (max)	3.7 V	12 V
	Capacity	650 F	2,600 mAh	3,400 mAh
	Energy	0.66 Wh	9.6 Wh	40.8 Wh
	Cost	$69/Wh	$3/Wh	$1/Wh
Configuration	Series	18	6	2
	Parallel	1	2	2
Bank	Voltage	48.6 V (max)	22.2 V	24.0 V
	Energy	6.3 Wh	115 Wh	163 Wh

charger. Therefore, changing the configuration of an EES bank module or adding/removing a module is simple and has limited influence to the whole system.

Supercapacitor bank We use 18 cells of Maxwell BCAP0650 supercapacitor connected in series to compose the supercapacitor bank [142]. Each cell has 650 F capacity with maximum voltage of 2.7 V, and so 18-series connection makes a 36 F supercapacitor array of maximum voltage of 48.6 V. The primary advantage of the supercapacitors is the extra long cycle life. The datasheet states that it has a cycle life of 1,000,000 cycles. The maximum energy stored in the supercapacitor array is 11.8 Wh when the charged to 48.6 V. Actual maximum energy capacity we utilize is 6.3 Wh because we limit the terminal voltage of the supercapacitor array within 6–36 V as specified in Section 6.2.1. Cost per energy of the supercapacitor is about $69/Wh based on the retail price for purchasing single cell, which is much more costly than that of batteries by an order of magnitude.

Lithium-ion battery bank We compose the lithium-ion battery bank with 12 cells of Samsung ICR18650-26F [143]. Each cell has 2,600 mAh capacity and nominal voltage of 3.7 V. We arrange the 12 cells into a $6{\times}2$ array which give us 22.2 V nominal voltage and 115 Wh energy capacity. The number of series connection is determined to make the nominal voltage be placed in the middle of voltage range of 6–36 V in order to mitigate power efficiency degradation which may be caused by voltage difference between the battery array and CTI. The total energy capacity is chosen to be small so as to shorten the time for experiments as we mentioned in Section 6.2.1. In fact, the rack case has a plenty of room for additional batteries.

Lead-acid battery bank The lead-acid battery bank consists of four Panasonic LC-R123R4P batteries [144]. Each battery is composed of six series cells which make nominal

voltage of 12.0 V. We make a 2×2 array to obtain a terminal voltage of 24.0 V. The lead-acid battery bank has the largest energy capacity thanks to its low cost, which is only $1/Wh based on the retail price for purchasing a single battery. The total energy capacity of the lead-acid battery bank is also set small for fast experiments.

6.2.2.2 Controller and Converter Module

The controller and converter module performs functionalities of system supervision and AC conversions (AC-to-DC and DC-to-AC conversions). The system supervision is conducted by the main controller which is implemented with a Texas Instruments LM3S2965 microcontroller running at 50 MHz. The microcontroller runs Micrium μC-OS II real-time operating system (RTOS) and monitoring, control, communication tasks on top of it. The microcontroller provides an enough computing power for simple control policies with real-time control loops, as well as connectivity to the PC with much more powerful computing capability for more elaborated control policies.

The main controller communicates with subsystems of the HEES systems at 1 Hz–1 kHz frequency depending on the data. It with the bidirectional chargers through the CAN bus for monitoring and control of the EES banks. We adopt CAN bus for the communication network within the HEES system. The CAN bus is a widely-used industrial standard for system control, and supports multi-master communication with up to 1 Mbit/s bit rate within tens of meters range. It provides a high scalability for multiple subsystems to be connected through the network that is hard to achieve with other types of communication networks. The data transfer between an EES bank and the main controller is less than 10 kbyte/s (1 byte = 8 bits), and so 1 Mbit/s bit rate is more than enough for the HEES system with small number of EES banks. The main controller also communicates with the user interface panel which provides useful information such as voltage and current of each

EES bank, CTI, and power grid. In addition, the main controller can be connected to a PC so that the user can monitor and control the HEES system manually. We discuss the software design for the main controller and the bidirectional charger in Section 6.2.2.4 in more detail.

The controller and converter module also performs both AC-to-DC conversion from the power grid to the CTI and DC-to-AC conversion from the CTI to the AC load devices. Since our focus is on the system design of the HEES system, not power converter circuit design, we use commercial high-efficiency AC converters rather than designing custom AC converters. We use the Mean Well SE-600 600 W AC–DC rectifier [145]. We need an adjustable output voltage in order to dynamically change the CTI voltage, but it generates a 36 V fixed output voltage. Therefore, between the AC–DC rectifier and the CTI, we implement a DC–DC converter which accepts 36 V input voltage and generates an adjustable wide output voltage for the CTI. The power converter connection is shown in Figure 6.7. The output voltage level of the DC–DC converter is controlled by the main controller.

We use Samlex PST-100S-24A 1000 W pure sine wave DC–AC inverter [146]. In contrast to the AC–DC rectifier, the DC–AC inverter is required to accept wide input voltage of 6 to 36 V of the CTI, but typical commercial inverters designed for batteries do not support such a wide input range. The PST-100S-24A is operational only for 21.4 to 33 V input, and the nominal input voltage is 24 V. Therefore, similar to the AC–DC rectifier, we implement a DC–DC converter which accepts 6–36 V input voltage and generates 24 V fixed output voltage.

Figure 6.8(b) is a photo of the converter and controller module. It shows the main controller, AC–DC rectifier, DC–AC inverter, and DC–DC converters inside. The back panel of this module is populated with AC and DC power ports and digital I/O ports (RS232, CAN, user switch, etc.).

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6.2.2.3 Charge Transfer Interconnect Capacitor Module

The proposed HEES system has five EES nodes including three EES banks, AC input, and AC output. The maximum number of possible simultaneous independent charge transfers among the five EES nodes is only two. Therefore, we employ the shared-bus architecture to the HEES system for simplicity among several CTI architectures, which is shown in Figure 2.8(c).

The CTI is positioned in the middle of power converters as the input or output of them, and so a sufficient amount of bulk capacitors is required to secure voltage stability in order to cope with large transient current variations. The power converters have limited capability to deal with sudden changes of the load current, which may result in rapid changes of the CTI voltage unless the CTI has enough energy buffer. Maintaining a desired CTI voltage level is important because non-optimal CTI voltage leads to degraded power conversion efficiency of the power converters. What makes the problem worse is that the CTI voltage drop may violate the minimum input voltage requirement of power converters and result in system failure.

We implement the energy buffer for the CTI with an array of large-capacitance aluminum capacitors. Figure 6.8(c) is a photo of the CTI capacitor module. We connect six of United Chemi-Con 22,000 μF aluminum capacitors in parallel to compose the CTI capacitor array. The total 132,000 μF capacitance is proven by experiments to be sufficient to maintain a stable voltage against 300 W load increase when charged over 25 V. The main controller determines the CTI voltage level with considerations on the energy efficiency of the charge transfers and predicted load demand. The CTI capacitor module has one voltage meter and two current meters on the front panel to show the CTI voltage, current from CTI to the load devices, and current from the power grid to the CTI. The emergency switch is

also placed on the front panel to cut off the main power to inactivate all the power paths manually in case of emergency.

6.2.2.4 Bidirectional Charger

The charger design is a key for the HEES system to achieve high efficiency and high reliability. It has integrated functionalities of a DC–DC converter, battery charger, and battery monitor. This is similar to conventional battery management systems, but provides more high-level functionalities for the HEES system management by being integrated with the main controller and other chargers. Specifically, the bidirectional charger implemented for the proposed HEES system has the following features:

- Bidirectional conversion: It is capable of charging the EES array from the CTI, as well as discharging the EES array to the CTI.

- Voltage and current regulation: It generates either a regulated voltage or regulated current. When it is charging the EES array, this is necessary to perform the constant-current and constant-voltage (CC-CV) charging. When it is discharging the EES array, this is necessary either for maintaining the CTI voltage or injecting designated amount of current into the CTI.

- Adjustable output regulation: The output voltage or current can be adjusted dynamically. The output voltage is determined by the EES array maximum voltage (when charging), or the desired CTI voltage (when discharging). The output current is determined by the main controller considering efficiency and reliability.

- Wide operational range: The terminal voltage of the EES arrays changes depending on their SoC, especially for supercapacitor array whose voltage is linearly proportional to the SoC. The CTI voltage also changes in a wide range for energy efficiency

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(a) Implemented charger   (b) Power path of the charger
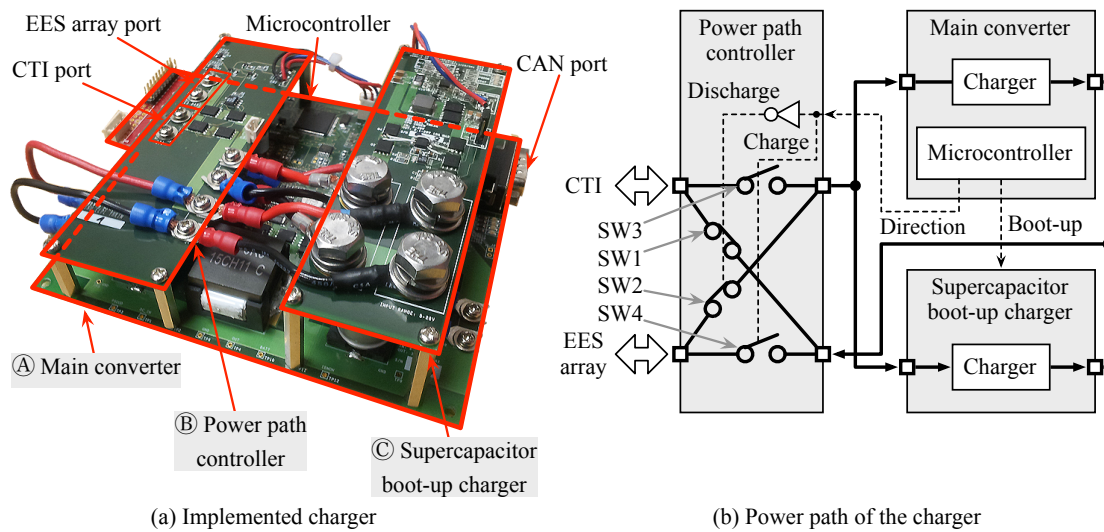
Figure 6.9: Implemented charger and the power path of the charger.

and reliability. Therefore, the charger has a wide input and output voltage range of 6–36 V.

- Board-to-board communication: It reports the current status of the bank to the main controller and receives operational commands from the main controller through the CAN bus.

Figure 6.9(a) shows the charger implemented for the proposed HEES system. The charger is composed of three parts: main converter (Ⓐ), power path controller (Ⓑ), and supercapacitor boot-up charger (Ⓒ). It is powered from a separated power rail, not from the CTI, for reliable operation of the system. Figure 6.10 shows the conversion efficiency of the main converter for different input and output voltage at 0.5 A and 1.5 A load current.

The main converter performs unidirectional adjustable voltage or current regulation with wide input/output voltage (6–36 V) and high-current (up to 10 A). The converter circuit uses a combination of the LTC3789 DC–DC converter [147] and the LTC4000 power management IC [148] from Linear Technology. The LTC4000 is originally designed to

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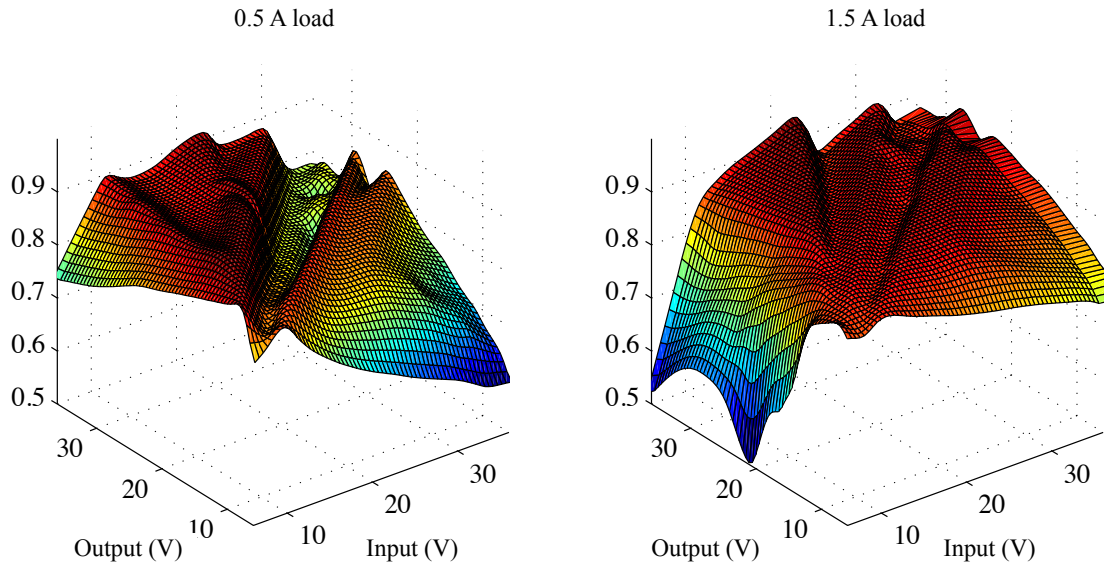
Figure 6.10: Efficiency of the main converter.

generate a fixed voltage or fixed current for charging battery from the wall power. We modify the voltage and current feedback loops with digital potentiometers to make them dynamically adjustable from the microcontroller. We use the Texas Instruments LM3S2965 microcontroller to control the charger as for the main controller. The charger has a CAN bus interface to communicate with the main controller as well.

The power path controller swaps the input and output of the main converter as needed to enable bidirectional power conversion. When charging the EES bank, the input is the CTI and the output is the EES array; and when discharging the EES bank, it is the opposite. We use four solid-state relays made of a pair of MOSFET switches to dynamically change the input and output as shown in Figure 6.9(b). Two solid-state relays are coupled as a pair and opened or closed together, and the two pairs are exclusively closed. For example, the microcontroller closes SW1 and SW2 are closed and opens SW3 and SW4 as shown in Figure 6.9(b) when charging. We implement a hardware protection circuit on the power

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path controller to prevent short circuit from the CTI and EES array by control flaws or signal glitches.

The supercapacitor boot-up charger is added to the charger for the supercapacitor bank module only. It is a fixed current buck mode switching charger made of the BQ24640 supercapacitor charger IC from Texas Instruments. The supercapacitor terminal voltage is linearly proportional to its SoC, different from the batteries that maintain relatively a constant terminal voltage regardless its SoC. Even though the main controller manages the terminal voltage of the supercapacitor array within the operational range of the main controller, sometimes we may have an under-voltage due to intended discharge (supercapacitor replacement) or unintended discharge (self-discharge). We use the boot-up charger to charge the supercapacitor array up to the minimum voltage level of 6 V that the main converter can handle in such cases.

The HEES systems has multiple chargers, one per each EES bank. We connect all the chargers through the CAN bus together with the main controller in order to perform systematic control of the HEES system. The chargers send voltage and current measurement results to the main controller through the communication network, and receive commands determined by the main controller based on the system management policies.

6.2.2.5 Supervising Control Software

The main controller and bidirectional chargers run μC-OS II RTOS to perform system management and EES bank management, respectively. The main controller mainly performs supervisory tasks for global HEES system management such as the charge management, while the chargers perform individual control of the EES bank. Figure 6.11 shows the block diagram of the control software implemented in the main controller and chargers.

The main controller is in charge of determining the CTI voltage and current of each EES
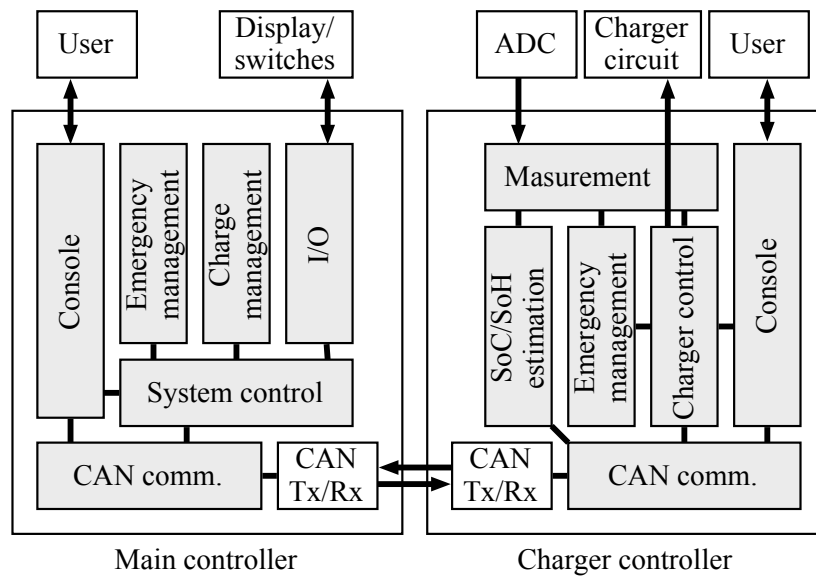
Figure 6.11: Design of the main controller and charger controller. Lines between tasks denote inter-task communication.

bank for high energy efficiency and reliability. We implement the charge management task in the main controller to determine the optimal values [107, 108, 109, 110]. The decision is made based on many parameters including voltage, current and SoC of the EES banks and load demand prediction. We do not cover the optimization methods minutely in this dissertation. The system control task makes the overall decision on energy flow of each EES node based on decisions of other tasks.

The charger is in charge of measuring the status of the EES bank and controlling the power conversion. The measurement task measures the voltage/current of the input/output of the power converter. The SoC/SoH estimation task calculates the SoC and SoH based on the measured voltage and current profiles. The converter control task changes the voltage/current regulation feedback loops according to the commands from the main controller.

There are also some common tasks implemented in both the main controller and charg-

ers. The CAN communication tasks collect messages from other tasks and deliver them over the CAN network layer periodically or on demand. Critical messages related with the main controller's decision (e.g., measured voltage/current and control commands) are delivered periodically with a high priority; while slowly changing values (e.g., SoC and SoH) are delivered upon request with a low priority. The console task provides manual control interface to the user which overrides the automated control. The emergency management task has a highest priority to detect abnormal status and shut-down all power paths and power converters in the system. The console task is for communication with the user for monitoring and manual control.

6.2.2.6 Component Assembly

Figure 6.12 shows the front and back views of the HEES system assembled in a 19-inch rack. Dimension of the whole system is 60 (W)×65 (L)×96 (H) cm (23.6×25.6×37.8 inch). Figure 6.12(a) shows the controller and converter module, CTI capacitor module, supercapacitor bank module, lithium-ion battery bank module, and lead-acid battery bank module from top to bottom. Figure 6.12(b) shows the back view of the system. The standard 19-inch rack makes it easier to change the system configuration and develop the modules independently. The modules are reusable for other HEES systems. Heat generated from the EES elements and circuits is removed from the rack by four cooling fans installed on the back (not shown in the figure).

6.2.3 Control Method

The CTI should maintain a certain voltage level in order to avoid under-voltage failure when the load current increases suddenly. Control of the CTI voltage is critical to energy-efficient and reliable operation of the HEES system. The net current, sum of inflow currents and out-

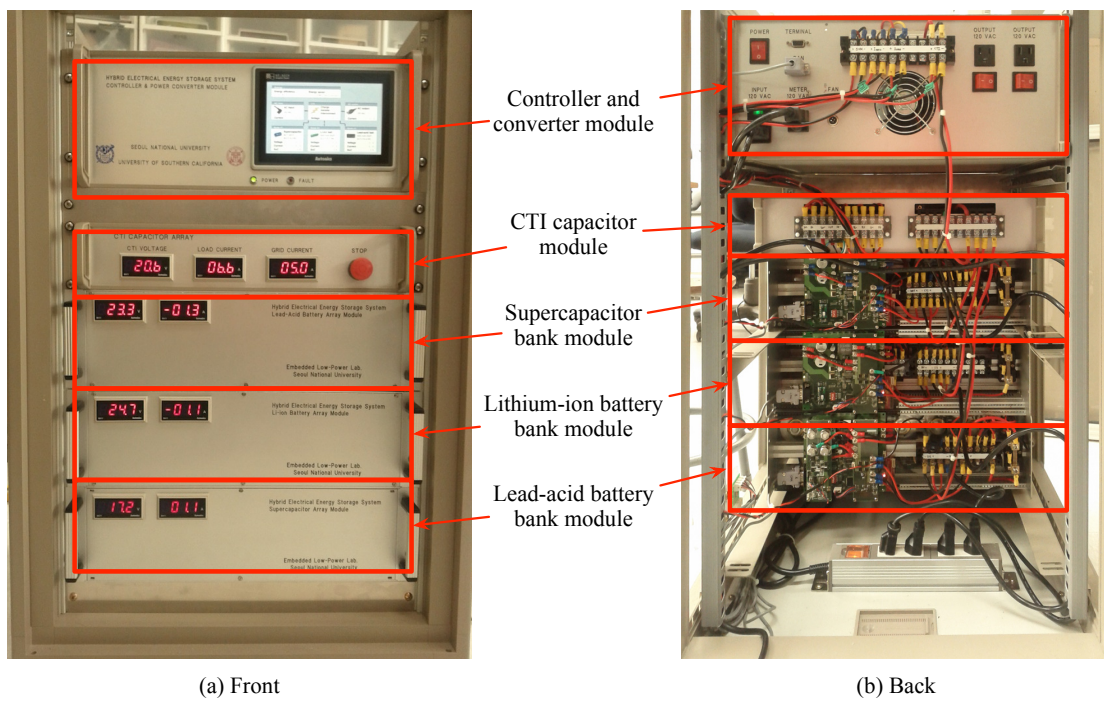(a) Front   (b) Back

Figure 6.12: Front and back views of the assembled HEES system.

flow currents, of the CTI should be zero in steady state in order to keep the CTI voltage constant. In an ideal case, we may operate all power converters in the current-regulating mode and adjust the output current immediately responding to CTI voltage variation. However, the capacitance of the CTI capacitor is not very large in practice, and thus the voltage changes very rapidly even with a slight mismatch between inflow and outflow currents. The software control is not fast enough to detect the CTI voltage variation and re-determine the current of EES banks in time. This is especially critical when experiencing a sudden increase of the load current but the system fails to increase the discharging current in time, resulting in the under-voltage failure.

We employ a cascaded control loop to overcome the CTI voltage reliability problem. We operate one of the discharging power converters in the voltage-regulating mode so that it regulates the CTI voltage with the hardware feedback control loop. The voltage regulation performed by the hardware voltage feedback control loop of the converter is fast enough to keep the CTI voltage at the desired level against the fluctuation of the input and output current of the CTI. Other current-regulating power converters extract or inject a designated amount of current from or to the CTI. Current supplied by the voltage-regulating power converter is consequently determined to the amount that makes the net current of the CTI zero. Choosing the voltage-regulating converter is an important decision though any of chargers of discharging EES banks and power converters from power sources can take this role. It is related to reliability because the it may have to solely maintain the CTI voltage during transient periods. We designate the DC–DC converter from the power grid as the voltage-regulating converter for reliability because the power grid has virtually unlimited power capacity and energy capacity. Consequently, the bidirectional chargers in the EES banks are in current-regulating mode.

This is similar to conventional control method introduced for shared bus HEES systems
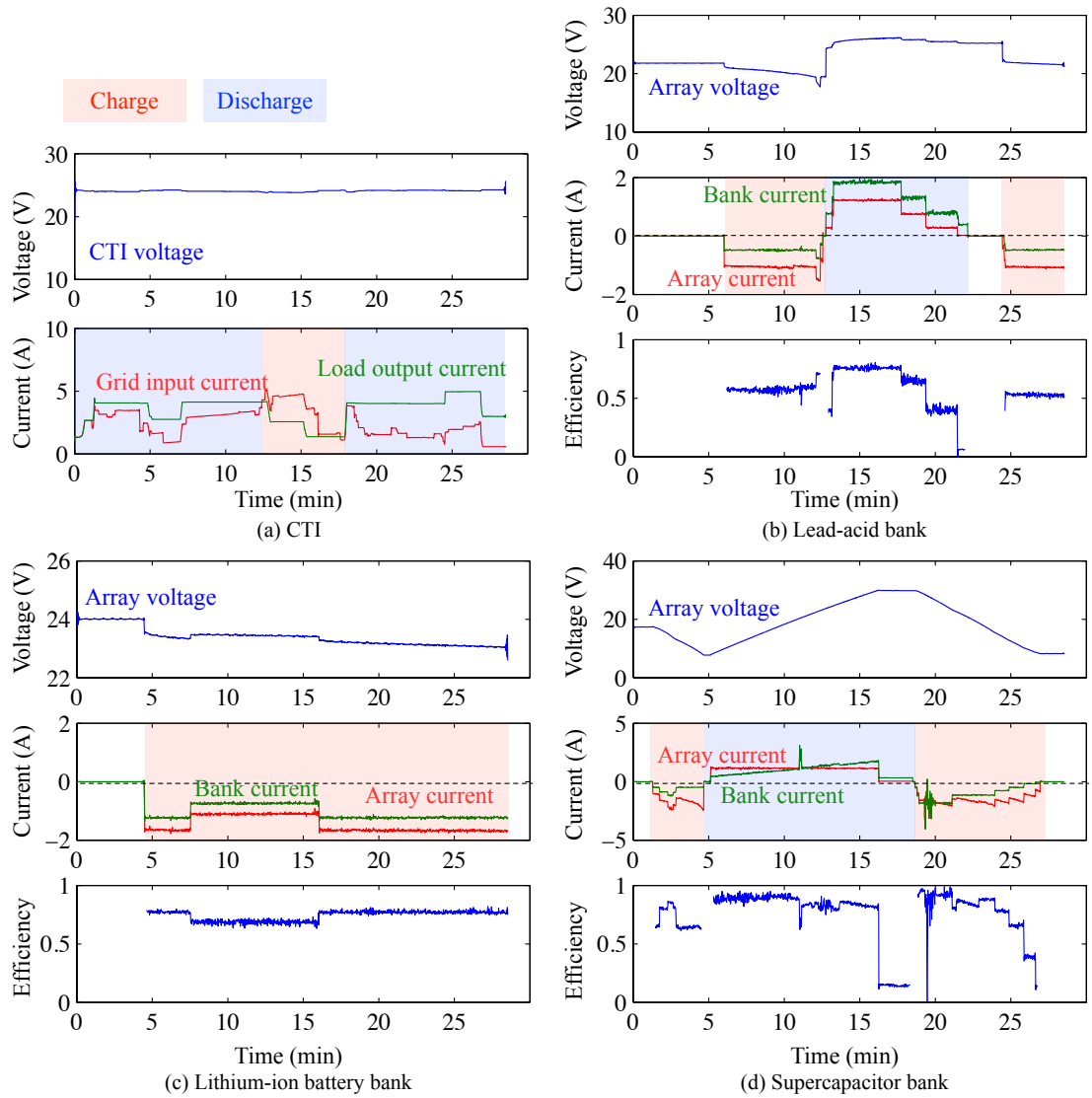
Figure 6.13: Voltage and current measured during operation.

at first glance [8, 84, 20]. However, the current control of each power source/EES bank is coupled with other power source/EES bank with a priori knowledge on them, and so limited in versatility and scalability. Our control method provides more flexibility and a higher degree of freedom for energy-efficient control by allowing arbitrary current for each EES banks as well as variable CTI voltage. Figure 6.13 shows the voltage and current of the CTI and banks while performing charging and discharging operations.

Chapter 7

Conclusions and Future Directions

Electrical energy storages (EES) systems offer various benefits of improved energy efficiency, reliability, availability, and cost-effectiveness for wide range of applications including the power grid, renewable power sources, electrical vehicle (EV)/hybrid electrical vehicle (HEV), and so on. Hybrid electrical energy storages (HEES) systems are a practical approach to implement EES systems with the current EES element technologies, where each of them has unique strengths and weaknesses. While design and control of the conventional homogeneous EES systems are straightforward, the HEES systems requires elaborated design and control methods to maximize its superiority over the homogeneous EES systems.

This dissertation studied the design considerations for practical implementation and deployment of the HEES systems. We proposed high-level HEES system architecture design and control methods to satisfy the design considerations. The proposed architecture-level HEES designs, which are the reconfigurable EES bank architecture and networked charge transfer interconnect (CTI) architecture, aim at reducing the maximizes the energy efficiency by reducing the energy loss induced by power conversion. We introduced optimiza-

tion problems and systematic solution methods involved in the proposed architectures. In addition, we proposed a design and operating method called the maximum power transfer tracking (MPTT) that achieves the joint optimality of HEES system with renewable power sources. We also introduced our HEES system prototype with detailed practical discussion on each component design.

The following issues are remained for future research:

- We devise a method to find the optimal sequence of charge transfers. This is an important step to schedule the operations in the HEES system from the power supply/demand profile. We first try to find the optimal sequence of charge transfers assuming the HEES system is given. Ultimately, the optimal sequence of charge transfers should be simultaneously derived with the optimal HEES system design.

- Optimization of HEES systems only is not enough for the true optimal of energy system. The power generation and power consumption should be optimized simultaneously. Power sources, HEES systems, and load devices should be aware of each other not only in design time, but also in runtime, to achieve the holistic energy optimization.

- We implement the charge management schemes in the HEES prototype and prove the practicality. This involves not only issues on theoretical optimality, but also practical issues such as reliable control and feasibility of real-time computation. We refine the management schemes with considerations on those issues and devise an effective implementation.

Bibliography

[1] H. T. Odum, "Energy quality and carrying capacity of the earth," *Tropical Ecology*, vol. 16, no. 1, p. 14, 1975.

[2] H. T. Odum, "Self-organization, transformity, and information," *Science*, vol. 242, no. 4882, pp. 1132–1138, 1988.

[3] C. J. Cleveland, "Energy quality and energy surplus in the extraction of fossil fuels in the U.S.," *Ecological Economics*, vol. 6, no. 2, pp. 139–162, 1992.

[4] M. Pedram, N. Chang, Y. Kim, and Y. Wang, "Hybrid electrical energy storage systems," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 363–368, 2010.

[5] F. Koushanfar, "Hierarchical hybrid power supply networks," in *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 629–630, 2010.

[6] C. Park, J. Seo, D. Seo, S. Kim, and B. Kim, "Cost-efficient memory architecture design of nand flash memory embedded systems," in *Proceedings of the International Conference on Computer Design (ICCD)*, pp. 474–480, 2003.

[7] P. Carter, J. Baxter, T. Newill, and T. Erekson, "An ultracapacitor-powered race car update," in *Proceeding of the Electrical Insulation Conference and Electrical Manufacturing Expo*, pp. 267–274, 2005.

[8] P. Thounthong, S. Raël, and B. Davat, "Energy management of fuel cell/battery/supercapacitor hybrid power source for vehicle applications," *Journal of Power Sources*, vol. 193, no. 1, pp. 376–385, 2009.

[9] S. Lukic, S. Wirasingha, F. Rodriguez, J. Cao, and A. Emadi, "Power management of an ultracapacitor/battery hybrid energy storage system in an HEV," in *Proceedings of the IEEE Vehicle Power and Propulsion Conference (VPPC)*, pp. 1–6, 2006.

[10] J. Moreno, M. Ortuzar, and J. Dixon, "Energy-management system for a hybrid electric vehicle, using ultracapacitors and neural networks," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 2, pp. 614–623, 2006.

[11] B. Frenzel, P. Kurzweil, and H. Rönnebeck, "Electromobility concept for racing cars based on lithium-ion batteries and supercapacitors," *Journal of Power Sources*, vol. 196, no. 12, pp. 5364–5376, 2011.

[12] M. Ortuzar, J. Moreno, and J. Dixon, "Ultracapacitor-based auxiliary energy system for an electric vehicle: Implementation and evaluation," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2147–2156, 2007.

[13] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," *IEEE Transactions on Vehicular Technology*, vol. 59, no. 6, pp. 2806–2814, 2010.

[14] V. Shah, R. Chaudhari, P. Kundu, and R. Maheshwari, "Performance analysis of hybrid energy storage system using hybrid control algorithm with bldc motor driving a vehicle," in *Proceedings of the Joint International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1–5, 2010.

[15] A. Allegre, A. Bouscayrol, and R. Trigui, "Influence of control strategies on battery/supercapacitor hybrid energy storage systems for traction applications," in *Proceedings of the IEEE Vehicle Power and Propulsion Conference (VPPC)*, pp. 213–220, 2009.

[16] W. Li and G. Joos, "A power electronic interface for a battery supercapacitor hybrid energy storage system for wind applications," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 1762–1768, 2008.

[17] A. Mirhoseini and F. Koushanfar, "HypoEnergy. hybrid supercapacitor-battery power-supply optimization for energy efficiency," in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1–4, 2011.

[18] D. Shin, Y. Kim, J. Seo, N. Chang, Y. Wang, and M. Pedram, "Battery-supercapacitor hybrid system for high-rate pulsed load applications," in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1–4, 2011.

[19] D. Shin, Y. Kim, Y. Wang, N. Chang, and M. Pedram, "Constant-current regulator-based battery-supercapacitor hybrid architecture for high-rate pulsed load applications," *Journal of Power Sources*, vol. 205, no. 0, pp. 516–524, 2012.

[20] Y. Zhang, Z. Jiang, and X. Yu, "Control strategies for battery/supercapacitor hybrid energy storage systems," in *Proceedings of the IEEE Energy 2030 Conference*, pp. 1–6, 2008.

167

[21] R. Dougal, S. Liu, and R. White, "Power and life extension of battery-ultracapacitor hybrids," *IEEE Transactions on Components and Packaging Technologies*, vol. 25, no. 1, pp. 120–131, 2002.

[22] C.-H. Li, X.-J. Zhu, G.-Y. Cao, S. Sui, and M.-R. Hu, "Dynamic modeling and sizing optimization of stand-alone photovoltaic power systems using hybrid energy storage technology," *Renewable Energy*, vol. 34, no. 3, pp. 815–826, 2009.

[23] S. Vosen and J. Keller, "Hybrid energy storage systems for stand-alone electric power systems: optimization of system performance and cost through control strategies," *International Journal of Hydrogen Energy*, vol. 24, no. 12, pp. 1139–1156, 1999.

[24] R. M. LaFollette and D. N. Bennion, "Design fundamentals of high power density, pulsed discharge, lead-acid batteries. 2. modeling," *Journal of the Electrochemical Society*, pp. 3701–3707, 1990.

[25] W. Henson, "Optimal battery/ultracapacitor storage combination," *Journal of Power Sources*, vol. 179, no. 1, pp. 417–423, 2008.

[26] S. Yoda and K. Ishihara, "The advent of battery-based societies and the global environment in the 21st century," *Journal of Power Sources*, vol. 81–82, no. 0, pp. 162–169, 1999.

[27] S. Brutti, J. Hassoun, B. Scrosati, C.-Y. Lin, H. Wu, and H.-W. Hsieh, "A high power Sn–C/C–LiFePO$_4$ lithium ion battery," *Journal of Power Sources*, vol. 217, no. 0, pp. 72–76, 2012.

[28] D. Bresser, E. Paillard, M. Copley, P. Bishop, M. Winter, and S. Passerini, "The importance of "going nano" for high power battery materials," *Journal of Power Sources*, vol. 219, no. 0, pp. 217–222, 2012.

[29] H. Akagi and H. Sato, "Control and performance of a doubly-fed induction machine intended for a flywheel energy storage system," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 109–116, 2002.

[30] H. Lund and G. Salgi, "The role of compressed air energy storage (CAES) in future sustainable energy systems," *Energy Conversion and Management*, vol. 50, no. 5, pp. 1172–1179, 2009.

[31] J. P. Deane, B. P. Ó. Gallachóir, and E. McKeogh, "Techno-economic review of existing and new pumped hydro energy storage plant," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 4, pp. 1293–1302, 2010.

[32] M. LeBreux, M. Lacroix, and G. Lachiver, "Control of a hybrid solar/electric thermal energy storage system," *International Journal of Thermal Sciences*, pp. 645–654, 2009.

[33] A. Bilodeau and K. Agbossou, "Control analysis of renewable energy system with hydrogen storage for residential applications," *Journal of Power Sources*, 2006.

[34] H. Chen, T. N. Cong, W. Yang, C. Tan, Y. Li, and Y. Ding, "Progress in electrical energy storage system: A critical review," *Progress in Natural Science*, vol. 19, no. 3, pp. 291–312, 2009.

[35] A. Czerwiński, S. Obrębowski, and Z. Rogulski, "New high-energy lead-acid battery with reticulated vitreous carbon as a carrier and current collector," *Journal of Power Sources*, vol. 198, no. 0, pp. 378–382, 2012.

[36] K. Pan, G. Shi, A. Li, H. Li, R. Zhao, F. Wang, W. Zhang, Q. Chen, H. Chen, Z. Xiong, and D. Finlow, "The performance of a silica-based mixed gel electrolyte in lead acid batteries," *Journal of Power Sources*, vol. 209, no. 0, pp. 262–268, 2012.

[37] C. Zhang, S. Sharkh, X. Li, F. Walsh, C. Zhang, and J. Jiang, "The performance of a soluble lead-acid flow battery and its comparison to a static lead-acid battery," *Energy Conversion and Management*, vol. 52, no. 12, pp. 3391–3398, 2011.

[38] R. Wills, J. Collins, D. Stratton-Campbell, C. Low, D. Pletcher, and F. Walsh, "Developments in the soluble lead-acid flow battery," *Journal of Applied Electrochemistry*, vol. 40, pp. 955–965, 2010.

[39] A. Oury, A. Kirchev, Y. Bultel, and E. Chainet, "PbO_2/Pb^{2+} cycling in methanesulfonic acid and mechanisms associated for soluble lead-acid flow battery applications," *Electrochimica Acta*, vol. 71, no. 0, pp. 140–149, 2012.

[40] D. A. Brownson, D. K. Kampouris, and C. E. Banks, "An overview of graphene in energy production and storage applications," *Journal of Power Sources*, vol. 196, no. 11, pp. 4873–4885, 2011.

[41] P. R. Abel, Y.-M. Lin, H. Celio, A. Heller, and C. B. Mullins, "Improving the stability of nanostructured silicon thin film lithium-ion battery anodes through their controlled oxidation," *ACS Nano*, vol. 6, no. 3, pp. 2506–2516, 2012.

[42] M. Ge, J. Rong, X. Fang, and C. Zhou, "Porous doped silicon nanowires for lithium ion battery anode with long cycle life," *Nano Letters*, vol. 12, no. 5, pp. 2318–2323, 2012.

[43] P. Guo, H. Song, and X. Chen, "Electrochemical performance of graphene nanosheets as anode material for lithium-ion batteries," *Electrochemistry Communications*, vol. 11, no. 6, pp. 1320–1324, 2009.

[44] P. Lian, X. Zhu, S. Liang, Z. Li, W. Yang, and H. Wang, "Large reversible capacity of high quality graphene sheets as an anode material for lithium-ion batteries," *Electrochimica Acta*, vol. 55, no. 12, pp. 3909–3914, 2010.

[45] G. Wang, X. Shen, J. Yao, and J. Park, "Graphene nanosheets for enhanced lithium storage in lithium ion batteries," *Carbon*, vol. 47, no. 8, pp. 2049–2053, 2009.

[46] H. Wang, L.-F. Cui, Y. Yang, H. Sanchez Casalongue, J. T. Robinson, Y. Liang, Y. Cui, and H. Dai, "Mn_3O_4-graphene hybrid as a high-capacity anode material for lithium ion batteries," *Journal of the American Chemical Society*, vol. 132, no. 40, pp. 13978–13980, 2010.

[47] E. Yoo, J. Kim, E. Hosono, H.-s. Zhou, T. Kudo, and I. Honma, "Large reversible Li storage of graphene nanosheet families for use in rechargeable lithium ion batteries," *Nano Letters*, vol. 8, no. 8, pp. 2277–2282, 2008.

[48] G. Zhou, D.-W. Wang, F. Li, L. Zhang, N. Li, Z.-S. Wu, L. Wen, G. Q. M. Lu, and H.-M. Cheng, "Graphene-wrapped Fe_3O_4 anode material with improved reversible capacity and cyclic stability for lithium ion batteries," *Chemistry of Materials*, vol. 22, no. 18, pp. 5306–5313, 2010.

171

[49] M. Zolot, A. A. Pesaran, and M. Mihalic, "Battery power for your residential solar electric system," tech. rep., National Renewable Energy Laboratory, 2002.

[50] F. Simjee and P. Chou, "Everlast: Long-life, supercapacitor-operated wireless sensor node," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 197–202, 2006.

[51] T. B. Atwater, P. J. Cygan, and F. C. Leung, "Man portable power needs of the 21st century: I. applications for the dismounted soldier. ii. enhanced capabilities through the use of hybrid power sources," *Journal of Power Sources*, vol. 91, no. 1, pp. 27–36, 2000.

[52] J. Jiang and A. Kucernak, "Electrochemical supercapacitor material based on manganese oxide: preparation and characterization," *Electrochimica Acta*, vol. 47, no. 15, pp. 2381–2386, 2002.

[53] T.-Y. Wei, C.-H. Chen, H.-C. Chien, S.-Y. Lu, and C.-C. Hu, "A cost-effective super-capacitor material of ultrahigh specific capacitances: Spinel nickel cobaltite aerogels from an epoxide-driven sol–gel process," *Advanced Materials*, vol. 22, no. 3, pp. 347–351, 2010.

[54] Q. Cheng, J. Tang, J. Ma, H. Zhang, N. Shinya, and L.-C. Qin, "Graphene and nanostructured MnO_2 composite electrodes for supercapacitors," *Carbon*, vol. 49, no. 9, pp. 2917–2925, 2011.

[55] Q. Cheng, J. Tang, J. Ma, H. Zhang, N. Shinya, and L.-C. Qin, "Graphene and carbon nanotube composite electrodes for supercapacitors with ultra-high energy density," *Physical Chemistry Chemical Physics.*, vol. 13, pp. 17615–17624, 2011.

[56] C. Liu, Z. Yu, D. Neff, A. Zhamu, and B. Z. Jang, "Graphene-based supercapacitor with an ultrahigh energy density," *Nano Letters*, vol. 10, no. 12, pp. 4863–4868, 2010.

[57] J. of the Korean Electrochemical Society, "hybrid capacitors using organic electrolytes," *Journal of the American Chemical Society*, vol. 6, no. 3, pp. 174–177, 2003.

[58] S. Vivekchand, C. Rout, K. Subrahmanyam, A. Govindaraj, and C. Rao, "Graphene-based electrochemical supercapacitors," *Journal of Chemical Sciences*, vol. 120, pp. 9–13, 2008.

[59] P. R. Abel, Y.-M. Lin, H. Celio, A. Heller, and C. B. Mullins, "Improving the stability of nanostructured silicon thin film lithium-ion battery anodes through their controlled oxidation," *ACS Nano*, vol. 6, no. 3, pp. 2506–2516, 2012.

[60] M. Chowdhury, M. Haque, M. Aktarujjaman, M. Negnevitsky, and A. Gargoom, "Grid integration impacts and energy storage systems for wind energy applications—a review," in *Proceedings of the IEEE Power and Energy Society General Meeting*, pp. 1–8, 2011.

[61] Y. Hou, R. Vidu, and P. Stroeve, "Solar energy storage methods," *Industrial & Engineering Chemistry Research*, vol. 50, no. 15, pp. 8954–8964, 2011.

[62] E. Shkolnikov, A. Zhuk, and M. Vlaskin, "Aluminum as energy carrier: Feasibility analysis and current technologies overview," *Renewable and Sustainable Energy Reviews*, vol. 15, no. 9, pp. 4611–4623, 2011.

[63] X. Zhao, B. M. Sanchez, P. J. Dobson, and P. S. Grant, "The role of nanomaterials in redox-based supercapacitors for next generation energy storage devices," *Nanoscale*, vol. 3, pp. 839–855, 2011.

[64] A. Evans, V. Strezov, and T. J. Evans, "Assessment of utility energy storage options for increased renewable energy penetration," *Renewable and Sustainable Energy Reviews*, vol. 16, no. 6, pp. 4141–4147, 2012.

[65] K. Divya and J. Østergaard, "Battery energy storage technology for power systems—an overview," *Electric Power Systems Research*, vol. 79, no. 4, pp. 511–520, 2009.

[66] "Battery power for your residential solar electric system," tech. rep., National Renewable Energy Laboratory, 2002.

[67] K. Darcovich, N. Gupta, I. Davidson, and T. Caroni, "Residential electrical power storage scenario simulations with a large-scale lithium ion battery," *Journal of Applied Electrochemistry*, vol. 40, pp. 749–755, 2010.

[68] S. Park, Y. Wang, Y. Kim, N. Chang, and M. Pedram, "Battery management for grid-connected pv systems with a battery," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 115–120, 2012.

[69] B. Roberts and J. McDowall, "Commercial successes in power storage," *IEEE Power and Energy Magazine*, vol. 3, no. 2, pp. 24–30, 2005.

[70] T.-Y. Lee and N. Chen, "Determination of optimal contract capacities and optimal sizes of battery energy storage systems for time-of-use rates industrial customers," *IEEE Transactions on Energy Conversion*, vol. 10, no. 3, pp. 562–568, 1995.

[71] S. Teleke, M. Baran, S. Bhattacharya, and A. Huang, "Optimal control of battery energy storage for wind farm dispatching," *IEEE Transactions on Energy Conversion*, vol. 25, no. 3, pp. 787–794, 2010.

[72] L. Barote, R. Weissbach, R. Teodorescu, C. Marinescu, and M. Cirstea, "Stand-alone wind system with vanadium redox battery energy storage," in *Proceedings of the International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, pp. 407–412, 2008.

[73] J. L. Bernal-Agustín and R. Dufo-López, "Simulation and optimization of stand-alone hybrid renewable energy systems," *Renewable and Sustainable Energy Reviews*, vol. 13, no. 8, pp. 2111–2118, 2009.

[74] O. Ekren, B. Y. Ekren, and B. Ozerdem, "Break-even analysis and size optimization of a PV/wind hybrid energy conversion system with battery storage – a case study," *Applied Energy*, vol. 86, no. 7–8, pp. 1043–1054, 2009.

[75] O. Ekren and B. Y. Ekren, "Size optimization of a PV/wind hybrid energy conversion system with battery storage using simulated annealing," *Applied Energy*, vol. 87, no. 2, pp. 592–598, 2010.

[76] S. Bashash, S. J. Moura, J. C. Forman, and H. K. Fathy, "Plug-in hybrid electric vehicle charge pattern optimization for energy cost and battery longevity," *Journal of Power Sources*, vol. 196, no. 1, pp. 541–549, 2011.

[77] S. J. Moura, D. S. Callaway, H. K. Fathy, and J. L. Stein, "Tradeoffs between battery energy capacity and stochastic optimal power management in plug-in hybrid electric vehicles," *Journal of Power Sources*, vol. 195, no. 9, pp. 2979–2988, 2010.

[78] P. Chanhom, S. Sirisukprasert, and N. Hatti, "DC-link voltage optimization for SOC balancing control of a battery energy storage system based on a 7-level cascaded PWM converter," in *Proceedings of the International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, pp. 1–4, 2012.

[79] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade PWM converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1099–1107, 2012.

[80] H. Qian, J. Zhang, J.-S. Lai, and W. Yu, "A high-efficiency grid-tie battery energy storage system," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 886–896, 2011.

[81] J. R. Miller and A. F. Burke., "Electrochemical capacitors: Challenges and opportunities for real-world applications," *The Electrochemical Society Interface*, vol. 17, pp. 53–57, 2008.

[82] A. Xu, S. Xie, and X. Liu, "Dynamic voltage equalization for series-connected ultracapacitors in EV/HEV applications," *IEEE Transactions on Vehicular Technology*, vol. 58, no. 8, pp. 3981–3987, 2009.

[83] R. Torah, P. Glynne-Jones, M. Tudor, T. O'Donnell, S. Roy, and S. Beeby, "Self-powered autonomous wireless sensor node using vibration energy harvesting," *Measurement Science and Technology*, vol. 19, no. 12, pp. 125202–125209, 2008.

[84] P. Thounthong, V. Chunkag, P. Sethakul, S. Sikkabut, S. Pierfederici, and B. Davat, "Energy management of fuel cell/solar cell/supercapacitor hybrid power source," *Journal of Power Sources*, vol. 196, no. 1, pp. 313–324, 2011.

[85] B. Liu, F. Zhuo, and X. Bao, "Fuzzy control for hybrid energy storage system based on battery and ultra-capacitor in micro-grid," in *Proceedings of the International Power Electronics and Motion Control Conference (IPEMC)*, vol. 2, pp. 778–782, 2012.

[86] C. Romaus, J. Bocker, K. Witting, A. Seifried, and O. Znamenshchykov, "Optimal energy management for a hybrid energy storage system combining batteries and double layer capacitors," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1640–1647, 2009.

[87] J. Miller, U. Deshpande, T. Dougherty, and T. Bohn, "Power electronic enabled active hybrid energy storage system and its economic viability," in *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 190–198, 2009.

[88] C. Jin, S. Lu, N. Lu, and R. Dougal, "Cross-market optimization for hybrid energy storage systems," in *Proceedings of the IEEE Power and Energy Society General Meeting*, pp. 1–6, 2011.

[89] X. Jiang, J. Polastre, and D. Culler, "Perpetual environmentally powered sensor networks," in *Proceedings of the International Symposium on Information Processing in Sensor Networks (IPSN)*, pp. 463–468, 2005.

[90] C. Park and P. Chou, "AmbiMax: Autonomous energy harvesting platform for multi-supply wireless sensor nodes," in *Proceedings of the IEEE Communications Society*

177

Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON), vol. 1, pp. 168–177, 2006.

[91] F. Koushanfar and A. Mirhoseini, "Hybrid heterogeneous energy supply networks," in *Proceedings of the IEEE International Symposium on Circuits and Systems (IS-CAS)*, pp. 2489–2492, 2011.

[92] A. Mirhoseini and F. Koushanfar, "Learning to manage combined energy supply systems," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 229–234, 2011.

[93] J. Zhuo, C. Chakrabarti, N. Chang, and S. Vrudhula, "Extending the lifetime of fuel cell based hybrid systems," in *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 562–567, 2006.

[94] J. Zhuo, C. Chakrabarti, N. Chang, and S. Vrudhula, "Maximizing the lifetime of embedded systems powered by fuel cell-battery hybrids," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 424–429, 2006.

[95] J. Zhuo, C. Chakrabarti, and N. Chang, "Energy management of DVS-DPM enabled embedded systems powered by fuel cell-battery hybrid source," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 322–327, 2007.

[96] K. Lee, N. Chang, J. Zhuo, C. Chakrabarti, S. Kadri, and S. Vrudhula, "A fuel-cell-battery hybrid for portable embedded systems," *ACM Transactions on Design Automation of Electronic Systems*, vol. 13, no. 1, pp. 19:1–19:34, 2008.

[97] J. Zhuo, C. Chakrabarti, K. Lee, N. Chang, and S. Vrudhula, "Maximizing the lifetime of embedded systems powered by fuel cell-battery hybrids," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 1, pp. 22–32, 2009.

[98] N. Chang, J. Seo, D. Shin, and Y. Kim, "Room-temperature fuel cells and their integration into portable and embedded systems," in *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 69–74, 2010.

[99] W. Liu, Y. Wang, W. Liu, Y. Ma, Y. Xie, and H. Yang, "On-chip hybrid power supply system for wireless sensor nodes," in *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 43–48, 2011.

[100] Y. Choi, N. Chang, and T. Kim, "DC–DC converter-aware power management for low-power embedded systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 8, pp. 1367–1381, 2007.

[101] A. J. Stratakos, *High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications*. PhD thesis, University of California, Berkeley, CA, 1999.

[102] V. Kursun, S. Narendra, V. De, and E. Friedman, "Monolithic DC-DC converter analysis and MOSFET gate voltage optimization," in *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 279–284, 2003.

[103] Linear Technology, "LTM4609: 36 V$_{in}$, 34 V$_{out}$ high efficiency buck-boost DC/DC μModule regulator."

[104] M. Villalva, J. Gazoli, and E. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1198–1208, 2009.

[105] D. Sera, R. Teodorescu, and P. Rodriguez, "PV panel model based on datasheet values," in *Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 2392–2396, 2007.

[106] R. Banakar, S. Steinke, B.-S. Lee, M. Balakrishnan, and P. Marwedel, "Scratchpad memory: design alternative for cache on-chip memory in embedded systems," in *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 73–78, 2002.

[107] Q. Xie, Y. Wang, Y. Kim, N. Chang, and M. Pedram, "Charge allocation for hybrid electrical energy storage systems," in *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 277–284, 2011.

[108] Q. Xie, Y. Wang, Y. Kim, D. Shin, N. Chang, and M. Pedram, "Charge replacement in hybrid electrical energy storage systems," in *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 627–632, 2012.

[109] Y. Wang, Y. Kim, Q. Xie, N. Chang, and M. Pedram, "Charge migration efficiency optimization in hybrid electrical energy storage (hees) systems," in *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 103–108, 2011.

[110] Y. Wang, Q. Xie, M. Pedram, Y. Kim, N. Chang, and M. Poncino, "Multiple-source and multiple-destination charge migration in hybrid electrical energy storage systems," in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2012.

180

[111] Y. Kim, S. Park, Y. Wang, Q. Xie, N. Chang, M. Poncino, and M. Pedram, "Balanced reconfiguration of storage banks in a hybrid electrical energy storage system," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pp. 624–631, 2011.

[112] Y. Barsukov, "Battery cell balancing: what to balance and how," tech. rep., Texas Instruments, 2009.

[113] Y. Kim, S. Park, N. Chang, Q. Xie, Y. Wang, and M. Pedram, "Networked architecture for hybrid electrical energy storage systems," in *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 522–528, 2012.

[114] Q. Xie, D. Zhu, Y. Wang, Y. Kim, N. Chang, and M. Pedram, "An efficient scheduling algorithm for multiple charge migration tasks in hybrid electrical energy storage systems," in *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC) (to appear)*, 2013.

[115] Q. Xie, X. Lin, Y. Wang, M. Pedram, D. Shin, and N. Chang, "State of health aware charge management in hybrid electrical energy storage systems," in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1060–1065, 2012.

[116] R. Balasubramonian, D. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, "Memory hierarchy reconfiguration for energy and performance in general-purpose processor architectures," in *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (Micro)*, pp. 245–257, 2000.

[117] H. Zheng, J. Lin, Z. Zhang, E. Gorbatov, H. David, and Z. Zhu, "Mini-rank: Adaptive dram architecture for improving memory power efficiency," in *Proceedings of the*

ACM/IEEE International Symposium on Microarchitecture (Micro), pp. 210–221, 2008.

[118] X. Fang, N. Kutkut, J. Shen, and I. Batarseh, "Analysis of generalized parallel-series ultracapacitor shift circuits for energy storage systems," *Renewable Energy*, 2010.

[119] P. Spindler, U. Schlichtmann, and F. Johannes, "Kraftwerk2 —a fast force-directed quadratic placement approach using an accurate net model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 8, pp. 1398–1411, 2008.

[120] M.-C. Kim, D.-J. Lee, and I. Markov, "SimPL: An effective placement algorithm," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 1, pp. 50–60, 2012.

[121] A. E. Caldwell, A. B. Kahng, and I. L. Markov, "Can recursive bisection alone produce routable placements?," in *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 477–482, 2000.

[122] M. Can Yildiz and P. H. Madden, "Improved cut sequences for partitioning based placement," in *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 776–779, 2001.

[123] K. Vorwerk, A. Kennings, and J. Greene, "Improving simulated annealing-based FPGA placement with directed moves," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 2, pp. 179–192, 2009.

[124] D. Hill, "A CAD system for the design of field programmable gate arrays," in *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 187–192, 1991.

[125] Y.-W. Chang, S. Thakur, K. Zhu, and D. F. Wong, "A new global routing algorithm for FPGAs," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pp. 356–361, 1994.

[126] L. McMurchie and C. Ebeling, "PathFinder: a negotiation-based performance-driven router for FPGAs," in *Proceedings in the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 111–117, 1995.

[127] J. S. Swartz, V. Betz, and J. Rose, "A fast routability-driven router for FPGAs," in *Proceedings in the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 140–149, 1998.

[128] J. Luu, I. Kuon, P. Jamieson, T. Campbell, A. Ye, W. M. Fang, and J. Rose, "VPR 5.0: FPGA cad and architecture exploration tools with single-driver routing, heterogeneity and process scaling," in *Proceedings in the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 133–142, 2009.

[129] Y. Kim, Y. Wang, N. Chang, and M. Pedram, "Maximum power transfer tracking for a photovoltaic-supercapacitor energy system," in *Proceedings of the ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 307–312, 2010.

[130] C. Lu, V. Raghunathan, and K. Roy, "Maximum power point considerations in micro-scale solar energy harvesting systems," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 273–276, 2010.

[131] M. Alonso-García, J. Ruiz, and F. Chenlo, "Experimental study of mismatch and shading effects in the I-V characteristic of a photovoltaic module," *Solar Energy Materials and Solar Cells*, 2006.

[132] W. Xiao, W. Dunford, P. Palmer, and A. Capel, "Regulation of photovoltaic voltage," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 3, pp. 1365–1374, 2007.

[133] E. Durán, J. Andújar, F. Segura, and A. Barragán, "A high-flexibility DC load for fuel cell and solar arrays power sources based on DC–DC converters," *Applied Energy*, vol. 88, no. 5, pp. 1690–1702, 2011.

[134] A. Koran, K. Sano, R.-Y. Kim, and J.-S. Lai, "Design of a photovoltaic simulator with a novel reference signal generator and two-stage LC output filter," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1331–1338, 2010.

[135] P. Sanchis, I. Echeverria, A. Ursua, O. Alonso, E. Gubia, and L. Marroyo, "Electronic converter for the analysis of photovoltaic arrays and inverters," in *Proceedings of Power Electronics Specialist Conference (PESC)*, vol. 4, pp. 1748–1753, 2003.

[136] Y. Kim, W. Lee, M. Pedram, and N. Chang, "Dual-mode power regulator for photovoltaic module emulation," *Applied Energy*, vol. 101, no. 0, pp. 730–739, 2013.

[137] Y. Kim, D. Shin, J. Seo, N. Chang, H. Cho, Y. Kim, and S. Yoon, "System integration of a portable direct methanol fuel cell and a battery hybrid," *International Journal of Hydrogen Energy*, vol. 35, no. 11, pp. 5621–5637, 2010.

[138] Linear Technology, "LT1083: 7.5A, 5A, 3A low dropout positive adjustable regulators."

[139] J. Neubauer, "Precision current source is software-programmable," *EDN*, p. 72, December 2004.

[140] S. Chakraborty, M. Lukasiewycz, C. Buckl, S. Fahmy, N. Chang, S. Park, Y. Kim, P. Leteinturier, and H. Adlkofer, "Embedded systems and software challenges in electric vehicles," in *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 424–429, 2012.

[141] J. Wiehagen and D. Harrell, "Review of residential electrical energy use data," tech. rep., NAHB Research Center, Inc., 2001.

[142] Maxwell Technologies, "K2 series ultracapacitors."

[143] Samsung SDI, "Specification of product for lithium-ion rechargeable cell model ICR18650-26F," 2009.

[144] Panasonic, "Value-regulated lead acid batteries: individual data sheet: LC-R123R4P," 2005.

[145] Mean Well, "600W single output power supply: SE-600 series," 2011.

[146] Samlex, "1000W DC–AC inverter pure since wave."

[147] Linear Technology, "LTC3789: High efficiency, synchronous, 4-switch buck-boost controller."

[148] Linear Technology, "LTC4000: High voltage high current controller for battery charging and power management."

초록

전기 에너지 저장 (electrical energy storage, EES) 시스템은 필요에 따라 에너지를 저장하였다가 사용함으로써 에너지 효율과 안정성을 높이고 에너지 단가를 낮추는 등의 기능을 한다. EES 시스템은 비상용 전기 공급, 부하 평준화, 첨두부하 분산, 재생에너지 발전을 위한 에너지 저장 등의 다양한 분야에서 응용할 수 있다. 현재 EES 시스템은 주로 단일 종류의 에너지 저장 기술을 사용하고 있는데, 아직까지 그 어떤 에너지 저장 기술도 높은 에너지 및 전력 밀도, 낮은 가격, 높은 충방전 효율, 긴 수명 등 이상적인 에너지 저장 기술의 모든 요건을 충족시키고 있지 못하고 있다. 하이브리드 전력 저장 (hybrid electrical energy storage, HEES) 시스템은 여러 다른 종류의 에너지 저장 소자를 이용하여 각각의 장점을 활용하여 단점을 보완하는 기법으로, EES 시스템의 성능을 개선시시키기 위한 실용적인 접근 방법 가운데 하나이다. HEES 시스템은 정교한 시스템 설계와 제어기법을 통해 각각의 에너지 저장 소자의 장점을 모두 합친 것과 같은 성능을 갖출 수 있다.

　본 학위 논문은 HEES 시스템의 에너지 효율을 최대화하기 위한 고수준의 최적화 기법들을 소개한다. HEES 시스템의 새로운 구조들과 체계적인 최적 설계 기법들을 제시한다. 제안된 네트워크 전하 전송망 (charge transfer interconnect, CTI) 구조와 뱅크 (bank) 재구성 구조는 전력 변환 손실을 최소화하여 HEES 시스템의 전하 전송 효율을 최대화한다. 또한 기존의 제어 기법들이 가진 한계점을 지적하고, 이를 보완

하기 위해 전력원을 동시에 고려하여 설계하고 제어하는 기법을 제시한다. 제안된 최대 전력 전달 추종 (maximum power transfer tracking, MPTT) 기법과 이를 고려한 설계 기법은 실직적인 에너지 수집량을 증가시키고 실제적으로 사용 가능한 에너지량을 증가시킨다. 마지막으로 제안된 기법의 실현 가능성을 검증하기 위한 HEES 시스템 프로토타입 구현을 소개한다.

주요어: 에너지 저장 시스템, 하이브리드 전력 저장 시스템

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