Ph. D. Dissertation

A Study on Multichannel Receivers with Enhanced Lane Expandability and Loop Linearity

데이터 전송로 확장성과 루프 선형성을 향상시킨 다중채널 수신기들에 관한 연구

by

Byoung-Joo Yoo

February, 2013

School of Electrical Engineering and Computer Science
College of Engineering
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指導敎授 鄭 德 均

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Abstract

Two types of serial data communication receivers that adopt a multichannel architecture for a high aggregate I/O bandwidth are presented. Two techniques for collaboration and sharing among channels are proposed to enhance the loop-linearity and channel-expandability of multichannel receivers, respectively.

The first proposed receiver employs a collaborative timing scheme recovery which relies on the sharing of all outputs of phase detectors (PDs) among channels to extract common information about the timing and multilevel signaling architecture of PAM-4. The shared timing information is processed by a common global loop filter and is used to update the phase of the voltage-controlled oscillator with better rejection of per-channel noise. In addition to collaborative timing recovery, a simple linearization technique for binary PDs is proposed. The technique realizes a high-rate oversampling PD while the hardware cost is equivalent to that of a conventional 2x-oversampling clock and data recovery. The first receiver exploiting the collaborative timing recovery architecture is designed using 45-nm CMOS technology. A single data lane occupies a 0.195-mm^2 area and consumes a relatively low 17.9 mW at 6 Gb/s at 1.0V. Therefore, the power efficiency is 2.98 mW/Gb/s. The simulated jitter is about 0.034 UI RMS given an input jitter value of 0.03 UI RMS, while the relatively

constant loop bandwidth with the PD linearization technique is about 7.3-MHz regardless of the data-stream noise.

Unlike the first receiver, the second proposed multichannel receiver was designed to reduce the hardware complexity of each lane. The receiver employs shared calibration logic among channels and yet achieves superior channel expandability with slim data lanes. A shared global calibration control, which is used in a forwarded clock receiver based on a multiphase delay-locked loop, accomplishes skew calibration, equalizer adaptation, and the phase lock of all channels during a calibration period, resulting in reduced hardware overhead and less area required by each data lane. The second forwarded clock receiver is designed in 90-nm CMOS technology. It achieves error-free eye openings of more than 0.5 UI across 9－28 inch Nelco 4000-6 microstrips at 4－7 Gb/s and more than 0.42 UI at data rates of up to 9 Gb/s. The data lane occupies only 0.152 mm^2 and consumes 69.8 mW, while the rest of the receiver occupies 0.297 mm^2 and consumes 56 mW at a data rate of 7 Gb/s and a supply voltage of 1.35 V.

Keywords: Multichannel receiver, forwarded clock, collaborative timing recovery, clock and data recovery, bang-bang phase detector, linearization technique, phase-locked loop (PLL), delay-locked loop (DLL)

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Chapter 1

Introduction

1.1 Motivations

Over the past decade, the dramatic technological progress of transistor scaling has increased the number of transistors per single die, following Moore's prediction in 1965 [1.1]. Advances in integrated circuits have led to an explosive increase of functions in a system and have consequently accelerated the complexity of systems. As a result, many recent systems require high-speed data communication to process their functions while consuming low levels of power. At present, numerous digital systems are capable of data rates of several gigabits per second, and they will achieve a total bandwidth greater than 100 Gbps soon. For example, the present Ethernet (e.g., 10GBASE-SR) has four lanes to transmit the 2.5 Gbps of NRZ data, but research on 100GBASE or 1T-BASE technology continues to achieve a data transmission rate of over 25 Gbps per lane [1.2]. The explosive growth in the need

for higher transmission rates in chip-to-chip communication has forced designers to increase the per-pin data rate and to expand the number of data channels.

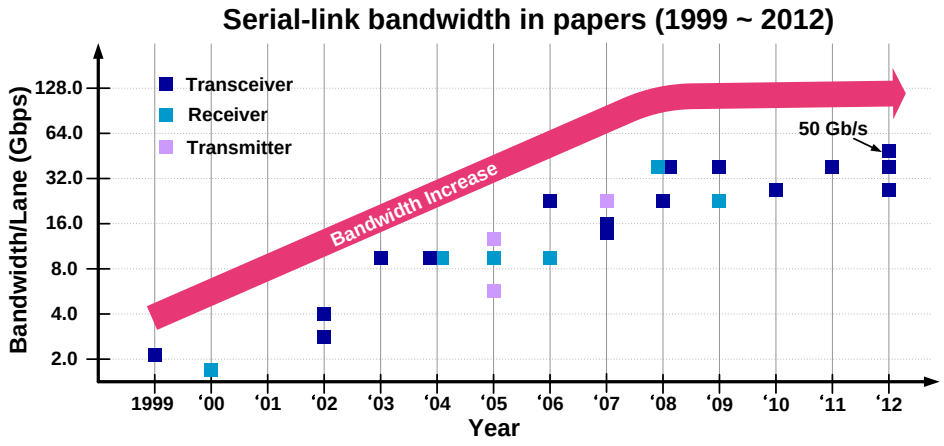


Fig. 1.1 The trend of bandwidth for wireline transceivers in papers.

Various techniques have been adopted to increase the per-pin data rate in a system, such as multi-level signaling [1.3], per-pin skew compensation [1.4], channel impedance matching [1.5], channel equalization [1.6], and others. However, the per-pin data rate is still limited by many factors, such as the channel characteristics, packages, unity gain of transistors, leakage current, and supply voltage. As a result, the bandwidth growth rate per lane has been gradually declining. Fig. 1.1 shows the trend of bandwidth for wireline transceivers as reported in papers from 1999 to 2012. During the first ten years, the data rate per lane increased by almost 16 times, from 2 Gb/s to 40 Gb/s. On the other hand, the data rate has remained almost unchanged since 2009. To expand the bandwidth, optical devices and fibers are drawing attention as viable alternatives to electrical devices and copper cables. In Fig. 1.1,

most transceivers which have a bandwidth that exceeds 40 Gb/s were designed for the 100G-BASE Ethernet and optical links [1.7]. However, the core circuits in a transceiver, such as the driver, the clock and data recovery (CDR) circuit, the phase-locked loop (PLL), the delay-locked loop (DLL), and others continue to be bottlenecks that prevent an expansion of the bandwidth. According to the ITRS roadmap of 2011 [1.8], the maximum I/O data rate will exponentially increase from year to year while the maximum I/O data rate and power dissipation per lane will remain unchanged or will only change slightly, as shown in Fig. 1.2. Therefore, the number of lanes per package will increase in proportion to the maximum package I/O data rate.

	2012	2014	2016	2018	2020	2022
Max. I/O Power Dissipation [Watts]	40	40	40	40	40	40
Max. I/O Data-Rate per Lane [Gb/s]	10	25	25	25	40	40
Max. Package I/O Data-Rate [Gb/s]	2500	4998	9994	19982	39952	79879
Number of Lanes per Package [#]	**250**	**200**	**400**	**799**	**999**	**1997**

Reference from ITRS 2011

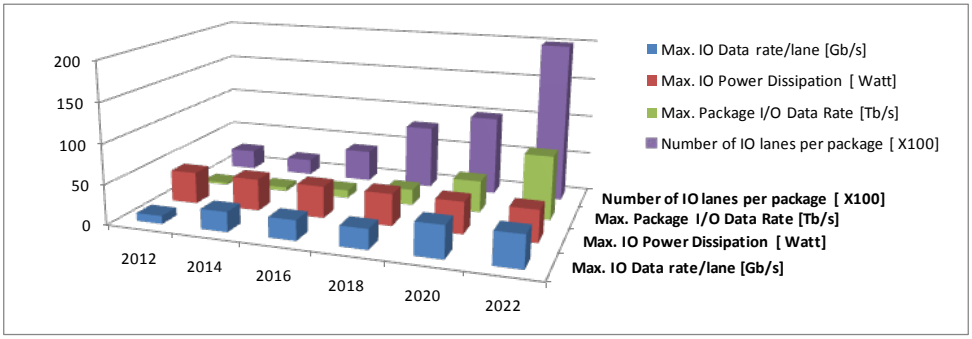


Fig. 1.2 The bandwidth and power roadmap for wireline transceivers.

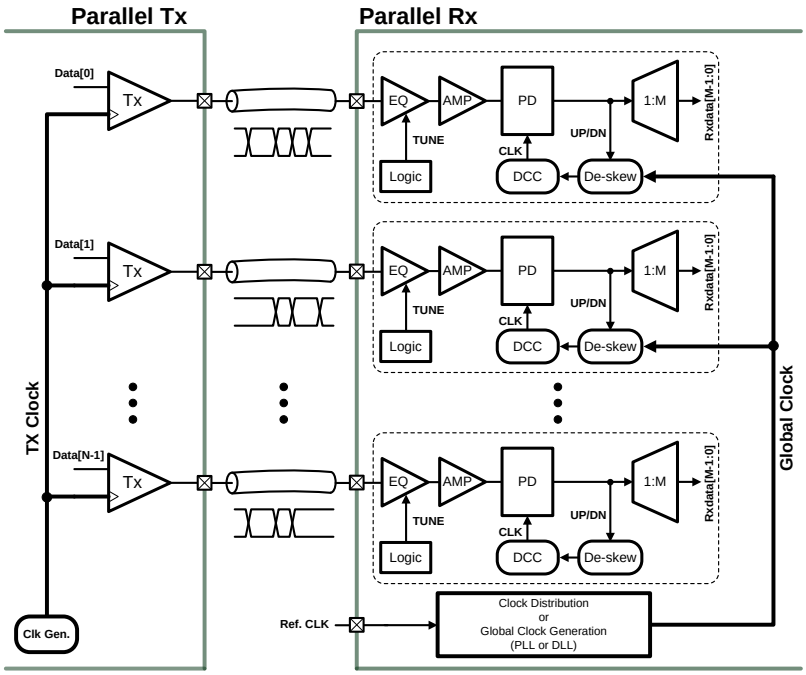


Fig. 1.3 A conventional multilane transceiver for a serial data communication.

Adding the number of channels in parallel interfaces [1.9] or wide I/Os [1.10] is a straightforward means of achieving high data transmission rates. However, those methods usually involve a trade-off between performance and cost. Fig. 1.3 shows a block diagram of a conventional serial-link transceiver employing multichannel architecture. As shown in Fig. 1.3, the expanded number of channels leads to a global clock distribution with a long distance to each channel and results in the need for many buffers to deliver the clock. Moreover, the increased distribution distance makes the clock more sensitive to noise and the skew problem of each channel degrades the bit-error rate (BER) of the recovered data. In addition to the clock distribution, the increased number of core components per single lane seriously

increases the cost. The number of limiting amplifiers for the linear phase detection at the front-end of lane, of which the layouts are largely drawn to reduce their offsets, requires a large amount of power to achieve the higher bandwidth. In addition, the dedicated clock and data recovery circuits (CDRs), duty cycle correctors (DCCs), and any de-skewers of each lane limit the number of lanes and require high power consumption and a large area. These independent CDRs also expose the weakness associated with the data pattern. Each CDR loop highly depends on the data transition density and encoding scheme such that its characteristics change according to the data pattern. Moreover, the lock state is broken.

A simple form of architecture in each lane of data transmission is desired, and an accurate clock recovery with tolerance against variations of environmental noise is required for a low bit-error rate. To meet these demands, many candidates for the transceiver architectures of serial-data communication have been reported in the literature, including forwarded-clock architecture [1.11], embedded-clock architecture [1.12], and collaborative timing recovery architecture types [1.13]. However, still, there are many circuits that can be removed in each lane or that can be shared among lanes with these types of architecture. For example, a clock recovery circuit, which is one of the major sources used to dissipate high power and to increase the area in each lane, can be shared by one global timing controller. Moreover, binary phase detectors to avoid the use of limiting amplifier have a nonlinear transfer characteristic resulting in the change of loop dynamics such as the loop bandwidth and phase margin [1.14-1.15].

To overcome these weaknesses, the characteristics of a multichannel receiver should be noted. The characteristics of multichannel links can be represented by their advantages and disadvantages, as shown in Fig. 1.4.

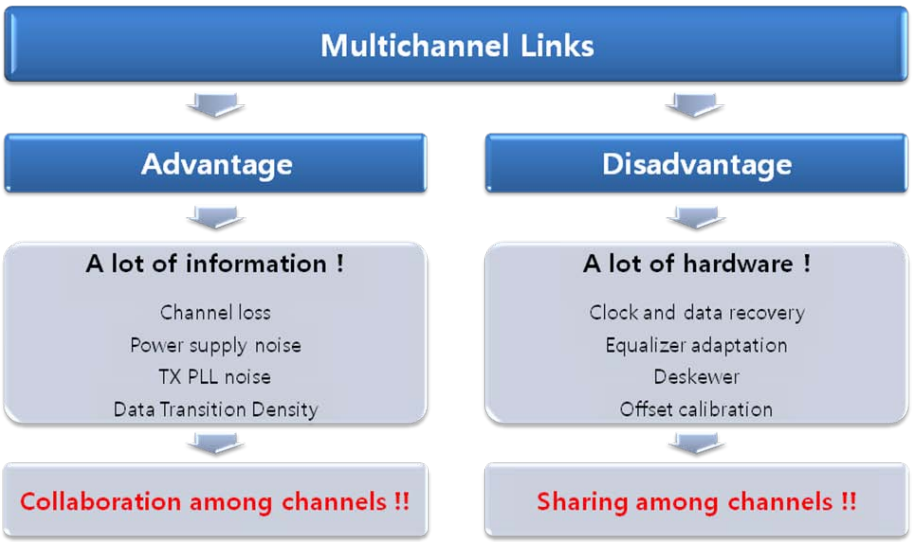


Fig. 1.4 A representative advantage and disadvantage of multichannel links.

The typical disadvantage is an increase in the hardware requirements. With the explosive increase in the number of channels, each CDR and common functional block for an equalizer adaptation, offset calibration, and de-skewing occupy a large area and consume much more power. One of the solutions for this problem is a hardware sharing technique among channels. The common functions among the channels can be shared and alternatively processed by a single global logic, resulting in a reduction of the hardware complexity of the entire receiver and simplifying the components of each lane. In contrast, the typical advantage of a multichannel receiver is the considerable amount of information which can be commonly tracked

and used in every lane. The channel loss, power supply noise, and TX PLL noise should be calibrated in the receiver to achieve a higher BER, and the number of data transitions should be combined and used for constant loop dynamics.

With this background, this research is motivated by the idea of creating two types of multichannel receivers, the first with very low hardware complexity and the second with superior tolerance against various types of environmental noise. The first is a multichannel clock and data recovery (CDR) circuit that employs binary phase detectors (PDs) while achieving linear loop dynamics with collaboration among the channels. The proposed CDR recovers the linear information of phase errors by exploiting its collaborative timing recovery architecture. Because the collaborative CDR combines the PD outputs of multiple data streams, one can add a deliberate phase offset to each PD to realize a high-rate oversampling PD without additional PDs. These deliberate phase offsets make it possible to remove the critical nonlinearity problem of a binary PD caused by the various jitter conditions of the data stream. Therefore, the first receiver focuses on improving the linearity of the PD by collaborative edge sampling among the channels while reducing the lane complexity by facilitating the sharing of the timing recovery circuits for the generation of the global clock. The second receiver employs forwarded clock architecture. The proposed source-synchronous receiver has a simple data link channel using a global calibration control logic which is shared among channels. The global calibration logic controls all common functions of channels to minimize the channel complexity, while single data lane consists of only a continuous-time linear equalizer, two half-rate samplers, and a 64-to-2 deserializer. All of the

functions to adjust the linear equalizer and to find the center of the data are performed in the global calibration control logic implemented externally with an FPGA. Therefore, this low channel complexity meets the needs of good channel scalability and cost-power optimization.

In conclusion, the proposed collaboration and sharing technique among channels has the potential to become a widely used type of multichannel architecture. The collaborative edge sampling technique will be helpful to design a reliable receiver regardless of different types of environmental noise and the sharing technique will be helpful to reduce the hardware complexity thus provide a solution for the increased cost of multichannel links. Prototype chips were fabricated in both 45nm and 90nm CMOS technology. The measurement results show that the designed receivers are suitable for multichannel architecture, with excellent performance.

1.2 Thesis Organization

This thesis is organized as follows. Chapter 2 introduces previous architectures of serial data communication transceivers. The building blocks and architectural issues of receivers for multichannel serial links are summarized and prior receivers in papers are reviewed briefly. Chapter 3 analyzes the loop dynamics of the implemented PLL-based CDR and describes the collaborative timing architecture. The linearization technique of the BBPD is proposed and an overview is given. Chapter 4 proposes the design of the DLL-based forwarded clock receiver and explains the detailed implementation of the global calibration logic. After the analysis and explanation of two types of receivers, experimental results with the fabricated prototype chips are shown in the last parts of each chapter. Chapter 5 concludes the work.

Chapter 2

Previous Receivers for Serial-Data Communications

2.1 Classification of the Links

This chapter describes the two types of link architecture for wireline data communication systems. After introducing a parallel and a serial link, the latest architecture trends and related design issues pertaining to modern serial links will be described.

Most inter-systems or chip-to-chip communication systems use either parallel links or serial links, as shown in Fig. 2.1. Each link is characterized by the number of channels and data streams. The parallel link transmits multiple data streams through multiple channels, as shown in Fig. 2.1(a). In addition to the data, the clock generated from the TX is also transmitted through the channel, which length is equal

to the data lane. The transmitted clock is commonly recovered by the DLL to generate the multiphase clock and to delay the clock to optimize the sampling phase in the RX. The transmitted data are then sampled at the samplers in the frontend of the RX by the recovered clock. There are numerous studies that use the parallel link architecture adapted to short-distance communications such as a ISA, ATA, PCI, and others [2.1]-[2.4].

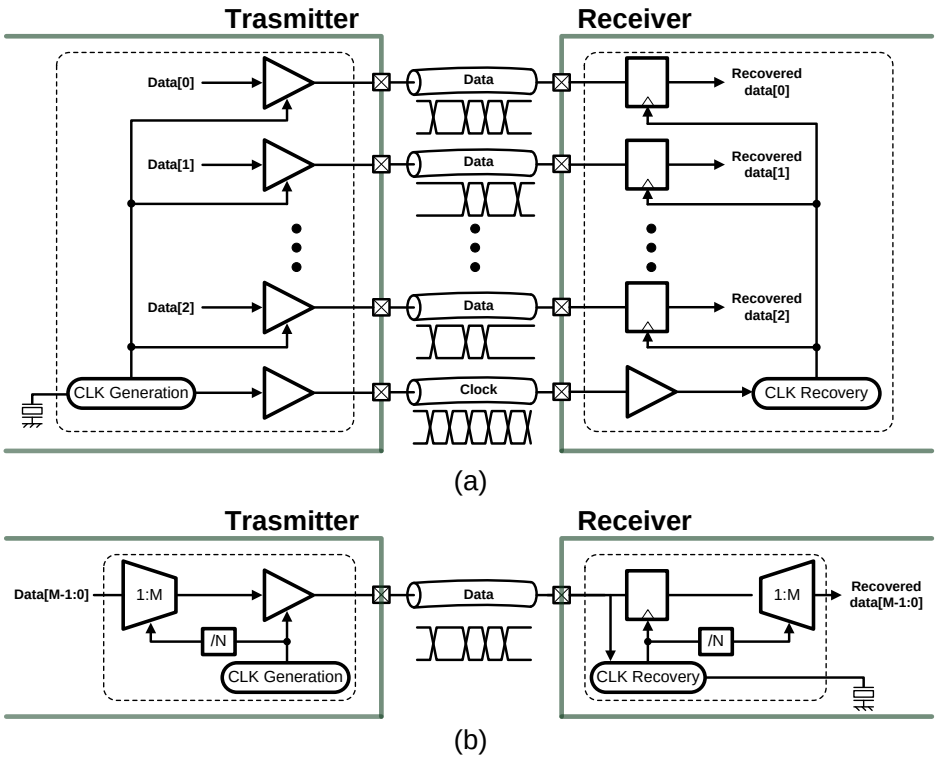


Fig. 2.1 Classification of links, (a) parallel link and (b) serial link.

The use of parallel links can achieve a higher data transmission rate due to the increase in the number of channels with low hardware complexity. However, the skew among the multiple channels, as generated by channel mismatch, clock-tree

mismatch, or the front-end circuit mismatch of the RX, for instance, leads to a critical problem related to the speed budget of the system. Moreover, numerous channels require a large area and high power consumption while also increasing the manufacturing cost. The PCB design is also very difficult due to the complicated signal routing. Therefore, the parallel link architecture is generally utilized for short-distance applications.

In contrast, serial links are widely used in long-distance communication systems. As shown in Fig. 2.1(b), the serial link transmits serialized data through a single channel [2.5]-[2.9]. The transmitted data is sampled by clocks which are recovered in the RX clock generator. Because the clock should be recovered from the incoming data stream without synchronization, the clock recovery circuit is commonly a PLL or PLL with a DLL. The sampled data are then parallelized by a deserializer to communicate with the digital processor. Unlike the parallel link, the serial interface does not require any skew calibration while achieving a very high data transmission rate. However, the added blocks of the data encoder and decoder, serializer, and deserializer increase the hardware complexity.

Nonetheless, the dramatic improvement of CMOS technology has accelerated the architectural shift from parallel links to serial links for short-distance applications as well as long-distance applications such as SATA or PCI-Express. The increased logic speed reduces the hardware complexity, and the scaling down of CMOS devices reduces the core area. Moreover, the single channel greatly reduces the cost such that many applications now adopt the serial architecture. As the data transmission rate per second reached tens of gigabits, serial links are now used many

applications due to this advantage. However, the recent I/O speed has reached its limit, and new types of architecture are required.

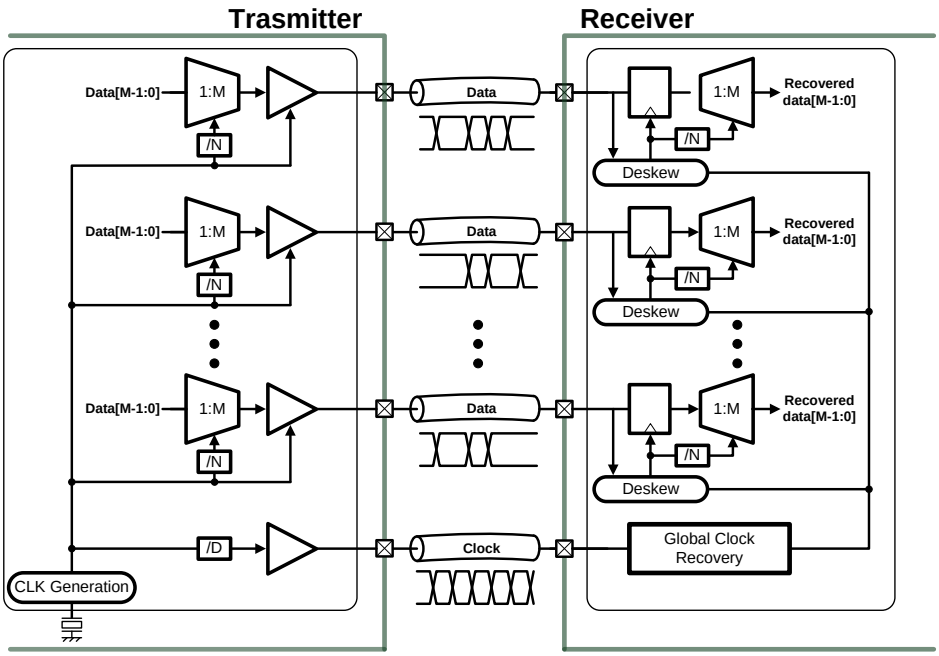


Fig. 2.2 The architecture of multi-channel serial-link.

Ironically, the multichannel architecture has again come to the fore to overcome the saturation of the I/O speed. Although the multichannel design is very similar to that of parallel links, implying that the skew problem remains among the channels, the each lane is based on the SER-DES architecture. As shown in Fig. 2.2, the multichannel serial link consists of deserializers, serializers, samplers, the de-skewing logic, and the global clock recovery circuit. Of course, a forwarded-clock channel does not always exist in the receiver. However, the source synchronous clocking scheme is being spotlighted as a high-speed solution to improve the jitter

tracking performance and thus improve the BER. Because the forwarded clock is correlated with the data stream and because both of them are transmitted from same clock source in the TX, a very high jitter-tracking bandwidth of more than 100MHz can be achieved [2.10] [2.11].

In addition to the skew problem, the multichannel links occupy a large area and require numerous I/O pins while also increasing the power consumption. Therefore, next-generation multichannel links should focus on reducing the cost. Moreover, information about the timing recovery will be helpful to improve the performance, such as the BER and the jitter of the recovered clock. A simple type of lane architecture is one of the keys to solving this problem. The simplified lane architecture will allow the number of channels to be easily expanded for a higher aggregate I/O bandwidth. Another solution to reduce the cost is sharing among the channels. Common functions such as skew calibration, offset calibration and timing recovery can be repeated by a shared block among multiple lanes. To improve the receiver performance, the collaboration among the channels will be a powerful technique. Because each lane transmits a data and clock with common timing information through very similar channels, PCB transmission lines, IC packages, and other such factors, collaborative techniques regarding the frequency and phase recovery will improve the BER or jitter performance.

2.2 Clocking architecture of transceivers

In addition to the number of channels, the links can be classified by the clocking methodology. In digital systems, the clock is very important because the transmitted and received data are synchronized by sampling clocks. To secure the timing margin when the clocks sample the data, synchronization between the data and the clock should be commonly guaranteed. This synchronization is determined by the relationship between the frequency and phase of the clock and data. There are five types of digital systems according to the frequency and phase difference between the data and clock [2.12]. These are the synchronous, mesochronous, plesiochronous, asynchronous, and periodic clocking types. These clocking schemes are closely related to system performance measures such as the jitter tracking, BER, jitter tolerance (JTOL), and the amount of jitter. Thus, a proper clocking scheme should be selected for each application based on the required specifications.

Fig. 2.3 shows a block diagram of a synchronous clocking system. In the synchronous system, the data is transmitted with a clock which is used to retime the data in the TX. This clock is only used to sample the data in the RX and not for passing through any buffers or clock-distribution logics. All of the conditions, including the length of the channels and the strength of the TX driver are equally applied to the data and clock. Hence, there are no frequency or phase differences between the clock and the data; i.e., the frequency of CLK_{TX} is equal to that of CLK_{RX} in Fig. 2.3. These well matched frequencies and phases guarantee a much

higher timing margin in the receiver compared to other types of clocking systems while lowering the BER. Also, the jitter tracking ability can be improved because the samplers in the RX use the same clock used with the TX. However, it is impossible for the path of the clock to be perfectly matched to that of the data, because many components in the paths of the clock and data cannot be perfectly designed for each other. These types of mismatches in the external components of the chip, such as the package, connectors, and PCB transmission lines and the internal components such as the clock tree, parasitic capacitances of the paths, and the local or global PVT variation leading to critical offsets of the paths of the clock and data. Consequently, the synchronous clocking system is generally suitable for short-channel applications such as an inter-system. Even with such systems, the mismatches generated from the external and internal components should not exceed the timing budget, which can be defined by the ISI, the underlying random noise, the setup time and the hold time of the samplers in the RX. Therefore, a means of reducing mismatches is very important in a synchronous system.

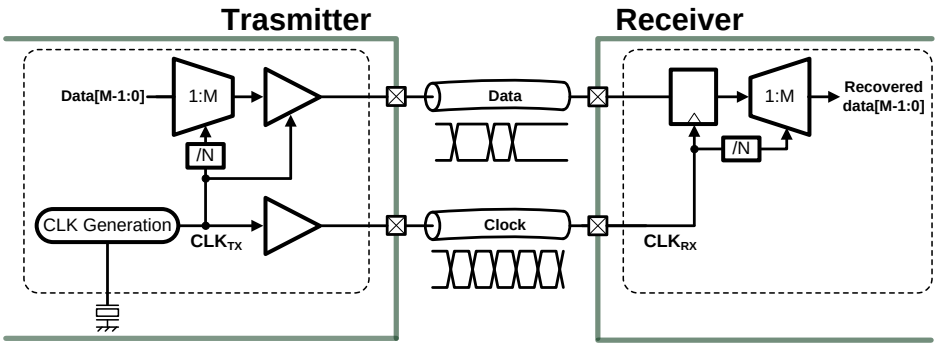


Fig. 2.3 Synchronous system

Unlike the synchronous system, the mesochronous clocking system needs retiming circuits in the receiver side, as shown in the Fig. 2.4. While the data is also transmitted with a frequency-synchronized clock so that the frequency of the receiving clock is matched to that of the data, its phase is not related to that of the data; i.e., the frequency of CLK_{TX} is equal to that of CLK_{RX} but the phase of CLK_{TX} is potentially different from that of CLK_{RX}.

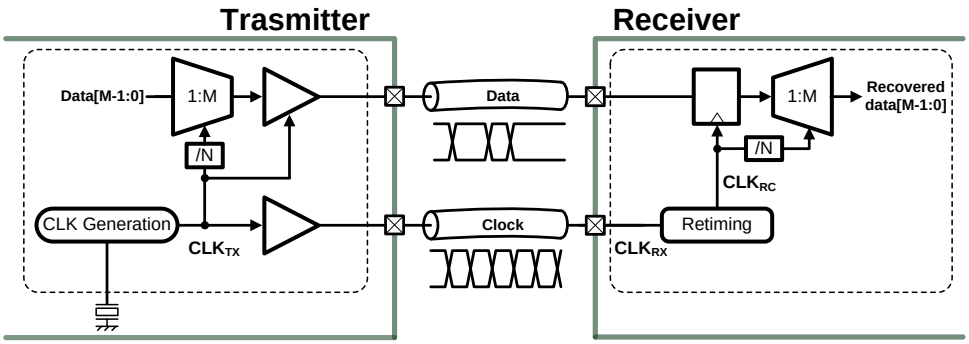


Fig. 2.4 Mesochronous system.

Thus, a retiming circuit or de-skewing circuit such as an injection-locked PLL, a DLL, or a phase rotator is required in the RX. With the retiming circuit, the required timing margin can be alleviated because the phase of the received data is equal to the phase of CLK_{RC}, as illustrated in the Fig. 2.4. However, the wide difference in the paths still causes a critical problem, such as a low BER and poor jitter tracking ability. Although the mesochronous clocking architecture is simpler than the plesiochronous and asynchronous types, it requires a clock channel and a retiming circuit while requiring more complex hardware than the synchronous architecture.

Therefore, the mesochronous clocking system is widely used in short-distance applications such as display interfaces and memory interfaces.

Plesiochronous clocking systems do not have a clock channel, unlike synchronous systems and mesochronous systems, as described in the Fig. 2.3 and the Fig. 2.4. Instead, a local oscillator is used for frequency locking in the receiver, as shown in Fig. 2.5. After the frequency lock, the frequency of CLK_{RX} is slightly different from that of CLK_{TX} such that frequency acquisition circuits are required. In addition to the frequency, its phase is also undefined, as it is independent of the phase of the incoming data. Therefore, the plesiochronous system commonly requires frequency detection logic and phase detection logic components. In comparison with previous systems, because the plesiochronous clocking system does not require a clock channel, it is suitable for relatively long-distance applications such as Ethernet and SONET/SDH. Also, the architecture can be used with optical communications with optical devices such as a laser diode or a photo diode.

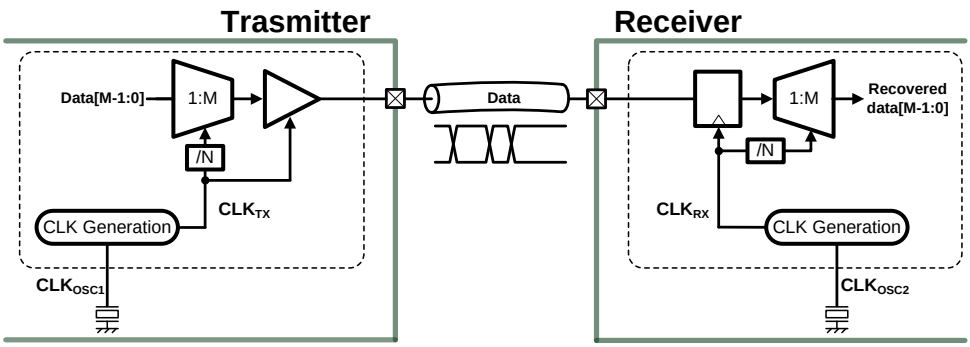


Fig. 2.5 Plesiochronous system.

On the receiver side, the plesiochronous system should recover the sampling clock from the reference clock to synchronize its frequency to that of the incoming data. Therefore, the receiver generally consists of a clock and a data recovery circuit (CDR).

Fig. 2.6 shows a block diagram of the asynchronous clocking system. An asynchronous system does not require an additional clock channel, like the plesiochronous system. However, the frequency of CLK_{RX}, which is generated from the clock generation circuit in the RX, is not correlated with the data rate. Instead of the frequency lock, a digital buffer such as an elastic buffer is used to save the bits of incoming data. The buffer solves the clock boundary problem with two pointers for input and output. Because there are no retiming circuits, the clock distribution on the receiver side can be more flexible. However, with a greater frequency difference between CLK_{RX} and CLK_{TX}, a larger size buffer is required to prevent data overflow. Moreover, the data rate is limited by the low-speed digital buffer. Consequently, the asynchronous system is generally used in short-distance and low-speed applications.

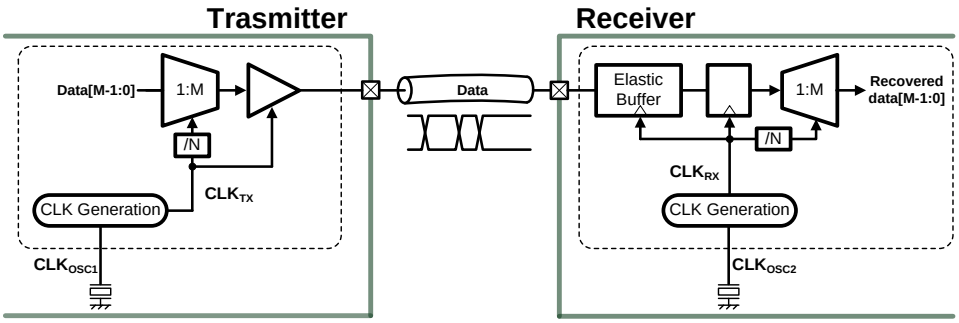


Fig. 2.6 Asynchronous system.

2.3 Components of receiver

There are numerous components which comprise a general receiver of a serial link. Regardless of the clocking system type, an equalizer is required in high-loss systems or in systems with high data transmission rates to offset the channel loss. In addition to the equalizer, the CDR is the most important block in the plesiochronous system. The frequency and phase error between the sampling clock and the received data directly affect the receiver performance, such as the BER and jitter. The CDR generally consists of a phase detector, a frequency detector, a charge pump (only in the case of an analog CDR), a loop filter, and a DCO or VCO. In the case of a source-synchronous system, including the synchronous clocking and mesochronous clocking systems, a clock generator or a clock distribution circuit is required. Also, the de-skewing circuit is the most important block for guaranteeing high receiver performance. Above these blocks, many components are required according the type of receiver architecture. This section explains the channel loss effect, after which the basic components of the receiver among these blocks are introduced and described.

2.3.1 Channel loss

The channel loss is the component that limits the system performance of a high-speed digital communication system most. The source of channel loss in a high-speed digital system can be simply divided into the skin effect and the dielectric loss [2.13].

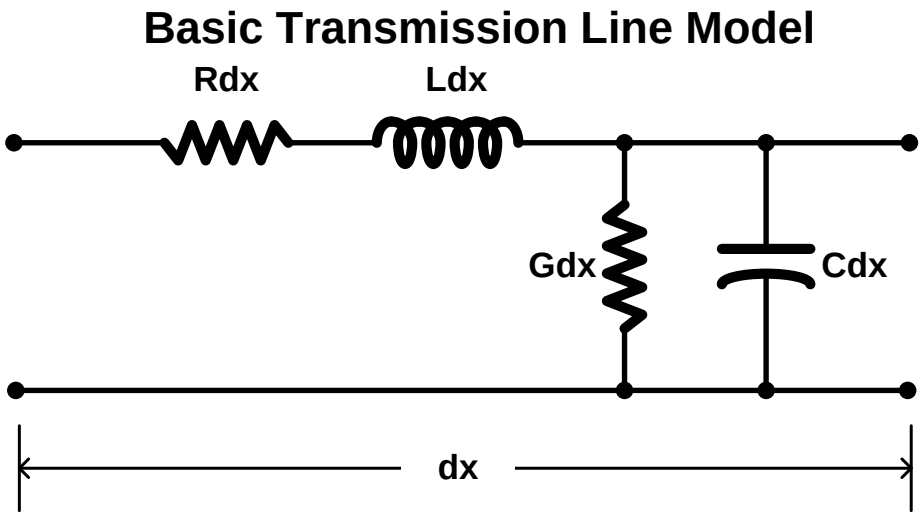


Fig. 2.7 Lumped-parameter channel model.

Before describing the loss, the basic lumped-parameter channel model is shown in Fig. 2.7. The basic transmission line model consists of four parameters: the series resistance (R), series inductance (L), shunt conductance (G), and shunt capacitance (C). The amounts of all parameters in the model are defined as per unit length quantities of *Ω/m, H/m, S/m, and F/m*. Here, *L* represents the total self-inductance of

the two conductors and the *C* represents the capacitance between the two conductors due to their close proximity. The *R* represents the resistance of the two conductors due to their finite conductivity and the *G* is the dielectric loss in the conductors according to their material. Thus, *R* and *G* are the loss parameters of the lumped-parameter channel model (i.e., the RLGC model). With these defined parameters, two important constants, the complex propagation constant and the characteristic impedance, which indicate the characteristics of transmission line, can be calculated. From the time domain equations of the transmission line:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.1}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.2}$$

Thus, those equations can be solved as

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.3}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2.4}$$

where the propagation constant is

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.5}$$

The solutions for the differential equations of Eq. (2.3) and Eq. (2.4) are:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.6}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{2.7}$$

Substituting Eq. (2.6) into Eq. (2.1) gives

$$I(z) = \frac{\gamma}{R + j\omega L}[V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}] \tag{2.8}$$

The characteristic impedance of the transmission line can then be defined by a comparison between Eq. (2.8) and the Eq. (2.7), as follows:

$$Z_o = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.9}$$

If the transmission line is not a lossy channel, with R and G values of zero, the propagation constant is reduced to

$$\gamma = \alpha + j\beta = j\omega\sqrt{LC} \tag{2.10}$$

Thus, the attenuation constant and phase constant are

$$\begin{aligned} \alpha &= 0 \\ \beta &= j\omega\sqrt{LC} \end{aligned} \tag{2.11}$$

In particular, α is termed the attenuation constant of the propagation constant. It is a very important parameter of a lossy channel.

The skin effect of the two loss sources is the tendency of an alternating electric current to distribute itself within a conductor so that the current density near the surface of the conductor is greater than its core. The skin depth is defined as the depth where the current has fallen off to e^{-1} of its original value. The skin depth can also be calculated from Maxwell's curl equation, which is very similar to Eqs. (2.1) and (2.2) [2.14]. If the conductivity of a material is σ (S/m) and the permeability is μ (H/m), the skin depth is as follows:

$$\delta_S = \sqrt{\frac{1}{\pi f \mu \sigma}} \tag{2.12}$$

The effective series resistance of the coaxial cable is then the resistivity (1/σ) over the area, as follows:

$$R_S = \frac{1}{2r}\sqrt{\frac{f\mu\rho}{\pi}} \tag{2.13}$$

Here, r is the radius of the conductor. The effective series resistance of the cable corresponding to the skin depth increases with the square root of the frequency. If the model for the channel is a current distribution shell model, there are many accurate models for the skin effect [2.15] [2.16]. With those models, as calculated in Eqs. (2.12) and (2.13), the skin effect can be utilized as R in the lossy lumped-parameter channel model.

With some insulating materials, dielectric absorption causes frequency-dependent attenuation. This loss is a dielectric loss, and it can be modeled as the conductance G_D between two conductors. The dielectric loss for each material is usually expressed in terms of a parameter, the loss tangent, as follows [2.17]:

$$\tan\delta_D = \frac{G_D}{\omega C} \tag{2.14}$$

Here, C is the capacitance between two conductors. In general, the dielectric constant is a complex number, as follows:

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' \tag{2.15}$$

The loss tangent is then defined by the ratio of the imaginary term and the real term, as

$$\tan\delta_D = \frac{\varepsilon_r''}{\varepsilon_r'} \tag{2.16}$$

Both losses as expressed by Eq. (2.13) and Eq. (2.14) are inversely proportional to the frequency. However, the roll-off ratio of the dielectric loss is larger than that of

the skin effect because R_S is proportional to the root of the frequency, whereas G_D is proportional to the frequency. Fig. 2.8 shows the frequency-dependent lossy transmission line model, which accounts for the skin effect and the dielectric loss. The additional resistance R_S caused by the skin effect of the conductor and the additional conductance G_D caused by the dielectric loss are modeled as summations of the constant resistance R_0 and conductance G_0, which are not dependent on the frequency.

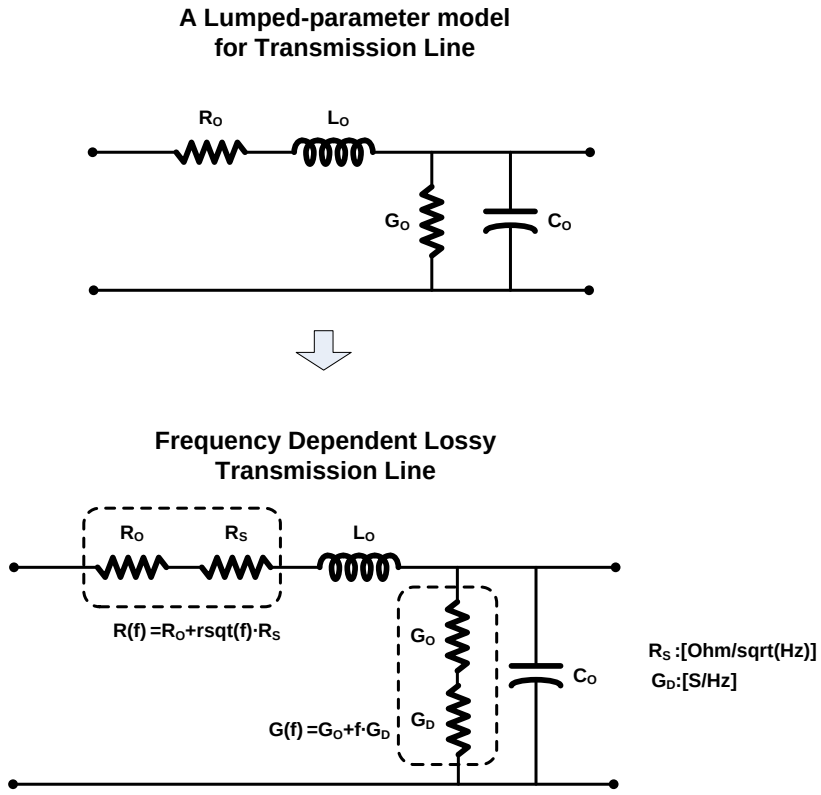


Fig. 2.8 Frequency-dependent lossy transmission line.

The frequency response of the transmission line model is equal to that shown in Fig. 2.9. The skin effect is the most dominant source at a low frequency, but the dielectric loss is more critical at a high frequency. As a result, the overall frequency response of the frequency-dependent lossy transmission line abruptly falls off over the frequency where the dielectric loss starts to increase.

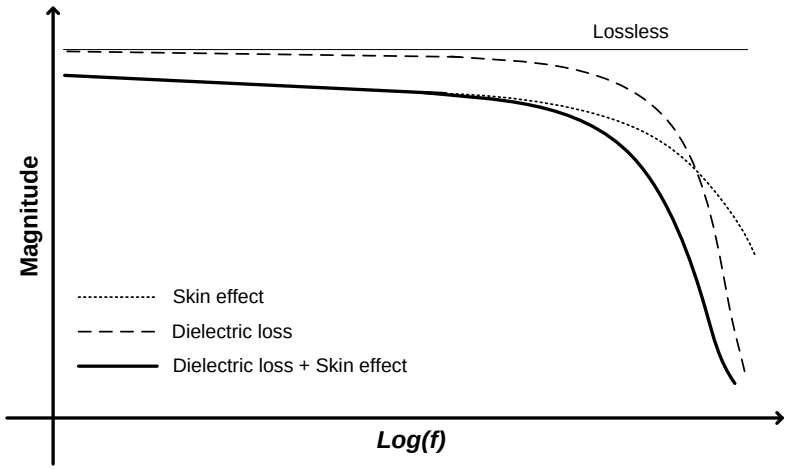


Fig. 2.9 Frequency-dependent attenuation of the channel model.

In this paper, the lossy transmission line model is used to simulate the continuous-time linear equalizer. The actual model based on the measured results of a RG58 coaxial cable is shown in Fig. 2.10. Note that the frequency response over some frequency abruptly falls off, identical to that shown in Fig. 2.9.

Because a digital system usually samples received data in the RX, the channel can also be modeled as a discrete-time system. Fig. 2.11 depicts the discrete-time channel model for a digital sampling system.

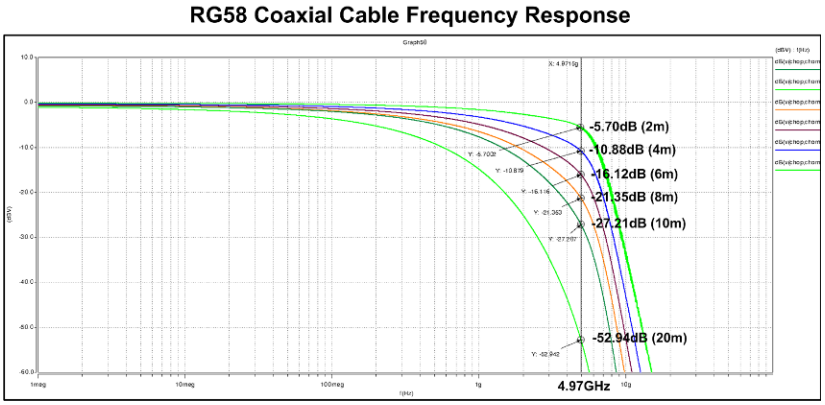


Fig. 2.10 The frequency response of various RG58-coaxial cables.

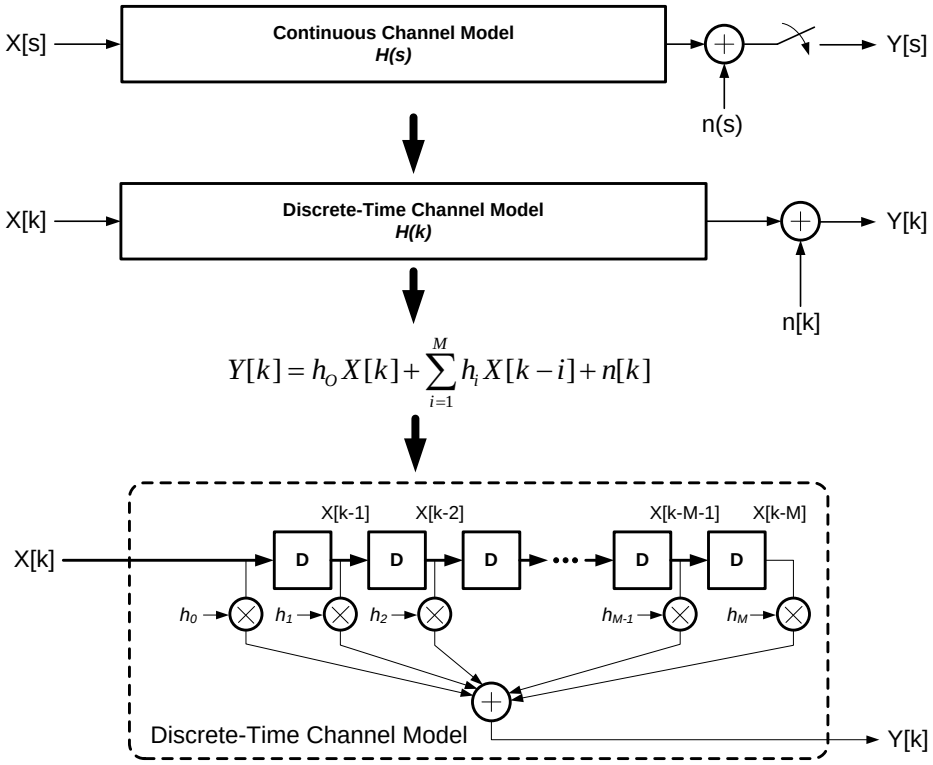


Fig. 2.11 The discrete-time channel model.

Regarding equation of the channel, h_0 denotes the original transmitted channel with some amplification and h_i when i is any integer from 1 to M denotes the ISI component after the channel. Finally, *n[k]* shows the sampled noise components in the receiver.

2.3.2 Equalizer

The ITRS roadmap predicts that the I/O clock rate will increase by 20% per year, whereas the channel bandwidth does not scale at the same rate [2.18]. Therefore, the equalizer will be the key block in high-speed digital communications. Given that the channel basically has a low-pass characteristic, the increased data rate makes transmission without error difficult. In addition, the increased channel length limits the possible data transmission rate. Therefore, recent high-speed digital communication systems frequently require an equalizer to improve the system performance. Although the types of equalizers vary, the target of all equalizers is to offset the loss which is generated when the data passes through lossy channels. Fig. 2.12 shows an eye-diagram of the receiver frontend after passing through RG58 coaxial cables of various lengths.

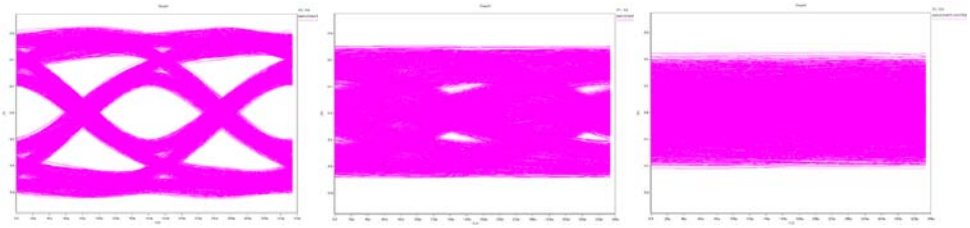


Fig. 2.12 Asynchronous system.

As shown in Fig. 2.12, the high-frequency loss of the channel closes the eye of the transmitted data. Ideally, the equalizer boosts the high-frequency components by the

amount of channel loss, after which the overall frequency response after the channel and the equalizer will be flat under the Nyquist rate of transmitted data, as shown in Fig. 2.13.

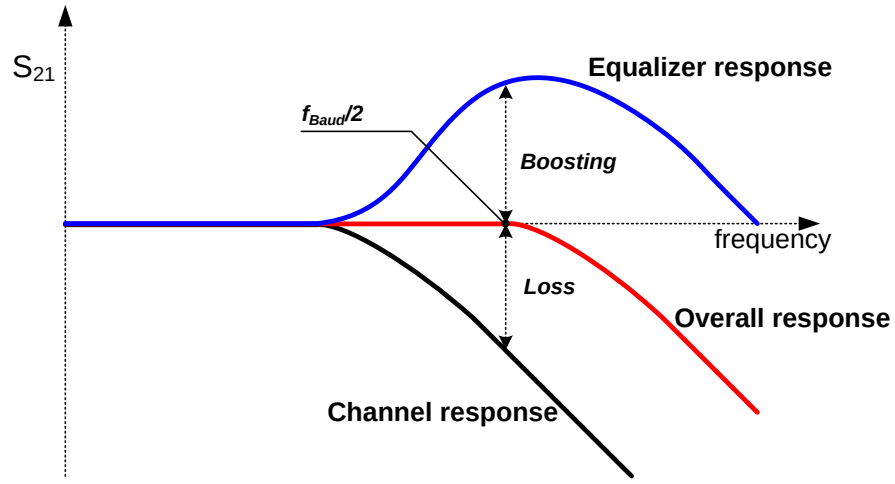


Fig. 2.13 Channel loss and ideal equalization.

To find the exact amount of loss, an elaborate adaptation method is required. Also, a high gain of the equalizer is necessary to compensate for the heavy loss. Many types of equalizers satisfying these conditions exist. The equalizers can be classified by various criteria, such as the on-chip/off-chip, the TX/RX, and the analog/digital control method. The typical off-chip equalizer is the cable-equalization equalizer. Most cable equalizers consist of passive devices which increase both their size and cost. In contrast, the on-chip equalizer is integrated into the chip, making its size very small and its cost low. However, the on-chip equalizer also uses a considerable amount of power and a relatively large size in the IC. Therefore, the design of the

on-chip equalizer should consider its area and power consumption while maximizing its performance. Examples of an off-chip equalizer are the pre-emphasis equalizer, the feed-forward equalizer, the decision-feedback equalizer, and others. On-chip equalization can also be classified in terms where the equalizer is positioned. The transceiver commonly adopts a pre-emphasis or FIR filter, and the receiver uses a continuous-time linear equalizer (CTLE) and a decision-feedback equalizer (DFE). The pre-emphasis equalizer is properly referred to as a pre-de-emphasis equalizer because the equalizer generally attenuates the low-frequency content at a limited supply voltage.

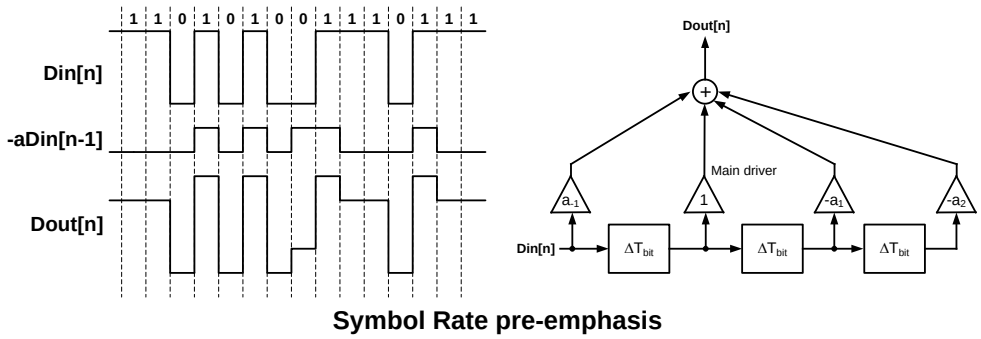


Fig. 2.14 Timing diagram and block diagram of pre-emphasis.

The pre-emphasis equalizer is widely adopted in high-speed digital communication transmitters due to its simple architecture [2.18] [2.19]. The pre-emphasis equalizer consists of delay units and weight-adjusted summation blocks, as shown in Fig. 2.14. The delayed NRZ data is delayed by the symbol rate or the half-symbol rate, and each delay signal is summed after it is properly weighted. The number of delay units is defined by the amount of the post-cursor ISI. The greater the number of tabs, the

more accurate the post-cursor cancellation can be. The result of the summation is illustrated on the left in Fig. 2.14. The high-frequency components of the NRZ data are relatively boosted, whereas the low-frequency components are reduced; as the channel filters out more high-frequency components of the data than low-frequency components, the received data has well-balanced high-frequency and low-frequency components while opening its eye. However, its adaptation requires information of the channel from the receiver by means of the backchannel, which complicates its implementation.

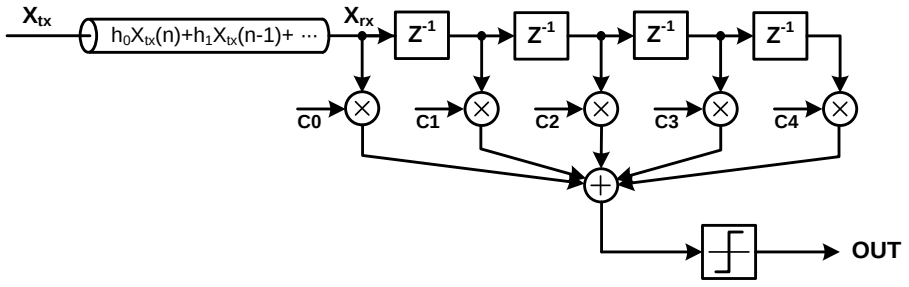


Fig. 2.15 Feed-forward equalizer.

The feed-forward equalizer (FFE) has the same architecture as the pre-emphasis equalizer, as shown in Fig. 2.15. However, it is usually used in the receiver, and its adaptation is easier compared to a pre-emphasis equalizer. Because the received data contains information about the channel loss, its adaptation is possible without a backchannel. Generally, the FFE is compared with the DFE. Because it does not require decision data, it has no timing constraints and has a simple design. A 40 Gb/s seven-tap FFE was reported in the literature [2.20].

In contrast, the decision-feedback equalizer has a more complicated architecture than the FFE. Because the DFE determines the direction of the feedback signal (whether it is positive or negative), it has a timing constraint. The critical delay path limits the speed of the equalizer; hence, a loop unrolling technique which prepares both directions and only selects one of them before the next bit arrives is widely used for high-speed operation [2.21].

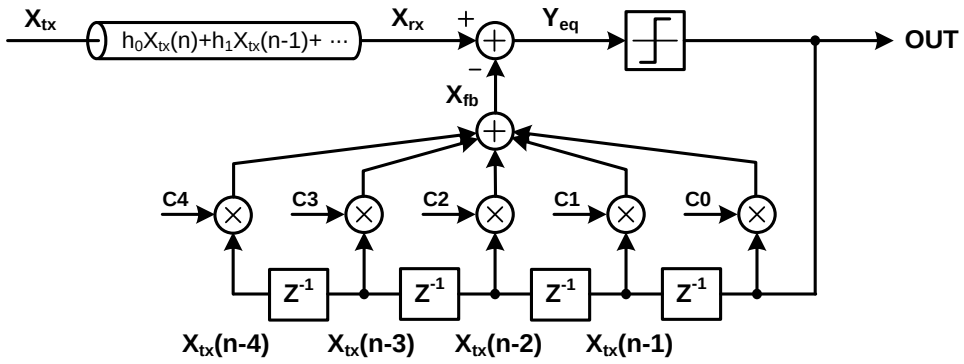


Fig. 2.16 Decision-feedback equalizer.

As shown in Fig. 2.16, the received data after the discrete-time channel model of the Fig. 2.11 is as follows:

$$X_{rx}(n) = h_0 X_{tx}(n) + h_1 X_{tx}(n-1) + ... \tag{2.17}$$

The weighted summation of the feedback signals after the correct decision is

$$X_{fb}(n) = C_0 X_{tx}(n) + C_1 X_{tx}(n-1) + ... \tag{2.18}$$

Therefore, the equalized signal can be expressed as follows:

$$Y_{eq}(n) = h_0 X_{tx}(n) + h_1 X_{tx}(n-1) + ... - C_0 X_{tx}(n) - C_1 X_{tx}(n-1) - ... \tag{2.19}$$

If the DFE coefficient C_0 is zero and C_1 is equal to h_1, Eq. (2.19) is simplified to

$$Y_{eq}(n) = h_0 X_{tx}(n) \tag{2.20}$$

This result is identical to the transmitted signal amplified by h_0. To achieve this result, an accurate adaptation of the coefficients is necessary. There are numerous adaptation algorithms, such as the sign-to-sign LMS algorithm, the blind LMS algorithm, the constant modulus algorithm, and the steepest descent algorithm. With these algorithms, the DFE shows superior performance. However, the summation block of the transmitted signal and the determined signal consume much power, and the digital block for the adaptation is very complicated. Moreover, if the decision is correct when the equalization is started up, the adaptation direction will be incorrect while increasing the BER.

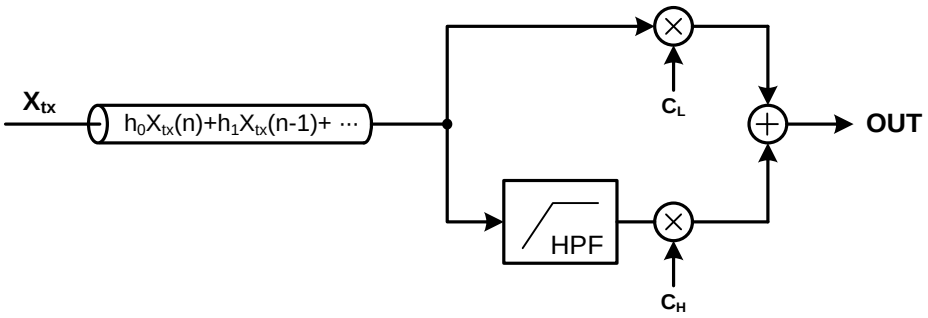
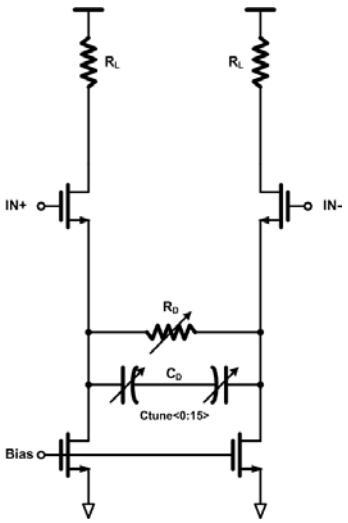


Fig. 2.17 Continuous-time linear equalizer

Unlike the DFE, a continuous-time linear equalizer has a simple architecture, and it is possible to equalize completely closed data. As shown in Fig. 2.17, the CTLE consists of a direct path and a high-pass filtering path. The coefficient C_L determines the amount of DC gain and C_H determines the amount of high-frequency boosting. To boost the high-frequency component, many techniques can be used in the

amplifier. For example, an inductive load in the amplifier boosts the high-frequency signal while generating a zero [2.22]. Also, the source degeneration of a common source amplifier with a capacitor and a resistor will generate a zero. A typical source-degeneration CTLE is illustrated in Fig. 2.18.



$$A_v = \frac{-g_m R_L}{1 + g_m Z_S}$$

$$A_v = \frac{-\frac{g_m R_L}{1 + 0.5 R_D g_m}(1 + sR_D C_D)}{1 + \frac{sR_D C_D}{1 + 0.5 g_m R_D}}$$

$$\omega_Z \approx \frac{1}{R_D C_D}$$

$$\omega_P \approx \frac{1 + 0.5 g_m R_D}{R_D C_D}$$

$$A_{V,Low} \approx \frac{g_m R_L}{1 + 0.5 R_D g_m}$$

Fig. 2.18 Source-degeneration continuous-time linear equalizer

The shunt-connected resistor and capacitor between the source nodes of a differential amplifier generates an additional zero. The location of the zero is determined by the capacitor C_D and load resistor R_D. As shown in the equation of Fig. 2.18, as the pole is located at a higher frequency than the zero, the frequency response of the equalizer contains high-frequency peaking. It should be noted that the low frequency or DC gain is determined by R_D, R_L, and gm. Therefore, a source resistor is commonly used to tune the low-frequency components of the DC gain, while a source capacitor is used to tune the amount of high-frequency peaking.

Despite this, the linear equalizer can easily adjust the gain of the high-frequency components, and the continuous-time equalizer boosts the high-frequency component of the input stream regardless of data or noise. Moreover, a bandwidth extension technique is required to achieve high-speed operation.

2.3.3 Clock and data recovery circuit

In a high-speed digital communication system, the clock and data recovery circuit is the core block. Generally, the frequency and phase between the transmitted data and the internal clock of the receiver are different. Moreover, the data stream has various types of noise, such as supply noise, TX clock jitter, underlying random noise, and ISI, increasing the error of the recovered data. The operation of the CDR can simply be divided into the three parts of a frequency lock, a phase lock, and data sampling. The target of the CDR is accurate data recovery with a low recovered clock jitter while reducing the lock-time of the frequency and phase. To achieve this goal, numerous types of architecture have been reported in the literature. The architecture of the CDR should be properly adopted depending on the application and the targeted performance. In this section, the clock and data recovery circuit based on a PLL is introduced and its components are explained.

2.3.3.1.Basic architecture

A general clock and data recovery circuit employing a charge-pump PLL is shown Fig. 2.19. The CDR commonly consists of a phase detector (PD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a decision logic. Although it is not shown in Fig. 2.19, a frequency detector is also required in the conventional CDR architecture.

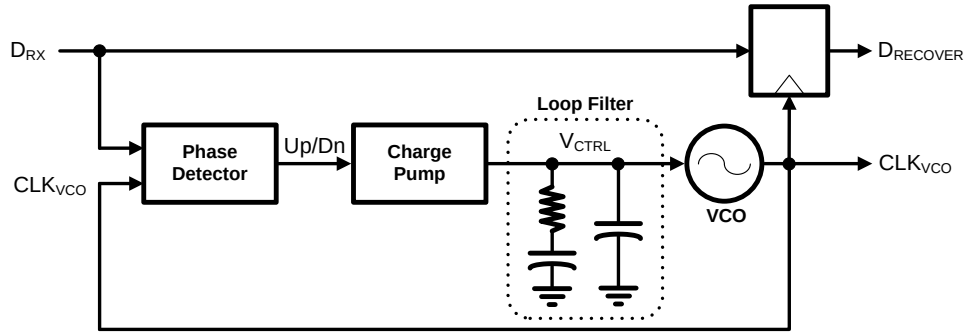


Fig. 2.19 The 3rd-order CDR circuit with a CPPLL

After the frequency of VCO clock is roughly locked to that of the data stream, their phases are also compared at the PD. The PD generates up and down signals according to whether CLK_{VCO} is leading or lagging D_{RX} or depending on how much the phase amounts differ. The charge pump manages the current so that it is proportional to the up and down signals and the loop filter changes the control voltage according to the integrated charge in the loop capacitor and the delta voltage caused by the loop resistor. Finally, the VCO generates the phase- and frequency-locked clock proportional to the control voltage, and the generated clock is used to sample the incoming data stream at the decision logic. This type of decision logic is commonly included in a phase detector, as there is no reason for the phase detection logic and the decision logic to be located in different positions, which could result in critical sampling-phase offset. The recovered data in the decision logic is de-serialized to communicate with the backend digital processing circuits.

Outside of the architecture in Fig. 2.19, the CDR can be designed with many different blocks. For example, the order of the loop filter can be reduced or increase, the phase detector can be designed as a binary or linear PD, and the VCO can be

designed using a LC resonator or a delay line. Moreover, all of the architecture of the CDR can be designed with digital blocks and control signals.

Because the CDR loop shown in Fig. 2.19 has a low-pass characteristic, the high-frequency phase error of the data stream is filtered out. In contrast, as the loop from the VCO to the output clock has a high-pass characteristic, the low-frequency components of the phase noise of the VCO will be reduced. Details of the blocks and an analysis are described in the following sections.

2.3.3.2.Phase detector

The phase detector compares the phase difference between the NRZ data stream and the feedback clock and generates the pulse width, which is proportional to the difference or constant regardless of the amount of the difference. The phase detector either handles linear-phase detection or binary phase detection.

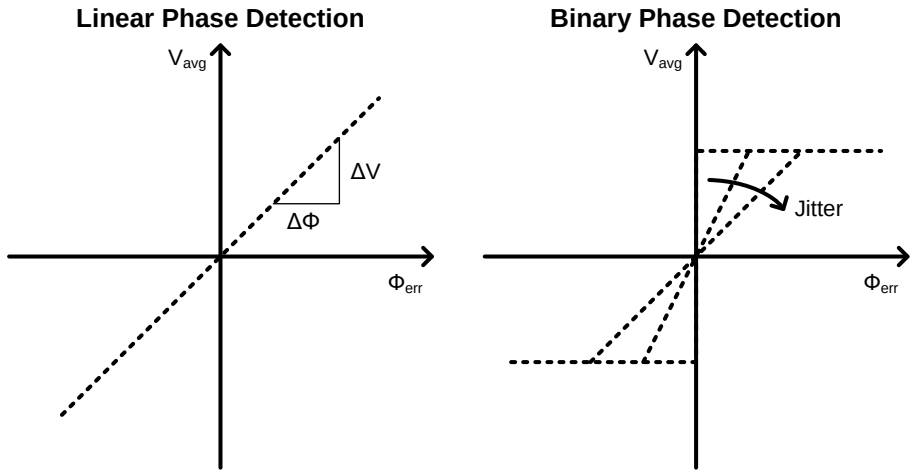


Fig. 2.20 Transfer curves of a linear PD and a binary PD

Fig. 2.20 shows the transfer curves of a linear PD and a binary PD. The output of the linear phase detector is proportional to the direction of the phase error and the amount of phase error. Its transfer curve is always continuous and the slope of the transfer curve is ideally constant within the 1-UI. In comparison, the binary phase detector, or bang-bang phase detector, is discontinuous close to the original lock point; its gain curve cannot be easily defined due to its nonlinearity. Actually, its transfer curve is changed by the amount of jitter, as shown in Fig. 2.20. Therefore, its gain should also be modified by the jitter amount. Statistically, the gain of a binary PD can be expressed by the multiplication of the data transition density, the ideal binary PD output value, and the probability distribution function of the jitter.

2.3.3.2.1. Linear phase detector

The linear phase detector has been widely used in high-speed PLLs, DLLs, and CDRs due to its simple architecture and high-speed performance. The linear phase detector generates two pulses proportional to the amount of phase error and its direction. Because the pulse width of the PD output changes according to the phase difference between two inputs, its transfer curve has a constant slope. The linearized gain curve of the PD makes a CDR loop that can be designed conveniently with constant loop parameters for the PD gain, charge pump current, resistor and capacitor of the loop filter, and the gain of the VCO. Moreover, the linear PD does not generate any pulse when the phase error is close to zero or when a data transition does not exist. This allows the jitter of the recovered clock to be relatively small.

However, the linear PD, which commonly uses an exclusive-or gate without clocking, usually requires limiting amplifiers or high-speed buffers to amplify the received data to a full-swing signal, as the data is often transmitted as a low-swing signal to reduce the transmission power while the channel reduces the data swing. As a result, the linear PD consumes more power than the binary PD.

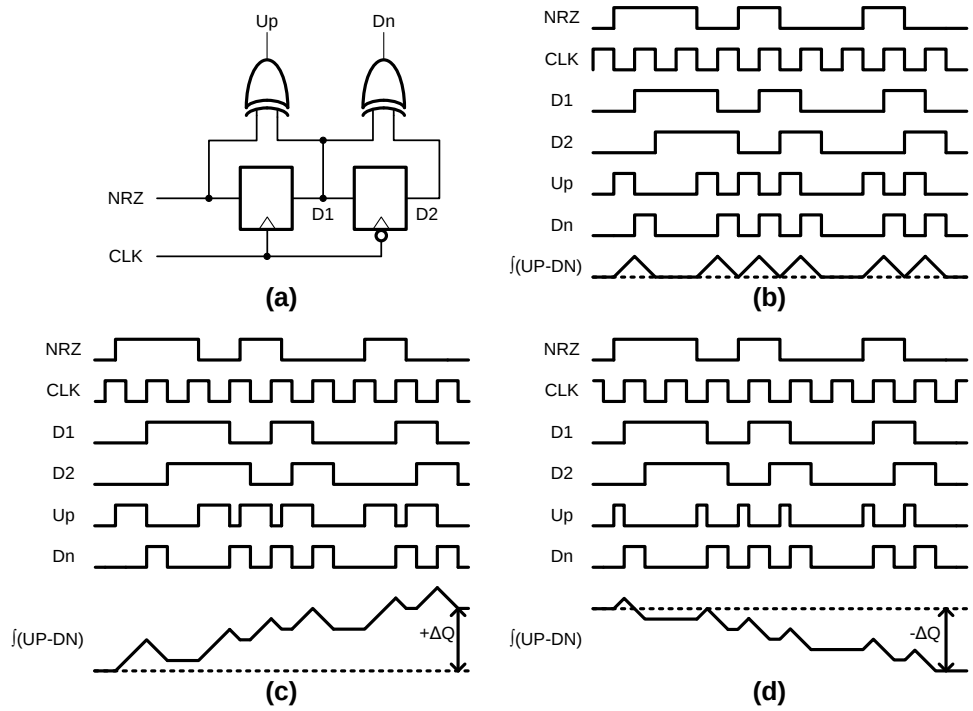


Fig. 2.21 Linear Hogge phase detector. (a) Block diagram. Timing diagram when (b) clock rising edge is aligned at data center, (c) clock is lagging to data by π/2, and (d) clock is leading to data by π/2.

Fig. 2.21 shows an old linear PD known as a Hogge phase detector [2.23]. The Hogge PD consists of two D flip-flops (DFFs) and two exclusive-or gates (XORs). First, incoming data are sampled at the rising edge of the clock, and the output is

then sampled again by the falling edge of the clock. The first sampled data D1 and the incoming NRZ data feed through a XOR gate and its result is the up-signal of the PD. The second sampled data D2 also goes through another XOR gate with D1 and its output is the down-signal of the PD. In this architecture, the down-signal is a reference signal with a constant period of 1/2-UI, whereas the width of the up-signal is proportional to the phase error. For good alignment between the clock and data, the periods of the up-signal and the down-signal are identical to a half-period of the clock, while the integration results of the up-signals minus the down-signals rise and fall by the same amount, as shown in Fig. 2.21 (b). When the clock is ideally locked to the data, the phase difference between the clock and data is π. Fig. 2.21 (c) shows a case in which the clock is lagging the data by $\pi/2$. In this case, the reference down pulse is fixed at half the period of the clock, whereas the pulse width of the up-signal is wider than that. As a result, the integrated up-signals minus the down-signals will increase and the CDR or PLL loop shifts ahead of the clock to reduce the phase error. In contrast, when the clock is leading the data by $\pi/2$, the pulse width of the up-signal is narrower than that of the down-signal, as shown in Fig. 2.21(d). The value of the integrated up-signals minus the down-signals decreases by the amount of the difference between the up pulse and the down pulse.

Going back to the well-aligned case shown in Fig. 2.21(b), even if there is no phase difference between the clock and the data, both the up-signal and the down-signal are generated and their integrated waveform is triangular. This triangular waveform shakes the VCO control voltage while increasing the output jitter. Thus, there have been a few modified Hogge phase detectors reported in prior works

[2.24-2.26]. They use additional XORs and flip-flops to generate more up- and down-signals. For example, a linear PD employing two up-detectors and one down-detector should give a doubly weighted value to the down-signal.

2.3.3.2.2. Binary phase detector

Unlike linear phase detectors, binary phase detectors only compare their direction in terms of whether the clock is leading or lagging. Basically, a binary phase detector adopts a sampling method without an analog amplifier, such as a limiting amplifier or an analog buffer. This binary phase detection mechanism is very simple and enables high-speed operation [2.27]. Moreover, the outputs of the phase detector inherently have a digital waveform, as they are retimed by the clock. These digital up and down values make it possible to design the system as a wholly digitally controlled architecture.

Despite the many advantages that can be utilized in a high-speed digital communication system, there exists a critical nonlinearity problem. Because the output of the binary phase detector is only dependent on the sampled values, its transfer characteristic is changed by the conditions of the input data, such as the ISI and random noise. For example, when greater jitter is shown in the data stream, a lower gain of the phase detector is induced, as shown on the right in Fig. 2.20.

A typical binary phase detector known as the Alexander PD [2.28] is shown in Fig. 2.25. The Alexander phase detector consists of flip-flops and exclusive-or gates, like the Hogge phase detector. However, the Alexander PD uses sampled data to compare the phase relationship between the data and the clock.

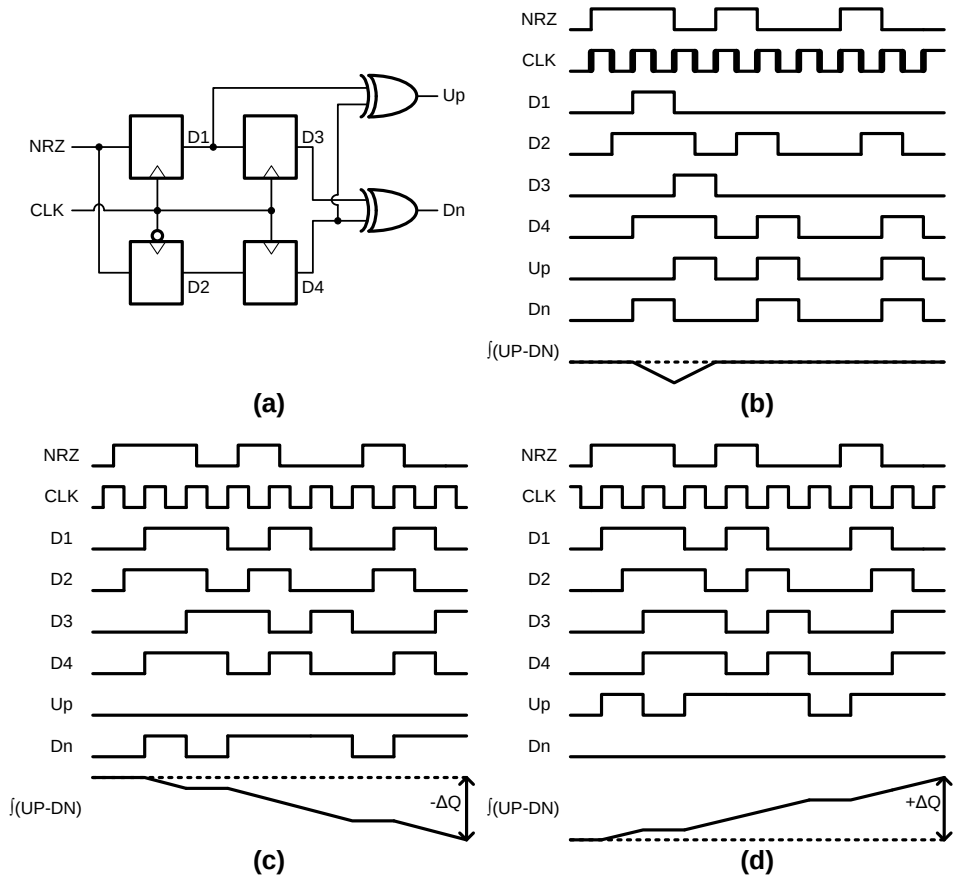


Fig. 2.22 Alexander phase detector. (a) Block diagram. Timing diagram when (b) clock rising edge is aligned at data center, (c) clock is leading to data by π/2, and (d) clock is lagging to data by π/2.

First, the data is sampled twice at the rising edge and falling edge of the sampling clock. Each sampled data instance is then is sampled again by the rising edge of the clock. If the first sampled values at the rising edge of the clock and the falling edge are D1 and D2, and the second sampled values of D1 and D2 are D3 and D4, respectively; the up-signal is the output of the XOR gate between D1 and D4; and the down-signal is the output of the XOR gate between the D3 and D4, as shown in Fig. 2.22(a). When the rising edge of the clock is well aligned with the data

transition, the values of the first sampled D1 and D2 are random due to the jitter of both the clock and the data. If the sampled timing is changed from clock-leading to clock-lagging or from clock-lagging to clock-leading for every data transition, the numbers of generated up and down pulses are statistically equal, as shown in Fig. 2.22(b). In the clock-leading case at $\pi/2$ radian, no up pulses are generated, whereas down pulses are generated during every data transition, as shown in Fig. 2.22(c). In contrast, the lagging clock at $\pi/2$ radian causes only up pulses while generating no down pulses, as shown in Fig. 2.22(d).

As shown in Fig. 2.22(a), the binary phase detector generates only one pulse, either up or down, during every data transition. Therefore, CDRs or PLLs employing a binary phase detector systematically undergo a dithering problem. This bang-bang jitter can be alleviated by the insertion of a dead zone into the binary PD [2.29]. However, because the PD does not detect small amounts of phase error which are narrower than the width of the dead zone, the phase and the frequency of the clock drift until the phase error is larger than the dead zone. This effect also causes periodic jitter in the system. Actually, the Alexander PD generally uses 2x-oversampling at the edge and the data. If the amount of oversampling increases, the intrinsic nonlinearity of the binary PD can be reduced [2.30]. However, an increase in the oversampling requires a considerable amount of additional hardware while occupying a large area and consuming a high level of power.

2.3.3.3.Frequency detector

In the plesiochronous and asynchronous clocking systems, due to the frequency between the transmitted data and the sampling clock of the receiver as well as the phase, a frequency detector is required. Frequency comparisons between periodic signals such as the VCO feedback clock and an external reference clock can be done with a phase and frequency detector (PFD) [2.31].

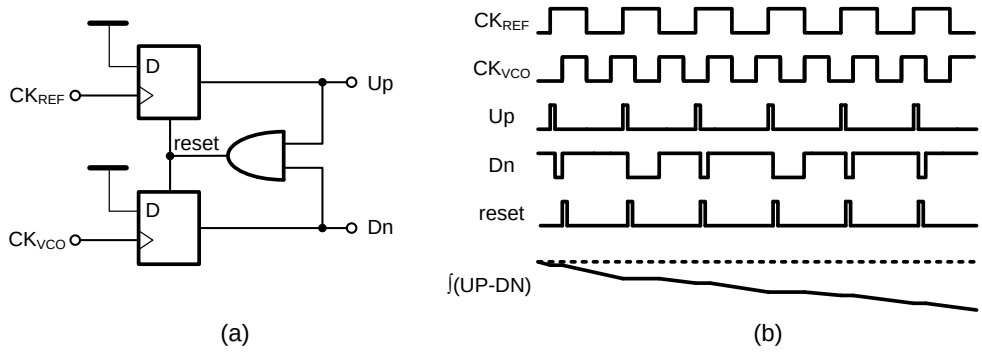


Fig. 2.23 Conventional PFD. (a) Block diagram and its (b) timing diagram when the frequency of CK_{REF} is slower than that of CK_{VCO}.

Fig. 2.23 (a) shows a block diagram of a conventional PFD which consists of two flip-flops with a reset path and an AND-gate. Its timing diagram when the frequency of reference clock CK_{REF} is lower than the frequency of VCO clock CK_{VCO} is shown in Fig. 2.23(b). The up-signal increases at the rising edge of CK_{REF} and the down-signal decreases at the rising edge of CK_{VCO}. If both the up-signal and the down-signal are high, the reset signal is triggered as high and changes both of them so that they have low values. As a result, the up-signal is high during only the delay of the reset path and the down-signal is high during the period from the rising edge of

CK_{VCO} until the triggered reset signal. Although the conventional PFD has a very simple architecture that is easy to implement, it cannot be adopted with random data because the triggering and resets occur randomly.

A FD which can be used in the NRZ data stream is shown in Fig. 2.24. This FD was proposed by Pottbaker [2.32] in 1992 and consists of two double-edged triggered flip-flops and a normal flip-flop, as shown in Fig. 2.24(a). Two clocks, which have a quadrature phase difference, are sampled by NRZ data at their rising and falling edges. The sampled quad-phase clock D1 is sampled again by the rising edge of the sampled in-phase clock D2. The sampled output indicates whether the clock frequency is lower or higher than the data.

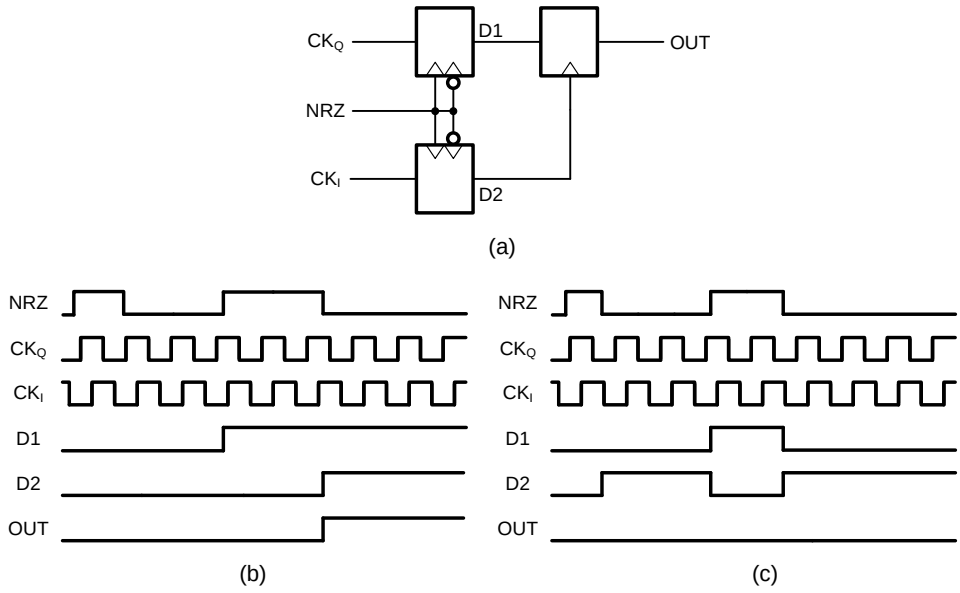


Fig. 2.24 Pottbaker FD (a) Block diagram. (b) Timing diagram when the minimum period of NRZ data is longer than that of CK and (c) timing diagram when the minimum period of NRZ data is shorter than that of CK.

When the frequency of the clock is higher than the data rate, its final OUT will be high, as shown in Fig. 2.24(b), whereas the OUT will be low in the opposite case, as shown in Fig. 2.25(c). This Pottbaker FD also has a very simple architecture. However, it requires quadrature-phase clocks, and the capture range of the frequency difference is very narrow.

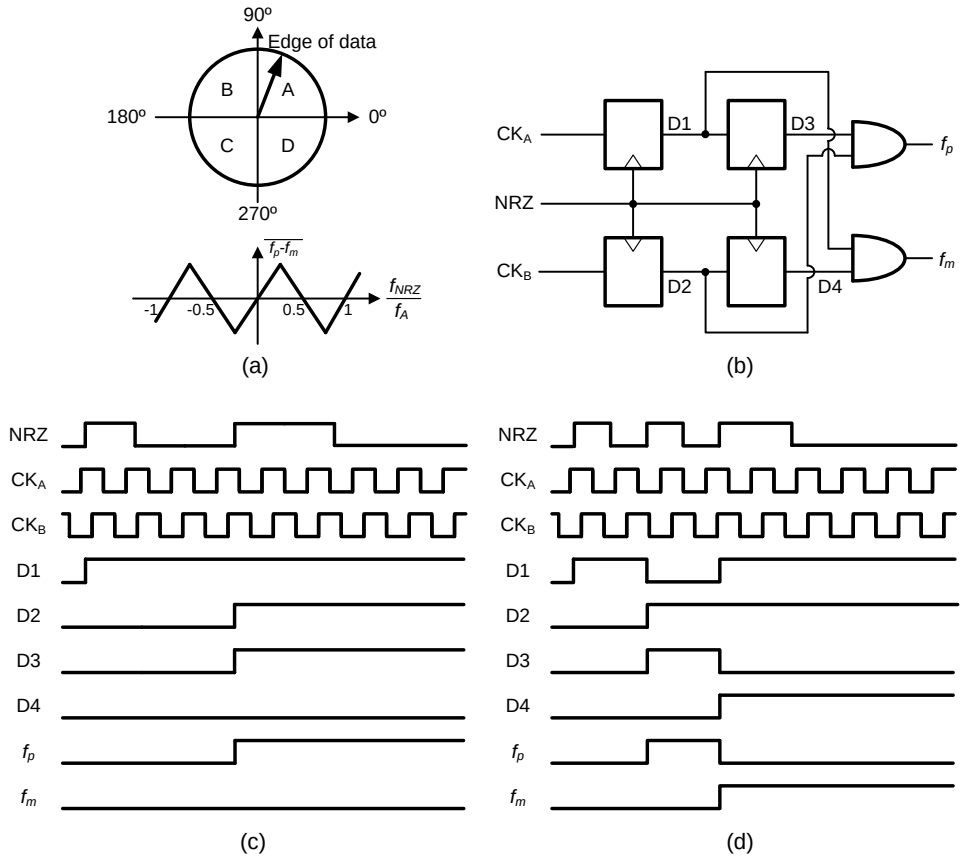


Fig. 2.25 Rotational FD (a) Block diagram. (b) Timing diagram when the minimum period of NRZ data is longer than that of CK.

To achieve a wider frequency capture range, rotational frequency detector can be used [2.33]. The rotational FD detects the directions of the cycle slip when the frequency between the NRZ data and the clock is different. If the frequency of the

clock is higher than the data rate, the cycle slip is generated in the clockwise direction. Otherwise, a lower frequency of the clock generates the counter-clockwise rotation, as shown in Fig. 2.25(a). In this figure, the arrow shows the position of the data edge which rotates according to the frequency error polarity. Fig. 2.25(b) shows one example of rotational FDs, and Fig. 2.25(c) and Fig. 2.25(d) show timing diagrams when the arrow rotates clockwise and counter-clockwise, respectively. Even if the rotational FD extends the frequency capture range by 50% of the clock frequency, as shown in the bottom of Fig. 2.25(a), there is always the risk of a harmonic lock.

Counter-based frequency detectors have a nearly unlimited frequency capture range without any harmonic-lock problems [2.34]. Their detection accuracy can also be improved dramatically. A counter-based PD uses the difference in the counting numbers between two counters which are synchronized to different clock sources.

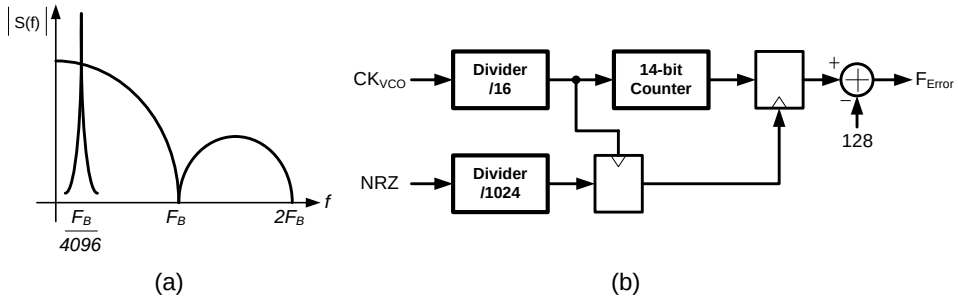


Fig. 2.26 Counter-based FD (a) Spectrum of the divided NRZ data. (b) Block diagram.

Instead of a clock, NRZ data also can be used to operate the counter, identically to using the clock as a source. If the NRZ data passes through a frequency divider, its

spectrum will be changed, as shown in Fig. 2.26(a), where F_B is the data rate. The spread frequency components are converged into the F_B/dividing ratio. Therefore, for every cycle of divided NRZ data, the output of the counter can be compared with a fixed counting value, which is the ratio between the data rate and the clock when the frequency is locked, as shown in Fig. 2.26(b). The compared output is the frequency difference. As mentioned above, the counter-based FD has a superior frequency capture range and superior accuracy. However, its hardware complexity is high and there is a trade-off between the frequency lock time and its accuracy.

2.3.3.4. Charge pump

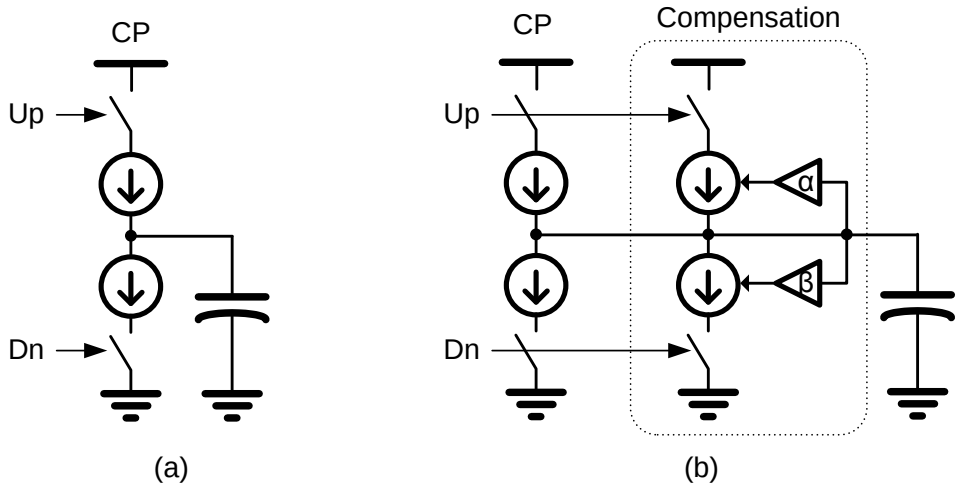


Fig. 2.27 (a) Basic charge pump, (b) charge pump with up and down current mismatch compensation.

A charge pump is an analog block that supplies charge to a loop filter. Generally, a charge pump consists of two current sources for the up- and down-signal that are generated from a phase detector or a frequency detector and two switches for the current sources to connect to the loop filter, as shown in Fig. 2.27(a). Because the charge pump is directly connected to the loop filter, noise and mismatches are very important in the design of the charge pump. The noise shakes the control voltage, resulting in increased jitter of the VCO clock, and the mismatch causes an offset phase and spurious jitter of the clock.

Even if process mismatches do not exist in the charge pump, a current mismatch is generated due to the different operating condition between the up-current source and the down-current source, and it varies with the level of the control voltage. To reduce the current mismatch, an additional charge pump with compensation circuits is added [2.35] [2.36]. The compensation circuit is designed as the replica circuit of the original charge pump and adopts active feedback circuits to compensate for the up- and down-current proportional to the amount of mismatch, as shown in Fig. 2.27(b). If the up-current is larger than the down-current, the gain of the up-current compensation α is reduced while decreasing the up-compensation current. Therefore, the summation of up- and down-current conducting into the loop filter is always constant regardless of the level of the control voltage.

2.3.3.5. Voltage controlled oscillator and delay-line

A voltage-controlled oscillator generates the self-resonating periodic signals proportional to the control voltage in the PLL or the CDR, as shown in Fig. 2.28(a).

Therefore, its gain curve can be expressed by the change rate of frequency in the response to the control voltage; its gain then becomes the ratio of the delta frequency over the delta control voltage, as shown in Fig. 2.28(b). With a limited supply voltage, the VCO has a limited tuning range. The components affecting the tuning range are the quality factor (Q) of the oscillation unit and noise sources generated from the supply voltage and devices.

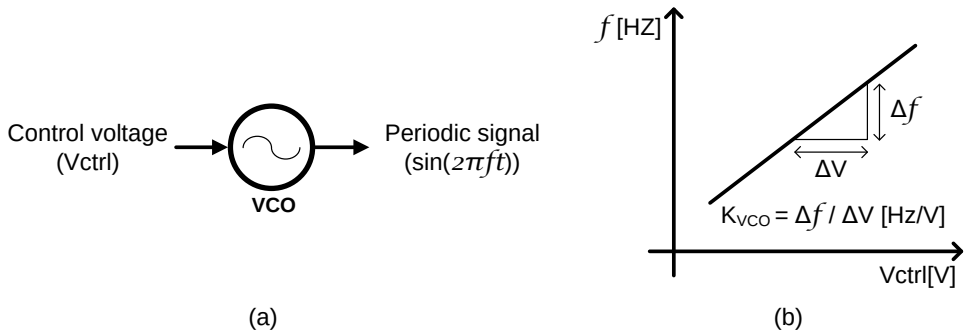


Fig. 2.28 Voltage-controlled oscillator (a) block diagram and (b) gain curve.

The performance of the VCO can be explained by parameters such as the tuning range, its linearity, the power dissipation, the supply rejection ratio, and the phase noise. Among these parameters, the phase noise is the most important consideration, because its result directly affects the jitter performance of PLLs or CDRs. The phase noise can be explained by the well-known Leeson's phase noise model [2.37].

The derivation of the Leeson's phase noise model as shown in Fig. 2.29 is based on a linear time-invariant (LTI) approach to the analysis of noise in oscillators. The Leeson phase noise model is given as follows:

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{2.21}$$

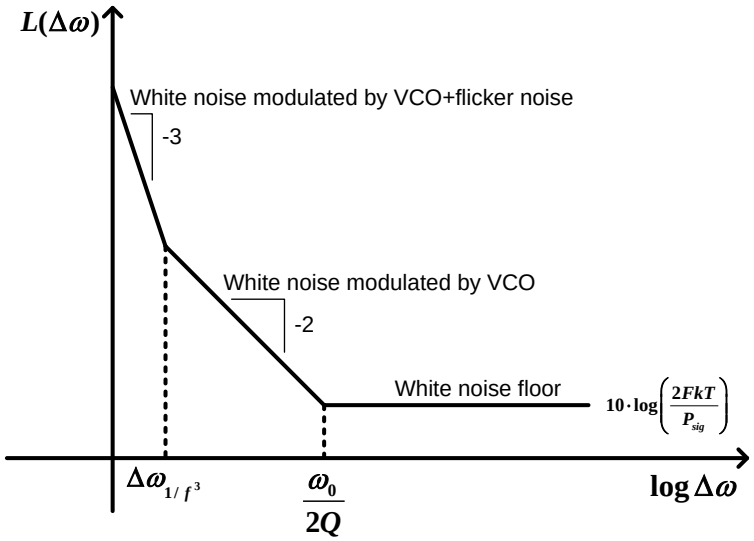


Fig. 2.29 Leeson phase noise model.

Here, Q is the loaded quality factor of the resonator, f_0 is the oscillation frequency, P_{sig} is the signal power of the oscillator, F is the noise factor for an active device, k is the Boltzmann constant, T is the temperature, and $\Delta\omega_{1/f}^{3}$ is the flicker noise corner frequency knee in the phase noise. The Leeson phase noise model shows clearly that three parameters Q, F, and P_{sig} have significant effects on the phase noise of an oscillator. A low oscillator requires a minimum F and maximum values of Q and P_{sig}.

The VCO can be classified as either a LC oscillator or a ring oscillator depending in the resonator type. The LC VCO uses a LC resonator for output oscillation. Fig. 2.30 shows a LC tank with loss and a VCO employing a LC tank. The R value of the LC tank in Fig. 2.30(a) denotes the loss in the tank. Due to the loss resistance, the

LC tank does not oscillate by itself. If the loss of the tank can be counterbalanced by the same amount of negative resistance, the LC tank will oscillate spontaneously.

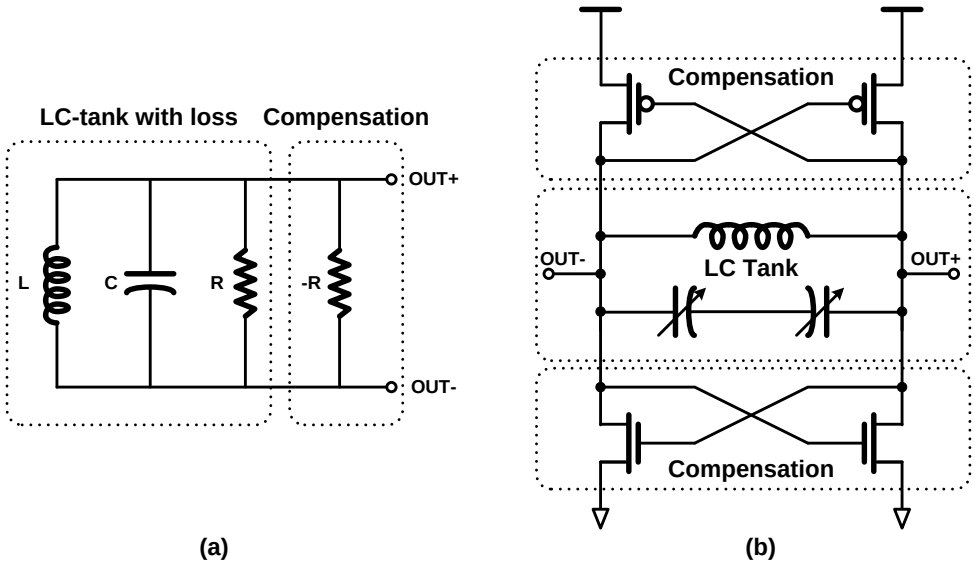


Fig. 2.30 (a) LC-resonant tank. (b) LC-VCO.

To calculate its spontaneous frequency, the output admittance can be used as follows:

$$Y(j\omega) = \frac{1}{R} + j\omega C + \frac{1}{jwL} - \frac{1}{R} \tag{2.22}$$

The imaginary term of Eq. (2.22) can be removed under a specific condition:

$$\omega L = \frac{1}{\omega C} \tag{2.23}$$

The output impedance will be zero, identical to the oscillation condition. The value of ω that satisfies the condition in Eq. (2.23) is called the resonant frequency. It value, ω_0, is as follows:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.24}$$

In the actual design of the LC VCO, the negative resistance $-R$ to offset the loss can be designed as a cross-coupled NMOS or a PMOS pair, as shown in Fig. 2.30(b). Because two negative resistors increase the output capacitance, the tuning frequency will be reduced. Thus, the negative resistors should be designed using small transistors. On the other hand, if the strength is insufficient, the oscillator does not start due to the uncompensated LC tank loss. As a result, because the strength of the negative resistors affects the frequency tuning range and the start-up properties, their strength is properly determined for the targeted frequency.

Another typical way to design a VCO is as a ring oscillator which consists of an odd number of inversion cells, with each cell connected in the form of a ring, as shown in Fig. 2.31. After passing through the odd number of inversion cells, the signal is fed back into the first cell with a phase inverted by 180 degrees. One of the commonly used inversion cells is the current-starved inverter, as shown on the right of Fig. 2.31. The top and bottom transistors of the inverter control the current conducting through the inverter. If the conducting current is low, the delay per stage increases, resulting in a low oscillation frequency; otherwise, the oscillation frequency is high. The oscillation frequency f_{osc} can be expressed as follows:

$$f_{osc} = \frac{1}{2NT_D} . \tag{2.25}$$

Here, T_D is the delay of the unit cell.

In comparison with a LC tank, the implementation of a ring-type VCO is easier and incurs a lower cost, as it does not use a large passive device that requires

accurate modeling. In contrast, it is very sensitive to PVT variations and noise because the oscillation frequency is determined by the amount of current conducting through the inverter cell and the amount of current is affected by the PVT condition and noise. Unlike the ring VCO, the LC VCO is insensitive to PVT variations because its frequency is determined by the LC resonator, resulting in low phase noise. However, its frequency tuning is more complicated and its tuning range is very narrow.

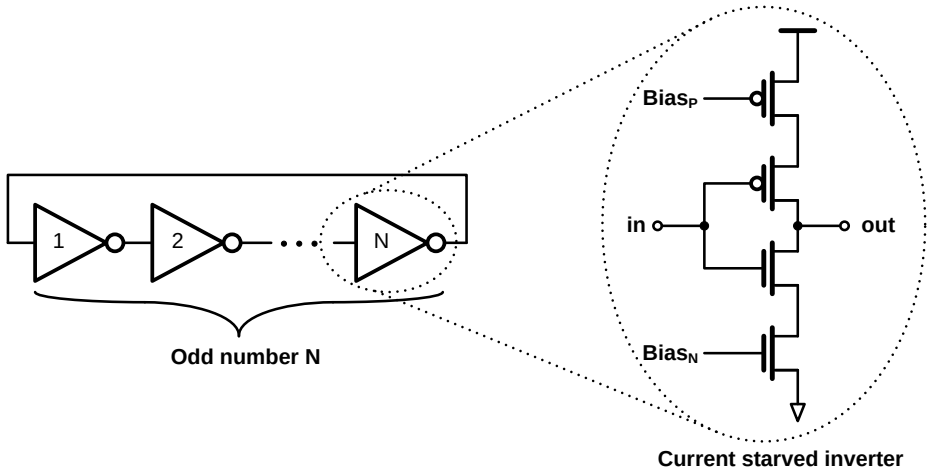


Fig. 2.31 A ring-type VCO and its unit cell.

Similar to the ring-type VCO, the voltage-controlled delay line (VCDL) also consists of multiple delay cells, as shown in Fig. 2.32(a). However, the number of stages N does not need to be an odd number. Moreover, the output of the last cell is not connected to the input of the first cell. Therefore, the VCDL does not create a feedback loop, resulting in its transfer characteristic being constant, unlike the VCO of K_{VCO}/s.

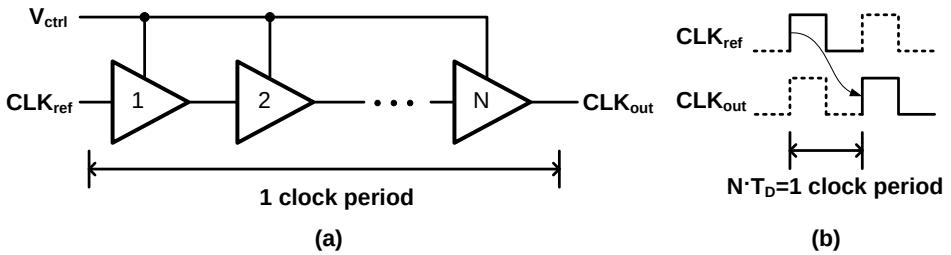


Fig. 2.32 (a) Voltage-controlled delay line and (b) its timing diagram.

Commonly, the total delay time is a multiple of the clock period with the integer K. If K is '1,' the phase difference between the reference clock CLK_{ref} and the output clock CLK_{out} is one clock period. In such a case, each delay of the cell will be T_{ref}/N, where Tref is a single period of the reference clock, as shown in Fig. 2.32(b). There is no self-oscillation in the VCDL; therefore, it has two ports. One is the clock input and the other is the control signal. Like the VCOs, the cells can be designed using a starved inverter or a buffer with a capacitive load, for instance.

2.3.4 Loop dynamics of PLL

A second-order CDR can be modeled identically to a second-order PLL. A simplified block diagram of a second-order charge-pump PLL is illustrated in Fig. 2.33(a). A phase detector compares the phase difference between the reference clock and the feedback VCO clock and generates up- and down-signals proportional to its phase difference. A charge pump supplies charge into the first-order RC loop filter according to the amount of phase error. Then, the control voltage of the loop filter adjusts the frequency and phase of the VCO so that they coincide with those of the reference clock. The reference clock commonly has a lower frequency than that of the VCO to facilitate its implementation. Therefore, the frequency of the VCO clock is divided into some integer or fractional ratio and is fed to the phase detector.

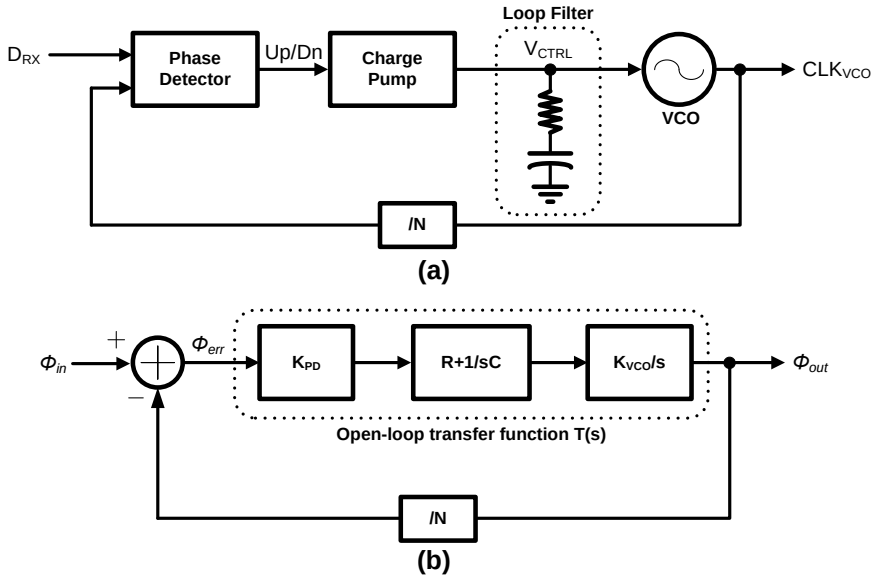


Fig. 2.33 The 2nd-order PLL (a) block diagram and (b) s-domain model.

Like other linear systems, the PLL can also be modeled as an s-domain, as shown in Fig. 2.33(b). This s-domain model provides several meaningful parameters which can be used in the analysis and the design [2.38]. The open-loop transfer function T(s) can be expressed as

$$T(s) = K_{PD} \cdot (R + \frac{1}{sC}) \cdot \frac{K_{VCO} / N}{s} = \frac{K_{PD} \cdot (sRC + 1) \cdot K_{VCO} / N}{s^2 C} \quad (2.26)$$

where K_{PD} accounts for the gains of the phase detector and the charge pump. The zero of the open-loop transfer function is then as follows:

$$\omega_Z = \frac{1}{RC} \quad (2.27).$$

If the phase detector is linear, the unity gain frequency of T(s) is

$$\omega_C = \frac{I_P K_{VCO} R}{2\pi N} \quad (2.28).$$

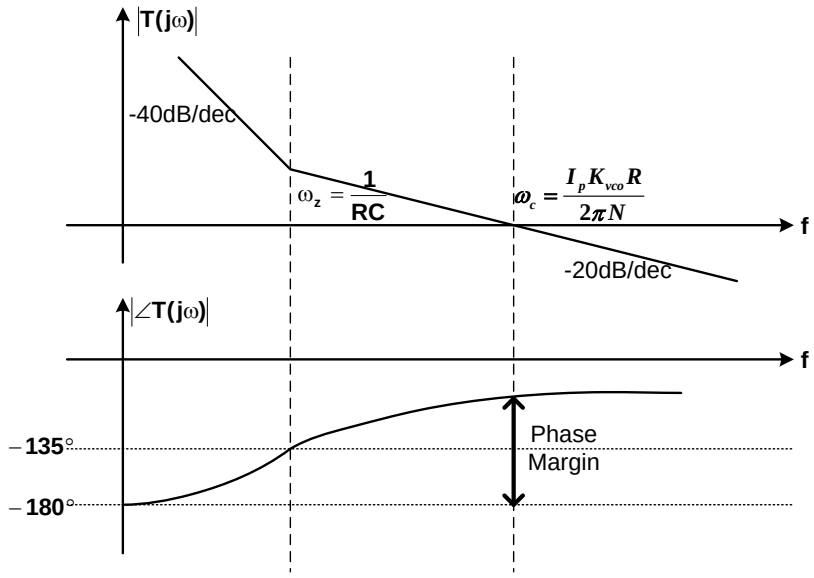


Fig. 2.34 The frequency response of open-loop transfer function.

The frequency response of the open-loop transfer function can be plotted as shown in Fig. 2.34. The phase margin can then be calculated at the frequency ω_C, as follows:

$$\begin{aligned} PM &= \angle T(j\omega_C) - (-180°) \\ &= -180° + \tan^{-1}\frac{\omega_C}{\omega_Z} - (-180°) = \tan^{-1}\frac{\omega_C}{\omega_Z} \end{aligned} \quad (2.29).$$

and

$$\frac{\omega_C}{\omega_Z} = \frac{I_P K_{VCO} R^2 C}{2\pi N} \quad (2.30).$$

As shown in Eqs. (2.27), (2.28) and (2.30), ω_Z should be much lower than ω_C for a high phase margin. Therefore, increasing R, C, I_P, and K_{VCO} improves the phase margin. However, R, K_{VCO}, and I_P also increase bandwidth of the system. Given that the higher bandwidth passes more input noise into the output clock, the parameters should be carefully designed.

The closed-loop transfer function can be written as follows:

$$H(s) = \frac{T(s)}{1+T(s)} = \frac{K \cdot (1+RCs)}{s^2 + KRCs + K} \quad (2.31).$$

Here, $K = \frac{K_{VCO} I_P}{2\pi CN}$. Eq. (2.31) shows the low-pass characteristics of a second-order PLL which has one zero and two poles. Therefore, the second-order PLL has inherent peaking in the frequency response caused by the zero, as shown in Fig. 2.35. This peaking is related to the damping factor. To calculate the damping factor and the natural frequency of the system, Eq. (2.31) can be compared to the classical two-pole system transfer function:

$$H(s) = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{2.32}$$

The damping factor and the natural frequency are as follows:

$$\zeta = \frac{RC\sqrt{K}}{2} = \frac{1}{2}\sqrt{\frac{K_{VCO} I_P R^2 C}{2\pi N}} = \frac{1}{2}\sqrt{PM} \tag{2.33}$$

$$\omega_n = \sqrt{K} = \sqrt{\frac{K_{VCO} I_P}{2\pi CN}} \tag{2.34}$$

Therefore, the increased damping factor can improve the phase margin, whereas the reduced damping factor decreases the phase margin with higher peaking.

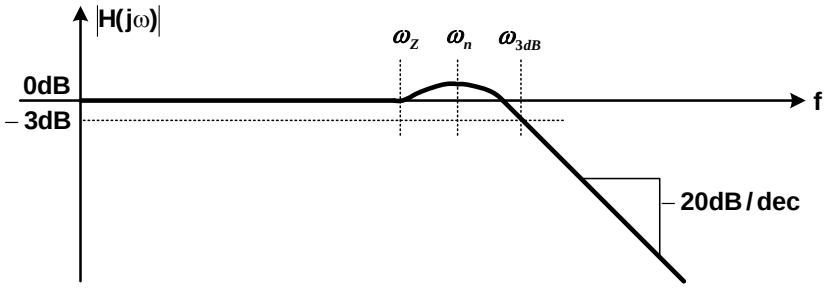


Fig. 2.35 The frequency response of closed-loop transfer function.

From Eq. (2.31), we can calculate the 3-dB frequency as follows:

$$\left|\mathrm{H}(\mathrm{j}\omega_{3\mathrm{dB}})\right|^2 = \left|\frac{jKRC\omega_{3dB} + K}{jKRC\omega_{3dB} + K - {\omega_{3dB}}^2}\right|^2 = \frac{(KRC\omega_{3dB})^2 + K^2}{(KRC\omega_{3dB})^2 + (K - {\omega_{3dB}}^2)^2} = \frac{1}{2} \tag{2.35}$$

$$(KRC\omega_{3dB})^2 + K^2 + 2{\omega_{3dB}}^2 K - {\omega_{3dB}}^4 = 0 \tag{2.36}$$

The solution of Eq.2.36 is approximately equal to

$$\omega_{3dB} \approx 2\zeta\omega_n \tag{2.37}$$

2.3.5 Loop dynamics of DLL

Unlike the PLL, the DLL is an unconditionally stable system because it is a first-order system with one pole. The DLL can be classified into two types [2.39]: a type-I DLL of which the reference is compared to the delay itself [2.40] and a type-II DLL of which the reference is compared to an uncorrelated clock source [2.41]. The type-I DLL is widely used in multiphase generators and the type-II DLL is widely used in clock recovery circuits. In Chapter 4 of this paper, the DLL is used to generate multiphase clocks from the forwarded clock. Hence, the analysis of type-I DLL will be focused on here.

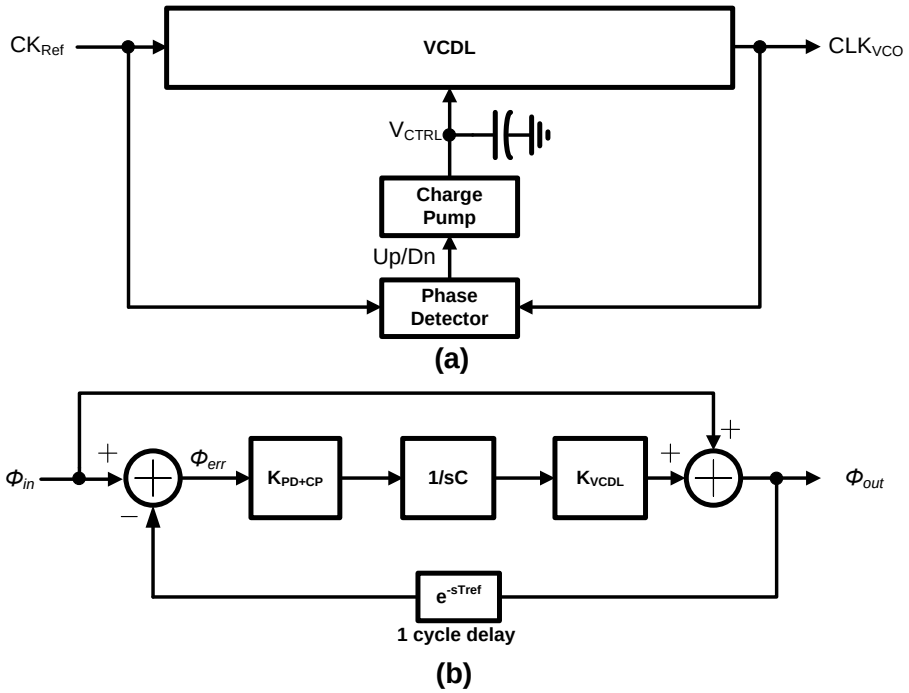


Fig. 2.36 The type-I DLL (a) block diagram and (b) s-domain model.

Fig. 2.36 shows a block diagram and the s-domain model of the type-I DLL. The type-I DLL reference clock is connected to both a VCDL and a phase detector. The VCDL delays the input clock for one-cycle period and the delayed clock is compared to the reference clock at the phase detector. The phase detector generates up- and down-signals in response to the phase difference between the two clocks. Then, a charge pump and a loop capacitor adjust the control voltage of the VCDL for its one-cycle delay. Because the VCDL adjusts the phase of the clock, the transfer characteristic of the VCDL can be expressed as a constant; its unit is radians per volts. Therefore, the entire system is a first-order system that does not require any resistors in the loop filter for loop stability.

Fig. 2.37 shows the s-domain model of the type-I DLL. Unlike the PLL, the DLL has a feed-forward path of a reference clock. In addition, the feedback path has a delay element for a one-cycle delay of e^{-sTref}. This one-cycle delay is caused by the delay of the feedback clock. Inherently, the DLL compares the incoming reference clock with the clock delayed by one cycle at the PD. The open-loop transfer function can be written as follows:

$$T(s) = \frac{K_{PD}K_{VCDL}}{sC} \tag{2.38}$$

Here K_{PD} is the transfer characteristic of the PD and CP, K_{VCDL} is the transfer characteristic of the VCDL, and C is the loop capacitor. The closed-loop transfer function can be written as shown below.

$$H(s) = \frac{1+T(s)}{1+T(s)\cdot D} = \frac{s+\frac{K_{PD}}{C}\cdot K_{VCDL}}{s+\frac{K_{PD}}{C}\cdot K_{VCDL}\cdot e^{-sT_{ref}}} \tag{2.39}$$

In this equation, D is the one-cycle delay e^{-sTref} of the feedback path and T_{ref} denotes one period of the reference clock. Assuming a small value of sT, the delay e^{-sTref} can be replaced by $1\text{-}sT_{ref}$. The closed-loop transfer function is then

$$H(s)=\frac{s+\frac{K_{PD}}{C}\cdot K_{VCDL}}{s(1-T_{ref}\frac{K_{PD}}{C}K_{VCDL})+\frac{K_{PD}}{C}\cdot K_{VCDL}}=A\cdot\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_P}} \qquad (2.40).$$

where ω_z is a zero and ω_p is a pole of the system. The zero and the pole can be expressed in terms of the transfer characteristic of each block, as follows:

$$\omega_z=\frac{K_{PD}K_{VCDL}}{C}$$
$$\omega_p=\frac{K_{PD}K_{VCDL}}{1-T_{ref}\frac{K_{PD}}{C}K_{VCDL}} \qquad (2.41).$$

Note that if the delay is zero in Eq. (2.40), the closed-loop transfer function will be an all-pass function with a flat magnitude for all frequencies. However, the characteristic of a closed-loop transfer with a one-cycle delay is no longer flat due to the different positions of the zero and the pole.

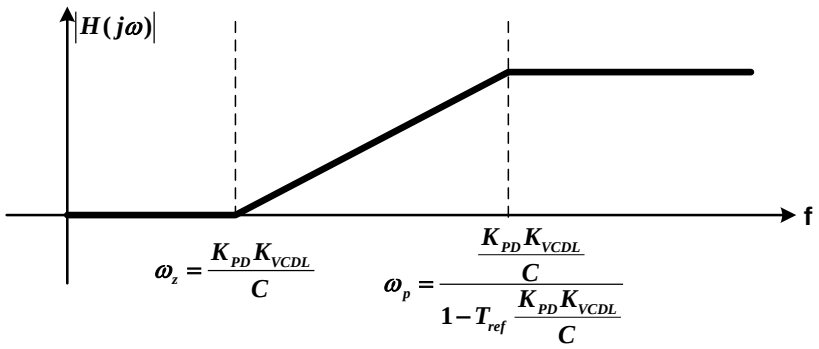


Fig. 2.37 The frequency response of closed-loop transfer function.

Generally, the frequency of ω_z is lower than that of ω_p because $T_{ref}*K_{PD}*K_{VCDL}$ is much less than '1'. As a result, the magnitude of the closed-loop transfer peaks, as shown in Fig. 2.37, while increasing the output jitter slightly. This jitter amplification can be reduced by various methods, such as a loop filtering technique or a phase filtering technique [2.39].

Chapter 3

The Proposed PLL-Based Receiver with Loop Linearization Technique

3.1 Introduction

A multichannel clock and data recovery (CDR) circuit that employs binary phase detectors (PDs) while also achieving linear loop dynamics is presented in this chapter. The proposed CDR recovers the linear information of the phase errors by exploiting its collaborative timing recovery architecture. Because the collaborative CDR combines PD outputs of multiple data streams, one can add a deliberate phase offset to each PD to realize a high-rate oversampling PD without additional PDs. The analysis shows that there exists an optimal spacing between these deliberate phase offsets that maximizes the linearity of the proposed PD for a given jitter condition. Under this condition, the loop dynamics of a second-order CDR model

which has different latencies between the proportional path and the integral path will be well matched with the simulation results. The linearized characteristics of the PD and the overall CDR designed for 45-nm CMOS technology are individually verified using an accurate time-step behavioral simulation.

3.2 Motivation

Many clock and data recovery circuits (CDRs) in high-speed serial data communication systems employ binary or bang-bang phase detectors (PDs) owing to their high-speed operation and low design complexity in spite of their nonlinear characteristics [3.1-3.3]. In comparison, linear phase detectors often require full-swing amplification of the incoming data stream and/or the propagation of short pulses, which adversely affect the performance-power trade-off [3.4]. The nonlinearity of binary PDs can cause critical problems for the overall CDR system; for instance, the jitter transfer characteristic can change depending on the amounts of jitter or noise present in the system. To address these problems, earlier CDR architectures aimed to make the CDR loop dynamics linear, including the over-sampling CDR [3.5] and the alternating edge-sampling PD [3.6]. A scrambling-technique-based time-to-digital converter (TDC) using a digitally controlled switched capacitor was also reported [3.7]. However, many of these approaches incur a high hardware cost, which makes them unsuitable for multichannel transceiver configurations. For instance, the over-sampling CDR requires additional samplers and retiming circuits, and both the alternating edge-sampling CDR and the scrambling-technique-based TDC have limited maximum oversampling ratios due to the growing complexity of the phase detection logic and the increasing number of delay elements.

In this paper, a simple linearization technique for binary PDs that exploits the collaborative timing recovery architecture of a multichannel CDR is proposed and validated with an accurate time-step behavioral simulation. The proposed technique adds different phase offsets to the PDs of the individual channels so that the whole set of PDs can effectively act as an oversampling PD. With the hardware cost equivalent to that of the conventional 2×-oversampling CDR, the proposed CDR can achieve PD gain variation of less than +/-5% when detecting phase differences from -0.2 to +0.2 UIs. In addition, it maintains constant linear jitter transfer characteristics for input jitter ranging from 0.03-UI_{rms} to 0.09-UI_{rms}.

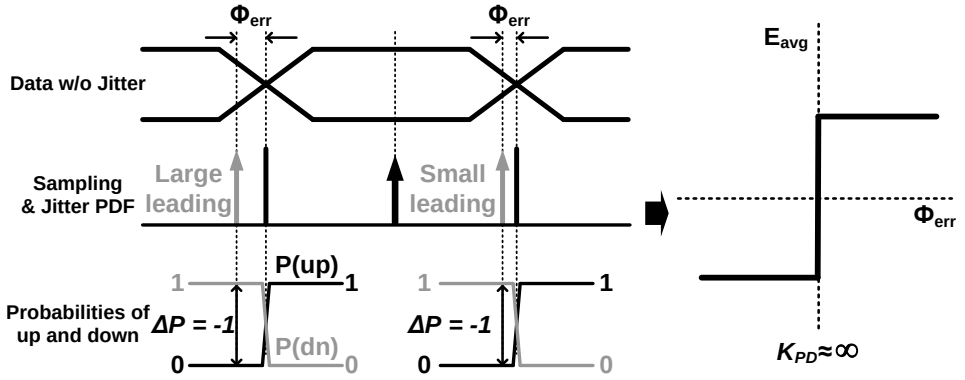
3.3 Overview of binary phase detection

A binary phase detector has been widely employed in high-speed serial links due to its many advantages, such as its simple hardware, inherent optimum sampling phase alignment, and adaptability to multiphase sampling structures compared to a linear phase detector [3.3]. However, the bang-bang characteristics of the binary phase detector exhibits highly nonlinear behavior, leading to design challenges and a serious trade-off between jitter generation and the tracking bandwidth.

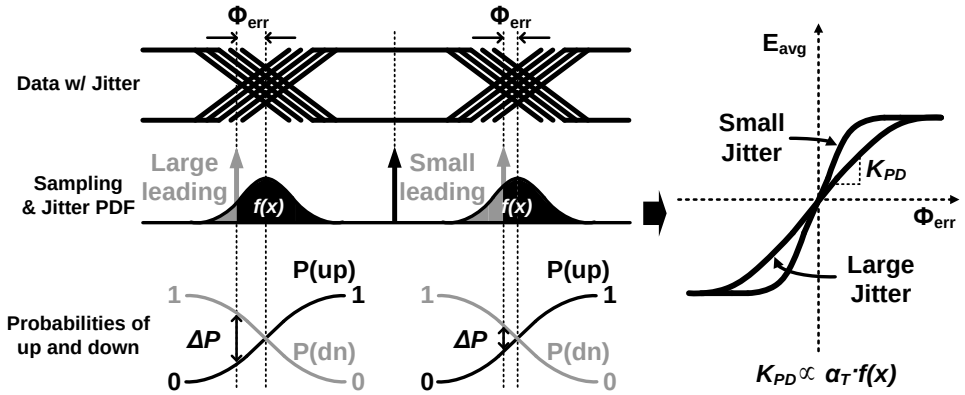
Before describing the proposed PD linearization technique, the basic principle of the binary PD transfer characteristic is reviewed. The average transfer characteristics of bang-bang PDs in the presence of jitter were analyzed in several earlier works [3.8, 3.9]. The analysis will be extended later to describe the linearized transfer characteristics of the proposed multichannel PD and to find its optimal configuration.

Fig. 3.1 shows the characteristics of a binary phase detector in the absence of jitter and in the presence of jitter. Unlike a linear PD, a binary PD detects only the polarity of the phase error regardless of whether the recovered clock phase is leading or lagging relative to the incoming data timing, as shown in Fig. 3.1(a). Regardless of the amount of phase error (Φ_{err}), the PD output is always up or down with a constant value. This nonlinearity implies that the PD gain K_{PD} is infinite right at the decision boundary and that it is zero elsewhere. As a result, a CDR with a binary PD cannot stay locked at one position; instead, it keeps dithering back and forth around

the locking point and the PD generates pseudo-randomly alternating up and down outputs.



(a)



(b)

Fig. 3.1 The characteristics of binary phase detector. (a) Nonlinearity in defect of jitter. (b) Linearization in presence of jitter.

However, various types of jitter are present either in the incoming data transitions or in the recovered clock such that the binary PD can statistically detect the magnitude information of the phase error. Intuitively speaking, the densities of up

and down outputs may gradually change from 50:50 as the phase error increases from zero. In other words, the PD gain is effectively smoothed and the PD has a finite range with a constant, linear slope. In most CDRs and PLLs whose PD sampling frequency is much higher than the loop bandwidth, the instantaneous noise (i.e., quantization noise) of the BB-PD outputs will be filtered out by the loop bandwidth, leaving only the smoothed and linearized transfer characteristics of the binary PD.

Fig. 3.1(b) illustrates the linearization of the binary PD transfer characteristics in the presence of jitter. Statistically, the average output of a binary PD is proportional to the difference ΔP between the up probability *P(up)* and the down probability *P(dn)*. Unlike the case shown in Fig. 3.1(a) with the constant ΔP, the jitter changes the value of ΔP proportional to the phase error Φ_{err}. In addition, the up and down probabilities can be calculated as the integration of the jitter probability density function (PDF) *f(x)*. When the phase error is denoted as Φ_{err}, the equation can be expressed as

$$\begin{aligned} E_{avg}(\phi_{err}) &= D_{BB}\alpha_T(P(up)-P(dn)) \\ &= D_{BB}\alpha_T\left(\int_{-\infty}^{\phi_{err}} f(x)dx - \int_{\phi_{err}}^{+\infty} f(x)dx\right) \end{aligned} \tag{3.1}$$

where D_{BB} is the quantized value of the binary PD output and α_T is the data transition density. This result shows that the net average PD output corresponds to the convolution between the jitter PDF and the ideal phase detection gain curve of the binary PD. This agrees with previously reported results [3.8]. Assuming an even-symmetric function for the PDF, the effective PD gain can be written as follows:

$$K_{PD}\Big|_{\phi=\phi_{err}} = \frac{\partial E_{avg}(\phi)}{\partial \phi}\Bigg|_{\phi=\phi_{err}} = 2D_{BB}\alpha_T f(\phi_{err}) \tag{3.2}$$

As a result, the effective PD gain increases for a high data transition density or a large amount of jitter, as shown on the right of Fig. 3.1(b). However, the amount of jitter is often not a parameter that a designer can predict or control. Also, the transition density of incoming data can change depending on the data encoding scheme of a transmitter or the data pattern itself. These lead to the variation of the CDR's loop bandwidth or stability depending on the jitter condition and the encoding method of the transmitted data.

3.4 The proposed BBPD linearization technique

This section introduces the proposed linearization technique for a binary PD and describes the four-channel receiver employing that technique. To explain the linearization process, a statistical analysis is used. The target of the linearization technique is a constant gain curve for the binary PD under various jitter conditions of incoming data streams while the hardware complexity and design overhead are equal to the conventional 2X-oversampling binary PD. To reduce the gain variation and to remove the quantization effect of the proposed PD, the optimized conditions are determined and simulated in this section.

3.4.1 Architecture of the proposed PLL-based receiver

The proposed receiver is based on the collaborative timing recovery circuit reported earlier in the paper [3.10]. Because a multichannel setup transmits more information pertaining to the TX clock, the channel loss, and the cross-talk, for instance, collaboration among the channels has numerous advantages in the design of a CDR, such as superior mid-band jitter tracking performance and low dependency on the transition density of the data. In addition to these advantages, collaboration during phase detection also improves the CDR performance, such as its loop linearization. The proposed receiver architecture is based on a PLL to generate global multi-phase clocks. It can be modeled as a second-order CDR.

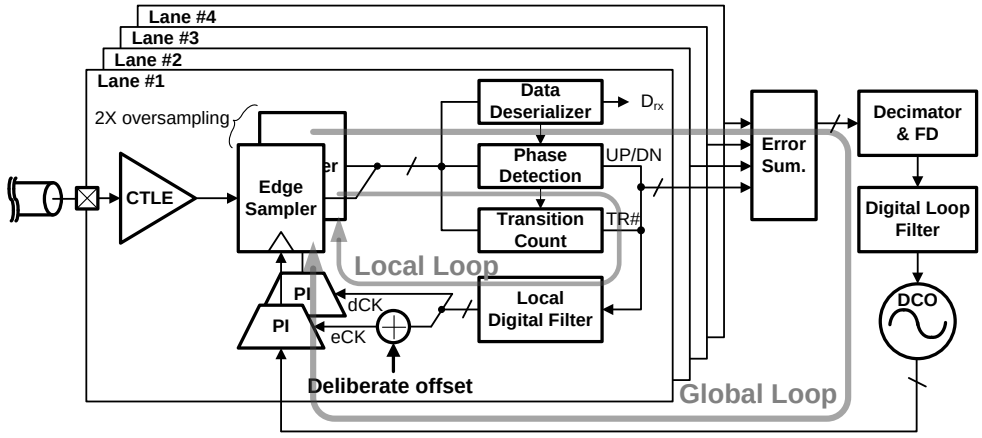


Fig. 3.2 Block diagram of a multi-channel receiver with a shared CDR employing the proposed PD linearization technique.

Fig. 3.2 shows an overall block diagram of a four-channel serial data receiver that incorporates a collaborative timing recovery CDR along with the proposed PD linearization technique. The receiver of each channel consists of a linear equalizer followed by a set of half-rate data and edge slicers for 2×-oversampling binary phase detection. The outputs of the individual phase detection logics are combined by the global digital filter, which controls the frequency and phase of a digitally controlled oscillator (DCO) to adjust the global clock timing. The global digital filter consists of an error summation block, a decimator, a frequency detector, and a digital loop filter that includes a delta-sigma modulator.

The collaborative timing recovery scheme extracts more information about the phase error and lowers the dependency on the data transition density fluctuation by aggregating the PD outputs of multiple channels. The assumption is that the data on the multiple channels are transmitted with a common timing while the data patterns and transition densities of the individual channels are sufficiently random and

independent of each other. Due to the aggregation, the change in the condition that affects all of the multichannel PDs (e.g., a shift in the common clock timing) is detected with a full PD gain, while a change that is local to just one of the PDs (e.g., fluctuation in the transition density in one of the data streams) is sensed with a 1/4-reduced gain. To suppress the dependency of the PD gain on the data transition density even further, the PD outputs are normalized to the total number of the data transitions detected before being aggregated. For example, a case with six up-signals out of four data transitions has the same consequences as the case with three up-signals out of two data transitions, as shown in Fig. 3.3. This decimation helps the CDR achieve relatively constant loop characteristics regardless of the data transition density.

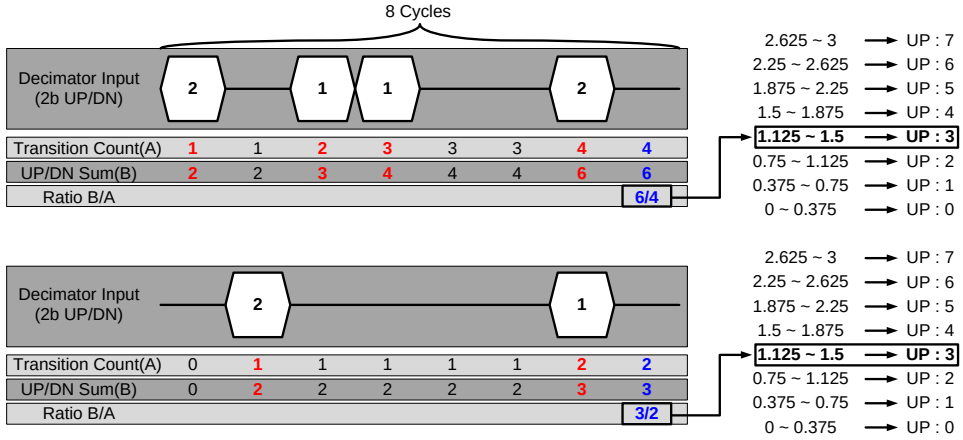


Fig. 3.3 Example of the decimator.

A local de-skewing circuit is added to each channel's clock path to compensate for any possible skew between the propagation delays of the channels. The local de-

skewing circuit consists of a local digital filter and phase interpolators. To prevent interaction between the global loop and the local loop, the bandwidth of the local loop filter is set at about 1000 times lower than that of the global loop. A set of four local digital filters adjusts the local clock skew by accumulating the corresponding PD outputs over time and using the result to control the phase interpolator settings. The implemented phase interpolator can adjust the timing of the globally distributed clock in steps of 1/30 UI. The shared DCO generates ten uniformly spaced clock phases and the phase interpolator stage synthesizes a new phase that is between two adjacent coarse phases.

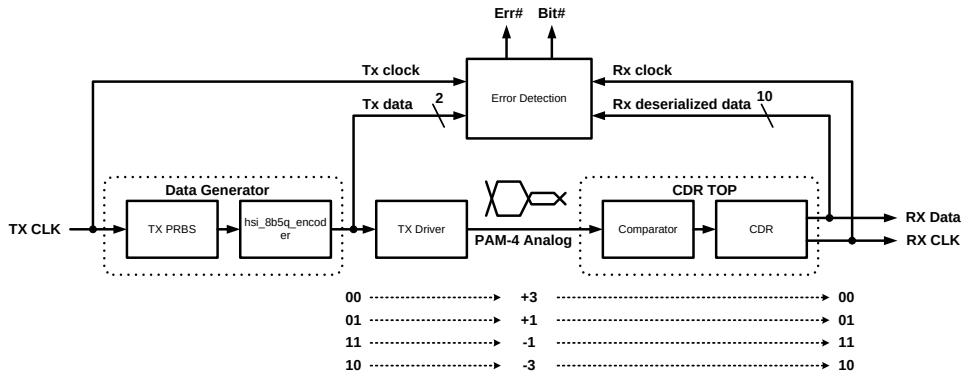


Fig. 3.4 Testbench for verifying each circuit block.

The deliberate phase offset applied to the PD of each channel is controlled by a digital offset added to the phase interpolation settings. Note that these deliberate offsets for PD linearization are added only to the edge-sampling clocks, meaning that they do not increase jitter in the data sampling clocks. The deliberate phase offsets are generated by a finite-state machine (FSM) that circulates through a

certain pattern to ensure zero bias in the effective PD transfer and uniform coverage of the sampling positions. A more specific linearization technique using deliberate offsets will be explained in the next sub-section.

For the test of proposed receiver, a transmitter model that changes its signal level between 4-PAM and 2-PAM is used, as shown in Fig. 3.4. In the case of 4-PAM, the transmitted data are encoded with the 8B5Q scheme and the transmitted data are encoded by a Gray scheme. After the receiver recovers data and clock from the incoming data, the de-serialized recovered data are compared with the transmitted data at the error detector to count the BER.

3.4.2 Linearization technique of binary phase detection

This section proposed the linearization technique of binary phase detection and describes its linearization process. The whole process can be divided into four parts, and each section is explained by a statistical analysis.

Fig. 3.5 shows the entire process of the proposed binary-PD linearization technique. The key idea of the proposed technique is that it intentionally adds a time-varying phase offset to each edge slicer. The edge slicer with a phase offset detects the polarity of the phase error compared with the given offset rather than with an ideal zero, as shown in Fig. 3.5(a). A different offset is applied to each edge slicer using phase interpolators, and the offset's position is rotated among the four channels using the FSM, as shown in Fig. 3.5(b). The phase offsets are rotated among the channels to remove the static phase offsets of each sampling clock caused by the process of local de-skewing.

If the jitter PDF of each data is $f_N(x)$, as shown at the bottom of Fig. 3.5(a), the four PDs sampling this distribution with four different phase offsets can be considered as equivalent to a single PD sampling the four overlapped jitter PDFs, each with the corresponding offset, as shown at the bottom of Fig. 3.5(b). Given that the contributions made by the individual jitter PDFs are linearly summed, the effective jitter PDF detected by the multichannel PDs would be that shown in Fig. 3.5(c). Again, it should be noted that the data slicers are still triggered by the clock without the phase offsets, implying that they do not detect this increased jitter distribution and that the timing margin of the receiver remains maximized.

Introducing these deliberate offsets to the edge sampling phases in the collaborative CDR enables the PDs statistically to over-sample the phase error and recover its linear magnitude information. However, the phase offsets which are positioned at discrete levels can cause quantization effects in the PD gain curve, similar to the case of an oversampling PD or a time-to-digital converter. Although the underlying jitter and noise in the system will smoothen the PD transfer characteristic, there may still exists gain variation due to the quantization steps. These quantization steps can be explained by the variation of the effective jitter PDF within the range of linearization, as shown at the bottom of Fig. 3.5(c). With a finite number of phase offset levels available, there exists an optimal spacing between the phase offset levels that maximize the PD's linearity for a given jitter condition, as shown in Fig. 3.5(d).

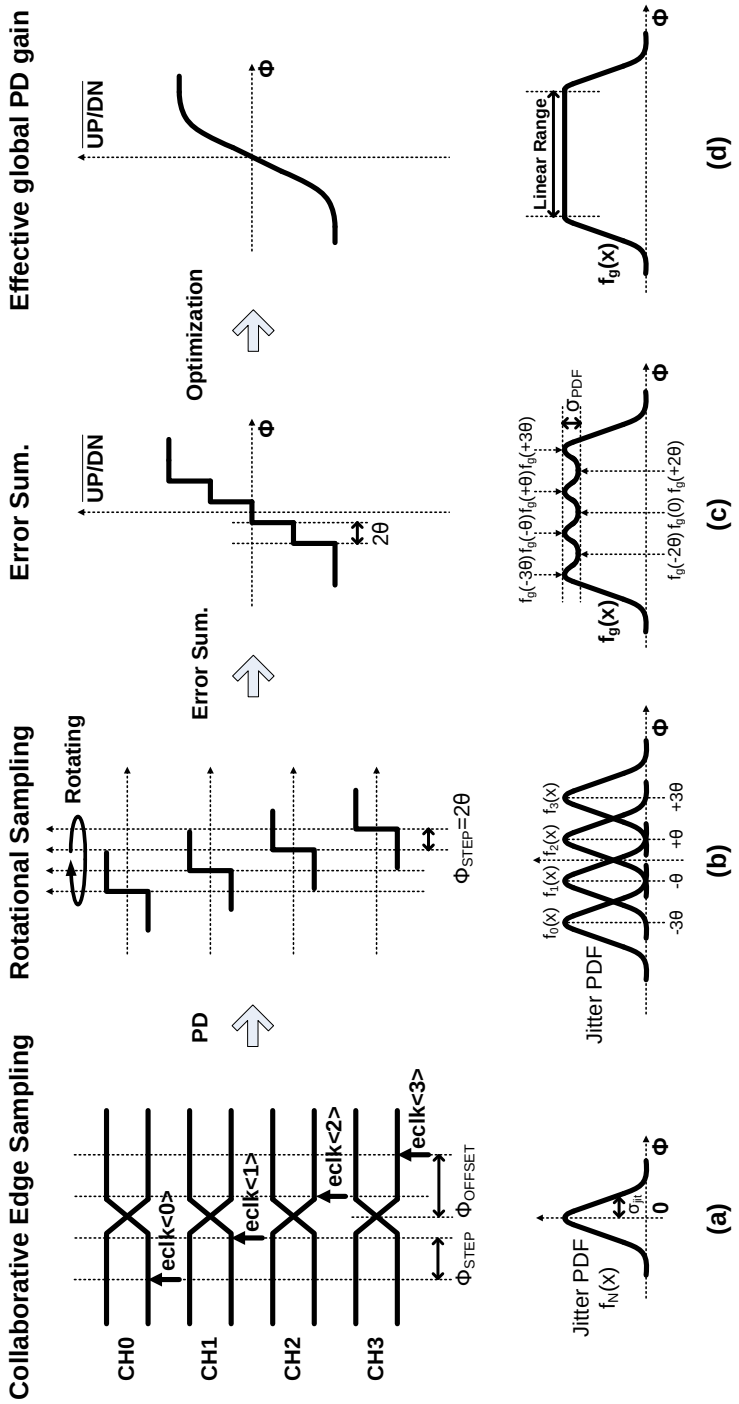
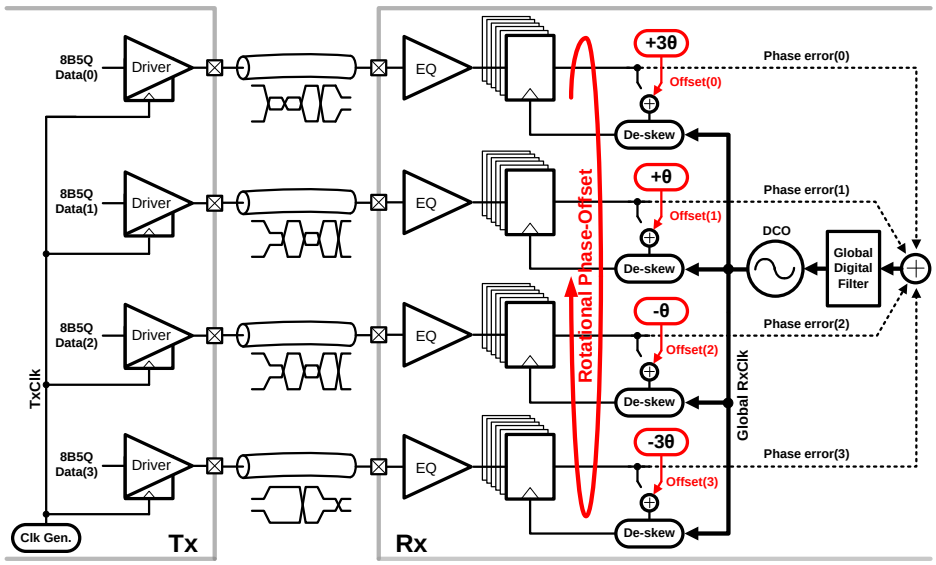


Fig. 3.5 Proposed linear phase detection process and its jitter PDF. (a) Collaborative edge sampling. (b) Rotational edge sampling. (c) Error summation. (d) Optimization of PD gain linearity.

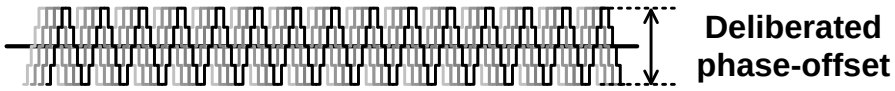
For a specific ratio between the phase offset and the sigma of jitter, the PD characteristics of the linearization of the PD gain are largely insensitive to the jitter condition, unlike with conventional binary PDs. The optimal conditions will be derived and discussed in Section 3.5.

3.4.3 Rotational pattern of sampling phase offset

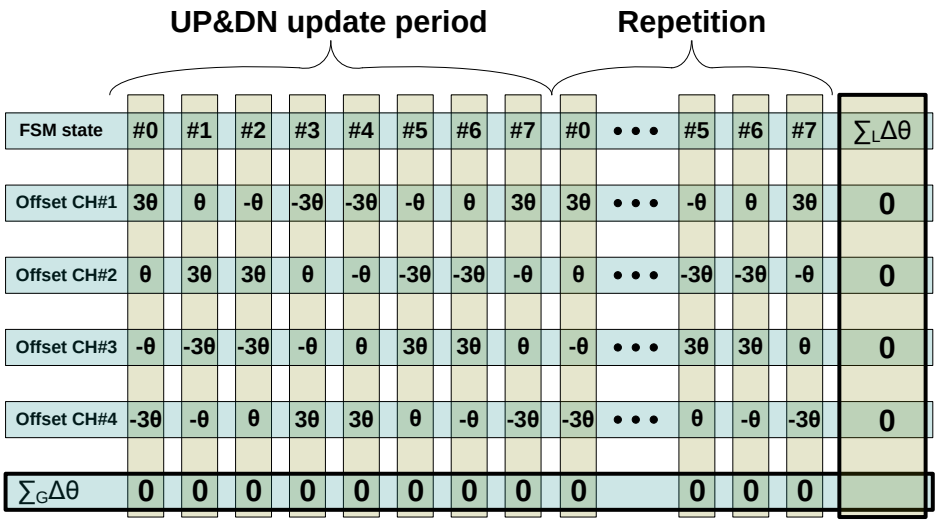
Fig. 3.6(a) shows the rotational sampling example in the receiver block with the deliberate phase offset of each edge-sampling clock. The deliberate phase offsets for a given PD makes it possible linearly to detect the phase error of the global clock, and their rotation also makes it possible to recover the linear information of the skew while requiring only one pair of sampling clocks, one at the edge and the other at the center of the incoming data (i.e., 2x oversampling). This is the edge-sampling clock whose phase is periodically changed by some offsets in accordance with a pre-programmed pattern. The frequency of this periodic pattern is set such that phase disturbances do not affect the average behavior of the CDR and cause periodic jitter or spurious tones in the local clocks.



(a)



(b)



(c)

Fig. 3.6 The rotating pattern of the deliberate phase offsets applied to the individual channels and their corresponding FSM states. (a) The block diagram of the transceiver sampling with the rotational deliberate phase-offset. (b) The phase of the edge-sampling clock with the deliberate phase-offset. (C) The pattern of rotational sampling phase-offset.

To avoid artificial bias due to the deliberate phase offsets, the sum of the offsets applied to one PD over one update period is always equal to zero. Also, for uniform coverage of the phase offsets, the sum of the phase offsets applied to the four PDs is always equal to zero at any given time. Fig. 3.6(b) plots the pattern of the deliberate phase offset of each edge-sampling clock over time while Fig. 3.6(C) shows the rotating pattern of the phase offsets across the four channels and their sums per channel and across the channels. The update period of the digital loop filter is eight DCO clock cycles; hence, the pattern is repeated every eight cycles. During this period, the global summation $\Sigma_G\Delta\theta$ and local summation $\Sigma_L\Delta\theta$ of the phase offsets are always zero. Most of the momentary shifts in the edge-sampling clock phase will be filtered by the low bandwidth of the CDR and will not adversely affect the jitter level of the recovered, data-sampling clock. In the meantime, both the global CDR and local de-skewing circuit can extract the linear phase-error information without any additional hardware other than the 2x-oversampling binary PD.

3.5 PD gain analysis and optimization

To realize linear system dynamics for the CDR, its PD should have a constant phase detection gain across a wide range of phase error. The phase detection gain corresponds to the slope in the average PD transfer characteristic curve, i.e., the curve of the average PD output $E_{avg}(\Phi)$ versus the phase error Φ. Therefore, the effective transfer curve of the proposed linearization PD will be analyzed and a condition for its constant slope will be defined in this section.

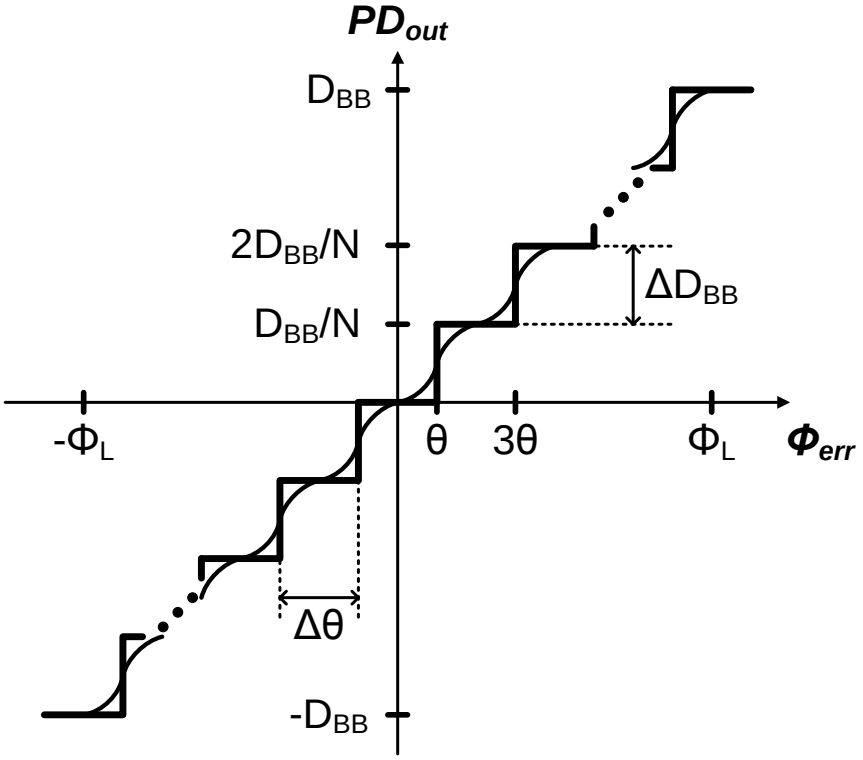


Fig. 3.7 Effective PD gain curve of the proposed 2N-channel receiver.

The linearization technique described in Section III effectively realizes a set of PDs that compare the phase error with multiple phase offsets. Fig. 3.7 shows the effective PD gain curve computed by the convolution between the jitter PDF and the binary PD transfer curve. The number of channels is *2N*, the maximum total PD output is assumed to be +/- D_{BB}, and the spacing between the adjacent phase offset levels is 2θ *or* Φ_L/N. The effective PD transfer characteristic can be derived by summing those with their own jitter PDFs, assuming that all jitter PDFs of all channels have the same standard deviation of the σ_{jit} distribution but different offsets:

$$\begin{aligned} K_{EPD}\big|_{\phi=\phi_{err}} &= \Delta D_{BB}\alpha_T \sum_{n=0}^{N-1}\left\{ f\left(\phi_{err}+(2n+1)\cdot\theta\right)+ f\left(\phi_{err}-(2n+1)\cdot\theta\right)\right\} \\ &= \Delta D_{BB}\alpha_T\, f_g(\phi_{err}) \end{aligned} \tag{3.3}$$

Here, $f_g(\Phi_{err})$ denotes the combined effective jitter PDF of the *2N* channels, as illustrated in the Fig. 3.5(c). Note that the expression is identical to that for the 2N-times over-sampling PD [3.5]. Assuming a sufficiently large N, the effective PD gain is

$$\begin{aligned} &\lim_{N\to\infty} K_{EPD}\big|_{\phi=\phi_{err}} \\ &\quad= \lim_{N\to\infty} \Delta D_{BB}\alpha_T \sum_{n=0}^{N-1}\left\{ f(\phi_{err}+(2n+1)\theta)+ f(\phi_{err}-(2n+1)\theta)\right\} \end{aligned} \tag{3.4}$$

such that

$$\begin{aligned}\lim_{N\to\infty} K_{EPD}\Big|_{\phi=\phi_{err}} &= \lim_{N\to\infty} \alpha_T \frac{\Delta D_{BB}}{\Delta\theta} \sum_{n=0}^{N-1} \left\{ f(\phi_{err} + (2n+1)\theta)\cdot\Delta\theta + f(\phi_{err} - (2n+1)\theta)\cdot\Delta\theta \right\} \\ &= \alpha_T \frac{\Delta D_{BB}}{\Delta\theta} \left\{ \int_0^{(2N-1)\theta} f(x)dx + \int_{-(2N-1)\theta}^{0} f(x)dx \right\}\end{aligned} \quad (3.5)$$

If the normalized jitter PDF *f(x)* is practically zero outside the linear range of ($\Phi_{err} < -\Phi_L$ or $\Phi_{err} > \Phi_L$), the integral parts of Eq. (3.5) can be assumed to be one. In addition, as shown in Fig. 3.7, the output of a single binary PD ΔD_{BB} and the phase spacing $\Delta\theta$ between the adjacent offsets are D_{BB}/N and Φ_L/N, respectively. The effective PD gain can be written as follows:

$$\lim_{N\to\infty} K_{EPD}\Big|_{\phi=\phi_{err}} \approx \alpha_T \frac{D_{BB}}{\phi_L} \quad (3.6)$$

Thus, Eq. (3.6) demonstrates that the effective gain of a binary PD using the proposed technique converges to a constant value as the number of channels increases. The converged value is determined only by the maximum output of the PD (D_{BB}) and the whole linear range (Φ_L), and it is independent of the jitter PDF.

However, when the number of channels ($2N$) is finite, a CDR employing the proposed binary PD linearization technique may have a non-uniform PD gain. For instance, if the ratio between the phase offset spacing θ and the jitter standard deviation σ_{jit} is too large, Eq. (3.3) predicts that the PD gain can fluctuate within the linear range. On the other hand, if the ratio is too small, the PD gain will be constant but the linear range becomes narrow.

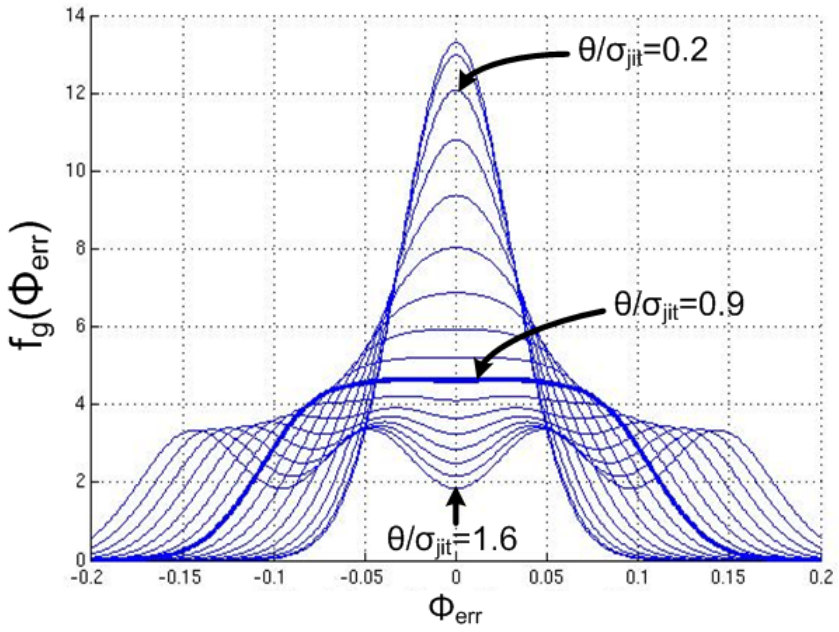


Fig. 3.8 Shape of the combined effective jitter PDF with the various ratio between θ and σ_{jit}.

Therefore, there is an optimal ratio between the θ and σ_{jit} that makes the PD gain uniform across the widest range instead of increasing the number of channels. Because the uniformity of the PD gain is dependent on the shape of the effective jitter PDF $f_g(\Phi_{err})$, as expressed by Eq. (3.3), the change of $f_g(\Phi_{err})$ within the linear range by various ratios between σ_{jit} and θ should be noted. Assuming a Gaussian distribution for each $f(x)$, $f_g(\Phi_{err})$ is also a function of σ_{jit} and θ; it can then be plotted by various ratios between σ_{jit} and θ, as illustrated in Fig. 3.8. The assumption of $f(x)$ as a Gaussian distribution is reasonable because the jitter histogram of well-equalized data commonly has a form similar to a Gaussian distribution, especially when using a continuous-time linear equalizer. At the much lower ratio of σ_{jit}/θ, the

effective jitter PDF $f_g(\Phi_{err})$ has multiple lofty peaks and valleys within the linear range between $\pm 2N \cdot \theta$, resulting in fluctuation of the PD gain. As the ratio increases to the optimized value, the fluctuation is reduced and $f_g(\Phi_{err})$ within the linear range becomes constant.

The optimized ratio σ_{jit}/θ can easily be obtained by the calculation of the maximum difference of the peaks and valleys. If the number of channels is even, the peaks and valleys of $f_g(\Phi_{err})$ within the linear range are located at phases of $k\theta$ and $k\theta/2$ for any integer k. For example, because the effective jitter PDF $f_g(\Phi_{err})$ of a four-channel CDR is the summation of four Gaussian functions that are shifted along the x-axis, we can create the following expression:

$$\begin{aligned} f_g(\phi_{err}) &= f(\phi_{err}+3\theta)+f(\phi_{err}+\theta)+f(\phi_{err}-\theta)+f(\phi_{err}-3\theta) \\ &= \frac{1}{\sigma_{jit}\sqrt{2\pi}}\left(e^{-\frac{(\phi_{err}+3\theta)^2}{2\sigma_{jit}^2}} + e^{-\frac{(\phi_{err}+\theta)^2}{2\sigma_{jit}^2}} + e^{-\frac{(\phi_{err}-\theta)^2}{2\sigma_{jit}^2}} + e^{-\frac{(\phi_{err}-3\theta)^2}{2\sigma_{jit}^2}} \right) \end{aligned} \tag{3.7}$$

In the range of -3θ to 3θ, the local maximum and minimum are respectively $f_g(\theta)$ and $f_g(2\theta)$. To define the optimal condition that makes the PD gain nearly constant, we consider the difference between the maximum and minimum via the following equation:

$$\begin{aligned} \Delta f_g &= f_g(\theta) - f_g(2\theta) \\ &= f(4\theta)+f(2\theta)+f(0)+f(-2\theta) \\ &\quad - f(5\theta)-f(3\theta)-f(\theta)-f(-\theta) \\ &= \frac{1}{\sigma_{jit}\sqrt{2\pi}}\left(-e^{-\frac{25\theta^2}{2\sigma_{jit}^2}} + e^{-\frac{16\theta^2}{2\sigma_{jit}^2}} - e^{-\frac{9\theta^2}{2\sigma_{jit}^2}} + 2e^{-\frac{4\theta^2}{2\sigma_{jit}^2}} - e^{-\frac{\theta^2}{2\sigma_{jit}^2}} + 1 \right) \end{aligned} \tag{3.8}$$

We note that Δf_g is determined by the ratio of θ and σ_{jit} for a specific jitter condition. Fig. 3.9 shows the calculated value of Δf_g, which is also normalized by the average value of f_g within the linear range for the four-channel CDR with various ratios of

deliberate phase offset and jitter. The value of Δf_g remains small for $\theta/\sigma_{jit} < 1.16$ and increases rapidly after that point. In other words, if the ratio θ/σ_{jit} is in the range below the dotted line (θ/σ_{jit}=1.16), the gain variation of the proposed PD will be reduced to less than 5%. The exact optimal ratio to minimize Δf_g while achieving the widest linear range is such that θ/σ_{jit}=0.9, which is obtained by solving a differentiated equation. Regardless of the absolute values of the jitter and phase offset, the optimal ratio is always close to 0.9 while the percentage of the gain variation is 1.04%. At a ratio of 0.9, the effective jitter PDF has a flat proof, as shown in Fig. 3.8.

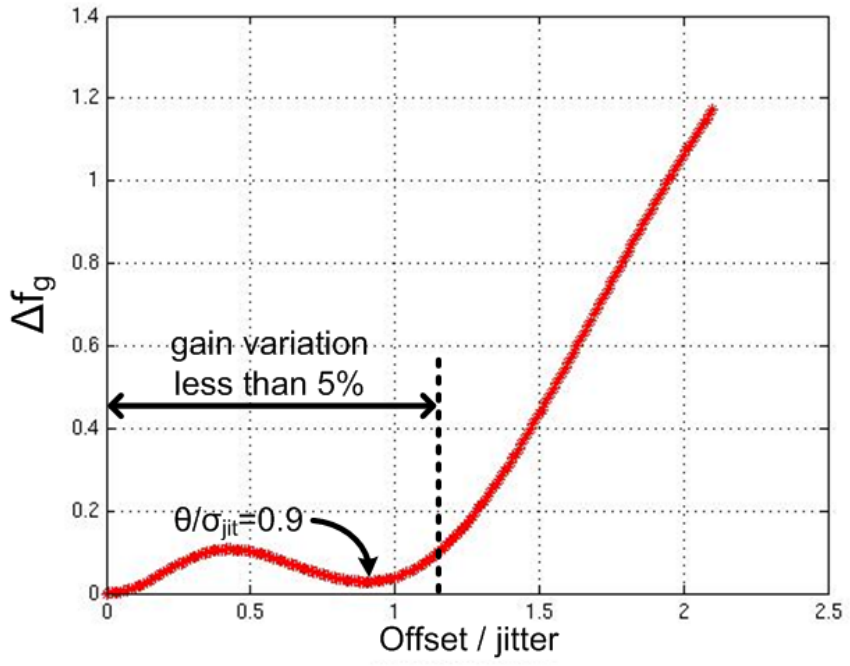


Fig. 3.9 Variance of the combined effective jitter PDF with the various ratio between θ and σ_{jit}.

Although the PD gain is relatively constant regardless of the input noise

conditions, the specific values of the result can change slightly depending on the number of channels, the form of the jitter PDF, or the noise of the devices. In addition, the result of the calculation shown in Fig. 8 and Fig. 9 exclude how the loop dynamic influences the binary PD gain. According to a previous report [3.9], the loop dynamics of the CDR decreases the gain of the binary PD as follows:

$$K_{BBPD}(\sigma_{jit}, \beta K_T) = D_{BB}\alpha_T f(0) \cdot \left[1 + e^{-A\left(\frac{\beta K_T}{\sigma_{jit}}\right)^2} \right] \tag{3.9}$$

Here, N is the feedback divider factor, β is the proportional path gain, and K_T is the period gain constant of the DCO. The result of Eq. (3.9) is always lower than the result of Eq. (3.2), as in a case with more jitter. Therefore, the optimized ratio will slightly shift to a lower value. However, the effect is not dominant due to the relatively small value of βK_T, and the optimized ratio σ_{jit}/θ is always close to a ratio 0.9. In the result of the optimized ratio, the gain of the binary PD using the proposed 2N-times linearization technique, as expressed by Eq. (3.3) can be approximated in the form of the following linear equation:

$$K_{PD} \approx \alpha_T \frac{D_{BB}}{2N\theta} \tag{3.10}$$

As discussed above, the gain within the phase range between $\pm 2N \cdot \theta$ is only in inverse proportion to the phase offset spacing θ regardless of the jitter PDF σ_{jit}.

3.6 Loop Dynamics of the 2nd-order CDR

The nonlinear dynamics of a bang-bang CDR or PLL can be analyzed by a nonlinear map plotting of the trajectory on a bi-dimensional phase plane [3.11]. Although this analysis is accurate and powerful, its procedure is very complicated. On the other hand, the linear model makes it possible to analyze the loop dynamics more simply and intuitionally. To verify the validity of Eq. (3.10), the jitter transfer characteristic of a CDR employing the proposed linearization technique is analyzed and simulated with the z-domain and s-domain models in this section. Also, the latency effect of the loop dynamics for accurate CDR modeling is analyzed.

Latencies that are unintentionally added to the paths of the CDR loop cause critical problems, such as dithering for binary CDRs and a reduction of the phase margin for linear CDRs. Many studies have reported the effect of latency with discrete or continuous models for all-digital PLLs and all-digital CDRs. However, the model for the latency is commonly added to all paths [3.12] or is only added to the integral path while ignoring the latency for the proportional path [3.13]. In the collaborative timing recovery architecture, the latency of the proportional path can no longer be ignored owing to its increased number of blocks. Unlike other CDRs, the collaborative timing recovery requires a summation block and a decimation block to process the errors generated from all of the channels before the loop filter. Hence, both the proportional path and the integral path must have more latency than one reference clock cycle. In addition, the integral path commonly has more blocks

than the proportional path, such as a delta-sigma modulator and an encoder for DCO frequency control. Consequently, the amount of latency should be applied separately to the proportional path and the integral path of the CDR model. Commonly, the integral path has more latency than the proportional path by a few clock cycles.

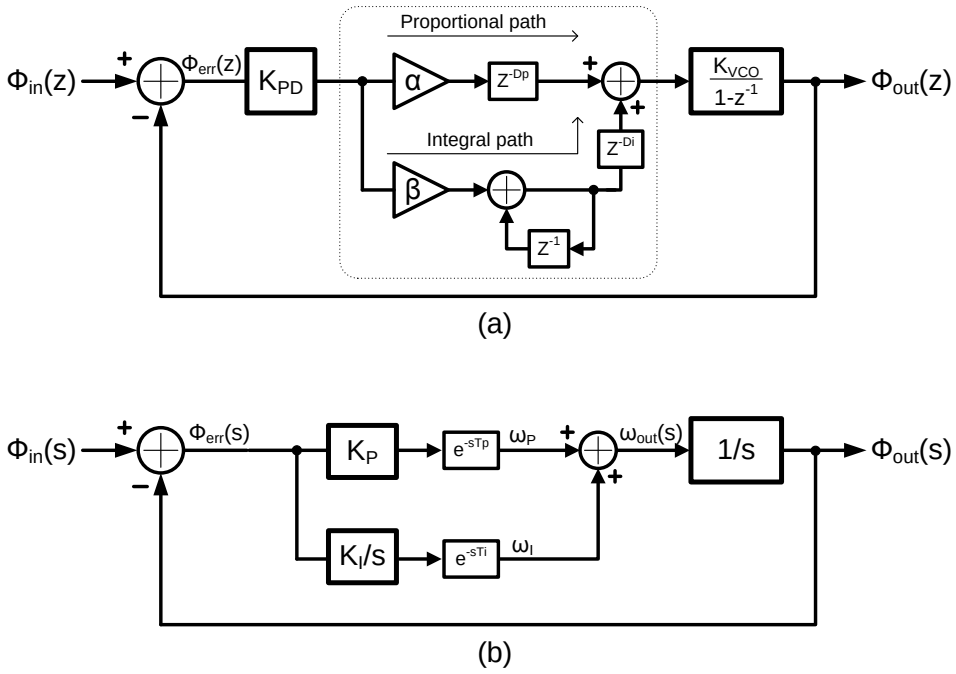


Fig. 3.10 Block diagram of the CDR models for (a) z-domain and (b) s-domain.

Fig. 3.10 shows z-domain and s-domain models of a second-order CDR. Both figures show a different latency model between the integral path and the proportional path. In the z-domain model shown in Fig. 3.10(a), K_{PD} is the transfer characteristic of the linearized binary PD (equal to Eq. (3.10)); thus, the open-loop transfer function is

$$G(z)=\frac{K_{PD}K_{DCO}(\alpha z^{-D_P+1}(z-1)+\beta z^{-D_I+2})}{(z-1)^2} \tag{3.11}$$

where D_P and D_I are the latencies of the proportional and integral paths and α and β are their gains, respectively. The closed-loop transfer function from Φ_{in} to Φ_{out} is

$$\begin{aligned} H(z) &= \frac{G(z)}{1+G(z)} \\ &= \frac{K_{PD}K_{DCO}\alpha z^{-D_P+1}(z-1)+K_{PD}K_{DCO}\beta z^{-D_I+2}}{(z-1)^2+K_{PD}K_{DCO}\alpha z^{-D_P+1}(z-1)+K_{PD}K_{DCO}\beta z^{-D_I+2}} \end{aligned} \tag{3.12}$$

With $z^{-1}= exp(-j\omega T)$ and with the loop-filter update period T, it is clear that the closed-loop transfer function has a low-pass characteristic. Nonetheless, an intuitive analysis is not feasible because the transfer function is not a second-order system due to the latency components. Sometimes, a z-domain analysis is simpler than a time-domain analysis due to the fact that the z-domain model can be easily obtained. However, well-known z-domain analysis methods such as the unit circle criterion are not convenient and do not support quantitative parameters that are familiar to designers, such as the phase margin, damping factor, and bandwidth.

To analyze the loop more conveniently and intuitively, the s-domain model of Fig. 3.10(b) was used. In common with the z-domain model, the different latencies are added to each path as the parameters $exp(-sT_P)$ and $exp(-sT_I)$. The parameters K_P and K_I can be calculated by the discrete forms of the PD gain, loop filter gain, and DCO gain [3.14]. Then, K_I can be expressed by the update frequency per cycle of the loop filter $\Delta\omega$ and phase error Φ_{err}, as follows:

$$K_I = \frac{\Delta\omega}{\phi_{err}} \cdot \frac{\omega_{ref}}{2\pi} \tag{3.13}$$

Here, $\omega_{ref}/2\pi$ is the update frequency of the loop filter. Under the same conditions, K_P can also be calculated by the amount of the update phase $\Delta\Phi$, as follows:

$$K_P = \frac{\Delta\phi}{\phi_{err}} \cdot \frac{\omega_{ref}}{2\pi} \tag{3.14}$$

Assuming that the update frequency and phase per single cycle of the loop filter are adjusted by a 1-bit control signal, the phase error Φ_{err} used in both Eq. (3.13) and Eq. (3.14) is equal to the inverse of Eq. (3.10). The open-loop transfer function from Φ_{err} to Φ_{out} is

$$G(s) = \frac{K_P e^{-sT_P} s + K_I e^{-sT_I}}{s^2} \tag{3.15}$$

In common with the z-domain model, this result also cannot be analyzed easily as a result of two terms of latency. Assuming a small value of sT where the frequency of interest is much lower than the Nyquist frequency (i.e., one half of the update frequency), we can simplify the function substituting the approximation expression of $1-sT$ for $exp(-sT)$ [3.15]. Then, Eq. (3.15) can be written as follows:

$$G(s) = \frac{-K_P T_P s^2 + (K_P - K_I T_I)s + K_I}{s^2} \tag{3.16}$$

Its closed-loop transfer function $H(s)=\Phi_{out}(s)/\Phi_{in}(s)$ then becomes

$$H(s)=\frac{\frac{-K_P T_P}{1-K_P T_P}s^2+\frac{K_P-K_I T_I}{1-K_P T_P}s+\frac{K_I}{1-K_P T_P}}{s^2+\left(\frac{K_P-K_I T_I}{1-K_P T_P}\right)s+\frac{K_I}{1-K_P T_P}} \tag{3.17}$$

The closed-loop transfer function *H(s)* can be compared to the classical two-pole system transfer function,

$$H(s)=\frac{2\zeta\omega_n s+{\omega_n}^2}{s^2+s\zeta\omega_n s+{\omega_n}^2} \tag{3.18}$$

where ω_n is the natural frequency and ζ is the damping factor. If we define $\omega_{n,0}$ and ζ_0 as the natural frequency and damping factor with zero latencies (i.e., $T_P=0$ and $T_I=0$), by a comparison between Eqs. (3.17) and (3.18), each parameter can be written as shown below.

$$\omega_{n,0}=\sqrt{K_I} \tag{3.19}$$

$$\zeta_0=\frac{K_P}{2\sqrt{K_I}} \tag{3.20}$$

To determine the effect of latency in the open-loop transfer function, Eq. (3.20) can be used. First, if we design the parameter ζ_0 with a value of '1,' we can define the relationship between K_P and K_I as follows:

$${K_P}^2=4K_I \tag{3.21}$$

Going back to Eq. (3.16), the location of zeroes can be calculated by the quadratic formula of the numerator, as follows:

$$\omega_z = \frac{\pm(K_P - K_I T_I) + \sqrt{(K_P - K_I T_I)^2 + 4K_P K_I T_P}}{2K_P T_P} \tag{3.22}$$

Assuming $K_P T_P \ll 1$ and $K_P T_I \ll 1$, the value of K_P-$K_I T_I$ is positive and its approximate expression is K_P. This assumption is generally reasonable, because the order of K_P is commonly much lower than the orders of $1/T_P$ and $1/T_I$ when the latencies are a few cycles of the update clock. After substituting Eq. (3.21), the high-frequency zero $\omega_{z,h}$ and the low-frequency zero $\omega_{z,l}$ are

$$\omega_{z,h} \approx \frac{1}{2T_P} + \sqrt{\left(\frac{1}{2T_P}\right)^2 + \frac{K_P}{4T_P}} \tag{3.23}$$

$$\omega_{z,l} \approx -\frac{1}{2T_P} + \sqrt{\left(\frac{1}{2T_P}\right)^2 + \frac{K_P}{4T_P}} \tag{3.24}$$

With these zeros, Eq. (3.16) can be written as shown below.

$$G(s) = \frac{-(s + \omega_{z,l})(s - \omega_{z,h})}{s^2} \tag{3.25}$$

The value of $\omega_{z,h}$ can be considered to be inversely proportional to the quite small value of the proportional-path latency T_P, and the phase of the open-loop transfer function around the zero starts to decrease. Because the amount of frequency change in response to T_P is much larger than the low-frequency zero $\omega_{z,l}$, the two zeros will move closer together as T_P increases. Fig. 8 shows the amplitude and frequency response of the open-loop transfer function (3.16) under various conditions of T_P. The increase in T_P moves $\omega_{z,h}$ toward $\omega_{z,l}$, which is located at a relatively constant frequency, and the reduced distance between the zeros decreases the phase margin.

As a result, the dominant source of the decreased phase margin is the latency of the proportional path, not the integral path.

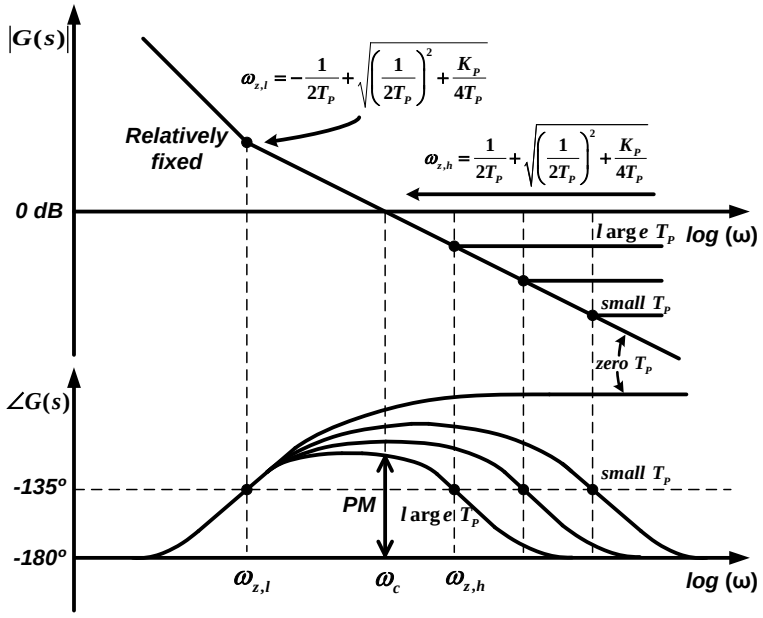


Fig. 3.11 Amplitude and phase response of the open-loop transfer function under the various conditions of T_P.

In addition to the phase margin, the natural frequency and damping factor are also affected by the latencies T_P and T_I. This relationship can be found by a comparison between Eq. (3.17) and Eq. (3.18) with non-zero latencies. Note that the second-order term of the numerator can be ignored when $K_P T_P \ll 1$. Thus, we can express ω_n and ζ in terms of K_P, K_I, T_P, T_I, $\omega_{n,0}$, and ζ_0, as follows:

$$\omega_n = \sqrt{\frac{K_I}{1 - K_P T_P}} = \frac{\omega_{n,0}}{\sqrt{1 - K_P T_P}} \tag{3.26}$$

$$\zeta = \frac{K_P}{2\sqrt{K_I}} \cdot \frac{\left(1 - \frac{K_I}{K_P} \cdot T_I\right)}{\sqrt{1 - K_P T_P}} = \zeta_0 \cdot \frac{\left(1 - \frac{K_I}{K_P} \cdot T_I\right)}{\sqrt{1 - K_P T_P}} \tag{3.27}$$

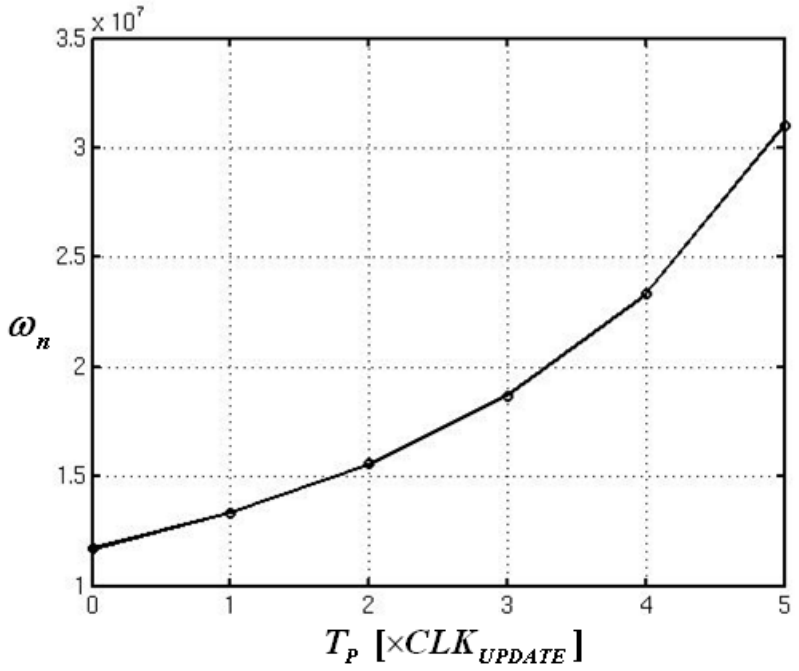


Fig. 3.12 The natural frequency of the 2nd-order CDR with the various latency conditions.

Fig. 3.12 and Fig. 3.13 plot the damping factor and the natural frequency of the proposed second-order CDR in response to various latency conditions. As shown in Fig. 3.12, the change of the natural frequency ω_n only depends on T_P, and ω_n increases from $\omega_{n,0}$ by the ratio of $1/\sqrt{1-K_P T_P}$ as T_P increases. The damping factor ζ is changed by both T_P and T_I. Given that T_I is always larger than T_P, it can be expressed

as $T_P+\alpha$. The damping ratio decreases in response to α, and the increased T_P accelerates the decrease of the damping ratio, as shown in Fig. 3.13.

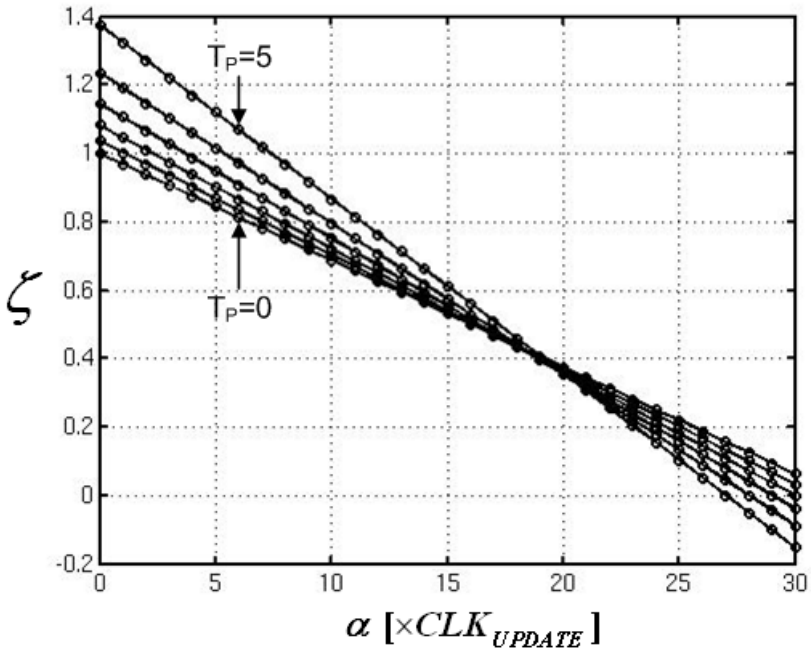


Fig. 3.13 The damping factor of the 2nd-order CDR with the various latency conditions.

Consequently, the latency of the proportional path cannot be ignored when designing a CDR with collaborative timing recovery, and it is a dominant source of changes in design parameters such as the phase margin, damping factor, and natural frequency from the first design. To keep the original design parameters, the latency of the proportional path should be considered and minimized first. In the proposed CDR, numerous functional blocks on the proportional path were merged into a single block in order to reduce the latency. Then, all functions in the block begin and

are completed within one clock cycle, reducing the number of registers. For example, the gain control block of the proportional path was combined with the decimator, and the multiplication blocks for dividing the aggregated up/down signal by the data transition count in the digital decimator were also merged with the error summation block. Moreover, the encoded up/down signals and transition counts to signed bits for reducing the number of transmitted bits from the each lane to the global error summation block were decoded to unsigned bits in the digital loop filter.

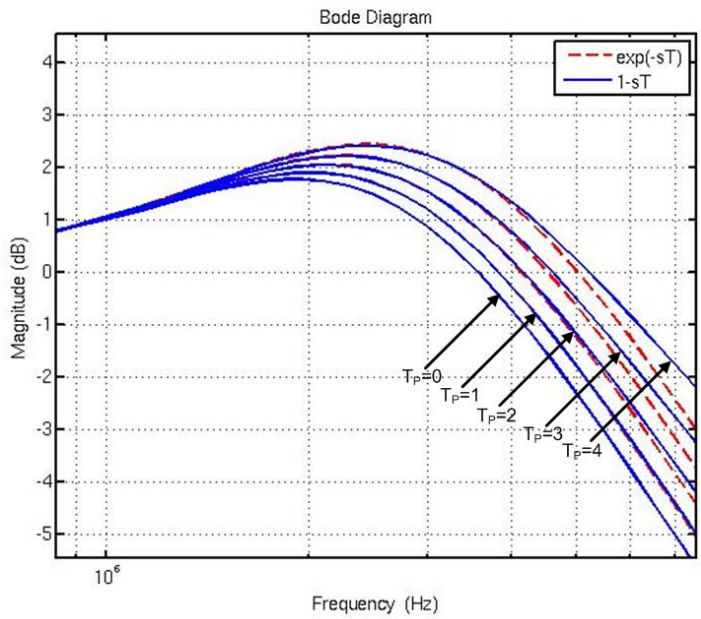


Fig. 3.14 Comparison of the 2nd-order CDR closed-loop transfer functions between *exp(-sT)* latency model (dashed-lines) and *1-sT* latency model (solid-lines) with the fixed α and various proportional latency conditions.

Although the analysis using the *1-sT* model is not perfectly matched to the real characteristics, it shows the effects of increased latency on the loop characteristics

and presents a methodology with which to design a CDR with different latencies between the integral and proportional paths. A comparison of the closed-loop transfer functions between $1-sT$ and the $exp(-sT)$ models is shown in Fig. 3.14. It should be noted that the bandwidth and peaking of the closed-loop transfer characteristics increase in proportion to the proportional latency while the phase margin decreases. In addition, as the proportional latency grows, the mismatch between the models becomes significant. When the latency increases excessively, $exp(-sT)$ can no longer be replaced by $1-sT$. Moreover, the assumption when solving Eqs. (3.23) and (3.24) is not correct.

3.7 Verification with the time-accurate behavioral simulation

To verify these analytical results, a time-accurate behavioral simulation is run on the conventional binary PD and the proposed linearized binary PD sampling method with deliberate phase offsets. The model for the time-accurate behavioral simulation was implemented with synthesizable digital blocks. These included a digital loop filter, a decimator, a FSM, and cell-based analog blocks for behavioral modeling, in this case frontend blocks, DCOs, and phase-interpolators. The entire proposed CDR was designed using a model-first flow, as reported in our prior work [3.16]. Starting the design with accurate, event-driven functional models to simulate a top-level mixed-signal system helps detect problems due to the interaction between the analog and digital circuits while also improving the validation of the design and productivity. Also, the fully automated physical design process gives more flexibility to complete the top design of the chip and allows for easy porting to technologies of different scales.

The gain curves of the conventional binary PD and the proposed linearized binary PD were simulated and compared. As shown in Fig. 3.15, the statistical gain of a conventional binary PD varies with the jitter in the range of 0.01-UI_{rms} to 0.09-UI_{rms}. Within this jitter range, the ratio of the minimum to maximum gain was about 6.65.

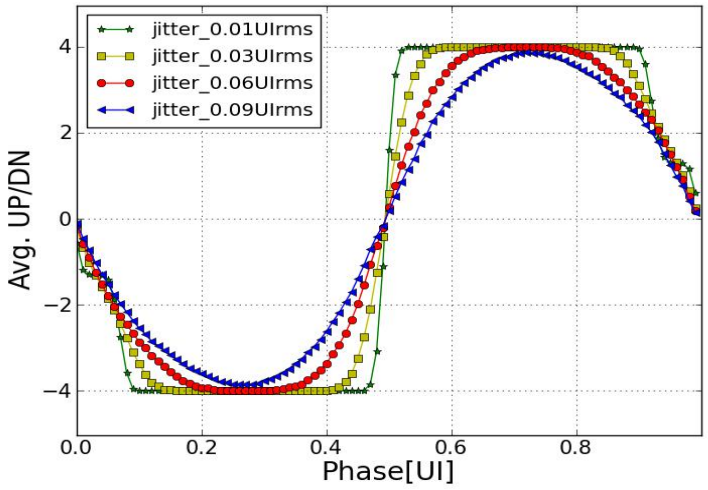


Fig. 3.15 The simulated gain curve of conventional binary PD.

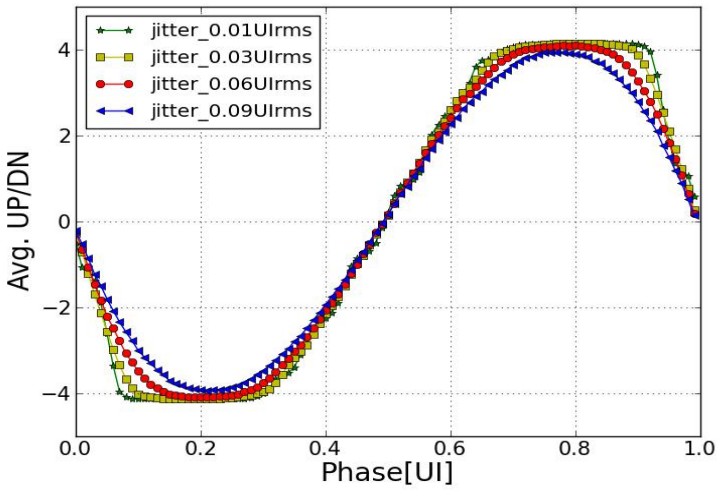


Fig. 3.16 The simulated gain curve of proposed collaborative edge-sampling PD.

On the other hand, the proposed PD maintains a relatively constant gain for various jitter conditions, as illustrated in Fig. 3.16. Under the same jitter condition shown in Fig. 3.15, the ratio of the minimum to maximum gain was only 1.178. The 2^{11}-1 PRBS data with a transition density of 0.5 was used for the test. The simulated CDR has a sampling phase offset θ of 0.033-UI between the channels, allowing linearization with a constant PD gain to be achieved for jitter higher than σ_{jit} = 0.03-UI_{rms} (θ/σ_{jit}=0.91). In the case with jitter of 0.01-UI_{rms}, the gain is also sufficiently bounded close to Eq. (3.10).

When the CDR is simulated with Gaussian random jitter on incoming PRBS data streams at a data rate of 3 Gb/s and with phase noise of -105dBc/Hz in the DCO at a 10MHz offset, the CDR exhibits a relatively fixed 3dB-bandwidth around 7.3-MHz for all of the listed jitter conditions, as shown in Fig. 3.17. As the input noise increases, the jitter transfer curve has bandwidth lower than 3dB. However, the variation is identical to the gain variation of the result shown in Fig. 3.16, bounded within 5% from the targeted loop bandwidth. The case with 0.09-UI_{rms} jitter caused the largest bandwidth shift with an unrealistic value, as its peak-to-peak jitter is more than 0.6-UI. The relatively high peaking of the transfer curve is due to the increased latencies of the proportional path and the integral path, as shown in Fig. 3.14. The design parameters of the simulated CDR are shown in Table I.

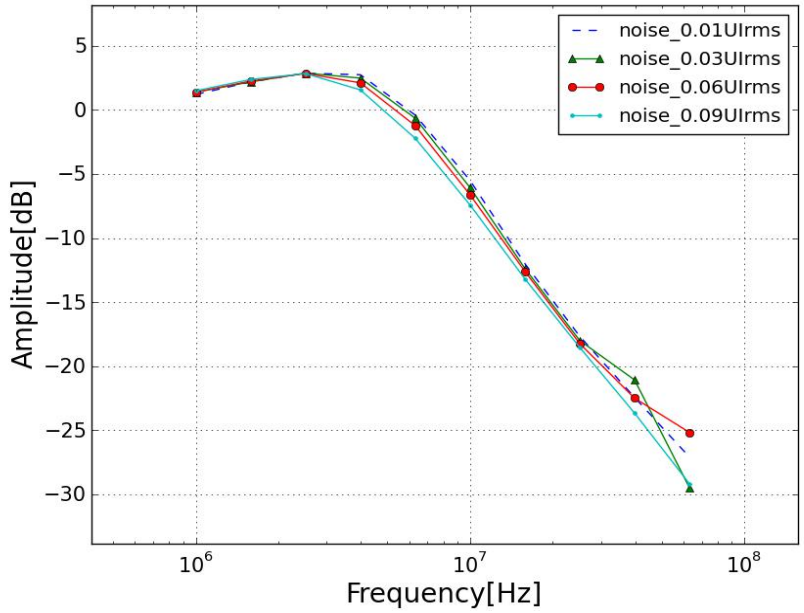


Fig. 3.17 The simulated jitter transfer curve of CDR under the various jitter conditions.

Symbol	Description	Quantity
2N	Number of channels	4
Data rate	Data Rate	6-Gbps
D_{BB}	Binary PD gain	4
θ	Deliberate phase offset	0.33 UI
K_P	Proportional path gain of s-domain model	2.34e7
K_I	Integral path gain of s-domain model	136.83e12
K_{DCO}	DCO gain at 1.5-GHz	2.03 MHz/LSB
P_{NOISE}	DCO Phase noise	-105dBc/Hz @ 10MHz
α	Proportional path gain of z-domain model	1/2
β	Integral path gain of z-domain model	$1/2^7$

Table 3-I. CDR loop parameters

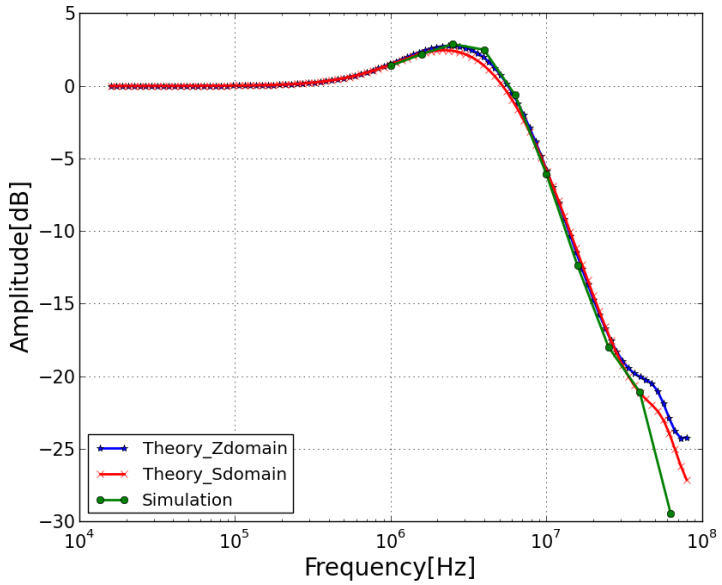


Fig. 3.18 The comparison of jitter transfer characteristic between the simulation and calculation of z-domain and s-domain model.

The designed CDR employing the proposed PD linearization technique has the proportional latency of three reference-clock cycles, which are generated from the error summation block and the decimator with inherent one-cycle delay in a sampled-data system. The integral path has two more sources of latency caused by an accumulator and a delta-sigma modulator. With these latencies, the proposed CDR has a phase margin of 55°, a damping factor of 1.067, and a natural frequency of 18.7 Mrad/s. The jitter transfer function of the designed CDR with those latencies was compared with the z-domain model and the s-domain model in Fig. 3.10, as shown in Fig. 3.18. With the PRBS data stream of each channel with 0.03-UI_{rms} random jitter, the simulated jitter transfer curve is in good agreement with both models. The amplitude of the jitter transfer out of the cut-off frequency decreased by

more than -20dB/decade. Because the added high-frequency zero is shifted to a lower frequency in response to the latency, amplitude peaking increases. Then, according to the imaginary poles with the damping ratio, which falls to below '1,' the amplitude declines more rapidly at a higher frequency than the zero and converges to the same values with the case of zero latency at a much higher frequency, where the effect of the zero is ignored.

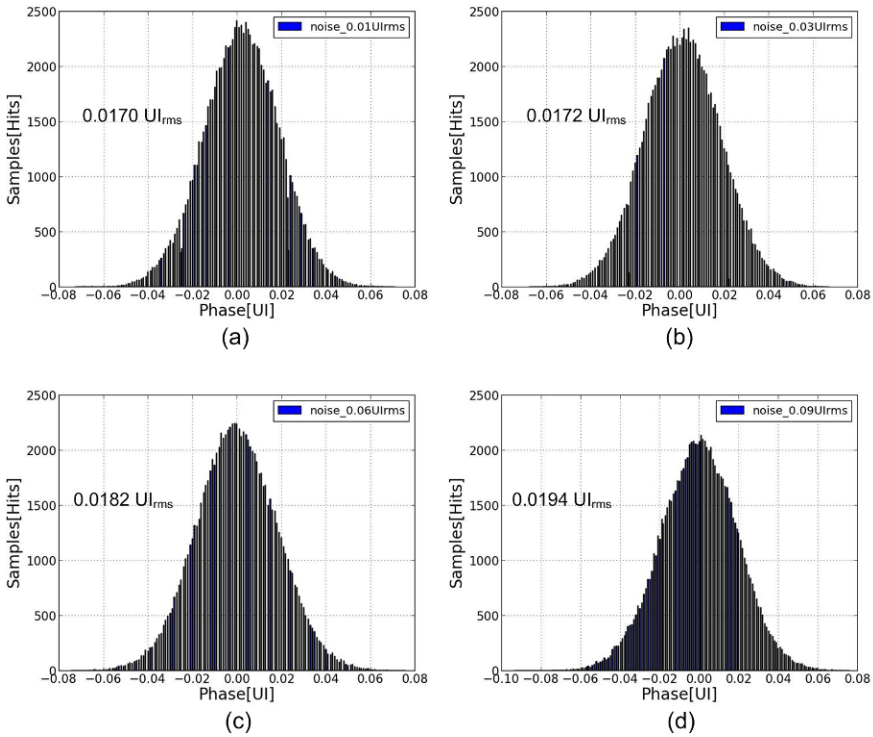


Fig. 3.19 The simulated jitter histogram of recovered clock under the DCO phase noise of -105dBc/Hz at 10-MHz offset and various input noise conditions of (a) 0.01-UI_{rms}, (b) 0.03-UI_{rms}, (c) 0.06-UI_{rms}, and (d) 0.09UI_{rms}.

The jitter of the recovered clock is determined by the noise of the data stream, the DCO phase noise, and the quantization noises of all digital CDRs. Fig. 3.19 shows

jitter histograms of the recovered clock with various noise conditions and DCO phase noise of -105dBc/Hz at a 10-MHz offset. If the phase noise of the DCO is more dominant than the input noise, the jitter is nearly identical in the cases with input jitter amounts of 0.01-UI,rms and 0.03-UI,rms, as shown in Figs. 3.19(a) and (b). In contrast, if the input noise is more dominant than the DCO phase noise, the jitter of the output clock increases according to the amount of jitter in the data stream, as shown in Figs. 3.19(c) and (d). If the loop bandwidth is reduced as the input noise increases, the additional DCO phase noise at a high frequency will greatly increase the output jitter, unlike results shown in Figs. 3.19(a) and (b). Moreover, in the event of dominant input noise, as shown in Figs. 3.19(c) and (d), the reduced bandwidth cannot change the output jitter because the level of the input noise will increase inversely proportional to the bandwidth, resulting in the same amount of filtered input noise. Therefore, this result shows that the proposed and implemented CDR always has a constant loop bandwidth regardless of the input noise conditions. Although the CDR has a constant loop bandwidth, the recovered clock jitter increases slightly due to the deliberate phase offsets at the PDs. This intentionally added noise can be filtered in the CDR loop with a sufficiently low loop bandwidth. However, the bandwidth of proposed receiver cannot be lower owing to spread-spectrum clock tracking. The amount of DCO phase noise used in the behavioral simulation was based on a practical design with the process of Samsung 45-nm CMOS technology.

3.8 Summary

The proposed receiver was fabricated in 45-nm CMOS technology. The entire chip occupied 1200x650 μm^2, as shown in Fig. 3.20. The area of a single core, which consists of a frontend, a phase interpolator, and the FSM of a four-channel receiver, was 0.109 mm^2. The area density for a single channel was 0.195 mm^2.

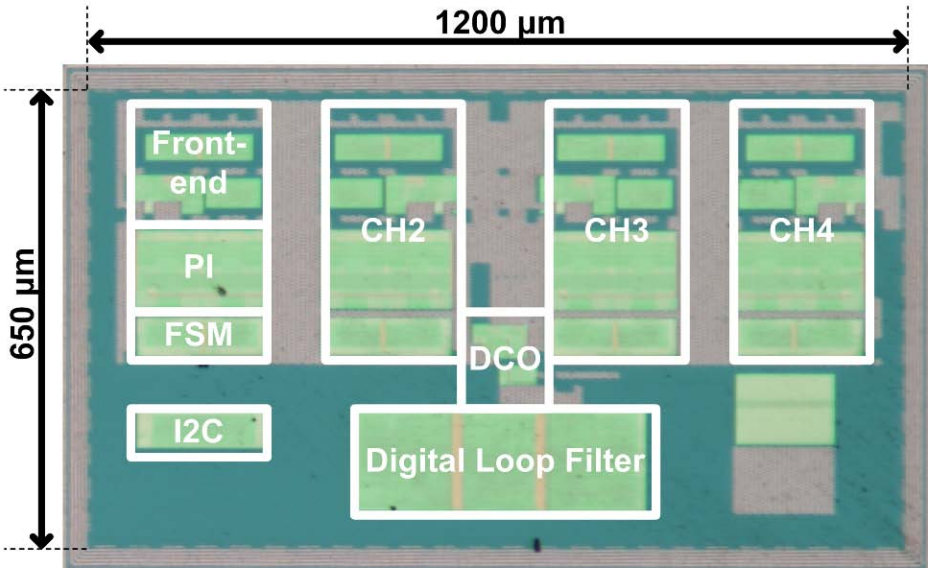


Fig. 3.20 Chip micro-photograph

The overall receiver consumes 71.6 mA with a 1.0 V supply voltage and a data rate of 6 Gb/s, as shown in the performance summary shown in Table 3-II. The largest amount of power was consumed in the phase interpolators and the samplers, which used 39.1% and 25% of the power overall, as shown in Table 3-III. The dominant sources consuming a large amount of power in the sampler are the level-

down converters and the many needed buffers to drive the multiphase clocks. In addition, the regulator of the phase interpolator also consumes considerable power. Although the entire receiver consumed a significant amount of power, the single channel consumed only 17.9 mW.

Process	45-nm CMOS
Circuits	Clock and data recovery circuit
Max. Speed	**6 Gb/s @ 1.0V (1.72V)**
Bandwidth	PAM-4 : 7.34-MHz PAM-2 : 6.60-MHz
Clock Jitter	0.15-UI_{pk-pk} (@6-Gbps) 0.16-UI_{pk-pk} (@3-Gbps)
Power Consumption at 6 Gb/s	Total: 71.6 mW Power/channel: 17.9 mW
Chip Area	Total: 1,200 μm × 650 μm Area/Channel: 195,000 μm^2

Table 3-II. PERFORMANCE SUMMARY

	Blocks	Numer	Power (%)
Frontend	Sampler	4	**25.0**
	Data deserializer Offset calibration Phase detection logics	4	18.3
Clock path	Digital Filter	1	5.4
	DCO	1	2.2
	Phase Interpolator	4	**39.1**
	FSM	4	8.6
	Etc.	1	0.3
Test	Test MUX	1	1.1
Total	Frontend + Clock path	1	100

Table 3-III. POWER BREAKDOWN FOR 6Gb/s

	JSSC-06 [3.17]	ISSCC-05 [3.18]	This work
Architecture	Receiver with CTLE	Receiver without equalizer	Receiver with CTLE
Technology (CMOS)	90 nm CMOS SOI	90 nm CMOS	45 nm CMOS
Supply voltage	1.1 V	1.2 V	1.0 V
Multi-level signaling	PAM-4	PAM-2/ Duobinary	PAM-2/PAM-4
Data rate	22 Gb/s	12 Gb/s	6 Gb/s
Channel number	1	1	4
Single channel area	120,000 μm^2	55,000 μm^2	270,000 μm^2
Area Density	5454 μm^2/Gb/s	4583 μm^2/Gb/s	45,000 μm^2/Gb/s
Power efficiency	10.40 mW/Gb/s	8.08 mW/Gb/s	**2.98 mW/Gb/s**

Table 3-IV. PERFORMANCE COMPARISON

A comparison of these results with those of previous receiver designs for a multilevel signal is shown in Table 3-IV. Even if the area density and the maximum data-rate are lower than Eqs. [3.17] and [3.18], the power efficiency of 2.98 mW/Gb/s of the proposed receiver is much more superior compared to these designs. The proposed receiver occupies a relatively large area due to the large size of the analog blocks, in this case the samplers and phase interpolators. This allows it reduce mismatches and increase the gain.

Chapter 4

The Proposed DLL-Based Receiver with Forwarded-Clock

4.1 Introduction

A source-synchronous receiver based on a delay-locked loop to simplify each lane is presented in this section. It employs a shared global calibration control scheme between the channels and yet achieves channel expandability for a high aggregate I/O bandwidth with the reduced lane complexity. The global calibration control accomplishes skew calibration, equalizer adaptation, and the phase locking of all channels during a calibration period, resulting in reduced hardware overhead and a smaller area of each data lane. In addition, the weight-adjusted dual-interpolating delay cell, which is used in the multiphase DLL, guarantees sufficient phase linearity without the use of dummy delay cells while offering high-frequency

operation. The proposed receiver is designed in 90-nm CMOS technology and achieves error-free eye openings of more than 0.5 UI across 9–28 inch Nelco4000-6 microstrips at 4–7 Gb/s and more than 0.42 UI at data rates of up to 9 Gb/s. The data lane occupies only 0.152 mm^2 and consumes 69.8 mW, while the rest of the receiver occupies 0.297 mm^2 and consumes 56.0 mW at a data rate of 7 Gb/s and a supply voltage of 1.35 V.

4.2 Motivation

Over the past decade, dramatic technological progress of CMOS scaling has increased system complexity, and has consequently necessitated high speed and low-cost I/O circuits. The explosive growth of the need for higher aggregate I/O bandwidth in chip-to-chip communication has forced designers to increase the per-pin data rate, and to expand the number of data channels.

Various techniques have been adopted to increase the per-pin data rate in a system, such as multi-level signaling [4.1], per-pin skew compensation [4.2], channel impedance matching [4.3], channel equalization [4.4] and so forth. Adding the number of channels in parallel interfaces [4.5] or wide I/Os [4.6] is a straightforward way to achieving high data-transmission rates. However, those methods usually have a trade-off between performance and cost. A simple architecture in each lane of data transmission is desired while an accurate clock recovery on the receiver is required for a low bit error rate. To meet these demands, many candidates for the transceiver architectures of serial-data communication have been reported in the literature, including source-synchronous clocking architectures such as forwarded-clock transceivers [4.7] and embedded-clock transceivers [4.8].

A source-synchronous clocking architecture is a simple solution to increase aggregate I/O bandwidth, while reducing channel complexity. When paths and circuits of its shared clock are ideally matched to those of data, the impact of transmit-induced jitter in the receiver can be minimized. Moreover, the cost and

power overhead are amortized across multiple links in the system [4.9]. On the other hand, an embedded-clock link, while no specific clock channel is required, incurs high hardware complexity and is unsuitable for multi-channel links. Since clock recovery must be done in each channel independently, samplers, multiphase generators, and duty-cycle correctors and many other functions must be included in all channels. In addition, any skews between channel propagation delays require local de-skewing circuits.

In this section, a source-synchronous receiver that employs a global calibration control logic for minimizing channel complexity is presented. The presented receiver has a simple data link channel, which consists of only a continuous-time linear equalizer, two half-rate samplers, and a 64-to-2 deserializer. With this simple data lane, only two half-rate clocks to sample at the center of incoming data are generated by a multiphase clock generator, and are distributed to each data lane. All of the functions to adjust the linear equalizer and to find the center of data are performed in the global calibration control logic implemented externally with an FPGA in the prototype chip. This low channel complexity meets the needs of good channel scalability and cost-power optimization.

4.3 Design consideration

To understand its advantages and disadvantages and to explain the development of the new type of architecture, a conventional source-synchronous architecture is introduced, as shown in Fig. 4.1. The receiver is divided into a forwarded-clock lane and a set of identical data lanes. In contrast to the simple forwarded-clock lane, each data lane consists of an equalizer with its adaptation logic, edge and data slicers for 2x-binary phase detection; de-skewing logic to calibrate the channel skew; a multiphase clock generator; a duty-cycle corrector; and a deserializer for serial-to-parallel conversion of the recovered data.

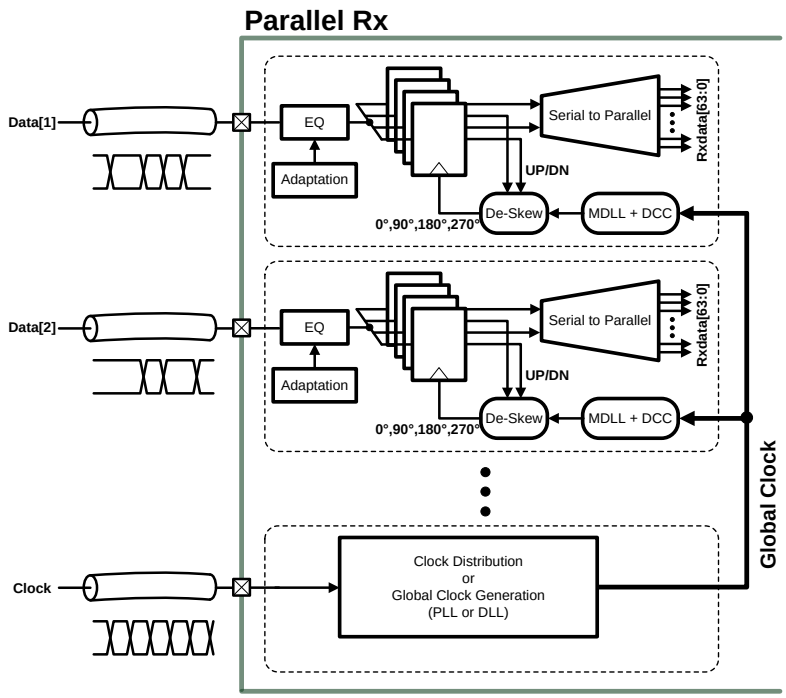


Fig. 4.1 Block diagram of the conventional source-synchronous receiver.

The forwarded-clock lane uses either a delay-locked loop (DLL) or phase-locked loop (PLL) to generate and send the global clock to data lanes or to send the forwarded clock directly to data lanes through the clock distribution circuit. Because a multiphase clock distribution requires many highly capacitive interconnection lines and their buffers, it consumes much power and occupies a large area. Thus, most source-synchronous architectures use a single global clock in either a single-ended or differential form. In each data lane, a DLL or PLL converts the distributed clock into multi-phase clocks, one of which is selected to cancel the channel skew and to sample the received data [4.10, 4.11]. In this architecture, each data lane requires a multiphase generator, a duty-cycle corrector and a de-skewing circuit.

With many functions in each data channel and with high structural complexity, it is inappropriate to expand the number of channels due to the high power and large area. If a receiver adopts a sub-rate sampling method to alleviate the speed budget, the number of multiphase clocks and samplers is increased inversely and exponentially in proportion to the sampling rate. Therefore, an alternative method to reduce the hardware complexity in each channel must be considered in a multichannel receiver, most likely at the cost of increased complexity at the central forwarded clock channel.

The design of a simple and effective equalizer is important for performance. A continuous-time linear equalizer (CTLE) and/or a decision feedback equalizer (DFE) are commonly used methods to compensate for the channel loss in the receiver [4.12]. However, a trade-off between accurate equalization and power

consumption is required; the complex adaptation algorithm of DFE and CTLE coefficients extends the bandwidth, thereby reducing the bit-error rate (BER) while increasing the power consumption and chip area. Therefore, devising a simple and fast equalizer is essential in order to achieve the required bandwidth.

In addition to equalization, the method of channel skew calibration can affect the system performance as represented by the BER. Background calibration is desired in response to the changes in the channel characteristics due to PVT variations. However, it requires a multiphase clock generator or a variable delay line (VDL) in each channel. Also, the additional de-skewing loop should have a very low bandwidth to avoid interaction with the global clock generator or duty-cycle corrector. Therefore, the calibration time is dependent not only on the skew compensation loop bandwidth but also on the other loop bandwidth. If a receiver is allowed a periodic idle time when data are not sent, a training sequence can be used to compensate for the channel skew during the idle time. A fixed training pattern sent during the idle time can be more effectively used to compensate for the channel skew and to accelerate the equalizer coefficient.

4.4 Architecture of the proposed forwarded-clock receiver

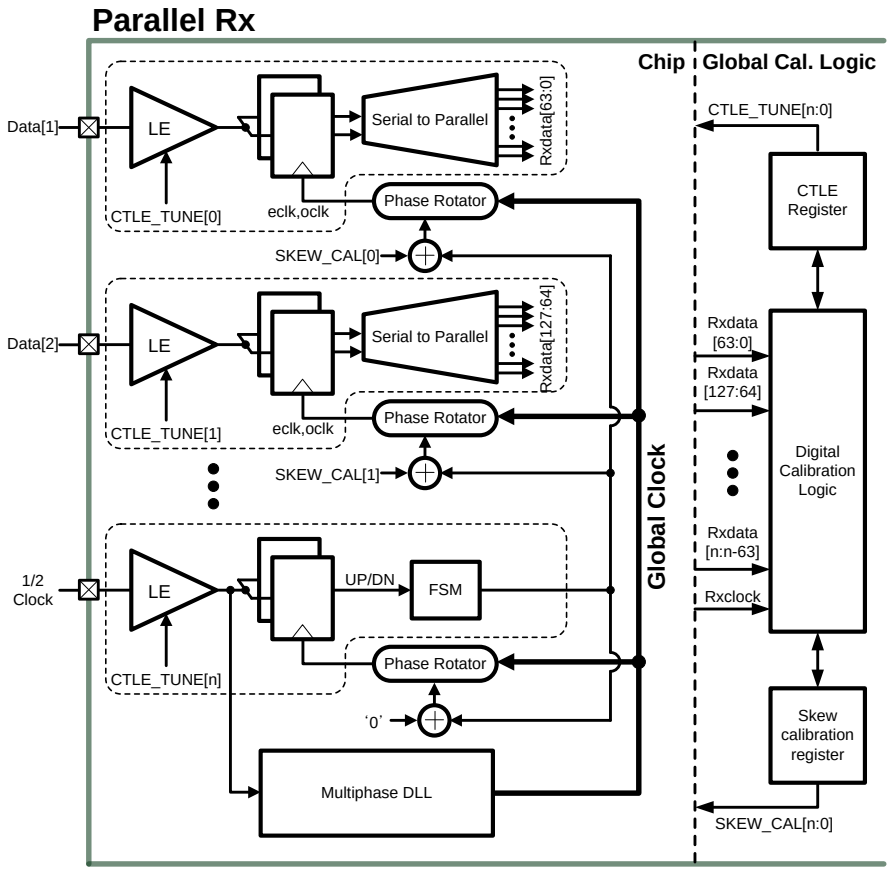


Fig. 4.2 Block diagram of the proposed source-synchronous receiver.

Fig. 4.2 shows the architecture of the proposed source-synchronous receiver. The receiver can be divided into four parts: data lanes, a clock lane, a multiphase generator, and a global calibration control logic. Each data lane compensates for the

channel loss of the incoming serial data stream and converts it to parallel data. The clock lane receives the incoming half-rate forwarded clock and the DLL generates multiphase clocks and distributes them as a global clock. With the globally distributed multiphase clocks, a phase rotator provides the samplers with two half-rate clocks which are aligned to the center of the data eye. The equalization and phase rotation in each data lane are digitally processed by the global calibration control logic. Note that the clock lane has the same equalizer and phase rotator as the data lane and that they are used as a tracking device for the PVT variation.

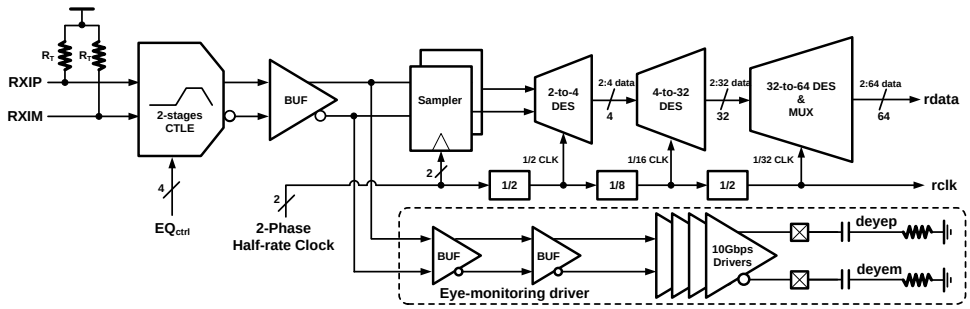


Fig. 4.3 Block diagram of the data lane with a 10-Gb/s driver for eye monitoring.

As shown in Fig. 4.3, each data lane consists of a CTLE, two strong-arm type samplers, and a serial-to-parallel converter to communicate with an external host. The chip includes a high-speed driver to monitor the waveform after equalization with the oscilloscope. This driver uses an inductive-peaking technique to enhance the bandwidth. In a SPICE simulation, the inductively peaked current-mode driver offers a bandwidth of more than 10-GHz under all PVT variations.

The data stream from the differential transmission lines is fed to the CTLE, which consists of a two-stage amplifier. The CTLE boosts the high-frequency components of the incoming data using the source degeneration of resistors and matching bypass capacitors, adapting to the channel attenuation with digitally controlled capacitance. After equalization by the CTLE, its output is buffered and sampled for decisions by two slicers. Finally, the recovered two-bit data are converted to 64-bit parallel data by a deserializer and are fed into the global calibration logic for processing while also being forwarded to an external host.

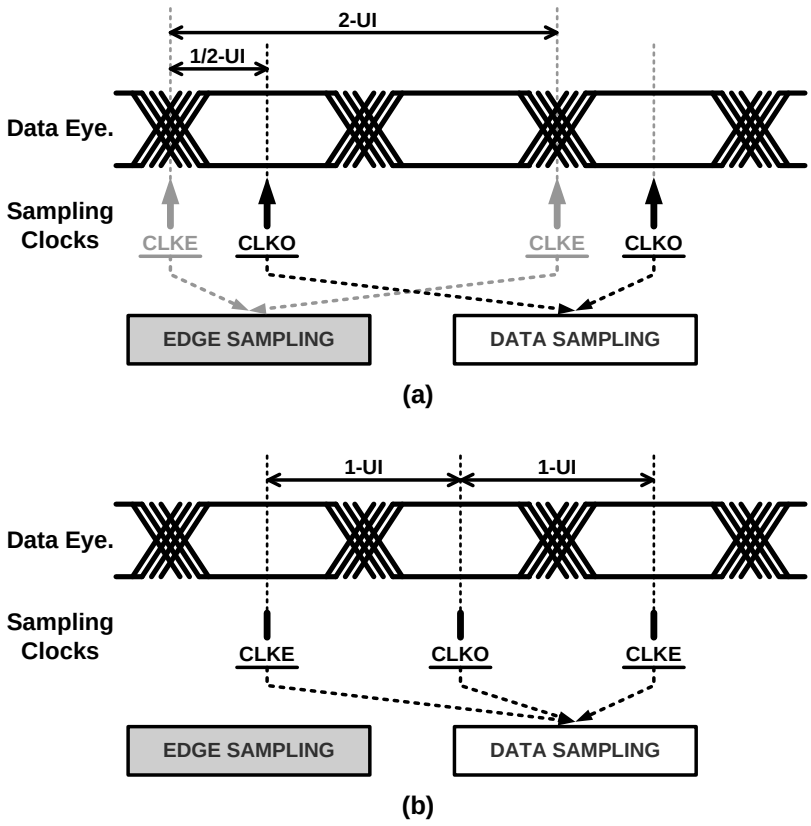


Fig. 4.4 The change of clocking scheme. (a) Calibration mode. (b) Normal mode.

To alleviate the requirements of a high-bandwidth buffer and a DLL, a half-rate clocking scheme is used in the receiver. In this scheme, two slicers are individually used for the sampling data and the edge during the calibration period, whereas both clocks are used for sampling even and odd data in the normal mode, as shown in Fig. 4.4. The number of samplers is reduced by half and the hardware cost is equivalent to that of the full-rate 2x-oversampling CDR, but with greatly reduced timing requirements. During the calibration mode, a full-rate scheme is used for a half-rate training pattern, as shown in Fig. 4.4(a) and, when switched to the normal operation mode, a half-rate scheme is used on the full-rate input as shown in Fig. 4.4(b). The correct sampling time is determined by estimating and cancelling two types of skew: on-chip skew due to the equalizer, clock generator, and clock distribution path and the skew among transmission lines. Both are cancelled in different ways.

The clock lane delivers the incoming half-rate clock to the multiphase clock generator and compensates for the delay variation of the clock path that is caused by the PVT variation. Except for the finite-state machine (FSM), the clock lane is a replica of the data lane to reduce the mismatch between the data path and the clock path. The FSM generates compensation codes for the variation in the delay, which is caused by the clock distribution from the multiphase DLL to the sampler of the individual channels. The distributed clock is compared with the incoming clock at the samplers of the clock lane. The FSM increases or decreases the phase control code of the phase rotator (PR) with hysteresis according to integrated up and down signals.

The clock received by the clock lane is distributed to each data lane by a multiphase clock generator. It has a dual-loop architecture that consists of an analog DLL to generate multiphase clocks, and a digital DLL to compensate for the channel skew. The analog DLL generates ten equally spaced multiple clocks, and the PR, which is a sub-block of the digital DLL, selects the data sampling clock by phase interpolation between two incoming adjacent clocks. The selected half-rate clocks are delivered to samplers of each channel through the clock distribution circuit with buffers. With the analog and digital DLL, the total number of phase steps to control is 80.

The CTLEs, PRs, and DLL of all lanes are controlled by the global calibration control logic monitoring the recovered data and the clock in the data lanes. The global calibration control logic consists of registers for the phase and equalizer control and a digital calibration logic that performs the following three functions: phase locking, channel skew calibration, and equalizer adaptation. Basically, methods of iteration and memorization are used to perform the functions for an appointed calibration period. When the equalizer coefficient and phase control are changed, the sampled and deserialized data in the data lane are monitored and stored in the digital calibration control logic and the logic builds a table to find the optimized results. The change will be repeated until the calibration logic finds the optimized equalizer coefficients and the accurate phase of edge crossing and they are stored in the CTLE register and the PR register, respectively.

In the global calibration control logic, the accuracy of skew compensation and equalizer adaptation is proportional to the multiphase resolution of the sampling

clocks. Because most of the equalizer adaptation results and the skew compensation results are memorized and processed using a unit with a minimal phase step, the receiver needs the fine phase resolution of the clocks. To achieve a high resolution, a large number of delay cells can be used in the design of a DLL. However, a large number of delay cells, including dummy cells, consumes too much power and occupies a large area of the DLL. In the proposed DLL, a weight-adjusted dual-input interpolating delay cell is used to reduce the number of dummy delay cells [4.13].

With this global calibration control logic, the proposed architecture takes advantage of the reduced hardware overhead. Because the global calibration logic finds the edge of the data and programs the register of the PR for the calibration period, the number of channel slicers is only half of the conventional architecture. In addition, the PRs are located close to the global DLL such that only two half-rate clocks are distributed to the samplers of each channel, reducing the buffer power and area.

The proposed receiver was designed for high-speed multichannel links, such as wide I/O memory interfaces requiring low channel complexity and small clock distribution circuits. A designed CTLE achieves a gain in the range of 9 dB to 25 dB at 7 GHz for various channels, such as Nelco4000-6 microstrips and RG58 coaxial cables. The multiphase generator, which consists of the DLL and PRs, provides 80-step multiphase clocks for two UIs.

4.5 Circuit description

4.5.1 Analog multi-phase DLL

As described in the introduction, the forwarded-clock architecture keeps the same transmit-induced jitter among channels. The correlated jitter should be tracked by a clock recovery circuit in the receiver. There are two general clock generation schemes, the PLL or the DLL, in the forwarded-clock architectures. Since the PLL has a low-pass jitter transfer characteristic, high-frequency jitter beyond the cut-off frequency is filtered out. Therefore, a recovered clock has superior jitter performance when compared to the DLL. However, the excessively low loop bandwidth lessens the tracking performance of data-correlated jitter. Eventually, the bit error rate (BER) can be worsened. Unlike the PLL, the DLL has an all-path jitter transfer characteristic. So the internal phase error is not accumulated and the sampling clock can be aligned more precisely at the center of a data eye. Therefore, the DLL-based source-synchronous architecture is a better solution toward achieving the high aggregate bandwidth.

The operation frequency of the DLL is often limited by the speed of the phase detector (PD), and the minimum delay of the voltage controlled delay line (VCDL). In the proposed DLL, the VCDL consists of dual-input interpolating delay cells (DIDCs) to achieve delay time less than an inverter delay. In addition, a divided-by-4 clock is used in the PD to alleviate its speed budget [4.13].

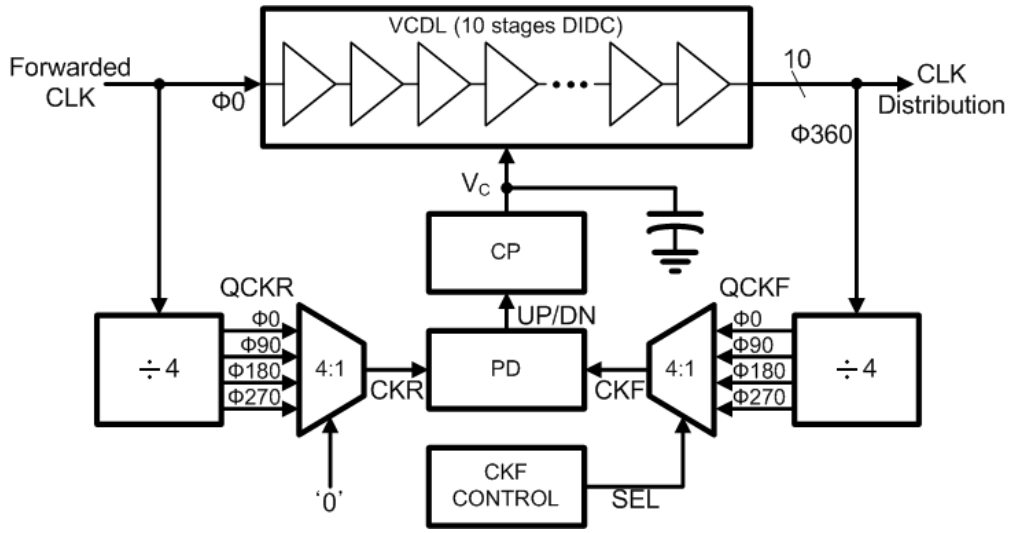


Fig. 4.5 Block diagram of the analog DLL with the anti-harmonic-lock circuit.

Fig. 4.5 shows the high-speed analog multiphase DLL that employs the 10-stage DIDC. The forwarded clock from the CTLE is transmitted to both the VCDL and the frequency divider. Then the divided clock is compared with the delayed and divided VDCL clock by the bang-bang phase detector (BBPD). Its comparison result (UP or DOWN) changes the Vc and controls the delay of the VCDL through the charge pump and the filter capacitor.

To prevent the harmonic-lock problem, CKF control block is used to select the phase of CKF. After frequency division, the phase difference between CKR and CKF could be more than one period of the forwarded clock, resulting in a harmonic lock. When the DLL is in the reset state, the control voltage Vc of the VCDL is pulled up to VDD to make the delay minimized. Then, the CKF control block samples all of the 4-phase CKF<0:3> with the CKR<0> which has a fixed phase. Using the sampled pattern S<0:3>, the CKF control block selects one of the 4-phase

clocks, whose phase is closest and leading to that of CKR<0>. For example, if the sampled values of CKF<0:3> with CKR<0> is '1100' like the case2, the selected CKF is CKF<1>. The selected clock guarantees the phase difference to be less than a single period of the forwarded clock (T_{ref}), the startup direction of phase detection is down, and consequently harmonic lock is prevented.

4.5.2 Dual-input interpolating deley cells

Under an operating frequency of a few Giga-hertz, the multiphase resolution of a clock generator is limited by the minimum delay of cells. To achieve a small delay of VCDLs, several techniques are employed in voltage-controlled oscillators (VCOs) such as the negative skewed delay scheme and dual-input interpolating delay cell [4.15-4.17].

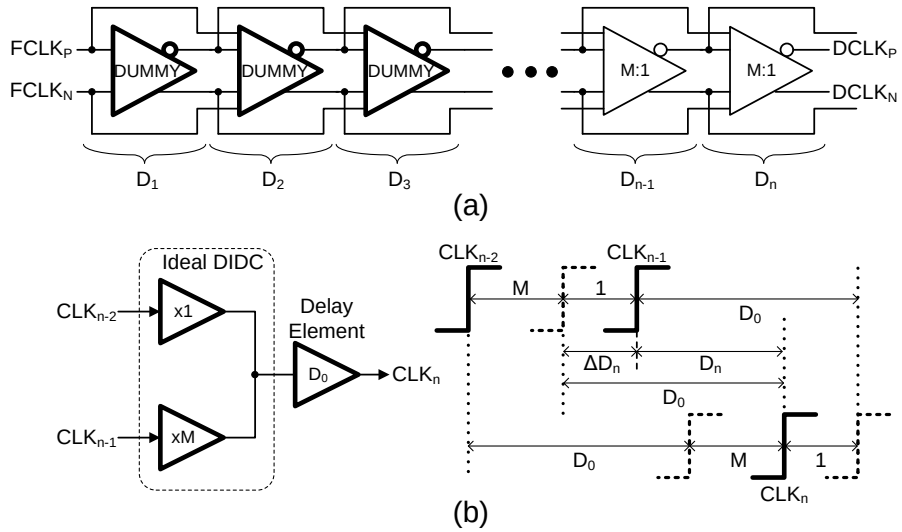


Fig. 4.6 (a) Dual-input interpolating delay cells and (b) an equivalent block diagram of a cell.

However, those methods cannot be easily applied to the VCDL because of delay mismatches among the delay cells [4.18]. In order to reduce the delay difference between early stages and following stages in the chain of delay cells, a few dummy delay cells are typically used until those operating conditions are equalized. Fig. 4.6 shows the basic principle and scheme of the DIDC chain. The delay mechanism of the dual-input interpolating delay cells can be explained by the phase interpolation, as illustrated in Fig. 4.6(a). If the phase interpolator (PI) has an intrinsic delay of D_0, the weighting ratio of its two inputs CLK_{n-2} and CLK_{n-1} is set to M:1, and the output is delayed by D_0 with interpolation ratio, then, the delay difference ΔD_n between the interpolated output and the CLK_{n-1} is given as

$$\Delta D_n = \left(\frac{1}{M+1} \right) D_{n-1} \tag{4.1}$$

where D_{n-1} is the time difference between two inputs which are equal to the delay of the previous stage in the DIDC. Then, the effective delay D_n between CLK_{n-1} and CLK_n can be written as

$$D_n = D_0 - \Delta D_n = D_0 - \left(\frac{1}{M+1} \right) D_{n-1} \tag{4.2}$$

This recursive equation shows that the delay in each cell just keeps decreasing as the clock propagates through the delay line and the delay of the DIDC converges to a specific value as follows, as the number of the delay cells approaches infinity:

$$\lim_{n \to \infty} D_n = \left(\frac{M+1}{M+2} \right) D_0 \tag{4.3}.$$

As a result, many dummy cells are required for all cells to have an equal delay time while consuming a lot of power.

If the interpolation weight of a few delay cells is adjusted to a different value from other delay cells [4.13], the number of required dummy delay cells can be drastically reduced. If the delay of the first stage is fixed at D_0, and the interpolating ratio of the second delay cell is M+1:1, the delay of the second stage can be expressed by

$$D_2 = D_0 - \left(\frac{1}{(M+1)+1}\right) D_1 = \left(\frac{M+1}{M+2}\right) D_0 \qquad (4.4)$$

This is identical with the converged value of Eq. (4.3). With the recursive relation shown as Eq. (4.2), the next delay times of the delay cells are always the same as that of the second delay cell. Therefore, delay times of the weight-adjusted DIDC converge to $(M+1)/(M+2)D_0$ from the second and following delay cells, regardless of the interpolating ratio M, while only one dummy cell is required.

4.5.3 Dedicated half-rate data samplers

To alleviate the speed budget of logics in the data lane, a half-rate clocking scheme is commonly used. The half-rate clocking scheme needs two sampling circuits to alternatively sample the data at the rising and falling edges. Then, the sampling with the rising and falling edges of a clock often requires a duty-cycle corrector (DCC), thus increasing the design complexity of each lane.

To remove the DCC and to change the sampling mode between calibration and data recovery in the data lane, an alternative interleaved data sampling scheme is

implemented, as shown in Fig. 4.7. Each sampler is triggered by different clocks, the phases of which are controlled by dedicated PRs, and ideally spaced at 180 degrees in the case of the data sampling mode.

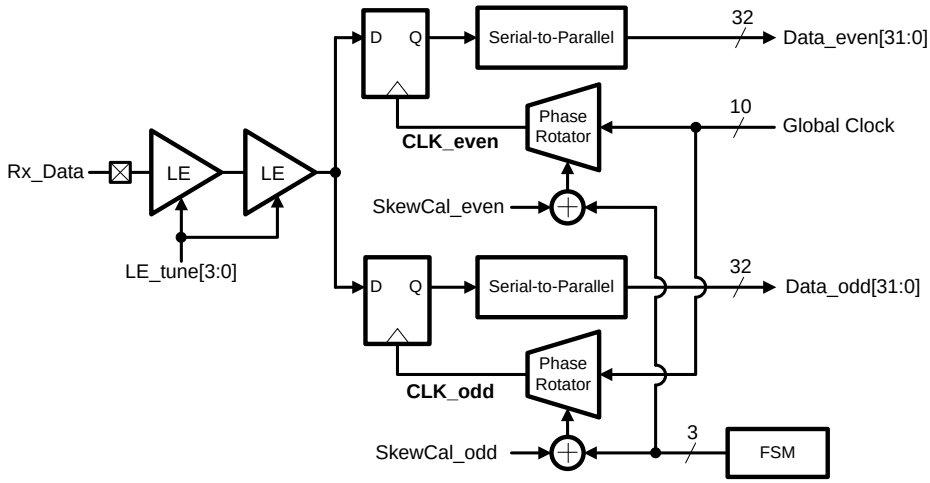


Fig. 4.7 A data lane employing the dedicated data samplers without DCC.

If the outputs of the equalizer or the transmitted global clocks have a duty distortion, the individual skew calibration code corrects the error. That is, CLK_even and CLK_odd can be individually located at the center of the data eye without any DCC when the duty of global clock is distorted. In addition, these separated clock control circuits can be used to detect the edge of incoming data during the calibration period during power-up. If CLK_even and CLK_odd are closely located at the adjacent phase, the sampling results around the data edge with those clocks are different. Particularly, when the data pattern is pre-programmed without any inter-symbol interference (ISI), such as ‘101010’, accurate edge information can be detected. In the proposed receiver, this edge detection method is

used to calibrate the channel-skew to adapt the equalizer and to align the sampling clocks to the center of data.

4.5.4 Cherry-Hooper continuous-time linear equalizer

A continuous-time linear equalizer is a very simple and effective solution to boost the high-frequency signal of the incoming data. However, its limited bandwidth is a bottleneck for the performance of the whole system. There are several methods to increase the bandwidth of a linear equalizer, such as inductive peaking and a negative capacitance technique [4.12]. But, those techniques are not suitable for designing passive devices for a multi-channel receiver configuration requiring a large area.

Fig. 4.8(a) shows the implemented linear equalizer exploiting the Cherry-Hooper broadband technique. The Cherry-Hooper technique incorporates local feedback in the drain-to-gate network to improve the speed [4.19]. The implemented linear equalizer consists of two cascaded common-source amplifiers. The first stage boosts the high-frequency signal of the incoming data, using a source degeneration resistor R_S and capacitor C_D. These degeneration devices are controlled by the 4-bit digital code generated by the global calibration logic. Each capacitor bank has a symmetric architecture to remove the mismatch of differential outputs, and the use of parallel connection reduces the area by 1/4 in comparison with a series connection [4.20].

The first stage amplifier is connected to the second common-source amplifier by a feedback resistor R_F. In contrast to the first stage, the second stage amplifies all frequency signals within its wide bandwidth. With the high resistance of R_F, the dominant pole of the linear equalizer is gm_2/C_X, where gm_2 is the transconductance of

transistor M2, and C_X is the capacitance of node X. This dominant pole is much higher than R_{D1}/C_X of the first stage, thus enlarging the whole bandwidth of the linear equalizer.

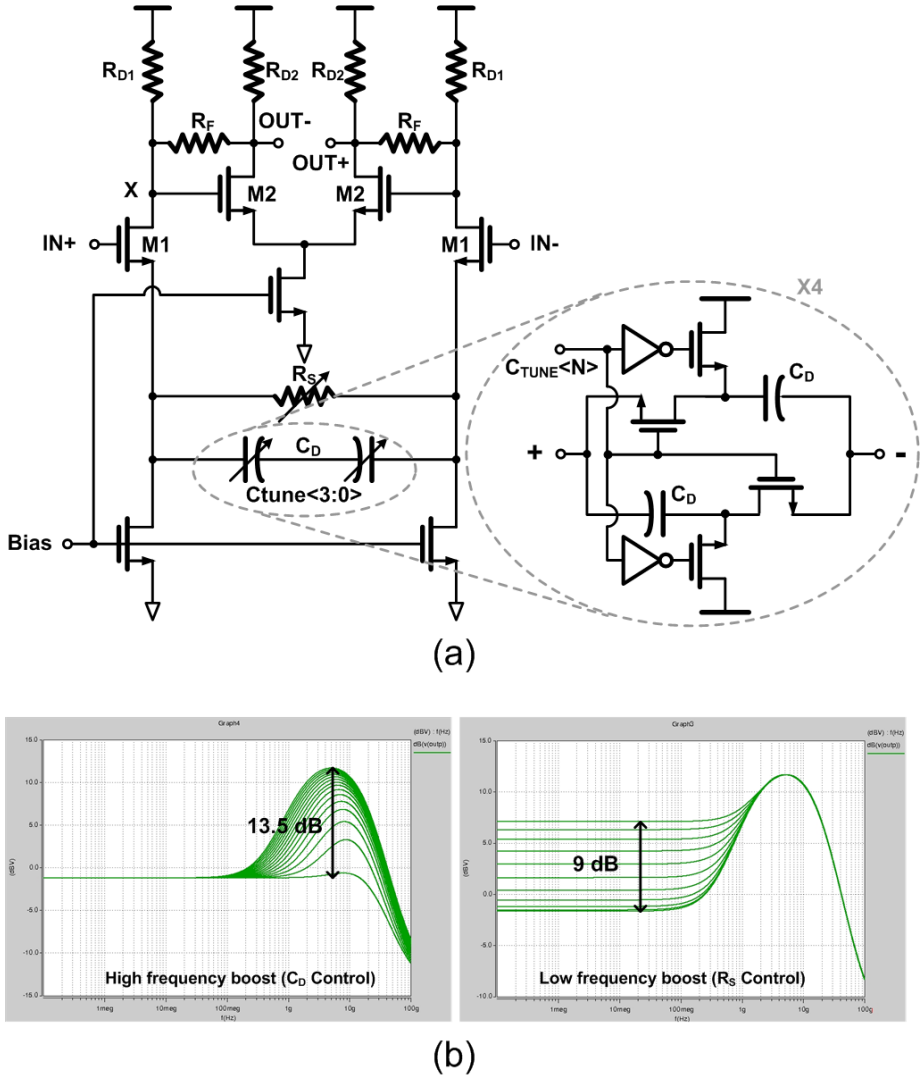


Fig. 4.8 (a) The Cherry-Hooper linear equalizer, and (b) its frequency response.

The single linear equalizer has a maximum 13.5-dB gain at the Nyquist rate of 7-Gb/s and 9-dB gain at the DC, as shown in Fig. 4.8(b). To compensate for channel loss of more than 16.5 dB, each lane in the proposed receiver has a two-stage Cherry-Hooper linear equalizer that can boost from 9 dB to 25 dB at 3.5 GHz.

4.5.5 Equalizer adaptation and phase-lock scheme

Since many widely used high-speed cables are minimum-phase-like systems [4.21], the magnitude of frequency response is related to its phase response. Therefore, an optimized result of amplitude equalization almost coincides with an optimized result of phase equalization. In other words, the well-equalized phase of received data guarantees fairly large vertical eye opening. In this paper, the CTLE for group delay or phase delay minimization, which also has a minimum-phase or minimum-phase-like characteristic, is used to compensate for the loss of the minimum-phase channel.

For phase equalization, group-delay variations under various frequency conditions of the training sequence can be minimized. If the signal is transmitted through the channel with a limited bandwidth, ISI will show up, due to the fact that different signal frequency components are delayed by different amounts. Fig. 4.9(a) shows the channel characteristic, and the results of ideal constant group delay equalization in the frequency domain. The linear equalization at high frequency is commonly described by the gain boosting, as shown in the left side of Fig. 4.9(a).

However, in the minimum-phase system, channel loss and equalization can be explained by the phase distortion, as shown in the right side of Fig. 4.9(a). The loss of real channel causes phase distortion above its cutoff frequency. On the other hand, the

phase below the cut-off frequency is relatively linear, similar to the phase characteristic of an ideal lossless channel.

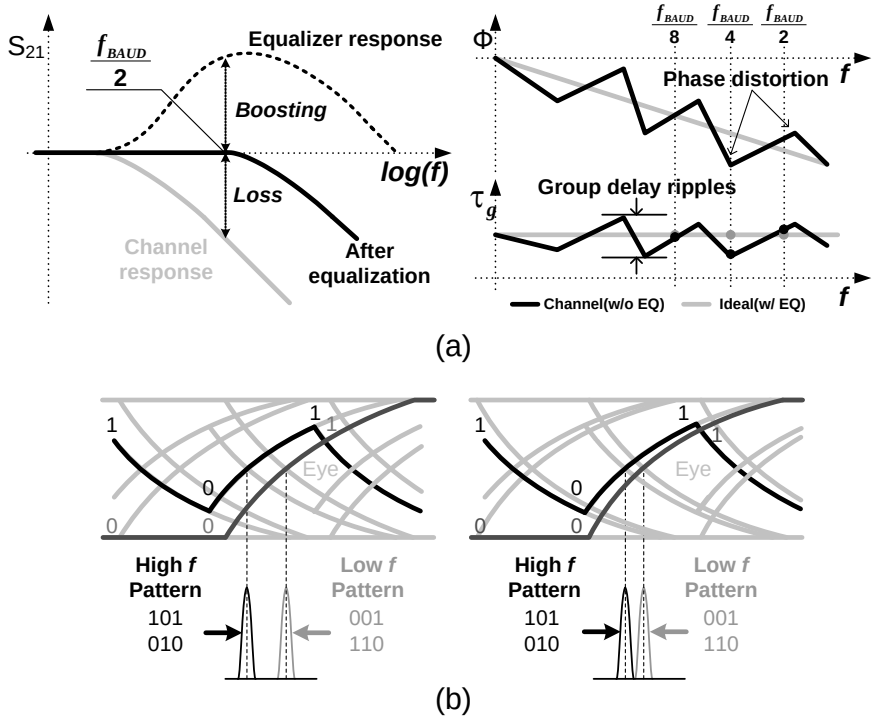


Fig. 4.9 Comparison between the output of channel and the result of constant group delay equalization by (a) frequency response and (b) eye-diagrams.

Since group delay is a derivative form of phase, a relatively linear phase means constant group delay, and phase distortion means group delay variations. If ripples or variations of group delay under various frequencies can be detected, the phase after equalization can be linear, close to that of an ideal lossless channel. In the proposed EQ adaptation, we use the segmented multiphase and pre-programmed calibration sequence, the frequency of which is generated by dividing the Nyquist rate by various integers, to detect the minimum variation of group delay under the various frequency

conditions. The results of group delay (or phase delay) variation, according to signal frequency in time-domain, are shown in Fig. 4.9(b). When the loss of received data is not compensated for, crossing points generated from different data patterns are located in different phases, and its convolution with random noise reduces the lateral and vertical eye opening, as shown in the left side of Fig. 4.9(b). In contrast, the crossings of gain-boosted data after adaptation using a CTLE are centered where the group delay variation is minimized, as shown in the right side of Fig. 4.9(b). Then, not only the lateral eye opening, but the vertical eye opening also is optimized.

The whole process of equalizer adaptation and phase lock is divided into two states: a coarse-lock state and a fine-lock state, as shown in Fig. 4.10. In the coarse-lock state, a CTLE control bit and a PR control bit for the group delay minimization are roughly detected using a pre-programmed training sequence such as ‘0101’ or ‘00001111’. When the calibration enable signal is turned on, the DLL in the receiver is locked to the forwarded clock, and generates 80 phases for 2 UIs. Then, the global calibration logic changes the CTLE control bits from minimum to maximum under various frequency conditions of the pre-programmed pattern, as shown in Fig. 4.11(a). At every control of the CTLE, positions of data transition are detected by the shift of the multiphase clock, and stored in a table, as illustrated in Fig. 4.11(b). After detecting and storing the results from all parameters, the global calibration logic calculates the CTLE control bit that minimizes the phase variation of the training sequence after equalization. Then, this CTLE control bit and the phase control bit are set to coarse lock parameters.

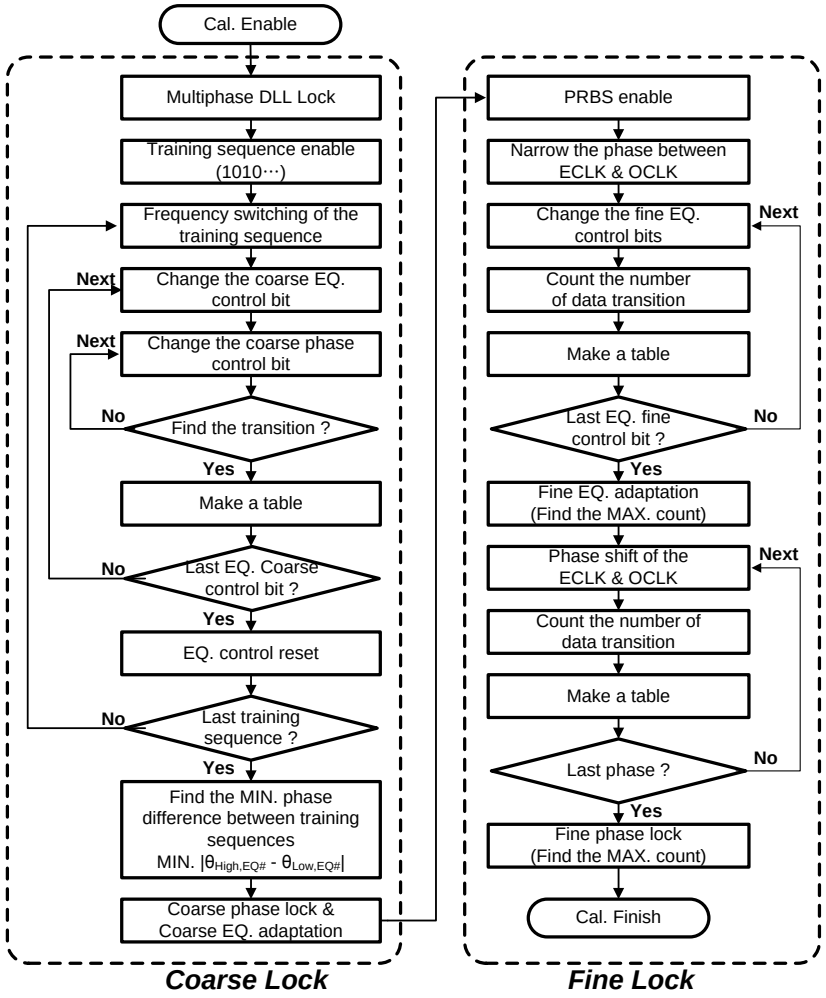


Fig. 4.10 The flowchart of equalizer adaptation and phase lock.

After the coarse lock, the training sequence is changed to PRBS, and then a fine CTLE control and a phase control are determined and stored in the registers. Unlike the coarse lock operation, only a few control bits around the fixed control bits are varied to find out the optimum parameters to reduce the calibration time. In addition, the number of different sampling results between the even and odd samplers, such as '10' or '01', are counted to scan the amount of jitter after equalization. First of all,

two even and odd sampling clocks (*CLKE* and *CLKO*) are suitably spaced near the edge of data, which is found in the coarse lock state by the targeted amount of jitter. Then, the counting results at every fine CTLE control are stored in a table. When the counted number is maximized, the control bit is finally set to the CTLE register.

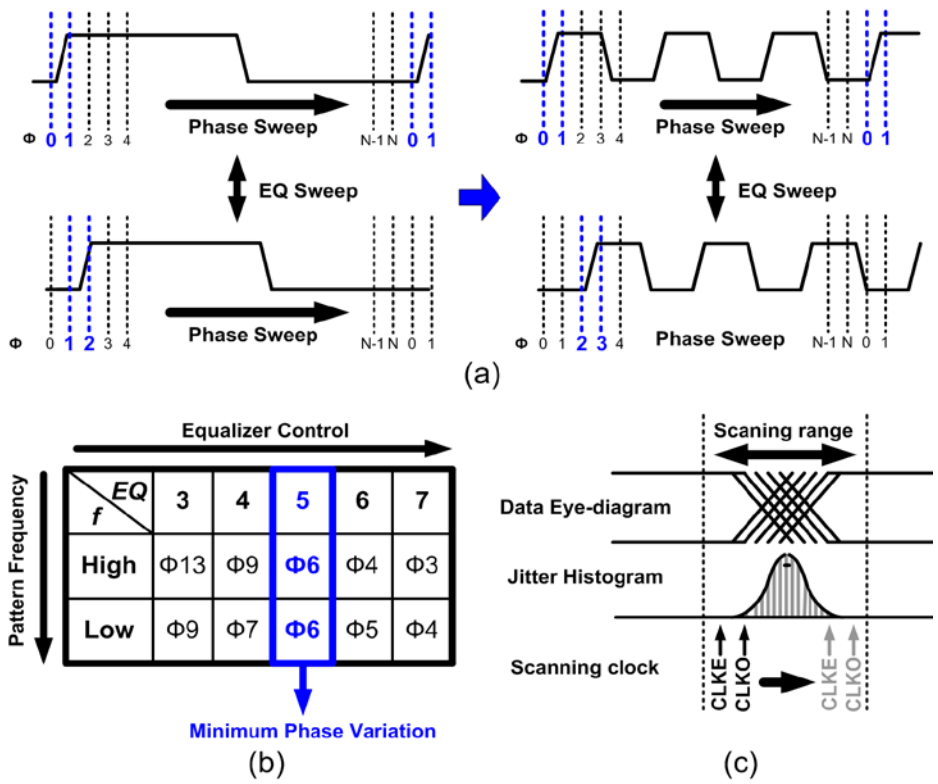


Fig. 4.11 (a) Equalizer sweep and phase detection at the high- and low-frequency training sequence. (b) Coarse phase lock and equalizer adaptation. (c) Scanning of the jitter histogram at the fine-lock states.

With this fixed CTLE control, the jitter histogram of the eye diagram is statistically monitored by scanning the XOR-outputs of sampling results at *CLKE* and *CLKO*, as shown in Fig. 4.11(c). Then, the phase at the maximum counts is selected to the accurate edge location of the equalized data. Finally, these fine CTLE

control bits and fine phase control bits are stored in the CTLE and PR registers, respectively. After the entire calibration process, the two sampling clocks are located to the center of even and odd data, respectively, without any channel skews.

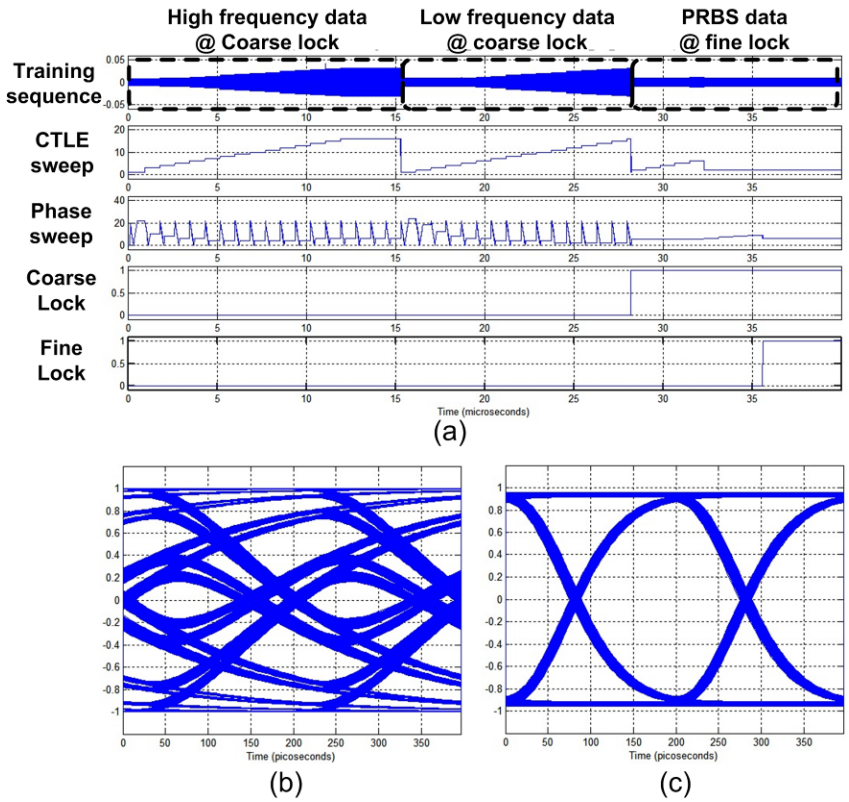


Fig. 4.12 The results of behavioural simulation: (a) The whole calibration process. (b) Eye diagram before the equalization. (c) Eye diagram after the equalization.

Fig. 4.12 shows behavioral simulation results of the entire process. As shown in Fig. 4.12(a), the training sequence can be divided into three sections: a high-frequency training sequence, a low-frequency training sequence, and a PRBS. During the period of high and low frequency training sequences, the global

calibration logic finds the coarse CTLE parameters and the location of edge crossing using equalizer sweep and phase sweep. In the case of coarse-lock state, the global calibration logic roughly increases and decreases the phase-control by two bits at a time. When the coarse-lock is done, the global calibration logic reduces the phase spacing between two sampling clocks to monitor the eye diagram after equalization. In this fine-lock state, both the equalizer sweep and the phase sweep are finely trimmed, by one bit, for a narrow range. In the simulation results, the CTLE is finally locked to the 5^{th} control bit of the total 15-steps, and the phase is locked to the 6^{th} control bit in the total of 80 steps. At the fine-lock state, the 5-Gb/s eye diagrams after channel (RG58-8m coaxial cable) and equalizer are shown in Fig. 4.12(b).

The total calibration time is about 40 μs for one channel. If single global logic rotationally calibrates all channels, the time will increase in proportion to the number of channels. In addition, this calibration process should be repeated in every idle state or special calibration period to adapt to the various time-variant conditions.

4.6 Measurement results

The proposed receiver was implemented using a 90-nm CMOS process. To confirm the function and performance of the receiver, the BER is measured by an Agilent J-BERT N4903A serial bit-error-ratio tester. The transmitted data and clock through the channel are recovered and parallelized by the fabricated chip. The parallelized data is fed to the FPGA, which serves as the global calibration logic. Using this FPGA, the equalizer is adapted to various channel conditions and the sampling clock is locked to the center of the incoming data while compensating for the channel skew. The result of the equalization and multiphase clocks can be monitored by an oscilloscope. The test environment for the fabricated chip is shown in Fig. 4.13.

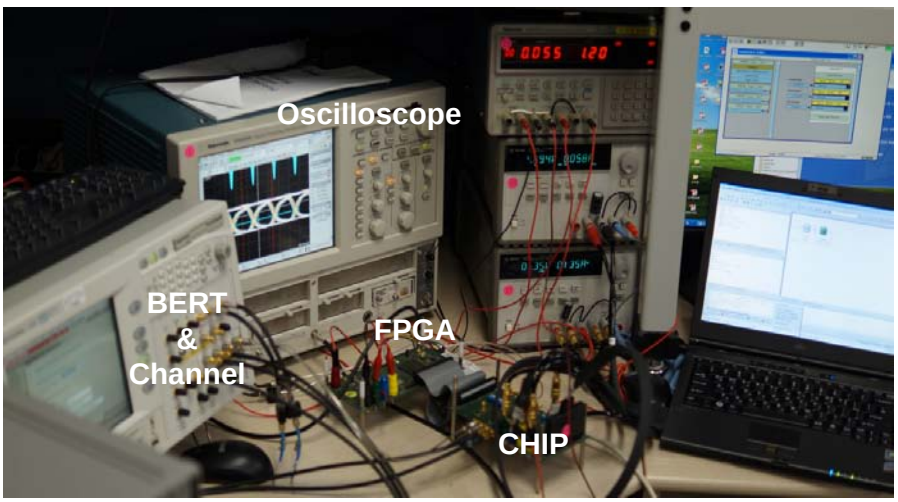
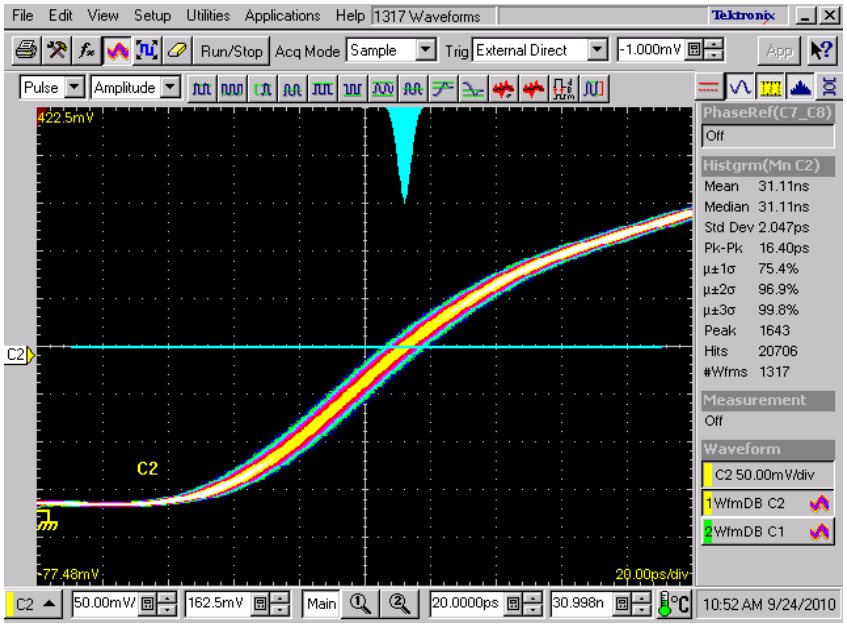
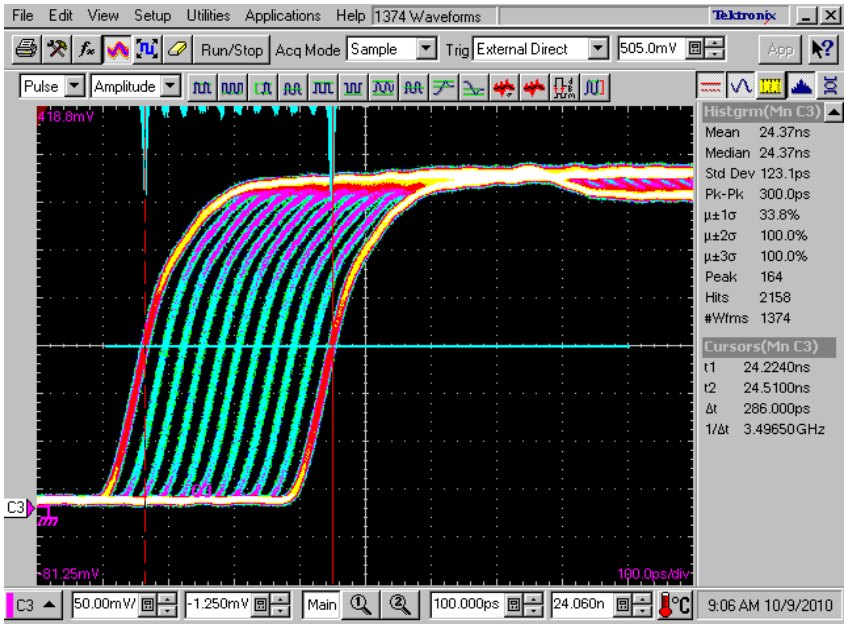


Fig. 4.13 Test environment for the fabricated chip.



(a)



(b)

Fig. 4.14 Recovered clock (a) jitter, (b) multiphase clocks at 3.5-GHz.

Digital and analog buffers are used to monitor the phase resolution of the multiphase generator and eye opening after the CTLE. The clock of the DLL was divided by 144 to mitigate the bandwidth requirement of the digital buffer. In contrast, the analog buffer uses inductive peaking to enhance the bandwidth by 10 GHz. The recovered and divided clock with the 3.5-GHz forwarded clock is shown in Fig. 4.14. The RMS jitter of the clock is 2.05 ps and the peak-to-peak jitter is 16.4 ps, as shown in Fig. 4.14(a). However, the RMS jitter of the forwarded clock is 1.50 ps such that the jitter added by the DLL is only 0.55 ps. Fig. 4.14(b) shows the phase space of the DLL exploiting the weight-adjusted DIDC. With just two dummy delay-cells, the DLL shows a small differential nonlinearity of less than +/-0.18 LSB between its ten phases at 3.5 GHz. However, the measured static phase offset caused by the mismatches between the BBPD and the charge pump was 7.14 ps when the DLL was locked at 4.5 GHz.

The total phase nonlinearity of the recovered clock, including the DLL and PR, is shown in Fig. 4.15. The measured results show a tendency for the linearity to degenerate when the data rate is lower. Under various frequency conditions, all results of differential non-linearity (DNL) and integral non-linearity (INL) are +/-0.8 LSB and 0/-5LSBs, respectively. Owing to the relatively large phase-interpolation mismatch in the PR, the entire multiphase linearity is changed for the worse. However, its phase resolution is small enough to obtain the targeted BER. Therefore, this is not a serious problem. In the ideal case, the phase resolution of the 3.5-GHz clock is only 3.57 ps.

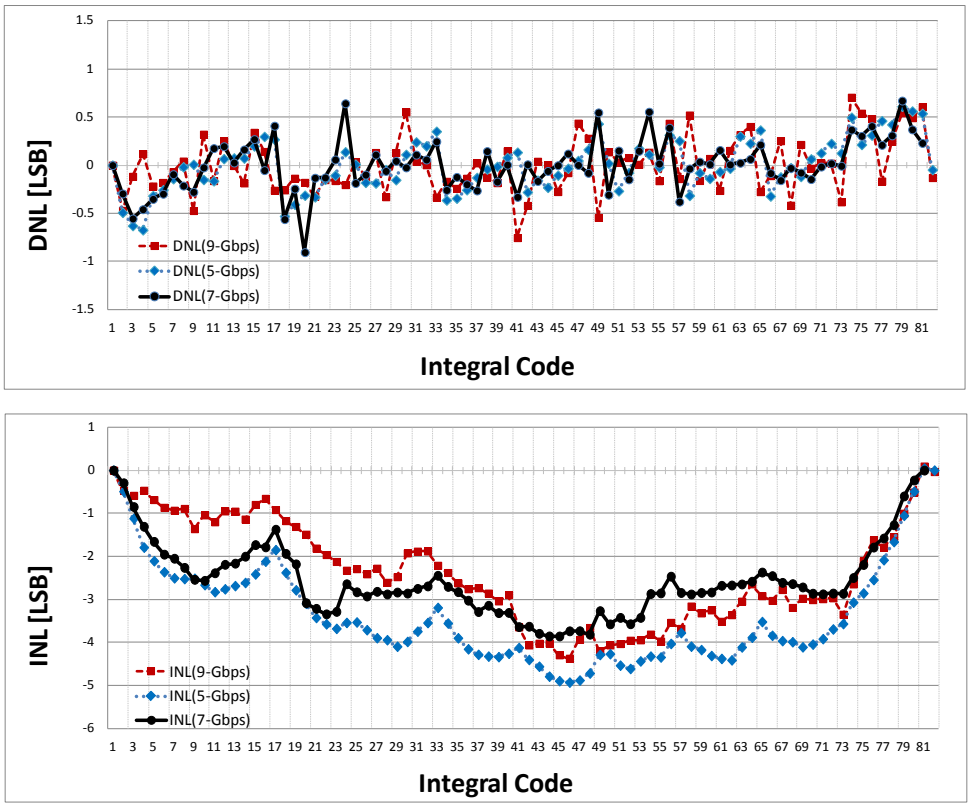


Fig. 4.15 Measurement of multiphase linearity at 2.5-GHz, 3.5-GHz, and 4.5-GHz. : (a) DNL and (b) INL.

Various channels, such as Nelco4000-6 microstrips and RG58-coaxial cables, are used to verify functions of the chip. The Nelco4000-6 microstrips are contained in an Agilent J-BERT N4903A serial bit-error-ratio tester. Fig. 4.16 shows the measured frequency response of these channels, for which s-parameters are measured by an Agilent ENA Network Analyzer E5071C. The nine-inch Nelco4000-6 microstrip has the lowest loss, at about -10 dB at 4.5 GHz. At the same frequency, the 8-m RG58 cable and 28-inch Nelco4000-6 microstrip show a loss of -22 dB. The proposed linear equalizer achieves a gain of over 20-dB at 7 Gb/s. However, the loss of SMA connectors and package requires a gain of more than 20-

dB at 9 Gb/s. Therefore, an eye opening at 9 Gb/s can only be achieved in the nine-inch Nelco4000-6 microstrip.

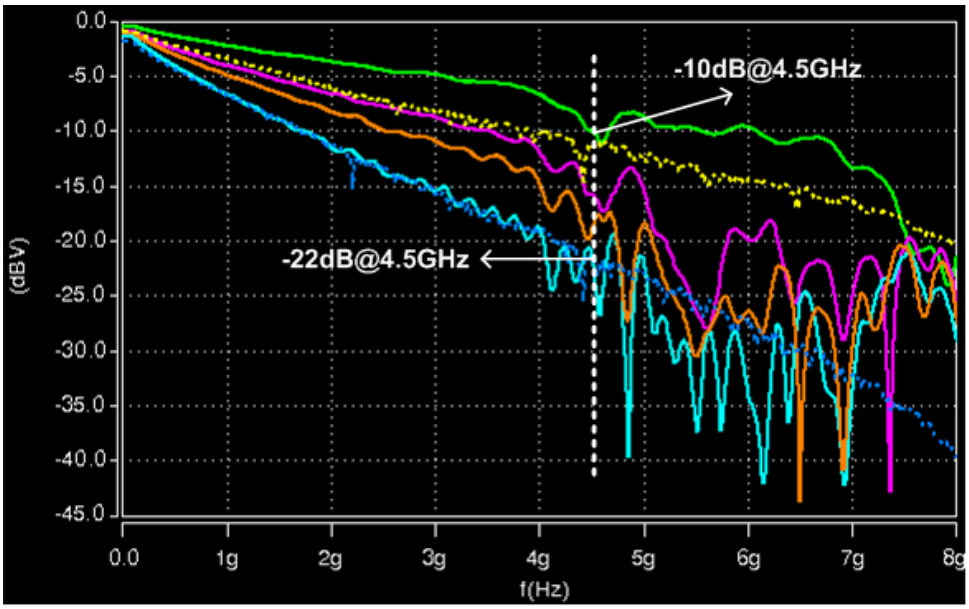
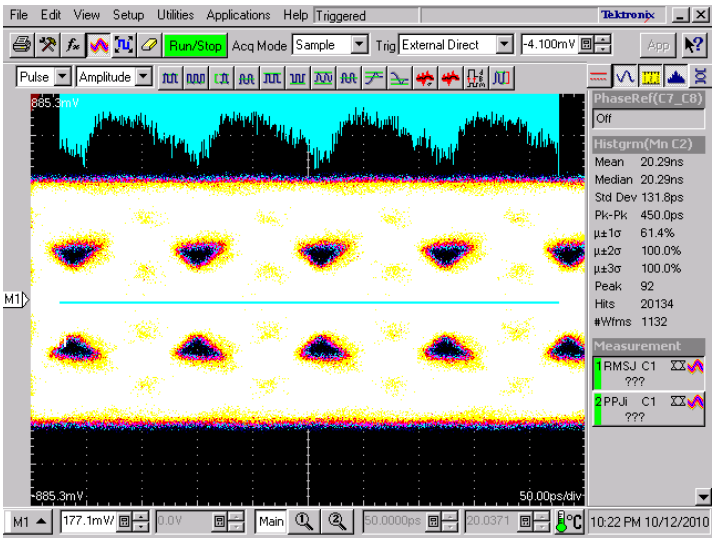
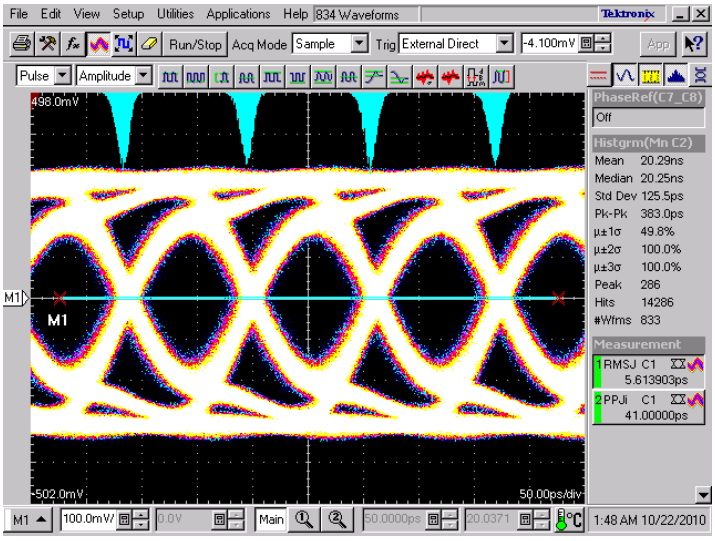


Fig. 4.16 Measured frequency response (s-parameter) of Nelco 4000-6 9-inch, 16-inch, 20-inch and 28-inch microstrips (solid-line), and RG58 5-m and 8-m coaxial cables (dotted-line).

Figures from 4.17 to 4.21 show the measured differential waveforms under various data rates and channels when the 2^{12}-1 PRBS pattern is injected. The left side of each figure is the eye diagram of the uncompensated channel output, and the right side is the eye diagram after compensation by the adapted CTLE. All equalization results are measured at the maximum possible data rate to achieve an eye opening of more than 0.5 UI with a supply voltage of 1.35 V. As shown in Fig. 4.17, the maximum data-rate with the nine-inch Nelco4000-6 microstrip, which has the lowest loss, is 9 Gb/s.



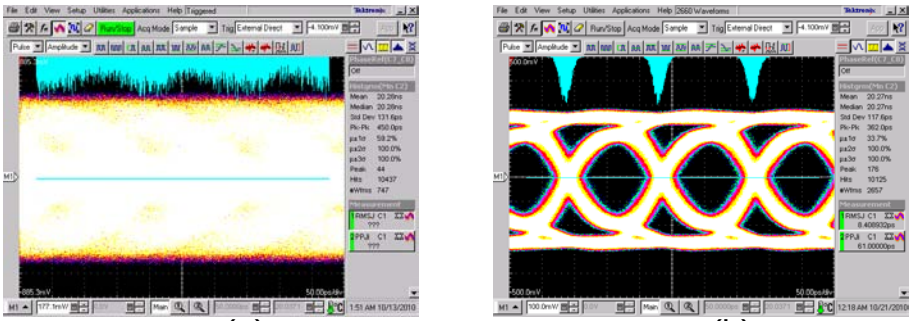
(a)



(b)

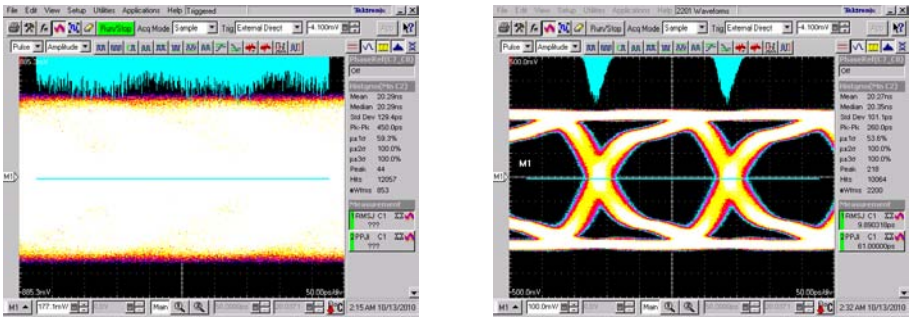
Fig. 4.17 Eye diagram comparison between (a) channel output of the 9-inch Nelco 4000-6 and (b) output of the adapted CTLE at 9-Gbps.

For the 20-inch and the 28-inch microstrips, the maximum data-rates are 7 Gb/s and 5 Gb/s, respectively, as shown in Fig. 4.18 and Fig. 4.19. With these channels, the eye diagram of the channel output is completely closed due to the channel loss.



(a) (b)

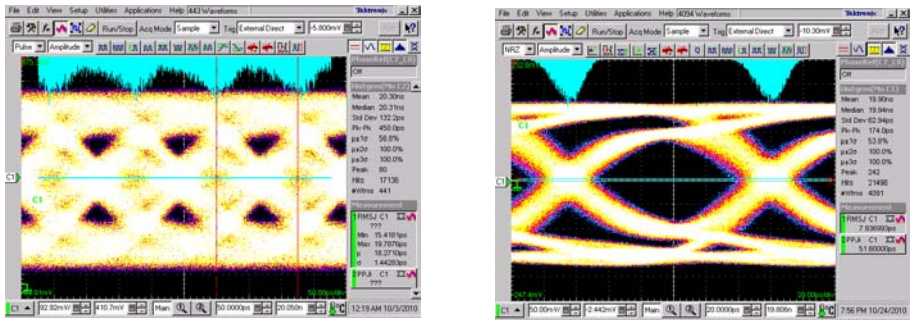
Fig. 4.18 Eye diagram comparison between (a) channel output of the 20-inch Nelco 4000-6 and (b) output of the adapted CTLE at 7-Gbps.



(a) (b)

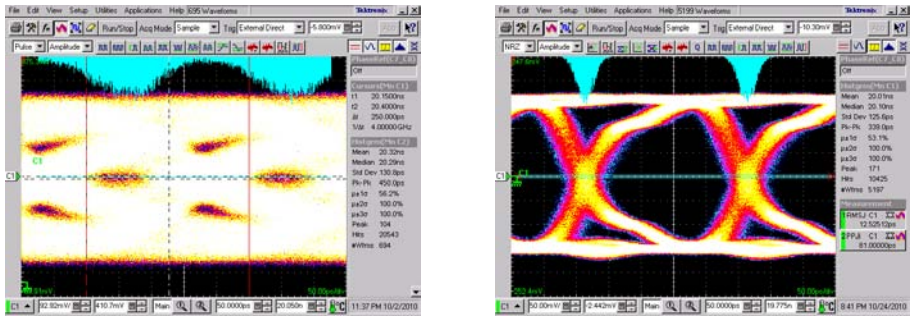
Fig. 4.19 Eye diagram comparison between (a) channel output of the 28-inch Nelco 4000-6 and (b) output of the adapted CTLE at 5-Gbps.

The eye openings with microstrip channels are relatively small compared to those of coaxial cables with the same amount of loss, as shown in Fig. 4.20 and Fig. 4.21. Due to the many stubs on the PCB, the impedance discontinuity distorts the signal waveforms.



(a) (b)

Fig. 4.20 Eye diagram comparison between (a) channel output of the 5-meter RG58 and (b) output of the adapted CTLE at 8-Gbps.



(a) (b)

Fig. 4.21 Eye diagram comparison between (a) channel output of the 8-meter RG58 and (b) output of the adapted CTLE at 4-Gbps.

Because the waveforms from Fig. 4.17 to Fig. 4.21 are at the outputs of the driver, exploiting inductive peaking, the eye openings are not identical to the results at the equalizer output. Therefore, the BER is measured at every 0.01-UI step of the sampling phase over 1 UI. Fig. 4.22 shows the bathtub curve measured under various conditions of the channel. In comparison with the waveform in Fig. 4.18, its eye opening is remarkably consistent with the bathtub curve of the 20-inch Nelco4000-6 microstrip at 7 Gb/s. As previously mentioned, the eye openings are more than 0.5 UI in most conditions. However, the error-free span at 9 Gb/s is about 0.42 UI, unlike the waveform in Fig. 4.17.

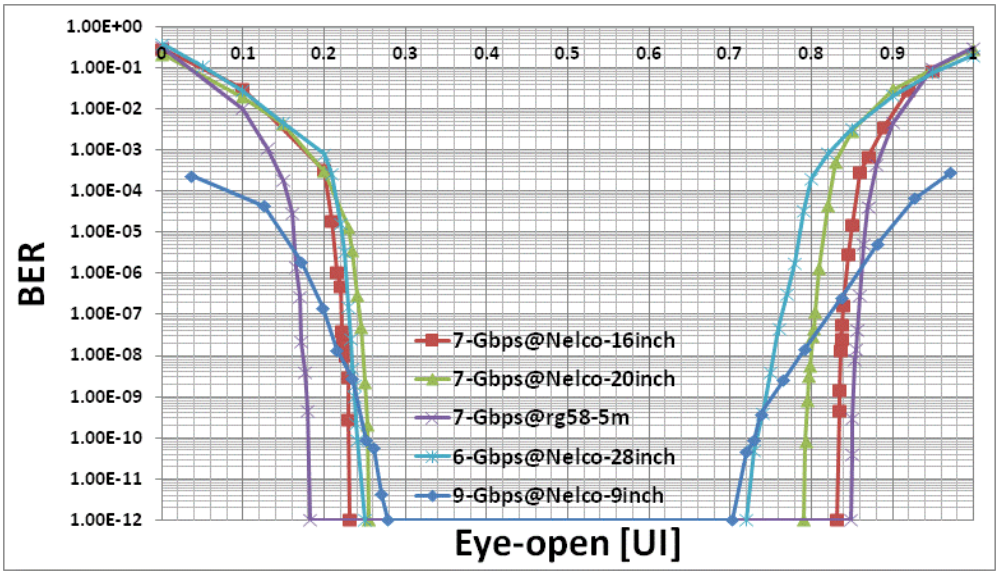


Fig. 4.22 Measurement results of bathtub curves.

This outcome is due to nonlinearity of the multiphase clocks and the limited timing margin of the logic gates. Also, the phase spacing between two half-rate

clocks greatly diverges from 1 UI at 9 Gb/s such that the BER in the vicinity of data transition is lower than the others.

Process	90nm CMOS
Circuits	Forwarded-clock receiver
Max. Speed	9 Gb/s @ 1.35 V
Eye Opening at 10^{-12} BER	w/o CTLE: closed w/ CTLE: over 0.50 UI at 4~7 Gb/s, over 0.42 UI at 9 Gb/s
Power Consumption at 7 Gb/s, 1.35V	Total: 125.8 mW Data lane: 69.8 mW Clock lane and Multiphase generator:56 mW
Chip Area	Total: 670 μm × 670 μm Data lane: 330 μm × 460 μm Clock lane and Multiphase generator: 330 μm × 670 μm

Table 4-I. MEASURED PERFORMANCE

	Blocks	Power (%)
Data Lane	CTLE	11.5
	Sampler	3.9
	Analog Buffers(CML)	8.5
	2:64 Deserializer	21.5
	Eye-Monitoring Driver	51.0
	Bias & Etc.	3.7
Clock Lane	CTLE	13.2
	Sampler	2.2
	Analog Buffers(CML)	9.8
	DLL Core	19.5
	Clock Distribution & Digital Buffer	51.1
	Bias & Etc.	4.2

Table 4-II. POWER BREAKDOWN FOR 7Gb/s

The measured performance is summarized in Table 4-I. The highest data rate to achieve an eye opening of more than 0.42 UI is 9 Gb/s. The total power consumption of the fabricated chip at a data rate of 7 Gb/s is 125.8 mW at a supply voltage of 1.35 V. The data lane consumes 69.8 mW and the clock lane consumes 56 mW. The major

power consumption in the data lane occurs in the CML-type buffer and the driver to monitor the equalized data. In the case of the clock lane, the digital buffers for the signal monitoring and clock distribution circuits are the dominant sources of power consumption. The simulated power breakdown for a data rate of 7 Gb/s is displayed in Table 4-II.

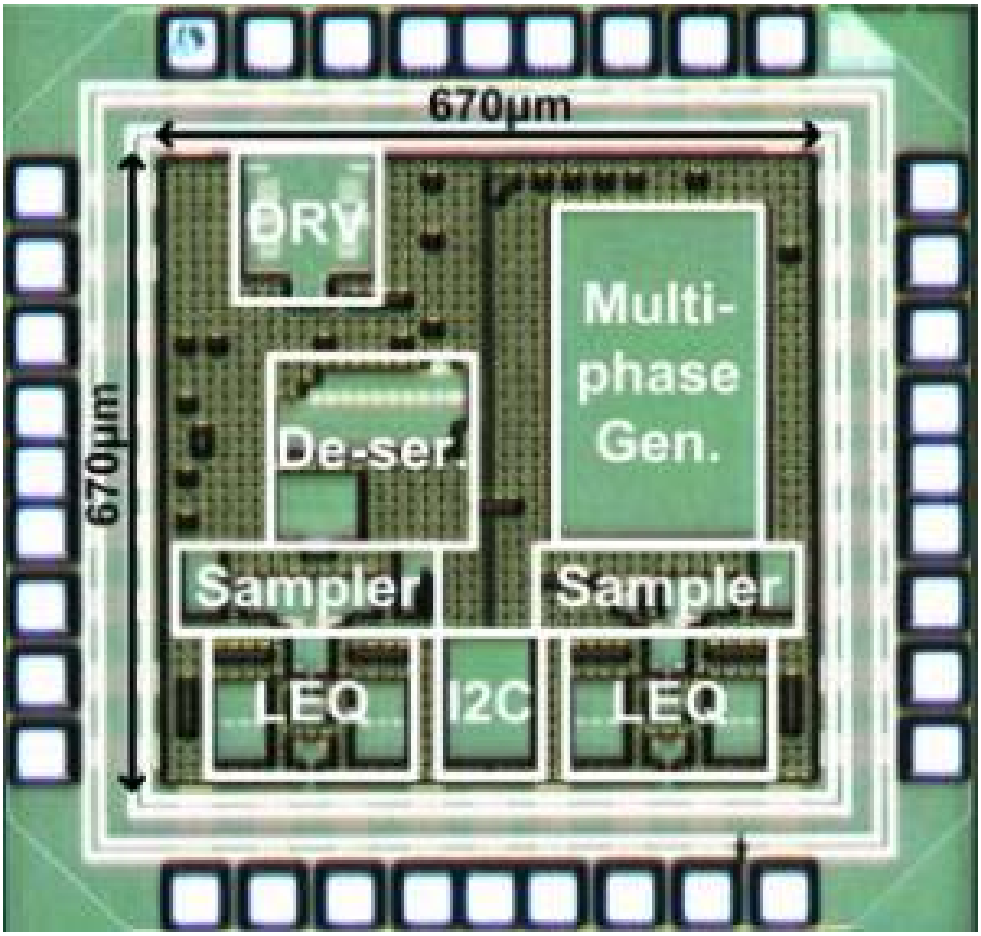


Fig. 4.23 Chip micro-photograph.

Although the complete chip area is 670 × 670 μm^2, the active chip area of the data

lane is just 330 × 460 μm^2. The core components of the data lane, which consists of a CTLE, samplers and a CML buffer, only amount to 256 × 304 μm^2. A comparison of this work with other RX architectures is shown in Table 4-III. Our work outperforms those in terms of power and the area per single data lane. A chip microphotograph is shown in Fig. 4.23.

	JSSC-09 [11]	ISSCC-06 [8]	This work
Architecture	CDR with ref. clock	Embedded clock	Forwarded clock
Technology (CMOS)	130 nm	90 nm	90 nm
Supply voltage	1.45 V	1.2 V	1.35 V
Scalable	5 Gb/s	20 Gb/s	4 ~ 9 Gb/s
Clock generation	PLL+DLL+PI	PLL+DLL+PI	DLL+PI
Rx power (Single lane)	450 mW (46.07 mW)	NA	125.8 mW (69.8 mW)
Single lane area	400,000 um^2	341,640 um^2	448,900 um^2
Core components	Sampler+ MDLL+DLL+DCC+CDR	CTLE+ Sampler+CDR	**CTLE+ Sampler**
Core area	102,235 um^2	256,230 um^2	**77,824 um^2**
Core area Density	20,447 um^2/Gb/s	12,812 um^2/Gb/s	**8,647 um^2/Gb/s**

Table 4-III. PERFORMANCE COMPARISON

Chapter 5

Conclusion

In this thesis, two multichannel receivers which focus on collaboration and a sharing technique among channels are presented. Despite the growing demand for higher data transmission rates, I/O speeds are saturated and the advance of suggested alternatives is slow, resulting in an acceleration of an increase in the number of channels. With the increased number of channels, collaboration among channels, such as sharing information about noise, skew, and channel loss, will be very helpful to improve the jitter tracking ability, channel-loss compensation, and loop-linearity. Moreover, a circuit-sharing technique for common functions such as skew calibration, offset cancellation, and equalizer adaptation will reduce the hardware complexity and simplify each lane, thus maximizing lane-expandability while lowering the design cost.

Specifically, in case of the first multichannel receiver, a simple yet effective collaboration technique to linearize the binary PD transfer characteristics of a 2×-oversampling CDR has been proposed, and the effect of different latencies between the integral and proportional paths in the collaborative timing recovery architecture

has been analyzed. With the proposed linearization technique, a CDR with binary phase detectors can realize constant and linear loop dynamics largely independent of the jitter conditions, while only requiring hardware complexity equivalent to a conventional 2×-oversampling CDR.

The second proposed receiver has adopted the DLL-based type of forwarded-clock architecture while sharing the global calibration logic among the lanes for common functions. With the global calibration logic, the data lane of the proposed architecture consists of only a CTLE, a sampler and a deserializer, thereby improving the channel expandability. To achieve high bandwidth for the DLL, a dual-interpolating delay cell is used, while a weight-adjustment technique is used with the delay line in order to reduce the number of dummy delay cells in the DLL.

The first and the second chip were respectively fabricated in the 45-nm and the 90-nm CMOS process, and the corresponding maximum data rates per lane were 6 Gb/s (PAM-4) and 9 Gb/s (PAM-2). The loop bandwidth of the first PLL-based multichannel receiver under various jitter conditions was relatively constant at 7.3 MHz due to its PD linearization technique while consuming 2.98 mW of power per gigabit. The second DLL-based receiver had a very slim data lane due to the shared global calibration logic, resulting in a low core-area density of 8,647-μm^2/Gb/s while occupying a total area of 670x670 μm^2. In conclusion, the two proposed techniques leading to the design of a multichannel receiver will solve problems such as high hardware complexity and a large area caused by the increased number of channels and will enable the design of highly cost-efficient receivers.

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초록

본 논문에서는 고속 디지털 통신을 위한 두 가지 방식의 다중채널 수신기를 제안하였다. 기존의 다중채널 수신기는 여러 채널을 통해 데이터 전송시의 손실되는 신호의 양, 송신기에서 발생하는 잡음 등의 더 많은 정보를 수신기에 전달하지만 각 채널 별로 반복되는 회로를 사용하여 많은 면적과 전력을 소모한다. 다중채널 수신기의 이러한 장점을 최대한 활용하기 위해 채널간의 협동에 초점을 맞춘 수신기와 단점을 최소화 하기 위해 채널간의 공유에 초점을 맞춘 수신기가 각각 제안되었다.

첫 번째 수신기는 전송되는 데이터의 위상정보를 채널간의 협력을 통하여 복원하는 구조를 채택하였으며, 각 채널의 면적과 전력소모를 줄이기 위해 2 진화 위상 검출기를 사용하였을 경우 발생하는 비선형특성을 개선하기 위해 위상 검출기에 고의적인 위상오차를 주는 방식을 사용하였다. 이러한 방식의 위상검출은 기존의 2x 다중샘플링 방식과 동일한 하드웨어를 요구하지만 선형성의 개선으로 인하여 전체 클록 및 데이터 복원 회로의 루프특성을 지터에 상관없이 일정하게 만들어 준다.

두 번째 수신기는 채널간의 공통적으로 처리할 수 있는 등화기의 적응, 오프셋 제거, 위상 잠금 등의 과정을 하나의 디지털 회로로 처리하여 각 채널에 대응하는 회로를 단순화하는 방법을 사용하였다. 우수한 지터 추적성능을 위해 송신기에서 데이터와 함께 동기화된 클록 또한 전달해주는 구조를 사용하였으며, 보정시간 동안 약속된 데이터를 사용하여 공통된 함수를 기존의 2x 다중샘플링 방식의 절반에 해당하는 하드웨어로 처리하였다. 이러한 방식을 통해 수신기의 채널 확장성을 높였으며, 높은 데이터 전송 속도를 보장하였다.

수신기들은 45-nm 과 90-nm 의 CMOS 공정에서 구현되었으며, 각각 6-Gb/s 와 9-Gb/s 의 전송속도를 갖는다. 첫 번째 수신기의 위상검출기 선형화기술은 다양한 외부 입력 지터에서 7.3-MHz 의 동일한 대역폭을 유지시켜주며, 두 번째 수신기의 채널간에 공통 회로 공유 기술은 채널의

구조를 매우 단순화하여 수신기의 전송속도 당 차지하는 면적을 8,647 μm^2/Gb/s 으로 줄여준다. 이러한 기술들은 다중채널 수신기의 비용 효율을 높여줄 것으로 예상한다.

주요어: Multichannel receiver, forwarded clock, collaborative timing recovery, clock and data recovery, bang-bang phase detector, linearization technique, phase-locked loop (PLL), delay-locked loop (DLL)

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