PH.D. DISSERTATION

A LOW-POWER DATA INTERFACE CIRCUIT AND ANALOG DATA CONVERTER FOR BIOMEDICAL DEVICE

생체의학용 장치를 위한
저전력 데이터 인터페이스 회로 및
아날로그 데이터 변환기

BY

SUNKWON KIM

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DEPARTMENT OF ELECTRICAL ENGINEERING AND
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지도교수 김 수 환

이 논문을 공학박사 학위논문으로 제출함

2013년 02월

서울대학교 대학원

전기컴퓨터 공학부

김 선 권

김선권의 공학박사 학위논문을 인준함

2013년 02월

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ABSTRACT

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In this study, a low-power referenceless clock and data recovery (CDR) circuit and cyclic analog data converters (ADC) were implemented and verified by standard CMOS technology for biomedical systems.

A Biomedical system performs signal acquisition, amplification, filtering and also undertakes quantization and neural stimulation. It needs to be small in size and power-efficient. First of all, the heat in proportion to power consumption generated by the circuit must be considered, in order to avoid the possibility of tissue damage. The battery size can be reduced by low power consumption in a battery-powered biomedical system. Also the biomedical system should small for improving bio-compatibility.

In this study, a low-power referenceless CDR is designed and validated in 0.18μm

standard CMOS technology. It adopts clock-edge modulation and a voltage-controlled oscillator based on a relaxation oscillator. Our CDR has an input data-rate of 200kbps to 10Mbps when the supply voltage is 0.7V, and operates at up to 24MHz with a supply voltage of 1.0V. The bit error-rate of our CDR is lower than 10^{-13}. The energy per bit is only 0.8pJ/bit, even though the circuit is implemented in a 0.18μm CMOS technology.

The demand for low-power low-voltage analog-to-digital converters (ADCs) for biomedical systems has recently grown dramatically. Among several ADC architectures, the cyclic ADC achieves high resolution with small chip area and low power, because it performs a conversion cyclically by repeated use of a single gain stage.

Our first prototype which is a 10-bit cyclic ADC adopts the comparator-based switched-capacitor (CBSC) technique, for the first time, so as to compensate for the technology scaling and to reduce power consumption by eliminating the need for high gain op-amps. A boosted preset voltage is also introduced to improve the conversion rate without consuming more power. The ADC operates at 2.5MS/s, and near the Nyquist-rate, the prototype has a signal-to-noise and distortion ratio (SNDR) of 55.99 dB and a spurious-free dynamic-range (SFDR) of 66.85 dB. The chip was fabricated in 0.18μm CMOS and it has an active area of $0.146mm^2$ and consumes 0.74mW from a 1.8V supply.

A proposed second cyclic ADC which has a 12-bit resolution with CBSC adopts the multi-level input tracking boosted preset voltage scheme, asynchronous clocking scheme and adjustable threshold voltage in the comparator. The multi-level input tracking preset voltages scheme can achieve shorter coarse conversion time than the conventional one.

Moreover, by reusing the sub-ADC in the MDAC, the proposed input tracking preset voltages scheme does not needed additional circuits. An asynchronous clocking scheme only synchronizes the sampling signal. After the end of the conversion time, sleep mode is maintained until the next signal of sample and helps reduce the power consumption because the current source and comparator are power down. The scheme of adjustable threshold voltage in the comparator reduces the coarse conversion time. Moreover, the overshoot is reduced which means that the fine conversion time is also shortened. The ADC operates at 3MS/s, and near the Nyquist-rate, the simulation results show a signal-to-noise and distortion ratio (SNDR) of 64.9dB and a spurious-free dynamic-range (SFDR) of 69.7dB. The chip was designed in 0.18μm CMOS and it has an area of $0.23mm^2$ and consumes 1.6mW from a 1.8V supply.

Keywords: biomedical system, clock and data recovery circuit, cyclic analog data converter, comparator-based switched-capacitor.

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CHAPTER 1

INTRODUCTION

1.1 INTEGRATED NEURAL INTERFACE

Recently, integrated neural interface systems are progressing dynamically and play an important role in modern medical treatments. There is a demand for an integrated neural interface system that treats neurological disorders and helps to understand neuroscience. The integrated neural interface performs signal acquisition, amplification, and filtering; and also undertakes quantization and neural stimulation.

The neural stimulation interface is used for stimulating the neurons in order to deliver some particular type of sensory information to the brain or to mimic a particular neurological function. The neural recording interface is used for real-time sampling and processing of large-scale brain or bio-potential signals.

As shown Fig 1.1.1, a closed-loop neural interface system contains a neural recording path, a neural stimulation path and microelectrodes arrays [1.1.1]. The neural stimulation can treat neurological disorders such as epilepsy, depression, and Parkinson's disease. And a neural recording system can diagnose diseases and help to understand neuroscience. The microelectrodes arrays which should be small to minimize tissue

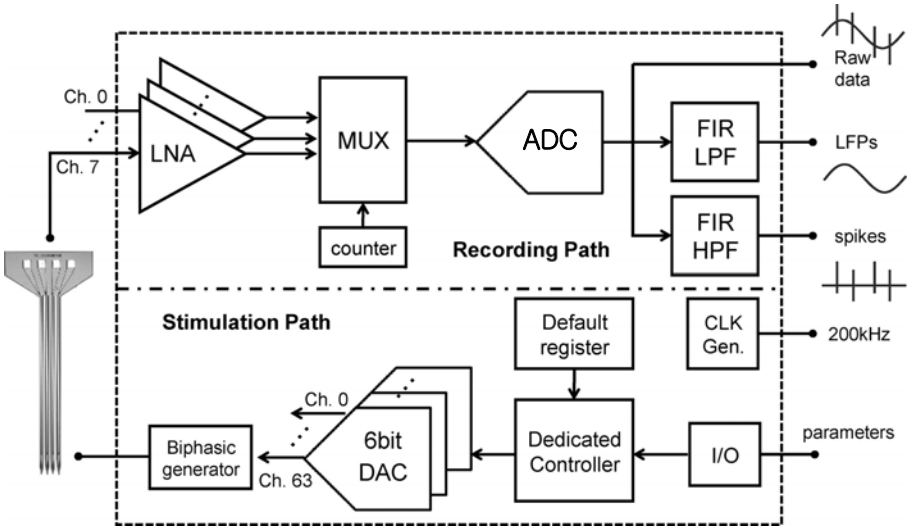


Fig. 1.1.1 Block diagram of the stimulation path and recording path [1.1.1].

damage and chemically inert are used for simultaneous stimulation and recording at multiple site.

1.1.1 MULTI-CHANNEL NEURAL RECORDING INTERFACE

Figure 1.1.2 shows the general architecture of the multi-channel neural recording system. The total number of channels is N and the total number of ADCs is M resulting in a multiplexing ratio of 2^{n-m} [1.1.4]. To reduce the area, the multi-channel neural recording interface using an analog multiplexer and an ADC is implemented as shown in Fig.1.1.3.

1.1.2 MULTI-CHANNEL NEURAL STIMULATION INTERFACE

A 64-channel current-steering DAC and parameter controller generate biphasic stimulation patterns in the stimulation path as shown in Fig. 1.1.1. To stimulate the neurons throughout the MEA simultaneously, an I/O interface with high transfer rate such as clock and data interface circuit is needed. Because of the limited port number and telemetry method, serialized CDR is widely used in biomedical applications. The CDR has the highest frequency signal and clock in the whole chip. Therefore, the CDR circuit is one of the most power-consuming blocks.

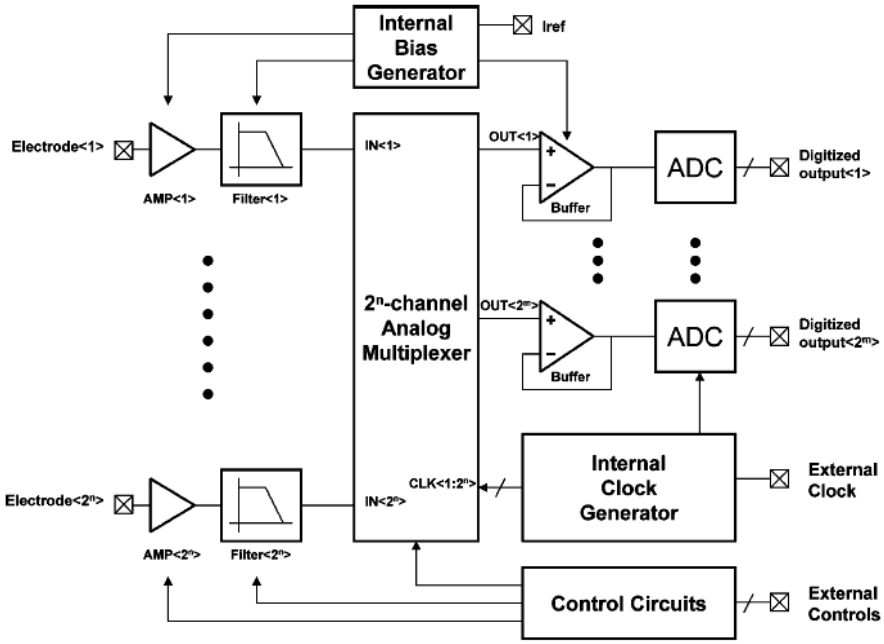


Fig. 1.1.2 The architecture of the multi-channel neural recording system [1.1.4].

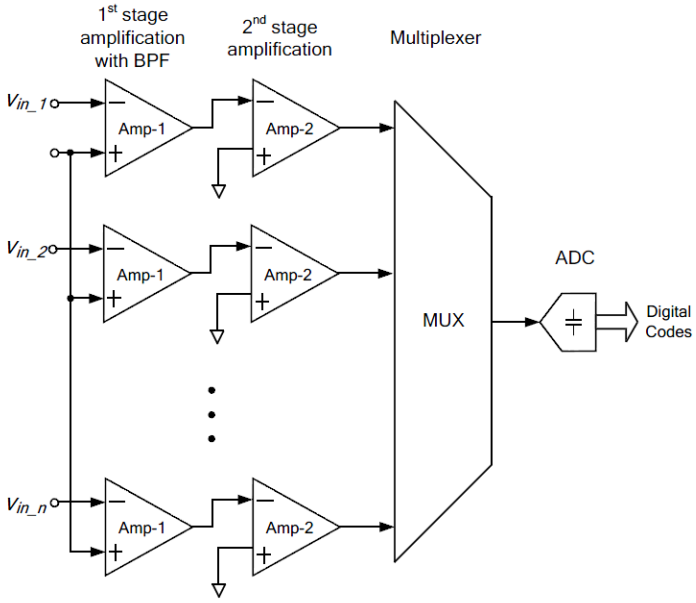


Fig. 1.1.3 The architecture of the multi-channel neural recording system with multiplexing signal using an ADC [1.1.5].

1.2 DESIGN CONSIDERATION FOR NEURAL INTERFACE

1.2.1 BIO-POTENTIAL SIGNALS

Bio-potential signals are generated due to the electrochemical activity of certain class of cells that are components of the nervous, muscular or glandular tissue. Electrically, these cells exhibit a resting potential, and when they are stimulated they generate an action potential. Bio-potential signals refer to the actions potentials from a single cell or to the average activity from groups of cells. Figure 1.1.4 shows the frequency and amplitude characteristics of most commonly recorded bio-potential signals [1.1.6].

Electroencephalogram (EEG), electrocorticogram (ECoG), and local field potentials (LFP) refer to the recording of electrical activity of the brain created by a group of neurons. The naming indicates the invasiveness of the recording. The EEG recording is the least invasive of all. It uses surface electrodes that are attached to the tissue of the skull, whereas, the electrodes for ECoG measurements are placed directly on the surface of the brain, beneath the skull.

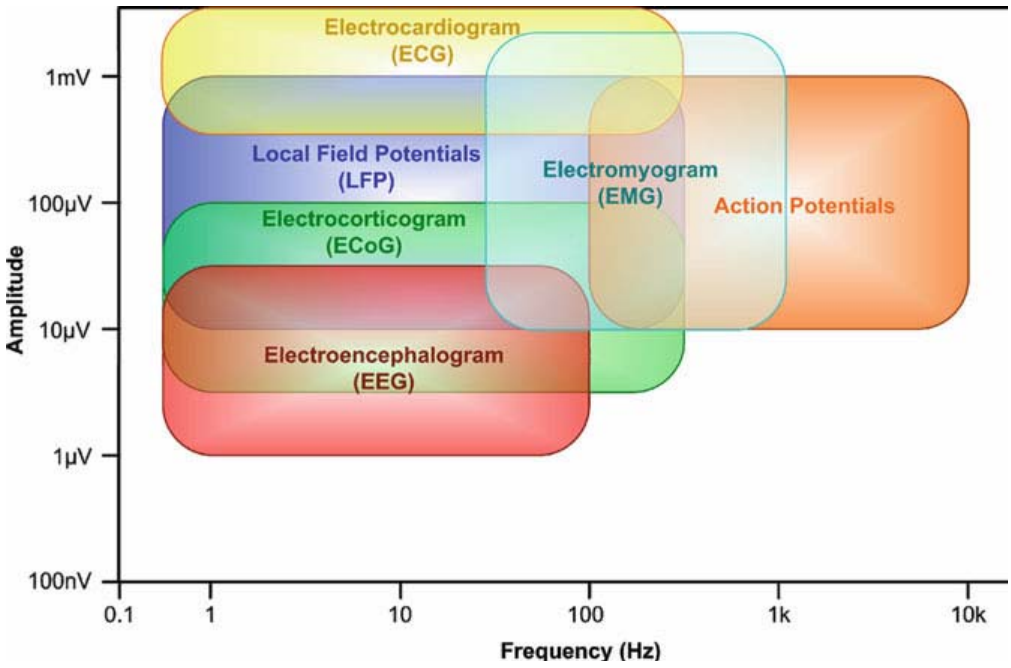


Fig. 1.1.4 Amplitude and frequency characteristics of bio-potential signals [1.1.6].

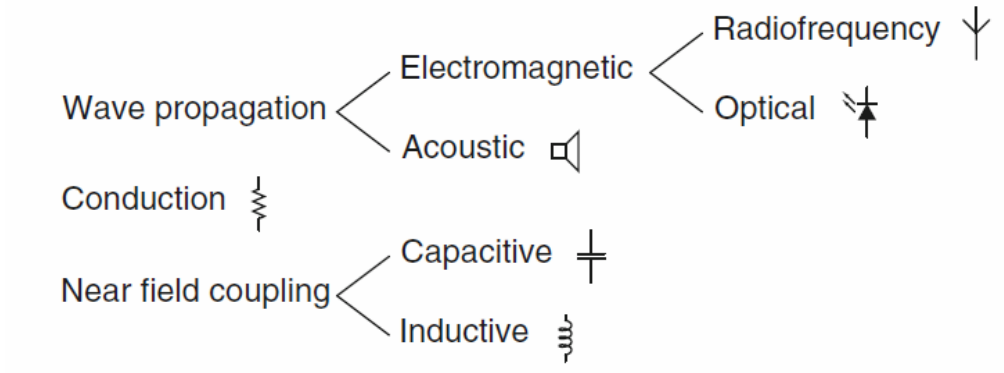


Fig. 1.1.5 Biomedical telemetry methods [1.1.7].

1.2.2 BIOMEDICAL TELEMETRY

Based on the physical connection between the biomedical implant transmitter and the external receiver, wireless communication can be divided into three classes: wave propagation, electrical conduction and near-field coupling [1.1.7], as seen Fig. 1.1.5.

1.2.2.1 Wave Propagation (optical and RF)

Optical wave communication uses (visible or IR) light as a carrier. For RF waves near or far-field antennas are required, whereas for optical communication light emitting and sensitive devices are used, such as photodiodes and phototransistors. The major advantage of optical data transmission is the extreme robustness against electromagnetic interference (EMI).

Common EU accepted bands for wireless RF communication in biotelemetry are the MICS band [66] (402–405 MHz) and the ISM band (433.05 MHz, 868 MHz and 2.4 GHz)

1.2.2.2 Near field coupling (capacitive and inductive)

A capacitive link is not used for biotelemetry applications until 2009 [1.1.8]. Inductive near-field links are the most widely used communication technique for biomedical implants. They offer the advantage of simultaneously supplying energy and providing a carrier for bi-directional communication. Induction telemetry however has a fairly small range, compared to RF, ultrasound and optical telemetry.

1.2.3 Design Consideration for Data interface and ADC for Neural Interface

The integrated neural interface system needs to be especially small and power-efficient. The heat in proportion to power consumption generated by the circuit must be 0considered, in order to avoid the possibility of tissue damage. It has been suggested that the power to area ratio should not exceed 80mW/cm^2 [1.1.9].

The signal of action potentials has the highest frequency in bio-potential signals. To record the 100 sites of action potentials signals, the conversion rate of an ADC should be higher than 2MS/s according to the Nyquist theorem. The resolution of the ADC is required to be 8 to 12 bits in biomedical applications.

SAR ADCs have been considered to have the most power efficient architecture for such conversion rates. However, the input capacitances of SAR ADCs are typically large due to the design consideration of mismatch requirement. Hence, the proceeding stages, such as variable gain amplifiers or filters, need to provide high driving capability. In terms of the overall system, power reduction in such ADCs might lead to the cost of excessive power consumption in the other circuit blocks. Due to the large capacitance required in an SAR ADC, the silicon area is significantly large [1.1.10].

An optically controlled neural interface system which is extremely robust against electromagnetic interference uses the optical diode. To receive both external clock and

data, separated optical diodes are needed. To make it worse, the wavelength of the external clock must be different from the wavelength of the optical data to avoid crosstalk. Therefore, a referenceless clock and data recovery circuit is suitable for optically controlled neural interface systems.

In this study, a referenceless clock and data recovery and low-power cyclic ADCs are presented to satisfy these design considerations.

1.3 THESIS ORGANIZATION

The organization of this thesis consists of two main topics, which are the clock and data interface and the analog-to-digital converters for neural interface system. Two main chapters include already published journal paper or conference proceeding [1.1.11-1.1.13]. In chapter 2, the referenceless clock and data recovery circuit for optically controlled neural interface system is presented. In chapter 3, two proposed cyclic analog to digital converters are presented. Finally, conclusions and summary of this dissertation are presented in chapter 4.

CHAPTER 2

DATA AND CLOCK INTERFACE CIRCUITS FOR NEURAL INTERFACE

2.1 REFERENCELESS CLOCK AND DATA RECOVERY CIRCUIT FOR OPTICALLY CONTROLLED NEURAL INTERFACE SYSTEM[†]

2.1.1 INTRODUCTION

Neural interface system as a biomedical system performs signal acquisition, amplification, and filtering; and also undertakes quantization and neural stimulation [2.1.1], [2.1.2]. It needs to be specially small and power-efficient, while supporting data transfer rates in the tens of Mbps [2.1.3], [2.1.4]. In such a system, the serial data interface and associated clock circuit must operate at the highest frequency of any component in the whole die. This requires a lot of power; thus the heat generated by the circuit must be considered, in order to avoid the possibility of tissue damage. It has been

[†] This sub chapter is published *proceeding of International Symposium on Low Power Electronics and Design (ISLPED'*11, **Best paper Award***)* [1.1.12]. And it is accepted for publication in *IEEE transactions on circuits and system-II* [1.1.11]. The author of the thesis is first author of the published papers.

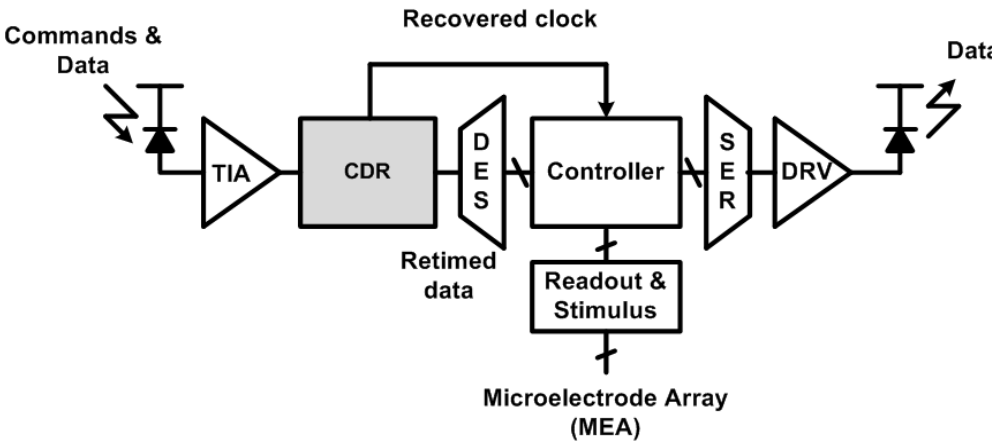


Fig. 2.1.1 Block diagram of optically controlled neural interface system.

suggested that the power to area ratio should not exceed 80mW/cm^2 [2.1.5]. There are obvious drawbacks to battery-powered implants, including size and bio-compatibility issues. The data is usually transmitted by RF telemetry. But high data-rates are not achievable by RF links due to the potential for interference from and with other devices. In a development designed to address this problem, a system receives data by free-space optics. For example, [2.1.6] includes a low-power clock and data recovery circuit (CDR), which consumes 217nW at a 3b4b encoded input data-rate of 200kbps.

However, a more flexible CDR that is able to lock over a wide range of data-rates (typically 45kbps – 200kbps) requires an expensive external clock to be provided by a separated optical diode. To make it worse, the wavelength of this external clock must be different to the wavelength of the optical data to avoid crosstalk.

Fig. 2.1.1 is a block diagram of an optically controlled neural interface system consisting of a TIA, a CDR, a controller, a driver, and readout and stimulus circuits. It

can read out neural signals and stimulate neurons through microelectrode array (MEA). The data and commands of our system are optically transmitted at high-data rate.

In this paper, we focus on the CDR circuit itself since it is one of the most power-consuming blocks. Our CDR does not need an external reference clock and achieves 0.8pJ/bit of energy per bit even though the circuit is implemented in a 0.18μm CMOS technology.

The rest of this chapter is organized as follows: in Section 2.1.2, we introduce the optically controlled referenceless CDR and the addressed mechanism of our clock-edge modulation, and the design of each block. Section 2.1.3 provides details of circuit implementation. In Section 2.1.4, we present experimental results obtained from the new CDR, and summary is drawn in Section 2.1.5.

2.1.2 CDR ARCHITECTURE

Research on CDRs for chip-to-chip transfer has mainly been focused on performance issues such as input data-rate, jitter and jitter tolerance [2.1.7]. However, a simpler CDR with lower power consumption that supports lower data-rates cannot be obtained by scaling high-performance designs. In a wireless biomedical application, whether communication is RF or optical, the design of a synchronous CDR must take into account crosstalk between the data and the clock. A synchronous CDR is an expensive part of an optical system, because it requires optics for several wavelengths, together with

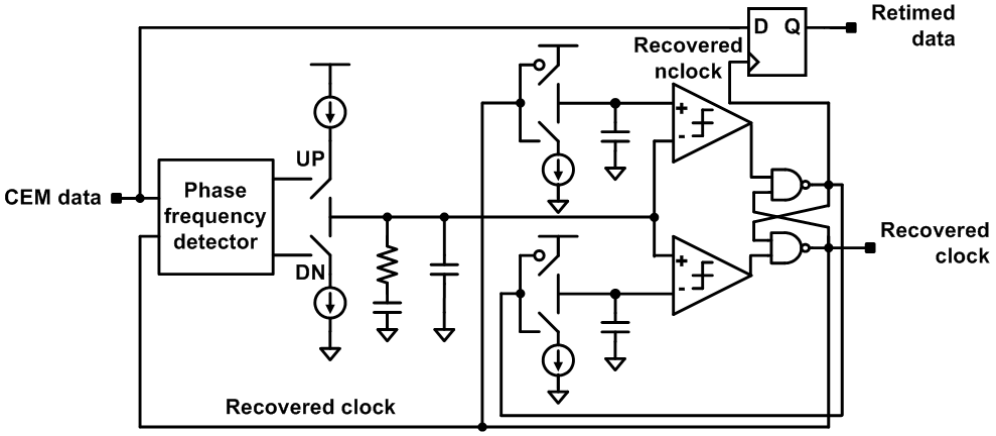


Fig. 2.1.2 Block diagram of the proposed referenceless CDR.

band-pass filters. Thus, a referenceless CDR [2.1.8]-[2.1.11] is more appropriate for this application.

The designs of CDR that do not have a reference clock require a complicated frequency detection circuit, which consumes a lot of power and area. An alternative is the clock-embedded CDR with additional voltage levels, which extracts the clock signal using information embedded in the data-stream itself. This approach simplifies clock recovery without introducing the possibility of harmonic locking, which suggests that it should be suitable for pad-limited design. However, this clock-embedded CDR, which extracts data information by means of additional voltage levels [2.1.10], makes it unsuitable for our application because of the limited dynamic range of a photodiode. The alternative is a clock-edge modulation (CEM) technique which can extract data information from clock signal by repositioning the clock edge [2.1.11].

We propose a low-power referenceless CDR architecture that achieves clock-edge

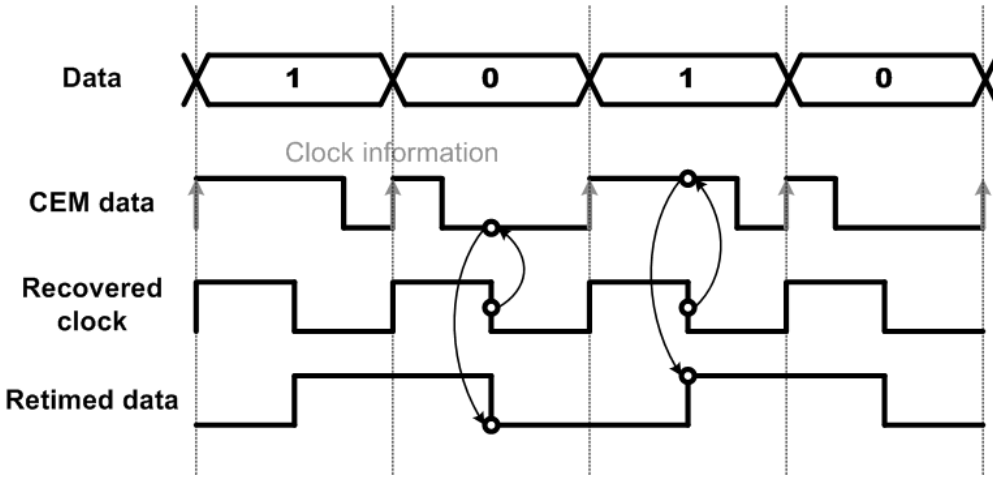


Fig. 2.1.3 Timing diagram of clock-edge modulation.

modulation with a single phase. As shown in Fig. 2.1.2, a clock recovery loop and sampling flip-flop triggered by falling edge are used to generate the clock and data. The clock recovery loop is based on a phase-locked loop (PLL) with a phase frequency detector (PFD), which is easily implemented due to the presence of CEM input signal.

Fig. 2.1.3 shows the timing diagram of the clock-edge modulation. The positive edges of the input signal contain both period and phase information. The negative edges of the input signal are related to a single bit of data. The PFD only extracts clock information for the positive edges of the input signal, and compares the recovered clock with this CEM input signal. The UP / DN signals from the PFD identify the leading and lagging phases of the recovered clock, and these signals are sent to the charge pump (CP). Then the voltage from the CP changes the period of the relaxation oscillator. Thus, the lead or lag between the input signal and the recovered clock determines the period and phase of the oscillator. This allows the recovered clock signal to be locked without

placing any limit on the run-length of the clock information. In the locked state, accurate data are obtained in quite a simply way, by sampling the input signal at the falling edge of the internal clock in the locked state. If the positions of a falling edge for 0 or 1 respectively are within 75% and 25% of the period, then the CDR keeps the jitter of the recovered clock signal below 0.25UI.

2.1.3 CIRCUIT IMPLEMENTATION

2.1.3.1 Phase and frequency detector

The PFD compares two input signals in terms of both phase and frequency [2.1.12]. The output is a pulse proportional to the phase difference between the inputs, and this output drives the charge pump to adjust the control voltage of the VCO. The phase characteristic of the PFD is important, as it is linked to jitter in the PLL. If the PFD fails to detect the phase error when it is within the dead zone, which is the undetectable phase difference range, then the PLL will lock to an incorrect phase [2.1.13].

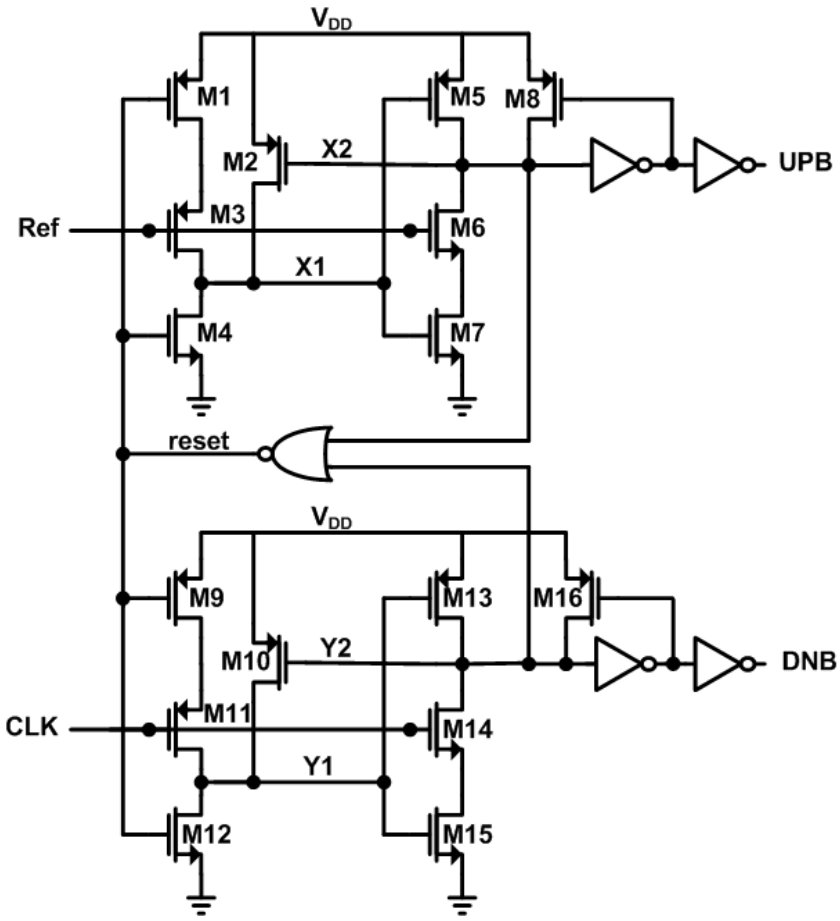


Fig. 2.1.4 Schematic diagram of phase and frequency detector.

We adopt a PFD with a reset pulse which has a reduced dead zone. The reset pulse applied to the PFD reduces the jitter arising from up and down current mismatch in the charge pump when it is operating at low voltage. The simple feedback keeper technique improves the noise immunity of the PFD. In our design, the keeper transistors also reduce the power requirement of the PFD and increase its speed. Fig. 2.1.4 shows our PFD design, in which the dead zone is effectively reduced by the gate and asynchronous delays.

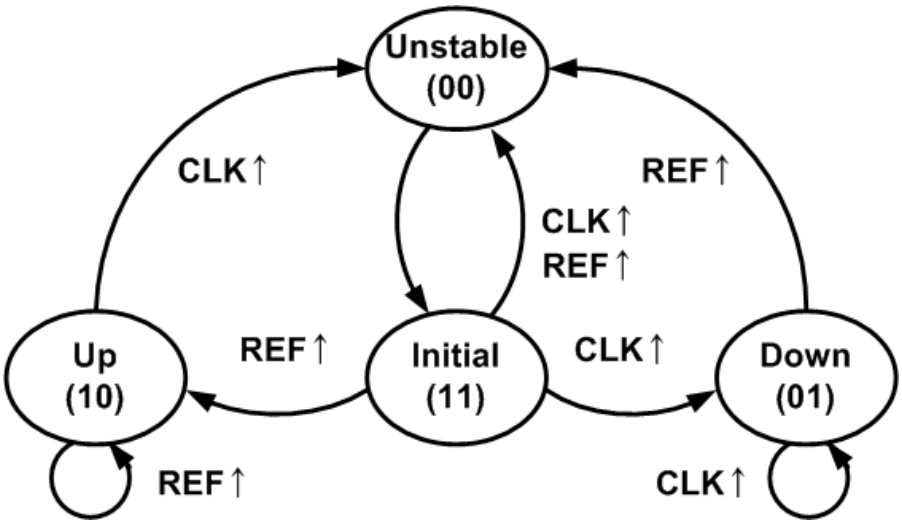


Fig. 2.1.5 Finite-state diagram of the PFD.

Fig. 2.1.5 shows a finite-state diagram of its four possible states, in which each state transition is annotated with the corresponding transition condition, which is basically the rising transition of the REF or CLK signals, denoted by REF↑ and CLK↑ respectively. Let us assume that UPB and DNB are both high (state = 11) initially, while REF and CLK are low. Then a rising edge of REF will drive UPB low, and a rising edge of CLK will drive DNB low. When both UPB and DNB are low, the circuit is reset, returning UPB and DNB to high. State 00 is unstable in Fig. 2.1.5. In this state, reset will turn on M4 and M12, nodes X1 and Y1 are discharged accordingly, and nodes X2 and Y2 will be charged to high through M5 and M13 respectively. This returns the circuit to state 11, in which the keepers M8 and M16 precharge nodes X2 and Y2 respectively, so as to stabilize dynamic nodes X2 and Y2, especially when the voltage is low.

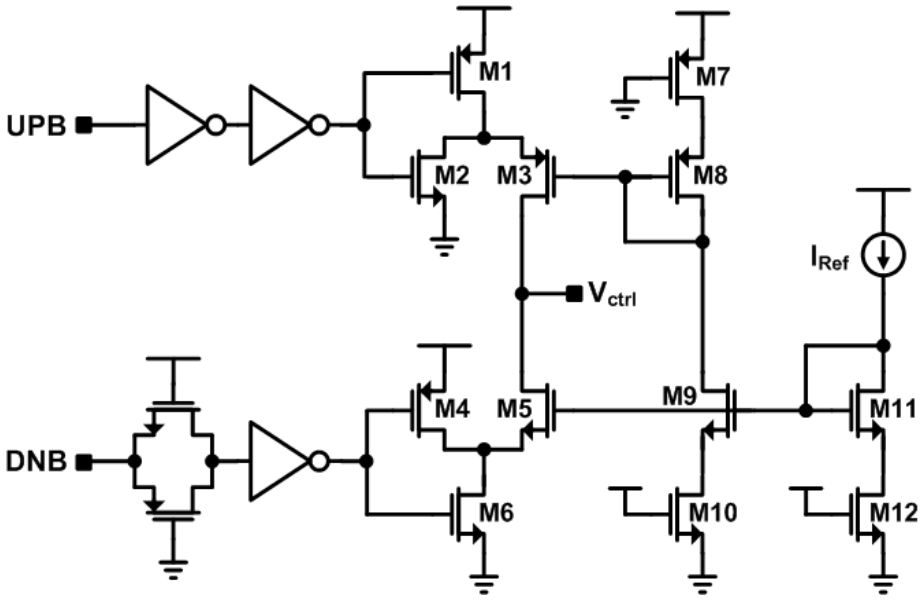


Fig. 2.1.6 Schematic diagram of the charge pump.

Fig. 2.1.6 is a schematic diagram of the charge-pump circuit, which has a single-ended source-switched architecture. The voltage V_{ctrl} is determined by switches M1 and M6, which respectively control outputs UPB and DNB of the PFD. Switches M2 and M4 are included to minimize the current mismatch due to charge-sharing. To improve the accuracy of current-mirroring, dummy switches are used in the bias branches.

2.1.3.2 Voltage controlled relaxation oscillator

The quartz crystal oscillators are large and consume a lot of power. Therefore, the ring or relaxation oscillators are preferable for implanted biomedical devices. Ring

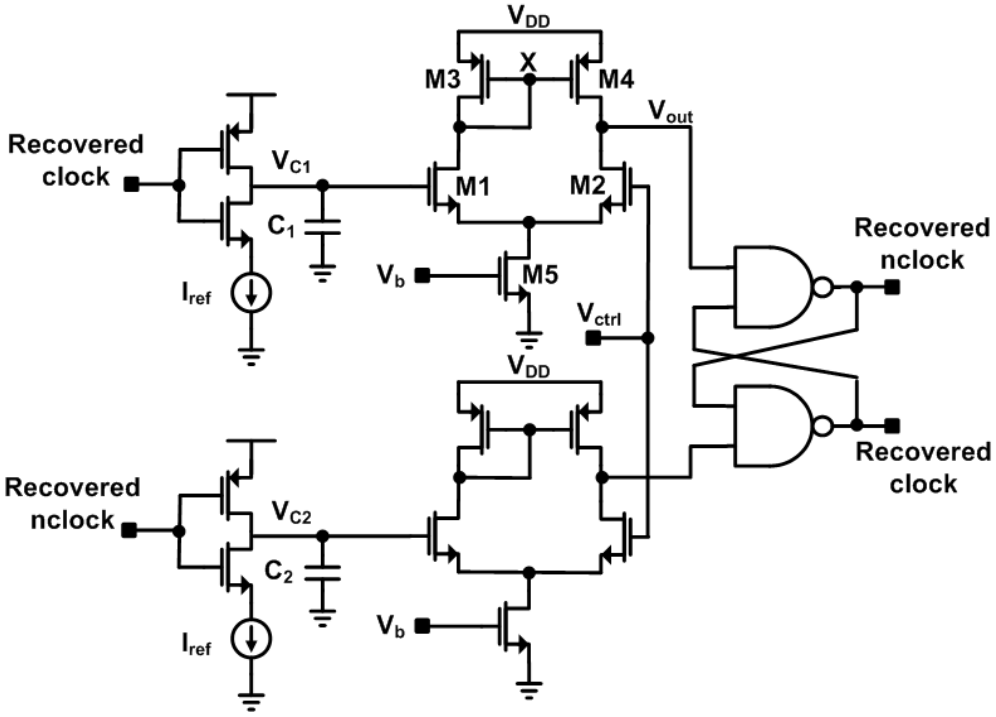


Fig. 2.1.7 Schematic diagram of our voltage controlled relaxation oscillator.

oscillators are commonly able to cope with higher frequencies and consume more power than that of relaxation oscillators [2.1.14]. However, relaxation oscillators have two more advantages over ring oscillators: they have a constant frequency tuning gain; and their phase can be read out continuously due to their triangular (or sawtooth) waveform [2.1.15]. The period of a relaxation oscillator is determined in a well-defined manner, at a modest cost in power and silicon area. We therefore, adopt a relaxation oscillator for our VCO, as shown in Fig. 2.1.7. A relaxation oscillator produces a constant frequency by charging and discharging capacitors between two fixed voltages. The VCO in our CDR has a constant charge voltage and a controllable discharge voltage. The VCO consists of a

constant-current source I_{ref} which is controlled by the recovered clock signal, and two comparators that compare the voltages on capacitors V_{C1} and V_{C2} with the control voltage V_{ctrl}. A set-reset (SR) latch receives the output voltages from the two comparators and the output of the latch provides feedback that turns the constant-current source on and off. As shown in Fig. 2.1.7, C_1 and C_2 are alternately charged to V_{DD}, controlled by the state of the SR latch, and then discharged to V_{ctrl} by I_{ref}. The triangular waveforms of V_{C1} and V_{C2} form one period of the clock. The length T_{OSC} of this period is determined as follows:

$$T_{OSC} = \frac{2C(V_{DD} - V_{ctrl})}{I_{ref}} \tag{2.1.1}$$

where I_{ref} is a constant current, V_{ctrl} is the control voltage, and $C = C_1 = C_2$. According to equation (2.1.1), mismatches of two I_{ref} and capacitors can affect the duty cycle of recovered clock. The VCO gain (K_{VCO}) is 83MHz/V.

At the normal operating voltage V_{DD}, symmetry requires that $V_{out} = V_X$. If V_{C1} or V_{C2} is much more positive than V_{ctrl}, then M4 operates in its deep triode region, carrying zero current. Thus, $V_{out} = V_{DD}$. As V_{C1} or V_{C2} approaches V_{ctrl}, M1 turns on, drawing part of I_{D5} from M3 and turning M4 on. The output voltage then depends on the difference between I_{D4} and I_{D2}. As V_{DD} drops, so do V_X and V_{out}, with a slope close to unity. As V_X and V_{out} fall below V_{ctrl}-V_{THN}, M1 and M2 enter their triode regions, but their drain currents are constant if M5 is saturated. A further decrease in V_{DD}, and hence in V_X and V_{out}, causes V_{GS1} and V_{GS2} to increase, eventually driving M5 into the triode region.

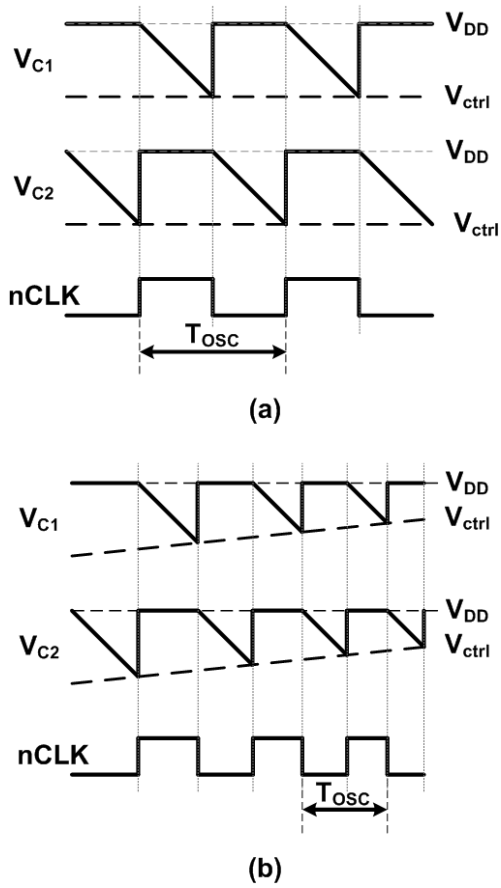


Fig. 2.1.8 Timing diagrams of (a) the lock state and (b) the lag state.

Thereafter, the bias current of all of the transistors drops, lowering the rate at which V_{out} decreases to the logic threshold. In our design, the logic threshold of the latch is lowered to operate at a low supply voltage. Thus, the UP / DN signals are determined by the lead or lag of the phase at the output of the PFD. This modifies V_{ctrl}, and the frequency of the relaxation oscillator is adjusted to align the phases, as shown in Fig. 2.1.8.

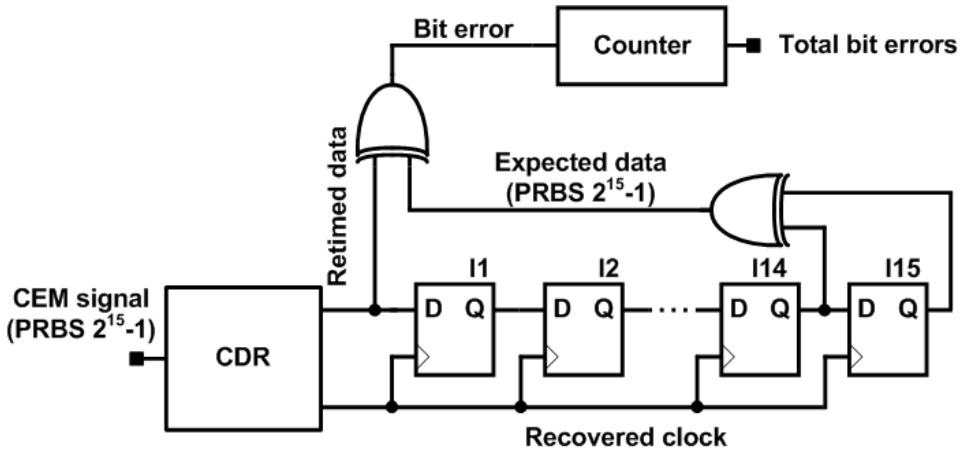


Fig. 2.1.9 Schematic diagram of the BER test circuit.

2.1.3.3 Bit error-rate (BER) test circuit

To verify the functionality of our CDR and establish its BER, the test circuit shown in Fig. 2.1.9 which generates pseudo-random binary sequences (PRBS) of length 2^{15}-1, was embedded in a DUT. The same known data pattern is sent to the CDR circuit. The feedback polynomial of the PRBS has terms with powers of 14 and 15. The retimed and expected data are compared to generate a bit error signal, and the BER can be calculated from this signal and the running time.

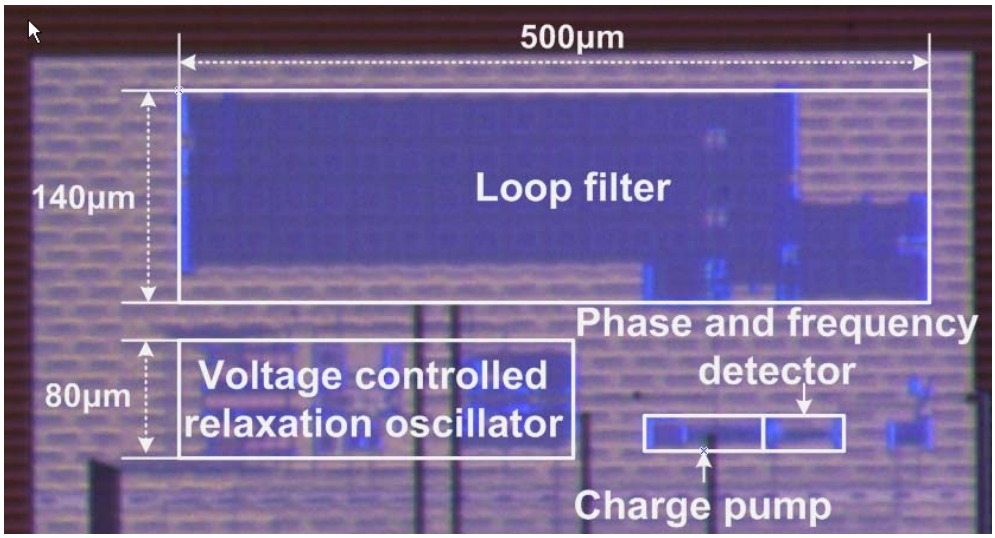
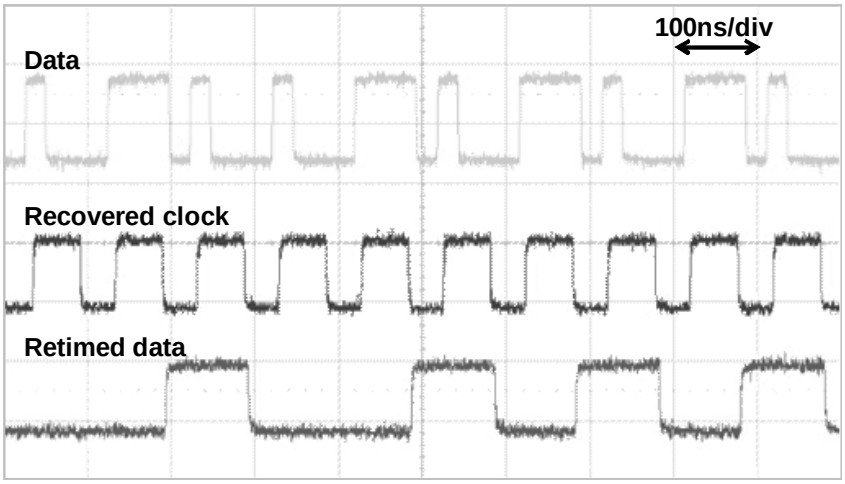


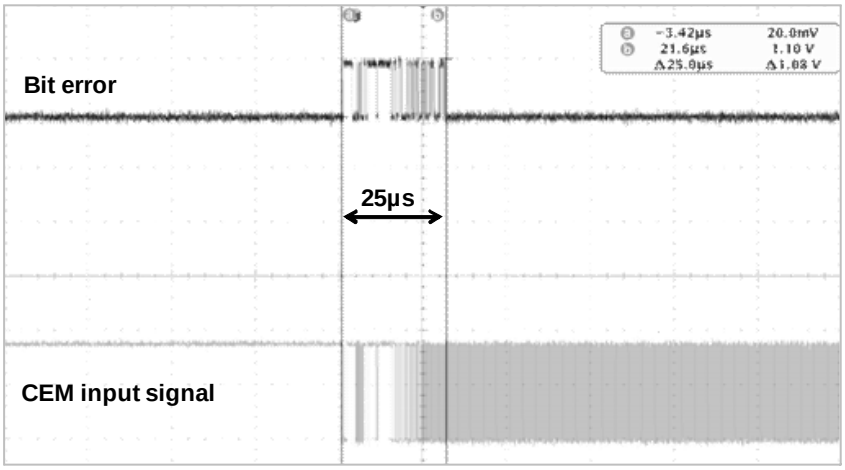
Fig. 2.1.10 Die photo.

2.1.4 EXPERIMENTAL RESULTS

The proposed CDR was implemented using a 0.18μm process. Fig. 2.1.10 shows the die photograph. The loop filter, which occupies most of the die area, is a second-order RC filter for stability. The core area is 0.09mm^2, including some test circuitry.



(a)



(b)

Fig. 2.1.11 Measured waveforms of (a) the recovered clock and retimed data, and (b) the settling time.

Fig. 2.1.11(a) is a screenshot of the oscilloscope when the supply voltage is 0.7V and the input data-rate is 10MHz. The input pattern is '1001010', which is part of a 2^{15}-1 PRBS. The bit error signal indicates that the CDR is not yet ready. As shown in Fig.

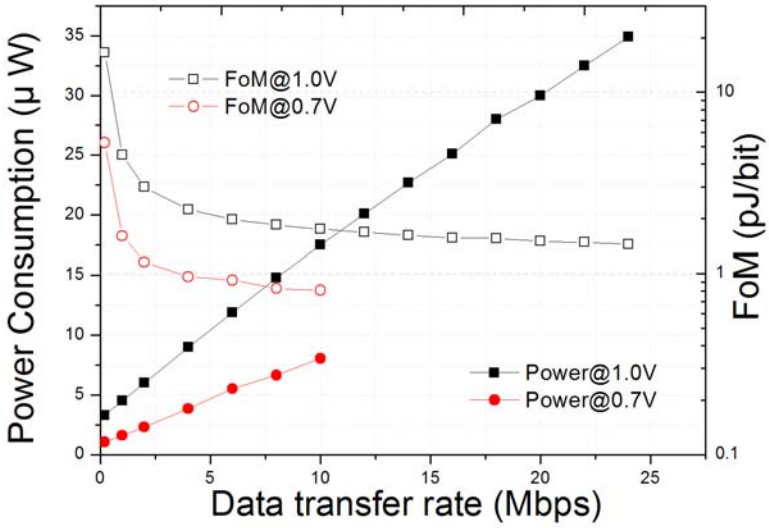
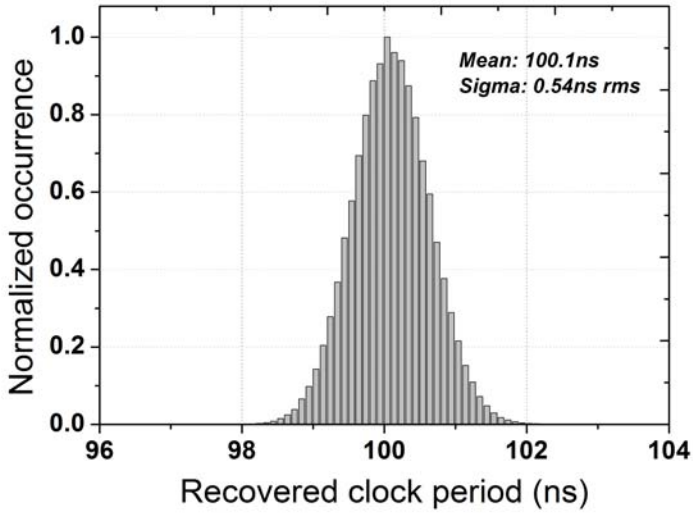


Fig. 2.1.12 Measured data transfer rate vs. power consumption and FoM.

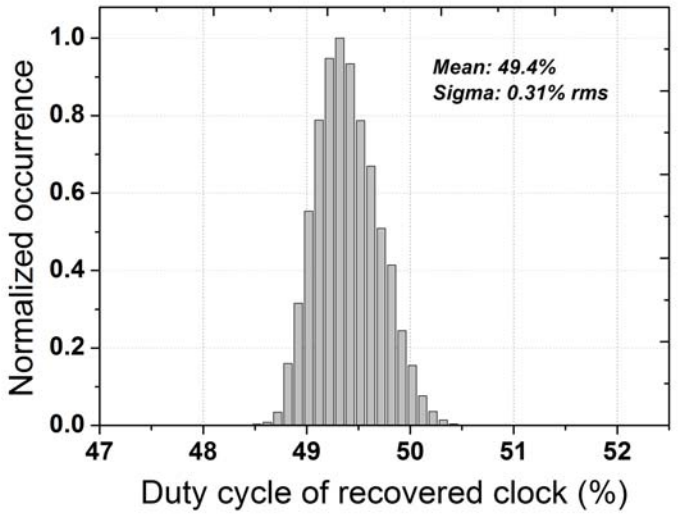
2.1.11(b), our CDR has a settling time of 25μs.

Fig. 2.1.12 is a plot of power consumption and a figure of merit (FoM) versus data transfer rate. This FoM is the ratio of power consumption to data transfer rate. Our CDR supports input data-rates from 200kbps to 10Mbps at a supply voltage of 0.7V, consumes 8μW at an input data-rate of 10Mbps, and its FoM is 0.8pJ/bit.

Since the chip area is 0.09mm^2, we have a power to area ratio of about 8.8mW/cm^2, which is almost an order of magnitude less than the critical heat flux threshold for implants of 80mW/cm^2 [2.1.5]. When the supply voltage is 1.0V, normal operation allows data-rates from 200Kbps to 24Mbps. We measured the power consumption using an input pattern which produces the maximum number of transitions.



(a)



(b)

Fig. 2.1.13 Measured histogram of (a) the recovered clock period and (b) duty cycle of recovered clock

Table 2.1.1 Comparison with other reported CDSs

	VLSI'09[2.1.16]	ISSCC'10[2.1.6]*	This work
Process	0.18μm	90nm	0.18μm
Design	Demodulator	CDR	CDR
Data rate	250kbps	200kbps	10Mbps
Vdd	0.7V	0.3V	0.7V
Power	21μW	217nW	8.05μW
FoM	84pJ/bit	1pJ/bit	0.8pJ/bit

** 3b4b coding and reference clock*

Fig. 2.1.13(a) and (b) show a histogram of measurements of the recovered clock period of 100ns and duty cycle respectively. The standard deviation in recovered clock period is 0.54ns and in duty cycle is 0.31%. During a 32-hour test, no error bits were detected, suggesting that the bit error rate (BER) is lower than 10^{-13}. The data-rate was 10Mbps, and the circuit was operating with a supply voltage of 0.7V and a 2^{15}-1 PRBS input pattern. Measured parameters for this CDR are compared with those of previous devices in Table 2.1.1. Our CDR uses the least energy at 0.8pJ/bit, and achieves the highest data-rate, which is 10Mbps at a supply voltage of 0.7V.

2.1.5 SUMMARY

We designed and experimentally validated an 8μW, 10Mbps referenceless CDR circuit with clock-edge modulation for biomedical system, which operates at a supply voltage of 0.7V. This design obviates the need for an external reference clock but is not subject to harmonic locking. A voltage-controlled oscillator based on a relaxation oscillator is used to reduce power consumption.

Our CDR has an input data-rate of between 200kbps and 10Mbps when the supply voltage is 0.7V, and operates at up to 24MHz with a supply voltage of 1.0V. The bit error-rate of our CDR is lower than 10^{-13}. The energy per bit is only 0.8pJ/bit, even though the circuit is implemented in a 0.18μm CMOS technology.

CHAPTER 3

ANALOG DATA CONVERTER FOR NEURAL INTERFACE SYSTEM

3.1 ANALOG DATA CONVERTER BASICS

3.1.1 BASIC OPERATIONS OF ADCS

Digital signal processing, as opposed to analog signal processing, is the preferred method in implementing large electronic systems. Digital circuits offer lower sensitivity to noise, robustness to supply and process variations, easier design and testing, and better programmability. In particular, aggressive down-scaling of IC process has allowed new generations of digital circuits to achieve higher speed, integration of more functionality on chips, low power consumption, and low cost.

Even if the digital signal processing provides a strong low-cost incentive, naturally occurring signals are analog, and human beings perceive and retain information in analog form. In order to interface digital signal processors with the analog world, data acquisition circuits such as ADCs must be used, as shown in Fig 3.1.1. Data conversion interfaces find applications in consumer electronics, portable multimedia systems, medical systems, and aerospace systems.

A number of ADC architectures such as integrating, oversampled, one-step or multi-step flash, folding and/or interpolated, pipelined, successive approximation, and cyclic or algorithmic structure have been employed depending on the speed and resolution requirements, as shown in Fig. 3.1.2.

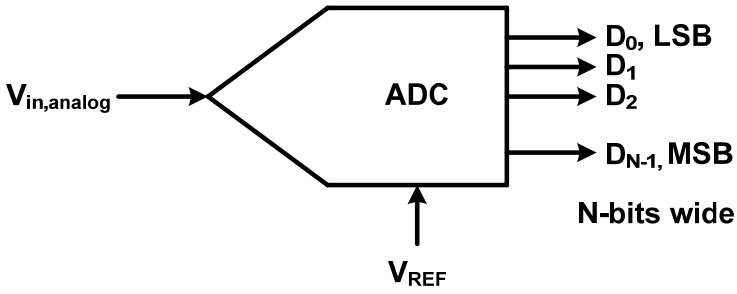


Fig. 3.1.1 Block diagram of the digital to analog converter

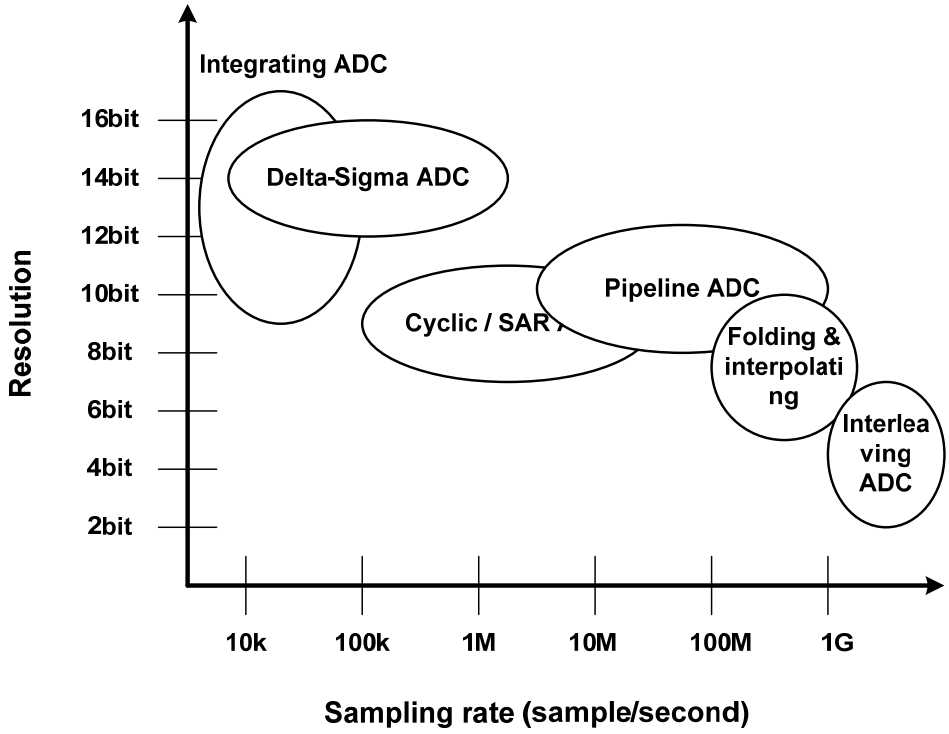


Fig. 3.1.2 Comparison of ADCs

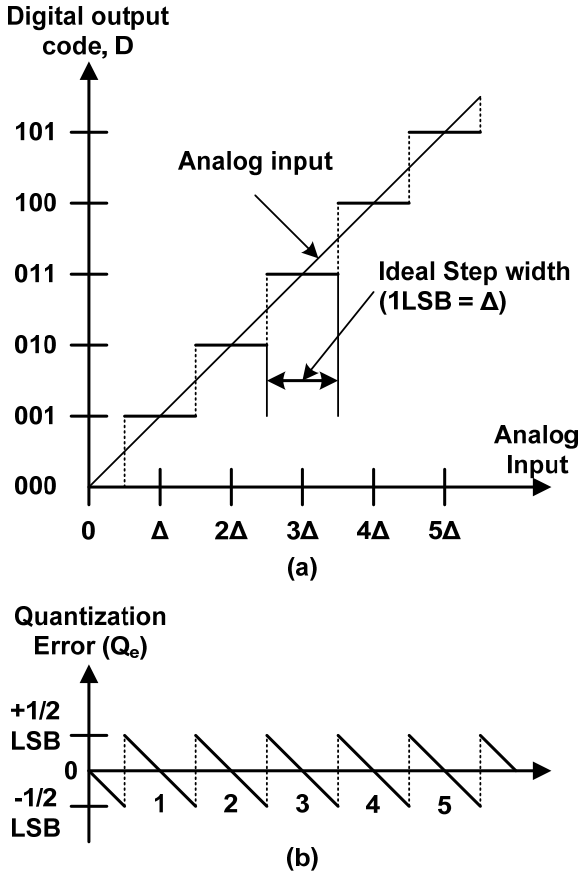


Figure 3.1.3 (a) Transfer function for an ideal ADC and
(b) its corresponding quantization error.

3.1.2 STATIC SPECIFICATIONS

The input-output transfer characteristic depicts the static behavior of a data converter. For an ideal case the input-output characteristic is a staircase with uniform steps over the entire dynamic range. Fig. 3.1.3 plots the initial part for a generic number of bits. If the first and last steps are $\Delta/2$ then the full-scale range is divided by 2^n-1 instead of 2^n to give

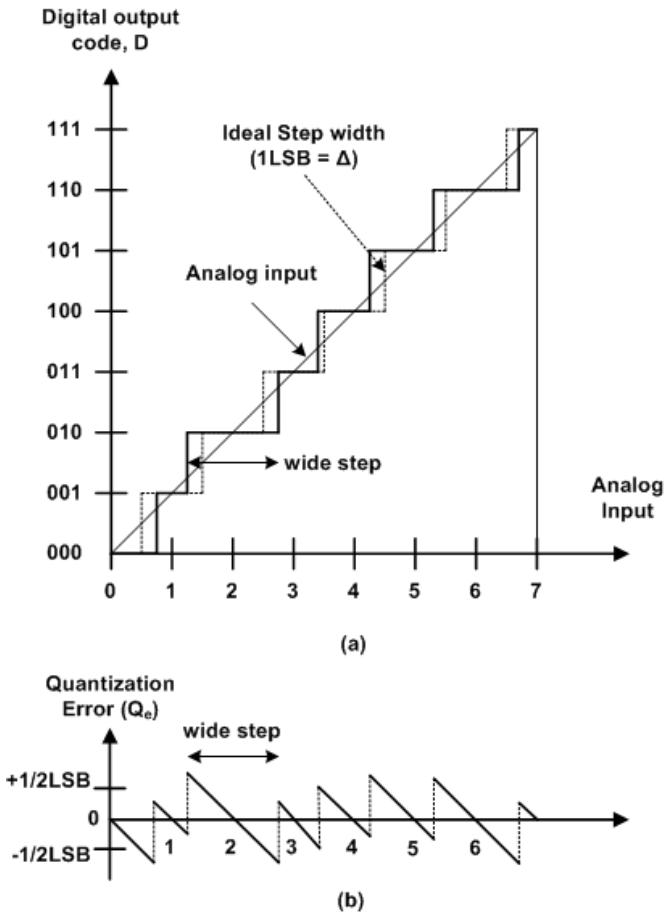


Figure 3.1.4 (a) Transfer function for an real ADC and
(b) its corresponding quantization error.

Δ. Fig. 3.1.3 outlines that a quantization interval can be encoded using both digital code or midstep point. Also, Fig. 3.1.3 shows the quantization error.

The quantization error ranges between ±Δ/2 and is equal to zero at the midstep. Deviations from the ideal transfer characteristic produce results like the ones shown in Fig. 3.1.4.

The curve of Fig. 3.1.4 (a) and (b) show an almost random variation of the quantization intervals and quantization error. There is no correlation between successive errors. The figure also shows the interpolating curve as a straight line running from the origin to the full scale. These features are quantified by the INL and DNL, two of the static specifications defined below.

3.1.2.1 Analog Resolution

This is the smallest analog increment corresponding to a 1 LSB code change. If the input signal amplitude scale is from zero to the full-scale voltage V_{FS} the ideal step corresponding to the lest significant bit of a converter is V_{LSB}

$$V_{LSB} = \frac{V_{FS}}{2^N} \tag{3.1.1}$$

3.1.2.2 Analog Input Range

This is the single ended or differential peak-to-peak signal (voltage or current) that must be applied to the A/D converter to generate a full-scale response. A peak differential signal is the difference between the two 180◦ out of phase signal terminals. Peak-to-peak differential is computed by rotating the inputs phase 180◦, taking the peak measurement again and subtracting it from the initial peak measurement.

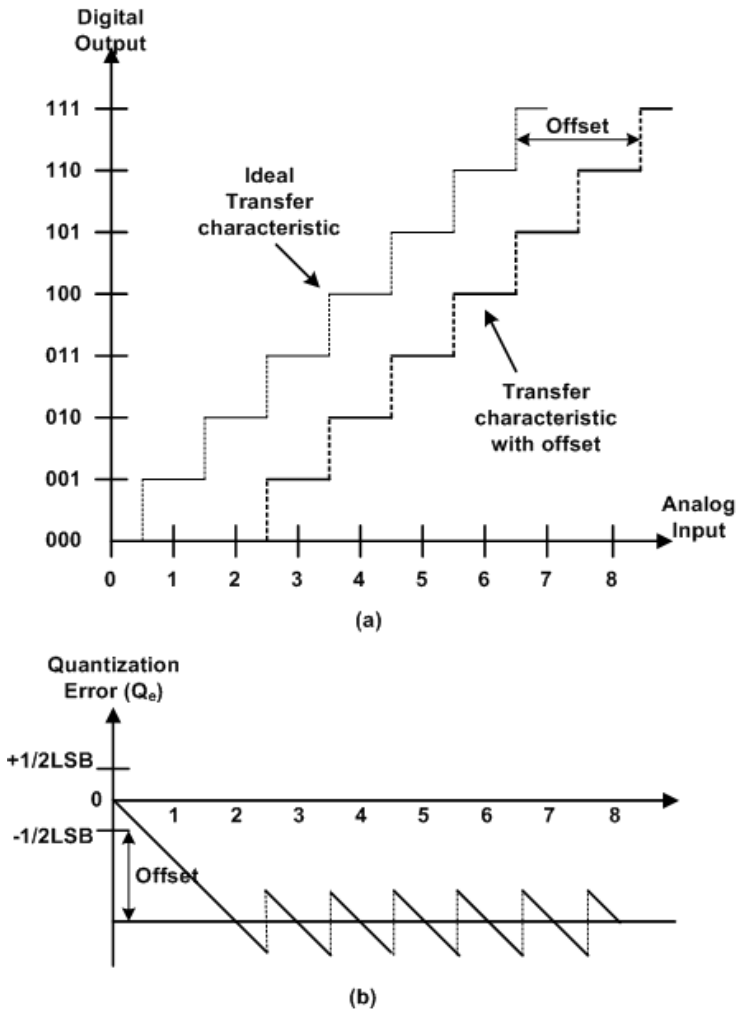


Figure 3.1.5 (a) Transfer function for an ADC with offset error and (b) its corresponding quantization error.

3.1.2.3 Offset

The offset describes a shift for zero input. Offset is an error that can affect an ADC. Fig. 3.1.5 compares the input-output transfer characteristics of a real and an ideal ADC.

The offset changes the transfer characteristics so that all the quantization steps are shifted by the ADC offset. The offset can be measured in LSB, absolute value (volts or amperes), or as % or ppm of the full scale.

3.1.2.4 Gain error

This is the error on the slope of the straight line interpolating the transfer curve. For an ideal converter the slope is D_{FS}/V_{FS}, where D_{FS} and V_{FS} are the full-scale digital code and full-scale analog range respectively. Since D_{FS} represents V_{FS}, we normally say that the ideal slope is one. The gain error defines the deviation of the slope of a data converter from the expected value. Another measure of the gain error is given by the difference between the input voltage causing a transition to the full scale and the reference (minus half LSB). When using this definition the gain error is known as the full scale error.

3.1.2.5 Monotonicity

This is the ADC feature that produces output codes that are consistently increasing with increasing input signal and consistently decreasing with decreasing input signal. Therefore, the output code will always either remain constant or change in the same direction as the input.

3.1.2.6 Missing code

This denotes when digital codes are skipped or never appear at the ADC output. Since missing codes cannot be reached by any analog input the corresponding

quantization interval is zero. Therefore, the DNL becomes −1.

3.1.2.7 Differential non-linearity error (DNL)

For an Ideal ADC, all digital codes have the same code length versus the analog input voltage. However, because of the nonlinearity errors such as offsets and etc., there are deviations from the ideal transfer function. The values for the DNL can be solved as follows:

DNL = Actual step width – Ideal step width

$$DNL(D_i) = \frac{V_{in}(D_i) - V_{in}(D_{i-1}) - V_{LSB}}{V_{LSB}} \tag{3.1.2}$$

DNL which means local error is critical performance parameter in control and video application.

3.1.2.8 Integral non-linearity (INL)

This is a measure of the deviation of the transfer function from the ideal interpolating line. Also INL is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset. It is more informative for estimating harmonic distortion and implying a monotonic behavior of the converter. Therefore INL is critical performance parameter in communication application. The INL for output D_m can be obtained by integrating the DNL until code m

$$INL(D_m) = \sum_{i=1}^{m} DNL(D_i) \tag{3.1.3}$$

3.1.3 DYNAMIC SPECIFICATIONS

The frequency response and speed of the analog components of a data converter determine its dynamic performance. Obviously, the performance becomes critical when the input bandwidth and the conversion-rate are high. Therefore, the specifications either correspond to defined dynamic conditions or are given as a function of frequency, time, or conversion data-rate. A quality factor of a dynamic feature is its capability to remain unchanged within the entire range of dynamic operation.

3.1.3.1 Analog Input Bandwidth

This specifies the frequency at which a full-scale input of an ADC leads to a reconstructed output 3 dB below its low frequency value. This definition differs from what is used for amplifiers which usually use a small signal input.

3.1.3.2 Aperture uncertainty (Clock Jitter)

This is the standard deviation of the sampling time. It is also called aperture jitter or timing phase noise. With the increasing input frequency, suppressing the sampling clock jitter is important not to degrade the SNR performance of ADC. $SNR_{aperture}$ can be solved as follows

$$SNR_{aperture} \cong 10\log\frac{1}{(2\pi f_{in}\sigma_t)^2} \quad (3.1.4)$$

where t is aperture uncertainty which is random with zero mean and standard deviation σ_t.

3.1.3.3 Signal-to-Noise Ratio (SNR)

This is the ratio between the power of the signal and the total noise produced by quantization and the noise of the circuit. The SNR accounts for the noise in the entire Nyquist interval. The SNR can depend on the frequency of the input signal and it decreases proportional to the input amplitude. According to the resolution of an ADC, the maximum SNR is determined by the equation

3.1.3.4 Signal-to-Noise and Distortion Ratio (SNDR)

This is similar in definition to the SNR except that non-linear distortion terms, generated by the input sine wave, are also accounted for. The SNDR is the ratio between the root-mean-square of the signal and the root-sum-square of the harmonic components plus noise (excluding dc). Since static and dynamic limitations cause a non-linear response the SNDR is dependent on both the amplitude and frequency of the input sine wave. Larger input amplitudes bring about distortion especially at high frequencies.

SNDR compares all undesired frequency components with the input signal. Therefore, SNDR is an overall measure of the ADC dynamic performance.

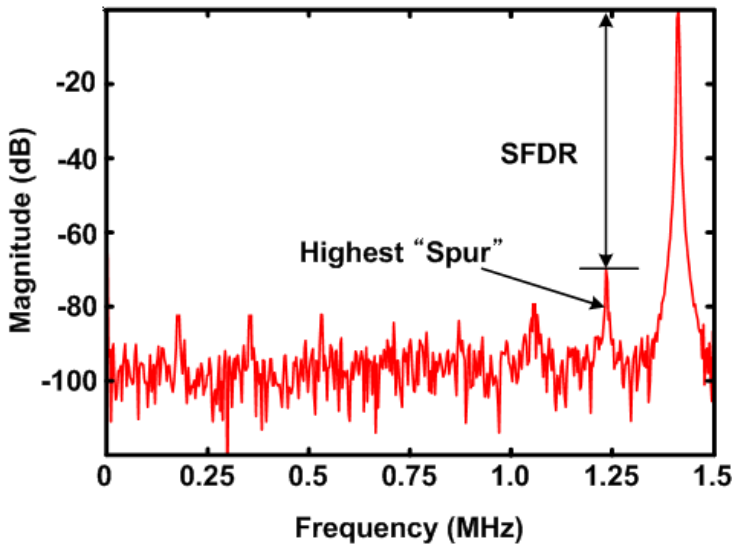


Figure 3.1.6 Spurious Free Dynamic Range

3.1.3.5 Effective-Number-of-Bits (ENOB)

This measures the signal-to-noise and distortion ratio using bits. SNDR in dB and ENOB are linked by

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{3.1.5}$$

3.1.3.6 Spurious Free Dynamic Range (SFDR)

SFDR is the difference between the signal power and the highest spur. The SFDR provides information similar to the total harmonic distortion but focuses on the worst tone. The SFDR depends on the input amplitude. With large input signals the highest tone is given by one of the harmonics of the signal. For input amplitudes well below the full

scale the distortion caused by the signal becomes negligible and other tones not caused by the input become dominant due to the non-linear nature of the converter.

The SFDR is important for communication systems. Often it is necessary to perform analog-to-digital conversion on a small signal representing a channel that the antenna receives together with other big channels. It may happen that a high spur generated by a big channel falls very close to the small channel thus masking the associated information.

3.2 A COMPARATOR-BASED CYCLIC ANALOG-TO-DIGITAL CONVERTER WITH BOOSTED PRESET VOLTAGE [†]

3.2.1 INTRODUCTION

The demand for low-power low-voltage analog-to-digital converters (ADCs) for biomedical sensor applications has recently grown dramatically. Among several ADC architectures, the cyclic ADC achieves high resolution with small chip area and low power [3.2.1]-[3.2.5], because it performs a conversion cyclically by repeated use of a single gain stage. The main disadvantage of this mode of operation is the long conversion cycles, which is exacerbated by the need to use closed-loop amplifiers instead of comparators.

With improvements in technology, the conversion rates achievable by cyclic ADCs have been increasing steadily and digital circuits operate faster and consume less power because of shortened gate lengths and lower power supply voltages. However, this technology scaling simultaneously causes problems in the design of the analog circuits in an ADC. For instance, reduced supply voltage and lower device gain make it difficult to design a high-gain opamp [3.2.6], [3.2.7]. Techniques such as correlated level shifting [3.2.8], open-loop residue amplifiers [3.2.9], gain calibration [3.2.10], and the comparator-based switched-capacitor (CBSC) technique [3.2.11] have been developed to

[†] This sub chapter is published in *proceeding of International Symposium on Low Power Electronics and Design (ISLPED'*11*)* [3.2.13]. The author of the thesis is co-author of the published paper.

address some of these challenges. These techniques either reduce the gain requirements for a given resolution, or eliminate the opamp completely.

Our present contribution to these developments is a new design of cyclic ADC which is an improved application of the CBSC technique [3.2.11]. Using CBSC, we replace the opamp in a switched-capacitor circuit with a comparator and current sources while maintaining the same function. It completely removes opamps from the design, and eliminate the need to stabilize a high-gain, high-speed feedback loop. This not only reduces complexity but also avoids the existing trade-off between bandwidth and power. Additionally, the proposed boosted preset voltage scheme which improves on the original application of CBSC to cyclic ADCs allows the system to obtain a quick, rough estimate of the output and the virtual ground voltage. And then, we enhance the conversion rate without increasing the power consumption.

In chapter 3.2.2 of this brief, we review the switched-capacitor circuits. In chapter 3.2.3, we present our new architecture and then describe a circuit implementation in chapter 3.2.4. Measured results are presented in chapter 3.2.5.

3.2.2 SWITCHED-CAPACITOR CIRCUITS

The operation of opamp-based and comparator-based switched-capacitor gain stages is very similar. The main difference is that, whereas an opamp forces the virtual ground voltage during the entire charge transfer phase, the comparator detects the virtual ground voltage and uses it to trigger a sampling process.

3.2.2.1 Opamp Based Switched-Capacitor Circuits

An opamp based switched-capacitor gain stage operates in two phases. The input voltage is sampled during the sampling phase and that voltage is multiplied during the charge transfer phase. During the sampling phase, the capacitors C_1 and C_2 sample the input voltage. The charge $Q_{1,2}$ on $C_{1,2}$ can be expressed as follows.

$$Q_{1,2} = C_{1,2}\left(V_{IN} - V_{COM}\right) \tag{3.2.1}$$

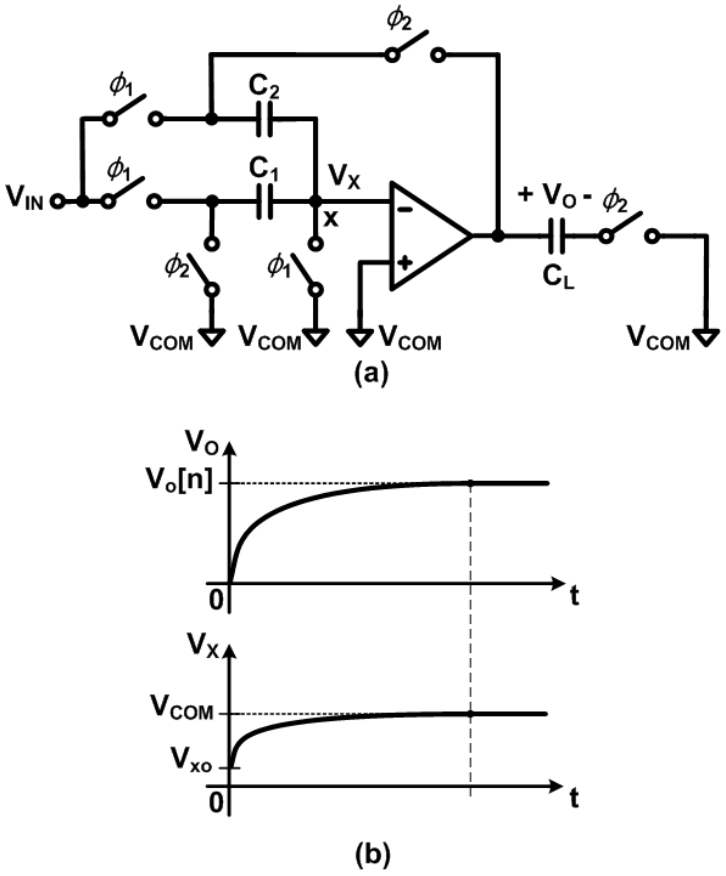


Fig. 3.2.1 (a) Opamp-based switched-capacitor gain stage, and
(b) its transient response.

Figure 3.2.1 (a) shows an opamp-based switched-capacitor gain stage in its charge transfer phase. The opamp forces the voltage of node X to the virtual ground voltage. Then, the gain stage transfers all the charge sampled by C_1 to C_2. Figure 1 (b) shows the charge transfer phase, during which V_X approaches the virtual ground voltage exponentially. Eventually, V_X settles at the virtual ground, and the output voltage is sampled by the load capacitance C_L. The settling time is heavily dependent on the driving

capability of the opamp.

The relationship between the input and the output voltages can be expressed as follows:

$$V_O = \left(\frac{C_1 + C_2}{C_2} \right) V_{IN} \tag{3.2.2}$$

During the charge transfer phase, the accuracy of the output voltage is directly dependent on the accuracy of the virtual ground voltage, and the opamp operates continuously to maintain this voltage. But this accurate virtual ground voltage is only necessary during the charge transfer phase in a switched-capacitor circuit. By providing the virtual ground voltage by means of a comparator and a current source during the charge transfer phase alone, the virtual ground condition can be maintained with less power than by using opamp.

3.2.2.2 Comparator Based Switched-Capacitor Circuits

A comparator-based switched-capacitor gain stage needs the same two phases as an opamp-based switched-capacitor gain stage. The sampling phase is essentially the same, even though the opamp has been replaced by a threshold-detection comparator and a current source. The charge transfer phase is preceded by a preset phase which ensures that

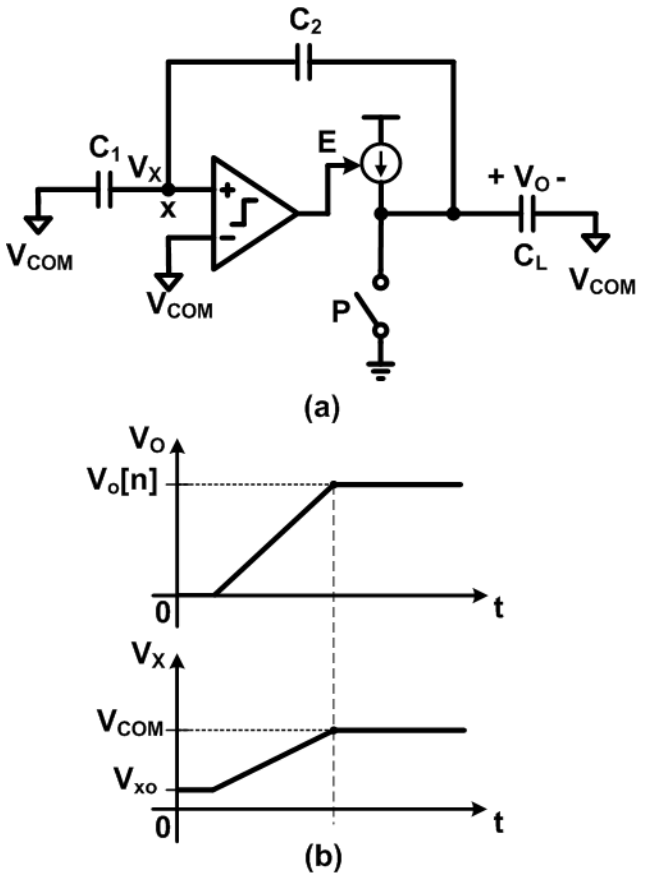


Fig. 3.2.2 (a) Comparator-based switched-capacitor gain stage, and
(b) its transient response

V_X starts below V_{COM}. Then, the current source is turned on, and it charges up the capacitor network consisting of C_1, C_2 and C_L, creating the ramp waveforms V_O and V_X shown in Fig. 2. At the end of the charge transfer phase, the voltage V_X is equal to V_{COM}.

During the preset phase, V_{COM} is connected to C_2, and the output of the stage is connected to the lowest voltage. This pulls V_X low and takes V_{XO} below V_{COM} over the

full range of the input voltages. A sampling switch is also closed during the preset phase to reset the load capacitance. Thus, the preset value of the summing node voltage V_{XO} can be expressed as follows:

$$V_{X0} = \left(2 - \frac{C_2}{C_1 + C_2}\right) V_{COM} - V_{IN} \tag{3.2.3}$$

We can see from this equation, the time required to complete the charge transfer depends on the preset voltage V_{XO}, which depends on the nature of the input signal. The charge transfer is self-timed, but correct operation requires that the charge transfer should be fully complete before the end of the time allocated for the entire charge transfer phase.

3.2.3 PROPOSED CYCLIC ANALOG TO DIGITAL CONVERTER

3.2.3.1 Comparator-Based Cyclic ADC

The block diagram of the proposed cyclic ADC is shown in Fig. 3.2.3 It consists of two multiplying DACs (MDACs), two 1.5-bit sub-ADCs (SADCs), digital correction logic, and a clock generator. The sample-and-hold amplifier (SHA) in a cyclic ADC has

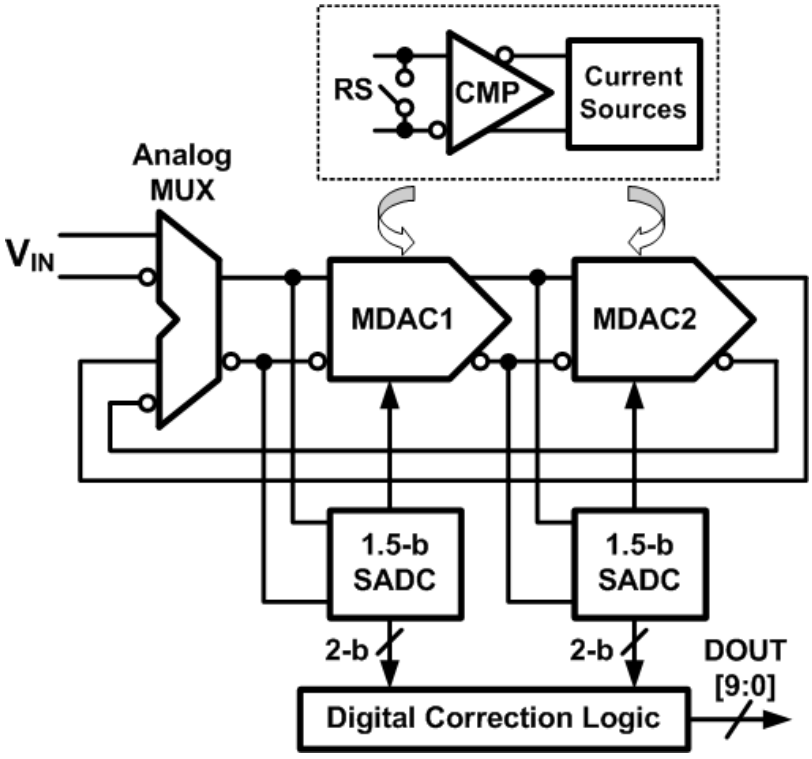


Fig. 3.2.3 Block diagram of the proposed cyclic ADC

two main functions: 1) sampling the analog input signal and 2) sampling the output of the MDAC and transferring it to the input of the same MDAC for the subsequent conversion cycle that produces the next. There is no SHA for sampling the analog input signal because switched-capacitor sampling by MDAC1 provides an equivalent function. This sampling is necessary because of the cyclic nature of the ADC timing, but it does not have any effect on the conversion speed. If SHAs were presented, they would only add noise to the signal path. In our prototype design, the redundant SHA was removed and an extra set of MDAC and SADC stages were added [3.2.12]. This doubles the conversion speed and avoids additional noise contributions of the redundant SHA. In other words, this leads to a reduction in chip area and power consumption despite an additional set of MDAC and SADC.

Comparator-based systems potentially use less power than opamp-based systems because of the differences in the noise-bandwidth and speed requirements of opamp and comparator based designs. In addition, comparator-based designs are easier to scale than opamp-based designs because a comparator and current sources have less stringent requirements than an opamp. The big difference is that comparator-based systems avoid feedback and stability concerns, and the high output resistance of the current sources are taken out of the signal path. Adopting the CBSC technique allows us to use a single comparator and current sources to support the two MDACs. This is a similar concept to amplifier sharing [3.2.3], and further reduces power consumption.

3.2.3.2 Boosted Preset Voltage Scheme

The offset and nonlinearity of a CBSC stage are proportional to the charging current: a large charging current produces a large overshoot and consequently a large offset. The nonlinearity of the output voltage is the product of the percentage change in the ramp rate and the overshoot voltage. Thus the nonlinearity can be reduced by reducing the overshoot, which can be achieved by having two charge transfer phases. The second phase uses a lower current and this reduces overshoot and hence the nonlinearity.

We have already mentioned the use of a brief preset phase to ensure V_X starts below the virtual ground condition V_{COM} using the lowest voltage. In our design, to enhance the operation speed, the output node is switched to the proper voltage which makes the voltage V_X starts slightly below the virtual condition V_{COM}. In the subsequent coarse charge transfer phase, the system can obtain a quick, rough estimate of the output and virtual ground condition.

To derive the effectiveness of this scheme, the voltage V_{XO} should be calculated including the preset voltage. In Fig. 3.2.2, from its initial value V_{COM} and the superposition of the voltage steps at V_X from closing switches at C_1 to V_{COM} and C_2 to V_{PRESET} instead of ground, the Equation (3.2.3) of the preset value of the voltage at the summing node V_{XO} is now expressed as follows:

$$V_{xo} = V_{com} + \frac{C_1}{C_1 + C_2} V_R - V_{IN} + \frac{C_1}{C_1 + C_2} V_{PRESET} \tag{3.2.4}$$

where V_{PRESET} is the preset voltage applied at the output node. V_R is one of DAC voltage levels. If values of the capacitors C_1 and C_2 are equal, then the constraint that the summing node voltage V_{X0} must be greater than zero and less than V_{COM} results in the following range of valid preset voltages;

$$V_{PRESET} \leq 2V_{IN} - V_R \tag{3.2.5}$$

$$(C_1 = C_2, V_{X0} \leq V_{PRESET})$$

According to 1.5bit stage transfer characteristic, the valid range of preset voltages in terms of V_{COM} and V_{REF} is expressed by:

$$0 \leq V_{PRESET} \leq V_{COM} - V_{REF} \tag{3.2.6}$$

After the preset phase, a large charging current is used to achieve a rough estimate of the output voltage. Assuming that the current source has a finite resistance, KCL yields the differential equation

$$I_0 = C_E \frac{dV_O(t)}{dt} + \frac{V_O(t)}{R_0} \tag{3.2.7}$$

where C_E is the capacitance at the output node, V_O is the output voltage, I_0 is the current from the current source, and R_0 is the output resistance of the current source. Solving this equation for the initial condition $V_O(0)=V_{PRESET}$ yields

$$V_0(t) = I_0 R_0 \left(1 - e^{-\frac{t}{R_0 C_E}}\right) + V_{PRESET} \tag{3.2.8}$$

Then the maximum charging time is determined by Equation (3.2.6) and the relationship between V_{IN} and V_O, as follows:

$$t_{\max} = -R_0 C_E \ln\left(1 - \frac{V_{COM} + V_{REF} - V_{PRESET}}{I_0 R_0}\right) \tag{3.2.9}$$

This equation tells us that boosting V_{PRESET} can reduce the time required to obtain a rough estimate of the output and virtual ground voltage. Because the switching threshold is not signal-dependent, no additional error is introduced, except a constant offset from the comparator. But we expect this to have negligible effect at 10-bit resolution.

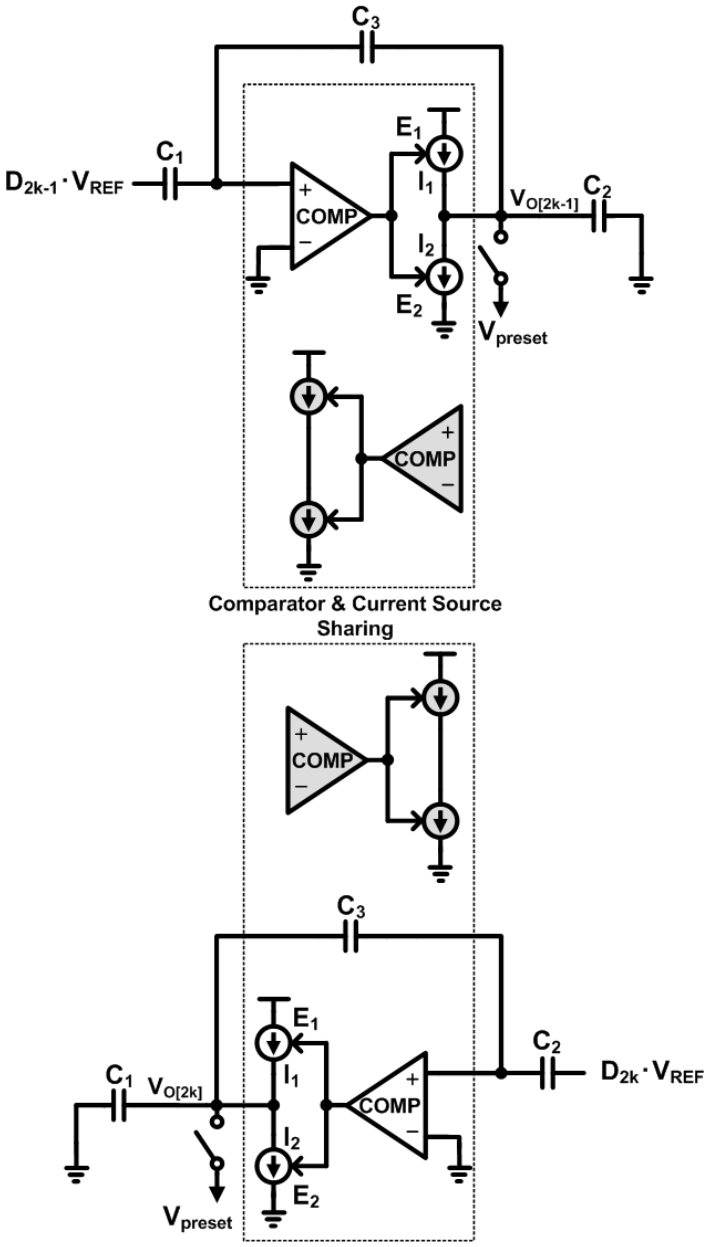


Fig. 3.2.4 Simplified representation of MDAC1 and MDAC2 during odd and even phases.

3.2.4 CIRCUIT IMPLEMENTATION

3.2.4.1 Simplified Schematic Diagram of the Cyclic ADC

Figure 3.2.4 is a simplified representation of MDAC1 and MDAC2 in our cyclic ADC. This circuit needs two SADCs, which are not shown in this figure. At first, the input voltage is sampled and determined by SADC1. Then, a value produced by SADC1 is used at odd phase, and the output voltage is sampled by SADC2. At each even phase, an output voltage is produced from the digital code generated by SADC2, and the output value is sampled by SADC1. The use of two SADCs allows each stage to use a single clock phase. The clocking scheme requires a half clock signal, and the two clock phases do not overlap.

To improve high accuracy and linearity, the charge transfer phase is divided into three sub-phases: a preset phase, a coarse charge transfer phase (E_1), and a fine charge transfer phase (E_2). The boosted preset voltage ensures that the input node of the comparator is brought just below the virtual ground voltage during the short preset phase. The coarse charge transfer phase (E_1) is used to get a fast, rough estimate of the output voltage and virtual ground condition. When the comparator makes its decision, the current source I_1 is turned off. The finite delay of the comparator and the high output ramp rate cause the voltage to overshoot the correct value. In the fine charge transfer phase (E_2), a more accurate value is obtained for the output voltage. The fine-phase current I_2 is much less than the coarse-phase current I_1, and flows in the opposite direction.

3.2.4.2 Threshold-Detection Comparator

The comparator is a critical part of the CBSC circuit, and is used to detect the virtual ground voltage accurately. The comparator should change its output as soon as its input crosses the virtual ground voltage. A high-gain comparator is required to reduce the error. The gain of a comparator can be increased by cascading gain stages, but this raises a stability problem in an opamp-based switched-capacitor circuit, because the opamp is

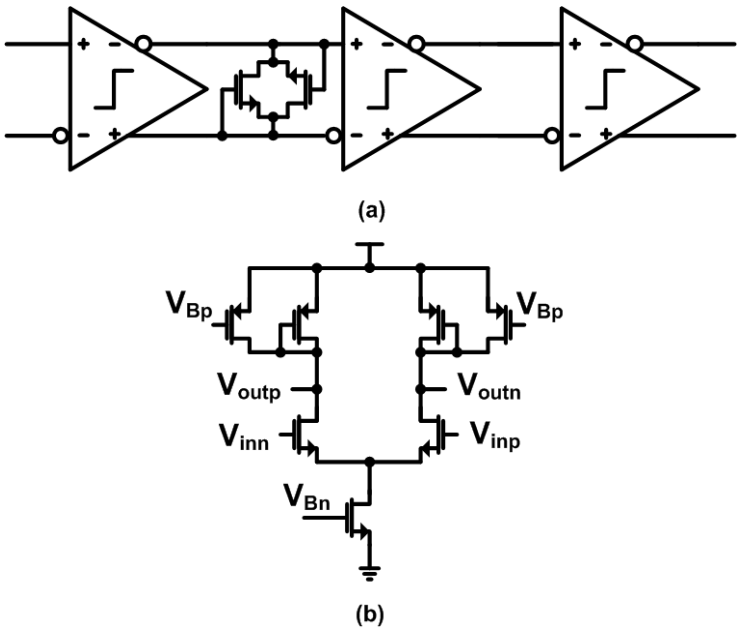


Fig. 3.2.5 Schematic diagram of (a) the threshold-detection comparator and (b) the preamplifier

configured as a closed loop. But the comparator in a CBSC circuit is an open loop, and so a cascading configuration poses no stability problem. Figure 3.2.5 shows a schematic diagram of our high gain comparator, which consists of three cascaded preamplifiers. The outputs of the first stage of the comparator are connected by two MOS diodes to reduce the conversion time, and the outputs of the final stage are buffered with inverters to drive logic circuits which control the current sources.

3.2.5 EXPERIMENTAL RESULTS

The proposed circuit was fabricated in 0.18µm CMOS technology and provided with a 1.8V supply voltage. Figure 3.2.6 shows a microphotograph of the die, which has the area of 0.146mm^2.

As shown in Fig. 3.2.7, at a 2.5MS/s conversion rate, with boosted preset voltage scheme, the measured signal-to-noise and distortion ratio (SNDR) and the spurious-free dynamic-range (SFDR) are 55.99 dB and 66.85 dB near the Nyquist-rate sinusoidal input.

As mentioned earlier, boosting the preset voltage speeds up the conversion rate. In order to prove the effectiveness of the proposed scheme, the preset voltages have been

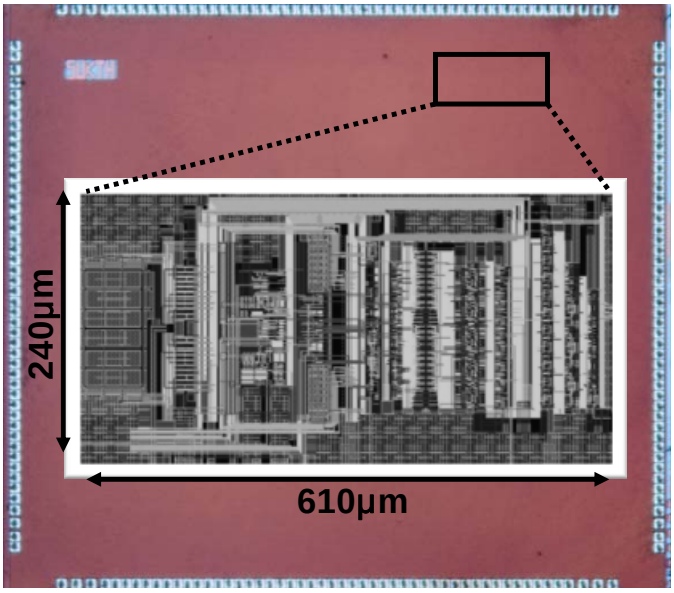


Fig. 3.2.6 Microphotograph of the prototype die

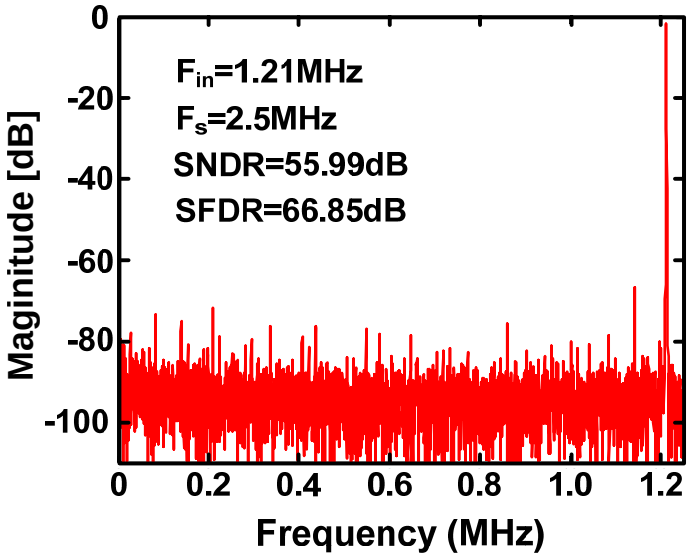


Fig. 3.2.7 FFT plot of measured data with boosted preset voltage at a sampling rate of 2.5MS/s.

assigned minimum and maximum values of Equation (3.2.7), and the measured SNDR and effective number of bits (ENOB) according to the sampling frequency at a same input rate are shown in Fig.3.2.8 and Fig. 3.2.9.

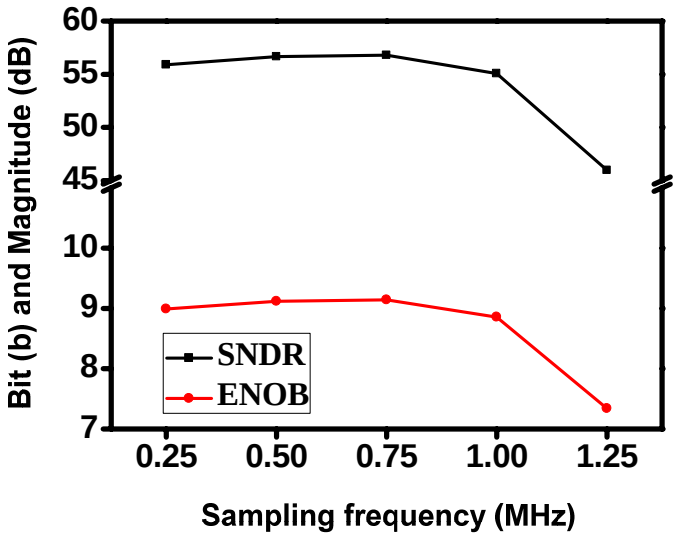


Fig. 3.2.8 Measured SNDR and ENOB versus sampling frequency at a input rate of 0.101MHz without boosted preset voltage.

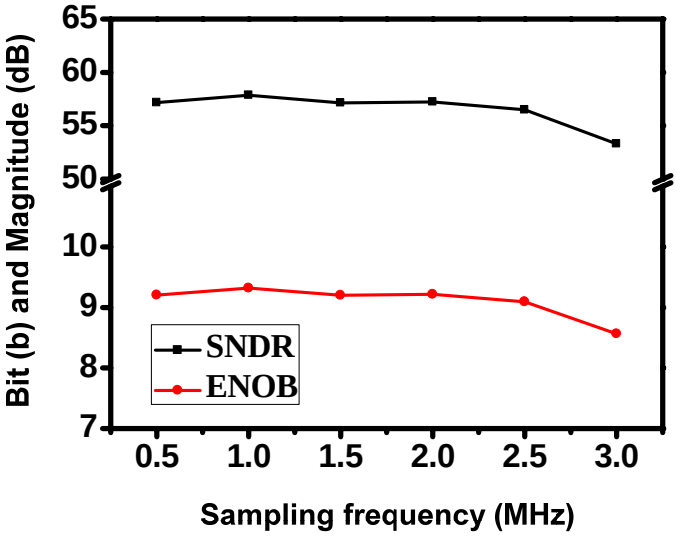


Fig. 3.2.9 Measured SNDR and ENOB versus sampling frequency at a input rate of 0.101MHz with boosted preset voltage.

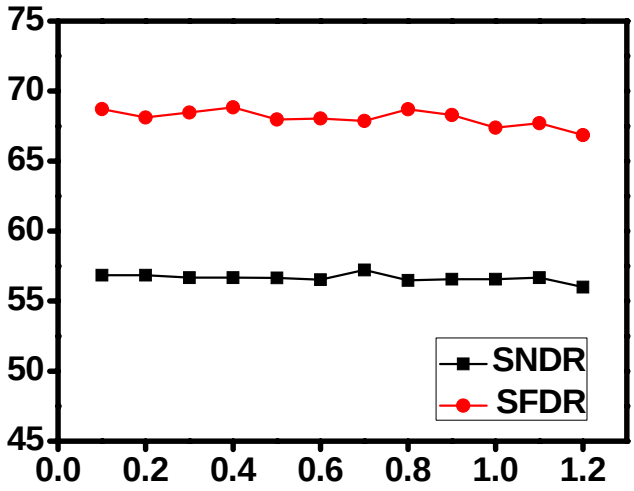


Fig. 3.2.10 Measured SNDR and SFDR versus input frequency
at a sampling rate of 2.5MS/s.

Without boosted preset voltage, there is no performance degradation to a maximum conversion rate of 1MS/s. However, if the proposed scheme is applied, the maximum sampling frequency increases to more than 2.5MHz. From these results, the proposed scheme enhances the conversion rate effectively without using additional power.

Figure 3.2.10 shows the relationship of the measured SNDR and SFDR with the input frequency. Until the Nyquist-rate input, the ENOB is more than 9.0.

Table 3.2.1 Performance summary

Parameter	**Value**
Supply voltage	1.8V
Technology	0.18 μm 1P6M CMOS
Resolution	10-bit
Sampling frequency (Clock frequency)	2.5MHz (12.5MHz)
Input range	$1V_{P-P}$
SNDR	55.99 dB (f_{in}=1.21MHz)
SFDR	66.85 dB (f_{in}=1.21MHz)
Power consumption (w/o I/O power)	0.74mW
Chip size	$0.146mm^2$

Table 3.2.1 summarizes the performance of the proposed cyclic ADC. Operating at a 2.5MHz sampling rate, with a $1V_{P-P}$ range, it consumes 0.74mW at the supply voltage of 1.8V.

3.2.6 SUMMARY

We have presented a comparator-based cyclic analog-to-digital converter in which the preset voltage is boosted. The use of a comparator-based switched-capacitor circuit saves a significant amount of power, compared to conventional opamp-based designs. Additionally, a scheme that boosts the preset voltage to enhance the conversion rate without using any extra power has been implemented and evaluated. This approach is more suitable for scaled technologies than equivalent opamp-based circuits.

Our prototype was fabricated in 0.18µm CMOS, has an active area of 0.146mm^2, and consumes 0.7mW from a 1.8V supply. When the input is near the Nyquist-rate, the SNDR is 55.99 dB and the SFDR is 66.85 dB, at 2.5MS/s. These results suggest that our circuit is superior to existing designs for usage in low-power high-resolution ADCs implemented in deep-submicron technology.

3.3 A 12-BIT ASYNCHRONOUS CYCLIC ADC WITH MULTI-LEVEL INPUT TRACKING BOOSTED PRESET VOLTAGE AND COMPARATOR WITH ADJUSTABLE THRESHOLD VOLTAGE

3.3.1 INTRODUCTION

As mentioned in the previous chapter, a comparator-based switched-capacitor gain stage needs the same two phases, sampling and charge transfer phases, as an opamp-based switched-capacitor gain stage. The sampling phase is essentially the same, even though the opamp has been replaced by a threshold-detection comparator and a current source. To achieve high resolution, the charge transfer phase of CBSC consists of three phases which are preset, coarse charge transfer and fine charge transfer phases. Figure 3.3.1 shows the schematic and the timing diagram of the comparator-based switched-capacitor gain stage. The voltage of the overshoot in the coarse charge transfer phase can be compensated by a small current source in the fine charge transfer phase. The current source in the fine charge transfer phase has a trade-off between conversion speed and resolution.

In chapter 3.3.2, to improve both conversion speed and resolution, we present multi-level input tracking boosted preset voltage, asynchronous timing control scheme, and comparator with adjustable threshold voltage. We describe the circuit implementation in chapter 3.3.3. Simulation results are presented in chapter 3.3.4.

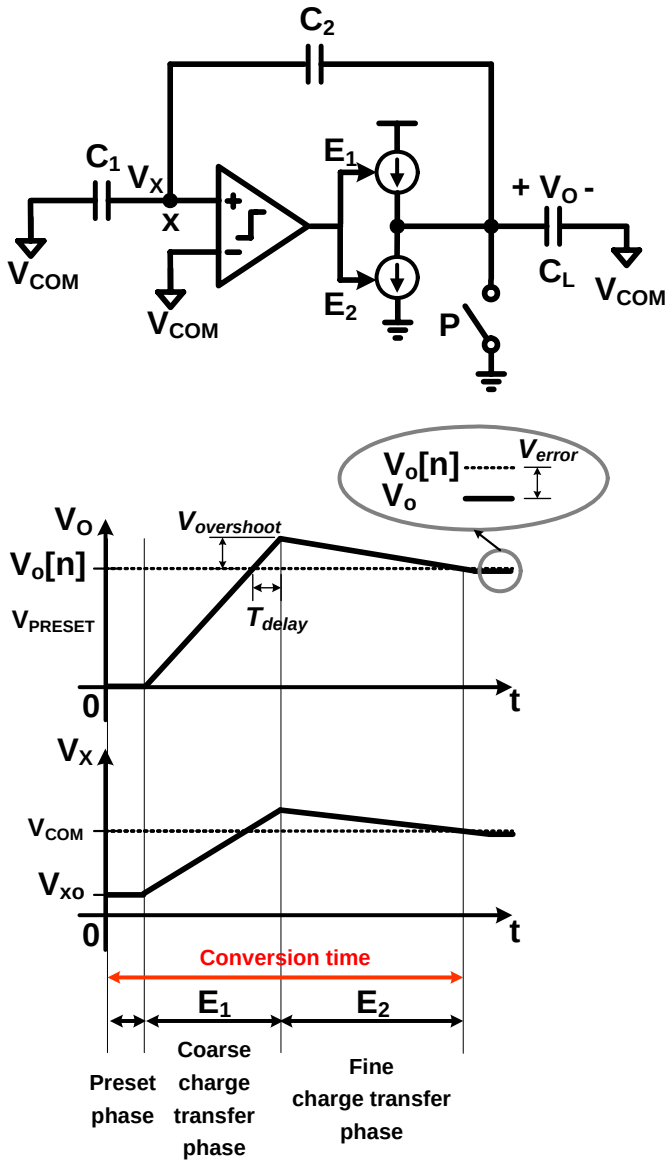


Fig. 3.3.1 The schematic and timing diagram of CBSC gain stage

3.3.2 PROPOSED CYCLIC ANALOG TO DIGITAL CONVERTER

3.3.2.1 Multi-level Input Tracking Boosted Preset Voltage

The prime constraint of CBSC is that V_X starts below the virtual condition V_{COM}. To satisfy this constraint, the conventional design adopts two preset voltages which are ground and V_{DD}. These two preset voltage guarantee the CBSC constraint. To enhance the conversion time, our previous work [3.3.10] used two fixed preset voltages.

Figure 3.3.2 shows the simplified block diagram of our proposed scheme and its transient response. One cycle conversion process consists of preset (P), coarse current evaluation (E1) and fine current evaluation (E2). The sub-ADC has three output levels in the 1.5bit stage. Input tracking preset voltages according to the input voltage or the residue voltage is used to enhance the conversion rate further. Moreover, by reusing the sub-ADC in the MDAC, the proposed input tracking preset voltages scheme does not needed additional circuits. The proposed method can achieve shorter coarse conversion time then conventional one. This technique can also reduce the power consumption because V_O node is discharged to V_{PRESET} which is higher than ground voltage. It means that the node of V_O can charge to V_{COM} with less coarse current.

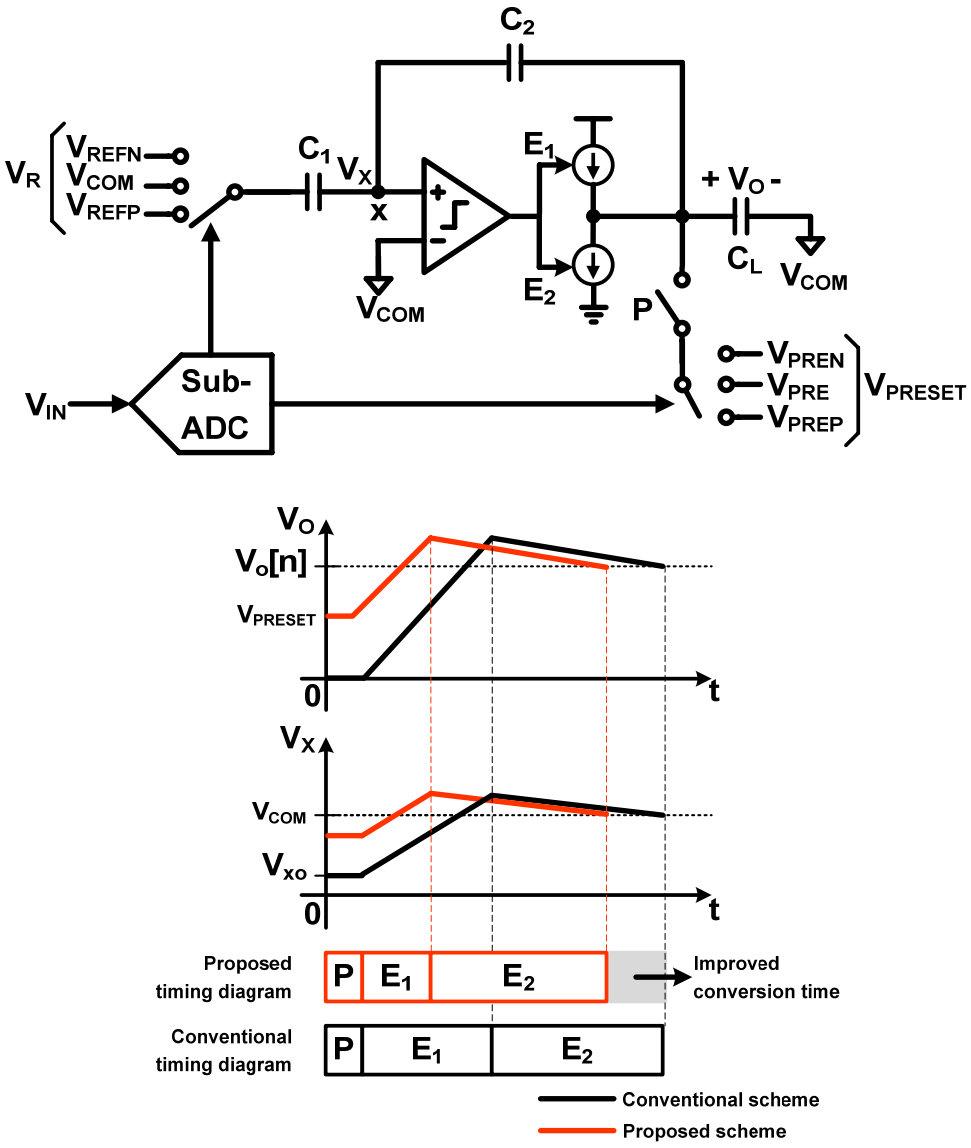


Fig. 3.3.2 (a) Proposed CBSC gain stage with multi-level input tracking boosted preset voltage, and (b) its transient response

3.3.2.2 Analysis of 1.5bit stage with Multi-level Input Tracking Boosted Preset Voltage

To derive the effectiveness of this scheme, the voltage V_{XO} should be calculated including the preset voltage. Considering V_{PRESET} and V_R, V_{XO} is now expressed as follows:

$$V_{xo} = V_{com} + \frac{C_1}{C_1 + C_2} V_R - V_{IN} + \frac{C_1}{C_1 + C_2} V_{PRESET} \tag{3.3.1}$$

where V_{PRESET} is the preset voltage applied at the output node. V_R is one of voltage levels which are $V_{COM}+V_{REF}$, V_{COM} and $V_{COM}-V_{REF}$. If values of the capacitors C_1 and C_2 are equal, then the constraint that the summing node voltage V_{X0} must be greater than zero and less than V_{COM} results in the following range of valid preset voltages;

$$V_{PRESET} \leq 2V_{IN} - V_R \tag{3.3.2}$$

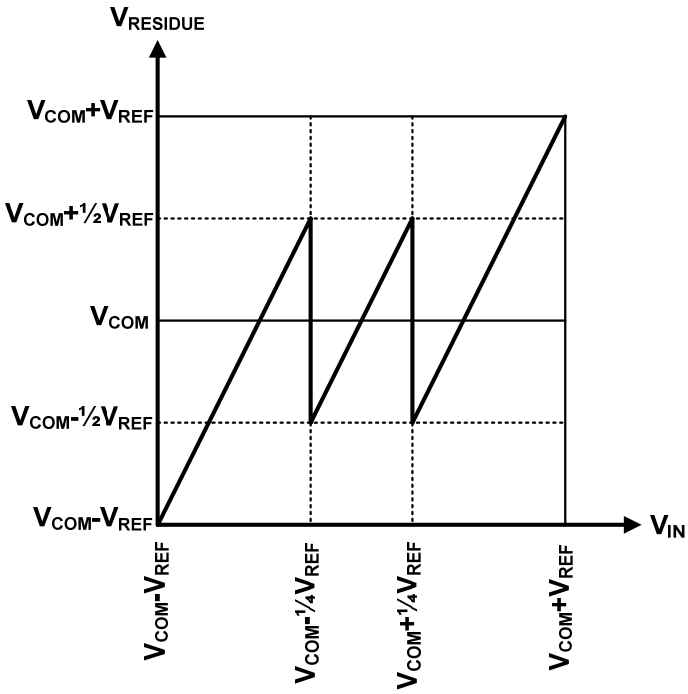


Fig. 3.3.3 Residue transfer characteristic of 1.5bit stage

From Fig. 3.3.3, the range can be split according to the input voltages, and equation (3.3.2) can be expressed as Table 3.3.1.

Table 3.3.1 Summary of V_{PRESET} and V_{XO} according to input voltage

Input voltage	MAX($V_{PRESEET}$)	MIN(V_{XO})
$V_{COM}-V_{REF} \le V_{IN} < V_{COM}-\frac{V_{REF}}{4}$	$V_{COM}-V_{REF}$	$V_{COM}-\frac{3}{4}V_{REF}$
$V_{COM}-\frac{V_{REF}}{4} \le V_{IN} < V_{COM}+\frac{V_{REF}}{4}$	$V_{COM}-\frac{V_{REF}}{2}$	$V_{COM}-\frac{1}{2}V_{REF}$
$V_{COM}+\frac{V_{REF}}{4} \le V_{IN} < V_{COM}+\frac{V_{REF}}{4}$	$V_{COM}-\frac{V_{REF}}{2}$	$V_{COM}-\frac{3}{4}V_{REF}$

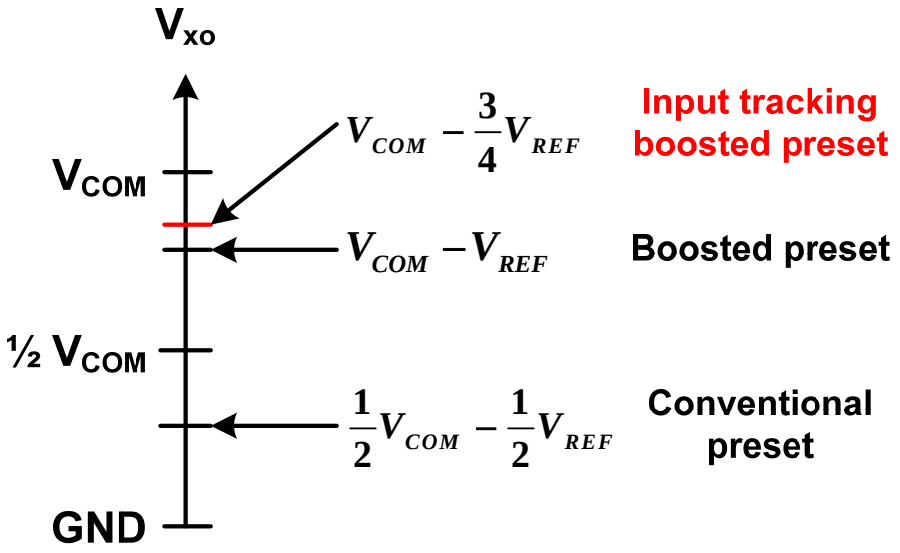


Fig. 3.3.4 V_{OX} comparison of various preset method

Figure 3.3.4 shows the V_{OX} comparison result between proposed preset method and previous ones. As shown in this figure, input tracking boosted preset scheme has smallest dropout, which means further reduction of the conversion time of coarse charge transfer phase.

3.3.2.3 Asynchronous Timing Control Scheme

In the conventional synchronous cyclic ADC, one cycle conversion time is synchronized by the external clock. Even though V_{XO} varies according to the input voltage is not fastened, cycle conversion time is fixed. Therefore sampling rate is affected by the maximum conversion time of one cycle. Fig. 3.3.5 shows the finite state machine of the proposed asynchronous cyclic ADC. The design only synchronizes the sampling signal. The other state transitions are controlled by internal signals such as the outputs of the comparator and counter. Initially, input is sampled during the sample signal.

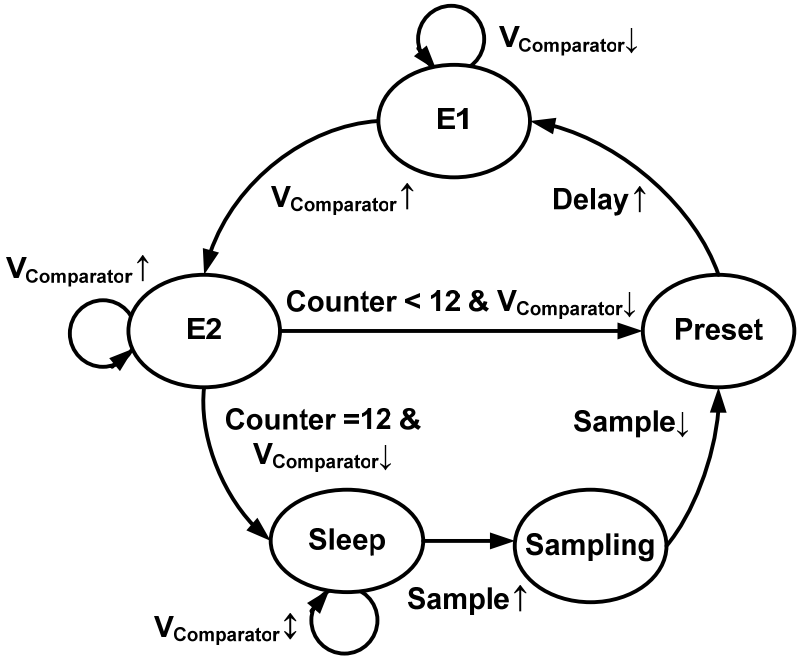


Fig. 3.3.5 FSM of proposed asynchronous cyclic ADC

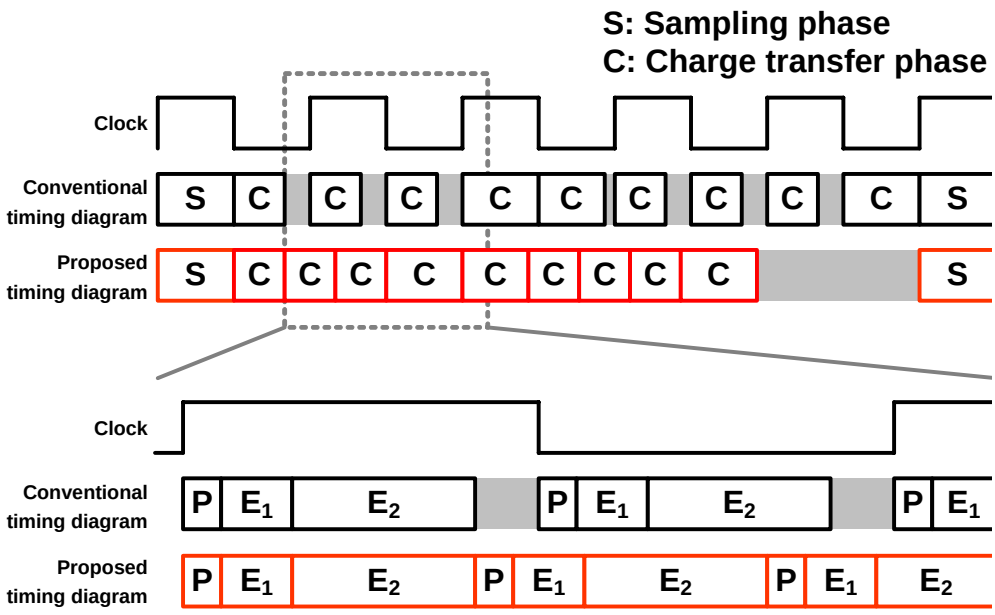


Fig. 3.3.6 Timing diagram of asynchronous cyclic ADC

Then the state transits sequentially to preset, then coarse charge transfer phase (E1), and then fine charge transfer phase (E2). When the 12 cycle conversion ends, finally the ADC enters sleep mode. This sleep mode is maintained until the next signal of sample and helps reduce the power consumption because the current source and comparator are power down. Figure 3.3.6 shows the timing diagram of asynchronous cyclic ADC.

3.3.2.4 Comparator with adjustable threshold voltage

The offset and nonlinearity of a CBSC stage are proportional to the charging current: a large charging current produces a large overshoot and consequently a large offset. The nonlinearity of the output voltage is the product of the percentage change in the ramp rate

and the overshoot voltage. Thus the nonlinearity can be reduced by reducing the overshoot, which can be achieved by having two charge transfer phases. The second phase uses a lower current and this reduces overshoot and hence the nonlinearity. In the CBSC which has two charge transfer phases CBSC, the charging current and feedback delay generates overshoot which affects the conversion rate. Also, the discharge current and feedback delay creates error voltage which affects the resolution. To alleviate overshoot and offset effect, the feedback delay which includes the comparator, switch and wire delays should be minimized. However, to reduce the comparator delay which is mainly occupied in the feedback delay large power consumption is needed.

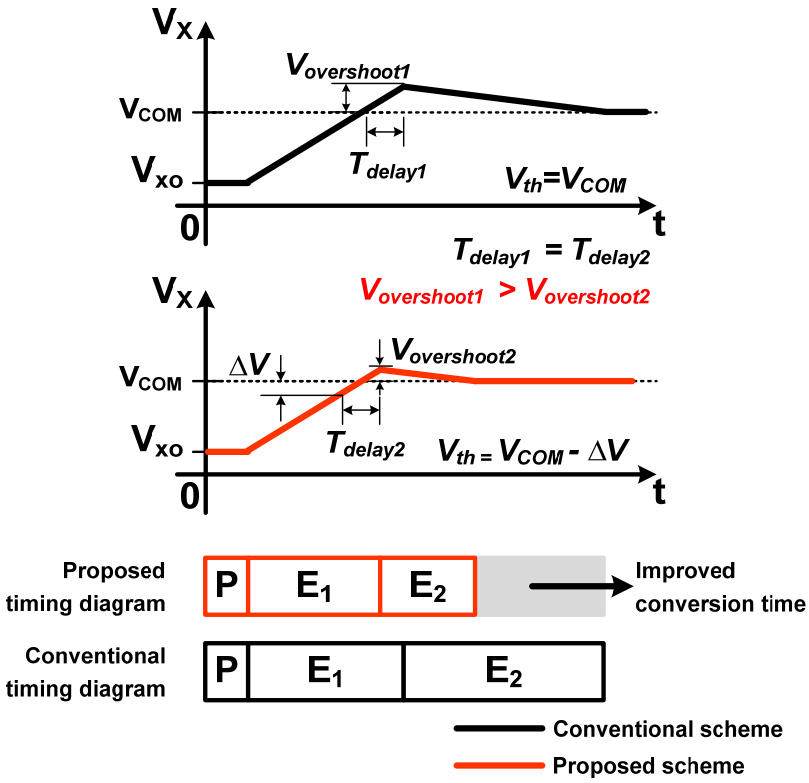


Fig. 3.3.7 Proposed comparator with adjustable threshold voltage in coarse charge transfer phase

To overcome the problem, the proposed comparator with adjustable threshold voltage is presented as shown in Fig. 3.3.7 and Fig. 3.3.8. The proposed comparator with adjustable threshold voltage is used to reduce the coarse conversion time with T_{delay}. Moreover the overshoot is reduced which means that the fine conversion time is also shortened. V_{th} of the comparator and the improved conversion time are now expressed as follows:

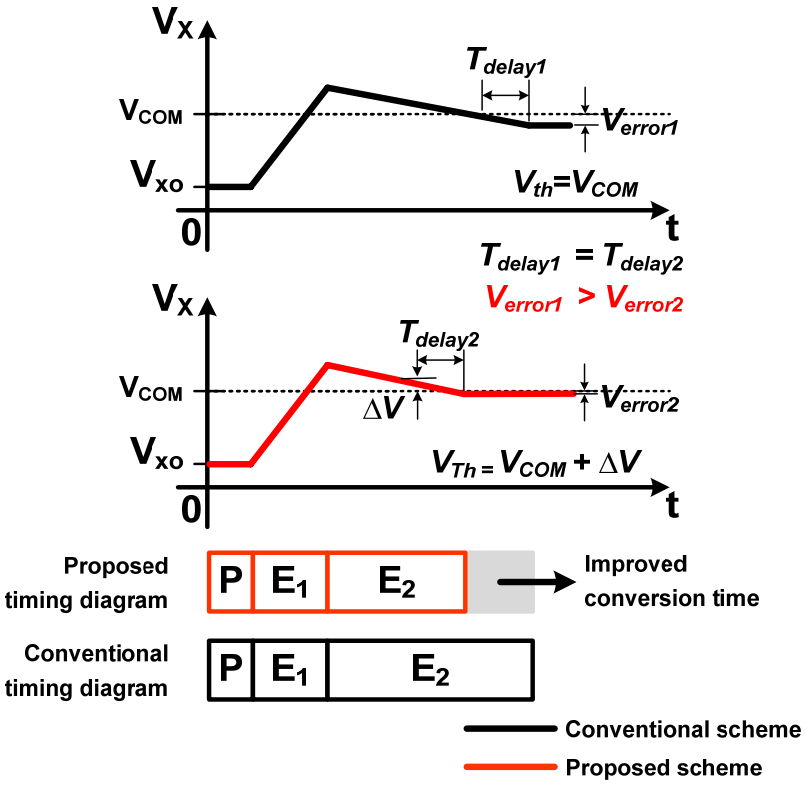


Fig. 3.3.8 Proposed comparator with adjustable threshold voltage in fine charge transfer phase

$$V_{th} = V_{COM} - \frac{I_{Coarse} \cdot T_{delay}}{C_L} \tag{3.3.3}$$

$$T_{improved\_conversion} = T_{dealy} + \frac{C_L \cdot (V_{overshoot1} - V_{overshoot2})}{I_{Fine}} \tag{3.3.4}$$

3.3.3 CIRCUIT IMPLEMENTATION

Figure 3.3.9 is a simplified representation of MDAC1 and MDAC2 in our cyclic ADC. This circuit needs two sub-ADCs, which are not shown in this figure. First, the input voltage is sampled and determined by SADC1. Then, the value produced by SADC1 is used at odd phase, and the output voltage is sampled by SADC2. At each even phase, an output voltage is produced from the digital code generated by SADC2, and the output value is sampled by SADC1. The use of two SADCs allows each stage to use a

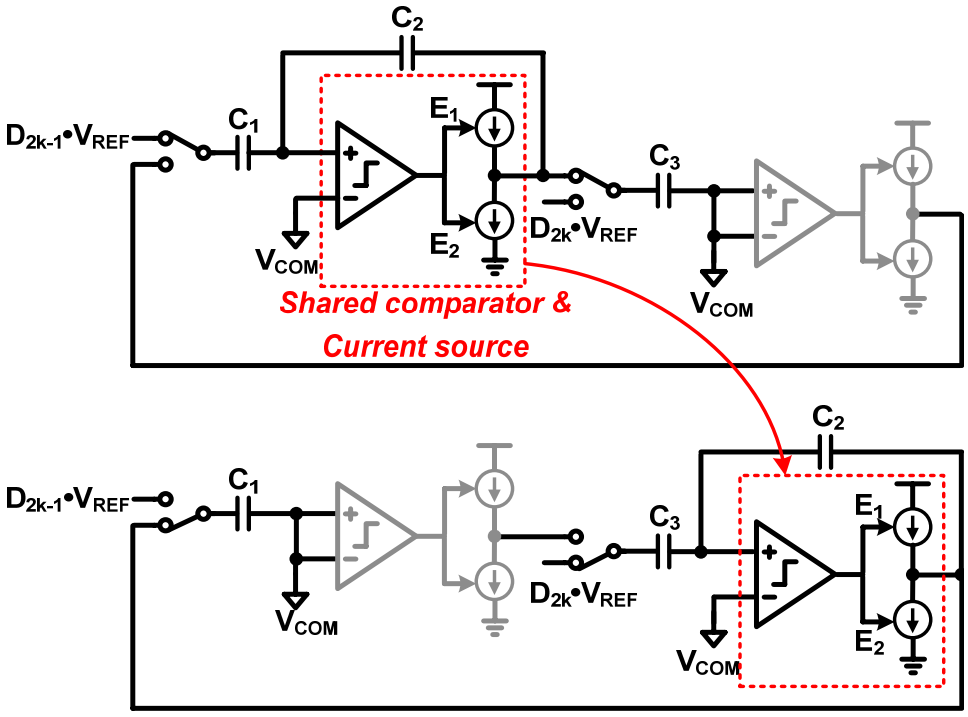


Fig. 3.3.9 Simplified representation of MDAC1 and MDAC2 during odd and even phases

single clock phase. The clocking scheme requires a half clock signal, and the two clock phases do not overlap.

To improve accuracy and linearity, the charge transfer phase is divided into three sub-phases: a preset phase, a coarse charge transfer phase, and a fine charge transfer phase. The boosted preset voltage ensures that the input node of the comparator is brought just below the virtual ground voltage during the short preset phase. The coarse charge transfer phase is used to get a fast, rough estimate of the output voltage and virtual ground condition. When the comparator makes its decision, the current source I1 is turned off. The finite delay of the comparator and the high output ramp rate cause the voltage to overshoot the correct value. In the fine charge transfer phase, a more accurate value is obtained for the output voltage. The fine-phase current I2 is much less than the coarse-phase current I1, and flows in the opposite direction. The shared comparator and current source are used for less power consumption in our design. The same residue voltage is held across both C_2 and C_3 when charge transfer phase is over. The C_2 is a feedback capacitor and also half the loading capacitor in MDAC1. Therefore only three capacitors are required during sample and charge transfer phase in MDAC1 and MDAC2.

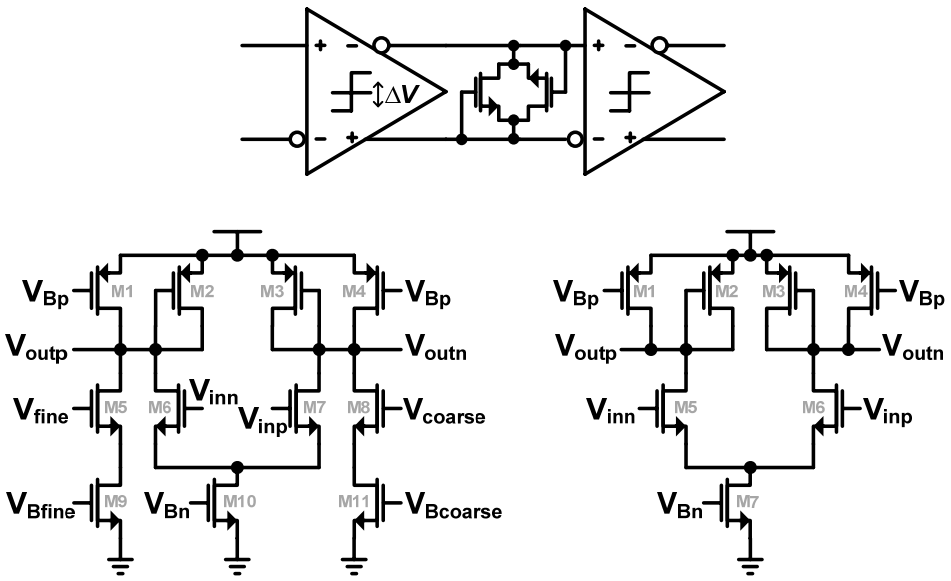


Fig. 3.3.10 Schematic diagram of the (a) the threshold–detection circuit (b) comparator with adjustable threshold voltage (c) amplifier

The comparator is a critical part of the CBSC circuit, and is used to detect the virtual ground voltage accurately. The comparator should change its output as soon as its input crosses the virtual ground voltage. A high-gain comparator is required to reduce the error in the conventional design. To get the high gain comparator, our first work has a three stage cascading configuration [3.3.7]. Figure 3.3.10 is the schematic diagram of the threshold–detection circuit and presents a detailed comparator circuit with adjustable threshold voltage. The outputs of the first stage of the comparator are connected by two MOS diodes to reduce the conversion time, and the outputs of the final stage are buffered with inverters to drive logic circuits which control the current sources.

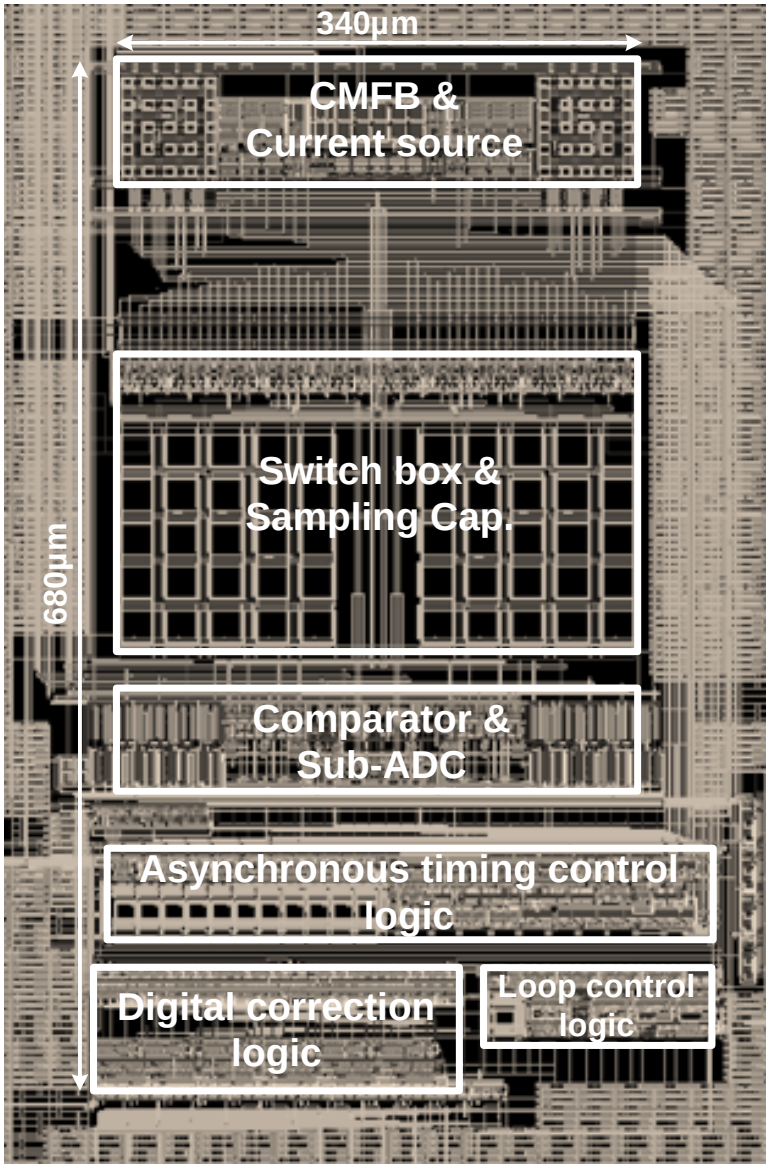


Fig. 3.3.11 Layout of proposed cyclic ADC

3.3.4 SIMULATION RESULTS

The proposed circuit was fabricated in 0.18μm CMOS technology and provided with a 1.8V supply voltage. Figure 3.3.11 shows a layout of the proposed cyclic ADC, which has an area of 0.23mm^2.

Table 3.3.2 summarizes the performance of the proposed asynchronous cyclic ADC. Operating at a 3MHz sampling rate, with a $1V_{P-P}$ range, it consumes 1.6mW at the supply voltage of 1.8V.

As shown in Fig. 3.3.12, at a 3MS/s conversion rate, the signal-to-noise and distortion ratio (SNDR) and the spurious-free dynamic-range (SFDR) are 64.9 dB and 69.7 dB near the Nyquist-rate sinusoidal input.

Table 3.3.2. Performance summary

Parameter	Value
Supply voltage	1.8V
Technology	0.18 ㎛ 1P6M CMOS
Resolution	12-bit
Sampling frequency (Clock frequency)	3MHz (18MHz)
Input range	$1V_{P-P}$
SNDR	64.9 dB (f_{in}=1.41MHz)
SFDR	69.7 dB (f_{in}=1.41MHz)
Power consumption (w/o I/O power)	1.6mW
Chip size	0.23mm^2

The Figure of Merit (FoM) is plotted in Figure 3.3.13. The FoM is used as an equation 3.3.1.

$$FoM = \frac{power}{F_S \cdot 2^{ENOB}} \tag{3.3.5}$$

Table 3.3.3 shows the comparison with other reported cyclic ADCs [3.3.1-3.3.7]. Our ADC has the lowest FoM of 368fJ/cs and achieves an SNDR of 65dB.

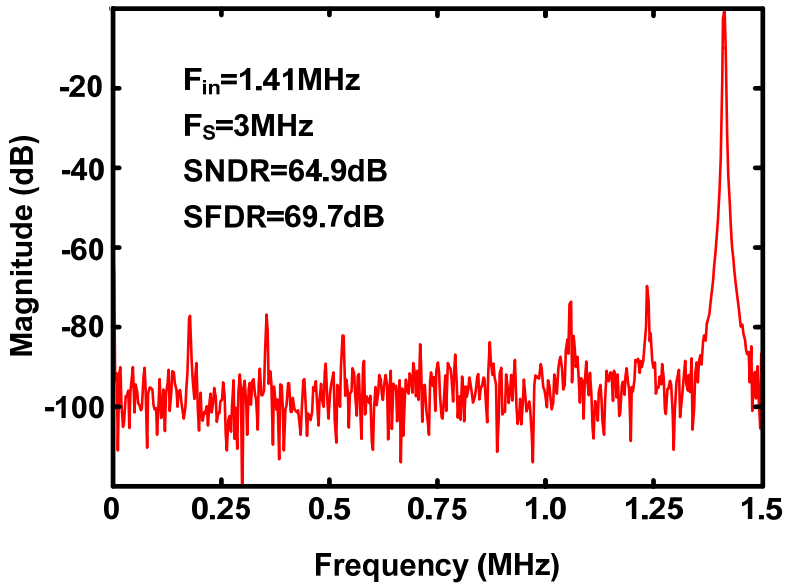


Fig. 3.3.12 FFT plot at a sample rate of 3MS/s

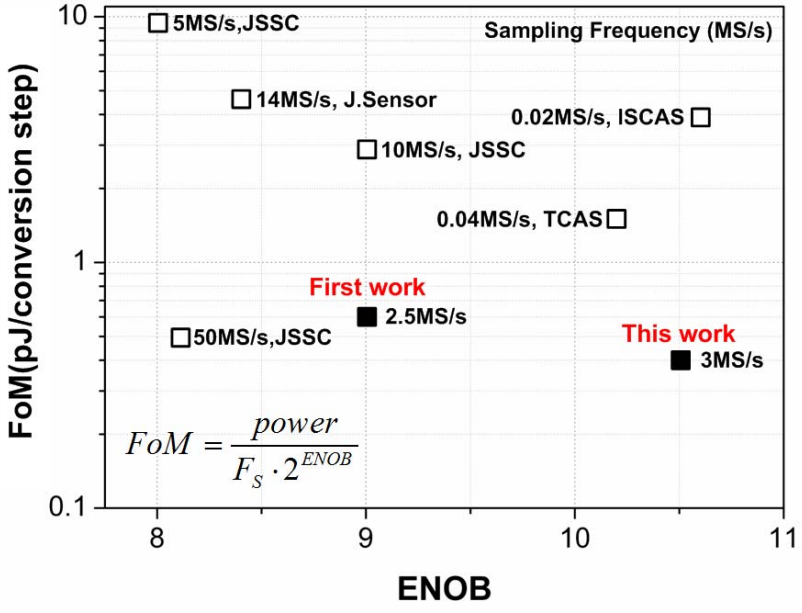


Fig. 3.3.13 FoM comparison with other reported cyclic ADCs

Table 3.3.3. Comparison with other reported cyclic ADCs

	08'TCAS1	***09'J.Sensor***	***10'ISCAS***	***05'JSSC***
Resolution	12	10	13	12
Technology(nm)	130	180	180	180
Sampling Frequency(MS/s)	0.04	14	0.02	5
SNDR(dB)	63.3	52.4	65.4	50
Supply(V)	1.8	3.3	1.8	0.9
Power(mW)	0.07	21.6	0.12	12
Area(mm^2)	0.04	0.38	0.06	1.4
FoM(fJ/C.S)	1465	4530	3943	9289

	09'JSSC	***10'JSSC***	***Fist Work***	***This work***
Resolution	11	9	10	12
Technology(nm)	130	90	180	180
Sampling Frequency(MS/s)	10	50	2.5	3
SNDR(dB)	56	50.5	56	65
Supply(V)	3	1	1.8	1.8
Power(mW)	15	6.9	0.74	1.6
Area(mm^2)	0.24	0.02	0.15	0.23
FoM(fJ/C.S)	2910	504	578	368

3.3.5 SUMMARY

In this paper, we describe an asynchronous cyclic ADC that adopts the comparator-based switched-capacitor (CBSC) technique so as to compensate for the technology scaling and reduce power consumption by eliminating the need for high gain op-amps. An input tracking boosted preset voltage and asynchronous clocking scheme are also introduced to improve the conversion rate without consuming more power. The offset control technique for comparator, which can reduce undesirable undershooting and overshooting of the residue signal, enhances both resolution and sampling rate. The ADC operates at 3MS/s, and near the Nyquist-rate, the proposed ADC has a signal-to-noise and distortion ratio (SNDR) of 64.9dB and a spurious-free dynamic-range (SFDR) of 69.7dB. The chip was fabricated in 0.18μm CMOS and it has an active area of 0.25mm^2 and consumes 1.6mW from a 1.8V supply.

CHAPTER 4

CONCLUSIONS

I have presented a low-power referenceless clock and data recovery circuit for optically controlled neural interface system. Also, I have introduced low-power cyclic analog data converters for recording of multi-channel in neural interface system.

In the study, for optically controlled neural interface systems, a low-power referenceless CDR adopting clock-edge modulation and a voltage-controlled oscillator based on a relaxation oscillator is designed and validated in 0.18μm standard CMOS technology. The CDR circuit is one of the most power-consuming blocks in the neural interface system. I focused on the power-efficiency and the area of the CDR. Our CDR has an input data-rate of 200kbps to 10Mbps when the supply voltage is 0.7V, and operates at up to 24MHz with a supply voltage of 1.0V. The bit error-rate of our CDR is lower than 10^{-13}. The energy per bit is only 0.8pJ/bit, even though the circuit is implemented in a 0.18μm CMOS technology.

Among various ADC architectures, SAR ADCs have been considered to have the

most power efficient architecture for such conversion rates. However, the silicon area of the SAR ADC is significantly large because of the design consideration of mismatch requirement. On the other hand, the cyclic ADC achieves high resolution with small chip area and low power, because it performs a conversion cyclically by repeated use of a single gain stage.

In the study, I have presented two types of cyclic ADCs which are 10-bit cyclic ADC with a boosted preset voltage scheme and a 12-bit asynchronous cyclic ADC with three proposed methods for enhancing the resolution and the conversion rate.

Our first prototype which is a 10-bit cyclic ADC adopts the comparator-based switched-capacitor (CBSC) technique, for the first time, so as to compensate for the technology scaling and to reduce power consumption by eliminating the need for high gain op-amps. A boosted preset voltage is also introduced to improve the conversion rate without consuming more power.

The ADC operates at 2.5MS/s, and near the Nyquist-rate, a prototype has a signal-to-noise and distortion ratio (SNDR) of 55.99 dB and a spurious-free dynamic-range (SFDR) of 66.85 dB. The chip was fabricated in 0.18μm CMOS and it has an active area of 0.146mm2 and consumes 0.74mW from a 1.8V supply.

A second proposed 12-bit cyclic ADC with CBSC adopts the multi-level input tracking boosted preset voltage scheme, asynchronous clocking scheme and adjustable threshold voltage in comparator.

The multi-level input tracking preset voltages scheme can achieve shorter coarse conversion time than the conventional one. Moreover, by reusing the sub-ADC in the MDAC, the proposed input tracking preset voltages scheme does not needed additional circuits. An asynchronous clocking scheme only synchronizes the sampling signal. After the end of the conversion time, sleep mode is maintained until the next signal of sample and helps reduce the power consumption because the current source and comparator are power down. The scheme of adjustable threshold voltage in the comparator reduces the coarse conversion time. Moreover, the overshoot is reduced which means that the fine conversion time is also shortened.

The ADC operates at 3MS/s, and near the Nyquist-rate, the simulation results of the proposed cyclic ADC has a signal-to-noise and distortion ratio (SNDR) of 64.9dB and a spurious-free dynamic-range (SFDR) of 69.7dB. The chip was designed in 0.18μm CMOS and it has an active area of 0.23mm^2 and consumes 1.6mW from a 1.8V supply.

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한글 초록

본 연구에서는 생체 의학용 시스템에 적합한 클럭 데이터 복구 회로와 아날로그 데이터 변환 회로를 제안하고 표준 CMOS 공정으로 그 회로를 구현하고 검증하였다.

신호 획득, 증폭, 필터링, 아날로그 데이터 변환 및 자극 작업을 수행 하는 생체 의학용 시스템은 전력소모, 칩 사이즈, 그리고 제한된 포트 수 등과 같은 엄격한 제한 조건을 만족 해야 한다. 우선 전력 소모에 비례하여 회로에서 발행 하는 열이 세포 조직을 손상시킬 수 있어 낮은 전력 소모는 매우 중요한 고려 사항이다. 또한 배터리를 통하여 전력을 공급 받는 생체 의학용 시스템의 경우에는 작은 전력 소모가 배터리 크기를 줄일 수 있는 요인으로 작용한다. 다음으로, 이러한 활용 분야에서는 칩 사이즈가 생체 내부의 이식 적합성을 향상 시키기 위하여 그 크기가 작아야 하는 제약 조건을 갖고 있다.

본 연구에서는, 광학적으로 컨트롤 할 수 있는 뉴럴 인터페이스 시스템을 위한 외부 클럭이 필요 없는 저 전력 클럭 데이터 복원 회로를 0.18μm CMOS 공정을 이용하여 구현하고 검증하였다. 제안된 회로는 릴렉세이션 오실레이터

를 이용한 전압 조정 발진기와 클럭 에지 모듈레이션 기법을 사용하였다. 클럭 데이터 복원 회로는 시스템에서 파워 소모가 가장 많은 블록 중에 하나이다. 제안한 클럭 데이터 복원 회로는 파워 효율과 면적에 중점을 두고 설계하였다.

제안한 클럭 데이터 복원 회로는 전원 전압이 0.7V일 때 입력 데이터 속도가 200kpbs 에서 10Mbps까지 정상 동작 하였고, 전원 전압이 1V일 때 입력 데이터 속도가 24Mbps까지 동작한다. 클럭 데이터 복원 회로의 비트 에러 레이트는 10^{-13}보다 낮다. 또한 제안된 클럭 데이터 복원 회로는 입력 데이터 속도가 10Mbps일 때 8μW의 전력을 소모하며 한 비트 당 에너지 소비량은 0.8pJ/bit을 갖는다.

여러 아날로그 데이터 변환기 구조 중에서 SAR 아날로그 데이터 변환기(SAR ADC)가 전력 소모면에서 가장 효과적이라고 알려져 있지만, 입력 커패시터의 불일치의 조건을 만족하기 위하여 면적이 크다는 단점을 가지고 있다. 반면 cyclic 아날로그 데이터 변환기(cyclic ADC)는 한 개의 이득 스테이지(gain stage)를 반복적으로 사용하는 구조 때문에, 작은 면적과 낮은 소모전력으로 고해상도를 얻을 수 있다.

본 연구에서는, 두 개의 사이클릭 아날로그 데이터 변환기를 제안하였다. 첫 번째 프로토 타입에서는, 10비트 사이클릭 아날로그 데이터 변환기에 처음

으로 비교기 기반 스위치 축전기 기술을 적용하였다. 전력 소모가 많은 높은 이득을 갖는 op-amps 대신 비교기 기반 스위치 축전기 기술을 사용함으로써 공정 스케일에 따른 어려움을 보안하였고 전력 소모를 줄였다. 또한 제안하는 사이클릭 아날로그 데이터 변환기는 증가된 프리셋 전위방법을 사용하여 추가적은 전력 소모 없이 변환 속도를 향상 시켰다. 0.18μm CMOS 공정으로 제작된 사이클릭 아날로그 데이터 변환기는 입력 샘플링 속도가 2.5MS/s 일때, 55.99dB의 SNDR과 66.85의 SFDR 값을 갖는다. 그 칩 크기는 0.146mm^2 이고 전원전압이 1.8V 일 때 0.74mW 전력을 소모한다.

두 번째 제안된 사이클릭 아날로그 데이터 변환기는 입력을 추적하는 증가된 프리셋 전위 방법, 비동기식 클럭 구동 방법 그리고 오프셋 조절 가능한 비교기를 제안하고 적용하였다.

입력을 추적하는 증가된 프리셋 전위 방법은 sub-ADC를 재사용 함으로서 추가적인 회로 없이 변환 속도를 높였다. 비동기식 클럭 방법은 오직 샘플링 신호에만 동기가 되어 있어, 변환이 끝난 이후에는 주변회로의 전류를 사용하지 않는 슬립 모드로 전환하여 전력 소모를 줄었다. 마지막으로 오프셋 조절이 가능한 비교기는 coarse 변환 시간과 오버 슛 전압을 줄여준다. 오버 슛 전압이 줄었다는 것은 fine 변환 시간 줄었다는 것을 의미하며, 이는 전체 아날로그 데이터 변환기의 변환 시간이 줄었다는 것을 나타낸다. 0.18μm CMOS 공정으로 설계된 12비트 사이클릭 아날로그 데이터 변환기는 입력 샘플링 속도

가 3MS/s 일때, 64.9dB의 SNDR과 69.7의 SFDR 값을 갖는다. 그 칩 크기는 0.23mm^2 이고 전원전압이 1.8V 일 때 1.6mW 전력을 소모한다.

주요어: 생체 의학용 장치, 클럭 데이터 복원 회로, 사이클릭 아날로그 데이터 변환기, 비교기 기반 스위치 축전기.

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