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Power Conversion Efficiency Optimization for Mobile Systems with Dynamic Voltage Scaling Enabled OLED Displays

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abstract

Modern mobile devices such as smartphone or tablet PC are typically equipped a high-performance CPU, memory, wireless interface, and display. As a result, their power consumption is as high as a small-size laptop computer. The boundary between the mobile devices and laptop computer is becoming unclear from the perspective of the performance and power. However, their battery and related power conversion architecture are only designed according to the legacy design so far. Smartphone and tablet PCs from major vendors such as iPad from Apple or Galaxy-tab from Samsung uses 1-cell Li-ion battery. The laptop PC typically has 3-cell Li-ion battery. The output voltage of the battery affect system-level power conversion efficiency.

Furthermore, traditional power conversion architecture in the mobile computing system is designed only considering the fixed condition where the system-level low-power techniques such as DVFS are becoming mandatory. Such a low-power techniques applied to the major components result in not only load demand fluctuation but also supply voltage changing. It has an effect on the battery lifetime as well as the system-level power delivery efficiency. The efficiency is affected by the operating condition including input voltage, output voltage, and output current. We should consider the operating condition of the major power consumer such as a display to enhance the system-level power delivery efficiency. Therefore, we need to design the system not only from the perspective of the power consumption but also energy storage design. The optimization of battery setup considering battery characteristics was presented in [1].

Beside the DVFS of microprocessor, a power saving technique based on the supply voltage scaling of the OLED driver circuit was recently introduced [2]. An organic light emitting diode (OLED) is a promising display device which has a lot of advantages compared with conventional LCD, but it still consumes significant amount of power con-

sumption due to the size and resolution increasing. The OLED dynamic voltage scaling (OLED DVS) technique is the first OLED display power saving technique that induces only minimal color change to accommodate display of natural images where the existing OLED low-power techniques are based on the color change. The OLED DVS incurs supply voltage change. Therefore we need to consider the system-level power delivery efficiency and battery setup to properly integrate the DVS-enabled OLED display to the system.

In this dissertation, we not only optimize the power consumption of the OLED display but also consider it's effect on the whole system power efficiency. We perform the optimization of the battery setup by a systematic method instead of the legacy design rule. At first, we develop an algorithm for the OLED DVS for the still images and a histogram-based online method for the image sequence with a hardware board and a SoC. We characterize the behavior of the OLED DVS. Next, we analyze the characteristics of the smartphone and tablet-PC platforms by using the development platforms. We profile the power consumption of each components in the smartphone and power conversion efficiency of the boost converter which is used in the tablet-PC for the display devices. We optimize not only the power consuming components or the conversion system but also the energy storage system based on the battery model and system-level power delivery efficiency analysis.

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1 Introduction

1.1 Supply Voltage Scaling for OLED Display

Display systems are primary sources of power consumption in battery-powered electronics despite the advances in low-power display technologies. As of today, liquid crystal display (LCD) panels are widely used in portable as well as desktop systems. The LCD panels do not illuminate themselves and require a high intensity backlight, which generally consumes a significant amount of power due to low transmittance of the LCD panels [3, 4]. On the other hand, an organic light emitting diode (OLED) is self-illuminating using organic light emission material. Therefore, OLEDs should provide higher brightness, higher luminance, faster response, wider viewing angle, and thinner and lighter-weight form factors compared with conventional LCD panels [5]. One of the known major disadvantages of OLED panels was their relatively short lifetime, which has been enhanced to be commercialized. However, the power efficiency of the OLED panels is not as high as expected due to serious total internal refection. As a result, most OLED smartphone users do not really feel extended battery life from the OLED display.

There have been extensive efforts to reduce the OLED panel power consumption. Most previous work attempted aggressive dimming of a part of the panel to reduce power consumption because the OLED power consumption is directly dependent on the pixel color. As red, green, and blue colors show distinctly different power efficiency, color swapping was also proposed. We summarize the previous work in Section 2.

In this dissertation, we implement and verify the OLED dynamic voltage scaling (OLED DVS). We dynamically change the supply (driving) voltage of the OLED panel in a prototype implementation and measure the power saving. The prototype equips pulse-width modulation (PWM) driver-based OLED display panel, and we develop a

SoC which enables online image processing and supply voltage changing. We develop an online method based on the luminance histogram and histogram optimization by luminance quantization. For the amplitude modulation (AM) driver-based panel, we show the effect of the OLED DVS by panel-level SPICE simulation.

1.2 Power Conversion Efficiency in Mobile Systems

The power saving technique in each component does not guarantee meaningful system-level power saving. OLED DVS-enabled system should equips output voltage adjustable DC-DC converter to supply the appropriate voltage to the display panel. The voltage-adjustable converter requires additional devices, and the added control logic and devices bring power overhead. We should consider the effect of the system modification to properly integrate the DVS-enabled display in the system. By extension, we examine the validity of the existing system setup, and develop a framework to properly design the system from the power source to the power consumption.

Modern mobile devices such a smartphone or tablet PC are typically equipped with a multi-core gigahertz processor, gigabytes of high-speed DDR SDRAM, dozens of gigabytes of flash memory, several up to 10 megapixel cameras, 1M+ pixel high-resolution color display, high-power audio, as well as 3G/4G, Wi-Fi and Bluetooth wireless communication devices. As a result, modern mobile devices suffer from the short battery lifetime. As reported in [6], average power conversion efficiency in the smartphone is around 60% to 70%. It is a surprisingly low value. There has been numerous effort on the development of low-power techniques from transistor-level to system-level. However, if we cannot enhance the power delivery efficiency, even cutting-edge low-power techniques cannot significantly increase the battery lifetime. Power delivery efficiency should be considered to extend the battery lifetime.

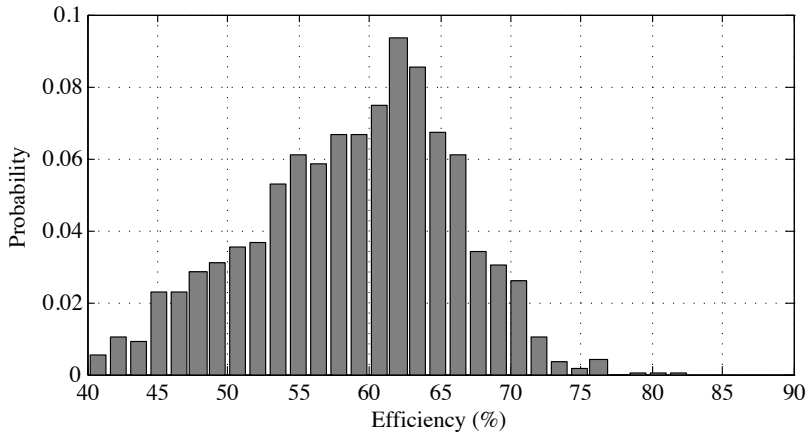


Figure 1: Average power efficiency for different input voltage with the same benchmark.

It is well known that the efficiency of the voltage converters are dependent on its input/output voltage and current. A Switching converter consumes part of input power to switch the MOSFET switches, and power dissipation by parasitic resistance in the MOSFET switches and passive devices such as an inductor cannot be ignored. Those power losses are dependent on the input/output voltage and current. Furthermore, power loss in a linear regulator is proportional to the voltage difference and current through the regulator. Therefore, the voltage converters should be carefully designed according to its operating condition, and input voltage from the battery also should be carefully selected.

1.3 Research Motivation

We measure the power consumption of the smartphone platform by using Snappdragon MDP from Quallcomm. For the experiment, we develop a benchmark which is designed to sequentially enable the system components in the platform and change the operating

status. Figure 1 shows the result of efficiency profiling. System level power efficiency is about 60 %. It is quiet low value beyond common expectation while the efficiency of the commercial DC-DC converters are known be higher than 90 %. The switching-mode DC-DC converters shows high efficiency only when they are appropriately integrated to the system. Their efficiency is strongly dependent on the operating condition including input/output current and voltage.

So far, a lot of efforts have been dedicated to reduce the power consumption of the components such as the CPU and display because it is believed that their power consumption is the key factor to reduce the system-level power consumption. However, if the system level power delivery efficiency is around 60 %, the power converter is the most power consuming component than any other component. We should enhance the system-level power delivery efficiency to extend the lifetime of the system.

The average power conversion efficiency is affected by the difference between the input and output voltage of the system. Figure 2 shows that the average efficiency of the Snapdragon MDP with the different input voltage. We connect the programmable power supply to the battery input socket to measure the efficiency with the different input voltage. The maximum voltage in the Snapdragon MDP is 3.8 V which is supplied to the ELVDD net of the LCD panel. Therefore, every voltage conversions in the platform is a step-down (buck) conversion, and the voltage difference between the input and output of the conversion is increasing as the battery input voltage is increasing. Figure 2 mostly shows that the overall conversion efficiency is decreasing as the difference between the input and output voltage is increasing.

The major power consumer in the smartphones are an application processor (AP), wireless interfaces, and display. Modern AP and wireless interface ICs accepts lower than 3.3 V input. Therefore, from the perspective of the power delivery efficiency, it is

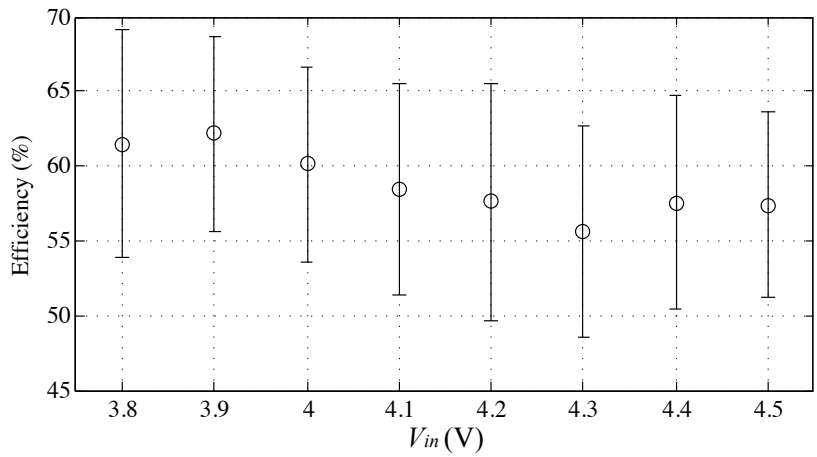


Figure 2: Average power efficiency for different input voltage with the same benchmark.

better to supply the input voltage to the converter as low as possible according to the observation presented in Figure 2. However, unfortunately, the display devices generally requires much higher voltage than the silicon devices in the system. LCDs and OLED displays commonly accept 12 V or higher voltage to illuminate themselves. Their input voltage is determined by the electrical and optical characteristics of the display cell elements and light source. For instance, an Odroid-A platform from Hardkernel, which is a development platform targeting the Galaxy tab from samsung, equips a LP101WH1 1366 x 768 TFT LCD panel [7]. The LP101WH1 consumes ?? mW on average, and it requires 12 V as a input. Several OLED display panel modules accept 3.7 V (1-cell Li-ion battery) as an input [8], but it internally boosts the input voltage by using the charge pumps to generate the input voltage to the OLED cells.

The battery setup should be determined under the consideration of the effect of the battery voltage on the overall system power efficiency. To derive the optimal setup,

We need to consider the power delivery efficiency of the system components and behavioral characteristics of the components. However, the smartphones and tablet PCs are designed only by a legacy design rule so far. Smartphones and tablet PCs from major vendors such as Apple or Samsung uses 1 cell Li-ion battery while the laptop PC typically have 3 cell Li-ion battery. Especially, modern tablet PCs which equip a several GHz multi-core processor and up to 10" size high-resolution display still use 1 cell battery because of the legacy design rule and compatibility issues though its hardware is close to Laptop PC rather than smartphone. It is time to examine the effectiveness of the legacy design rule.

In this dissertation, we introduce a systematic approach to design the power delivery architecture considering the behavioral characteristics of the system. We introduce an estimation model power conversion efficiency based on the system activity analysis. Based on the model, we maximize the power delivery efficiency by changing the battery setup. We also consider the internal characteristics of the batteries to optimize the battery setup.

Table 1: Classification of display power saving techniques.

Techniques	Applicable devices	Applicable images
Backlight control-based	LCD	Natural image
User behavior-based	LCD, OLED	Interactive applications
Clock and frame rate control	Display controller	Natural image
Frambuffer compression	Framebuffer memory	GUI
OLED cell pre-charging	OLED	Natural image
Color remapping	LCD, OLED	GUI

2 Related Work

2.1 Low-Power Techniques for Display Devices

Display systems account for a significant portion of the total power consumption in battery-powered electronics despite the advances in low-power display device technologies. As of today, liquid crystal display (LCD) panels are widely used in portable as well as desktop systems. The LCD panels do not illuminate themselves and require a high intensity backlight which generally consumes a significant amount of power due to low transmittance of the LCD panels. On the other hand, an organic light emitting diode (OLED) is a self-illuminating device using organic light emission material. Therefore, OLEDs provide high brightness, high luminance, fast response, wide viewing angle, and thin and lightweight form factors compared with conventional LCD panels. Despite of the technological advances, OLED display is still one of the major power consumer in the system. In this section, we will introduce and categorize the low-power techniques for display devices related with the proposed method.

We categorize the system-level low-power techniques for displays as shown in Table 1. The backlight control-based approaches can reduce the power consumption of the light source without image distortion.however, unfortunately, it is not applicable to self-illuminating display devices such as the OLED panels. The user behavior-based approaches are too complex to be implemented in the portable electronics because it requires dedicated hardware and software-level support. Architectural approaches also has some limitations. Variable dot clock and frame refresh rate control cannot reduce the power consumption of the light source, and the framebuffer compression is hard to apply for the natural images. We can save the wasted energy by the cell pre-charging, but we cannot reduce the energy to illuminate the cell itself. The color remapping is effective low-power technique for the OLED display, but is not always feasible. It is applicable only to the graphics user interface (GUI) and applications not dealing with natural images, photos, or video.

There exist no OLED display power saving technique that reduce the power consumption of the light source without the distortion of the displayed image. We need to reduce the power consumption of the light source because it is the biggest power consumer in the display system. We can access the light source of the LCD panel, the backlight, but we do not have a method to access the light source of the OLED display, the OLED cell, without changing the color. This is because of the nature of the OLED panel. The power consumption of an OLED panel is dependent on each pixel color value and, in therefore, existing OLED power management techniques are not capable of altering power consumption of the OLED panel, without changing the pixel color values.

This research aims at developing the first OLED power saving technique that overcomes the above limitations. We call the technique OLED dynamic voltage scaling (DVS). The proposed technique exploits the unique characteristics of the OLED driver

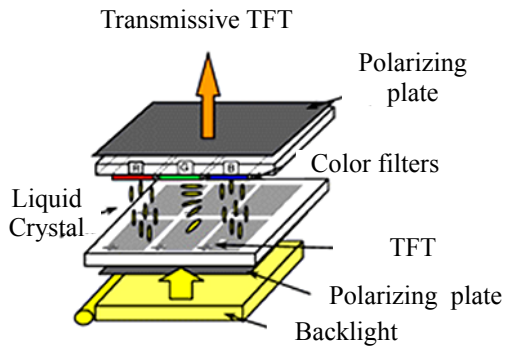


Figure 3: Vertical structure of thin-film transistor LCD panel [3].

circuits. The OLED panel requires a controllable supply current driver circuit for each OLED pixel. Generally, the supply voltage of an OLED driver circuit is set to the maximum value to support the full luminance of a pixel. However, the supply voltage of pixels with less luminance does not need to be the maximum, and thus it has some margin for supply voltage reduction. We define a headroom as the difference between the actual supply voltage and the required voltage to illuminate the pixel with a given luminance. If we decrease the supply voltage, the luminance of pixels will decrease. Fortunately, if the scaled voltage is within the headroom of the pixel, we can restore it by increasing the brightness of the image data.

2.1.1 Light Source Control-Based Approaches

The most effective way to reduce the power consumption is to control the light source. We can find several low-power techniques which involve change of the backlight luminance, brightness, and contrast of the image to reduce the power consumption without the image quality degradation.

A dynamic luminance scaling of the backlight with appropriate image compensation was introduced in [3, 4]. The liquid crystal display (LCD) panel does not illuminate itself, but it filters light from the light source from the rear of the LCD panel as shown Figure 3 A reflective LCD uses ambient light as the light source of the LCD so as to eliminate the power-greedy backlight lamp. Instead, it has a reflector to reverse the direction of the ambient light from the front. However, reflective LCDs do not offer a quality display. Transflective LCDs are compromises between transmissive and reflective designs but are usually operated with the backlight on. Backlight systems dominate the power requirements of battery-operated hand-held devices with color thin-film transistor (TFT), LCDs.

Dynamic backlight luminance scaling (DLS) keeps the perceived intensity or contrast of the image as close as possible to the original while achieving significant power reduction. DLS compromises quality of image between power consumption, which fulfills a large variety of user preferences in power-aware multimedia applications. DLS saves 20% to 80% of power consumption of the backlight systems while keeping a reasonable amount of image quality degradation. Figure 4 show the behavioral concept of the DLS. The backlight luminance is decreased (a) to (b), at the same time, the image data is shifted from (c) to (d). Consequently, scaled image (f) conserve the original luminance of (e) with some saturated pixels.

A Concurrent Brightness and Contrast Scaling (CBCS) technique for a cold cathode fluorescent lamp (CCFL) backlit TFT-LCD display was introduced in [9, 10]. The proposed technique aims at conserving power by reducing the backlight illumination while retaining the image fidelity through preservation of the image contrast. Figure 5 show the behavioral concept of the DLS. The proposed technique is based on the non-linear model between its backlight illumination and power consumption. The contrast distor-

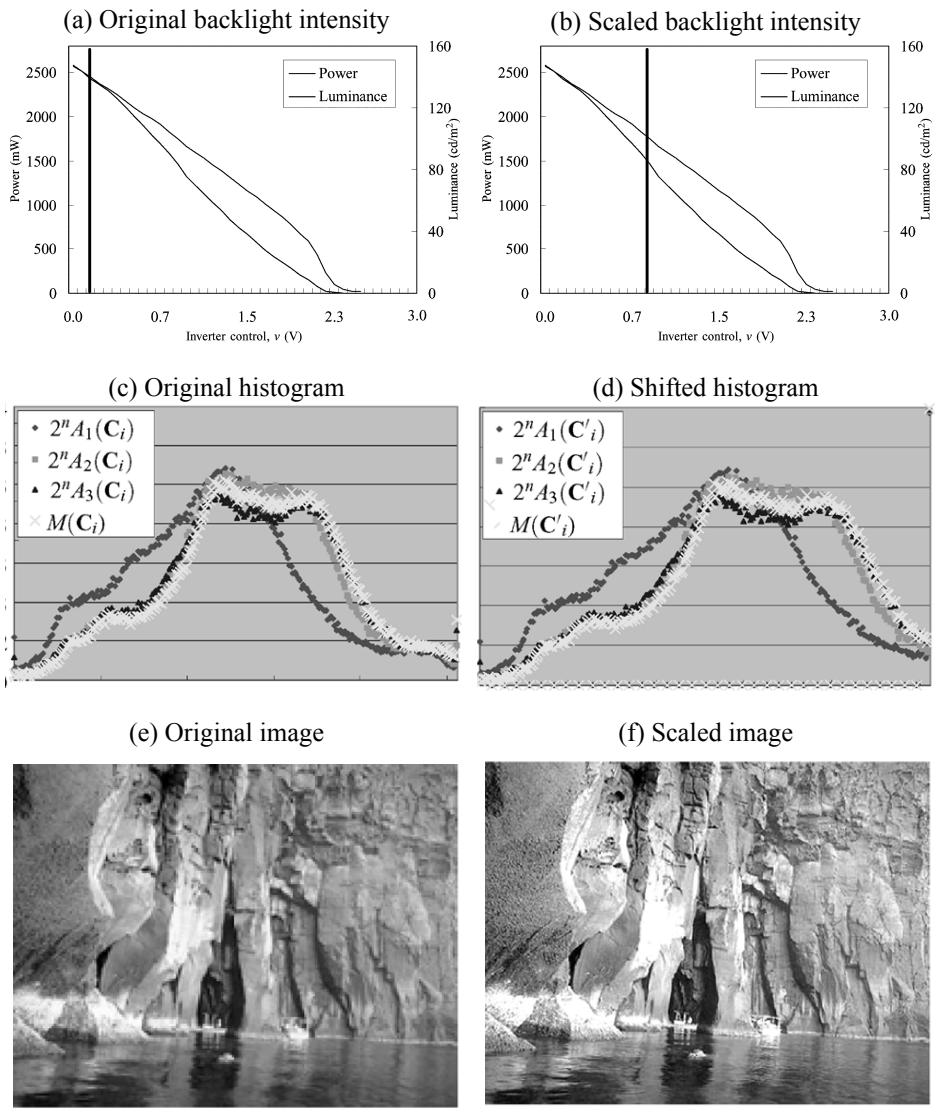


Figure 4: Dynamic backlight luminance and image compensation [4].

Figure 5: A concurrent sontrast and brightness scaling [9].

tion metric is also proposed to quantify the image quality loss after backlight scaling. The solution for the CBCS optimization problem subject to contrast distortion shows that an average of 3.7X power saving can be achieved with only 10% of contrast distortion.

The partial control techniques for the light source device are introduced in [11, 12]. They attempt partial display turnoff. Some LCD panels have a zoned backlighting system, which can be partially turned off or dimmed. One such technique selectively turns off or dims the backlights that do not illuminate any displayed object of interest to the user [11]. Background dimming techniques set the background colors to a dark color, which results in lower power consumption in OLED panels [12].

A 1-D LED backlight scanning and a 2-D local dimming technique for large LCD TVs are presented in [10]. These techniques not only reduce the motion blur artifacts by means of impulse representation of images in video but also increase the static contrast ratio by means of local dimming in the image(s). Both techniques exploit a unique

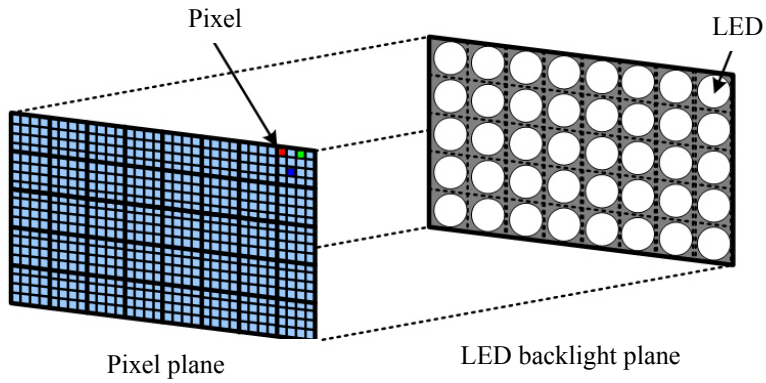


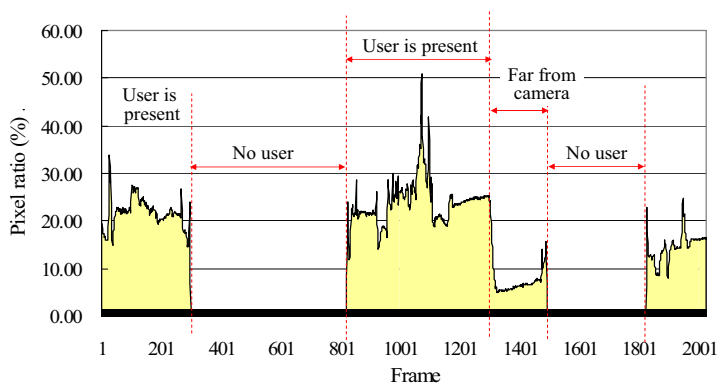
Figure 6: A structure of LCD panel with LED backlight [10].

feature of LED backlight in large LCD TVs as shown in Figure 6 in which the whole panel is divided into a pre-defined number of regions such that the luminance in each region is independently controllable. The proposed techniques are implemented in a Xilinx FPGA and demonstrated on a Samsung 40-inch LCD TV. Measurement results show that the proposed techniques significantly reduce the motion blur artifacts, enhance the static contrast ratio by about 3X, and reduce the power consumption by 10% on average.

2.1.2 User Behavior-Based Approaches

Observing the behavior of the user to obtain the clue for the power reduction is an effective way. A face detection techniques and user input behavior analysis are also used to find the intention of the user [13, 14]. The proposed method links the display operation to a key press or movement of the mouse. The authors employ a video camera to bind the display power state to the actual attention of the user. The proposed method keeps display active only if its user looks at the screen as shown in Figure 7. When the user detracts his/her attention from the screen, the method dims the display down or even

(a) User face detection



(b)Pixel ratio control

Figure 7: Pre-charging enabled OLED column driver circuit [14].

switches it off to save energy. Experiments show that the method can reduce the display energy significantly in environments which frequently detract the display viewer.

These techniques are applicable to any types of display with an interactive application where the user does not always pay attention to the display. The user behavior-based approaches are an ultimate way to save the wasted energy. However, it is too complex to be implemented in the portable electronics because it requires dedicated hardware and software-level support.

2.1.3 Low-Power Techniques for Controller and Framebuffer

We can find some architectural approaches in the previous studies. Variable dot clock frequency and variable frame refresh rate control techniques are introduced in [15]. Almost LCD power minimization has focused on technology and circuit design. An orthogonal approach, several software-only techniques for LCD dynamic power management, which do not require any hardware changes on existing LCDs and their controllers was introduced. Dot clock can be set to the lower possible frequency until flicker becomes excessive. This setting causes a slowing down of every display signal and, consequently a reduction of power consumption for every component of the display subsystem. This method reduces the system bus time dedicated to the DMA of the LCD controller. Dot clock can be set dynamically by means of a function in the LCD driver that modifies a configuration register. In this case the running programs (or the OS) can set the appropriate refresh frequency so that a simple text editor should use the lowest frequency, while programs where images change quickly can use higher frequencies. This method allows power saving when the image refresh is low and, at the same time it does not limit the use of high-refresh applications.

We can delay refresh until the flicker becomes appreciable, i.e. before the effects

of LCD internal capacitance discharge become noticeable. During this time the LCD controller can be disabled to save power. Instead of slowing down refresh, it is possible to shut down the controller. Power saving is now higher because it is possible to close the communication with the LCD display for long time. Simply disabling via software the LCD controller through the configuration register can do it. In this way power savings are on all LCD controller components. Dedicated DMA transfers are suspended and the screen is not refreshed. This method is viable because liquid crystals can maintain their orientation (and then the image) for a time as long as the discharge of storage capacitance in the active matrix display. Storage capacitance has been introduced for this purpose. During this time, the image persists on the screen varying its luminance according to the discharge of the capacitor.

The power savings of the proposed methods are significant: from 40% (with no perceivable image degradation) to 60% (with significant, but tolerable degradation) of total system power, measured on a prototype wearable system platform. However, the effect of the Variable dot clock frequency and variable frame refresh rate control is limited because the biggest power consumer in the display system is a light source element such as a backlight or an OLED cell. Although, one use lower dot clock frequency or frame refresh rate, the light source element consumes the same amount of the energy as far as the image is not changed.

Another architectural approach is a framebuffer compression method [16]. Due to 60Hz or higher LCD refresh operations, a framebuffer memory is a significant power consumer because it is usually implemented with a high-speed memory such as SDRAM. If we compress the image data in the framebuffer and decompress it before transmitting to the display devices, then we can reduce the data transaction between the framebuffer and the display controller. An efficient frame buffer compression

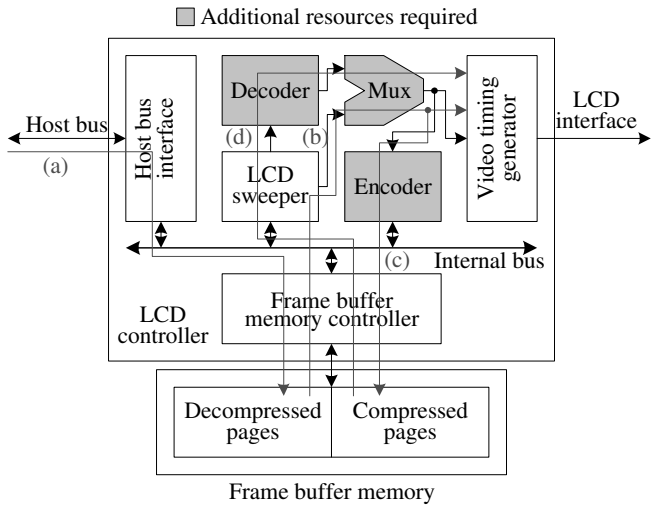


Figure 8: Framebuffer compression architecture [16].

scheme that uses differential Huffman coding and its hardware implementation was introduced. It results in reduced power and bus bandwidth requirement for the image data transmission. The effect of the framebuffer compression is highly dependent on the performance of compression algorithm. The compression and decompression must be simple and not incur distinct power overhead involving no CPU operations. Both on-the-fly compression and high compression efficiency devising a limited-size code book, color-difference reduction techniques and an adaptive code book update scheme was developed. On the MobileMark 2002 benchmark, the proposed techniques reduce the frame buffer activity by 52% to 90%, saving up to 86mW including the overhead.

Unfortunately, we cannot apply complicate compression algorithm such as JPEG due to the power and area overhead. The simple compress algorithm such as run-length encoding is only good for the discrete images. Therefore, the framebuffer compression

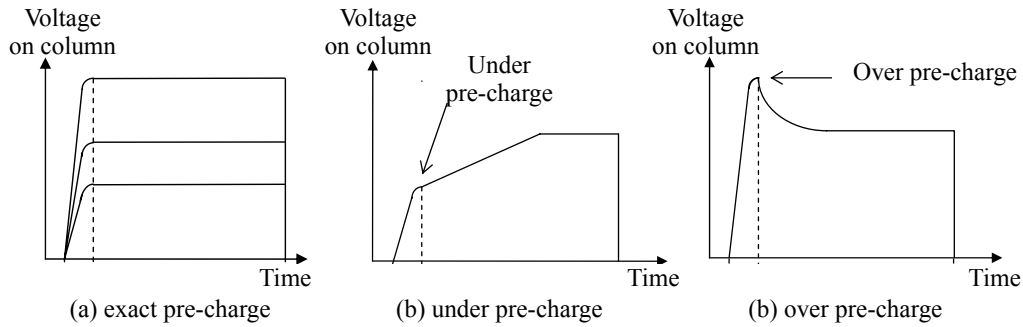


Figure 9: Effect of OLED cell pre-charging [17].

is not suitable for a natural image such as a photo and a movie.

2.1.4 Pre-Charging for OLED

An OLED unit cell has significant parasitic capacitance due to its structural characteristics. This parasitic capacitance causes inrush current as shown in Figure 9 when it is driven. The rush current shorten the lifetime of the cell and reduce the efficiency. OLED cell pre-charging methods are introduced to handle this rush current. We can save the wasted energy by the cell pre-charging, but we cannot reduce the energy to illuminate the cell itself.

Pre-charging enabled driver circuit was introduced in [17]. According to current-luminance characteristics of OLED, the pre-charging module is added on the basis of single constant current source, as shown in Figure 10. In the process of pre-charging, activation signal invalidity, the pre-charging power supply can be used to charge the pixel strongly instead of the operation cell driving power supply , column output the pre-charging current. The pre-charging constant current source is switched to the constant current source which drive normally when the current reaches the luminance threshold

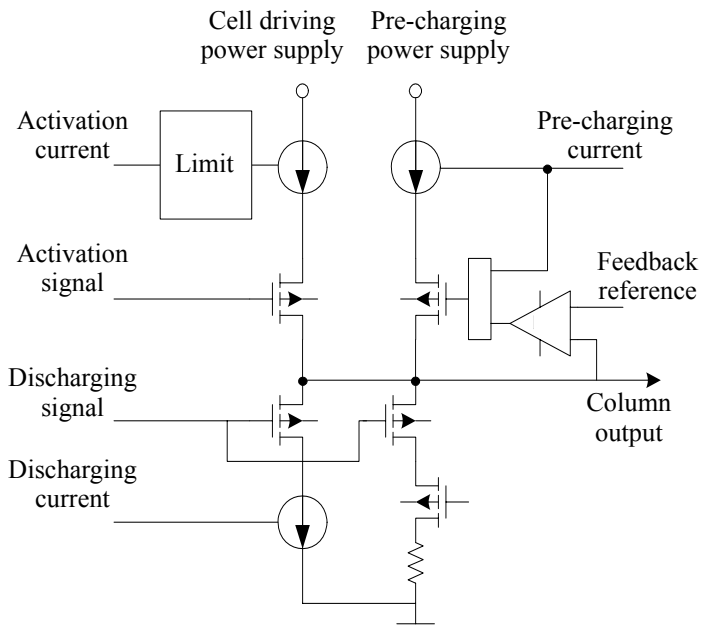


Figure 10: Pre-charging enabled OLED column driver circuit [17].

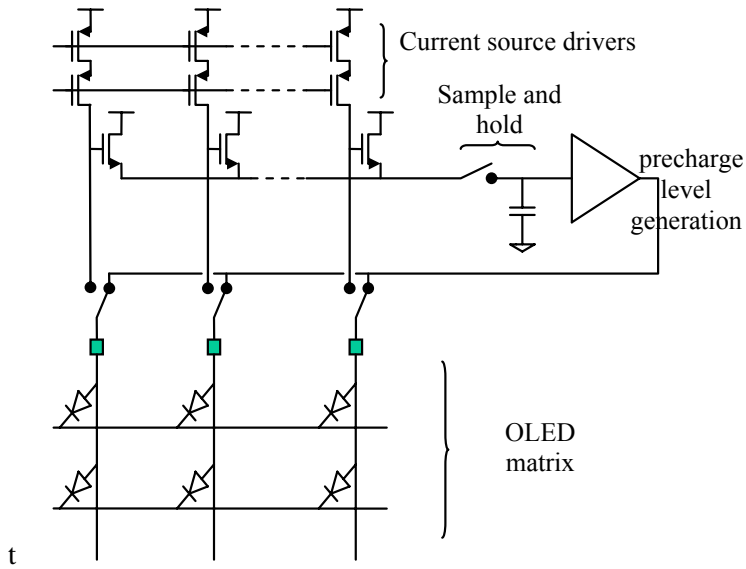


Figure 11: Pre-charging level generation circuit [18].

current which is limited by feedback refernce. The threshold voltage value is lower than theoretical value and can be changed by software to ensure the threshold precision, the pre-charging time is controlled by the drive chip. In the discharge process, discharging current outputs validly, the strong discharge will be applied to OLED pixel cell by the discharge constant current source X3.

A circuit-level method to find exact pre-charging level was introduced in [18]. The proposed IC driver is a passive color OLED controller and driver, which has been specifically designed to fit the application and physical properties of OLED, to simplify adjustments, and to improve the picture quality. Fitted with an automatic pre-charge level generation, the device adapts the voltage of pre-charge to the panel needs, precisely matching its physical characteristics, then increasing the picture quality and avoiding the programming table for pre-charge purposes. Including an on-chip DC/DC converter,

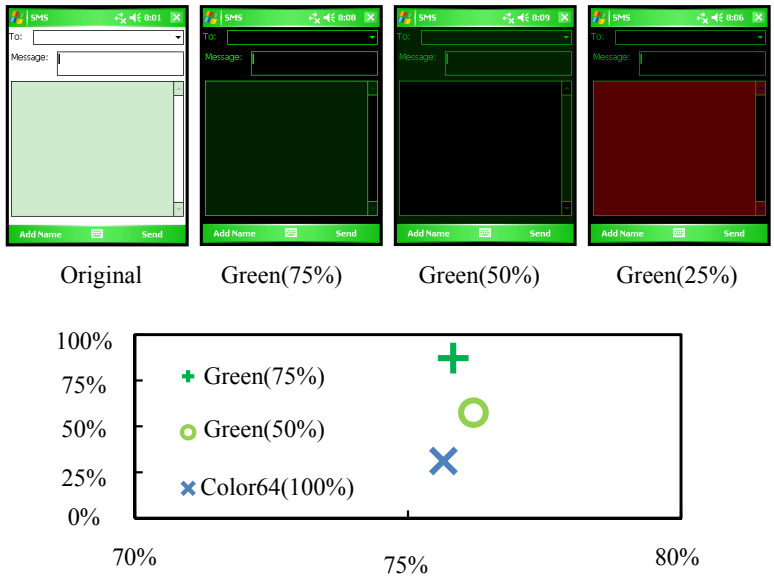


Figure 12: Color remapped GUI image and power reduction [20].

the device automatically maintains the supply voltage on the lower value acceptable for an accurate current drive of pixels, optimizing precision and power consumption.

2.1.5 Color Remapping

We can find image manipulation techniques that attempt content (color) change of the displayed image exploiting the power consumption difference by the pixel colors [19, 20, 21]. LCD panels exhibit around 10% power consumption difference due to change in the colors being displayed [22]. In addition, pixel color remapping provides more headroom for backlight dimming and, in turn, higher power saving [19].

Color remapping also has an big impact on the OLED panel power consumption [20]. OLED-based displays have drastically different power consumption when displaying

different colors, due to their emissive nature. They bring a new opportunity for power saving by transforming the graphics user interface (GUI) colors. A techniques that adapt GUIs based on existing mechanisms as well as arbitrarily under usability constraints was presented. Measurement and user studies show that more than 75% display power reduction can be achieved with user acceptance as shown in Figure 12.

Unfortunately, color remapping is not always feasible. It is applicable only to the GUI and applications not dealing with natural images such as photos or video.

2.2 Battery discharging efficiency aware low-power techniques

Battery models for the electronic systems have extensively been studied during the past few decades. We can find many analytical models based on electrochemical modeling and analysis [23, 24], but the electrochemical battery models are too complicated to be used for the system-level design of electronics. Battery models in the form of an electric circuit are suitable for this purpose [25, 26]. Based on the characteristics of the batteries, several techniques are proposed to enhance the battery discharging efficiency [27, 1].

Supercapacitors are widely used for energy storage in various applications. Specifically, supercapacitors are gaining more attention as electrical energy storage elements for renewable energy sources which tend to have a high charge-discharge cycle frequency, and demand high cycle efficiency and good depth-of-discharge (DOD) properties [28].

There are several related battery-supercapacitor hybrid architectures in the literature on hybrid electric vehicles (HEVs). For example, a bidirectional converter based approach is introduced for the regenerative brake equipped HEVs [29]. A DC power bus based general architecture for the battery-supercapacitor hybrid system is described in [30]. However, it is difficult to directly apply these architectures to portable applications

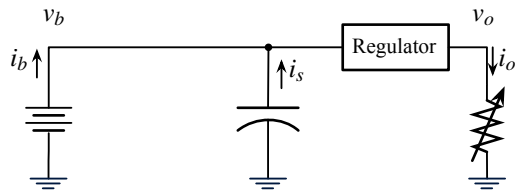


Figure 13: Parallel connection architecture.

because they are designed for the HEV which involve high-power operation. Different from the HEV, many other factors such as size, weight, cost, and circuit complexity must be addressed in portable battery-powered system.

A supercapacitor in parallel with a Li-ion battery forms a hybrid energy storage that supports a higher rate of discharging current thanks to the high power density of the supercapacitor [31], and thus reduces the impact of the rate capacity effect. Under pulsed load conditions, the supercapacitor acts as a filter that relieves peak stresses on the battery. This type of parallel battery-supercapacitor connection storage has been characterized and evaluated by the use of Ragone plots with pulsed load current and compared with the battery-alone systems in [32]. A simplified model, which helps theoretical analysis in terms of performance enhancement of this hybrid storage, is provided in [33]. Duty ratio, capacitor configuration and pulse frequency play important roles in performance optimization of such a hybrid storage [34].

2.2.1 Parallel Connection

A battery-supercapacitor hybrid shown in Figure 13 is an intuitive way of reducing the effect of load fluctuation on the supplied voltage level. The supercapacitor connected in parallel acts as a low pass filter that prunes out rapid voltage changes. The battery-supercapacitor hybrid is thus effective in mitigating the rate capacity effect for intermit-

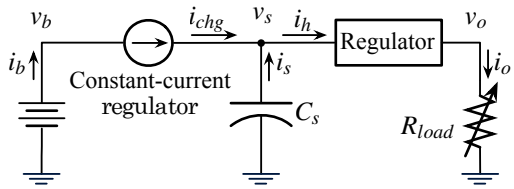


Figure 14: Constant-current regulator-based architecture.

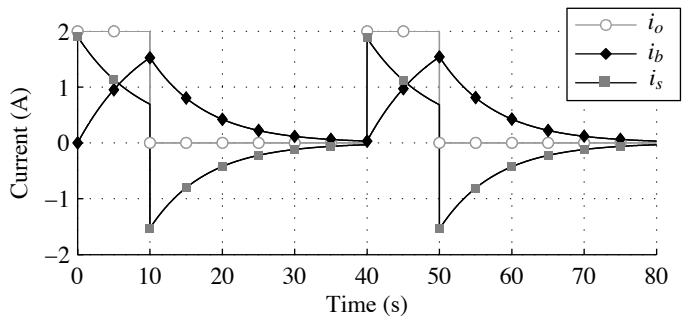
tent (rather than continuous) high load current. The supercapacitor shaves the short duration, but high amplitude load current spikes and makes a wider duration but lower amplitude current, which subsequently results in better energy efficiency due to lower rate capacity effect in the Li-ion batteries.

In the parallel connection configuration, the filtering effect of the supercapacitor is largely dependent on its capacitance. A larger capacitance results in better filtering effect. As a result, the parallel connection has a limited ability to reduce the rate capacity effect in the Li-ion battery when the capacitance value of the supercapacitor is not sufficiently large. Unfortunately, due to the volumetric energy density and cost constraints in its practical deployment, the supercapacitor capacitance is generally rather small.

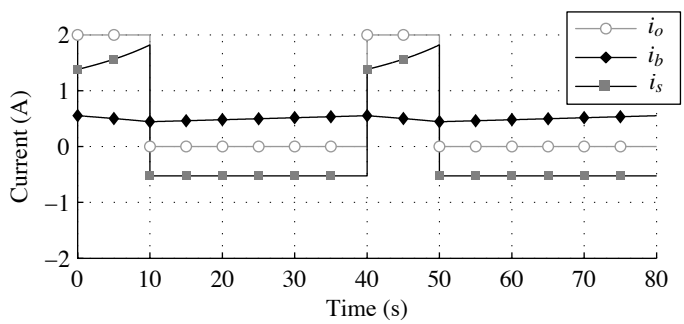
2.2.2 Constant-Current Regulator-Based Architecture

We introduce a new hybrid architecture using a constant-current regulator (cf. Figure 14)to overcome the disadvantage of the conventional parallel connection hybrid architecture. The constant current regulator separates the battery from the supercapacitor.

The supercapacitor in the parallel connection basically reduces the voltage variation, not the current variation. SPICE simulation results reported in Figure 15 show that, in the parallel connection, the battery current exhibits a relatively larger variation than the



(a) Current responses of the battery and supercapacitor to the load current pulse in the parallel connection.



(b) Current responses of the battery and supercapacitor to the load current pulse in the proposed onstant-current regulator-based architecture.

Figure 15: Current response of the constant-current regulator-based architecture with pulsed load.

battery voltage. In particular, as the load current (i_o) changes from valley to peak, the battery discharging current (i_b) also changes considerably and nearly reaches the peak load current (cf. Figure 15(a)). The constant-current regulator-based architecture maintains a desired amount of the charging current regardless of the state of charge of the supercapacitor whereas, in the conventional parallel connection configuration, the charging current is not controllable and varies greatly as a function of the state of charge of the supercapacitor. Current from the supercapacitor (i_s) compensates the difference between the battery and load. Consequently, the proposed hybrid architecture reduces variation in the battery discharging current even with a small supercapacitor.

2.3 System-level power analysis techniques

There are numerous studies on power analysis and modeling of the computing systems including not only and general-purpose systems but also mobile embedded systems. The majority of existing studies focus on specific components in the system. We can find a lot of power models for each device such as microprocessors, memory devices, wireless communications, those models are usually too complicated for application development. The power management of microprocessor is well studied in [35]. A low-power techniques for OLED display considering the efficiency of driver circuits is introduced in [36].

Several system parameter-based power model for the mobile computing system has been introduced. A Measurement based power estimation model was introduced in [37, 38, 39]. They collect the system activity parameter and measure the system power consumption. The power coefficients are derived by regression analysis. A simulation technique based on an energy-state model and cycle-accurate characterization was introduced in [40]. A performance monitoring unit was designed by using a variable

reduction technique. Recently, battery-behavior monitoring-based approaches have been introduced. An adaptive modeling method based on the battery monitoring was introduced in [41]. Some method used a embedded voltage, current, and temperature sensor for batteries to automatically build the system-level power model [42]. They usually model the system with an analytical equations, and provide automatic coefficient deriving method. Based on the power consumption characteristics of the system, DC-DC converter reconfiguration technique is introduced to enhance the power efficiency [43].

3 Preliminary

3.1 Organic Light Emitting Diode (OLED) display

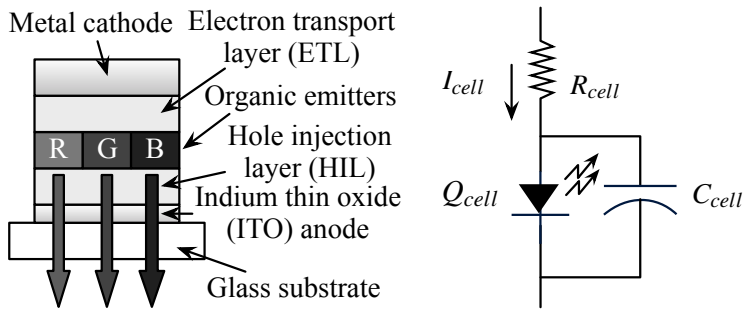
3.1.1 OLED Cell Architecture

Figure 16(a) shows the typical structure of the OLED cell [5]. The OLED device has a large area, but the thickness of the organic layers between the electrodes is only 100–200 nm. As a result, OLED cells have a large internal capacitance. The internal capacitance is not constant, but depends on the voltage and switching frequency. The value of C_{cell} is typically 200–400 pF/mm^2. OLED cells have a resistive component for each layer that lies between anode and cathode. The dominant resistive component is caused by the transparent Indium-Thin-Oxide (ITO) layer. Hence, the parasitic resistor is in series with the internal capacitance. The value of the parasitic resistor is strongly dependent on the design of the ITO electrode (anode). A typical value of the cell resistance is 15Ω/sq[1]. We calculate the R_{cell} with the cell area and sheet resistance. A simple equivalent circuit obtained with the physical parameters is depicted in Figure 16(b). It consist of the parasitic resistor R_{cell}, internal capacitance C_{cell}, and a diode Q_{cell}.

3.1.2 OLED Panel Architecture

There are several ways to classify the OLED driver architectures. Like LCD panels, we can make an OLED panel with a passive matrix (PMOLED) or an active matrix (AMOLED). PMOLED panels have a relatively simpler structure and thus a low cost. However, the practical maximum size is limited, typically up to 3”. In contrast, a thin film transistor (TFT) controls every pixel of AMOLED panels similar to TFT LCD panels.

[1] Ω/sq denotes the sheet resistance.



(a) OLED device struture. (b) Equivalent circuit model.

Figure 16: Device structure of OLED and equivalent circuit model.

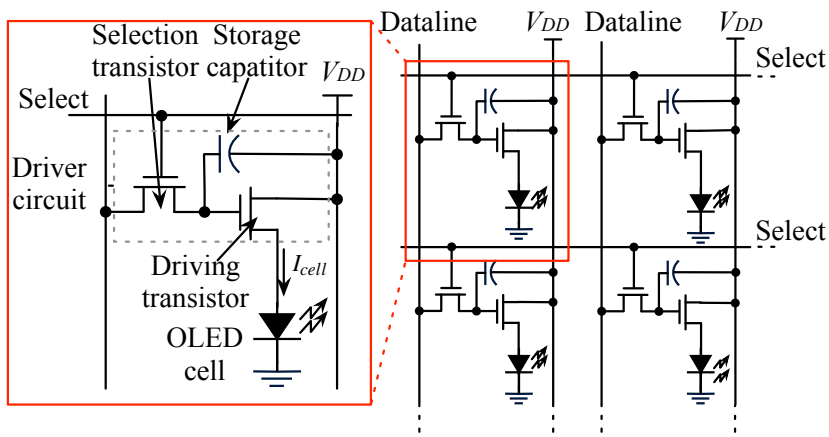


Figure 17: DVS-applicable amplitude modulation AMOLED driver.

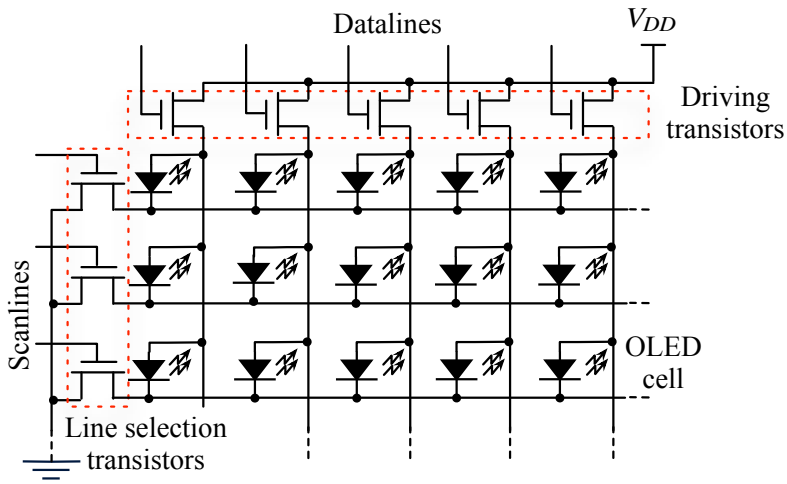
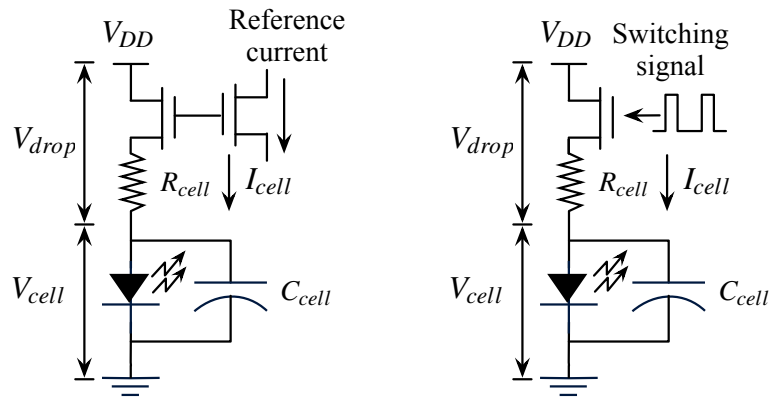


Figure 18: Driver matrix circuit for PMOLED driver.

Thus, AMOLED panels can be implemented with large size, but more complicated and expensive.

3.1.3 OLED Driver Circuits

The OLED cell current, I_{cell}, determines its luminance. The cell current is basically controllable by adjusting the cell voltage, V_{cell}. However, because the parasitic resistance is not stable, we commonly use a constant current driver. We can easily make a constant current source with a current mirror. We call an OLED driver using a current mirror-based current steering circuit an amplitude modulation (AM) driver. AMOLED panels are typically controlled by an AM driver circuit. There is a current source transistor whose gate voltage is maintained by a storage capacitor in the AM AMOLED driver. The AM driver scheme ensures a higher reliability and efficiency of the OLED cells.



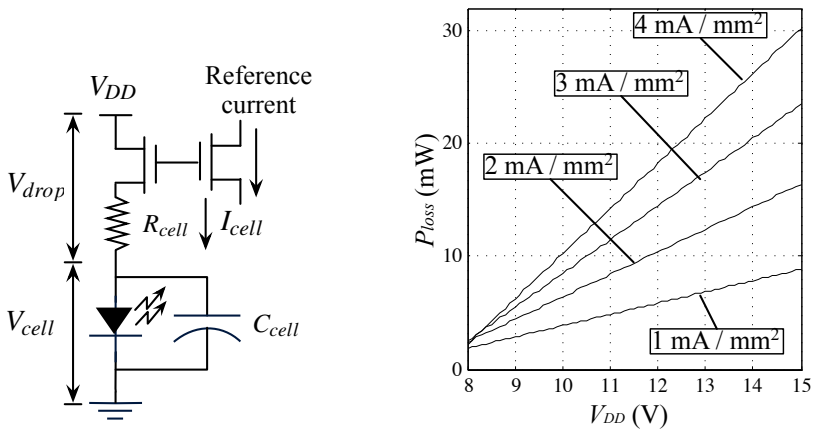
(a) AM driver.

(b) PWM driver.

Figure 19: Behavioral concept of AM driver and PWM driver for the OLED display.

However, the current steering circuit consumes large area, which results in higher cost.

On the other hand, PMOLED panels have a row-column structure driver circuit as shown in Figure 18. There is no storage capacitor in the PMOLED driver circuit. The cell current can be a pulsed current. We can easily achieve a pulse width modulation (PWM) of the cell current in the PMOLED panels. The luminance of an OLED cell is actually dependent on the average value of I_{cell}. The PWM cell current steering is inexpensive and provides precise luminance control. However, it is known to be less power efficient in high luminance region [5]. Unfortunately, the PWM driver in AMOLED panels is expensive. Some AMOLED drivers use both PWM and AM at the expense of even higher cost to tackle both display quality and power consumption.



(a) AM driver

(b) SPICE simulation result

Figure 20: Behavioral concept of AM driver and SPICE simulation result of P_{loss} with different V_{DD} and I_{cell} in AM driver circuit.

3.2 Effect of V_{DD} scaling on driver circuits

3.2.1 V_{DD} scaling for AM drivers

The concept of DVS of an OLED panel is to reduce power loss due to V_{drop} by scaling down V_{DD}. Although we scale down the V_{DD} of the AM driver circuit, there is only small change in I_{cell} due to the Early Effect in the AM driver as far as the driving transistor remains in the saturation mode (Figure 20 (a)). The driving transistor is in the triode mode when I_{cell} becomes too large with the scaled V_{DD}. The cell luminance decreases as we scale down V_{DD} in the triode mode, which causes image distortion.

The power loss of OLED cell is defined by $P_{loss} = I_{cell}V_{drop}$ where V_{drop} is determined by the characteristics of the OLED cell and I_{cell} is determined by the saturation current of the driver transistor. The excessive power should be dissipated by the driver

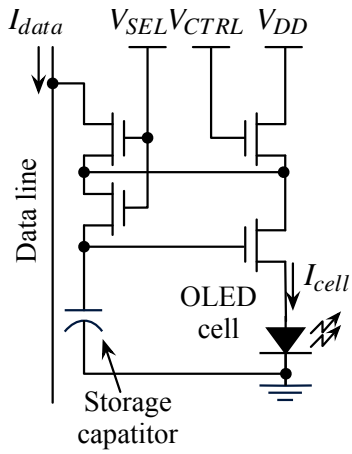


Figure 21: DVS-friendly AM driver circuit.

transistor, and P_{loss} is given by

$$P_{loss} = I_{cell}V_{drop} = I_{cell}(V_{DD}V_f), \tag{1}$$

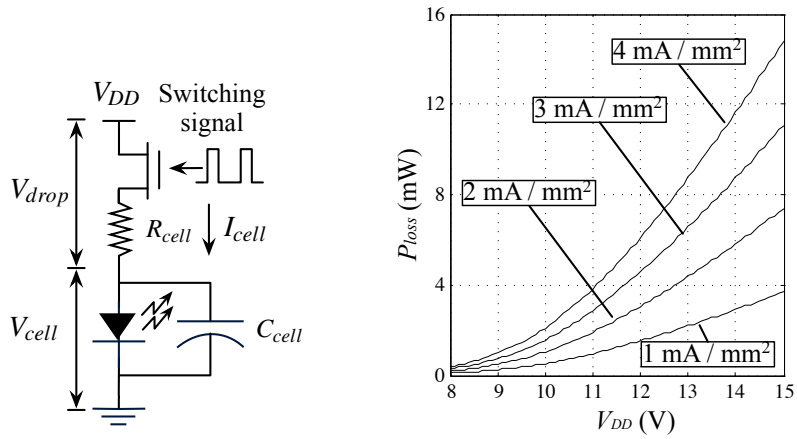
where V_f is the forward bias voltage of the diode.

Figure 20(b) shows a SPICE simulation to estimate P_{loss} with the parameters from [5]. The simulation model has an V-I characteristics as follows:

$$I_{cell} = 1.4144 \cdot 10^{-6}(e^{\frac{V_{cell}}{0.93678}}1),$$

and 20 mm^2 active area. We estimate P_{loss} with various V_{DD} values while delivering four different I_{cell} values from 1 mA/mm^2 to 4 mA/mm^2. The simulation result depicted in Figure 20 (b) shows that $P_{loss}$is proportional to the V_{DD} and I_{cell} as described in (1).

Fig 21 depicts a DVS-friendly OLED driver circuit that is more resilient to supply voltage variations [44]. The DVS-friendly driver makes color distortion happen only when V_{DD} is too low to supply I_{cell} = I_{data} because the bias condition of T_4 is maintained



(a) PWM driver

(b) SPICE simulation result

Figure 22: Behavioral concept of PWM driver and SPICE simulation result of P_{loss} with various V_{DD} and I_{cell} values.

by storage capacitor and V_{ctrl}. So, I_{cell} is equal to I_{data} as long as the V_{DD} is high enough. The DVS-friendly AM driver makes OLED DVS more efficient.

3.2.2 V_{DD} scaling for PWM drivers

DVS acts a bit differently in a PWM driver (Figure 22 (a)). Scaling V_{DD} down directly affects I_{cell}. We have to restore the luminance of image even with a slight V_{DD} scale. We apply a model-based image compensation and restore the luminance. A brighter color makes a higher PWM duty ratio in the PWM driver. The image compensation cannot always restore the original luminance if the original I_{cell} is too large. The maximum possible I_{cell} under the scaled V_{DD} cannot be the same as the original I_{cell} even when the PWM duty ratio is set to 100%. Thus, luminance distortion for some very bright pixels becomes unavoidable. We sacrifice a small display quality by allowing a certain amount

of color distortion of the image but save significant amount of power consumption.

With the PWM drivers, V_f and R_{cell} determine the maximum value of I_{cell} as follows:

$$I_{cell} = \frac{V_{DD}V_f}{R_{cell}}. \tag{2}$$

The luminance of the OLED is approximately proportional to the average value of I_{cell}, $\overline{I_{cell}}$, which is calculated by

$$\overline{I_{cell}} = I_{cell}d = I_{cell}\frac{t_{on}}{t_{on}+t_{off}}, \tag{3}$$

where PWM duty, $d = t_{on}/(t_{on}+t_{off})$, and t_{on} and t_{off} are the switch turn on and off durations in a PWM period, respectively. The power loss of an OLED cell during a PWM period is given by

$$P_{loss} = \overline{I_{cell}}^2 R_{cell}. \tag{4}$$

Figure 22 (b) shows a SPICE simulation result to estimate P_{loss} of the PWM driver such that P_{loss} quadratically increases as the V_{DD} and I_{cell} increase as described in (4). We use the same simulation parameters in Section 3.2.1. We estimate P_{loss} with various V_{DD} while delivering four different I_{cell} values from 1 mA/mm^2 to 4 mA/mm^2.

4 Supply Voltage Scaling and Image Compensation of OLED displays

4.1 Image quality and power models of OLED panels

We use human perception-aware color model to evaluate the image distortion. Typical RGB and CMYK spaces reflect the output of physical devices rather than human visual perception. CIE Lab color space is designed to approximate human-perceived vision. It is derived from the CIE 1931 XYZ color space, which reflects the spectral distribution of colors, and can be computed via simple formulas from the XYZ space. Due to its perceptual uniformity, its L component closely matches the human perception of brightness. The Euclidean distance in the Lab color space is widely used as a metric to measure the human perceived color difference [45].

The XYZ measurement result shows that X, Y, and Z values of RGB pixels are highly correlated (almost linearly proportional) with the cell current or almost constant regardless of the cell current. We build a transformation function using regression analysis which is given by

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} a_X \\ a_Y \\ a_Z \end{bmatrix} I_{cell} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix}, \tag{5}$$

where coefficients a_X, a_Y, a_Z, b_X, b_Y, and b_Z are obtained by performing the regression analysis on the measurement results.

We construct an I_{cell} model for a PMOLED structure OLED panel with a PWM driver based on (2) and (3). The cell current I_{cell} is proportional to V_{DD} and d such that

$$I_{cell}(d, V_{DD}) = p_1 V_{DD} d + p_2 d + p_3, \tag{6}$$

wherep_1, p_2, and p_3 are characteristic coefficients.

We describe the human-perceived image difference with the Euclidean distance in the Lab color space. We transform $I_{xyz} = (X,Y,Z)$ into a Lab color space image such that $I_{lab} = (L,a,b)$ by using the following transform functions [46].

$$\begin{aligned} L =& 116 \cdot (Y/Y_w)^{\frac{1}{3}} - 16 \\ a =& 500 \cdot ((X/X_w)^{\frac{1}{3}} (Y/Y_w)^{\frac{1}{3}}) \\ b =& 200 \cdot ((Y/Y_w)^{\frac{1}{3}} (Z/Z_w)^{\frac{1}{3}}), \end{aligned} \tag{7}$$

where L, a and b are matrices representing brightness, red-green content, and yellow-blue content in the Lab color space, respectively. Values of X_w, Y_w, and Z_w are the color coordinate values of the reference white in the color space. The Euclidean distance between two different colors $c_1 = (L_1,a_1,b_1)$, $c_2 = (L_2,a_2,b_2)$ in the Lab color space is calculated by

$$\varepsilon = \sqrt{(L_1 - L_2)^2 + (a_1 a_2)^2 + (b_1 b_2)^2}. \tag{8}$$

4.2 OLED display characterization

We chose a target OLED panel from Univision Technology [47], UG-2076GDEAF02, that has a 2.2" display area, a 220×176 resolution and a PMOLED structure with a PWM driver. We measure the relationship between the power consumption and luminance/chromaticity of the OLED panel with various V_{DD} values and pixel colors. We setup the measurement environment as shown in Figure 23. We control V_{DD} with a programmable power supply and measure the current with an Agilent 24401A multimeter. We use a Konica Minolta CS-200 color meter to measure the luminance and chromaticity of the OLED panel. The experiment is automated by a National Instruments LabView console. We perform the entire measurement process in a darkroom to block the effect

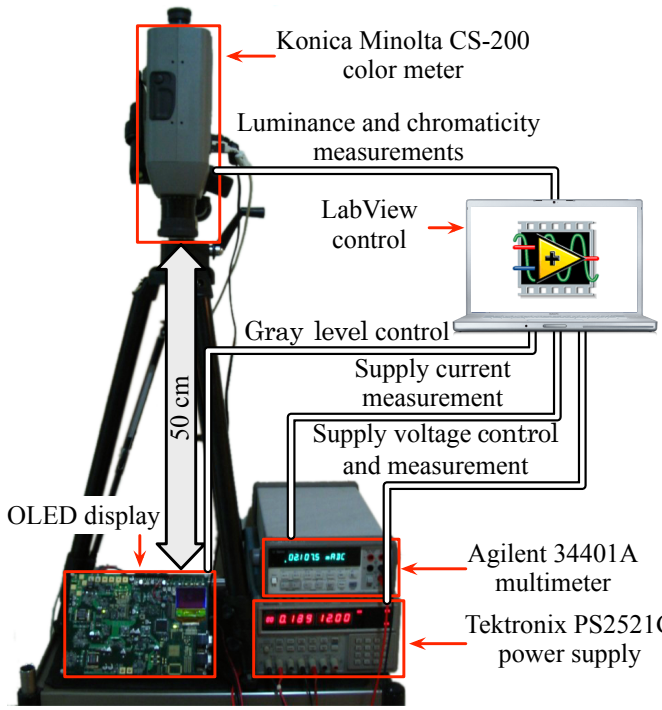


Figure 23: Experimental setup for the OLED display panel characterization.

Table 2: Extracted parameters for the power estimation and image difference evaluation

	R		G		B	
I_{cell} (μA) estimation	p_1	2.222e-2	p_1	2.234e-2	p_1	2.245e-2
	p_2	-1.650e-1	p_2	-1.648e-1	p_2	-1.599e-1
	p_3	1.652e	p_3	1.664e0	p_3	1.597e0
Image difference evaluation	a_X	3.573e5	a_X	1.035e5	a_X	4.903e4
	b_X	-4.554e-1	b_X	-2.764e-1	b_X	-3.230e-1
	a_Y	1.793e5	a_Y	2.556e5	a_Y	6.139e4
	b_Y	-2.282e-1	b_Y	-7.086e-1	b_Y	-3.020e-1
	a_Z	0.000e0	a_Z	2.263e4	a_Z	2.384e5
	b_Z	7.100e-3	b_Z	-6.030e-2	b_Z	-1.937e1

of ambient light. TWe acquire the coefficients by measurement and summarize them in Table 9. They show that the OLED cell of the UG-2076 OLED display panel has approximately 15 Ω of R_{cell} and 7.4 V of V_f.

We visualize a part of characterization data in Figure 24. The OLED display achieves the same luminance by adjusting the color value (gray level here) even with different V_{DD} levels. In other words, we can restore the color value with even a reduced V_{DD}, which proves the key premise of DVS for OLEDs. Figure 24 shows that the OLED panel generates a 70 cd/mm^2 luminance with a 15 V, a 13 V, a 11 V, and a 9 V V_{DD} by setting the gray level to 57%, 59%, 64%, and 77%, respectively. It turns out that the luminance is not affected by V_{DD} when the gray level is below a certain level such as non-linear region in Figure 24. Therefore, we compensate the V_{DD} scaling-induced luminance reduction by modifying image data only in the linear region of Figure 24.

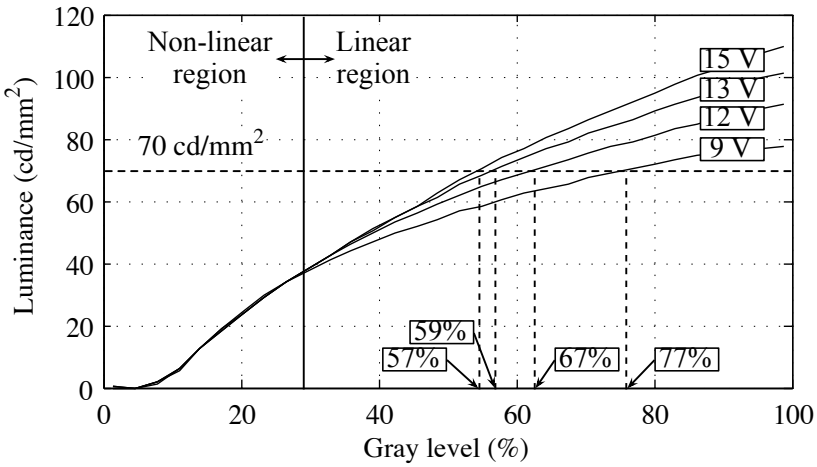


Figure 24: Measured luminance by V_{DD} and gray level with AM driver.

4.3 V_{DD} scaling and image compensation

The transistor in the AM driver is originally designed to operate in the saturation mode. The driver transistor is in the the saturation mode though we scale V_{DD} as shown in Figure 25 as long as V_{DS} is higher than $V_{GS}V_T$. The saturation mode operation ensures the almost same I_{cell} regardless of changes in the V_{DD}. There is only small change of I_{cell} due to the Early effect. Consequently, V_{DD} scaling only only affects pixels with high brightness as shown in Figure 25. High brightness pixels can no longer deliver the same amount of the cell current with a reduced V_{DD}. We need to limit the number of distorted pixels to maintain the image quality, and V_{DD} should be determined under the considerations of the upper bound of the distorted pixels.

We have more potential to save power consumption from V_{DD} scaling with the PWM drivers. We reduce P_{loss} in an OLED cell while preserving the luminance through a reduced V_{DD} and prolonged d according to (2), (3), and (4). The scaled V_{DD} for PWM drivers evenly decreases the luminance of all the OLED cells. At the same time, we

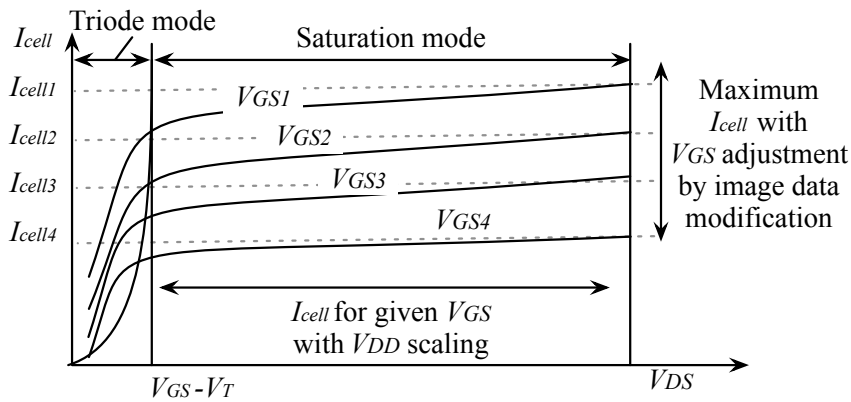
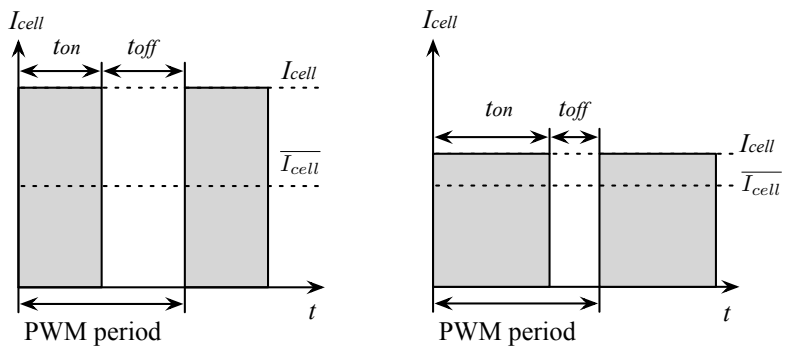


Figure 25: Effect of V_{DD} scaling and image compensation on the OLED cell current with AM drivers.



(a) OLED cell current with the maximum V_{DD} (b) OLED cell current with the scaled V_{DD}

Figure 26: Effect of V_{DD} scaling and image data modification on OLED cell current with (a) the maximum V_{DD} and (b)scaled V_{DD} for PWM drivers.

restore $\overline{I_{cell}}$ and the luminance by increasing the PWM duty ratio d in (3) as shown in Figure 26. Then we obtain the same $\overline{I_{cell}}$ with less P_{loss}.

Algorithm 1: Algorithm for OLED DVS.

Input: Image $I = (R, G, B)$ and image distortion tolerance τ_{image}.

Output: Transformed image I'

1: Set V_{DD} at the maximum supply voltage V_{max}.

2: Decrease a V_{DD} step ΔV_{DD} from the previous V_{DD}.

3: Calculate the power reduction by (6).

4: Calculate the average image distortion $\bar{\varepsilon}$ caused by V_{DD} scaling by (8).

5: Calculate minimum grayscale step increment for R, G, and B by (6)–(8) to increase enough amount of I_{cell} to satisfy the image distortion tolerance constraint ($\bar{\varepsilon} \leq \tau_{image}$).

6: Calculate the power of the modified image and scaled voltage by (6).

7: If the voltage scaling induced power reduction is less or equal to the required power to satisfy the the image distortion tolerance constraint, then stop the DVS.

8: Otherwise, repeat 2–7.

The Lab color space regards two different colors perceptually identical when the Euclidean difference between the two color is less than a certain threshold. The threshold is generally determined by the human vision characteristics and environmental conditions, but it can also be determined by the user. We formulate an optimization problem to find a transformed image $I' = (R', G', B')$ and V_{DD} that maximize the power saving subject to a threshold for distinguishing two colors. The threshold, τ_{image}, can be thought of as the maximum allowable average Euclidean distance $\bar{\varepsilon}$ between the original and compensated images. We develop an iterative algorithm to find the solution with image quality

and power model of the OLED display as shown in Algorithm1.

Figure 27 illustrates the behavior of the OLED DVS algorithm with the OLED panel. Upper surface plot of Figure 27 shows the OLED panel power consumption and lower surface plot shows the luminance value according to the gray level of pixels and V_{DD}.

The 'Original' dot in the Figure 27 represents the original V_{DD} and gray level. The dot moves straight down by V_{DD} scaling ((a) in Figure 27), losing luminance and consuming less power. The image compensation ((b) in Figure 27) recovers the luminance with a higher gray-level value. This new gray-level incurs higher power consumption, but the 'Scaled' dot eventually exhibits lower power consumption than that of the 'Original' dot while having the same luminance. As the available voltage levels are limited desecrate values, V_{DD} and gray level are discrete, too. Algorithm 1 depicts how to iteratively derive the optimal discrete V_{DD} and gray scale level.

The major computational overhead of OLED DVS is the estimation of the image distortion and calculation of image compensation. We derive them by using a pre-generated lookup table depending on the characteristics of the OLED panel and the driver architecture [3]. Size of the table is determined by the number of color values and the number of V_{DD} levels. These parameters strongly affect the performance obtained by the proposed OLED DVS scheme such as delay penalty to display/update an image on the OLED panel and power saving.

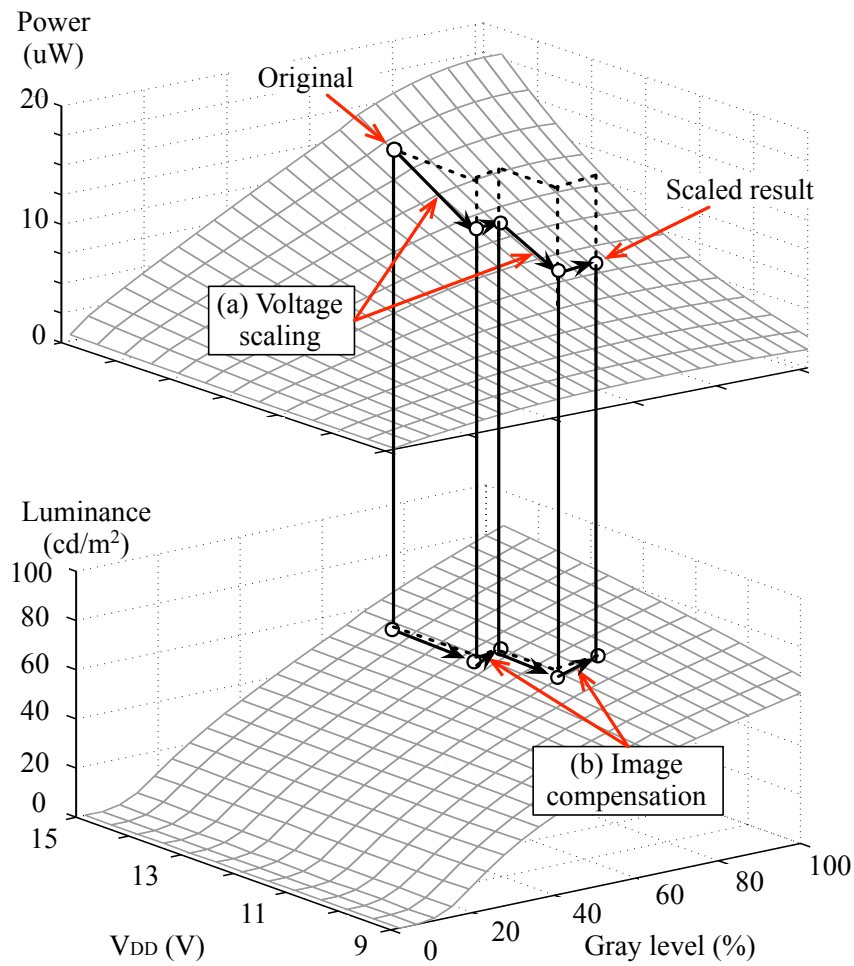


Figure 27: Power and luminance measurement with a different V_{DD} and image data.

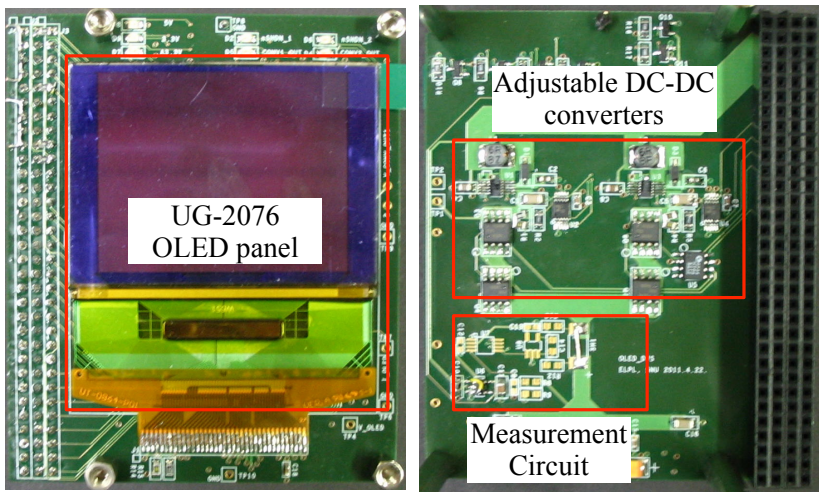


Figure 28: Output voltage adjustable DC-DC converter equipped OLED display board.

5 OLED DVS implementation

5.1 Hardware prototype implementation

We develop an hardware board which enables V_{DD} scaling and the image compensation for the target OLED display panel. This platform equips two output voltage adjustable DC-DC converters for an UG-2076 OLED display panel. We modify the output voltage feedback loop of a LT3495 DC-DC converter form Linear Technology by using an AD5161 digital potentiometer from Analog Device. The platform is compatible with the peripheral interface of a Xilinx Virtex-5 FPGA-based evaluation platform. We control the OLED display panel and power converters through the FPGA platform. Supply voltage and current are measured by an INA194 current shunt monitor form Texas Instrument and an ADC102S Analog-Digital converter from National Semiconductor.

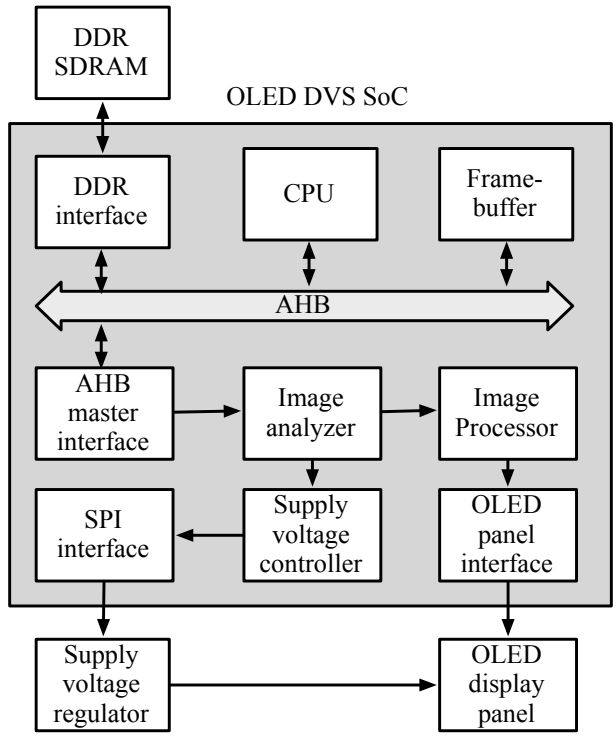


Figure 29: OLED DVS enabled system-on-chip implemented with an FPGA.

5.2 OLED DVS System-on-Chip implementation

We implement a system-on-chip (SoC) on the FPGA as shown in Figure 29. The SoC consists of an ARM7 microprocessor, a DDR SDRAM interface, an on-chip SRAM framebuffer, an image analyzer, an image processor, a V_{DD} controller, and a SPI interface. The microprocessor transfers the image data to the framebuffer, and the AHB master interface provide the frame data to the OLED display panel interface according to the sweep rate of the OLED display panel. The image analyzer finds the optimal V_{DD} and a lookup table map of image data by constructing the histogram of the pixel data. According to the value obtained by the image analyzer, the V_{DD} controller adjusts the

output voltage of the V_{DD} regulator through the SPI interface, and the image processor modifies the pixel data synchronized with each other.

The image analyzer builds a luminance histograms of the image for each color. It consists of pixel counter and threshold values. The number of histogram step is synthesizable, and the threshold values are programmable by user. We separately setup the threshold values in the linear region and non-linear region according to the relation between the luminance and V_{DD} as shown in Figure 24. We estimate the image distortion from the image histogram and select the V_{DD} level. The image processor consists of arithmetic operators and lookup table. The image data output value is calculated by a piece-wise linear model and the lookup table. The number of piece in the model is synthesizable, and the lookup table is programmable. The OLED DVS unit accepts the V_{DD} level and original image data as a input, and generates compensated a image data value. The V_{DD} controller adjusts the output voltage of the DC-DC converter by changing the value of feedback resistance. We connect the digital potentiometer to the feedback input of the DC-DC converter. The resistance value of the digital potentiometer can be controlled by a SPI interface. The V_{DD} controller transmits SPI signal synchronized with a frame synchronization signals. We obtain the silicon area and estimated power consumption value for the OLED DVS controller unit by using Synopsys Design Complier with TSMC 45 nm technology library. The results are summarized in Table 3.

Table 3: Silicon area and estimated power consumption of OLED DVS unit TSMC 45 nm technology library.

Area	
Number of ports	1705
Number of nets	2274
Number of cells	173
Number of references	41
Combinational area	3667.18
Non-combinational area	1181.53
Total area	4848.71
Power consumption	
Global operating voltage	0.99
Cell internal power	199.09 uW (73%)
Net switching power	72.88 uW (27%)
Total dynamic power	271.98 uW
Cell leakage power	297.76 uW

Table 4: Synthesis result and power measurement of OLED DVS unit in FPGA.

		Original	OLED DVS
Synthesis result	Slices	8353	8993
	Slice Reg.	7910	8131
	LUTs	13261	14629
	LUTRAM	1109	1109
	BRAM	130	130
Power consumption		6.273 W	6.319 W

We implement the OLED DVS controller in a FPGA. Table 4 summarizes space complexity of the DVS-enabled OLED display panel controller synthesized in the FPGA. We measure the average power consumption of the Xilinx XUPV5-LX110T platform when the OLED DVS module is on and off with the same image sequence.

5.3 Optimization of OLED DVS SoC

We design hardware support unit for an online OLED DVS control. We use pixel luminance histogram and build a lookup table with the scaled V_{DD} as the input and estimates of the image distortion as the output. The estimates identifies pixels having higher luminance value that cannot be produced with the scaled V_{DD} even after image compensation.

We count the number of pixels from the brightest one to limit the image distortion within t_{image}. More precise characterization result is obtained with a smaller intervals in the histogram [4]. We estimate the side effect in power saving from the histogram quantization interval and derive the most efficient quantization granularity.

Figure 30 shows how to derive the threshold luminance L_T, a function of d and V_{DD} from (5), (6), and (7). The luminance threshold L_T represents an upper limit of luminance

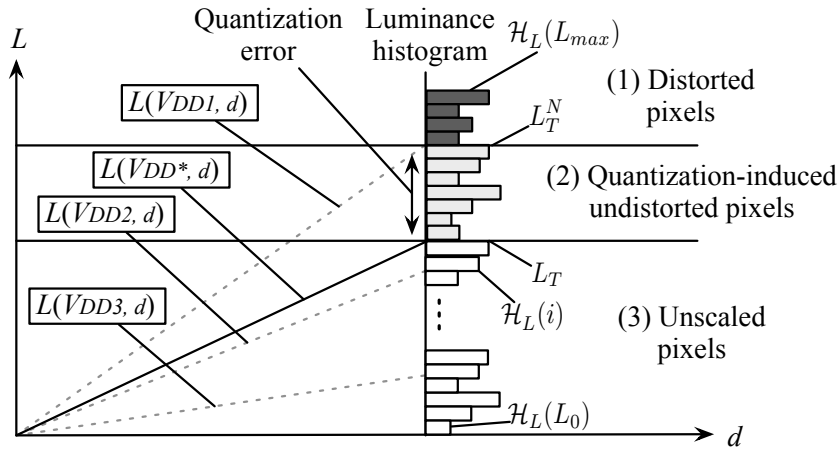


Figure 30: Side effect in power saving due to the quantization in the histogram.

that is not distorted by the V_{DD} scaling. The highest possible luminance value without V_{DD} scaling is L_{max}. We define L_T corresponding to the image distortion threshold τ_{image} by the following condition:

$$\sum_{i=L_T}^{L_{max}} D(i)\mathcal{H}_L(i) \leq t_{image} \text{ and } \sum_{i=L_T 1}^{L_{max}} D(i)\mathcal{H}_L(i) > t_{image}, \tag{9}$$

where $\mathcal{H}_L(i)$ represent the number of pixels whose luminance value is i, and $D(i)$ represents the corresponding distortion value. Pixels with the luminance higher than L_T (Figure 30 (1) and (2)) should be distorted even with a histogram without quantization. OLED DVS reduces P_{loss} by scaling V_{DD} to V_{DD}^* corresponding L_T where V_{DD}^* denotes required voltage level to illuminate the pixels as L_T with the maximum d value. Pixels with the luminance lower than L_T (Figure 30 (3)) are restored by the image compensation.

Histogram quantization in image compensation [4] affects the upper limit of lumi-

nance that is not distorted by the V_{DD} scaling. Let us denote the luminance value with a quantized N-step histogram as L_T^N. Quantization error makes $L_T \leq L_T^N$.

$$L_T^N = \lceil \frac{L_T}{(L_{max}/n)} \rceil \frac{L_{max}}{n}. \tag{10}$$

Pixels with the luminance higher than L_T^N (Figure 30 (1)) are distorted because the luminance value should be mapped to L_T^N while pixels in (Figure 30 (2)) are not distorted. However, less pixel distortion implies less power saving.

We analyze the amount of power saving sacrificed due to histogram quantization by the interval step, N. This is a guidance to obtain the optimal design of image analyzer considering accuracy and overhead. The difference between P_{loss} and ΔP_{loss} by V_{DD} and V'_{DD} is power saving, which is given by

$$\begin{aligned} &\Delta P_{loss}(V_{DD}, V'_{DD}, d) \\ &= R_{cell} \left[\left(\frac{V_{DD} V_f}{R_{cell}} \right)^2 \cdot d \left(\frac{V'_{DD} V_f}{R_{cell}} \right)^2 \cdot d' \right], \\ &= R_{cell} \frac{V_{DD} V_f}{R_{cell}} \cdot (V_{DD} V'_{DD}) \cdot d \end{aligned} \tag{11}$$

where d' is determined by following equation to supply the same average I_{cell} with V_{DD} and V'_{DD}.

$$d' = \frac{V_{DD} V_f}{V'_{DD} V_f} \cdot d. \tag{12}$$

We calculate the difference of P_{loss} between the histogram with and without N-step quantization by V^*_{DD} and V^{*N}_{DD} that correspond to V_{DD} for L_T and L_T^N, respectively. We denote required voltage level to illuminate the pixels as L_T^N with the maximum d value

by V_{DD}^{*}. Expectation of the difference between $\Delta P_{loss}(V_{DD}^{*}, V_{DD}^{*N}, d))$ is calculated by

$$\overline{\Delta P_{loss}} = \overline{\Delta P_{loss}}(V_{DD}^{*}, V_{DD}^{*N}, d)) = \tag{13}$$
$$\sum_{j=L_0}^{L_{max}} \Bigg\{ \sum_{k=L_0}^{\bar{j}} \sum_{l_k=0}^{N_{pixel}N_{dist}} \Big[\Delta P_{loss}(V_{DD}^{*}, V_{DD}^{*N}, d)) \cdot l_k \cdot Pr(l_k, j) \Big]$$
$$+ \sum_{k=\bar{j}}^{L_{max}} \sum_{l_k=0}^{N_{dist}} \Big[\Delta P_{loss}(V_{DD}^{*}, V_{DD}^{*N}, 1) \cdot l_k \cdot Pr(l_k, j) \Big] \Bigg\}.$$

where $\bar{j}$ represents the corresponding L_T^N value for j, which is given by

$$\bar{j} = \lceil \frac{j}{(L_{max}/n)} \rceil \cdot \frac{L_{max}}{n}, \tag{14}$$

and the number of distorted pixel are calculated by

$$N_{dist} = \sum_{i=\bar{j}}^{L_{max}} \mathcal{H}_L(i). \tag{15}$$

We calculated d, V_{DD}^{*}, and V_{DD}^{*N} from (3), (5), (6) and (7). We denote the probability such that k-th interval in the histogram without quantization has l_k pixels where $L_T = j$ by $Pr(l_k, j)$, which is given by

$$Pr(l_k, j) = Pr(\mathcal{H}_L(k) = l_k | L_T = j) \tag{16}$$
$$= \Bigg\{ \begin{pmatrix} N_{pixel} \\ N_T \end{pmatrix} (\frac{L_{max} j}{L_{max}})^{N_T} (1 - \frac{L_{max} - j}{L_{max}})^{N_{pixel}N_T} \cdot$$
$$\begin{pmatrix} N_{pixel}N_T \\ l_k \end{pmatrix} (\frac{1}{L_{max}})^{l_k} (1 - \frac{1}{L_{max}})^{N_{pixel}N_T - l_k} \Bigg\},$$

where N_{pixel} is the total number of OLED cells on the panel, N_T is the number of pixels that have higher luminance than L_T, and the value of L is uniformly distributed from L_0 to L_{max}. Without loss of generality, each binomial probability mass function component

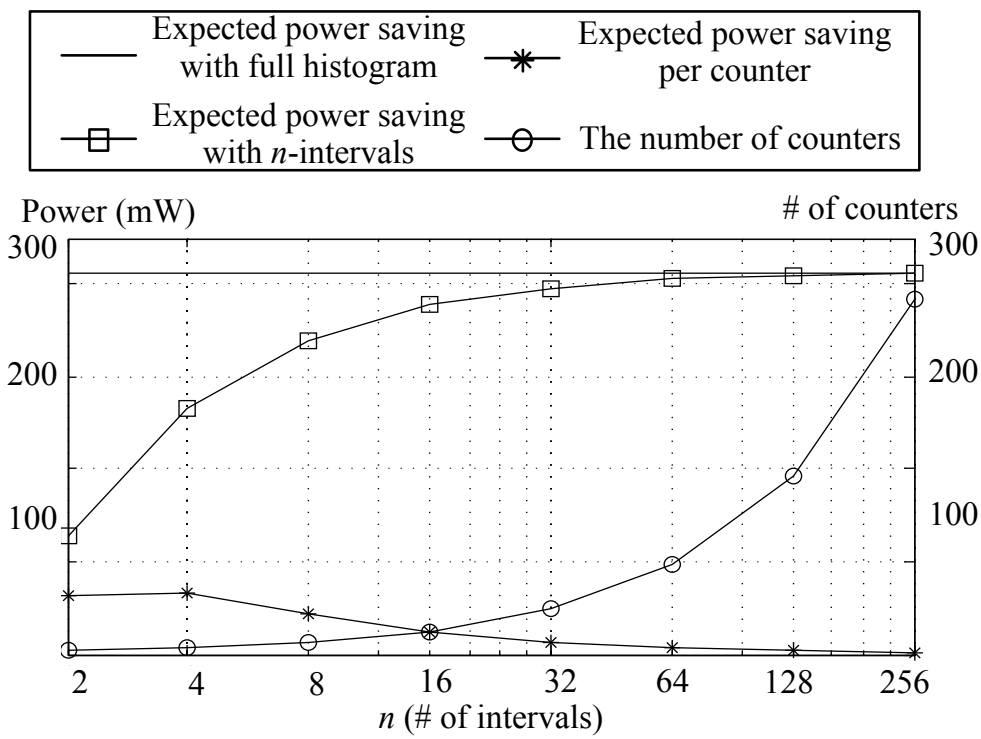


Figure 31: P_{saving} vs. the number of counters.

in (16) can be approximated to the normal distribution because N_{pixel} is large enough and $N_{pixel} \cdot (1/L_{max})$ is far greater than 10 as far as N_T is smaller than 10 % of N_{pixel}.

Figure 31 shows $\overline{\Delta P_{loss}}$ for different n in a 220 $\times$ 176 display panel with τ_{image} corresponding to the 10 % of totally distorted pixels. The less power saving due to the side effect exponentially decreases as N increases. We obtain the expected power saving with n-interval histogram by

$$\begin{aligned} \overline{P_{saving}} = & \overline{\Delta P_{loss}}(max(V_{DD}), V_{DD}^{*}, d) \\ & \overline{\Delta P_{loss}}(V_{DD}^{*}, V_{DD}^{*N}, d), \end{aligned} \tag{17}$$

where the $max(V_{DD})$ is 15 V which is used in the implementation.

Each histogram interval requires a counter register that can accommodate N_{pixel}. We consider the number of register and calculate P_{saving} per counter, P_{saving}/N, to consider resource complexity. As shown in Figure 31, P_{saving}/N decreases as $N > 4$. We confirm that 4-step histogram shows the most efficient results for the target OLED system.

5.4 V_{DD} transition overhead

Transition energy overhead in a DVS-enable system was carefully studied in [48]. When V_{DD} range is from 8 V to 15 V with a 22 μF output bulk capacitor in the DC-DC converter (which is used in our implementation), the required energy to charge the output bulk capacitor is about 0.76 mJ. The maximum voltage transition frequency is determined by the refresh rate of the OLED panel. If we use 60 Hz refresh rate, then the expected power overhead for the voltage transition is about 46 mW. However, as indicated in [48], the excessive energy to upscale V_{DD} can be retrieved in downscaling process in discontinuous mode. Consequently, the expected amount of wasted energy is negligible for random V_{DD} change.

Modern DC-DC converter requires for a few tens of μs for voltage transition [48]. OLED display panels have idle intervals during VSYNC is active. The length of each VSYNC period are typically about 3 HSYNC cycles, and the HSYNC is asserted at the end of horizontal scan. Consequently, VSYNC period is about 9 horizontal scan cycles. The length of data transfer cycle is determined by the refresh rate and the display size. If we use 60 Hz refresh rate in a display which has 1920 x 1200 size, then the idle period between the refresh operation is about 130 μs. Therefore, the voltage transition is feasible during the idle period even when we use a large-size panel.

6 Power conversion efficiency and delivery architecture in mobile Systems

6.1 Power conversion efficiency model of switching-Mode DC–DC converters

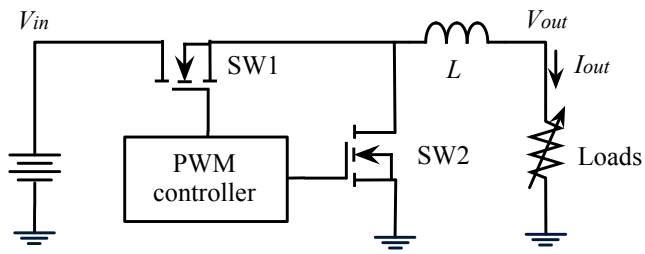
Switching DC-DC converters are used to transfer power between two different voltage levels. They exhibit a higher efficiency than linear regulators. Batteries and supercapacitors, which have variable terminal voltages that are set according to their state of charge, are commonly paired with switching DC-DC converters to supply a regulated current or a regulated voltage level to the load.

The switching DC-DC converter efficiency is defined as

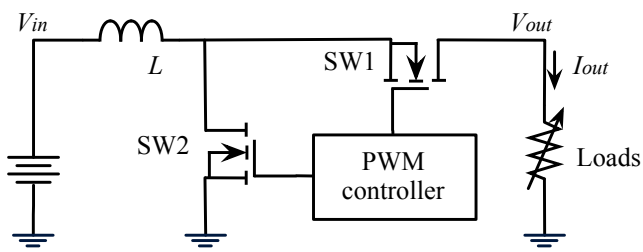
$$\eta_{conv} = \frac{P_{out}}{P_{in}} = \frac{P_{in} P_{loss}^{conv}}{P_{in}}, \tag{18}$$

where P_{conv} denotes the power consumed by the converter, which comprises the conduction losses, gate-drive losses, and controller power dissipation. P_{in} and P_{out} are the input power and output power of the converter, respectively.

The power loss model of a DC-DC converter is well-studied in [43]. In general, the major sources of power loss in a DC-DC converter are conduction loss, switching loss in the power switches, and controller power loss. We denote them as $P_{conduction}$, $P_{switching}$, and P_{ctrl}, respectively. The switching-mode DC-DC converters can be implemented by using a switch and a diode or two switches. The switching-mode DC-DC converters using two switches basically replace the diode with the synchronous switch (lossless diode) to avoid the power loss due to the voltage drop in the diode. It shows better efficiency but also requires more components and complicated control. Power loss in the switching mode DC-DC converter with the synchronous switch in continuous mode is



(a) Switching-mode buck converter topology.



(b) Switching-mode boost converter topology

Figure 32: (a) Switching-mode buck converter topology and (b) boost converter topology.

approximately given by

$$
\begin{aligned}
P_{loss}^{sw} =& P_{conduction} + P_{switching} + P_{ctrl} \\
P_{conduction} =& {I_{out}}^2 (R_L + DR_{sw1} + (1-D)R_{sw2}) \\
&+ \frac{1}{3}(\frac{\Delta I}{2})^2 (R_L + DR_{sw1} + (1-D)R_{sw2} + R_C) \\
P_{switching} &+ V_{on} f_s (Q_{sw1} + Q_{sw2}), \\
P_{ctrl} &= V_{in} I_{ctrl},
\end{aligned}
\tag{19}
$$

where f_s is the switching frequency; and I_{ctrl} denotes the current used in the control logic section of the converter. Series resistances of the inductor L and capacitor C are denoted by R_L and R_C, respectively. Similarly, series resistances of the two MOSFET switches are represented by R_{sw1} and R_{sw2}, respectively, while the amounts of their gate charge are denoted by Q_{sw1} and Q_{sw2}, respectively. V_{on} denotes turn on input voltage of the MOSFET gate and Q_{sw} is equals to $C_{sw} * V_{on}$. ΔI represent the inductor current ripple. ΔI for the buck converter, ΔI_{buck}, and boost converter, ΔI_{buck}, with the input voltage, V_{in}, and output voltage, V_{out}, are given by

$$
\begin{aligned}
\Delta I_{buck} &= \frac{V_{in} V_{out}}{Lf} D_{buck}, \\
\Delta I_{boost} &= \frac{V_{in}}{Lf} D_{boost},
\end{aligned}
\tag{20}
$$

where switching duty for buck converter and boost converter are determined by

$$
\begin{aligned}
D_{buck} &= V_{out} / V_{in}, \\
D_{boost} &= 1 V_{in} / V_{out}.
\end{aligned}
\tag{21}
$$

If we use the diode, $P_{conduction}$ should be changed to as follows:

6.2 Power conversion efficiency model of Llnear regulator power loss model

A typical linear regulator consists of an error amplifier, a pass transistor, and a feedback resistor network. The power loss of the linear regulator, denoted by P_{linear}, is given by:

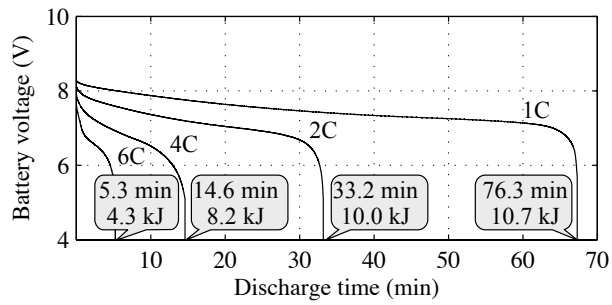
$$P_{linear} = I_{out}(V_{in} - V_{out}) + I_q V_{in}, \tag{22}$$

I_q denotes the quiescent current of the linear regulator. The power loss of the linear regulator is proportional to the difference between input and output voltage. The pass transistor solely dissipates the power difference between input and output.

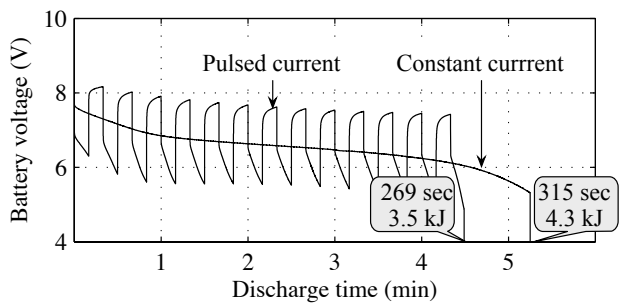
6.3 Rate Capacity Effect of Li-ion Batteries

We measure the voltage of the Li-ion battery for different discharging currents to show the impact of rate capacity effect on the battery capacity. Figure 33(a) shows the voltage drop and total amount of delivered energy from the battery with a constant discharging current of 1C, 2C, 4C, and 6C, when using 2-cell series Li-ion GP1051L35 cells [49]. The discharging efficiency (defined as the ratio of energy delivered from the battery to the load to the nominal energy storage in that battery) at 6C load current is merely 40% of the 1C discharging efficiency. In practice, intermittent large amount of discharging current is often applied to batteries due to significant load current fluctuation of a typical battery-powered electronics circuit or systems.

Furthermore, as presented in Figure 33(b), drawing a pulsed current of 12C with a 50% duty cycle, which is 6C on average, results in only 81.3% delivered energy and a shorter service life compared to drawing a constant current of 6C. This example clearly demonstrates the need of the peak current reduction.



(a) Discharging at a constant current of 1C, 2C, 4C, and 6C.



(b) Discharging at a 6C constant current and 12C pulsed current of a 20 s period and a 50% duty cycle.

Figure 33: Discharging a 350 mAh 2-cell Li-ion battery with (a) different constant current and (b) pulsed and constant currents.

7 Power conversion efficiency-aware battery setup optimization with DVS-enabled OLED display

7.1 System-level power efficiency model

In typical mobile devices, the power conversion loss in the path can be regarded as a combination of P_{loss}^{sw} and P_{loss}^{ldo}. The switching converters are generally used to generate a specific voltage for the components due to the conversion efficiency and heat dissipation. The linear regulators are typically placed between the switching converter and components which require low-noise voltage supply as illustrated in Figure 34. The linear regulators are only used for the step-down conversion.

For step-down conversion, we model the equivalent power loss for the path in terms of the combination of P_{loss}^{sw} and P_{loss}^{ldo} from (19), (20), (21) and (22). P_{loss} model for step-down conversion with a fixed output voltage is given by

$$P_{loss}^{conv} = a_1 {I_{out}}^2 + a_2 I_{out} + a_3 V_{in} I_{out} + \frac{a_4}{V_{in}^2} + \frac{a_5}{V_{in}} + a_5 V_{in} + a_6 \tag{23}$$

where V_{in} and I_{out} denote a system input voltage from the battery and output current to the components and a_1 to a_6 represent the coefficiency which are obtained by the regression of the measured P_{loss}.

For the system with multiple subcomponents, the system-level P_{loss}^{sys} can be calculated by summing the component-level $P_{loss}^{conv,i}$, which is given by

$$\begin{aligned} P_{loss}^{sys} &= \sum P_{loss}^{conv,i} \\ &= \sum (a_1^i {I_{out}^i}^2 + a_2^i I_{out}^i + a_3^i V_{in} I_{out}^i + \frac{a_4^i}{V_{in}^2} + \frac{a_5^i}{V_{in}} + a_5 V_{in}) + a_6 \end{aligned} \tag{24}$$

where n denotes the number of subcomponents in the system.

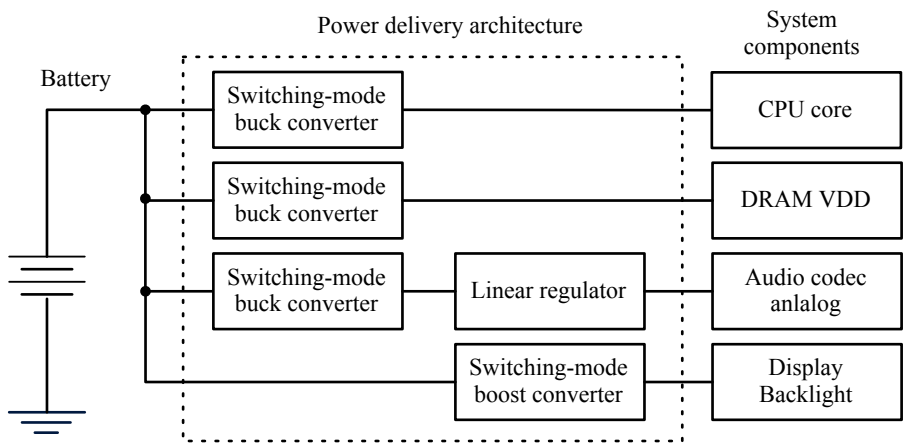


Figure 34: Power delivery architecture concept.

7.2 Power conversion efficiency analysis of smartphone platform

We use the MSM8660 SnapDragon MDP from Qualcomm as a target platform [51]. The Snapdragon MDP incorporates embedded power sensors that monitors fine-grain module (a set of devices) current values. It is a cutting-edge development platform for the smartphone equipped with Google Android OS 2.3 on the top of Snapdragon 1.5 GHz asynchronous dual-core CPU, a 3D-supporting GPU, 3.61″ WVGA multi-touch screen, 1 GB internal RAM, 16 GB on-board flash, Wi-Fi, Bluetooth, a GPS, dual-side cameras, etc. However, since its primary purpose is to develop prototype applications, it does not has a cellular module. We perform power measurement of each modules using the application profiling tool named *Trepn*™. Use of *Trepn*™ ensures more accuracy of measurement, but the proposed idea can be applied to the system without the embedded sensors.

We develop a benchmark application to enable component-wise activity control. The

benchmark generates various usage patterns by repeatedly activating each component with minimum to maximum utilization while other components are disabled to reduce the correlated power consumption. We utilize some component sets simultaneously to simulate real usage patterns. We randomly change the activated time to avoid the same periodic patterns. The benchmark controls following components:

CPU The benchmark generates cache hits and misses through matrix traversal operations. After create a 2048 $\times$ 2048 integer matrix in the main memory, in order to calculate simple summation, load the integers sequentially from the matrix in row-major order and column-major order alternately. After these repetition, Fast Fourier transform (FFT) is executed for full utilization.

GPU GPU is utilized through matrix manipulations such as cropping, rotating, skewing, resizing, and rendering bitmap images.

DSP We play high-quality video and audio files encoded various codecs.

Wi-Fi We downloads files which have different size from a web server via Hypertext Transfer Protocol (HTTP).

Display We changes the screen brightness from 0% to 100%

GPS A GPS module is activated to locate current position of the smartphone during random periods.

We characterize the power consumption of the components in the target platform with the benchmark. The target platform provides 29 measurement point with embedded current sensor. We measure the current by using *Trepn*™ profiler with 100 ms sampling period. The supply voltage and current statistics is summarized in Tables 5 and 6 We se-

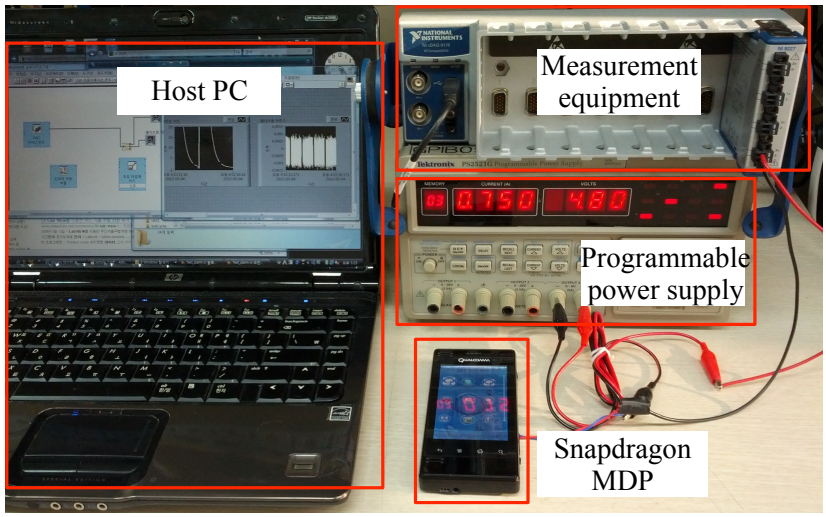


Figure 35: Experimental setup for power characterization of Snapdragon MDP development platform.

lect the components which are characterized, where the standard deviation of the current is greater than 5 to obtain meaningful regression result with sufficient I_{out} values.

We connect the PG2521 programmable power supply from Tektronix to the battery connector of the target platform to maintain the V_{in} during the measurement. The measurement environment is presented in Figure 35. We change the V_{in} by changing the output voltage of the programmable power supply. The regression result illustrated in Figures 36, 37 and 38 show that P_{loss} of each component is proportional to I_{out} and V_{in}.

The extracted parameters are summarized in Table 7. The P_{loss} model shows less than 1% average estimation error. The estimation result is presented in Figure 39.

Table 5: Power consumption characteristics of target platform components (1/2).

Component	Supply Voltage (V)	Average current (mA)	Current standard deviation
Audio DSP	1.1	0.5195	0.6332
VREG L16A	1.8	5.7261	6.8969
SD Card	2.85	0.3182	1.434
Audio Codec IO	1.8	0.0543	0.0603
Audio Codec VDDCX 1	1.2	0.0552	0.0604
Audio Codec Analog	2.2	0.0858	0.092
Touch Screen	2.85	3.4592	3.7758
CPU Core 0	0.9-1.2	29.6233	48.8773
Internal Memory	1.1	11.9731	13.1627
CPU Core 1	0.9-1.2	29.5807	50.1398
eMMC	2.85	0.0901	0.5602
Digital Core	1.1	71.6834	75.1188
ISM VDD2	1.35	0.1208	0.1326
IO PAD3	1.8	1.9533	2.4165
IO PAD2	2.85	0.0948	0.2627
Haptics	2.6	3.8972	3.9384
VDDPX1 LPDDR2	1.2	4.3597	5.4995
DRAM VDD1	1.8	0.4462	0.505
Ambient Light Sensor	2.85	0.0716	0.0748
Display ELVDD	3.8	5.2717	13.091
Display IO	1.8	0.0603	0.0815

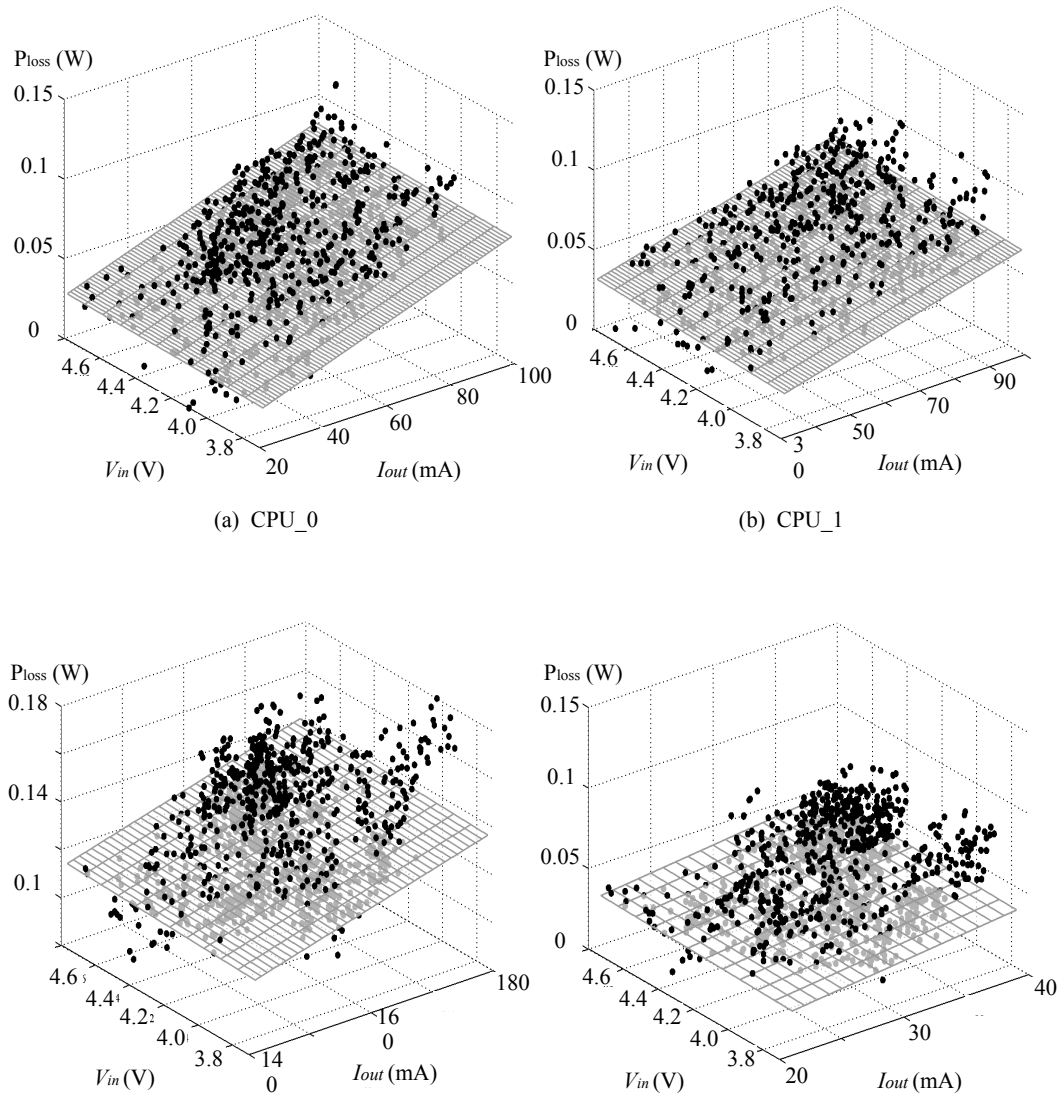
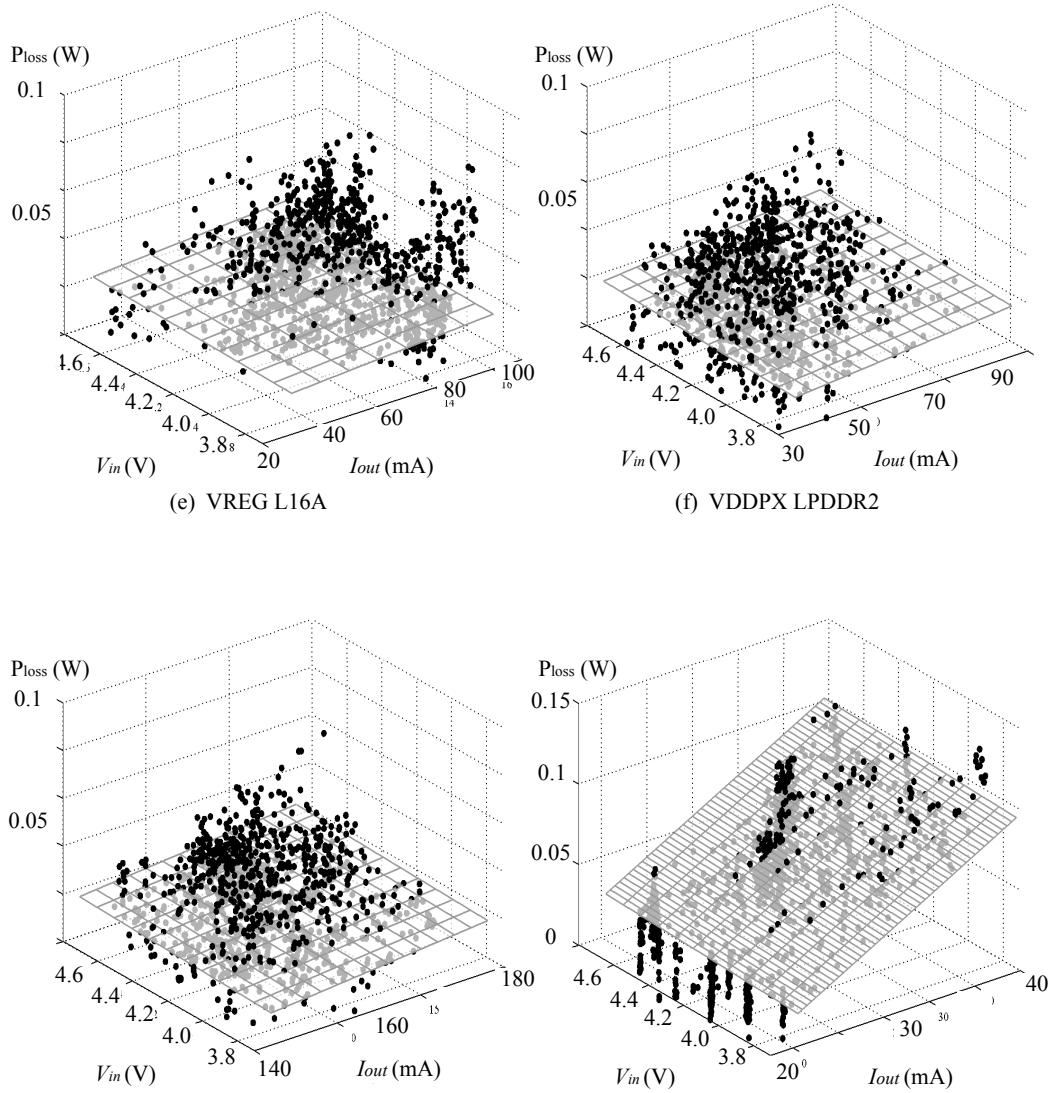


Figure 36: Regression result of P_{loss} with V_{in} and I_{out} for major power components in Snapdragon MDP (1/2).



(e) VREG L16A

(f) VDDPX LPDDR2

(g) DRAM VDD2

(h) Display ELVDD

Figure 37: Regression result of P_{loss} with V_{in} and I_{out} for major power components in Snapdragon MDP (2/2).

Table 6: Power consumption characteristics of target platform components (2/2).

Component	Supply Voltage (V)	Average current (mA)	Current standard deviation
Display IO	1.8	0.0603	0.0815
Display Memory	3	2.8102	3.7988
eMMC Host Interface	1.8	0.0549	0.3631
HDMI	5	0.0388	0.0555
Camera IO	1.8	0.1084	0.1374
Camera Digital	1.2	0.051	0.0669
Camera Analog	2.85	0.0494	0.071
DRAM VDD2	1.2	4.23	5.9156

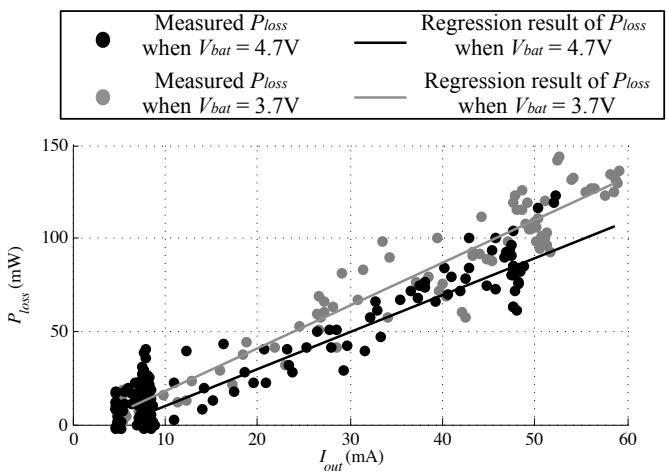


Figure 38: Regression result of P_{loss} with V_{in} and I_{out} for display device in Snapdragon MDP (2/2).

Table 7: Extracted parameters for power loss model

CPU	a_1	2.045e-4	a_2	7.152e-1	a_3	5.444e-4
Core0	a_4	1.217e-4	a_5	2.490e-3	a_6	7.641e-6
CPU	a_1	3.003e-4	a_2	5.703e-1	a_3	5.312e-4
Core1	a_4	2.236e-5	a_5	2.641e-3	a_6	7.641e-6
Digital	a_1	3.093e-3	a_2	7.133e-1	a_3	5.353e-4
core	a_4	2.026e-5	a_5	2.599e-3	a_6	7.641e-6
Internal	a_1	1.081e-3	a_2	8.456e-1	a_3	5.353e-4
memory	a_4	2.027e-5	a_5	2.597e-3	a_6	7.641e-6
VREG	a_1	9.451e-4	a_2	8.235e-1	a_3	5.209e-4
L16A	a_4	5.672e-5	a_5	2.609e-3	a_6	7.641e-6
VDDPX1	a_1	8.788e-4	a_2	5.967e-1	a_3	5.329e-4
LPDDR2	a_4	2.470e-5	a_5	2.502e-3	a_6	7.641e-6
DRAM	a_1	7.638e-4	a_2	6.286e-1	a_3	5.330e-4
VDD2	a_4	2.471e-5	a_5	2.601e-3	a_6	7.641e-6
Display	a_1	8.401e-3	a_2	1.571e0	a_3	2.340e-14
ELVDD	a_4	5.244e-4	a_5	5.011e-3	a_6	7.641e-6

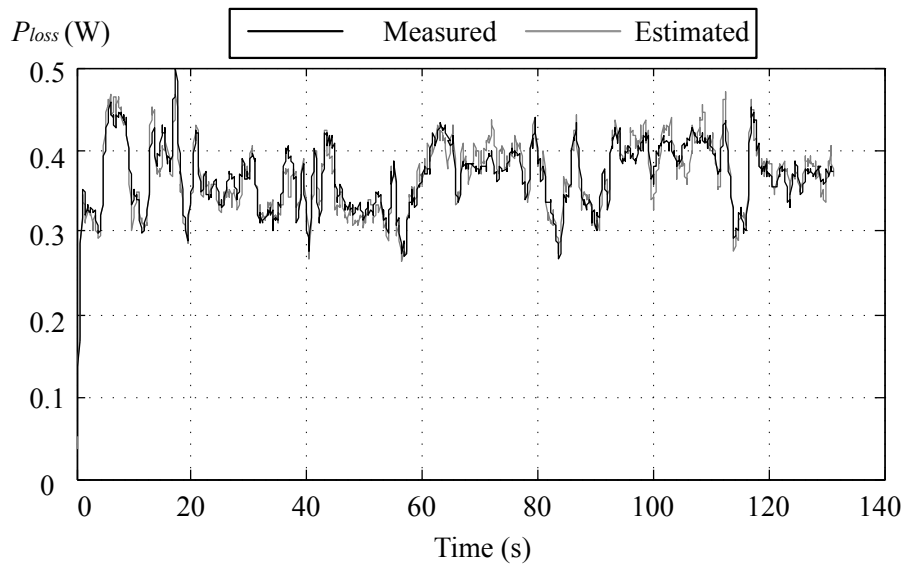


Figure 39: P_{loss} measurement result from the target platform and P_{loss} estimation result by the regressed model.

Table 8: MAX1790 Boost converter simulation parameters.

Parameter	Value	Parameter	Value
L	4.7 uH	R_L	46.4 mΩ
f_s	1.2 MHz	R_C	0.9 mΩ
R_{sw1}	21 mΩ	R_{sw2}	21 mΩ
C_{sw1}	12.8 pF	C_{sw2}	12.8 pF
R_d	20 mΩ	V_f	0.5 V

7.3 Power conversion efficiency for OLED power supply

We select a commercial switching-mode boost converter to characterize the power converter for the OLED display panel. We choose the MAX1790 from Maxim [52] which is used in an Odroid-A development platform from Hardkernel [53]. The Odroid-A platform is a high-end development platform for the smartphone and tablet PC which has has very similar features to Samsung Galaxy tab. We estimate the power efficiency of the boost converter by using the power loss model introduced in Section 6.1. We use the physical parameters of CDMC6D28NP-4R7MC power inductor from Sumida corporation [54], B120/B rectifier diode from Diodes inc. [55], and several capacitors form Taiyo Yuden [56]. The simulation parameters are summarized in Table 8.

The efficiency simulation result is illustrated in 40. We change the input voltage from 3.7 V (1-cell Li-ion battery) to 11.1 V (3-cell Li-ion battery) output voltage. The output current is up to 1600 mA which is the maximum rating of MAX1790. It shows that the efficiency is very with small output current due to the static power consumption of the boost converter including controller power and switching power. The efficiency gradually decreases after peak point because of the conduction loss. The input voltage affects the duty ratio of the PWM switch control and degrades the efficiency as the

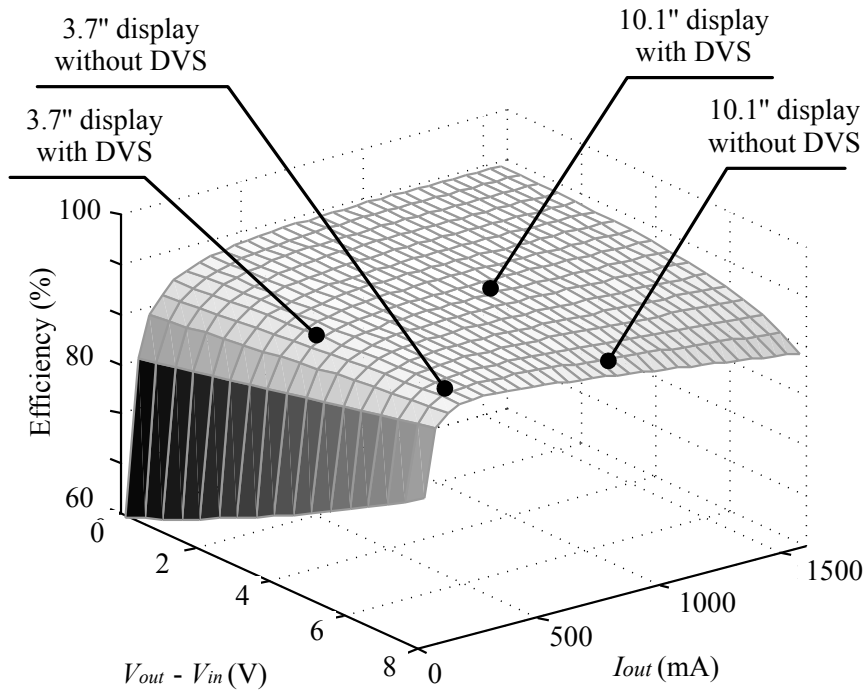


Figure 40: Simulation result of MAX1790 boost converter efficiency.

difference between the input and output voltage increasing.

7.4 Li-ion battery model

Battery models for the electronic systems have extensively been studied during the past few decades. We have found many analytical models based on electrochemical process modeling and analysis [23, 24], but the electrochemical battery models are too complicated to be used for the system-level design of electronics. Rather, battery models in the form of an electric circuit are much more suitable for this purpose [25, 26].

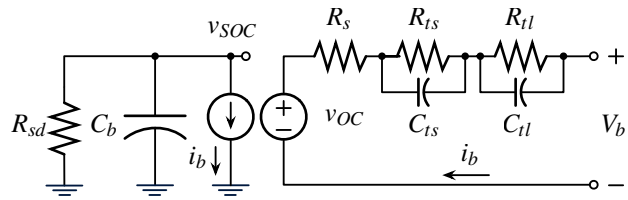


Figure 41: Li-ion battery equivalent circuit model.

We import a circuit model of the Li-ion battery from [26] as shown in Figure 41. This includes a runtime-based model as well as a circuit-based model for accurate capturing of the battery service life and I-V characteristic. We can describe the behavior of a Li-ion battery with the equivalent circuit and the following non-linear equations.

$$
\begin{aligned}
v_{OC} &= b_{11}e^{b_{12}v_{SOC}} + b_{13}{v_{SOC}}^3 + b_{14}{v_{SOC}}^2 + b_{15}v_{SOC} + b_{16}, \\
R_s &= b_{21}e^{b_{22}v_{SOC}} + b_{23}, R_{ts} = b_{31}e^{b_{32}v_{SOC}} + b_{33}, \\
C_{ts} &= b_{41}e^{b_{42}v_{SOC}} + b_{43}, R_{tl} = b_{51}e^{b_{52}v_{SOC}} + b_{53}, \\
C_{tl} &= b_{61}e^{b_{62}v_{SOC}} + b_{63}, C_b = 3600 \cdot Capacity,
\end{aligned} \tag{25}
$$

where b_{ij} are empirically-extracted regression coefficients, while $Capacity$ denotes the nominal energy capacity of the battery. Notice that all circuit model component values, such as value of R_s, R_{ts}, etc., are easily calculated from these equations based on v_{SOC} and $Capacity$ data.

7.4.1 battery model parameter extraction

We obtain the discharging characteristics of Li-ion battery by measuring and extracting the regression coefficients for (25). Table 9 shows the parameters for the GP1051L35

Table 9: Extracted parameters for the battery model.

b_{11}	-0.669	b_{12}	-16.208	b_{13}	-0.035
b_{14}	1.280	b_{15}	-0.399	b_{16}	7.553
b_{21}	0.104	b_{22}	-4.325	b_{23}	0.344
b_{31}	0.151	b_{32}	-19.602	b_{33}	0.188
b_{41}	-72.389	b_{42}	-40.832	b_{43}	102.803
b_{51}	2.071	b_{52}	-190.412	b_{53}	0.203
b_{61}	-695.302	b_{62}	-110.630	b_{63}	611.504

Li-ion cell 2-cell series battery pack of 350 mAh capacity, NessCap supercapacitor ESHSR0010C0-002R7 of 10 F capacitance [57], and Linear Technology LTM4607 converter. We validate the battery, supercapacitor, and the converter model with the measurement result of various pulsed discharging and constant discharging currents.

7.5 Battery setup optimization

We can change the distribution of the battery output (system input) voltage, V_{bat} by changing the connection of the battery cells. V_{bat} is determined by the number of battery cells in series. Li-ion battery typically has 3.7 V output voltage per cell. If we connect two cells in series, then V_{bat} would be 7.4 V. If we connect three cells in series, then V_{bat} would be 11.1 V. Figure 42 shows the distribution of V_{bat} during 1/2C discharging for GP105L35 Li-ion cell [49]. We use a Li-ion cell which has small capacity during characterization to shorten the experiment time. We measure the voltage and use its distribution to calculate the system efficiency.

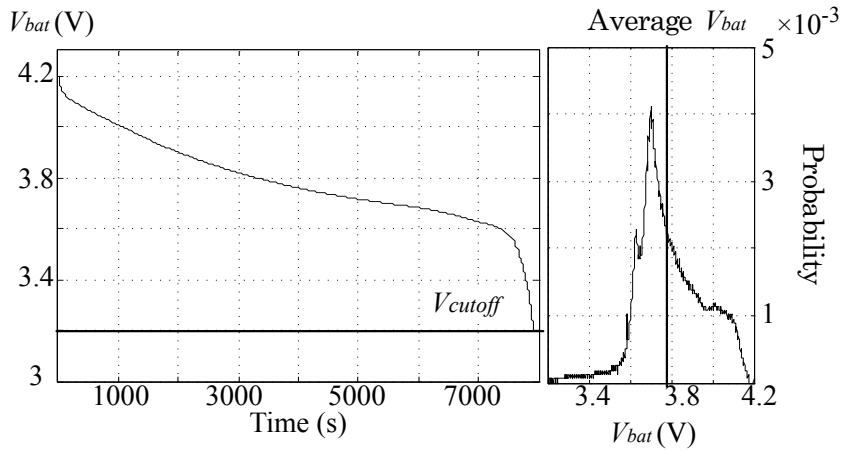


Figure 42: V_{bat} curve and distribution during discharging with average power.

8 Experiments

8.1 Simulation result for OLED display with AM driver

The implemented prototype equips PWM driver-based OLED display. We perform a simulation to evaluate the effect of OLED DVS with AM driver-based OLED display. Figure 43 shows the I-V characteristics of the driver gate. Based on the driver gate characteristics presented in Figure 43 and optical characteristics presented in Section 4.2, we evaluate the OLED DVS with several standard test images.

Figure 45 shows the result for a Lena, a mandrill, a boat and an airplane. We use the characterization result presented in Section 4.2 to calculate the power consumption and image distortion. The images in first row in Figure 45 are original test images. The second row is V_{DD}-scaled images constrained by the number of distorted pixels. We limit the number of distorted pixels within 5%. The average power saving is 37%.

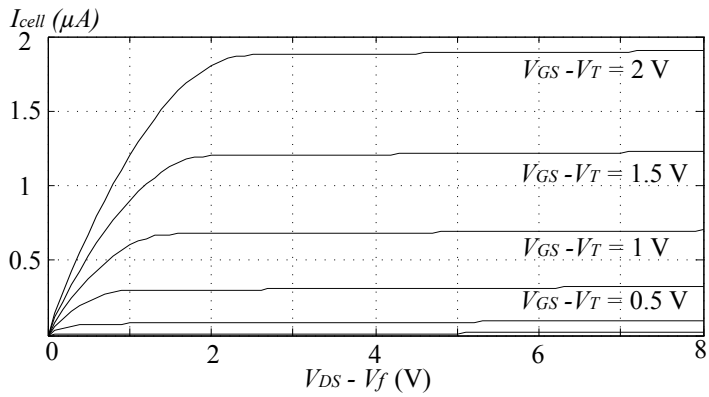


Figure 43: TFT driver gate characteristics for simulation of OLED panel with AM driver.

As described in Section 4.3 we cannot compensate the image distortion with the AM driver circuit due to the current mirror operation in the saturated region. Therefore, the distortion of bright pixel is not avoidable. We show the location of distorted pixels in the last row of Figure 45. The distorted pixel are represented by color inversion. We can see that the bright parts of the images are distorted.

We evaluate the histogram-based OLED DVS by simulation. Figure 46 shows the V_{DD} scaling and estimated power result for the movie clip. We use 10 seconds of movie clip from the 'How to Train Your Dragon.' The movie clip is carefully chosen to contain bright scenes and dart scenes keeping the balance. V_{DD} is scaled up to 9 V while play the movie clip. The original movie clip with 15 V V_{DD} shows 5.45 J energy consumption during 10 s, and a movie clip with a 5% distortion constraint shows 3.54 J.

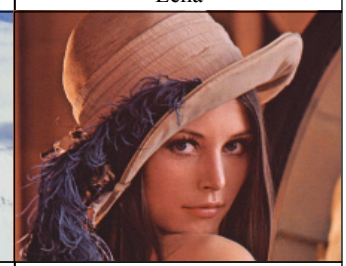
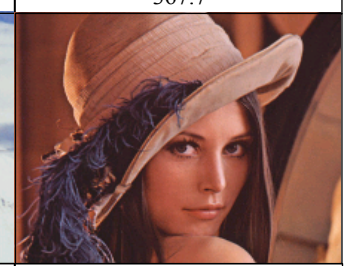
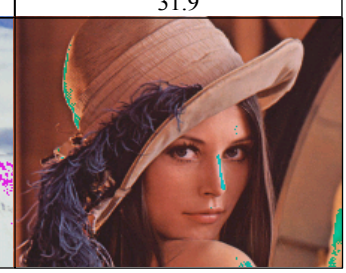
	Airplane	Lena
Original image		
V_{DD} (V)	15.0	15.0
Power (mW)	1412.9	367.7
Scaled image with 5 % distorted pixels		
V_{DD} (V)	9.32	9.49
Power (mW)	877.8	250.3
Saving (%)	44.1	31.9
Distorted pixels (inverted color)		

Figure 44: Simulation results for AM driver-based OLED display with standard test images (1/2).

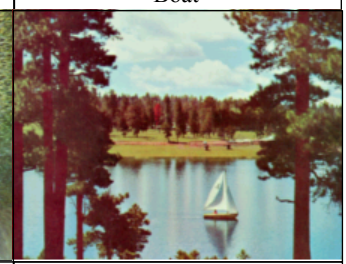
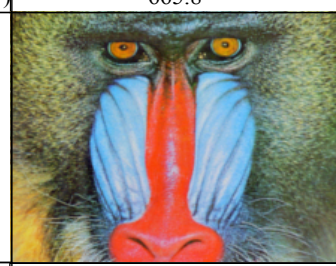
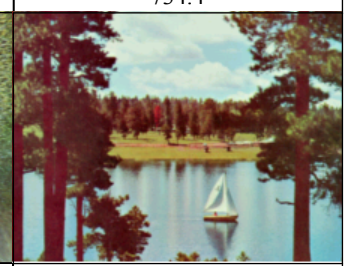
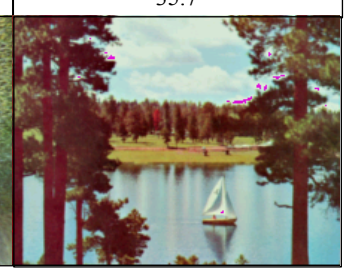
	Mandrill	Boat
Original image		
V_{DD} (V)	15.0	15.0
Power (mW)	665.8	734.4
Scaled image with 5 % distorted pixels		
V_{DD} (V)	9.55	9.64
Power (mW)	423.7	472.1
Saving (%)	36.3	35.7
Distorted pixels (inverted color)		

Figure 45: Simulation results for AM driver-based OLED display with standard test images (2/2).

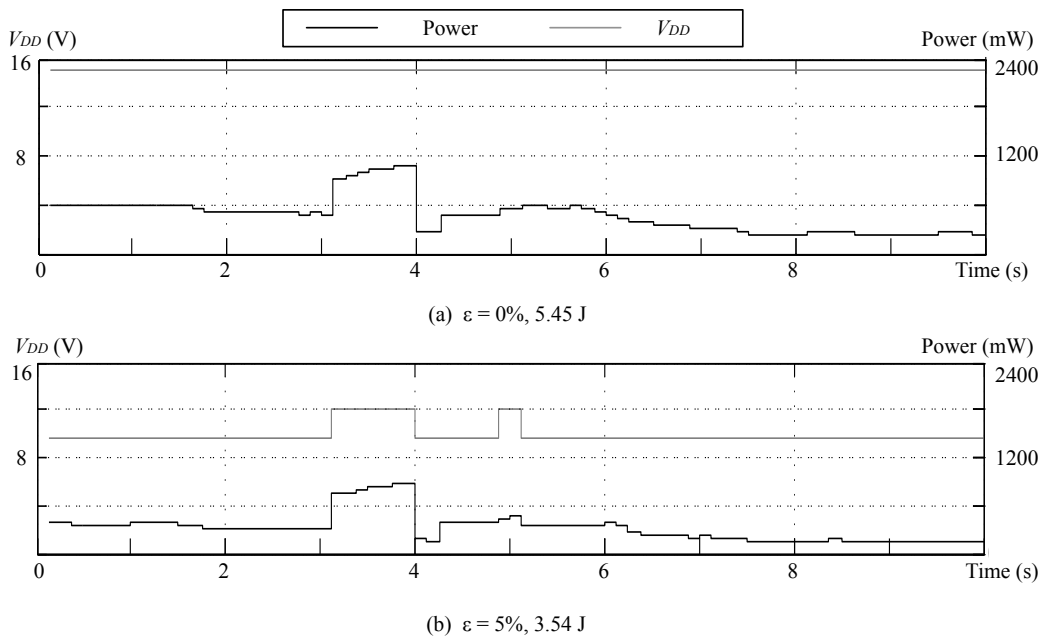


Figure 46: Simulation results of power consumption with OLED DVS for the movie clips with (a) 0% distortion tolerance (b) 5% distortion tolerance.

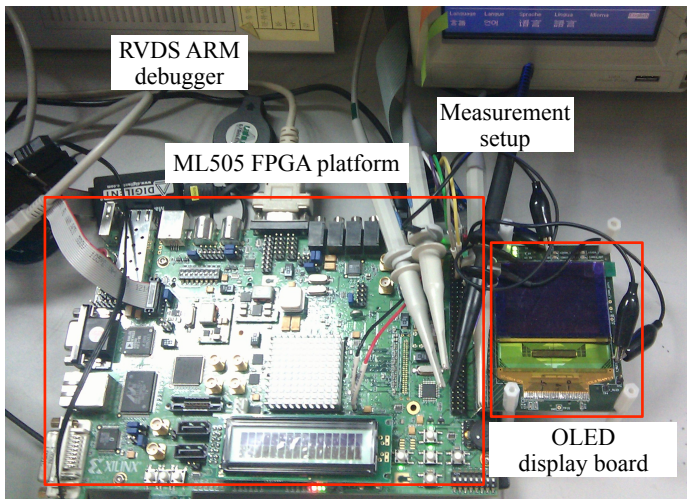


Figure 47: Experimental setup for the OLED DVS with the prototype implementation.

8.2 Measurement result for OLED display with PWM driver

We evaluate the power gain and resultant image quality from the proposed OLED DVS on real still images and image sequence from a movie clip. Figure 47 shows the experimental setup with the implemented prototype.

Figures 48 and 49 summarizes the result for the still images. We capture the displayed images on the target OLED display panel by digital camera. The Lena and mandrill images have a typical balanced color distribution while the boat and airplane images have a severe skew toward the bright colors, which is challenging for the OLED DVS. The originally high luminance pixels are saturated to the maximum luminance as shown in the compensated images and histograms. The saturated pixels result in the image distortion, but the overall image quality is not appreciably altered within the threshold value. The Lena image shows 52.5% power saving compared with the original image

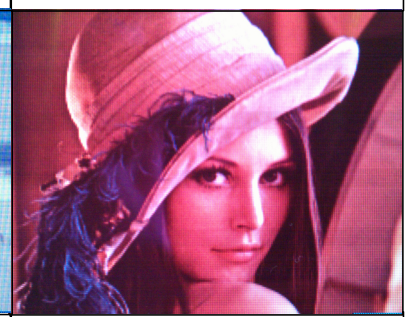
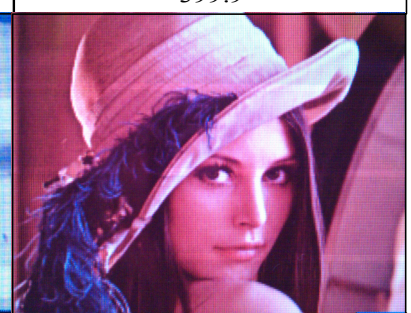
	Airplane	Lena
Displayed original images		
V_{DD} (V)	15.0	15.0
Power (mW)	731.7	399.9
Displayed scaled images		
V_{DD} (V)	12.0	8.7
Power (mW)	572.5	189.8
Saving (%)	21.8	52.5

Figure 48: Viewed image results in PWM driver equipped prototype with standard test images (1/2).

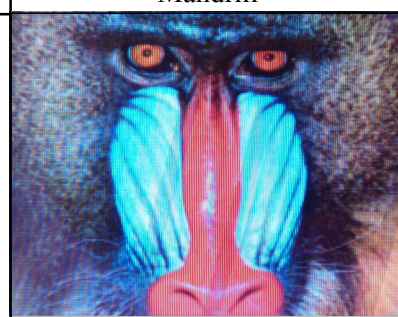
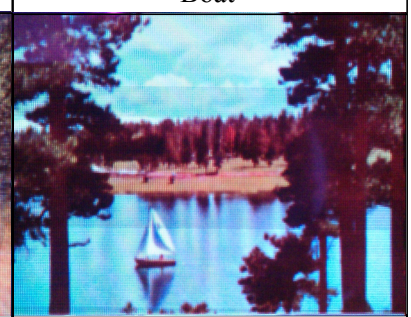
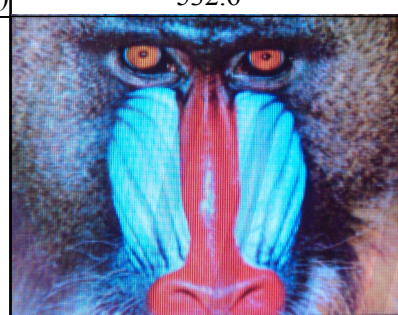
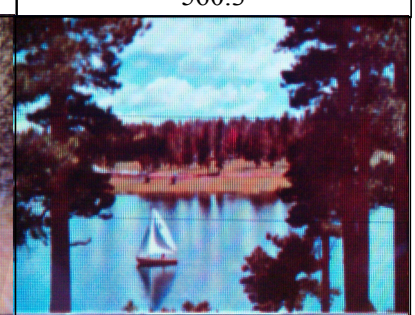
	Mandrill	Boat
Displayed original images		
V_{DD} (V)	15.0	15.0
Power (mW)	532.6	560.3
Displayed scaled images		
V_{DD} (V)	8.6	9.6
Power (mW)	134.4	161.0
Saving (%)	74.7	71.3

Figure 49: Viewed image results in PWM driver equipped prototype with standard test images (2/2).

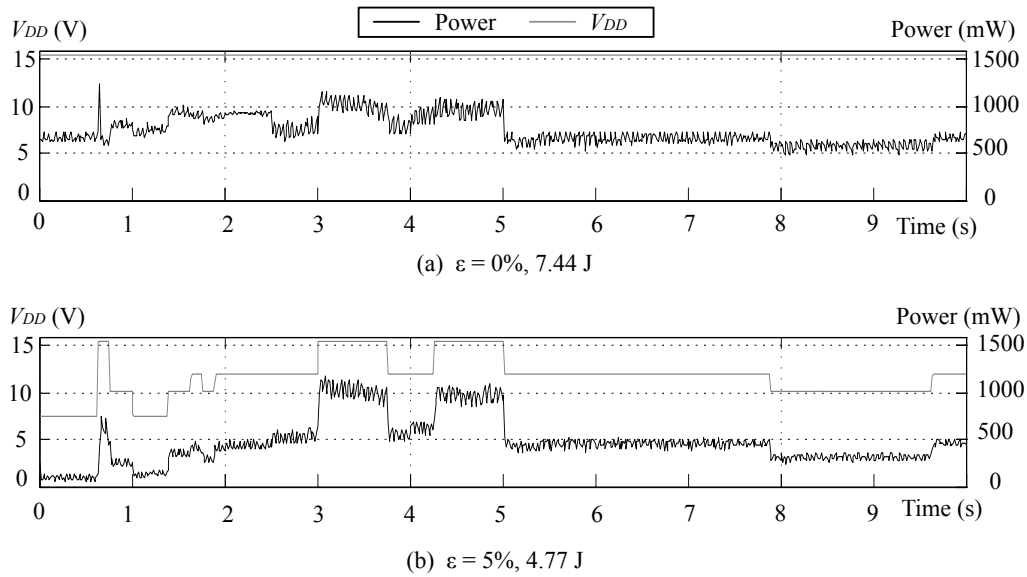


Figure 50: Measured power consumption with OLED DVS for the movie clips with (a) 0% distortion tolerance (b) 5% distortion tolerance

while V_{DD} being scaled down from 15 V to 8.7 V and with nearly zero color distortion. The mandrill image shows 74.7% power saving while V_{DD} being scaled down from 15 V to 8.6 V and with 300 as the average distortion. The boat image shows 71.3% power saving V_{DD} being scaled down from 15 V to 9.6 V and with 300 as the average distortion. As for the worst case among the benchmarks, the airplane still exhibits 21.8% power saving compared to the original image with 15 V V_{DD} for the threshold value of t_{image} = 300.

We measure the display power consumption while playing the same movie clip in Section 8.1 to evaluate the prototype and SoC. As shown in Figure 50, the original movie clip with a 15 V V_{DD} shows 7.44 J energy consumption during 10 s, and a movie clip

with a 5% distortion constraint shows 4.77 J. We confirm that V_{DD} is more aggressively scaled with larger distortion threshold in Figure 50.

8.3 Design space exploration of battery setup with OLED displays

We calculate the expectation of system power consumption, $\overline{P_{sys}}$, by summing the expectation of each power component power consumption, which is given by

$$\overline{P_{sys}} = \sum_{i=1}^{n} \int_{I_{min}}^{I_{max}} V_{supply}^{i} Pr(I_{out}^{i} = I) IdI \tag{26}$$

where I_{min} and I_{max} denote the minimum and maximum value of i-th component current I_{out}^{i}. $Pr(I_{out}^{i} = I)$ represents the probability that I_{out}^{i} equal to I. V_{supply}^{i} is the supply voltage for i-th component. Imin, Imax, and Ioiut are obtained from the measurement result in Section 7.2. We estimate the expectation of system level power loss, $\overline{P_{sys}}$, in similar way. Each P_{loss}^{conv} is integrated and then summed with the probability of each loss current, which is given by

$$\overline{P_{loss}^{sys}} = \sum_{i=1}^{n} \int_{I_{min}}^{I_{max}} P_{loss}^{conv,i}(V_{in}, V_{out}, I)) Pr(I_{out}^{i} = I) IdI \tag{27}$$

where $P_{loss}^{conv,i}$ is calculated by (24) and (25) with the coefficient in Table 6.

We calculate the internal loss of battery with the internal loss R_s, R_{ts}, and R_{tl}. We ignore the transient aspect of battery loss to simplify the model because the simulation time is order of hour.

$$\overline{P_{loss}^{batt}} = \int_{I_{min}}^{I_{max}} P_{loss}^{batt}(V_{batt}, I)) Pr(I_{batt}^{i} = I) IdI \tag{28}$$

We use the measured R_s, R_{ts}, and R_{tl} values presented in Table 8.

The output power from battery is equals to the sum of power consumption and power loss:

$$\overline{P_{batt}} = \overline{P_{sys}} + \overline{P_{loss}^{sys}} + \overline{P_{loss}^{batt}} \tag{29}$$

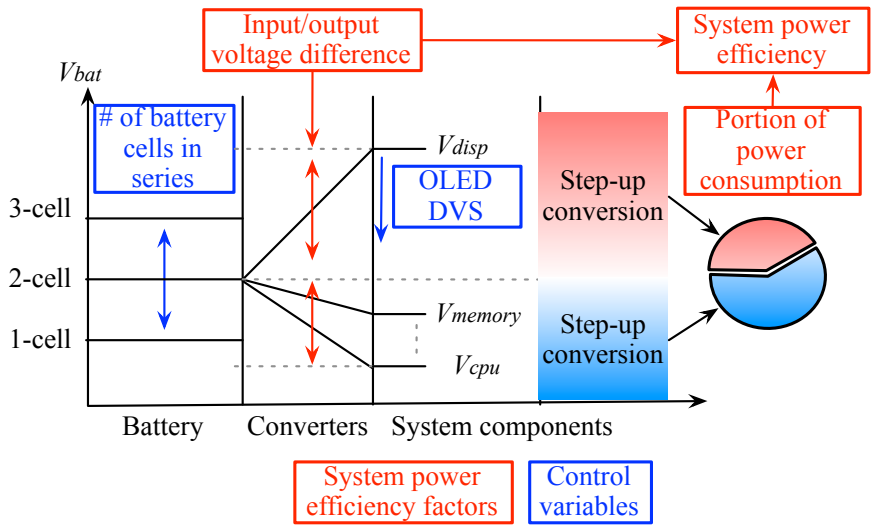


Figure 51: System voltage setup and efficiency with battery setup and OLED DVS.

Finally, we get the overall efficiency, $\overline{\eta_{oveall}}$, by

$$\overline{\eta_{oveall}} = \frac{\overline{P_{sys}}}{\overline{P_{batt}}} = \frac{\overline{P_{sys}}}{\overline{P_{sys}} + \overline{P_{loss}^{sys}} + \overline{P_{loss}^{batt}}}, \tag{30}$$

Figure 51 show the relation between the voltage setup of the system and its power efficiency. The supplied voltage values to the ICs and display are determined by its behavioral characteristics and opto-electrical characteristics. The portion of power consumption and corresponding conversion efficiency finally determine the system power efficiency. The system should be optimize under the consideration of the voltage setup and corresponding conversion efficiency. We can increase the input voltage of the conversion circuits from the battery by changing the battery setup and decrease the output voltage of the setup-up converter to the display by using OLED DVS. The battery voltage can be set in discrete manner by changing the number of the cells in series. The OLED DVS

reduces the supply voltage to the display in average. Consequently, we can extend the available design space to optimize the system when we use those two techniques at the same time.

Figure 52 shows the aspect of P_{loss} with different display power consumption, P_{disp}, and battery output (system input) voltage, V_{bat}. The marker on the surface represent the 1-cell, 2-cell, and 3-cell battery setup. We get the average power consumption of different size OLED display. We use the cell model introduced in Section 3 and TFT model introduced in [58] to estimate the average power consumption of different sized OLED panel. Solid lines with the markers in Figure 52 respectively indicate the average power consumption of 220x176, 640x480, 800x600, and 1024x768 resolution displays which correspond to 3.7" and 10.1" size, respectively. As shown in Figure 52, we can minimize the the power loss of 2.2", 3.7", 5.4", and 10.1" size displays with 1-cell, 1-cell, 2-cell, and 3-cell, respectively. The expected system-level power efficiency is illustrated in Figure 53. If we use 1-cell battery, overall efficiency is decreasing with larger than 640×480 display.

The OLED DVS reduce the effect of voltage difference on the conversion efficiency because it reduce the supply voltage on average. Figures 54 and 55 show P_{loss} and $\eta_{overall}$ with OLED DVS-enabled system. The power consumption of the display is reduced, which result in the optimal number of battery cells in series in generally decreased.

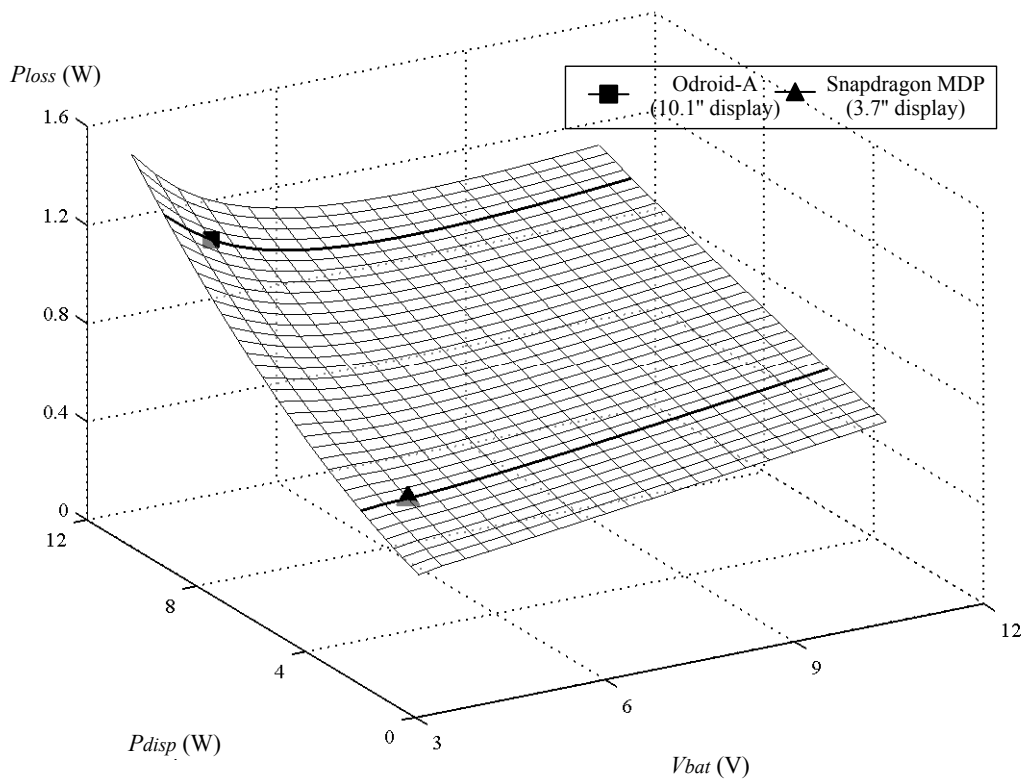


Figure 52: Simulation result of $\overline{P_{loss}^{sys}} + \overline{P_{loss}^{batt}}$ for different V_{bat} and P_{disp} without OLED DVS.

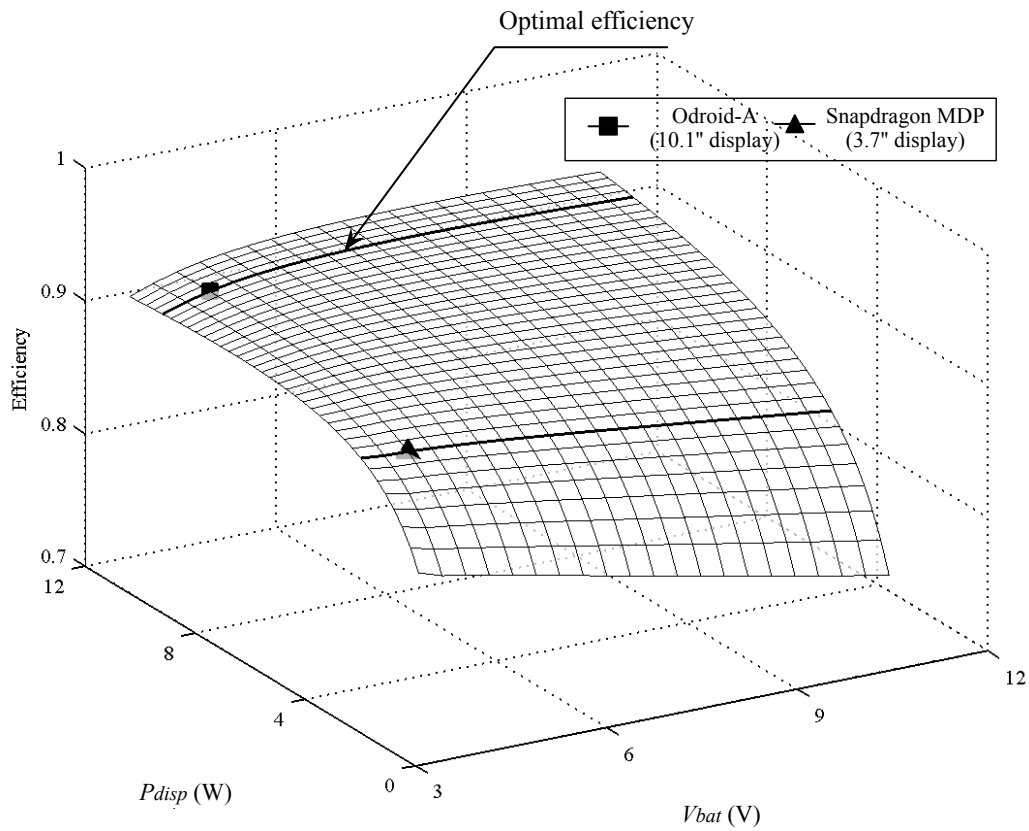


Figure 53: Simulation result of $\eta_{overall}$ for different V_{bat} and P_{disp} without OLED DVS.

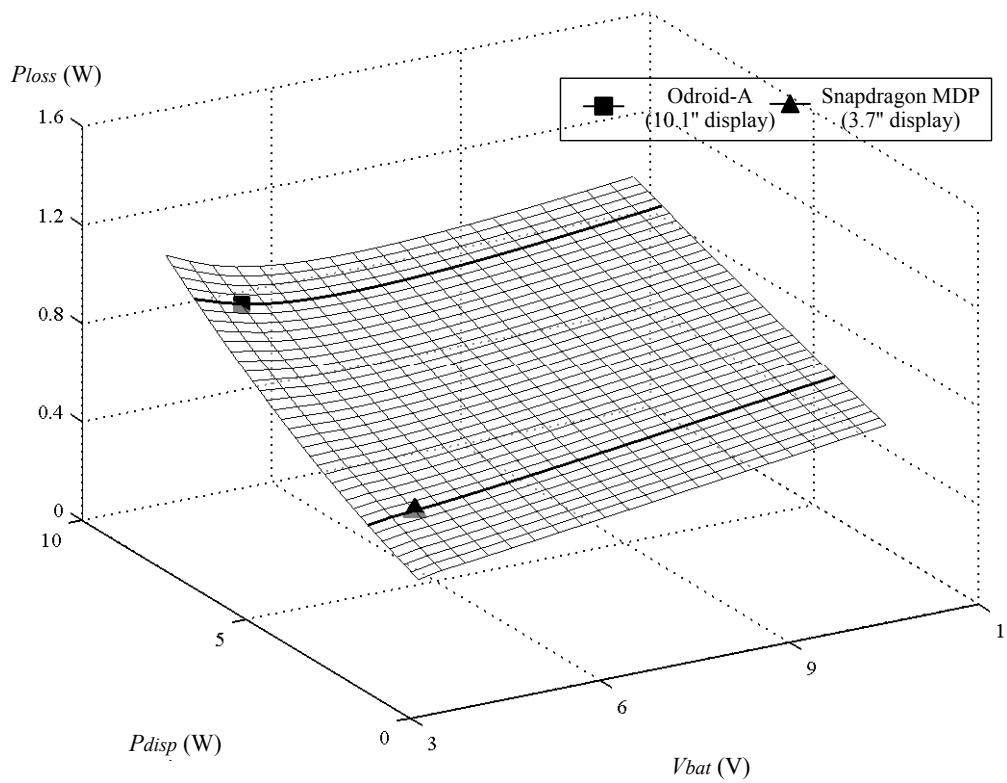


Figure 54: Simulation result of $\overline{P_{loss}^{sys}} + \overline{P_{loss}^{batt}}$ for different V_{bat} and P_{disp} with OLED DVS.

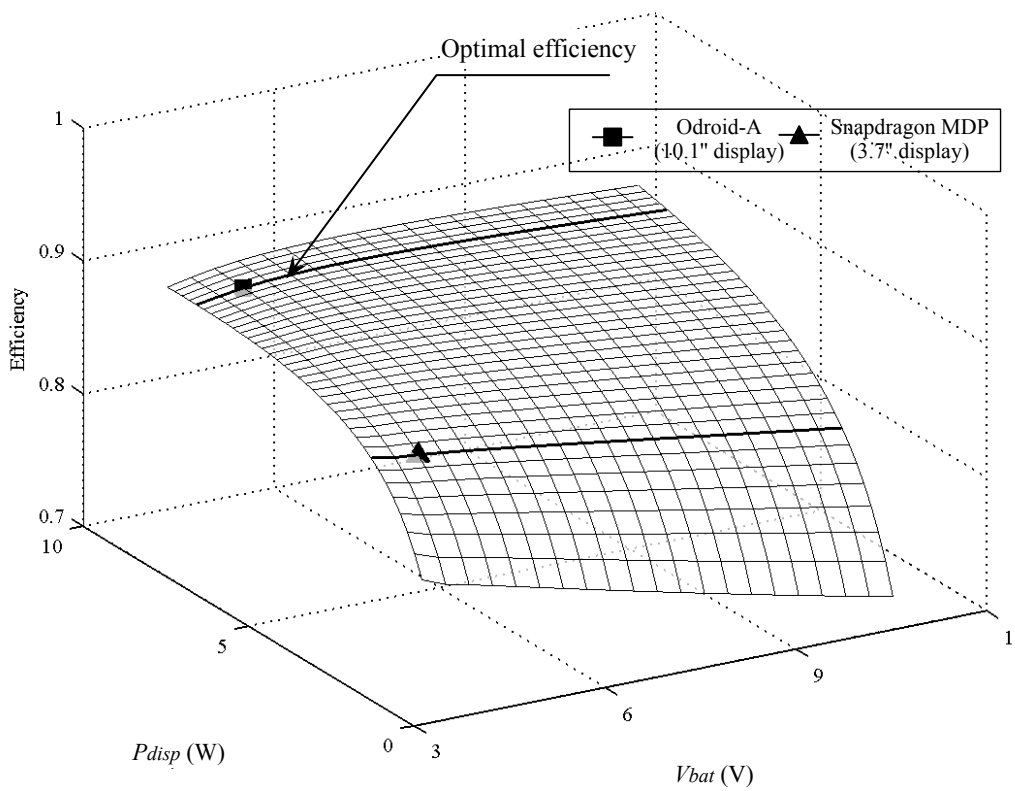


Figure 55: Simulation result of $\eta_{overall}$ for different V_{bat} and P_{disp} with OLED DVS.

9 Conclusion

Organic light emitting diode panels are promising display devices capable of self-illumination and thus exhibiting high power efficiency. However, even such a high-efficiency OLED panel generally consumes more power than a microprocessor that is present in the same system. All previous OLED power saving methods change the pixel colors since the pixel color determines the OLED power consumption. Unfortunately, these methods result in significant degradation of the image.

This paper presented the first OLED power saving method that enables only minimal pixel distortion, small enough to work with natural images. Furthermore, the proposed technique can be applied to most OLED panel structures. We developed such a unique power saving technique based on a careful analysis of the OLED driver architectures. The proposed method is called OLED dynamic voltage scaling (OLED DVS). The idea is to scale down the supply voltage and, in turn, dramatically reduce the wasted power caused by the voltage drop across the driver transistor as well as internal parasitic resistance. The proposed OLED DVS may incur image distortion after the supply voltage scaling. In this case, we compensate the image data based on the human-perceived color space.

We develop a prototype implementation of a supply voltage control circuit and an image compensation method allowing OLED DVS and image compensation. We demonstrated the OLED DVS for a still images with a prototype implementation and confirmed significant power saving for the Lena image with virtually zero distortion. We will measure the power saving of the OLED DVS for the sample movie clips by the using the prototype.

OLED display-equipped modern mobile devices such as smartphones and table PCs are suffer from rapidly increasing power consumption. Furthermore, traditional power

conversion architecture in the mobile computing system is designed only considering the fixed supply voltage condition where the system-level low-power techniques such as DVFS are mandatory. Therefore, we should consider the operating condition of the major power consumers including microprocessor and display to enhance the system-level power delivery efficiency.

In this dissertation, we not only optimize the power consumption of the OLED display but also consider it's effect on the whole system power efficiency. We perform the optimization of the battery setup by a systematic method instead of the legacy design rule that uses 1-cell Li-ion batteries for smartphones and tablet-PCs and from 3-cell to 5-cell Li-ion batteries for laptop PCs. We optimize not only the power consuming components or the conversion system but also the energy storage system based on the battery model and system-level power delivery efficiency analysis.

The estimation result shows that we can expect higher power conversion efficiency with 2-cell Li-ion batteries when the size and power consumption of the display are growing (which means that portion of the boosted power is growing). The battery setup and charging circuit have been standardized for several decades. It is clear that the legacy design rule cannot guarantee the optimal solution anymore, but it requires significant effort to change the standard. The OLED DVS may slacken this tendency by reducing the boosting voltage on average. The one who designs the mobile system should understand the characteristics of the components and the mechanism of power delivery to find appropriate solution which cannot be found by just following the legacy design rule without systematic analysis.

10 Future Work

Supercapacitors have superior characteristics over batteries in terms of their cycle efficiency. The cycle efficiency, which is defined as the ratio of the energy input to energy output of an electrical energy storage element, reaches almost 100% [57]. We model the supercapacitor by a connection of various circuit elements. More precisely, the equivalent circuit model incorporates a transmission line behavior, a parasitic inductor model, a charge redistribution element, and a self-discharging current model [59].

Key parameters of the supercapacitors in the hybrid system are the voltage rating and capacitance. These parameters are directly related to the energy transfer efficiency and energy density of the proposed system. The capacitance value of the supercapacitor affects the efficiency due to its filtering effect on the pulsed load. Moreover, the volume of the supercapacitor is determined by its capacitance value and voltage rating. Because different amounts of charging current result indifferent steady states, the value of charging current results in different requirement for the voltage rating for the supercapacitor. These two design parameters, i.e., the supercapacitor capacitance and charging current, also strongly influence the efficiency of the regulator. The operating conditions of the switching DC-DC converters, battery, and supercapacitor should be considered as constraints.

The volume, weight, and cost are limited in the mobile systems different from the desktop PCs. As a future work, we will optimize the portion of batteries and supercapcitors in the hybrid energy storage from the perspective of energy density and cost to maximize the user satisfaction.

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초록

오늘날 스마트폰, 태블릿 PC 와 같은 휴대용 전자기기는 고성능의 중앙처리장치(CPU), 대용량 메모리, 대형 화면, 고속의 무선 인터페이스 등을 탑재함에따라 전력 소모량이 급속히 증가하여 그 전력 소모는 이미 소형의 랩탑 컴퓨터 수준에 이르고 있다. 성능과 전력 소모량의 측면에서 휴대용 전자기기와 랩탑 컴퓨터 사이의 구분이 점차 사라지고 있음에도 배터리 및 전력 변환 회로는 기존의 설계 원칙들만을 따라 설계되고 있는 실정이다. 삼성전자의 갤럭시 탭 및 Apple 사의 iPad 등 스마트폰 및 태블릿 PC의 경우 1-cell 직렬 리튬 이온 전지를 사용하는 반면, 랩탑 컴퓨터의 경우는 제조사에 따라 3-cell 에서 5-cell 직렬 등으로 설계되고 있다. 이는 배터리 출력 전압을 다르게 함으로써 전력 변환 효율에 영향을 준다.

전력 변환 회로의 효율 및 배터리의 수명은 입출력 전압/전류를 비롯한 동작 환경의 영향을 받는다. 휴대용 전자기기에 사용되는 각종 전자부품은 전력 소모를 줄이기 위한 다양한 기능들을 구현하고 있으며, 중앙처리장치의 동적 전압/주파수 조절 기법 등 공급전압의 변화를 수반하는 기법 역시 다양하게 적용되고 있다. 이는 각 장치의 공급 전압 및 전류의 변화로 인한 전력 변환 회로의 효율의 변화를 초래한다. 따라서 중앙처리장치, 디스플레이 등 주요 전력 소비 장치의 전력 절감 기법을 개발할 때에는 개별 장치의 전력 소비를 줄이는 것과 동시에 개별 장치의 동작 행태에 대한 정확한 분석에 기반하여 배터리, 전력 변환회로의 설계가 함께이루어져야 한다. 선행 연구를 통해 배터리의 특성을 고려한 배터리 구성의 최적화 기법이 제안되었다 [1].

중앙처리장치의 동적 전압/주파수 제어 기법에 이어 유기발광다이오드(OLED) 기반 디스플레이의 동적 구동회로 공급 전압 기법이 제안되었다 [2]. 유기발광다이오드 디스플레이는 전력 소모 및 시야각 등 기존 액정 표시장치에 비해 여러 우수한 특성으로 인해 주목받고 있는 차세대 디스플레이 장치이다. 유기발광다이오드 디스플레이의 적은 전력 소모량에도 불구하고 화면의 대형화 및 해상도의

고밀도화에 따라 시스템 전력 소모에서 여전히 큰 비중을 차지하고 있다. 유기발광다이오드 디스플레이의 동적 구동회로 공급 전압 기법(OLED DVS)는 색상의 변화의 기초한 기존의 유기발광다이오드 디스플레이 전력 절감 기법과는 달리 최소한의 이미지 왜곡만을 수반하여 대부분의 사진, 동영상 등에 적용가능한 전력 절감 기법이다. 해당 기법은 공급 전압의 변화시킬 필요가 있으며, 이를 시스템에 올바르게 통합시키기 위해서는 전력 변환 회로 및 배터리 구성에 미치는 영향을 고려해야 한다.

본 논문에서는 유기발광다이오드 디스플레이의 전력 소모와 함께 전체 시스템 효율에 미치는 영향을 함께 고려하여 시스템을 최적화한다. 배터리 구성 역시 기존의 설계 표준 대신 체계적인 시스템 분석에 기반한 최적화가 시도되었다. 공급전압이 조절 가능한 유기발광다이오드 디스플레이 하드웨어 및 제어기 시스템-온-칩 (System-on-a-chip, SoC) 가 제작되었고, 그 동작 특성이 분석되었다. 기존 스마트폰 및 태블릿 PC 개발용 플랫폼의 전력 변환 효율 및 동작 특성 역시 분석되었다. 유기발광다이오드 디스플레이의 동적 구동회로 공급 전압 기법의 동작 특성 및 스마트폰 플랫폼의 동작 특성, 배터리 특성에 대한 분석을 기반으로 시스템 수준에서의 전력 변환 효율이 최적화되었다.

감사의 글

무엇보다도 학위 과정 동안 열정적으로 지도해주신 장래혁 교수님과 여러 전기. 컴퓨터공학부 교수님들께 먼저 감사의 인사를 드립니다. 학위 과정을 마치고 이제 독립적인 연구자로서 자신의 몫을 다할 수 있도록 더욱 노력하겠습니다. 연구나 생활 모든 면에서 저의 든든한 버팀목이 되어주었던 여러 연구실 선배님들과 미국에서 같이 고생했던 재현이, 영현이, 상용이를 비롯한 후배들에게도 진심어린 감사 인사를 전하고 싶습니다.

논문을 통해 관련 분야의 연구의 작은 기여라도 할 수 있었다면, 저를 늘 바라보고 격려해 주셨던 어머님과 부족한 손자와 조카를 늘 자랑스러워 하시다 돌아가신 할머님과 작은 아버지, 막내 삼촌 덕분임을 되새기면서, 어려운 때에도 저를 늘 묵묵히 지켜준 여러 친구들과, 앞으로 아내가 되어 평생을 함께하게 될 사랑하는 빛나씨에게 감사의 인사를 드립니다.