



저작자표시-비영리-변경금지 2.0 대한민국

이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:



저작자표시. 귀하는 원저작자를 표시하여야 합니다.



비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.



변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 [이용허락규약\(Legal Code\)](#)을 이해하기 쉽게 요약한 것입니다.

[Disclaimer](#)

공학박사 학위논문

**High quality GaP and InP growth on
Si (001) substrates by MOCVD**

MOCVD를 이용한 실리콘(001) 기판 위에
고품질 GaP 및 InP 성장에 대한 연구

2015년 2월

서울대학교 대학원

재료공학부

이 상 문

High quality GaP and InP growth on Si(001) substrates by MOCVD	
2015	
이 상 문	
↑ 2cm ↓	↑ 2.5cm ↓
	↑ 4cm ↓
	↑ 3cm ↓
	↑ 2cm ↓

Abstract

High quality GaP and InP growth on Si (001) substrates by MOCVD

Lee Sangmoon

Department of Materials Science and Engineering

College of Engineering

Seoul National University

High-quality epitaxial growth of III-V on silicon substrates has been of great interest for many years due to because of the potential for monolithic integration of III-V based devices with Si metal-oxide semiconductor (MOS) integrated circuits and high performance and low power logic devices. Particularly, integration of III-V on Si can open up opportunities for new functionalities and multiple integration platforms, such as terahertz electronics, optoelectronics, integrating logic and communication platforms on the same Si wafer.

In this dissertation, the epitaxial growth of InP layers on Si (001) substrates by selective area growth (SAG) has been studied in order to explore the potential applications as mentioned before. High quality InP layers were grown using a thin GaP buffer layer in SiN_x trenches on Si (001) substrates. There are three main challenges for growth of high quality epitaxial layers.

The first challenge is the high defect density in the epitaxial layers due to the large lattice mismatch between InP and the Si substrates. The second is the large difference in thermal expansion coefficient between InP and the Si substrates or SiN_x mask in SAG. Last one is the generation of polar/non-polar interfaces between InP and Si substrates. The main focus of this work is to understand the defect formation mechanism as well as to develop solutions for defect reduction and to grow InP layers having extremely flat top surface for CMOS applications without CMP process.

A thin GaP buffer layer is used as the intermediate layer between the InP and the Si substrates to alleviate the large lattice mismatch and to facilitate the InP nucleation. We find the optimized growth condition of GaP layers on exact Si (001) substrate through a multi-step MOCVD process to achieve such high quality GaP/Si (001) template substrates by planar method. We have investigated the generation process of low defects in GaP layers grown on Si substrates by FME. It was found that there were optimized growth conditions as growth temperature, V/III ratio and growth rate. RMS roughness is 2.8 nm from the optimized growth conditions. InP epilayers were grown on Si substrates using buffer layers of GaP. AFM, SEM and TEM examination results showed that GaP is a proper material as a buffer layer, and that its optimum thickness is about 3~5nm. TEM observation showed that the inserted InGaAs strained layers were very helpful to reduce the surface roughness and defect reduction. It also confirmed that GaP acted as a buffer to

alleviate the lattice mismatch between InP and Si. The best AFM roughness obtained from inserted InGaAs strained layers was 2.1nm for $5 \times 5 \mu\text{m}^2$.

Next, we also propose a new scheme of SiN_x mask for SAG process to grow InP layers with high quality and flat top surface by applying to mask with etched Si surfaces and rounded top shape SiN_x . The extremely flat InP top surface is obtained by the optimized SiN_x mask for SAG.

In last part, we investigated SAG of InP layers on patterned Si substrates with InP/GaP buffer layers at various growth temperatures ranging from 500 °C to 650 °C. In order to grow high quality InP, a thin GaP buffer layer was grown on stepped sidewall surfaces of etched Si. The different growth temperature resulted in different top surfaces. The high quality InP layer with smooth surface can be attributed to the dislocation necking effect together with the formation of void. Finally we demonstrated the formation of InGaAs/InP heterostructures using the suggested InP templates, which can be used in applications of electronic devices.

Keywords: Indium phosphide, Gallium phosphide, Selective Area Growth (SAG), Metalorganic chemical vapor deposition (MOCVD), defect necking, Anti-phase boundary (APB), Surface morphology

Student Number: 2011-30192

Contents

Abstract	I
Contents.....	V
List of Tables	IX
List of Figures	X

Chapter 1. Introduction.....1

1.1 Motivation	3
1.2 Si and III-V material properties.....	7
1.3 Thesis organization	11
1.4 References	13

Chapter 2. Growth and characterization of InP on Si.....15

2.1 Challenges of InP growth on Si.....	16
2.1.1 Lattice mismatch.....	16
2.1.2 Thermal mismatch	18
2.1.3 Defects Associated to Polar on Non-Polar Epitaxy	19
2.2 Metalorganic Chemical Vapor Deposition (MOCVD) system	30
2.2.1 Overview	30
2.2.2 MOCVD system.....	32
2.2.3 Source Molecules.....	33
2.2.4 Principle of MOCVD.....	36
2.3 Characterizations.....	44
2.3.1 Nomarski DIC microscope	44
2.3.2 Field emission scanning electron microscopy (FE-SEM)...	45
2.3.3 Transmission electron microscopy (TEM).....	45

2.3.4	Atomic force microscopy (AFM)	46
2.3.5	High resolution X-ray diffractometry (HR-XRD)	46
2.4	References	47

Chapter 3 GaP blanket growth on Si (001) substrates52

3.1	Introduction	53
3.2	Experimental details	58
3.3	Results and discussions	59
3.3.1	Optimization of LT GaP layers on Si	60
3.3.2	Optimization of HT GaP layers on Si	72
3.4	Summary	78
3.5	References	79

Chapter 4 Heteroepitaxial InP growth on Si(001)and Ge (001) substrates.....81

4.1	Introduction	82
4.2	Experimental details	84
4.3	Results and discussions	86
4.3.1	Heteroepitaxial InP growth on Si(001) and Ge(001) substrates.....	86
4.3.2	Optimization of InP growth on Si using GaP buffer	99
4.4	Summary	101
4.5	references	102

Chapter 5 SAG of high quality InP on Si substrate using a GaP thin buffer layer105

5.1	Introduction	106
5.2	Experimental details.....	108
5.3	Results and discussion.....	110
5.3.1	Effects on growth temperature on surface morphology	110
5.3.2	Defect formation mechanisms	121
5.4	Summary	129
5.5	References	131
Chapter 6 Conclusions		134
	국문 초록	138
	List of publication	142
	감사의 글	146

List of Tables

Table 1-1. Physical properties of common group IV and III-V semiconductors [5].....	8
Table 2-1. Thermal pyrolysis (or decomposition) of various metal–organic (MO) and gas sources.	35

List of Figures

Figure 1-1 Microprocessor performance increase due to scaling [9]	3
Figure 1-2 Active and standby power density trends plotted from industry data. The extrapolations indicate a cross over below 20nm gate length [10].....	4
Figure 1-3 The chain of communication systems versus the length of the interconnection and the business volume of the corresponding technology. (Source: Intel).....	5
Figure 1-4. Illustration of types of optical and electrical propagation and their velocities [11]	6
Figure 1-5. Primitive cells of diamond (a) and zinblende (b) crystals. The two identical sublattices in the diamond crystal structure are shifted toward each other along the diagonal direction. The zinblende crystal structure has two sublattices composed of different elements.	9
Figure 1-6. Example of heterointegration of Ge and III-V MOS transistors on a Si substrate. Different device structures can be made on the strain-relaxed III-V and Ge buffer layers. On the left, a quantum- well device architecture is shown and the III-V barrier layer is inserted to block the source-to-drain leakage current. On the right shown is Ge channel strain engineering by embedded source and drain.....	10
Figure 2-1 Band gap energy and lattice constant of various III-V and IV semiconductors at room temperature [3]..	17
Figure 2-2 Schematic diagram of anti-phase domains boundaries in InAs formed by a single-atom step on the silicon substrate surface. Figure modified according to reference [11]..	22

Figure 2-3 Schematic diagram of anti-phase domains boundaries in InAs formed by a single-atom step on the silicon substrate surface. Figure modified according to reference [11]..	22
Figure 2-4 Self-annihilation anti-phase domains on [011] plane in a (001) zinc blende semiconductor by the close proximity of bonding of two APD faces. Figure modified according to reference [9]..	25
Figure 2-5 HR-TEM image of stacking faults defects found in InP/GaP/Si system.	27
Figure 2-6 HRTEM image of micro twin and stacking faults defects (S1,S2) in GaP/Si system. Figure modified according to reference [24].....	29
Figure 2-7 Schematic illustration of the MOCVD system [Aixtron].	31
Figure 2-8 (a) Layout of the AIX 2400 G3 susceptor in the 8×3 inch. (b) Photo of the reactor chamber of the AIX 2400 G3 in the 8×3 inch configuration.....	32
Figure 2-9 (a) Schematic illustration of the line for metal–organic (MO) source provided by bubblers.....	33
Figure 2-10 (a) Schematic illustration of the flow into the reactor, gas velocity decreasing near the susceptor surface, and boundary (stagnant) layer. The δ represents the thickness of boundary layer. The gas flow feeds from left side ($x < 0$, upper stream of the reactor) to right side ($x > 0$, downstream of the reactor) of this figure. The black rectangle lied on the susceptor represents the growth substrate. The vertical axis represents the direction, which is perpendicular to the surface of the susceptor or to the growth surface of the substrate. (b) Schematic illustration of the some kinds of mechanisms involved in the MOCVD process.....	38
Figure 2-11 Schematic illustration of the some kinds of mechanisms involved in the selective–area (SA) MOVPE process.....	40
Figure 2-12 Schematic of arsenic–trimer coverage on GaAs (111)B surface.	43

Figure 3-1. Sketch of the APB formation in the {111} and {110} lattice planes of the GaP zinc-blende structure due to the presence of monolayer steps on the Si surface..... 56

Figure 3-2 Growth sequence of InP/GaP epilayers on Si substrates. 59

Figure 3-3 AFM images of the surface of bare Si substrates after annealed at 830 °C for 30min in different reactor pressures of H2 ambient. (a) no annealing (b) 100 mbar (c) 500 mbar (d) 950 mbar..... 61

Figure 3-4 AFM images of the surface of bare Si substrates after annealed at 830 °C for different annealing time in 100 mbar reactor pressures of H2 ambient. (a) 15min (b) 30min (c) 120min. 62

Figure 3-5 AFM images of the surface of bare Si substrates after annealed at 830 °C for 30min in 100 mbar reactor pressures of H2 ambient using different substrate orientations. (a) exact (b) 2° off (c) 4° off (d) 6° off toward [110] direction respectively..... 63

Figure 3-6 SEM micrographs of LT-GaP layers grown at different growth temperature after annealed at at 830 °C for 30min in 950 mbar reactor pressure. (a) 450 °C (b) 500 °C (c) 550 °C respectively. 65

Figure 3-7 SEM images of LT-GaP layers grown at different growth temperature after annealed at at 830 °C for 30min in 500 mbar reactor pressure, (a) 400 °C (b) 425 °C (c) 450 °C respectively..... 65

Figure 3-8 SEM images of LT-GaP layers grown at different growth temperature after annealed at at 830 °C for 30min in 100 mbar reactor pressure. (a) 400 °C (b) 425 °C (c) 450 °C respectively..... 66

Figure 3-9 SEM images of LT-GaP layers grown at 450 °C after annealed at

830 °C for 30min in different reactor pressure, (a) 950 (b) 500 (c) 100 mbar respectively.....	67
Figure 3-10 RMS roughness as LT-GaP growth temperature for different H2 annealing reactor pressure (a) 100 mbar marked as a solid square (b) 500 mbar marked as a solid circle.....	68
Figure 3-11 SEM and AFM images of LT-GaP layers grown at different V/III ratio and growth rate of (a) V/III=5000, growth rate=0.16Å (b) V/III=1000, growth rate=0.22Å, (c) V/III=500, growth rate=0.25Å respectively. All of samples are grown at 425 °C after annealed at 830 °C for 30min in 150 mbar reactor pressure.....	68
Figure 3-12 Schematic depiction of the time dependences of the metal organic precursor injection during continuous (a) or flow rated modulated (b) epitaxy. The nucleation was either started by P for both cases.....	70
Figure 3-13 AFM images of LT-GaP layers grown at 400 °C after annealed at at 830 °C for 30min in 100 mbar reactor pressure using different growth mode, (a) continuous nucleation, (b) FME respectively. RMS roughness of each sample is same as 0.17nm... ..	71
Figure 3-14 AFM images of GaP bulk layers grown at different growth temperature (a) 500 °C, (b)525 °C, (c) 550 °C, (d) 650 °C, (e) 700 °C, (f) 800 °C respectively. LT-GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 10.9nm, (b) 10.8nm, (c) 18.9nm, (d) 4.3nm, (e) 2.94nm, (f) 3.44nm respectively.. ..	72
Figure 3-15 AFM images of GaP bulk layers grown at 700 °C with different V/III ratio (a) 5000 (b) 1000, (c) 500, (d) 100 respectively. LT-	

GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 2.9nm, (b) 2.1nm, (c) 2.0nm, (d) very hazy respectively and last sample (d) is measured by Normalski optical microscopy due to very hazy surface.75

Figure 3-16 AFM images of GaP bulk layers grown at 700 °C with different V/III ratio (a) 500 (b) 250, (c) 100 respectively. Sample (d) is grown at sample temperature with V/III =100 and 2 times growth rate than that of sample (c). LT-GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 3.5nm, (b) 2.7nm, (c) 2.5nm, (d) 2.1nm respectively.....76

Figure 3-17. GaP bulk layers grown at 700°C on GaP nucleation layers grown at 400 °C having 3nm-thickness after annealed at at 830°C for 30min in 100 mbar reactor pressure using different growth mode.....77

Figure 4-1 1 x 1 μm² AFM images of InP layers grown on vicinal Si(001) at (a) 450 and (b) 400 °C for 10 min. 87

Figure 4-2 Plan-view SEM images of two-step InP layer grown on vicinal Si(001). The growth temperatures of second layer were (a) 650, (b) 600 and (c) 550 °C. The insets of (b) and (c) are AFM images of corresponding samples. The RMS roughnesses of (b) and (c) are 68.0 and 32.5 nm, respectively..... 89

Figure 4-3 (a) Plots of RMS roughness and (b) XRC FWHM of InP layers depending on growth conditions. The insets of (a) are 10 x 10 μm² AFM images of InP layers of 2.6 μm grown on nominal and vicinal Si(001) with the RMS roughnesses of 23.4 and 7.7 nm,

respectively.....	90
Figure 4-4 CL images of InP layers on (a), (b) vicinal and (c) nominal Si(001) substrates at 80 k. The thickness of InP layers are (a) 1.3 and (b), (c) 2.6 μm . (d) Plan-view SEM image corresponding to (c)..	92
Figure 4-5 10 x 10 μm^2 AFM images of 1.3 μm -thick InP layer grown on vicinal (a) Si(001) and (b) Ge(001) substrates. RMS roughnesses are (a) 26.4 and (b) 7.8 nm.	94
Figure 4-6 Plan-view TEM images of InP layer grown on vicinal (a), (b) Si(001) and (c) Ge(001) substrates. Thicknesses of InP layers are (a), (c) 1.3 and (b) 2.6 μm . (d) the plot of TDD and planar defect density of InP layer grown on vicinal Si(001) and Ge(001) substrates...	97
Figure 4-7 XRD rocking curves of InP layers grown on vicinal Si(001) and Ge(001) substrates.	98
Figure 4-8 AFM images of InP top layers from (a) to (c) and bright field ($g=(001)$) cross-sectional TEM micrograph are from (d) to (f) with different growth condition and buffer structure. All samples have the same GaP buffer growth conditions and RMS roughness is (a) 9.4nm, (b) 5.5nm, (c) 2.1nm respectively.....	100
Figure 5-1 Cross-sectional TEM images of InP layers grown on patterned Si (001) substrate at various growth temperatures ranging from (a) 500 $^{\circ}\text{C}$ to (d) 650 $^{\circ}\text{C}$ with increment of 50 $^{\circ}\text{C}$..	112
Figure 5-2 Cross-sectional (a) SEM and (b) TEM images of epitaxially grown InP layer on a patterned Si (001) wafer with SiNx mask. HT InP layer is grown at 650 $^{\circ}\text{C}$.	113
Figure 5-3 Cross-sectional (a) SEM and (b)TEM image of HT InP layer grown on a patterned Si (001) wafer with SiNx mask. HT InP	

layer is grown at 550 °C..	116
Figure 5-4 Evolution of growth behavior of InP layer from the (a) SiN _x patterning to (e) the HT InP growth.....	118
Figure 5-5 AFM images recorded from the surface of HT InP layer grown at 550 oC. The lower figure shows the magnified image of the flat top region.....	120
Figure 5- 6. Cross sectional TEM image of InGaAs grown on HT InP template grown at 550 oC. The inset shows the STEM image of the same structure	121
Figure 5-7. Normalized distribution of DLDs with respect to DLD width extracted from sample K with layer thickness of 100 μ m. The crystal energy/unit length of SF with respect to SF width is included for comparison. The arrows indicate on which scale the data is plotted on [21].	125
Figure 5-8. Normalized distribution of DLDs with respect to DLD width extracted from sample K with layer thickness of 100 μ m. The crystal energy/unit length of SF with respect to SF width is included for comparison. The arrows indicate on which scale the data is plotted on [21]	126

Chapter 1

Introduction

Silicon is the basic material of electronics. About 95% of all semiconductor devices are manufactured using silicon substrates. As a carrier, the Si substrate is undoubtedly advantageous due to its small mass, good thermal conductivity, low cost, maximum wafer diameter, and wide prevalence. In addition, Si channel based complementary metal oxide semiconductor (CMOS) microelectronics industry has moved into a new era of nanoelectronics driven by the well-known Moor's scaling law [1,2]. The fast scaling has been slowed down in the past few years as the physical gate lengths of CMOS devices approach about 20 nm [1]. Further shrinking the dimensions does not give any performance benefit but bring up great challenges in device fabrication.

As an alternative to the Si-channel devices, high mobility materials have been widely considered and triggered extensive research interest over the past decade in order to further boost the device performance [3,4]. The high hole mobility of Ge makes it a good candidate for pMOS devices while III-V compound semiconductor materials generally have higher electron mobility [5]. The combination of Ge and III-V materials provides a promising approach to making high performance non-Si channel CMOS devices. However, the mechanical and thermal properties of both Ge and III-V materials make them incompatible with the mainstream Si processing technologies [6]. Furthermore, Ge and III-V materials are much more expensive with limited availability compared to Si. Therefore, the benefit of

Ge and III-V materials has to be accomplished by epitaxial growth on Si, which allows a thin layer instead of bulk substrates for device fabrication by using the Si processing platform. To manufacture non-Si CMOS devices, selective area growth (SAG) of Ge and III-V materials on Si proves to be one of the best solutions. In SAG, epitaxial growth only occurs on the dedicated device areas while the deposition on oxide or nitride surfaces is prevented [7]. Therefore, different materials can be integrated on a single Si substrate by using SAG. However, there are many challenges in SAG of Ge and III-V materials in order to make device quality epitaxial layers on Si substrates.

This dissertation describes our contributions on monolithic integration of InP on Si for the CMOS technologies and optical detection technologies. This introductory chapter begins with a brief background and discussion of the motivation of this work. The limitations of scaling of conventional Si bulk MOSFETs and electrical wires are summarized. Finally, the organization of the dissertation is presented.

1.1. Motivation

The Silicon Metal-Oxide-Semiconductor Field Effect Transistor has been the workhorse of the semiconductor industry for the last three to four decade. Device scaling has improved both packing density and transistor performance, resulting in increase in cost per function, which propelled the success of semiconductor industry. Figure 1-1 depicts the exponential increase in microprocessor performance represented by millions of instructions per second, over technology generations. Even though the physical dimensions have been continually shrinking by a factor of 2-3 in accordance with Moore's Law [8], the fundamental architecture and materials of the device has remained the same. However, as we further shrink the device dimension, transistor with conventional structure and material is reaching its fundamental scaling limit.

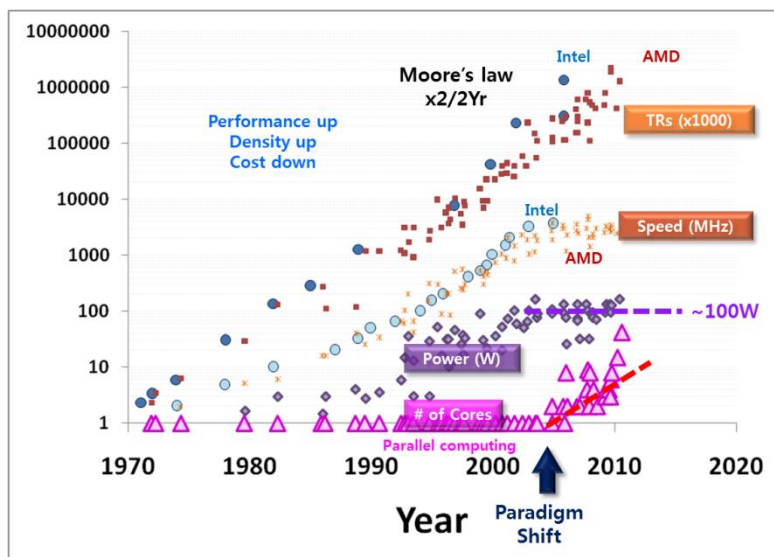


Figure 1-1 Microprocessor performance increase due to scaling

[Source : Intel & AMD]

Without change in transistor geometry and introduction of novel materials, exponential decrease in device dimensions cannot continue further, as beyond the 22nm node fundamental as well as practical constraints will limit the maximum performance achievable by these scaled transistors.

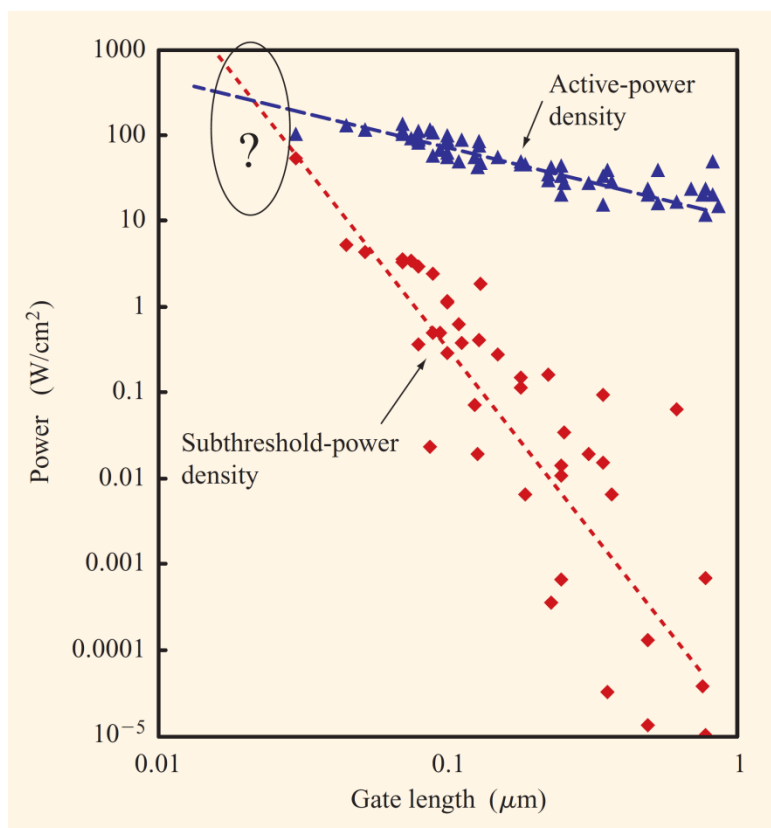


Figure 1-2 Active and standby power density trends plotted from industry data. The extrapolations indicate a cross over below 20nm gate length [10]

Increased performance has come at a cost of increased off state power in transistors. Figure 1-2 depicts the evolution of power density as the devices are scaled traditionally. The static power has increased more rapidly compared with the linear increase in the active power dissipation. Around the

gate length of 20 nm, static power would approach the active power, and even surpass it, as we continue the scaling. Hence, beyond gate length of 20nm, it is questionable if the traditional scaling techniques would be effective. The major reason for this rapid increase in static power is the subthreshold leakage. With decreasing channel length, gate bias cannot form effective potential barrier between the source and the drain when the transistor is turned off, which blocks the current flow. This results in the increased static leakage current, and increases the static power dissipation. Management and suppression of static power is one of the major challenges to continued gate length reduction for higher performance.

Once the scaling of conventional bulk MOSFETs starts slowing down, the insertion of performance boosters, like novel materials and non-classical device structures, will be necessary to continue to improve performance.

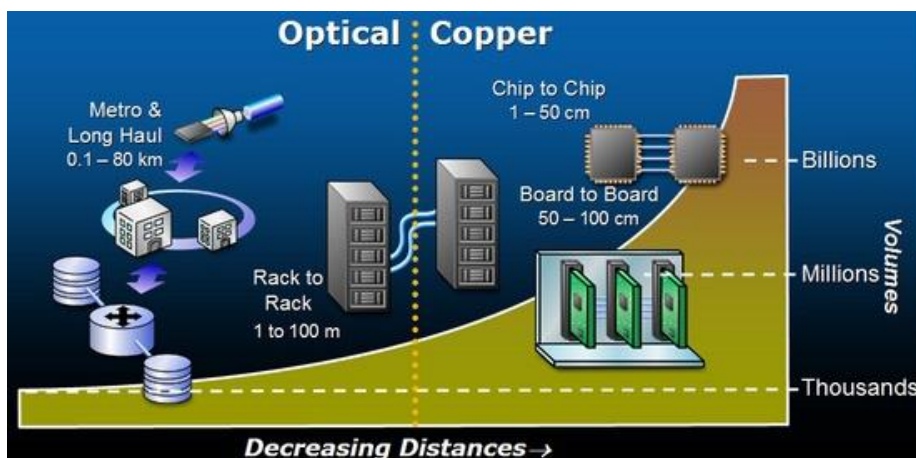


Figure 1-3 The chain of communication systems versus the length of the interconnection and the business volume of the corresponding technology.

(Source: Intel)

On the other hand, while individual logic elements have become significantly smaller and faster, computational speed is limited by the communication between different parts of digital systems. This bottle neck is identified as one of the grand challenges in the progress of integrated electronics.

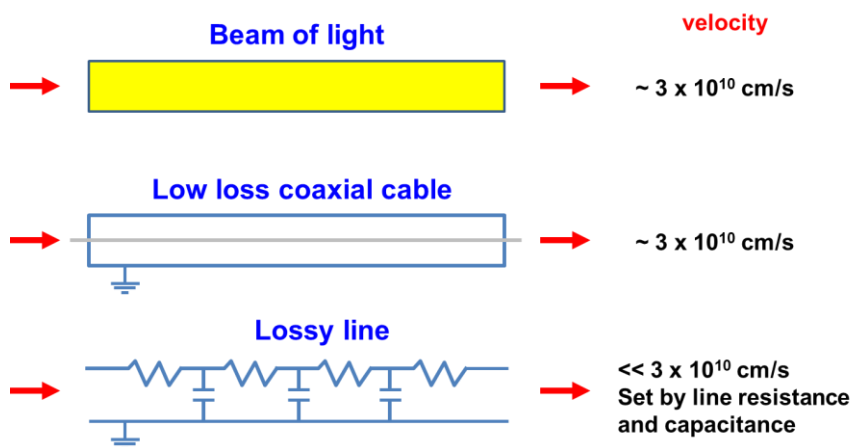


Figure 1-4. Illustration of types of optical and electrical propagation and their velocities [11]

Since the introduction of low-loss silica fibers for optical communications, optics has been dominating the long haul communications and it has consistently made its way down to short distance (Figure 1-3). There are several benefits for replacing conventional electrical cables with optics. Signals in both optical and electrical links are carried by electromagnetic waves. Information in typical electrical wires such as coaxial cables propagates almost at the velocity of light similar to that in optical links as illustrated in Figure 1-4. However, with increased modulation frequencies, the traditional electrical wires are becoming increasingly resistive and the signals moves at a slower rate due to dissipative wave propagation.

An excellent review of the potential benefits offered by optical interconnections is presented in [11] based on the fundamental physical differences of the higher frequency, shorter wavelength and larger photon energy of optics compared to electrical interconnections. Optics has negligible propagation loss from large bandwidth signals because the carrier frequency of light is very high compared to any practical modulation frequency. On the other hand, electrical interconnects suffer from significant signal distortion and frequency dependent cross-talk at high modulation frequencies. Owing to the short optical pulses, optics provide increased time precision over electrical interconnects, and this leads to the ability to transmit multi-channels down a single optical link thanks to wavelength division multiplexing. Furthermore, for optics, it is relatively easy to guide optical wave. The transmitted signal can be confined into the material boundaries of the guiding medium owing to the small waveguide of the optical signals. Additionally, due to the quantum nature of the physical processes, optics does not suffer from the impedance mismatching problem, which is quite challenging for electronics. While electronic devices have high impedance and low capacitance, the communication between such devices rely on low impedance and high capacitance transmission lines. In electronics, line drivers are used to match the impedance, which increase power dissipation and chip area at high operation frequencies. On the other hand, for the optics, the classical field or voltage is irrelevant.

1.2. Si and III-V material properties

The high carrier mobility of Ge and III-V materials make them attractive in fabricating future CMOS devices. Meanwhile, there are many drawbacks associated with these materials. The most striking one is that these materials

do not have a stable and high-quality native oxide that can act as a natural surface passivation layer. This is the reason Si has become the dominant material in CMOS industry despite the first transistor being made on Ge substrates at Bell Labs in 1947 [12]. The lack of high-quality native oxides requires additional efforts in developing other surface passivation dielectrics [13-16]. One of successful passivation layers for Ge pMOS is a few monolayer (ML) thick Si cap layer which mimics the Si substrate and gives high-quality SiO₂ passivation layer [15]. In contrast, III-V passivation is much more complicated and less successful even though a great deal of efforts have been dedicated to this field [14,17].

Table 1-1. Physical properties of common group IV and III-V semiconductors [5].

		Si	Ge	GaP	InP	GaAs	InAs	GaSb	InSb
Electron mobility (cm ² /Vs) 300K		1450	3800	160	5400	9000	330000	7620	77000
Electron effective mass(/m ₀) 4K	m _h	0.19	0.0823	0.21	0.808	0.0662	0.23	0.039	0.01359
	m _L	0.916	1.59	7.25					
Hole mobility (cm ² /Vs) 300K		370	1800	135	190	400	450	680	850
Hole effective mass (/m ₀) 4K	m _{hh}	0.537	0.0438	0.67	0.455	0.34	0.57	0.3	0.032
	m _h	0.153	0.284	0.17	0.121	0.094	0.35	0.042	0.016
Band gap (eV) (300K)		1.1242	0.664	2.272	1.344	1.424	0.354	0.75	0.18
Band gap (eV) (0K)		1.17	0.785	2.35	1.4236	1.519	0.418	0.822	0.2352
Lattice constant nm (300K)		0.5431	0.5658	0.5451	0.5869	0.5654	0.6058	0.6096	0.6479
Melting point (K)		1687	1210	1749	1327	1511	1221	991	800
Debye T (K)		636	374	445	321	344	247	266	203
Thermal conductivity (W/cmK) 300K		1.56	0.4	0.77	0.7	0.455	0.3	0.4	0.4
Thermal expansion coefficient (ppm) 300K		2.92	5.9	4.65	4.75	6	4.52	7.75	5.37
Density (g/cm ³) 300K		2.329	5.3234	4.138	4.81	5.3161	5.66	7.75	5.7747

The second challenge of using Ge and III-V materials for CMOS device fabrication is the process and cost issue. Due to the mechanical properties and thermal expansion issues (see Table 1-1), large scale wafer substrates are not commercially available. The largest Ge substrates available is 200 mm and the mainstream III-V wafer size is 100 mm while 300 mm Si wafers are routinely used in the state-of-the-art Si fabs. Small wafer substrates do not allow cost-effective high volume production. Thirdly, these wafers are not

compatible with the Si processing equipments. The higher densities and poor mechanical properties of Ge and III-V materials make them much more fragile than Si. Fourthly, Ge and III-V materials are less abundant than Si, resulting in prohibitive wafer costs.

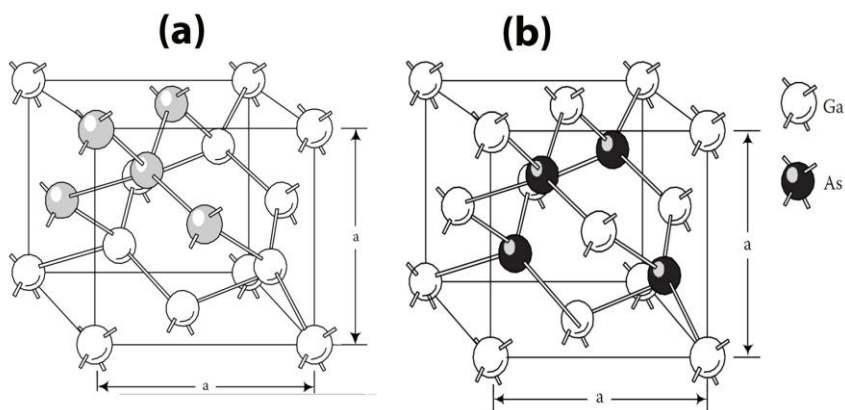


Figure 1-5. The fcc crystal structures of different semiconductors: (a) The diamond crystal structure. All atoms are of the same type (e.g., Si). (b) The zinc blende crystal structure. The white and black atoms belong to the two different sublattices (e.g., Ga and As) [20].

From the above-mentioned issues, it is technologically and economically challenging to use Ge and III-V bulk substrates for device fabrication. Fortunately, all these challenges except the surface passivation can be addressed by heteroepitaxial growth on Si substrates. Si has the diamond crystal structure as Si (Figure 1-5a). III-arsenides and III-phosphides have zincblende crystal structure which has the same atomic stacking as diamond except that the cations and anions are stacked alternately (Figure 1-5b). The same crystal structure makes it possible to grow Ge or III-V compounds on Si substrates epitaxially. Generally, thin (typically $<1\mu\text{m}$) layers are grown on Si substrates and the devices can be made on the epitaxial layers. These thin

layers overcome the high substrate cost and the processing equipment incompatibility. Furthermore, when SAG is performed, both Ge and III-V materials can be grown on one Si substrate in a way that both pMOS and nMOS can be made adjacent to each other to give CMOS function. SAG allows us to use Si wafers with standard shallow trench isolation (STI) that gives good lateral electrical isolation. An integration scheme is shown in Figure 1-6 [3, 18]. The nMOS III-V channel is grown on top of a strain-relaxed buffer layer that has the same lattice constant as the bulk material. The pMOS device is made on a strain-relaxed Ge buffer layer. To ultimately boost the device performance, source and drain engineering can be employed [18]. There are other options in the details of device structure design such as high electron mobility transistors (HEMT) [19]. Therefore, device quality strain-relaxed Ge and III-V buffer layers provide a platform for the subsequent device engineering.

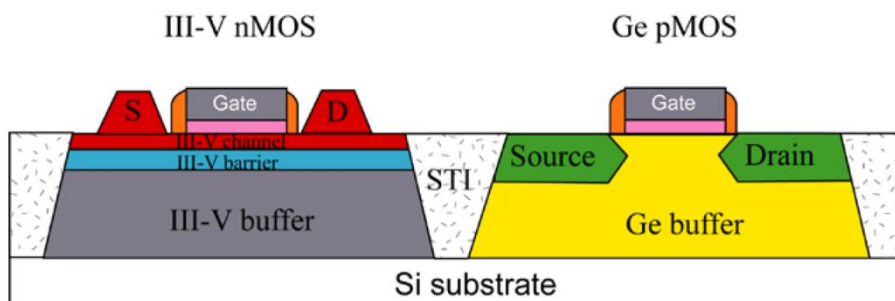


Figure 1-6. Example of heterointegration of Ge and III-V MOS transistors on a Si substrate. Different device structures can be made on the strain-relaxed III-V and Ge buffer layers. On the left, a quantum-well device architecture is shown and the III-V barrier layer is inserted to block the source-to-drain leakage current. On the right shown is Ge channel strain engineering by embedded source and drain [37].

1.3. Thesis organization

This thesis is organized as following. Chapter 2 deals with the growth and characterization and chapter 3 is GaP and InP blanket growth on Si (001) substrates, chapter 4 and 5 are about InP SAG epitaxial growth. The conclusions and future work are summarized in chapter 6.

Chapter 2 starts with a short introduction to the growth and characterization of InP on Si substrates, including the MOCVD system and principle. Then the characterizations of III-V on Si substrates are briefly discussed followed.

Chapter 3 discusses GaP blanket growth on Si (001) substrates that have been developed within the frame of this PhD work by optimization of several growth parameters. One approach for growing GaP on Si (001) substrates is to use the high V/III ratio and the low growth.

In chapter 4, InP layers were grown on Si(001) and Ge(001) substrates by using metalorganic chemical vapor deposition (MOCVD). Two-step InP growth on Si(001) was optimized by controlling growth conditions such as growth temperature, V/III ratio and thickness. Finally, high quality InP top layers using a thin GaP buffer layer and inserted $\text{In}_{0.6}\text{Ga}_{0.4}\text{As}$ strained layers on Si (001) substrates.

In chapter 5, we investigated SAG of InP layers on patterned Si substrates with InP/GaP buffer layers at various growth temperatures ranging from 500 °C to 650 °C. In order to grow high quality InP, a thin GaP buffer layer was grown on stepped sidewall surfaces of etched Si. The different growth temperature resulted in different top surfaces. The high quality InP layer with smooth surface can be attributed to the dislocation necking effect together with the formation of void. Finally we demonstrated the formation of InGaAs/InP heterostructures using the suggested InP templates, which can be

used in applications of electronic devices.

In the end, the summary of this PhD work and future work are given in chapter 6. High-quality InP virtual substrates are obtained in SiN_x trenches, which enables the integration III-V MOSFET devices and optoelectronic devices on standard Si (001) substrates. The remaining interest in further exploring this subject is given as the future work.

1.4. References

- [1] <http://www.itrs.net>.
- [2] <http://www.intel.com/technology/mooreslaw/>.
- [3] M. Heyns, M. Meuris, and M. Caymax, *ECS Trans.* **3 (7)**, 511 (2006).
- [4] E. Fitzgerald, M. Bulsara, Y. Bai, C. Cheng, W. K. Liu, D. Lubyshev, J. M. Fastenau, Y. Wu, M. Urtega, W. Ha, J. Bergman, B. Brar, C. Drazek, N. Daval, F. Leterte, W. E. Hoke, J. R. LaRoche, K. J. Herrick, and T. E. Kazior, *ECS Trans.* **16 (10)**, 1015 (2008).
- [5] O. Madelung, *Semiconductors: Data Handbook* (Springer, 2004).
- [6] M. Heyns, C. Adelman, G. Brammertz, D. Brunco, M. Caymax, B. De Jaeger, A. Delabie, G. Eneman, M. Houssa, D. Lin, K. Martens, C. Merckling, M. Meuris, J. Mittard, J. Penaud, G. Pourtois, M. Scarrozza, E. Simoen, S. Sioncke, and W. E. Wang, *10th Int. Conf. Ult. Integ. of Si*, 83 (2009).
- [7] D. J. Dumin, *J. Cryst. Growth*, **8**, 33 (1971).
- [8] Z. M. Sze and N. K. K., *Physics of Semiconductor Devices*, 3rd ed. (John Wiley & Sons, Inc., New Jersey, 2007).
- [9] G. E. Moore, "No exponential is forever: but "forever" can be delayed! [semiconductor industry]", in *Digest of Technical Papers – IEEE International Solid-State Circuits Conference*, pp. 20-23 (2003).
- [10] E. J. Nowak, "Maintaining the benefits of CMOS scaling when scaling bogs down", in *IBM Journal of Research and Development*, **46(2/3)**, pp. 169-180 (2002).
- [11] D. A. B. Miller, "Physical reasons for optical interconnection," *Int. J. Optoelectron.* **11**, 155-168 (1997).
- [12] C.-T. Sah, *Fundamentals of Solide State Electronics* (World Scientific Publishing Co. Pte. Ltd., Singapore, 1991).
- [13] M. Kobayashi, T. Irisawa, B. M. Kope, Y. Sun, K. Saraswat, H. S. P.

- Wong, P. Pianetta, and Y. Nishi, *Symp. VLSI Techn.*, 76 (2009).
- [14] J. Kwo and M. Hong, *J. Cryst. Growth* **311**, 1944 (2009).
- [15] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryman, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, *IEDM*, **873** (2008).
- [16] J. Mitard, C. Shea, B. De Jaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W. E. Wang, J. C. Lin, F. E. Leys, R. Loo, G. Windericks, E. Vrancken, A. Stesmans, K. De Meyer, M. Caymax, M. Pantisano, M. Meuris, and M. Heyns, in 2009 Symp. on *VLSI Tech.*, Kyoto, Japan, 2009.
- [17] M. W. Hong, J. R. Kwo, P. C. Tsai, Y. C. Chang, M. L. Huang, C. P. Chen, and T. D. Lin, *J. J. Appl. Phys.* **46**, 3167 (2007).
- [18] R. Loo, G. Wang, L. Souriau, J. C. Lin, S. Takeuchi, G. Brammertz, and M. Caymax, *J. Electrochem. Soc.* **157**, H13 (2010).
- [19] A. Kasamatsu, K. Kasai, K. Hikosaka, T. Matsui, and T. Mimura, *Appl. Surf. Sci.* **224**, 382 (2004).
- [20] J. E. Ayers: Heteroepitaxy of semiconductors : theory, growth, and characterization, CRC Press Taylor & Francis Group, (2007)

Chapter 2

Growth and characterization of InP on Si

2.1. Challenges of InP growth on Si

Though InP has its advantages over Si, it has some drawbacks, for example, high cost and mechanical weakness compared with Si. Furthermore, today's industry is much concentrated in Si technology. So, to exploit advantages of InP on Si-based platform, monolithic integration of InP on Si is needed, and InP growth technology on Si would be a starting point to the monolithic integration. However, the lattice mismatch between InP and Si causes much problem in growing InP on Si.

2.1.1. Lattice mismatch

If a material, for example, Si is to be grown on the same material (homoepitaxy), since lattice constants of the starting material and the epi material are same, high quality layers can be achieved, without incurring significant defects like threading dislocations. In Fig. 2-1, shown against the background of the lattice constant dependences of the band gaps of the group IV semiconductor materials (Si and Ge) and III-V compounds are the crystallographic transition pathways from silicon to InP, on the latter of which GaAs or Ge type heterosystems can be grown by known techniques, and then various devices can be created on their bases. Even if the two materials are different (hetero-epitaxy), if they have the same lattice constant, equally high quality epi-layers can be achieved. Growth of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on InP and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ on InP are examples for hetero-epitaxial growth with same lattice constants.

Difficulties rise if the lattice constants for the substrate and the epi material are different. If the mismatch is only a few percent and the layer is thin, the epitaxial layer grows with a lattice constant in compliance along the surface plan as its lattice constant adapts to the seed crystal. Such a layer is called pseudomorphic because it is not lattice-matched to the substrate without incurring strain. However, if the epitaxial layer exceeds a critical thickness (t_c), which depends on the lattice mismatch, the strain energy leads to formation of defects called misfit dislocation. In our research, we want to grow high quality indium phosphide layers on silicon. However, indium phosphide's lattice constant is 5.868 Å whereas silicon's is 5.4307 Å [1]. Thus the percent difference is 8.052%.

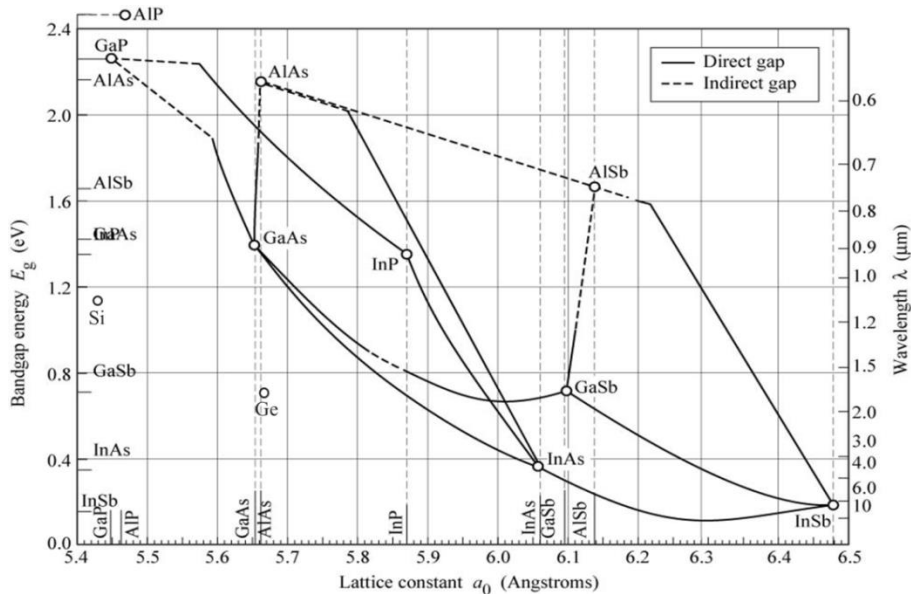


Figure 2-1 Band gap energy and lattice constant of various III-V and IV semiconductors at room temperature [3].

If the mismatch is considerable and relatively thick epi-layer is needed, additional epitaxial growth techniques are needed. As one starts to grow InP on Si, the new InP layer will conform to the lattice spacing of the Si substrate. The InP layer is now compressively strained as the lattice is reduced. So below a certain thickness, one can grow defect-free compressively strained InP on Si. This thickness has been shown to be around several nm. As one continues to grow thicker layers, it is energetically favorable to relieve the strain by forming dislocations at the InP/Si interface. In addition, the islanding can occur as an additional means of reducing the elastic strain energy of the film [2]. This leads to rough surfaces unsuitable for device applications.

2.1.2. Thermal mismatch

Growth of InP on Si or III-V in general, takes place at high temperature typically around 600°C which demands a wide temperature range of cooling to room temperature. As a consequence the lattice constants of InP and Si are subjected to change differently due to the difference in the thermal expansion of the two materials. The thermal expansion coefficient difference induces significant strain in the layer, bending of the substrate and incase of tensile stress cracks in the epitaxial layer. The thermal strain induced by the thermal expansion coefficient difference is given by [4],

$$\varepsilon = \int_{T_0}^{T_g} (\alpha_s - \alpha_l) dT \quad (2.1)$$

where T_0 is the reference temperature which is normally room temperature (300K), T_g is growth temperature and α_s and α_l are thermal expansion coefficients of substrate and layer, respectively. The thermal expansion coefficients of InP, GaAs, Si and SiO₂ in units of K⁻¹ are 4.56×10^{-6} , 6.80×10^{-6} , 2.60×10^{-6} and 0.54×10^{-6} . Thus, using GaAs as a buffer layer for InP on Si growth could reduce the lattice strain in InP due to the thermally induced compressive strain at the InP/GaAs interface [5]. In addition, InP and GaAs have a 4% lattice mismatch and that is what the InP epi-layer experiences. Therefore, In SAG of InP on Si where selective area starts from an InP seed layer grown on Si using a GaAs buffer layer, the thermal strain in the SAG layer is mainly a tensile strain due to the difference in thermal expansion coefficient difference between the dielectric mask (SiO₂) and the SAG InP [6].

2.1.3. Defects Associated to Polar on Non-Polar Epitaxy

An unavoidable issue of III-V/Si heteroepitaxy is the integration of polar and non-polar heterointerface. However, a complete understanding of polar on nonpolar epitaxy is a critical challenge for successful III-V semiconductor compound integration. Silicon, being made up of a single atomic species, forming purely covalent chemical bonds with zero net dipole moments, is a non-polar crystalline material. On the other hand, III-V like InAs, made up of both In and As atoms whose ionic bonds possess a significant net dipole moment, is a so-called polar crystalline material; the interface between two such materials presents a number of challenges that must be taken into account. It was proposed that if the first III-V atomic plane adjacent to the silicon bulk substrate were a perfect atomic plane, a large electrical charge would be induced [7]. To neutralize the interface charge, rearrangement of

atoms may result, creating an environment of III-V island formations. Growing at low temperature with a layer by-layer growth mode, referred to as migration enhanced epitaxy (MEE), was used to address this issue. This growth technique proved indispensable for previous successful GaAs/Ge work [8]. The polar/non-polar charge neutrality dilemma is nearly impossible to monitor except by observation of possible post-epitaxy effects, such as the formation of interfacial planar defects such as: antiphase domain boundaries (APBs), stacking faults (SFs) and microtwin (MT) defects. The goal of this work, therefore, is the suppression of these heterointerface-driven defects through the proper surface preparation of the Si substrates and optimization of the growth and nucleation conditions of the III-V heteroepitaxial layers.

2.1.3.1. Autodoping by interdiffusion

Additional difficulties may arise when atomic species are interchanged at III-V/Si interfaces. Interdiffusion of atoms across a hetero-interface is possible, when enough atoms are thermally excited to a mobilize limit within the crystals for atomic exchange mechanism [9]. However, if the III-V/Si interface consists of III-Si or V-Si bonds, then electrical neutrality is lost and the interface becomes polarized. Therefore, inter-diffusion between III-V/Si can lead to an effect known as autodoping, due to the fact that group-III and group-V materials are common p-type and n-type dopants of silicon, respectively. On the other hand, silicon species are amphoteric in the zinc blende crystal structure through their preference for the group-III sites. They can act as an n-type dopant for the III-V material. Inter-diffusion by itself presents the additional complication of unwanted autodoping across the interface. Autodoping tends to produce undesired doping proles, which can

hinder devices performance. So keeping the diffusion at the interface to minimum is a priority. In practice, interface polarity is likely compensated during growth by the presence of charged point defects and dislocation cores as well as some atomic exchange across the interface [12]. Previous work in the GaAs/Ge or GaP/Si systems indicated that a multi-stage growth approach involving initial low-temperature MEE GaAs growth mode, prior to a conventional high-temperature heteroepitaxial MBE growth mode, sufficiently suppressed autodoping between the two materials [8]. A similar approach was examined for the GaP/Si system and will be discussed in the experimental part of the growth in this thesis work.

2.1.3.2. Antiphase domain boundary

A number of planar crystal defects are encountered in III-V semiconductor heteroepitaxy on silicon, as it was discussed before. The far greater concern during III-V/Si heteroepitaxy is the possibility of antiphase disorder formation. Antiphase (domain) boundaries (APBs) are one type of the planar defects that will be introduced through the growth of compound semiconductor materials on an elemental crystal, such as the case of InAs/Si, can result in the formation of crystalline subdomains referred to as anti-phase domains and anti-phase domain boundaries (APBs) also known as, inversion domains boundaries (IDBs) [10].

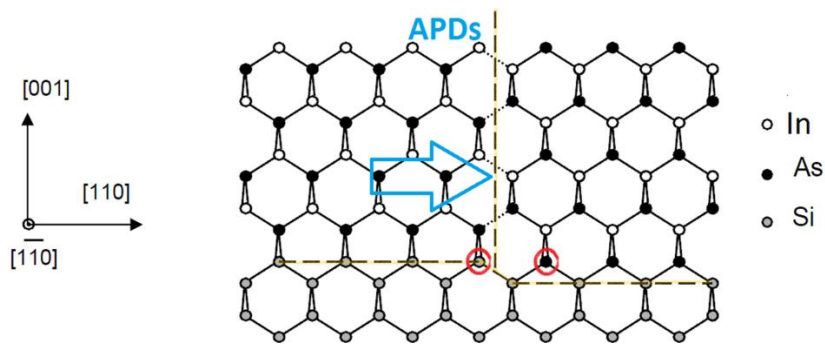


Figure 2-2 Schematic diagram of anti-phase domains boundaries in InAs formed by a single-atom step on the silicon substrate surface. Figure modified according to reference [11].

There are a few theoretical reasons for their formation. During growth initiation of a compound material, two crystal domains can form independently of one another, each the result of different nucleation species like In vs. As; the planes at which the domains of reversed polarity meet, referred to as APBs, possess In-In and/or As-As bonds instead of proper In-As bonds, as in the case of GaP/Si system [12].

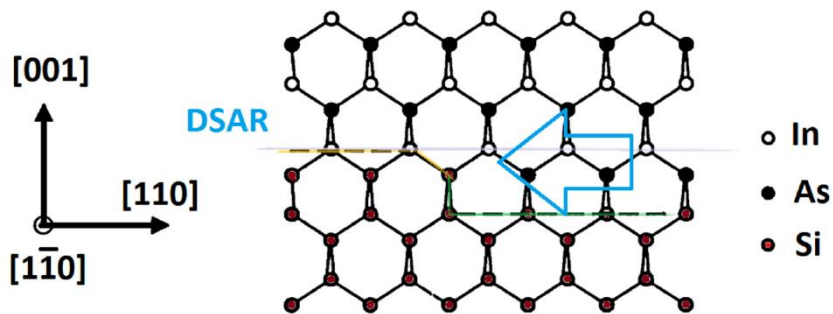


Figure 2-3 Schematic diagram of anti-phase domains boundaries in InAs formed by a single-atom step on the silicon substrate surface. Figure modified according to reference [11]

In another case, APDs can be formed if the elemental crystal (i.e. silicon) has single atomic steps on its surface as shown in Fig. 2.2. A surface variation such as an atomic-level step on the Si substrate can cause the III-V layer above this step to rotate its orientation, and thus lead to the formation of a propagating boundary layer between two distinct III-V domains [13].

Due to the lower symmetry of the polar semiconductor, it can grow with one of two (nonequivalent) crystal orientations on the nonpolar substrate. The boundaries between regions having these two orientations will also result in the formation of inverted domain boundaries. The nature of the chemical bonding across the APBs causes them to be electrically active, which directly relates to the degradation in material quality. Experiments involving time resolved photoluminescence of GaAs/Ge system demonstrated a large decrease in minority carrier lifetime with a large increase in interface recombination rates in the samples containing the APD defects versus those without [10]. Generally, APDs are expected to introduce states within the energy gap and give rise to non-radiative recombination. They therefore degrade the efficiencies of LEDs and cause excess leakage in p-n junctions. Avoiding the APDs defect is tricky and demands control of the substrate surface structure prior to III-V growth, but it has been accomplished in systems like GaAs/Ge [8, 14]. Early research into direct III-V/Si MBE integration focused on high indexed Si substrates with a surface atomic structure providing bonding sites for alternating group-III and V-atoms,

creating an electrically neutral interface to help preventing the formation of APDs [15]. However, many other authors have investigated surface preparations recipes, and reported many nucleation conditions which can minimize or eliminate the formation of APDs for many III-V/IV systems like GaAs/Si, GaP/Si and GaAs/Ge [10,12,16]. Another method has been provided efficient APDs suppression [17], utilizes silicon substrates whose surfaces are polished such that the surface atomic plane is intentionally misoriented a few degrees toward an orthogonal [110] direction away from the (001) surface in order to induce a double atomic step reconstruction (DASR) as schematically shown in Fig. 2.2. In contrast to the irregular single steps of nominally on-axis (001) Si surface, deliberately mis-orienting the substrate toward [110] direction introduces a regular array of single steps running the [110] direction. These regular arrays of single steps line up in a manner of proper atomic positions, with planar atomic growth occurring in the (001) direction, as illustrated in Fig.2.2. However, as the off-cut angle is increased, the density of steps increases and the average terrace width w decreases according to Eq. 2.2. Where h is the height of the step.

$$w = h \tan^{-1}(\phi) \tag{2.2}$$

At high temperatures and under ultra-high vacuum conditions, off-cut (001) surfaces are known to transform from their initial single-stepped two-domains configuration to a lower energy single-domain configuration of double steps reconstruction [18-19]. Double steps surfaces preserve sublattice orientation between neighboring terraces, thereby facilitating APDs-free III-V epitaxial growth on silicon substrates. In the event that single-stepped two-domains surface is not achieved, substrate o-cut may also serve to limit the extent of APDs in zinc-blende crystal structures by self-annihilation as a

result of APD-APD interaction.

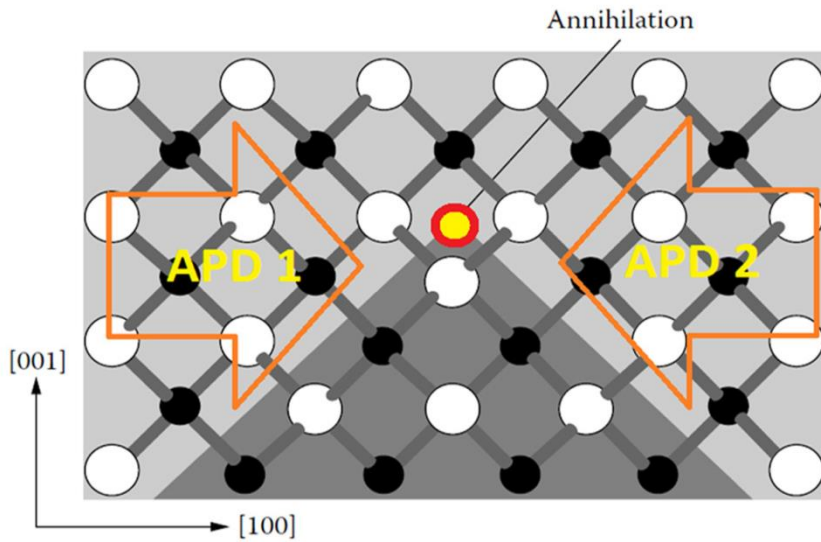


Figure 2-4 Self-annihilation anti-phase domains on [011] plane in a (001) zinc blende semiconductor by the close proximity of bonding of two APD faces. Figure modified according to reference [9].

Here, APDs annihilation occurs at the line of intersection of the two APD planes, which lies along a [110] direction parallel to the interface [20]. Annihilation reactions can also occur between APDs on [011] planes [9], which can meet along a [010] direction, as shown in Fig. 2-4. The high single density afforded by substrate misorientation decreases the spacing between neighboring APDs, hence increasing the probability that neighboring APDs will find one another and form small close domains. Many reports of single

domain GaAs/Si and GaAs/Ge in the literature actually refer to initial two domain III-V growth, followed by rapid annihilation of APDs near the interface, leaving a single dominant domain [21-23]. In the limit of vicinal (001) substrates, however, the spacing between adjacent APDs is thought to be quite large such that self-annihilation near the interface of single-domain becomes less likely [17].

2.1.3.3. Stacking Faults

Stacking faults (SFs) are produced when the regular arrangements of layer atoms are disturbed. A perfect crystal can be considered a stack of atomic layers occurring in a particular sequence. The stacking of the zinc blende structure of III-V semiconductor in the [111] direction can be described as ABCABC. A stacking fault can occur with an extra plane of atoms inserted into the stacking sequence, as in ABCBABC, a B layer is inserted. This is called an extrinsic stacking fault.

Another possible type of stacking fault involves the removal of one plane, as in ABCBC, an A layer is removed and is called an intrinsic stacking fault [10]. Stacking faults are planar defects that are bounded on either side by partial dislocations. Fig. 2-5 shows a high resolution transmission electron microscopy image of SFs defects and SF loops found in InAs QDs embedded in Si matrix system, grown in our MOCVD system. It was also reported for GaP/Si system that initial planar nucleation of GaP/Si is difficult to control, often creating many small faceted GaP islands. Coalescence of these GaP islands often results in the formation of SFs, which then propagate throughout the entire GaP layer [24]. Later reports indicated that SFs could

be suppressed by forcing a 2D growth mode for the first few layers of GaP using migration enhanced epitaxy (MEE) for the nucleation process on Si substrate. Thus, it is essential to carefully monitor polar/non-polar of III-V/Si interface and ensure a low density of SFs.

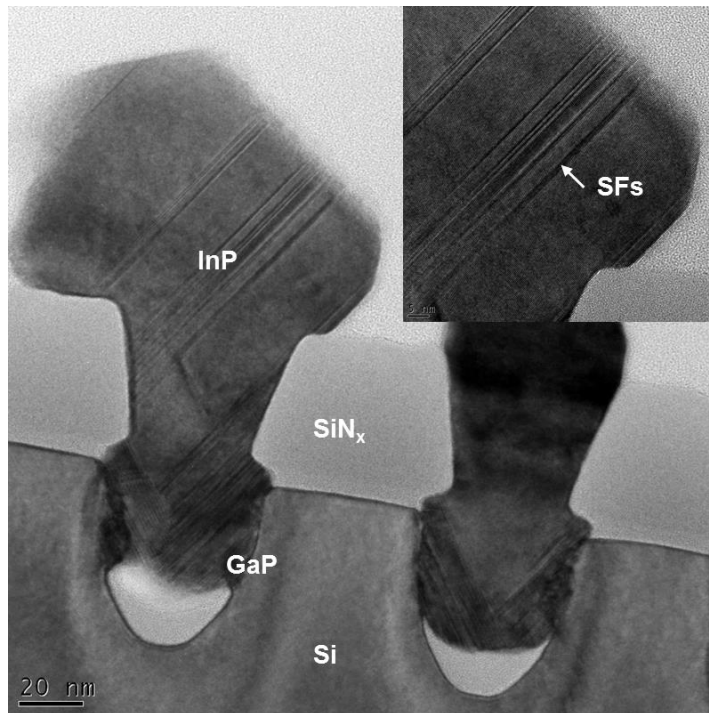


Figure 2-5 HR-TEM image of stacking faults defects found in InP/GaP/Si system.

2.1.3.4. Micro twins

Another type of planar defect resulting from a change in the stacking sequence is the micro twins (MTs). In diamond and zinc blende crystals,

twinning occurs almost exclusively on [111] planes. Using the stacking notation used in the last section (Sec. 2.1.3.3), a twin boundary in a diamond or zinc blende crystal may be denoted as ABCABACBA. There is a change in crystal orientation at the twinning plane. Here the normal crystal and its twin share a single plane of atoms (the twinning plane or composition plane) and there is reflection symmetry about the twinning plane as shown in Fig.2-6. In other words, the MTs defect occurs when the stacking faults sequence is disturbed in such a way as to create a mirror image of itself, as in ABCABCCBAACBA [10]. Twinning involves a change in long-range order of the crystal; it therefore cannot result from the simple insertion or removal of an atomic plane, as in the case of the stacking fault. Therefore, twins cannot be created by the glide of dislocations. Instead, twinning occurs during crystal growth, either bulk growth or heteroepitaxy.

Finding ways to reduce the density of dislocations at a given mismatch strain level is an important goal for successful strained-layer heteroepitaxy. As mentioned before, dislocations and defects can act as non-radiative recombination centers in optoelectronic devices, because the localized mid-bandgap energy levels in the dislocations cores will act as highly efficient trap states for injected minority carriers [26].

A great volume of research activities has already been dedicated to the various barriers to III-V integration on silicon. Nevertheless, it has yet to be shown the quality of III-V on Si material can offer reliability and performance demanded optoelectronic and other device applications. In this research work, a new approach for III-V on silicon heteroepitaxy based on self-assembled and localized growth of nanostructures like quantum dots and dashes will be investigated. The idea is to minimize the above mentioned problems of the formation of dislocations during the growth of relaxation

layers. However, the materials integration processes were conducted by the means of the epitaxial growth of III-V quantum dots and dashes on silicon substrates via MOCVD technique, using the most challenging materials integration approach, by limiting the III-V material to the active region.

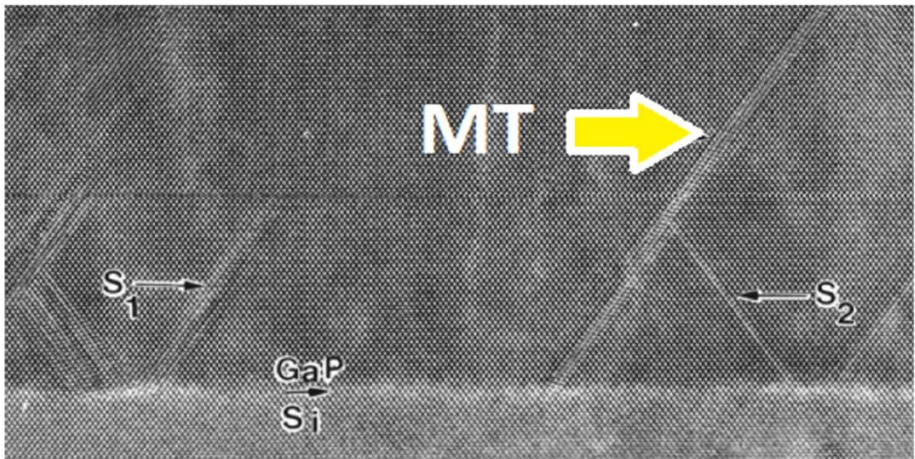


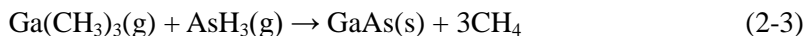
Figure 2-6 HRTEM image of micro twin and stacking faults defects (S1,S2) in GaP/Si system. Figure modified according to reference [24].

2.2. Metalorganic Chemical Vapor Deposition (MOCVD) system

2.2.1. Overview

Epitaxial growth is defined as a precise oriented growth of a single crystal material upon the surface of a single crystal substrate. Growth of a layer with the same kind of atoms as are in the substrate is called homoepitaxy, and growth with a different kind of atoms is called heteroepitaxy. The growth of epitaxial films can be done by a number of methods including liquid phase epitaxy (LPE), molecular beam epitaxy (MBE), vapor-phase epitaxy (VPE), hydride vapor-phase epitaxy (HVPE), and metal-organic vapor-phase epitaxy (MOVPE) or metal-organic chemical vapor deposition (MOCVD). Such methods for the epitaxial growth are important and are used to produce high quality single crystal layers with low defect density and complex heterostructures for electrical and optical applications. In particular, MOVPE is one of the leading techniques for the production of III-V materials for electric and photonic devices. In this technique, III and V metal-organic (MO) and hydride molecules are used for growing III-V compound semiconductors. These source molecules are provided to growth substrate with purified hydrogen or nitrogen gas and diffuse near the surface of the growth substrate. These molecules are thermally decomposed and then chemically react near the surface of growing substrate. Atoms are incorporated at certain positions on the surface in relationship to the underlying crystal structure. For instance,

trimethylgallium (TMGa), $\text{Ga}(\text{CH}_3)_3$, and arsine, AsH_3 , are introduced above a heated GaAs substrate, an epitaxial film of GaAs can grow according to the following reaction,



where (g) and (s) represent “gas” and “solid” phase, respectively.

The major attraction of MOCVD relative to the other techniques is that the MOCVD is suitable for mass production. Moreover, this single growth technique can be used to produce virtually all of the III–V materials and structures required for the cutting edge of electronic and photonic devices including AlGaInP for red or yellow light–emitting diodes (LEDs), III–V nitrides for blue LEDs, and III–V highest efficiency tandem solar cells.

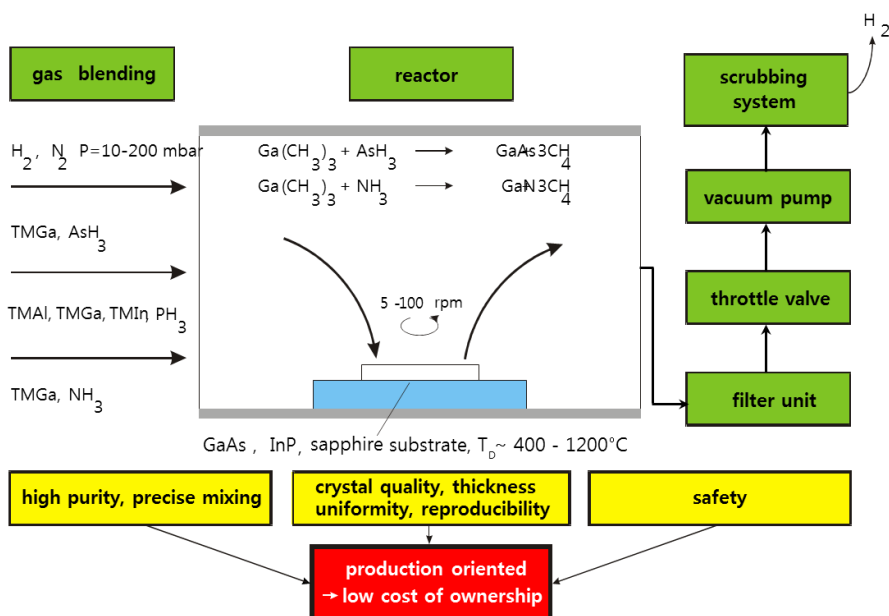


Figure 2-7 Schematic illustration of the MOCVD system [from Aixtron].

2.2.2. MOCVD system

This section explains the MOCVD system used in this work. Figure 2-7 shows the schematic illustration of the MOCVD system. The essential components are the gas delivery system, the reactor and temperature controller, and the low pressure pumping system. All growth in this work was carried out with a horizontal low-pressure MOCVD system.

First, we describe about gas delivery system. Palladium diffused purified hydrogen (H_2) is used as a carrier gas. The carrier gas transport the source gases flowing over the heated susceptor and substrate to the exhaust as shown in Figure 2-7. The vapor-phase source molecules are fed to the reactor in separate lines for metal-organic (MO) source and gas source. The MO sources are provided from bubblers and gas sources are provided from gas cylinders.



Figure 2-8 (a) Layout of the AIX 2400 G3 susceptor in the 8×3 inch. (b) Photo of the reactor chamber of the AIX 2400 G3 in the 8×3 inch configuration.

Fig. 2-8 shows a schematic of the susceptor of the AIX 2400 G3 in the 8×2 inch (a) and a corresponding photo of the reactor chamber (b). The gases enter the reactor chamber through the central inlet in the reactor lid (not visible in the photo) and stream radially outward across the deposition zone. The susceptor is heated by RF induction heating from below and rotates at rotation frequencies of typically 10 rpm. In addition the wafer discs are rotating utilizing AIXTRON's patented Gas Foil Rotation technique. This double rotation insures highest uniformities.

2.2.3. Source Molecules

The MO source materials for group-III are trimethylgallium (TMGa), trimethylindium (TMIn), trimethylaluminum (TMAI). PH_3 and AsH_3 are used for the gas source materials for group-V. Silane (SiH_4 , gas) and diethylzinc (DEZn, MO) are used for n-type and p-type doping, respectively.

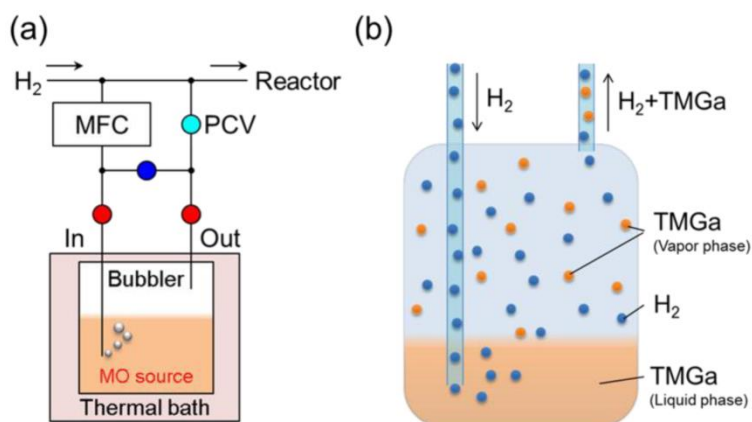


Figure 2-9 (a) Schematic illustration of the line for metal-organic (MO) source provided by bubblers [37].

The MO sources are provided in the bubblers, which are kept at a certain temperature by the thermal bath to control and maintain the partial pressure of material supply as shown in Figure 2-9(a). The carrier gas is led through the liquid or solid source material in the bubbler. As a result, the carrier gas contained MO sources with saturated vapor pressure, which is controlled by the temperature of the bubbler, is provided to the reactor (Figure 2-9(b)).

The partial pressure of each MO sources fed to the reactor is determined by the carrier gas flow through the bubbler which is controlled by mass-flow controllers (MFCs). Pressure controller keeps a fixed pressure in the bubbler, and then, mixture of H₂ and MO down to the reactor pressure. The vapor pressure of a MO sources is a critical parameter used to control the precise concentration of MO sources entering the reactor, and subsequently the rate of deposition in the MOVPE process. Hence, an accurate evaluation of the vapor pressures of the MO sources is essential to the MOVPE process. The vapor pressure equation in linear logarithmic form,

$$\log_{10} P_{MO} = B - A/T \quad (2-4)$$

has been found to be the most acceptable form for representing the vapor pressure of MO sources (P_{MO} (Torr)) in MOVPE, where T (K) is the absolute temperature of MO sources (or thermal bath) and A and B are the gas constant for each MO sources.

2.2.4. Thermal decomposition of Source Molecules

Supplied metal-organic (MO) and gas sources are thermally decomposed by the heated temperature of susceptor near the surface of substrate. The

decomposition behavior is dependent on the kinds of source material, and this factor is also important for the crystal growth. The thermal pyrolysis (or decomposition) of MO and gas sources has been studied [27-34]. Typically these studies monitor, optically or through mass spectrometry, the decrease in the concentration of a particular reactant as it passes through a SiO₂ reactor. The temperature ranges for thermal pyrolysis for various MO and gas sources are summarized in Table 2-1.

Table 2-1. Thermal pyrolysis (or decomposition) of various metal–organic (MO) and gas sources [37].

	Carrier gas & Experimental condition	Pyrolysis range (°C)	
		start	completed
TMGa	H ₂	370	470
TMGa	H ₂	400	580
TMGa	N ₂	450	570
TMIn	H ₂	~ 250	~ 340
TMIn	H ₂	~ 300	~ 340
TMIn	N ₂	~ 340	~ 430
AsH ₃	H ₂	650	750
AsH ₃	H ₂	~ 470	~ 640
AsH ₃	H ₂ + GaAs wafer	< 450	~ 640
AsH ₃	H ₂ + TMGa (V/III =25)	< 450	~ 570
AsH ₃	H ₂ + TMGa (V/III =10)	< 450	~ 570
TBP	H ₂	400	550

The kind of carrier gas affects the pyrolysis range, for instance, the pyrolysis range for TMGa diluted in N₂ is higher than that for H₂ carrier gas. In addition, the pyrolysis range for AsH₃ is strongly affected by the presence of GaAs wafer and TMGa [33].

2.2.4. Principle of MOCVD

The study of the kinetics in MOVPE involves the attempts to understand the actual processes how the vapor phase source materials are transformed into the atoms constituting the semiconductor solid. Because these mechanisms are extremely complex, the description of the processes should be divided into that of some major processes. The key processes during the crystal growth in MOVPE have been summarized by Stringfellow [35] and are listed below.

i. Mass transport: The carrier gas carries the source materials to the reactor. A boundary layer above the growing surface is formed by the laminar flow of the vapor in the reactor. Molecules diffuse through the boundary layer towards the surface before surface reactions can take place. The growth pressure and the velocity of the carrier gas define the thickness of the boundary layer.

ii. Physical process: At the surface during growth, adatoms such as molecules and radicals absorb at the substrate surface, and in homogeneously deposit at the surface. Adatoms incorporate into appropriate lattice positions at kinks or steps, or desorb into the vapor phase, while species at the surface diffuse at the substrate surface. At

the growing surface, two- or three-dimensional nucleation can be occur and surface takes the energetically stable configuration as a surface reconstruction, simultaneously.

iii. Chemical reactions: It must be taken into account for a more detailed description of the growth process. For MOCVD, the chemical processes have very complex radial reactions. Surface reconstruction, adsorption or desorption process of precursors, and density of step, kink or other defects are also strongly depended by the chemical reaction. Moreover, we should consider the thermal decomposition of source molecules under certain growth conditions.

iv. Thermodynamics: The growth rate is affected by thermodynamic properties since these define the deviation from equilibrium and thus the driving force for growth. The incorporation of native defects or dopants and surface stoichiometry are also influenced by thermodynamics. Furthermore, the reason to selective growth can be explained by thermodynamics.

Mass Transport (Boundary Layer Model)

The precursor gases are transported to the reactor with the carrier gas and flowing over the growth substrate. The boundary condition between the gas flow and the reactor walls or surface of substrate is that the velocity is zero according to Newton fluid model. Naturally, the velocity component perpendicular to the surface is zero since no flux across the boundary exists.

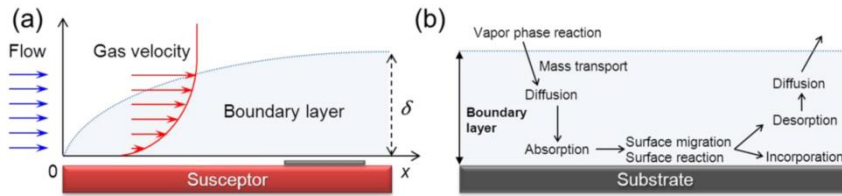


Figure 2-10 (a) Schematic illustration of the flow into the reactor, gas velocity decreasing near the susceptor surface, and boundary (stagnant) layer. The δ represents the thickness of boundary layer. The gas flow feeds from left side ($x < 0$, upper stream of the reactor) to right side ($x > 0$, downstream of the reactor) of this figure. The black rectangle lied on the susceptor represents the growth substrate. The vertical axis represents the direction, which is perpendicular to the surface of the susceptor or to the growth surface of the substrate. (b) Schematic illustration of the some kinds of mechanisms involved in the MOCVD process [37].

As a consequence of this boundary condition, the gas velocity is slower near the wall of the reactor as shown in Figure 2-10(a). This region, in which gas velocity is decreased, is referred to as the boundary layer. The boundary layer thickness, δ , defined here as the distance from the interface at which the velocity component parallel to the wall becomes 99% of its free-stream value, is inversely proportional to the square root of the gas velocity. The boundary layer model is the most widely used model for the calculation of the growth rate in the mass transport limited growth. This model assumes that mass transport occurs only by diffusion through the boundary layer.

Figure 2-10(b) shows schematic illustration of the different mechanisms involved in the MOVPE process. There are some concentration gradients of

the growth species during the growth, because the growth species are consumed at growth surface by incorporation of growth species into the crystal. The precursors diffuse from the gas flow to the surface of substrate driven by the concentration gradients of growth species. The diffusion flux from the boundary layer by concentration gradient, J_{in} , is

$$J_{in} \approx (P_{in-III} - P_{sub-III}) / RT_s \delta \approx P_{in-III} / RT_s \delta \quad (2-5)$$

where P_{in-III} is input partial pressure of group-III material in the gas flow, $P_{sub-III}$ is partial pressure of group-III material at the growth surface, R is gas constant, T_s is growth temperature and δ is thickness of boundary layer. In the case of planar growth, $P_{sub-III}$ can be ignored, because almost growth species at the growth surface consumed by the crystal growth. Under the standard growth condition for III-V compound semiconductors, group-V precursors are sufficient near the surface of the substrate and maintain a thermal equilibrium condition between the surfaces, because the partial pressure of group-V materials is much higher than that of group-III material. For instance, at standard growth condition of GaAs in MOVPE, concentration of TMGa is only 0.01 ~ 0.001 % in all of gas flow. Moreover, chemical reaction rate at the surface is much higher than the diffusion flux of precursors. Therefore, in the case of planar growth, desorption of group-III materials from the surface can be ignored, and the growth rate is determined by only J_{in} .

As for the co-relationship between δ and the growth rate, Leys and Veenvliet showed that increasing the flow velocity increases the growth rate due to a decrease in the mass transport boundary layer thickness [36]. This led to the idea of tilting the susceptor or superior wall of flow channel to compensate for gas phase depletion effects and the increasing boundary layer

thickness along the flow direction due to the developing concentration profile. The use of this reactor configuration of controlling the gas flow leads to improved thickness uniformity.

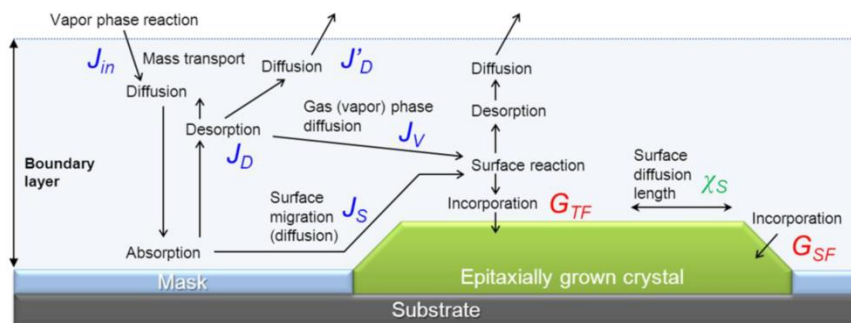


Figure 2-11 Schematic illustration of the some kinds of mechanisms involved in the selective-area (SA) MOVPE process [37].

In the case of selective-area growth, the situation is more complicated. Figure 2-11 shows schematic illustration of some kinds of mechanisms involved in the selective-area (SA) MOVPE process. We should take into account that the growth rate is affected by diffusion of the growth species from masked region and desorption to the outside of the boundary layer, in addition to controlling the boundary layer thickness and diffusion of growth materials etc. for the planar growth. G_{TF} and G_{SF} shown in Figure 2-11 indicate the growth rate for top and side facet of the grown crystal, respectively. In the case of $G_{TF} \gg G_{SF}$, G_{TF} is determined by J_{in} , J_V , and J_S . J_V is gas (vapor) phase diffusion flux from lateral direction, and J_S is surface

diffusion flux on side facet.

$$G_{TF} \propto J_{in} + J_V + J_S \quad (2-6)$$

Therefore, growth rate in SA-growth is affected by diffusion of the growth species from masked region. In addition, the diffusion flux of desorbed growth species from masked region, J_D is partially contribute to the crystal growth as J_V , and the other species diffuse to out of boundary layer existing on the masked region, as J'_D shown in Figure 2-116. J_D is indicated by following equation,

$$J_D = J_V + J'_D, \quad (2-7)$$

where J_D highly depends on the growth temperature. In addition, χ_S is diffusion length of group-III species on the growth surface, and this is indicated below.

$$\chi_S = \sqrt{D_S \tau_S} \quad (2-8)$$

Here, τ_S is the life time of growth species at the growth surface, where the life time means resident time from the growth species are absorbed on growth surface to those are left from surface by the incorporation of growth species into the crystal or the desorption. In addition, D_S is surface diffusion factor, and this is determined by next equation,

$$D_S = a^2 \nu \exp(-E_S/k_B T), \quad (2-9)$$

where a is lattice constant, ν is oscillation frequency of absorption molecules and E_S is activation energy of surface diffusion. Consequently, smaller E_S and/or higher temperature result in larger D_S . We thus need to

longer diffusion length of growth species (or precursors) to improve the flatness of grown surface in the SA-growth, because the growth species mainly diffuse from masked region to the opening area of surface. This is the reason why we use higher growth temperature in the SA-growth compared with the planar growth.

Another important point of the SA-growth is to avoid a deposition of poly-crystals on the masked region. Desorption of poly-crystals is dependent on J_{in} and τ . The τ is the life time of growth species (or precursors) on the masked region. Poly-crystals are preferentially deposited by longer τ , because the encounter probability of group-III species becomes higher for longer τ . On the other hand, τ can be shortened by increasing the probability of desorption of growth species under the higher growth temperature condition. Consequently, to suppress the deposition of poly-crystals on the masked region, we have to choose the growth condition with low J_{in} and short τ . In other words, we should carry out the crystal growth under the low working pressure and high growth temperature.

Physical Processes on Surface

At the surface during growth, adatoms (such as molecules and radicals) adsorb at the substrate, and inhomogeneously deposit at the surface. Adatoms incorporate into appropriate lattice positions at kinds or steps, or desorb into the vapor phase, while the species diffuse at the substrate surface. Desorbed species are transported away with the carrier gas. The surface during growth has been thought to consist of atomically flat regions separated by steps, as shown schematically in Figure 2-11. Kossel model (Terrace-Step-Kink

model) simply describes the thermodynamics of crystal surface formation and transformation. It is based upon the idea that the energy of an atom's position on a crystal surface is determined by its bonding to neighboring atoms and that stability involving the counting of bond formations. Thus, this model brings an intuitive understanding of the physical process on the surface structure.

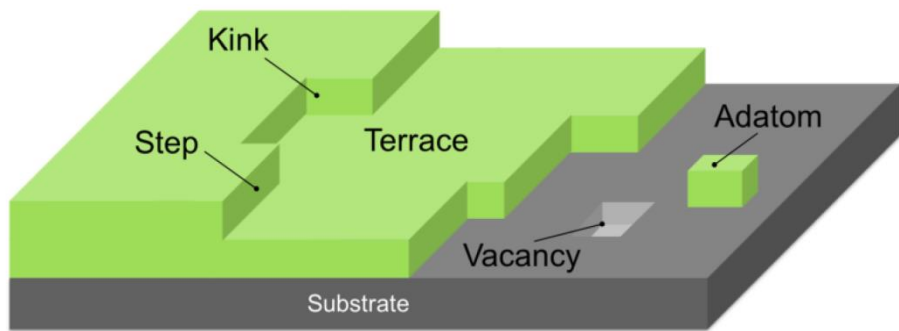


Figure 2-12 Schematic of arsenic–trimer coverage on GaAs (111)B surface [37].

2.3. Characterization

2.3.1. Nomarski DIC microscope

After the epitaxial growth, the samples are first characterized by Nomarski differential interference contrast (DIC) microscope before any other more sophisticated characterization tools. Optical microscopy is used to investigate the layer morphology, defects, and degree of selectivity of SAG. Although a smooth layer does not necessarily guarantee a high quality growth, a rough surface is often found to be highly defective. Likewise, a perfect selective growth does not necessarily guarantee a desired epilayer characteristic, but a non-selective growth is often undesirable in a device structure.

A Nomarski DIC microscope is composed of a light source, a polarizer, a DIC prism, a condenser, a movable sample stage, an objective, a DIC slider, and an analyzer. Nomarski DIC amplifies contrast by using the principle of interferometry of polarized light. First, the light emitted from the light source is polarized by the polarizer. The polarized light is then separated into two signals that are perpendicular to each other by the DIC prism. When the separated signals pass through the sample of different refractive indexes, one of lights is delayed. Finally the two signals are combined by the DIC slider and analyzer. It is the phase difference between the two signals that produces an interference contrast in the image.

The theoretical resolution, R , of an optical microscope is given by the following equation:

$$R = 0.61\lambda/NA \quad (2.10)$$

where R is the smallest resolvable distance between two objects, NA is the microscope numerical aperture, and λ is the wavelength of the light source.

2.3.2. Field emission scanning electron microscope

FE-SEM analyses were performed by using a SU-70 of Hitachi, which incorporates a cold field emission electron source and provides 1 nm microscope resolution at 10 kV, magnification range of 30 - 800,000x

2.3.3. Transmission electron microscope

The TEM specimens were made by using focused ion beam (FIB). The cross-sectional and plan-view images of transmission electron microscopy (XTEM) were obtained by a JEOL JEM-2100F in Korea Advanced Nano Fab Center and JEOL JEM-3000F in Seoul National University. Bright field techniques were used to observe the threading dislocations.

2.3.4. Atomic force microscopy (AFM)

Non-contact AFM measurements were performed in using Park systems XE-100 in order to investigate surface morphology. The Au-coated Si tips were used. For statistical analyses, XEI ver. 1.8.0 was used.

2.3.5. High resolution X-ray diffractometry (HR-XRD)

Panalytical X'pert instrument was used for high resolution XRD measurement and ω -scan. The angle divergence of 12 arcsec or less can be obtained by 4 bounce Ge 022 channel cut monochromator.

2.4. References

- [1] Ben Streetman and Sanjay Banerjee, *Solid State Electronic Devices*, Prentice Hall (1998)
- [2] R. People and J.C. Bean, "Calculation of critical layer thickness versus lattice mismatch $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained-layer heterostructures," *App. Phys. Lett.*, **47(3)**, 322-324 (1985)
- [3] Tien P. K. Original version of the graph is courtesy of P. K. Tien of AT&T Bell Laboratories (1988)
- [4] A. Segmuller, "Characterization of Epitaxial Films by X-ray Diffraction", *Advances in X-ray Analysis* **29**, 353 (1985)
- [5] M. Sugo, Y. Takanashi, M.M. Al-jassim, M. Yamaguchi, Heteroepitaxial growth and characterization of InP on Si substrates, *J. Appl. Phys.* **68** (1990) 540–547
- [6] Y.T. Sun, K. Baskar, S. Lourduoss, Thermal strain in indium phosphide on silicon obtained by epitaxial lateral overgrowth, *J. Appl. Phys.* **94**, 2746–2748 (2003)
- [7] J. F. Klem, E. D. Jones, D. R. Myers, and J. A. Lott: Characterization of thin AlGaAs/InGaAs/GaAs quantum-well structures bonded directly to SiO₂/Si and glass substrates, *Journal of Applied Physics* **66**, 459-462 (1989)
- [8] S. M. Ting, R. M. Sieg, S. A. Ringel, and E. A. Fitzgerald: Range of Defect Morphologies on GaAs Grown on Ocult (001) Ge Substrates, *Journal of Electronic Materials* **27**, 451 (1998)

- [9] M. R. Brenner: GaP/Si Heteroepitaxy (Suppression of Nucleation Related Defects), Master Thesis, The Ohio State University, (2009)
- [10] J. E. Ayers: Heteroepitaxy of semiconductors : theory, growth, and characterization, CRC Press Taylor & Francis Group, (2007)
- [11] S. M. Ting: Monolithic Integration of III-V semiconductor materials and devices with silicon, Dissertation, Massachusetts Institute of Technology (MIT), (1999)
- [12] M. R. Brenner: GaP/Si Heteroepitaxy (Suppression of Nucleation Related Defects), Master Thesis, The Ohio State University, (2009)
- [13] M. E. Gronert: Monolithic Heteroepitaxial Integration of III-V semiconductor Lasers, Dissertation, Massachusetts Institute of Technology (MIT), (2002)
- [14] Y. Li, G. Salviati, M. M. G. Bongers, L. Lazzarini, L. Nasi, and L. J. Giling : On the formation of antiphase domains in the system of GaAs on Ge, *Journal of Crystal Growth* **163**, 195 - 202 (1996)
- [15] S. L. Wright, M. Inada, and H. Kroemer: Polar-on-nonpolar epitaxy: Sublattice ordering in the nucleation and growth of GaP on Si(211) surfaces, *Journal of Vacuum Science and Technology* **21**, 534-539 (1982)
- [16] D. B. Holt: Antiphase boundaries in semiconducting compounds, *Journal of Physical Chemistry of Solids* **30**, 1297 (1969)
- [17] S. M. Ting, and E. A. Fitzgerald: Metal-organic chemical vapor deposition of single domain GaAs on Ge/GexSi1-x/Si and Ge substrates,

Journal of Applied Physics **87**, 2618-2628 (2000)

[18] R. Kaplan: LEED study of the stepped surface of vicinal Si (100), *Journal of Surface Science* **93**, 145-158 (1980)

[19] B. Z. Olshanetsky and A. A. Shklyaev: Phase transitions on clean Si(110) surfaces, *Journal of Surface Science* **67**, 581-588 (1977)

[20] Y. Ishida, T. Takahashi, H. Okumura, and S. Yoshida: Investigation of antiphase domain annihilation mechanism in 3C-SiC on Si substrates , *Journal of Applied Physics* **94**, 4676-4689 (2003)

[21] M. Kawabe, and T. Ueda: Self-Annihilation of Antiphase Boundary in GaAs on Si(100) Grown by Molecular Beam Epitaxy, *Japanese Journal of Applied Physics* **26**, 944-946 (1987)

[22] A. Hashimoto, N. Sugiyama, and M. Tamura: In-situ Characterization of the Initial Growth Stage of GaAs on Si by Coaxial Impact-Collision Ion Scattering Spectroscopy, *Japanese Journal of Applied Physics* **30**, 3755-3758 (1991)

[23] S. Strite, D. Biswas, N. S. Kumar, M. Fradkin, and H. Morkoc: Antiphase domain free growth of GaAs on Ge in GaAs/Ge/GaAs heterostructures , *Applied Physics Letters* **56**, 244-246 (1990)

[24] V. Narayanan, S. Mahajan, K. J. Bachmann, V. Woods, and. N. Dietz: Stacking faults and twins in gallium phosphide layers grown on silicon, *Philosophical Magazine A* **82**, 685 (2002)

[25] K. Umeno, Y. Furukawa, A. Wakahara, R. Noma, H. Okada, H. Yonezu,

Y. Takagi and H. Kan: MBE growth of GaAsN/GaP(N) quantum wells with abrupt heterointerfaces for photonics applications on Si substrates, *Journal of Crystal Growth* **311**, 1748 - 1753 (2009)

[26] M. E. Gronert: Monolithic Heteroepitaxial Integration of III-V semiconductor Lasers, Dissertation, Massachusetts Institute of Technology (MIT), (2002)

[27] T.F. Kuech, "Metal–Organic Vapor Phase Epitaxy of Compound Semiconductors", *Materials Science Reports*, **2** (1987) 1–50

[28] M. Yoshida, H. Watanabe, and F. Uesugi, "Mass Spectrometric Study of Ga(CH₃)₃ and Ga(C₂H₅)₃ Decomposition Reaction in H₂ and N₂", *J. Electrochem. Soc.*, **132** (1985) 677.

[29] J. Nishizawa, and T. Kurabayashi, "On the Reaction Mechanism of GaAs MOCVD", *J. Electrochem. Soc.*, **130** (1983) 413.

[30] C.A. Larsen, and G.B. Stringfellow, "Decomposition Kinetics of OMVPE Precursors", *J. Cryst. Growth*, **75** (1986) 247.

[31] J. Haigh, and S. O'Brien, "The Mechanism of the Growth of InP by MOCVD: A Flow– Tube Investigation of the Pyrolysis of the Indium Precursor", *J. Cryst. Growth*, **68** (1984) 550.

[32] N.J. Buchan, C.A. Larsen, and G.B. Stringfellow, "Mass Spectrometric Studies of Trimethylindium Pyrolysis", *J. Cryst. Growth*, **92** (1988) 591.

[33] S.P. DenBaars, B.Y. Maa, P.D. Dapkus, A.D. Danner, and H.C. Lee, "Homogeneous and Heterogeneous Thermal Decomposition Rates of

Trimethylgallium and Arsine and Their Relevance to the Growth of GaAs by MOCVD”, *J. Cryst. Growth*, **77** (1986) 188.

[34] C.H. Chen, C.A. Larsen, and G.B. Stringfellow, D.W. Brown, A.J. Robertson, “MOVPE Growth of InP Using Isobutylphosphine and Tert-Butylphosphine”, *J. Cryst. Growth*, **77**(1986).

[35] G. B. Stringfellow, “Organometallic Vapor-Phase Epitaxy: Theory and Practice, Second Edition”, (*Academic Press, Inc.*, 1999).

[36] M.R. Leys, and H. Veenvliet, “A Study of the Growth Mechanism of Epitaxial GaAs as Grown by the Technique of Metal Organic Vapour Phase Epitaxy”, *J. Cryst. Growth*, **55** (1981) 145.

[37] Yoshinori Kohashi, “Growth Dynamics and Applications of Selectively-Grown InGaAs Nanowires”, (Doctor dissertation, 2014).

Chapter 3

GaP blanket growth on Si (001) substrates

3.1. Introduction

The defect-free nucleation of III/V-layer structures on Si (001)-substrate is of key importance for the future integration of III/V-device structures such as lasers, solar cells or n-channel layer stacks on Si. “Silicon photonics” aims in combining the advantages of optical data processing with the mature Silicon-microelectronic technology. This merge becomes more and more essential for future high-speed technology and enters various fields of applications. One of the key interests concentrates on the integration of reliable lasers on Si-based integrated circuits for inter- and intra-chip optical interconnects. Because of the indirect bandgap of silicon and hence its low light emission efficiency, a lot of effort has been devoted to the monolithic growth of direct band gap III/V semiconductors like GaAs or InP on Si substrate [1-2]. These attempts suffer from the high densities of threading dislocations due to the large lattice mismatch and result in no long-term stable lasing operation of the devices. Other approaches focus on wafer bonding of III/V lasers on Si-substrates [3], an approach which is difficult to accomplish site-selectively on the Si substrates. Other groups again focus on the exploitation of the Raman effect [4] or of silicon nanostructures [5-6] to add optoelectronic functionalities to Si-substrates.

To overcome the shortcomings of the above-mentioned concepts, our approach to realize a monolithically integrated laser or high speed n-channel device on silicon substrate is different. We grow the nearly lattice-matched III/V semiconductor GaP on Si by metal organic vapor phase epitaxy (MOVPE).

A defect-free pseudomorphic nucleation of GaP on exact (001) silicon would allow for a monolithic integration of the Ga(NAsP) laser with CMOS-compatible exact (001)Si substrates. CMOS industry requires these substrates, as all processing steps for devices, which, are nowadays used, are specified on these substrates, which have a maximum miscut of $\pm 0.5^\circ$ the [001] orientation. Re-specification of processes on substrates having larger offcut angles would be extremely cost-intensive and is highly improbable.

With the growth of a polar III/V semiconductor like GaP on nonpolar Si substrate, various challenges inevitably arise [7]. It is essential to ensure charge neutrality along the interface and avoid unwanted cross-doping caused by atom diffusion into the respective heterolayers. Mono-atomic steps on the group IV substrate surface lead to antiphase disorder in the compound side of the interface. Antiphase domains (APDs) and antiphase boundaries (APBs) are caused by the fact that the diamond lattice of Si consists of a one-atomic basis whereas the zinc-blende lattice of GaP is built

from a two-atomic basis. Therefore a mono-atomic stepped Si surface initiates APBs in the III/V layer at each terrace edge. A crystal model in Fig. 3-1 shows in [1-10] projection possible APB configurations. In this sketch the APBs lay on the $\{110\}$ or the $\{111\}$ planes, respectively. Self-annihilation is possible if two APBs cross each other as indicated in Fig. 1 for the APBs on the $\{111\}$ lattice planes. In order to achieve an antiphase domain free GaP layer either a perfect doubling of all Si surface steps must be enforced and/or self-annihilation of all APD ensured.

From literature it is known, that an “as-polished” exactly (001)-oriented Si surface commonly reveals a mono-atomic stepped surface. These terraces consist of alternating 1×2 and 2×1 dimerization corresponding to different diamond structure sublattices, respectively. The steps are denoted with S_A and S_B [8] according to whether the dimerization on the upper terrace is perpendicular (A) or parallel (B) to the step edge. In the same way there is a nomenclature for double steps: D_A (D_B) for dimers perpendicular (parallel) to the double step edge.

The tendency of step doubling with increasing annealing temperature was proven for off-orientated Si substrates. On a perfectly double-stepped surface all step terraces belong to the same sublattice, hence, there must be a preference for one of the two Si sublattices over the other. Since the two

kinds of sublattice planes differ from each other only by a 90° rotation in space, the preferential mechanism must include atomic arrangement at the double edges. Aspnes and Ihm [8] introduced a π -bonded step reconstruction at D_B steps that lowers the enthalpy significantly in relation to the dangling bond configuration at D_A steps or both kinds of mono-layer steps.

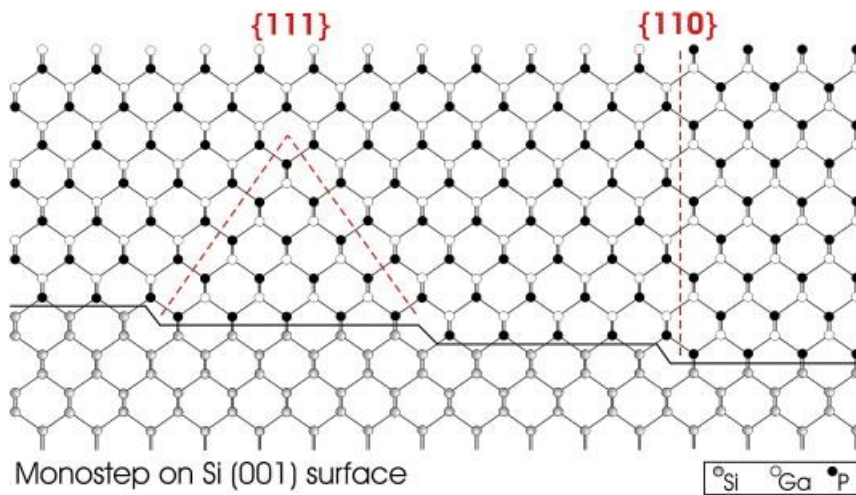


Figure 3-1 Sketch of the APB formation in the $\{111\}$ and $\{110\}$ lattice planes of the GaP zinc-blende structure due to the presence of mono-layer steps on the Si surface [15].

The energetic preference for D_B terraces is most pronounced for surface misorientation corresponding to a rotation about one of the two $\langle 110 \rangle$

directions, allowing the formation of D_B steps that line up parallel to the $\langle 110 \rangle$ direction, respectively. In view of these aspects, one would suppose that even a slight miscut of an exact orientated substrate will affect the possibility of step doubling. A further crucial condition is temperature together with sufficiently long time to permit diffusion of Si atoms to form the favourable DB steps. Since the 1980s much literature has been published about Si surface preparation in ultra-high vacuum (UHV) systems, e.g. like molecular beam epitaxy (MBE) systems. The π -bond calculation in [8] also refers to a clean Si surface, but the scenario in a VPE chamber is very different and the presence of hydrogen carrier gas should have an impact on the surface reconstruction [9].

This paper presents a growth procedure for realizing a low defect density GaP layer on a Si substrate. The growth procedure consists of two parts. One is the optimization of GaP with various growth conditions on Si substrate. Another one is the InP growth optimization using GaP buffer layers on Si substrate. Growth mechanism is explained by simplified growth models based on the observation of initial growth modes.

3.2. Experimental details

The MOCVD Si-growth of all samples under investigation took place in an Aixtron AIX 2400G3 reactor system using Pd-purified H₂ as carrier gas. The substrates used in this study were 2" p-type on-axis Si (001). The In, Ga, Al, P and As sources were trimethylindium(TMI), trimethylgallium(TMg), trimethylaluminum(TMA), phosphine(PH₃) and Tertiarybutylarsine (TBA), respectively. Initial experimentation was performed by using a two-step growth method and optimizing growth conditions on planar Si (001) substrates. A typical sequence for growing InP/GaP on Si is shown schematically in Fig. 3-2. Si substrates are preheated at 830°C for 30min in a H₂ atmosphere to remove thin oxide films prior to epitaxial growth. The first 5nm-thick GaP nucleation layer is deposited at 400°C followed by a 50nm-thick GaP intermediate layer grown at 700°C. The growth rates are 0.1Å/s and 3.8 Å/s, respectively. Then the growth temperature is decreased to 400°C for InP buffer layer growth with 60nm thickness and finally the top InP 600nm thick layer is grown at 650°C and 550°C.

The surface morphology and step formation of the annealed Si samples were investigated in an atomic force microscope (AFM) (SPA 500) working

in tapping mode with standard silicon tips. The AFM imaging was carried out without any specific sample preparation or environment condition. For the transmission electron microscopy (TEM) imaging, [1-10] and [110] cross sections of the InP/GaP/Si heterostructures were prepared by mechanical grinding and polishing followed by Ar ion milling. For the imaging we used a JEOL JEM 3010 UHR utilizing a special dark field technique.

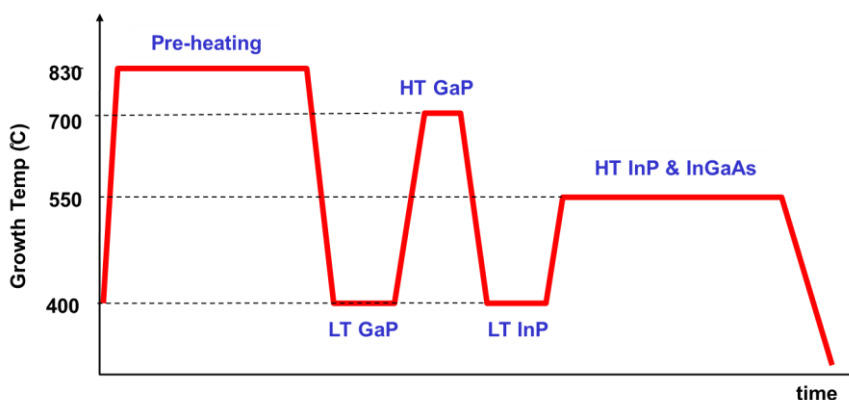


Figure 3-2 Growth sequence of InP/GaP epilayers on Si substrates.

3.3. Results and Discussion

The following presentation of our results is split in two parts: we first explain the optimization of GaP epi layers on Si, depending on different growth conditions (like growth temperature, growth rate, V/III ratio and

growth mode). Subsequently, results of InP epi layers using the upper GaP buffer layers with best growth conditions will be explained, depending on the different structures.

3.3.1. Optimization of LT GaP nucleation on Si

3.3.1.1. Annealing of Si substrates : influence of reactor pressure

AFM images of bare Si substrates annealed for 30 min at 830°C in different reactor pressures of H₂ ambient ((a) no annealing (b) 100 mbar (c) 500 mbar (d) 950 mbar) are shown in Fig. 3-3. The nominal specification (as given by the supplier) of the Si substrates was exact (001) $\pm 0.5^\circ$. All Si substrates exhibited a slight misorientation in a random direction if not specified explicitly. The scan area of all AFM images was $5 \times 5 \mu\text{m}^2$. From the measurement of line scans we know that all steps, which can be seen in the AFM images depicted in Fig. 3-3 corresponds to a step height equal to one Si monolayer in the [001] direction (i.e., 0.136nm). One of the <110> cleavage directions is marked in every image. As the reactor pressure for annealing is increased, the terrace steps appear and the width of terrace is decreased. However, at the 950 mbar reactor pressure, terrace steps

disappear and look like bare Si substrate, i.e., no annealed surface. The step edge of 100 mbar (b) is always triangular shaped and the other one of 500

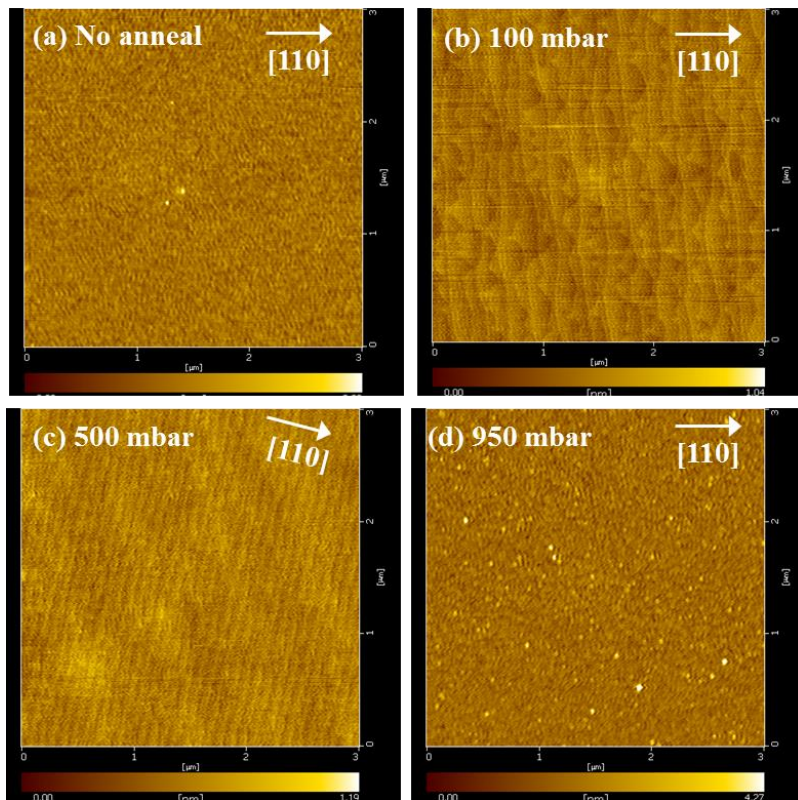


Figure 3-3 AFM images of the surface of bare Si substrates after annealed at 830°C for 30min in different reactor pressures of H₂ ambient. (a) no annealing (b) 100 mbar (c) 500 mbar (d) 950 mbar.

mbar (c) is uncertain step edge shape because the width is too small to distinguish the shape. After growth of GaP layers we can find that the (c) sample has also triangular shape like sample (a) due to surface having APBs.

Comparing those surface images to the literature [10-12], one could conclude that the step with triangular shape is the one named S_B step. Consequently, all steps of these annealed samples have single step and as suggested by the theory, the single step always forms in one of the $\langle 110 \rangle$ directions, which can also be concluded from fig. 3-3 (b) and (c), where a clear tendency towards stepping in the $[110]$ direction is observed.

Figure 3-4 shows AFM images of the surface of Si substrates after annealed at 830°C for different annealing time in 100 mbar reactor pressures of H_2 ambient (a) 15min (b) 30min (c) 120min. Step width is wider as annealing time is increased, however, for over 2 hours annealing time, the step width is narrow rather than 30min. It means that there is optimum annealing time to get the wider surface step.

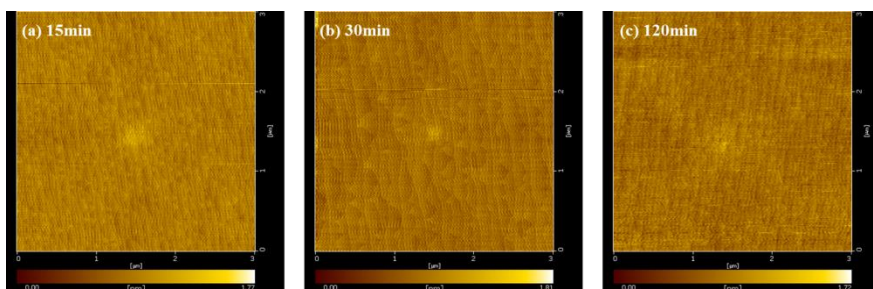


Figure 3-4. AFM images of the surface of bare Si substrates after annealed at 830°C for different annealing time in 100 mbar reactor pressures of H_2 ambient. (a) 15min (b) 30min (c) 120min.

Figure 3-5 shows AFM images of the surface of bare Si substrates after annealed at 830°C for 30min in 100 mbar reactor pressures of H₂ ambient using different substrate orientations. (a) exact (b) 2° off (c) 4° off (d) 6° off toward [110] direction respectively. For off-cut wafers regardless of angle, no stepped surface found different from prior studies.

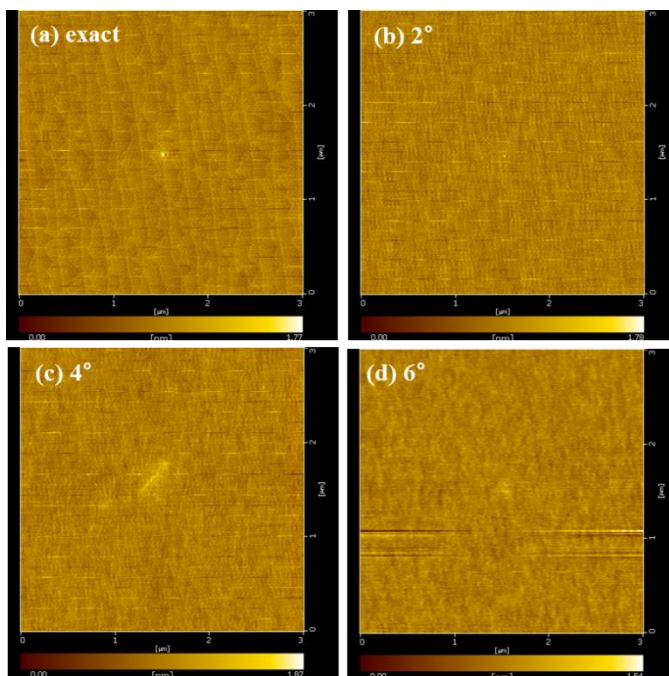


Figure 3-5. AFM images of the surface of bare Si substrates after annealed at 830°C for 30min in 100 mbar reactor pressures of H₂ ambient using different substrate orientations. (a) exact (b) 2° off (c) 4° off (d) 6° off toward [110] direction respectively.

3.3.1.2. Effects of growth temperature on LT GaP growth

This section explains the effects of annealing reactor pressure on LT GaP growth on Si. Figure 3-6 shows SEM micrographs of LT-GaP layers grown at different growth temperature after annealed at at 830°C for 30min in 950 mbar reactor pressure. (a) 450 °C (b) 500 °C (c) 550 °C respectively. The final GaP thickness is 100nm and growth rate is between 0.1 and 0.15 Å/s. All the samples of LT GaP layers grown on Si are founded as 3D growth. As the growth temperature increase 3D islands tends to be bigger so the roughness of LP GaP layers increase. Even though grown at 450°C, the lowest growth temperature in this paper, LT GaP layers was not merged. As shown in figure 3-3, the surface of annealed Si in 950mbar reactor pressure does not have stepped surface. As a result, LT GaP layers cannot have 2D surface if the surface before growth does not have stepped surface after H2 annealing.

Figure 3-7 shows SEM images of LT-GaP layers grown at different growth temperature after annealed at at 830°C for 30min in 500 mbar reactor pressure. (a) 400 °C (b) 425 °C (c) 450 °C respectively. On the other hand, for the 950mbar reactor pressure case, all the samples were grown by 2D scheme. As the growth temperature increases the surface roughness increases and white spots more appears. The white spots seen in Figure 3-7

are formed by the termination of threading dislocations and APBs. It is well known that lower temperature growth is positive effect on surface roughness in III-V growth on Si substrates.

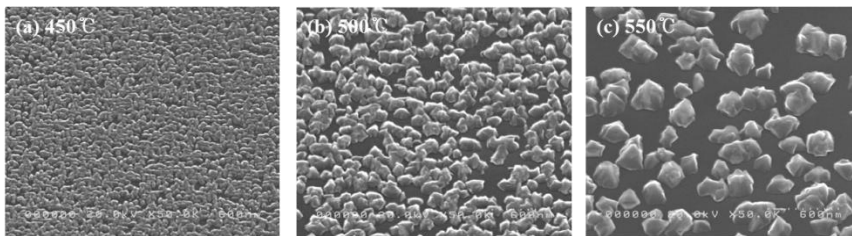


Figure 3-6. SEM micrographs of LT-GaP layers grown at different growth temperature after annealed at at 830 °C for 30min in 950 mbar reactor pressure. (a) 450 °C (b) 500 °C (c) 550 °C respectively.

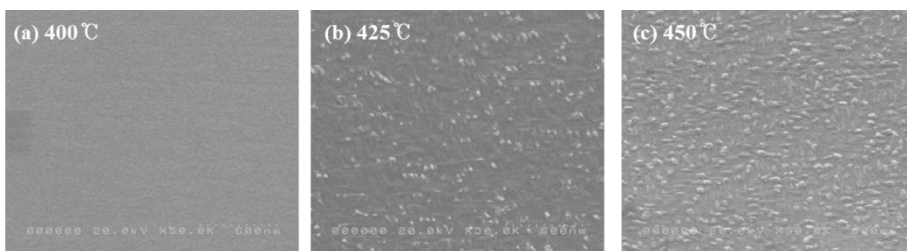


Figure 3-7. SEM images of LT-GaP layers grown at different growth temperature after annealed at at 830 °C for 30min in 500 mbar reactor pressure, (a) 400 °C (b) 425 °C (c) 450 °C respectively.

Figure 3-8 shows SEM images of LT-GaP layers grown at different growth

temperature after annealed at at 830°C for 30min in 100 mbar reactor pressure. (a) 400 °C (b) 425 °C (c) 450 °C respectively. All the samples were grown by the two dimensional growth mode and have very smooth surface. As the growth temperature increases, the surface roughness increases. White spots appear in the sample grown at 450°C, however, no white spots in samples grown at both 400 and 425°C resulting from the long diffusion length of precursors. Once the GaP nucleated at the APB or terminated dislocations, the next GaP growth tends to grow on those GaP nucleation layer rather than the smoother surface due to the long diffusion length in higher growth temperature.

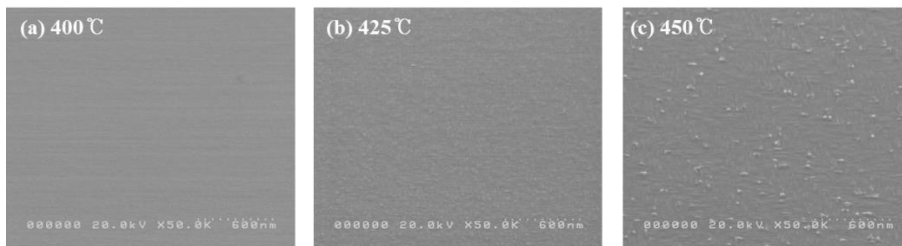


Figure 3-8. SEM images of LT-GaP layers grown at different growth temperature after annealed at at 830°C for 30min in 100 mbar reactor pressure. (a) 400 °C (b) 425 °C (c) 450 °C respectively.

Figure 3-9 shows the summary of annealing reactor pressure effect on LT

GaP growth on Si substrate. As mentioned before, 3D nucleation happens for the sample annealed in a 950 mbar reactor pressure and 2D nucleation happens for samples annealed less than 500 mbar reactor pressure.

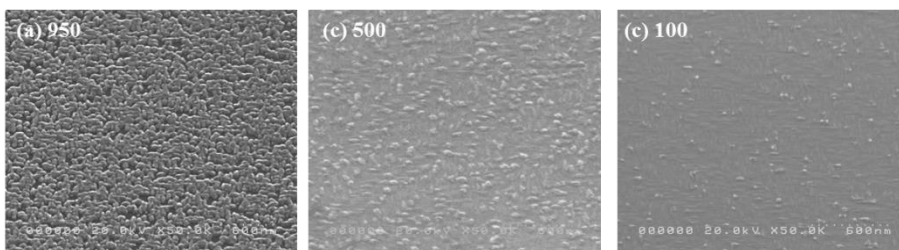


Figure 3-9. SEM images of LT-GaP layers grown at 450 °C after annealed at 830 °C for 30min in different reactor pressure, (a) 950 (b) 500 (c) 100 mbar respectively.

3.3.1.3. Effects of V/III ratio on LT GaP growth

Figure 3-11 shows SEM and AFM images of LT-GaP layers grown at different V/III ratio and growth rate of (a) V/III=5000, growth rate=0.16Å (b) V/III=1000, growth rate=0.22Å, (c) V/III=500, growth rate=0.25Å respectively. All of samples are grown at 425 °C after annealed at 830 °C for 30min in 150 mbar reactor pressure. We changed the V/III ratio as changing the mole flow of Ga precursor so higher V/III ratio has lower growth rate. RMS roughness increases as the V/III ratio decreases from 5 × 5

μm^2 AFM images. In higher growth rate and lower V/III sample, the surface of GaP nucleation layers has a lot of thin GaP stipe lines, result from tendency of GaP growth on the rough GaP nucleation.



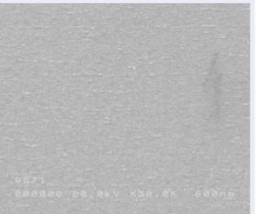
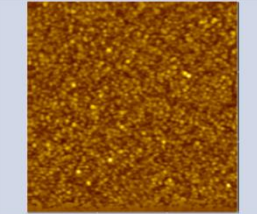
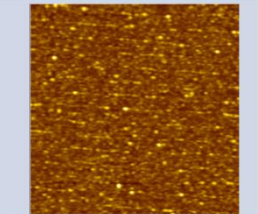
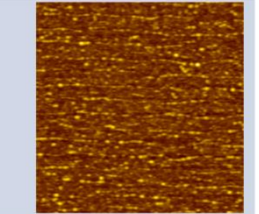
	(a) V/III=5000, GR=0.16Å	(b)V/III=1000, GR=0.22Å	(c) V/III=500, GR=0.25Å
rms	0.555 nm	0.74 nm	0.958 nm
SEM			
AFM			

Figure 3-11. SEM and AFM images of LT-GaP layers grown at different V/III ratio and growth rate of (a) V/III=5000, growth rate=0.16Å (b) V/III=1000, growth rate=0.22Å, (c) V/III=500, growth rate=0.25Å respectively. All of samples are grown at 425 °C after annealed at 830 °C for 30min in 150 mbar reactor pressure.

3.3.1.4. Effects of growth mode on LT GaP growth

We investigated effects of growth mode on LT GaP layers as well as

growth temperature and growth rate. Flow rate modulated growth, where, the groups III and V precursors are sent one after the other in pulsed mod in the reactor, as schematically depicted in figure 3-15. For continuous growth the nucleation is started with both Ga and P precursors simultaneously injected. Flow-rate modulated growth is characterized by alternating injection of PH₃ and TMGa into the reactor. Each pulse is followed by a growth interruption of 1s, during which no precursor flows into the reactor.

Figure 3-13 shows samples which were grown and nucleated using continuous epitaxy at 400°C after annealed at at 830°C for 30min in 100 mbar reactor pressure using different growth mode, (a) continuous nucleation, (b) FME respectively. RMS roughness of each sample is same as 0.17nm. It means the surface morphology is not affected by growth mode in LT GaP layers differently compared to other study groups [13-14]. Flow rate rate modulated growth, where the groups III and V precursors are sent one after the other in pulsed mode in the reactor, results in higher diffusivity of the atoms than continuous growth. RMS roughness is same for both cases, however white spots as seems to be Ga droplets are bigger in FME mode than that of continuous mode. This results from deposited during the first tow monolayers, Ga and P have not to be precisely controlled. These droples can deteriorate the surface morphology of the GaP overgrowth layer and can

increase the number of defects in this layer. This will be addressed later after HT GaP growth (figure 3-17).

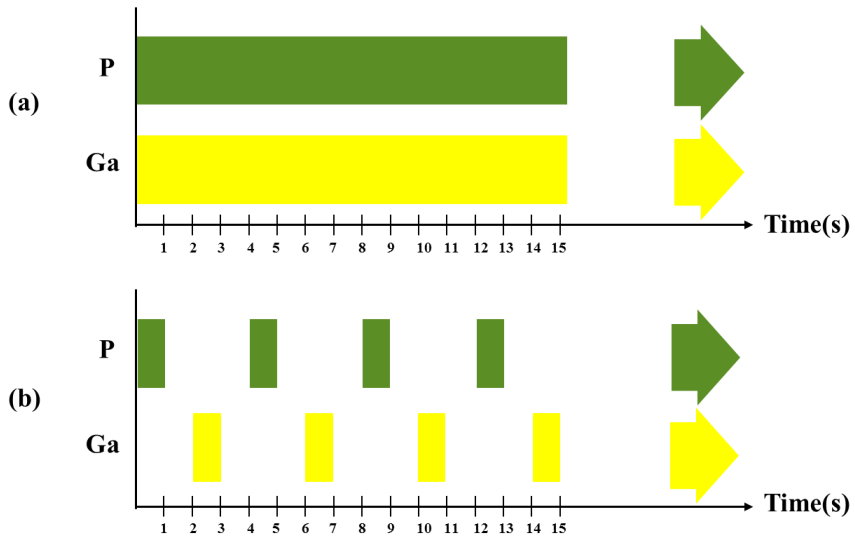


Figure 3-12. Schematic depiction of the time dependences of the metal organic precursor injection during continuous (a) or flow rated modulated (b) epitaxy. The nucleation was either started by P for both cases.

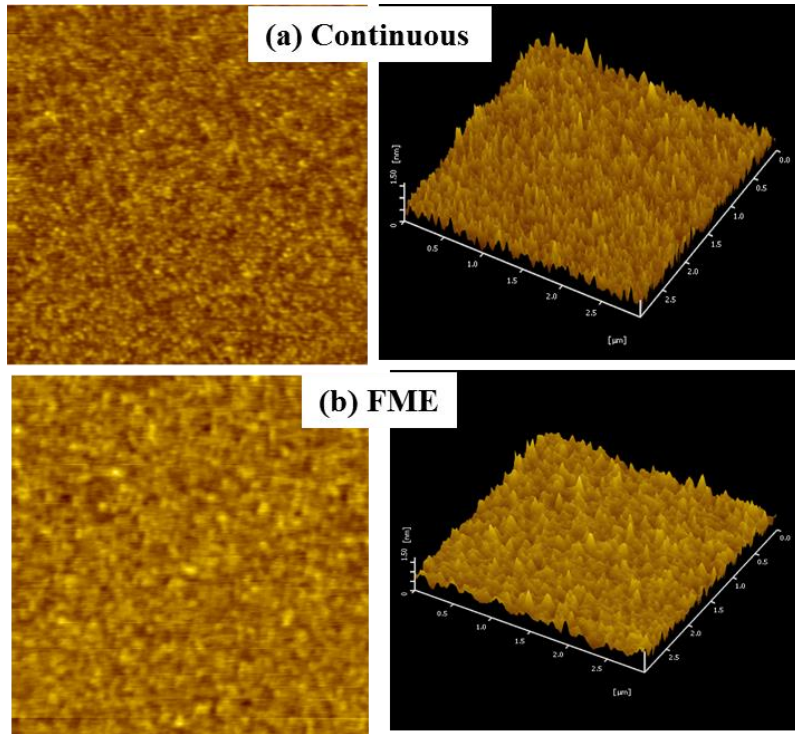


Figure 3-13. AFM images of LT-GaP layers grown at 400 °C after annealed at at 830 °C for 30min in 100 mbar reactor pressure using different growth mode, (a) continuous nucleation, (b) FME respectively. RMS roughness of each sample is same as 0.17nm.

3.3.2. Optimization of HT GaP growth on Si

3.3.2.1. Growth temperature of HT GaP layers

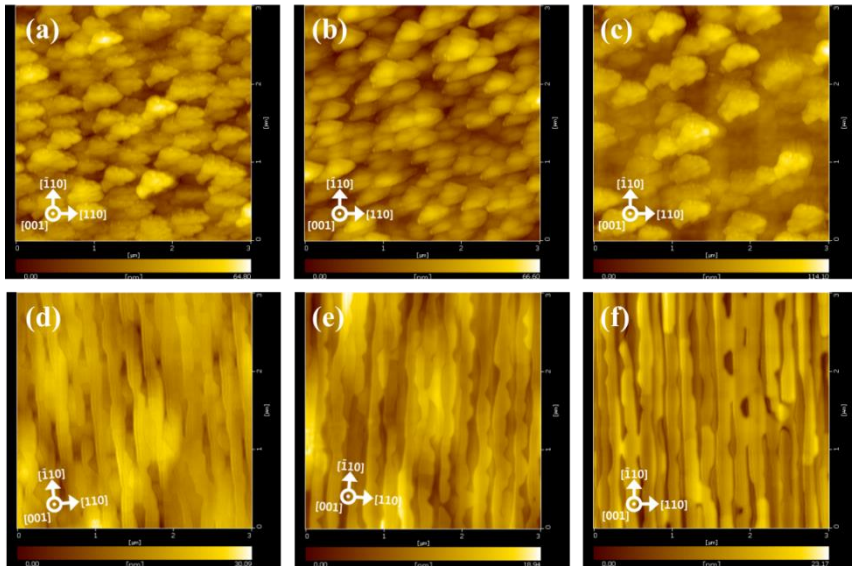


Figure 3-14. AFM images of GaP bulk layers grown at different growth temperature (a) 500 °C, (b) 525 °C, (c) 550 °C, (d) 650 °C, (e) 700 °C, (f) 800 °C respectively. LT-GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 10.9nm, (b) 10.8nm, (c) 18.9nm, (d) 4.3nm, (e) 2.94nm, (f) 3.44nm respectively.

AFM images of GaP bulk layers grown at different growth temperature (a) 500 °C, (b) 525 °C, (c) 550 °C, (d) 650 °C, (e) 700 °C, (f) 800 °C

respectively were shown in Figure 3-12. LT-GaP nucleation layers of all samples were grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 10.9nm, (b) 10.8nm, (c) 18.9nm, (d) 4.3nm, (e) 2.94nm, (f) 3.44nm respectively. High surface roughness and island growth mode was shown in GaP layers grown at less 650°C, however, dramatically smooth surface in grown samples at over 650°C growth temperature and striped APBs were also shown in those samples.

3.3.2.2. V/III ratio and growth rate of HT GaP layers

Figure 3-14 shows AFM images of GaP bulk layers grown at 700 °C with different V/III ratio (a) 5000 (b) 1000, (c) 500, (d) 100 respectively. LT-GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 2.9nm, (b) 2.1nm, (c) 2.0nm, (d) very hazy respectively and last sample (d) is measured by Normalski optical microscopy due to very hazy surface.

In the middle of V/III ratio, 500, by changing PH3 flow rate at fixed Ga flow rate, APBs shape was changed from stripe to randomly round. Surface roughness slightly decreased as the V/III ratio decreased from 5000 to 500. APBs shape in samples with lower V/III ratio and higher growth rate was shown in figure 3-16. APBs shape was changed clearly with V/III ratio,

however, there was no tendency with V/III ratio. For V/III=500 sample, as shown in figure 3-15 (c), APBs have striped shape and randomly round shape in a V/III=250 sample, finally striped shape appears again in a V/III=100 sample. APBs density increased in two times higher growth rate than a sample (c) as shown in figure 3-15 (d). Figure 3-17 shows GaP bulk layers grown at 700°C on LT-GaP nucleation layers grown at 400 °C having 3nm-thickness using different growth mode. Left panel : continuous nucleation, right panel : FME nucleation. (a and b) : AFM images of the surface of the approximately 100 nm thick GaP layers having rms (a) 2.9nm and (b) 2.8nm respectively. (c and d) : bright field ($g=(001)$) cross-sectional TEM micrograph of the GaP/Si layer system.-

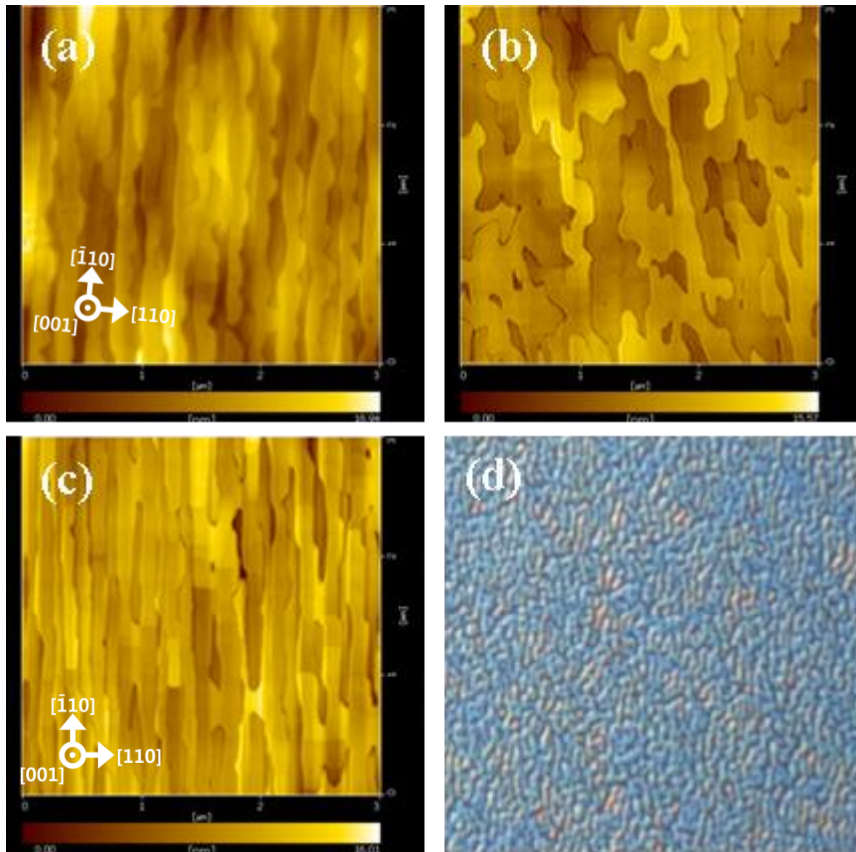


Figure 3-15. AFM images of GaP bulk layers grown at 700 °C with different V/III ratio (a) 5000 (b) 1000, (c) 500, (d) 100 respectively. LT-GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 2.9nm, (b) 2.1nm, (c) 2.0nm, (d) very hazy.

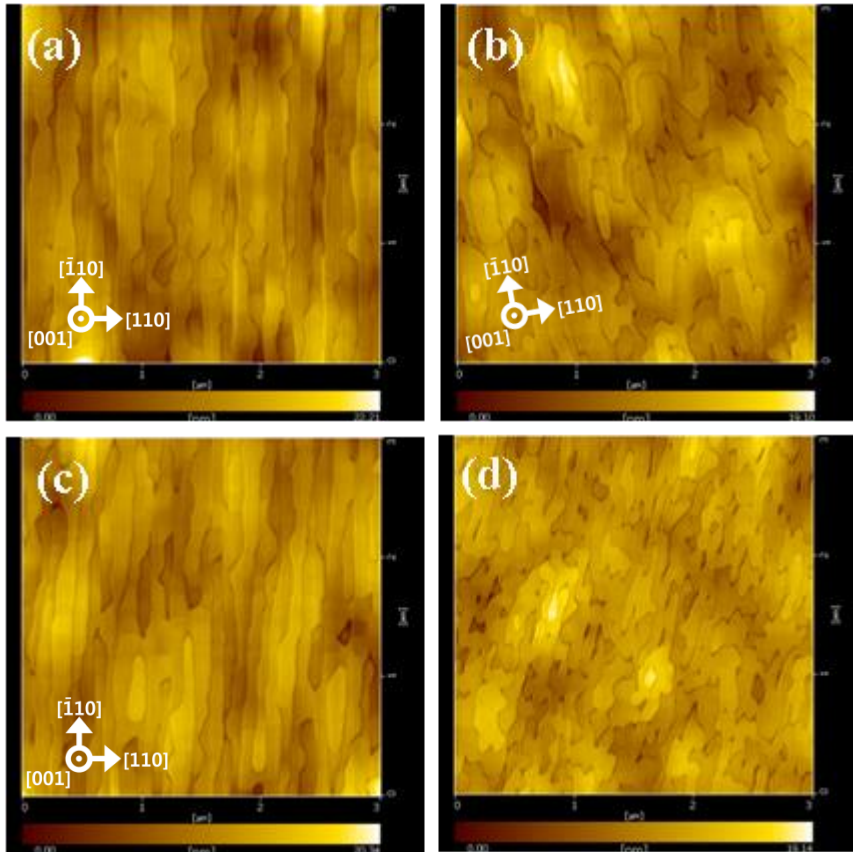


Figure 3-16. AFM images of GaP bulk layers grown at 700 °C with different V/III ratio (a) 500 (b) 250, (c) 100 respectively. Sample (d) is grown at sample temperature with V/III =100 and 2 times growth rate than that of sample (c). LT-GaP nucleation layers of all samples are grown at 400 °C and have 3nm-thickness. RMS roughness is (a) 3.5nm, (b) 2.7nm, (c) 2.5nm, (d) 2.1nm respectively.

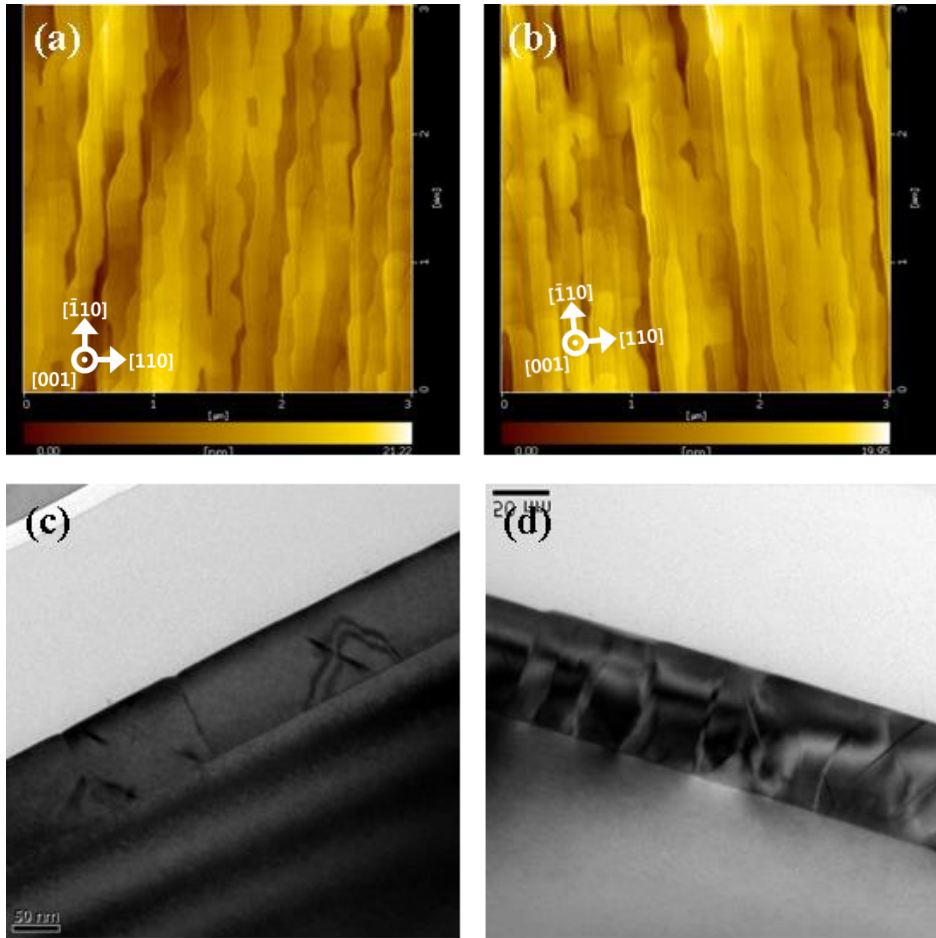


Figure 3-17. GaP bulk layers grown at 700°C on GaP nucleation layers grown at 400 °C having 3nm-thickness after annealed at at 830 °C for 30min in 100 mbar reactor pressure using different growth mode.

3.4. Summary

High quality GaP growth on exact (001) Si substrates is an important prerequisite for integrating III/V-based device layers with Si-based nanoelectronics. The present chapter summarizes a multi-step MOCVD process to achieve such high quality GaP/Si (001) template substrates after the growth of only 100nm Ga layer thickness.

We have investigated the generation process of low defects in GaP layers grown on Si substrates by FME. It was found that the APBs could be annihilated during the growth, and there were optimized growth condition as growth temperature, V/III ratio and growth rate. RMS roughness is 2.8 nm from the optimized growth conditions. Moreover, it was clarified that a few stacking faults and threading dislocations were detected during the lattice relaxation process in the MOCVD grown GaP/Si. It is considered that the generation of stacking faults in the MOCVD growth would be attributed to the coalescence or expansion of isolated islands at the initial growth stage. The presence of stacking faults would result in the generation of threading dislocations during the lattice relaxation process.

3.5. References

- [1] W.Stolz, F.E.G.Fuimaraes, K.Ploog, *J.Appl.Phys.*63(3) 492 (1988).
- [2] M.Razeghi, M.Defour, R.Blondeau, F.Omnes, P.Maurel, O.Acher, F.Brillouet, J.C. C-Fan, J.Salerno, *Appl.Phys.Lett.* **53**(24) 2389 (1988).
- [3] H.Park,A.W.Fang,S.Kodama,J.E.Bowers,*Opt.Express* **13**(23) 9460 (2005).
- [4] H.Rong, R.Jones, A.Liu,O.Cohen, D.Hak, A.Fang, M.Paniccia, *Nature* **433** 725 (2005).
- [5] L.Pavesi, L.DalNegro, C.Mazzoleni, G.Franzo, F.Priolo, *Nature* **408** 440 (2000).
- [6] G.Fanzo, F.Priolo,S.Coffa,A.Polman,A.Carnera, *Appl.Phys.Lett.***64**(17) 2235 (1994).
- [7] H.Krömer, *J.Cryst.Growth* **81** 193 (1987).
- [8] D.E. Aspnes, J. Ihm, *Phys. Rev. Lett.*, **57** (1986), p. 3054
- [9] M. Dürr, U. Höfer, *Surf. Sci. rep.*, **61** (2006), p. 465
- [10] O.L.Alerhand, A.N.Berker, J.D.Joanopoulos, D.Vanderbilt, R.J.Hamers, J.E. Demuth, *Phys.Rev.Lett.***64**(1990)2406.

- [11] A.J. Hoven, J.M. Lenssinck, D. Dijkkamp, E.J. van Loenen, J. Dieleman, *Phys. Rev. Lett.* **63** (1989) 1830.
- [12] B.S. Swartzentruber, Y.W. Mo, R. Kariotis, M.G. Legally, M.B. Webb, *Phys. Rev. Lett.* **65** (1990) 1913.
- [13] Y. Takagi, H. Yonezu, K. Samonji, T. Tsuji, N. Ohshima, *J. Cryst. Growth* **187** (1998)
- [14] T. Grassman, et al., *Appl. Phys. Lett.* **94** (2009) 232106
- [15] T. E. Crumbaker, M. J. Hafich, G. Y. Robinson, K. M. Jones, M. M. Al-Jassim, A. Davis and J. P. Lorenzo, *Appl. Phys. Lett.* **59** (1991) 1090

Chapter 4

Heteroepitaxial InP growth on Si (001) and Ge (001) substrates

4.1. Introduction

InGaAs-based compound semiconductors are promising materials for the high performance electronic devices due to their high electron mobility. The integration of InGaAs quantum well field effect transistors (QWFET) onto Si substrate is advantageous in that high speed device can be connected to well-established Si CMOS platform. Furthermore, the availability of cheap and large wafer is another merit of Si wafer. However, InGaAs growth on Si causes the generation of defects from the interface due to the lattice mismatch between epitaxial layer and substrate materials. Until now, most efforts to reduce defects in InGaAs layer has been focused on using compositional graded buffer layer.[1, 2] In the fabrication of InGaAs transistor, InGaAs with high In content is desirable because electron mobility increases as the In content increases in InGaAs. InP has lattice constant of 0.357 nm which is matched with In_{0.53}Ga_{0.47}As. Thus, InP can be used as a buffer layer for the growth of InGaAs with high In contents on Si substrate. However, lattice mismatch of 8% makes it difficult to grow high quality InP layer on Si. Two-decade ago, planar InP layer growth on Si was achieved by using two-step method for the solar cell applications.[3-5] Moreover, GaAs or GaP intermediate layers were inserted between InP and

Si to improve crystal quality of InP.[6- 8] It is proposed that stress due to thermal expansion coefficient between InP and Si was relieved by inserting such intermediate layers. Recent study of InP growth on Si has been focused on selective area growth (SAG).[9-10] During SAG, defects are confined in the trench, resulting in defect-free InP in the top region. However, 3-dimensional growth within trench requires post planarization process such as chemical-mechanical polishing.

Ge also can be used as a substrate for the InP growth. The main advantage of Ge is less thermal and lattice mismatch with InP compared to Si. Ge has a higher mobility rather than other semiconductor materials. The growth of III-V on Ge allows to fabricate complementary metal-oxide-semiconductor (CMOS) composed of Ge pMOS and III-V nMOS.[11] In addition, thermal annealing at lower temperature is possible to remove native oxide compared to Si, reducing thermal budget.[12-13] Despite merits of Ge as a substrate, InP on Ge has been barely reported. There were a few reports about solar cell operation using InP on Ge but growth of InP on Ge has not been announced.[14]

In this study, InP layers were grown on Si(001) and Ge(001) substrates by using metalorganic chemical vapor deposition (MOCVD). Two-step InP growth on Si(001) was optimized by controlling growth conditions such as

growth temperature, V/III ratio and thickness. The quality of InP layer was improved by growing on Ge(001) substrate. SiO₂ is the most widely used dielectric material and it has been often used for contact windows.

4.2. Experimental details

InP layers were grown on 2-inch Si(001) and Ge(001) substrates in metalorganic chemical vapor deposition (MOCVD). Trimethylindium (TMIn) and phosphine (PH₃) were used as In and P sources, respectively. During the growth, reactor pressure was set to 76 torr. The orientations of Si substrates were (001) and (001) 6° offcut toward <111>. Si wafers were cleaned by using SC1 (NH₄OH : H₂O₂ : DI = 1 : 1 : 10) and HF. Subsequently, wafers were loaded into MOCVD reactor. Before epitaxy, Si wafers were thermally cleaned at 830 °C for 30 min under H₂ ambient. Then, InP nucleation layer was grown at the low temperature of 350-450 °C, at V/III ratio of 1500. Two-step InP growth was proceeded as follows: InP nucleation layers of 40 nm were grown at 400 °C. Subsequently, InP main layers were grown on the top of InP nucleation layers at the elevated temperature from 550 to 650 °C at V/III ratio of 300 and 900. The total thicknesses of two-step InP layers were 0.7, 1.3 and 2.7 μm.

For the InP growth on Ge, 2-inch Ge(001) wafer 60 offcut toward <111> was used. Without any ex-situ treatments, Ge wafer was loaded into MOCVD reactor. In-situ thermal cleaning was performed at 700 °C for 10 min under H₂ ambient. 1.3 μm-thick InP layer was grown on Ge(001) in a two-step: 40 nm-thick InP nucleation layer was grown at 400 °C, followed by InP main layer growth at 550 °C. V/III ratios for nucleation and main layers were 1500 and 300, respectively.

Surface morphologies of InP layers on Si(001) and Ge(001) substrates were characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM) using a Hitachi SU70. Crystallinity of the InP layers was investigated by X-ray diffraction (XRD) using a Panalytical X'pert PRO high resolution XRD system. Optical properties of the InP layers were examined at 80 K by cathodoluminescence (CL) with Gatan MonoCL4. Defects in InP layers were analyzed by JEM-2100F transmission electron microscopy (TEM) .

4.3. Results and Discussion

4.3.1. Heteroepitaxial InP growth on Si(001) and Ge(001) substrates

In order to optimize the growth condition for InP nucleation layer, InP layers were grown on vicinal Si(001) at the temperature of 400 to 450 °C for 10 min. Fig. 1(a) and (b) are 1 x 1 μm^2 AFM images of grown InP layers on vicinal Si(001) at 450 and 400 °C, respectively. When grown at 450 °C, InP islands are formed on the vicinal Si(001) surface as shown in Fig. 1(a). The nucleation rate of InP islands on Si surface increases and the adatoms mobility on surface decreases with growth temperature decreasing. Whole vicinal Si(001) surface was covered by InP layer of 40 nm by decreasing temperature to 400 °C in Fig. 1(b). However, it is suggested that InP growth at more reduced temperature of 350 °C leads to formation of In-rich phase due to the low cracking ratio of PH_3 . [4]

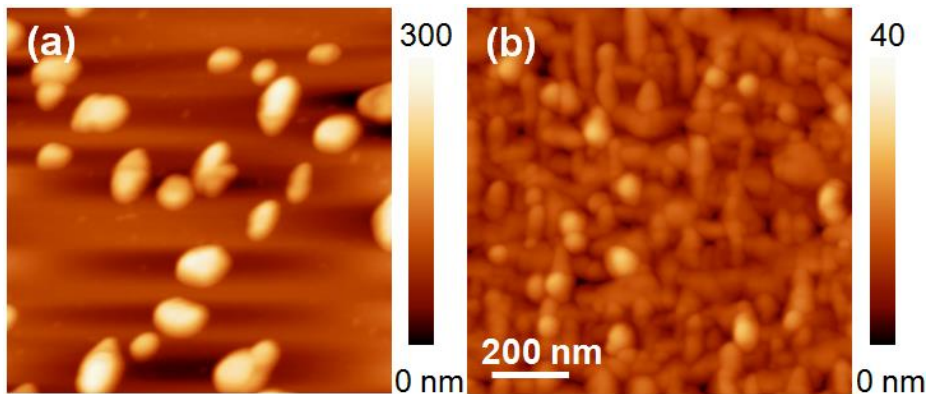


Figure 4-1 $1 \times 1 \mu\text{m}^2$ AFM images of InP layers grown on vicinal Si(001) at (a) 450 and (b) 400 °C for 10 min.

After the growth of InP nucleation layer at 400 °C, main InP layers were grown on InP nucleation layers for 60 min at V/III ratio of 300, varying the temperature from 550 to 650 °C. Figure 2 includes the plan-view SEM images of two-step InP layers with different growth temperatures of main layer. For all growth temperatures, smooth surfaces are not observed. While the 650 °C growth results in the 3-dimensional growth with hillocks, InP layer is partially coalesced with holes on surface by lowering temperature to 600 °C. Further reduction of growth temperature to 550 °C decreases depth of holes and increases their density as shown in Fig. 2(c). The surface RMS roughness is reduced from 68.0 to 32.5 nm by decreasing temperature of second layer from 600 to 550 °C in the inset of Fig. 2(b) and (c), meaning

that 550 °C growth is desirable to obtain flat InP surface. Thus, we selected 550 °C as a growth temperature for InP main layer.

In order to grow InP layer with the smoother surface, and thickness of total InP layers and V/III ratio for growth of InP main layer were varied. The RMS roughnesses and full width at half maximum (FWHM) of XRD rocking curve are plotted depending on growth conditions in Fig. 4. It is clearly shown that as the thickness increases from 0.7 to 2.6 μm , RMS roughness is lowered from 32.5 to 7.7 nm.

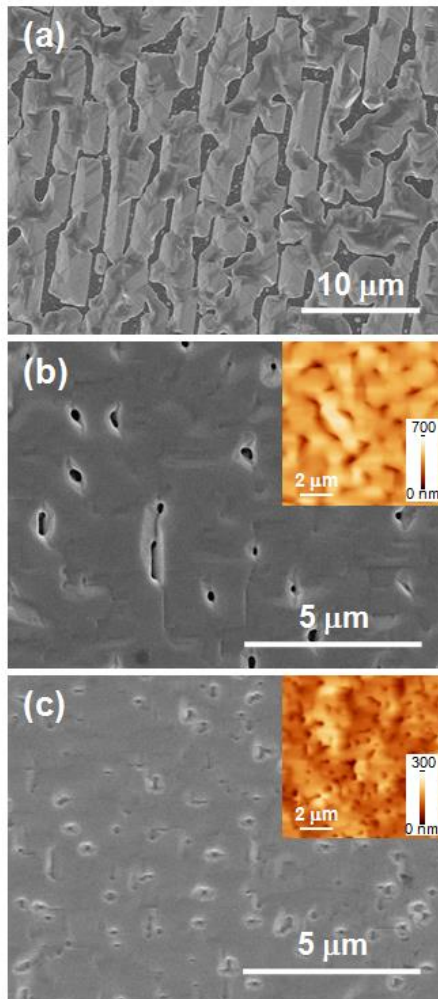


Figure 4-2 Plan-view SEM images of two-step InP layer grown on vicinal Si(001). The growth temperatures of second layer were (a) 650, (b) 600 and (c) 550 °C. The insets of (b) and (c) are AFM images of corresponding samples. The RMS roughnesses of (b) and (c) are 68.0 and 32.5 nm, respectively.

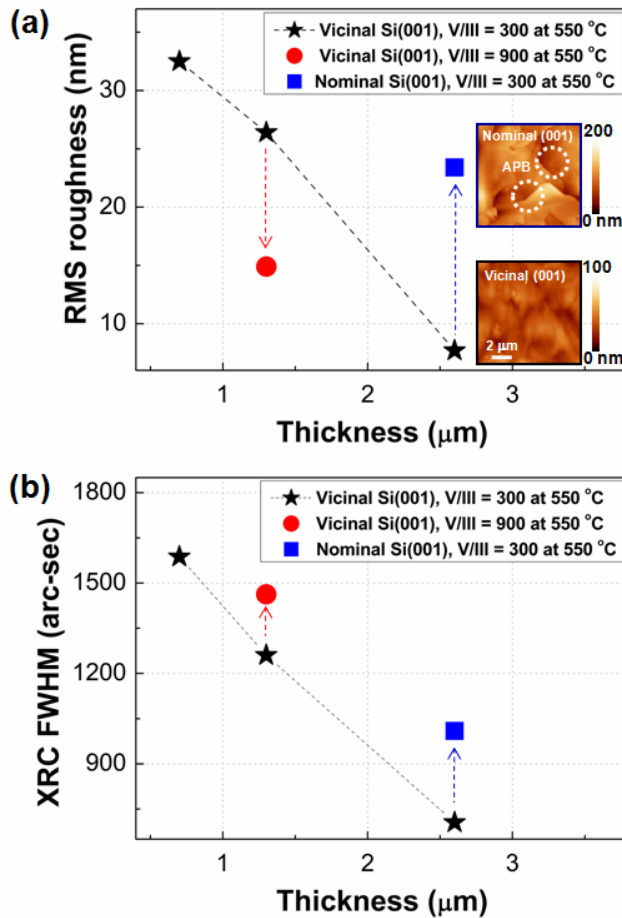


Figure 4-3 (a) Plots of RMS roughness and (b) XRC FWHM of InP layers depending on growth conditions. The insets of (a) are 10 x 10 μm^2 AFM images of InP layers of 2.6 μm grown on nominal and vicinal Si(001) with the RMS roughnesses of 23.4 and 7.7 nm, respectively.

The holes existed on InP surface in Fig. 2(c) are disappeared during 2.6 μm -thick InP growth, flattening InP surface as presented in the inset of Fig. 3(a). In addition to thickness increasing, growth of InP main at higher V/III ratio also improve surface of InP. The increasing V/III ratio from 300 to 900 reduces RMS roughness of 1.3 μm -thick InP from 26.4 to 14.9 nm. Higher V/III ratio reduces diffusion and desorption of In on the facet plane of islands, leading to more lateral growth.[18] Thus, smoother surface can be obtained at higher V/III ratio. Furthermore, when 2.6 μm -thick InP is grown on nominal Si(001), some boundaries are observed. On the surface of nominal Si(001), there are single steps.[15] When polar materials such as InP are epitaxially grown on non-polar materials such as Si, In-In and P-P bonds are generated from the Si surface due to the monolayer steps and they are called anti-phase boundaries (APBs). Such APB is boundary between two different domains and is propagates toward surface during III-V growth.[16] The formation of APBs leads to the rough surface with RMS roughness of 23.4 nm. The smoother InP layer on vicinal Si(001) than that on nominal Si(001) is caused by avoiding APB formations by using a substrate with the higher density of double steps.[17]

Growth conditions affect not only surface morphologies but crystal quality. XRC FWHM decreases from 1587 to 705 arc-sec with thickness increasing

from 0.7 to 2.6 μm as presented in Figure 3(b). In rocking curve, degree of peak broadening is related to the crystal quality. The rocking curve is more broadened when dislocation density is higher in epitaxially grown layer due to the rotation of lattice and strain field by dislocations.[19] Threading dislocation density (TDD) in InP layer is reduced as the thickness increases due to the reaction and annihilation of threading dislocations during growth.[20]

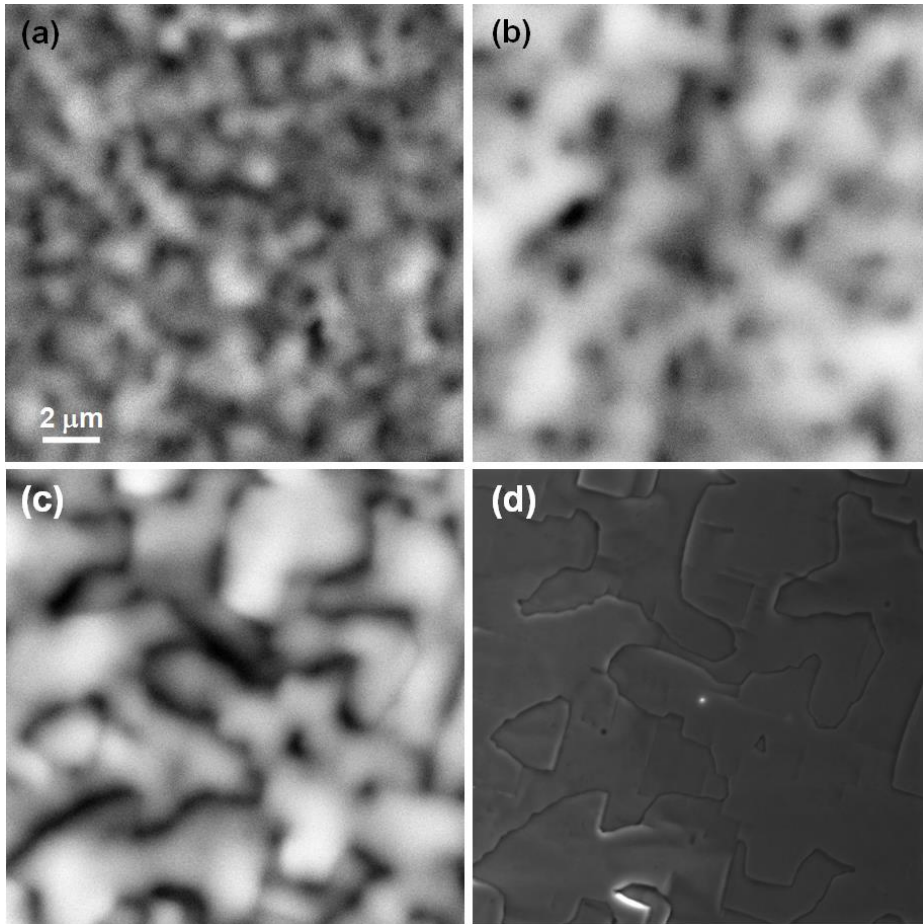


Figure 4-4 CL images of InP layers on (a), (b) vicinal and (c) nominal Si(001) substrates at 80 k. The thickness of InP layers are (a) 1.3 and (b), (c) 2.6 μm . (d) Plan-view SEM image corresponding to (c).

The improved crystal quality influences optical properties of InP layers. Figure 4(a) and (b) present the 80 k CL images of 1.3 and 2.6 μm -thick InP layers vicinal Si(001) substrates. In CL images, non-radiative centers are

represented by dark spots. Dark regions are reduced as the thickness increases from 1.3 to 2.6 μm in Fig 4(a) and (b), indicating the enhanced optical properties. Although the growth of main InP layer at V/III ratio of 900 is advantageous in obtaining the smoother surface, shortened diffusion length of adatom leads to the broadened rocking curve with FWHM of 1463 arc-sec. In addition, InP on vicinal Si(001) shows lower FWHM than that of InP on nominal Si(001). APB is known to be a non-radiative recombination center.[21] Figure 4(c) and (d) shows that dark lines in CL image are matched to the APBs in SEM image, meaning that APBs deteriorate the crystallinity and the optical property of InP layer on nominal Si(001). In brief, the better quality with the smoother surface is obtained by growing the thicker main InP layer on vicinal Si(001) at the lower V/III ratio.

Finally, InP layer of 1.3 μm was grown on vicinal Ge(001) substrate and its material properties were compared with InP layer on vicinal Si(001). The lattice mismatch between InP and Ge is 4% which is smaller than that between InP and Si (8%). Thus, quality improved InP layer was grown on Ge(001).

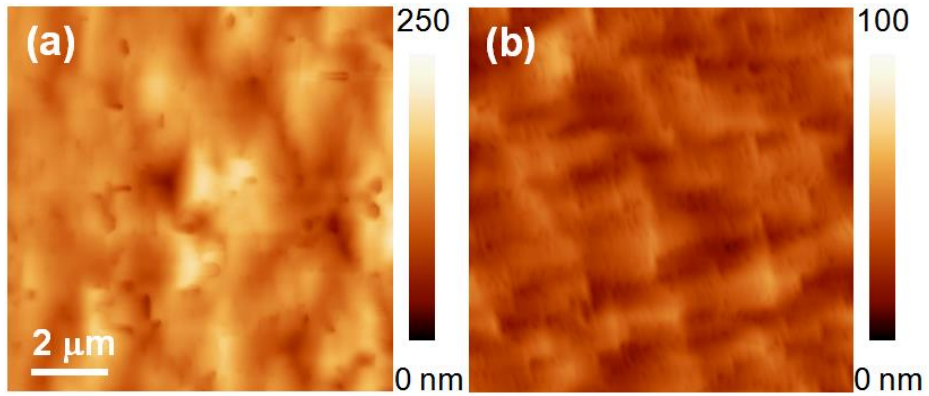


Figure 5-5 $10 \times 10 \mu\text{m}^2$ AFM images of $1.3 \mu\text{m}$ -thick InP layer grown on vicinal (a) Si(001) and (b) Ge(001) substrates. RMS roughnesses are (a) 26.4 and (b) 7.8 nm

Figure 5 includes $10 \times 10 \mu\text{m}^2$ AFM images of $1.3 \mu\text{m}$ -thick InP layers grown on both substrates. In the case of InP on Si(001), holes exist on the surface and high RMS roughness of 26.4 nm is obtained. As shown in Fig. 3(a), merged surface with lower RMS roughness of 7.7 nm is achieved by growing $2.6 \mu\text{m}$ -thick layer. However, growth of $1.3 \mu\text{m}$ -thick InP results in merged surface with RMS roughness of 7.8 nm by replacing Si(001) substrate with Ge(001) substrate.

The usage of Ge(001) substrate affects the defect formation in InP layer. Figure 6(a)-(c) shows the plan-view TEM images of InP layers grown on vicinal Si(001) and Ge(001) substrates. For all cases, defects are formed on

the InP surface because of lattice mismatch between InP and substrate materials. Threading dislocation and planar defect densities are plotted in Fig. 6(e). When InP layers are grown on Si(001) substrates, TDD is reduced from 6.5 to $4.0 \times 10^8 \text{ cm}^{-2}$ as the thickness increases from 1.3 to 2.6 μm , respectively as shown in Fig. 6(a) and (b).

The TDD reduction is due to the annihilation during InP growth. In addition to threading dislocations, planar defects are observed. The formation of planar defects such as stacking fault and/or twin boundary is due to the adsorption of atoms on {111} planes.[ref] The planar defect density also decreases from $8.2 \times 10^3 \text{ cm}^{-2}$ to $5.5 \times 10^3 \text{ cm}^{-1}$ by with thickness increasing. Although lattice mismatch between InP and Ge is less than that between InP and Si, more threading dislocations are observed in 1.3 μm -thick InP on Ge(001) in Fig. 6(c). The TDD of InP is $1.1 \times 10^9 \text{ cm}^{-2}$ which is higher value than both InP layers grown on vicinal Si(001). However, less planar defects exist with the density of $1.2 \times 10^3 \text{ cm}^{-1}$ compared to InP on Si(001). Planar defects act as barriers which block the propagation of threading dislocations. Thus, TDD is higher in InP on Ge(001) rather than InP on Si(001). The origin of less planar defects is not clear.

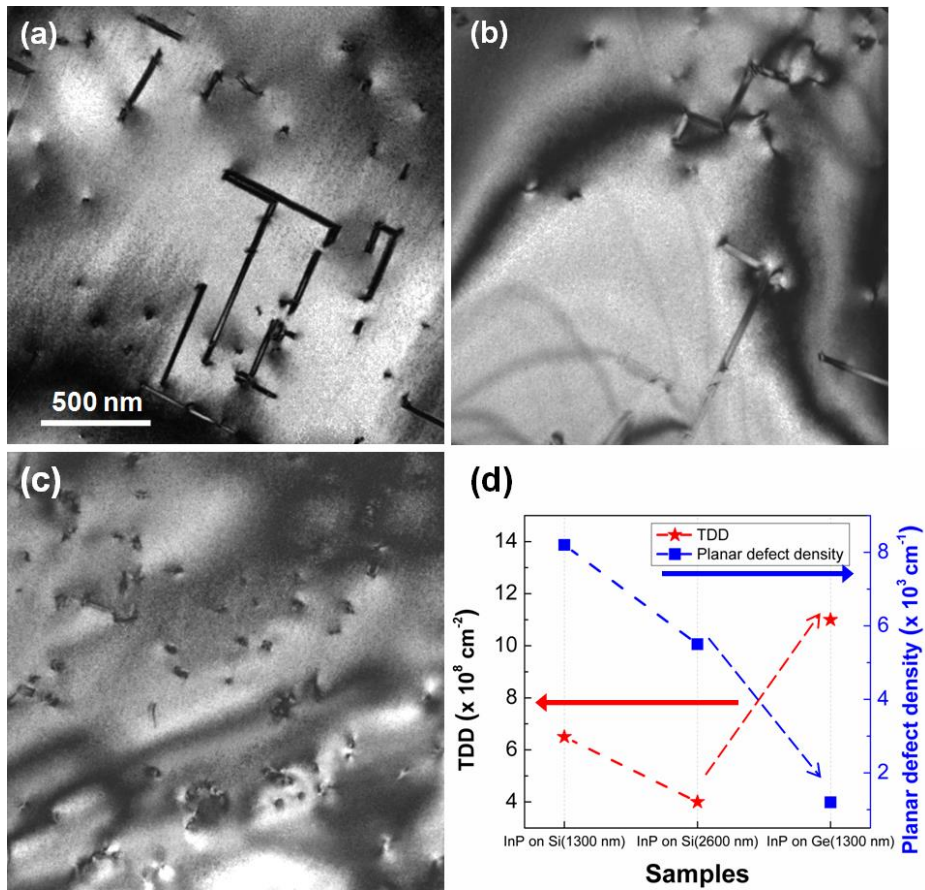


Figure4-6 Plan-view TEM images of InP layer grown on vicinal (a), (b) Si(001) and (c) Ge(001) substrates. Thicknesses of InP layers are (a), (c) 1.3 and (b) 2.6 μm . (d) the plot of TDD and planar defect density of InP layer grown on vicinal Si(001) and Ge(001) substrates.

In spite of the higher TDD, InP on Ge(001) shows better crystal quality. Figure 6 shows the rocking curves of InP layer grown on vicinal Si(001) and

Ge(001) substrates. When 1.3 μm -thick InP is grown, the narrower rocking curve is obtained with the FWHM of 781 arc-sec by using Ge(001) substrate, which is the slightly higher values than that of 2.6 μm -thick InP on Si(001). The lattice mismatch between InP and Ge is 4% which is smaller than that between InP and Si (8%), leading to the lower TDD in InP layer. Therefore, crystal quality is enhanced by growing InP layer on Ge(001) substrate.

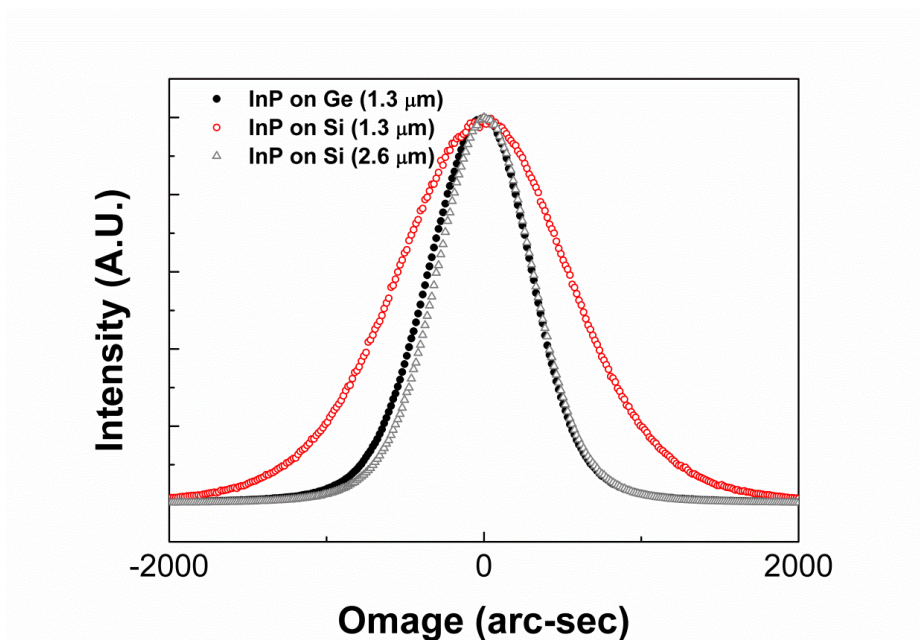


Figure 4-7 XRD rocking curves of InP layers grown on vicinal Si(001) and Ge(001) substrates.

4.3.2. Optimization of InP growth on Si using GaP buffer

InP epilayers grown on Si substrates provide a promising way to combine InP-based optical devices with Si integrated circuits, using high-quality commercial Si substrates. This section reports InP epilayers grown on Si substrates with GaP as buffer layers. This GaP buffer layers was adopted from the best optimized condition of previous chapter. InP epilayers are then grown on those GaP buffer layers using a conventional two-step growth method. Total optimized GaP buffer layer thickness is around 50nm, which grown at 700°C for HT GaP bulk layers and at 400°C for nucleation layers with 5nm thickness. 1st InP buffer layers were grown on those GaP buffer layers using two step growth, 400°C and 550°C growth temperature for LT InP and HT InP respectively. 2nm-thick InGaAs having over 50% In composition and InP superlattice layers were grown on 1st InP buffer layers.

Figure 4-8 shows AFM images of InP top layers from (a) to (c) and bright field ($g=(001)$) cross-sectional TEM micrograph are from (d) to (f) with different growth condition and buffer structure. All samples have the same GaP buffer growth conditions and RMS roughness is (a) 9.4nm, (b) 5.5nm, (c) 2.1nm respectively. (a) Thick 1st InP buffer layers and InGaAs/thin InP superlattice layers on 4° miscut Si substrate, (b) thin 1st InP

buffer layers and InGaAs/thick InP superlattice layers on exact Si substrate and (c) thin 1st InP buffer layers and InGaAs/thick InP superlattice layers on 4° miscut Si substrate. We obtained high quality InP top layers with very smooth surface using 2nm-thick InGaAs and 80nm-thick InP superlattice buffer. Most threading dislocations from the interface between InP and GaP, GaP and Si substrates are self-annihilated within lower InGaAs/InP superlattice buffer.

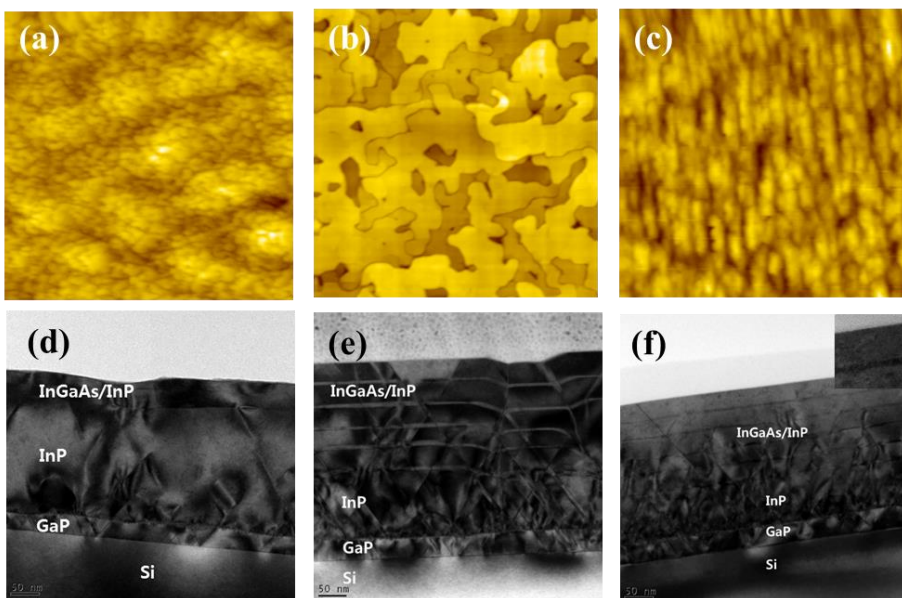


Figure 4-8. AFM images of InP top layers from (a) to (c) and bright field ($g=(001)$) cross-sectional TEM micrograph are from (d) to (f) with different growth condition and buffer structure. All samples have the same GaP buffer growth conditions and RMS roughness is (a) 9.4nm, (b) 5.5nm, (c) 2.1nm

respectively.

4.4. Summary

InP epilayers were grown on Si substrates using buffer layers of GaP. AFM, SEM and TEM examination results showed that GaP is a proper material as a buffer layer, and that its optimum thickness is about 3~5nm. TEM observation showed that the inserted InGaAs strained layers were very helpful to reduce the surface roughness and defect reduction. It also confirmed that GaP acted as a buffer to alleviate the lattice mismatch between InP and Si. The best AFM roughness obtained from inserted InGaAs strained layers was 2.1nm for $5 \times 5 \mu\text{m}^2$.

4.5. References

- [1] M. K. Hudait, G. Dewey, S. Datta, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit and R. Chau, IEEE IEDM 625 (2007).
- [2] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah and R. Chau, IEEE IEDM 319 (2009).
- [3] M. K. Lee, D. S. Wu and H. H. Tung, Appl. Phys. Lett. 50(24), 1725 (1987).
- [4] A. Yamamoto, N. Uchida and M. Yamaguchi, J. Cryst. Growth 96, 369 (1989).
- [5] G. -P. Tang, A. Lubnow, H. -H. Wehmann, G. Zwinge and A. Schlachetzki, Jpn. J. Appl. Phys. 31, L1126 (1992).
- [6] A. Seki, F. Konushi, J. Kudo, S. Kakimoto, T. Fukushima and M. Koba, Jpn. J. Appl. Phys. 26, L1587 (1987)
- [7] Y. Kohama, Y. Kadota and Y. Ohmachi, Jpn. J. Appl. Phys. 28, 1337 (1989).
- [8] M. Sugo, Y. Takanashi, M. M. Al-jassim and M. Yamaguchi, J. Appl Phys. 68(2), 540 (1990).
- [9] G. Wang, M. R. Leys, N. D. Nguyen, R. Loo, G. Brammertz, O. Richard,

- H. Bender, J. Dekoster, M. Meuris, M. M. Heyns and M. Caymax J. Electrochem. Soc. 157(11), H1023 (2010).
- [10] G. Wang, M. R. Leys, N. D. Nguyen, R. Loo, G. Brammertz, O. Richard, H. Bender, J. Dekoster, M. Meuris, M. M. Heyns and M. Caymax, J. Cryst. Growth 315,32(2011).
- [11] B. Brammertz, M. Caymax, M. Meuris, M. Heyns, Y. Mols, S. Degroote and M. Leys, Thin Solid Films 517, 148 (2008).
- [12] J. Oh and J. C. Campbell, J. Electronic. Mater. 33, 364 (2004).
- [13] T. Yamazaki, N. Miyata, T. Aoyama and T. Ito, J. Electrochem. Soc. 139(4), 1175 (1992).
- [14] S. Wojtczuk, S. Vemon and E. Burke, XIII NASA Spaec Photovoltaic Res. And Tech. Conf. (1994).
- [15] D. J. Chadi, Phys. Rev. Lett. 59, 1691 (1987)
- [16] Polar on non polar
- [17] M. E. Ware, R. J. Nemanich, J. L. Gray and R. Hull, J. Appl. Phys. 95, 115 (2004).
- [18] H. Heinecke, A. Milde, B. Baur and R. Matz, Semicond. Sci. Technol. 8, 1023 (1993).
- [19] J. E. Ayers, J. Cryst. Growth 135, 71 (1994).
- [20] A.E. Romanov, W. Pompe, G. E. Beltz and J. S. Speck, Appl. Phys. Lett.

29(22), 3342 (1996).

[21] C. Yang, S. Lee, K. -W. Shin, S. Oh, D. Moon, S. -D. Kim, Y. -W. Kim, C. -Z. Kim, W. -k. Park, W. J. Choi, J. Park and E. Yoon, J. Cryst. Growth 370, 168 (2013).

Chapter 5

**SAG of high quality InP on Si substrate
using a GaP thin buffer layer**

5.1. Introduction

Among III–V compound semiconductors, indium phosphide (InP) has attracted much interest for various applications including high speed optoelectronics for optical communications [1]. In order to satisfy the requirements to be used in InP-based optoelectronic devices as well as low power logic devices with high performance, the high quality epitaxial growth of InP on Si substrates is essentially necessary. Although many research groups have made their efforts to obtain high quality InP for many decades, several problems still remain unresolved due to the considerable lattice constant mismatch (~8%), a large difference in thermal expansion coefficient (~50%) and the generation of polar/non-polar interfaces between InP and Si substrate [2,3]. These challenges are being addressed by the use of III-V buffer layer growth, either on blanket Si wafers [4,5] or on patterned Si wafers [6], which reduces the number of defects degrading the device performances. To reduce the number of defects in InP layers grown on Si substrate, many growth techniques such as selective area growth (SAG) [7], epitaxial lateral overgrowth [8], strain engineering by buffer layer [9], and migration enhanced epitaxy (MEE) [10], etc., were explored. Among them, SAG is the most widely used to form III-V compound semiconductor

heterostructures on Si substrate with shallow trench isolation (STI) structures [6,11].

In the case of III-V compound semiconductor epitaxial layers grown on Si (001) substrates, the reduced symmetry of III-V compounds induces antiphase domain boundaries (APBs), resulting in deep-levels in the band gap [6.12]. To avoid the formation of APBs, miscut Si (001) substrates are commonly used. However, miscut substrates induce additional issues in SAG, such as crystal quality and surface morphology dependence on trench orientations, which can be a significant barrier for CMOS device fabrication using III-V materials [13]. Therefore, it is of great importance to obtain APB-free III-V layers on on-axis (001) Si substrates.

In this study, we investigated the growth behaviors of InP layer on (001) Si substrate to obtain high quality InP with atomically smooth surface using SAG with submicron trenches. For the growth of high quality InP layer, a GaP thin buffer layers was used on the stepped sidewall surface of etched Si surface. In terms of InP growth, GaP layers have several advantages such as small lattice mismatch with Si substrate, high band gap energy that would lower leakage current through buffer layers and no interfacial fluctuation by using the same group-V source (P), compared to GaAs buffer layer. APBs could be eliminated from the interface between GaP layers and Si substrates,

and crystallographic defects, such as threading dislocations, stacking faults (SFs) and micro twins could be also trapped within the etched Si surface with necking effects. Finally, we demonstrated the epitaxial growth of InGaAs/InP heterostructure on SAG InP to show its feasibility as a channel layer in field effect transistors (FETs).

5.2. Experimental details

The substrates used in this study were 2-inch p-type on-axis (001) Si. After Si cleaning process, a thin SiN_x layer was deposited on Si substrates by inductively coupled plasma chemical vapor deposition, followed by conventional photolithography and reactive ion etching (RIE) to form trench patterns along [110] direction. After the formation of stripe patterns using RIE with CF_x chemistries, the trenches about 800 nm deep were formed. Then, Si wafers were loaded into a low pressure metal organic chemical vapor deposition (MOCVD) system (AIX 2400 G3), the epitaxial growth was made. For the In, Ga, Al, and P sources, trimethylindium, trimethylgallium, trimethylaluminum, and phosphine were used, respectively. Prior to the growth of epitaxial InP layer on patterned Si substrates, initial experiments were performed by using a two-step growth method following

the optimized growth conditions on planar Si (001) substrates. A typical sequence for growing InP/GaP on Si was conducted as follow; Si substrates are preheated at 830 °C for 30 min in a H₂ atmosphere to remove thin native oxide from the substrate prior to epitaxial growth. The first 5 nm-thick GaP nucleation layer was deposited at 400 °C (low temperature GaP), followed by a 25 nm-thick GaP intermediate layer grown at 700 °C (high temperature GaP). The growth rates for nucleation and intermediate GaP layers were 0.1 Å/s and 3.8 Å/s, respectively. Then, the growth temperature was decreased to 400 °C for the growth of 30 nm-thick InP buffer layer (low temperature InP) and finally 300 nm-thick HT InP layers were grown at various growth temperatures (high temperature InP). It was found that the formation of facet planes and growth rates were affected by growth conditions such as temperature and pressure [14]. The surface morphologies of the high temperature (HT) InP layers grown at various growth temperatures ranging from 500 to 650 °C were characterized by atomic force microscopy (AFM), scanning electron microscopy (SEM). Transmission electron microscopy (TEM) was used with 300 keV acceleration voltage to study details of defects.

5.3. Results and Discussion

5.3.1. Effects on growth temperature on surface morphology

Figure 5-1 shows the low magnification cross-sectional TEM images of InP layers grown on patterned Si substrates at various HT InP growth temperatures from 500 to 650 °C with increment of 50 °C. Figure 1(a) shows the polycrystalline InP layers, suggesting that the relatively too low growth temperature under 550 °C would not be suitable for the growth of single crystalline InP layers. Fig. 5-1(b) shows that the InP layers with flat (001) surfaces and many SFs and micro twins generated from free {111} surfaces inside InP buffer layers. As growth temperature increased over 600 °C, surface morphology of HT InP layers began to have {111} planes near the SiN_x mask (See Fig. 5-1(c)). Finally, the InP layer grown at growth temperatures 650 °C clearly showed the triangular shapes with {111} facets. From the results of morphological dependence on the growth temperature, we found that the growth temperature of HT InP should be near 550 °C to obtain flat surfaces with single crystalline nature. The HT-InP grown at 550 °C has more regular and uniform surface morphology than the case of 525°C as shown in the inset Fig. 5-1(b).

Figure 5-2 shows the cross-sectional SEM and TEM images of InP layer grown at 650 °C. The top HT InP layers were triangularly shaped with {111} facets and high crystallographic quality. TEM image analysis was made, as shown in Fig. 5-2(b), to study the defects in detail. Most defects were trapped within the sidewalls of etched Si surface and the rest of them were trapped underneath the sidewalls of SiN_x mask. These results clearly illustrate that the defects created during the InP growth on Si substrate could be effectively and significantly reduced by a two-step growth method. Furthermore, APBs arising from polar epitaxial growth on nonpolar substrates could be effectively suppressed at the interface between GaP intermediate layers and Si substrates. APBs are known to have harmful effect such as the reduction of mobility of electrons and holes in electronic devices [2].

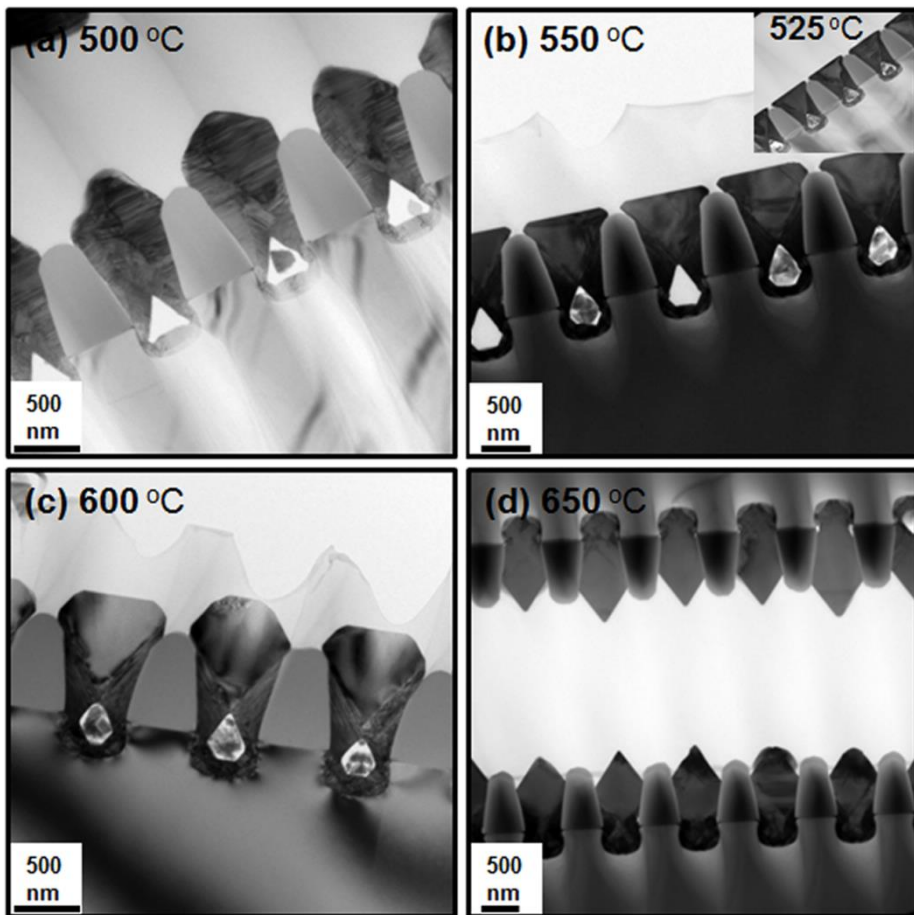


Figure 5-1. Cross-sectional TEM images of InP layers grown on patterned Si (001) substrate at various growth temperatures ranging from (a) 500 °C to (d) 650°C with increment of 50 °C.

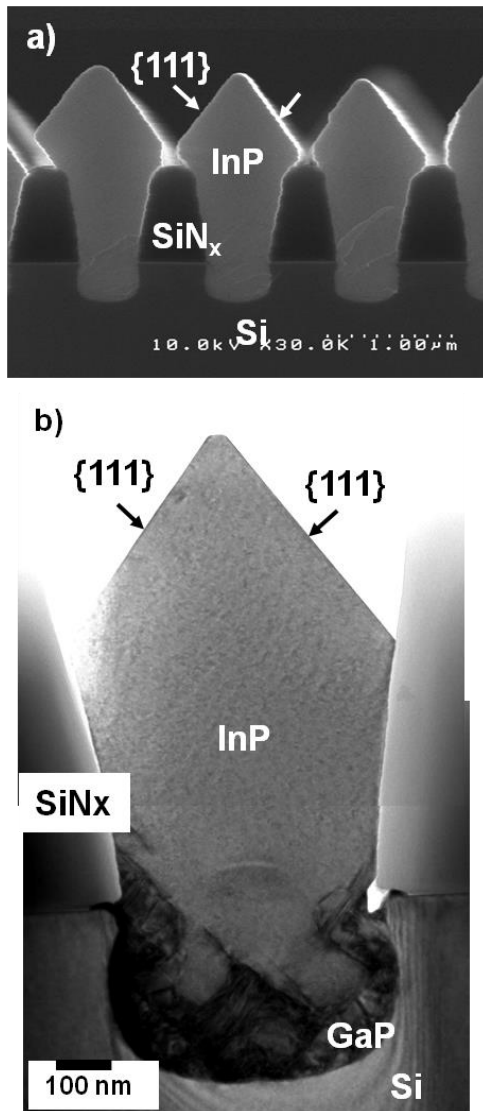


Figure 5-2. Cross-sectional (a) SEM and (b) TEM images of epitaxially grown InP layer on a patterned Si (001) wafer with SiN_x mask. HT InP layer is grown at 650°C.

Moreover, the defects originated from lattice mismatch between InP and GaP intermediate layers were reduced in the LT InP layers grown at 400 °C. The atomic steps formed by over-etching of Si substrates with a rounded surface were effective in reducing the density of APBs [5]. In our work, the over-etched and concave shaped Si trenches were found critical to remove or reduce crystallographic defects including APBs by the formation of InP/GaP buffer layers both at the bottom and at sidewall of etched surface. Conventionally, threading dislocations tend to stretch toward top surface along the growth direction. In our experiment, however, the LT InP layers from the sidewalls merged along $\langle 110 \rangle$ directions and could block the propagation of defects threading upward from the (001) bottom surface during LP InP growth.

Figure 5-3 shows the cross-sectional SEM and TEM images of the InP layer grown at 550 °C on patterned Si substrate with the same trench along the [110] direction as in Fig. 5-2. In contrast to the InP layer grown at 650 °C, top HT InP layers had very flat surfaces. The flat surface morphology can be attributed to the different growth rate according to crystal planes and the different surface diffusion length of precursors according to the growth temperature.

After growth of LT InP layers, the top InP surface has (001) planes on the

center of trench and {311} planes appear at the both edge side of trench as shown in Fig. 5-4(d). Relatively lower surface diffusion of precursors at 550 °C allows similar growth rate for both (001) and {311} planes, so final HT InP top layers has flat (001) surface with negligible {311} planes nearby SiN_x mask. However, in case of HT InP growth temperature of 650 °C as in Fig. 5-2, precursors has the highest surface mobility on {111} planes which means the lowest growth rate on {111} planes so that {111} facets appear during HT InP growth. These results are good agreement with the Si selectively growth according to growth temperature [15]. In our experiment, SiN_x mask layers were used since they were not etched by a dilute HF solution, and mask shape did not change before and after pre-cleaning process. In addition, the SiN_x had shorter surface migration length compared to SiO₂ for some precursors, which facilitated the formation of flat surfaces [16]. The formation of void can be also attributed to the lower growth rate of {111} facets inside void than that of (001) plane of LT InP. The merger of two fast growth (001) planes toward <110> direction prevents the supply of precursors to the bottom of trench area, resulting in the void formation.

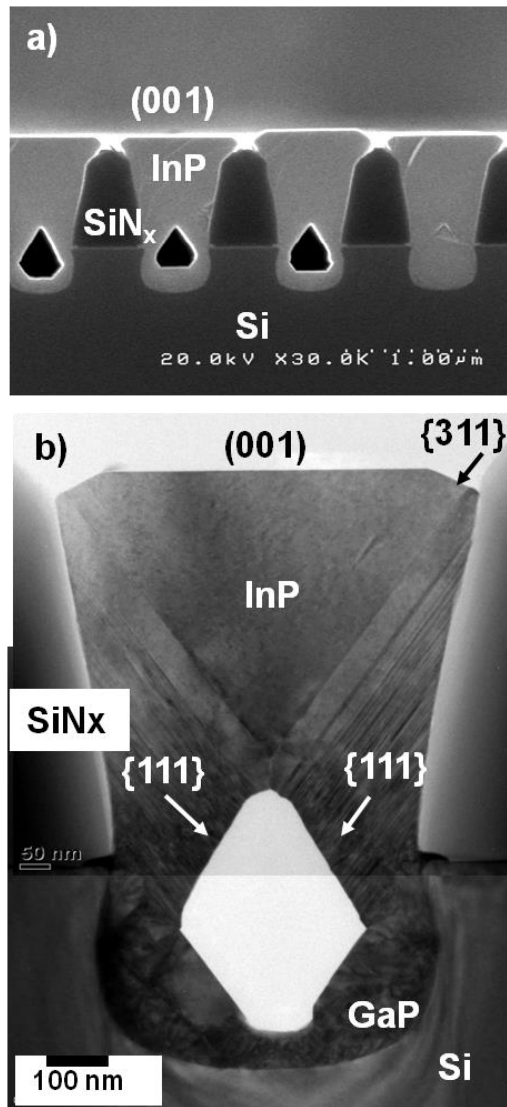


Figure 5-3. Cross-sectional (a) SEM and (b)TEM image of HT InP layer grown on a patterned Si (001) wafer with SiN_x mask. HT InP layer is grown at 550°C .

The details for defects in InP layer could be found in the TEM image as shown in Fig. 5-3(b). Stacking faults and micro twins stretched out to the edge of the top surface along the {111} planes and most threading dislocations were confined at the interface of GaP intermediate and LT InP layers. This result suggests that a defect-free top InP epilayer with smooth surface can be grown at 550 °C. The top InP layers grown at 650 °C were faceted, as shown in Fig. 5-2; however, the reduction of InP growth temperature to 550 °C resulted in the formation of (001) planes with smooth surface morphology.

Figure 5-4 shows the step-by-step morphological evolution of the growth of InP layers on patterned Si substrate with SiN_x mask on Si substrate to the final HT InP growth. The left column indicates the schematic diagram of each growth step with the corresponding cross sectional SEM images in the right column. Fig. 5-4(a) shows the cross sectional image of etched SiN_x masked Si substrate. After then, GaP buffer layers having {111} facets were grown at the bottom of trench, as shown in Fig. 5-4(b). During the LT InP growth, InP layers grew on the initial planes of HT GaP layers with different growth rate of {111} and (001) plane. Sidewall InP islands nearly touched each other at the end of LT InP growth. Further growth of HT InP at 550 °C led to the coalescence of sidewall islands with (001) top plane, as shown in

Fig. 5-4(d) and 4(e), indicating the possibility to obtain relatively smooth surface by the different growth rate and surface diffusion length according to both crystal planes and the growth temperature as mentioned before. It is speculated that the formation of void may affect the residual stress state of overgrown InP layer and can be advantageous in obtaining less defect layers.

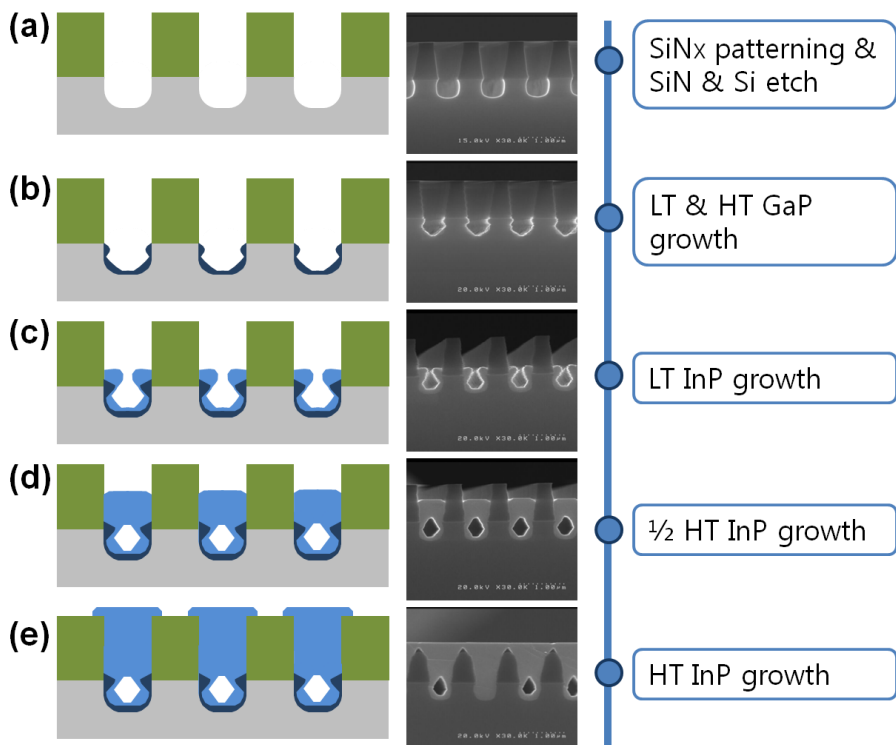


Figure 5-4. Evolution of growth behavior of InP layer from the (a) SiN_x patterning to (e) the HT InP growth.

In order to evaluate the surface roughness, which is an important issue to fabricate electronic devices, AFM measurements were conducted with HT InP layer grown on patterned substrate at 550 °C. As shown in the Fig. 5-5, the top HT InP has a very flat surface with RMS roughness of 2.3 Å. No defects including APDs and mixed dislocations were observed. Dark color lines along the [110] direction exhibits the region of unmerged HT InP layers overgrown on the SiN_x mask. The improvement of surface morphology using the patterned substrate can be attributed to the well-known growth mechanism of SAG method [5].

Finally, the n⁺-InGaAs/InP/InGaAs heterostructure, which is essential for the formation of transistor channel layers in electronic and optoelectronic device applications [17], was grown on the InP layer. The successful formation of the heterostructure on InP with flat surface could be confirmed, as shown in Fig. 5-6. The high surface flatness of InGaAs was achieved by using the HT InP templates grown at optimized growth temperature of 550 °C on patterned Si substrate. However, some stacking faults from the center of HT InP stretched out to the surface through InGaAs channel layers which can affect the final device performance.

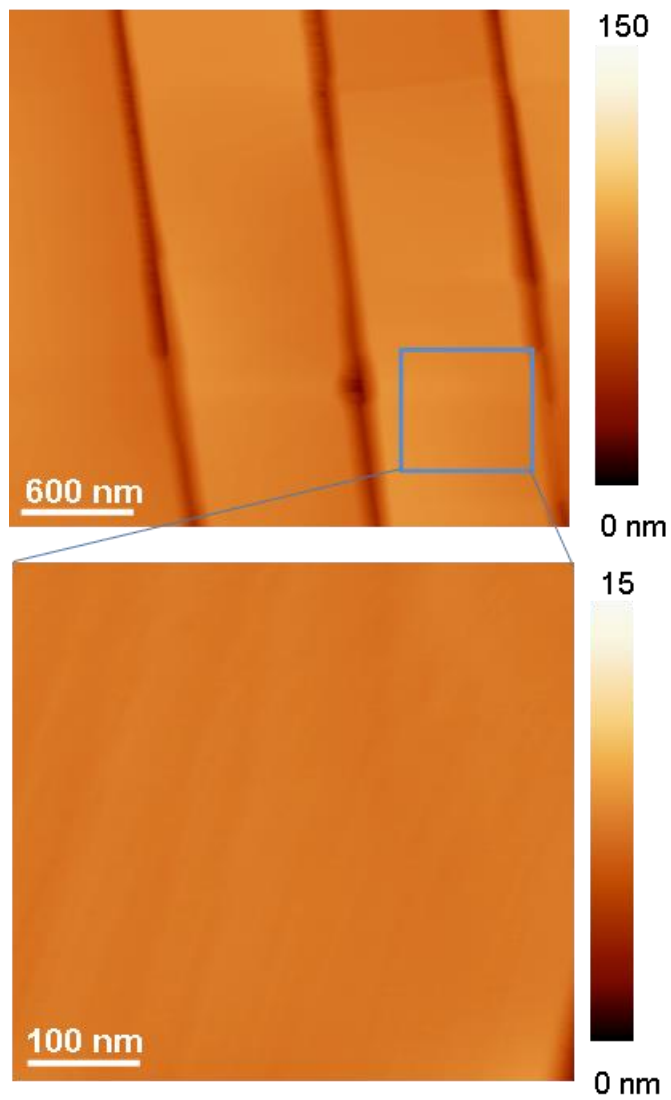


Figure 5-5. AFM images recorded from the surface of HT InP layer grown at 550 °C. The lower figure shows the magnified image of the flat top region.



Figure 5- 6. Cross sectional TEM image of InGaAs grown on HT InP template grown at 550 °C. The inset shows the STEM image of the same structure.

5.3.2. Defect formation mechanisms

There are two fundamentally different mechanisms for formation of extended lattice defects; relaxation of strain and deposition errors. A third case can be said to be constituted by defects formed during coalescence; the exact mechanism for formation of defects is not perfectly clear and may in

fact involve the other two. In all above cases, dislocations are created whereas stacking faults do not necessarily arise in the first and third cases. Furthermore, since defects are present already in the seed layer, those in the ELOG layer may consist both of defects that propagate through the mask openings and of newly formed ones.

5.3.2.1. Relaxation strain

Strain affects both the formation of defects as well as their behavior; after reaching a critical thickness, a strained layer may relax by forming misfit dislocations at the layer substrate interface [18].

Threading 60° misfit dislocations are not as efficient in relieving strain as 90° misfit dislocations lying in the interface of two mismatched lattices. Still, glissile 60° TDs tend to dominate in low-strain systems because they can glide on $\{111\}$ planes to the interface where strain is most efficiently relieved [19]. In the present case however, the gliding movement would be blocked by the mask and thus the dislocations would not be able to reach the interface. Since the SAG layer is assumed to be able to slip across the SiN_x mask because there is no nucleation taking place on top of the mask, it is doubtful if they would contribute much to strain relaxation at the InP SAG– SiN_x mask interface. Thus, relaxation of strain by formation of misfit

dislocations is not likely; instead, in uncoalesced ELOG layers, strain would be relieved predominantly by elastic readjustment. However, TDs pre-existing in the seed layer, predominantly 60° dislocations, may propagate through the mask openings and subsequently dissociate into pairs of Shockley or Shockley and Frank partial dislocations. As previously noted, the TDs corresponding to single dark spots in the PCL maps are likely not partial dislocations since they do not appear to be bounding planar defects. Thus, these TDs were not formed in conjunction with associated planar defects such as SFs. Therefore, the TDs observed in the InP ELOG layer in the present investigation are not the result of relaxation of residual strain, nor are they a result of the formation of stacking faults. Instead, they more likely formed during coalescence of merging growth fronts and to some extent due to propagation of pre-existing TDs through the mask openings.

5.3.2.2. Dissociation of dislocations

A perfect dislocation may dissociate into Shockley partial dislocations bounding an SF according to the reactions of the type:

$$\frac{1}{2} \langle 110 \rangle \rightarrow \frac{1}{6} \langle 211 \rangle + \frac{1}{6} \langle 2\bar{1}\bar{1} \rangle \quad (5.1)$$

Whereas the two dislocations will repel each other, the SF will provide a

force pulling them together, yielding the following expression for total force acting on the partials [20]:

$$F = \frac{Gb^2}{4\pi d} - \gamma \quad (5.2)$$

where G is the shear modulus, b, the magnitude of the Burgers vector, d, the separation between the partial dislocations and γ , the stacking fault energy per area, providing a line force per unit length of dislocation. U, the additional crystal energy per unit length due to the partial dislocations and the SF is then the work performed when the dislocations are moved apart which can be found by integrating the total force over the width w of the fault:

$$\begin{aligned} \int_{a/\sqrt{2}}^w F dr &= \int_{a/\sqrt{2}}^w \left(\gamma - \frac{Gb^2}{4\pi r} \right) dr = \left[\gamma r - \frac{Gb^2}{4\pi} \ln(r) \right]_{a/\sqrt{2}}^w \\ &= \gamma \left(w - \frac{a}{\sqrt{2}} \right) - \frac{Gb^2}{4\pi} \left(\ln(w) - \ln \frac{a}{\sqrt{2}} \right) \end{aligned} \quad (5.3)$$

where d in (5.2) has been substituted by r to avoid confusion with the integrand. The lower boundary is $a/\sqrt{2}$ since this is the least distance between adjacent atoms on {111} planes in the $\langle 110 \rangle$ directions.

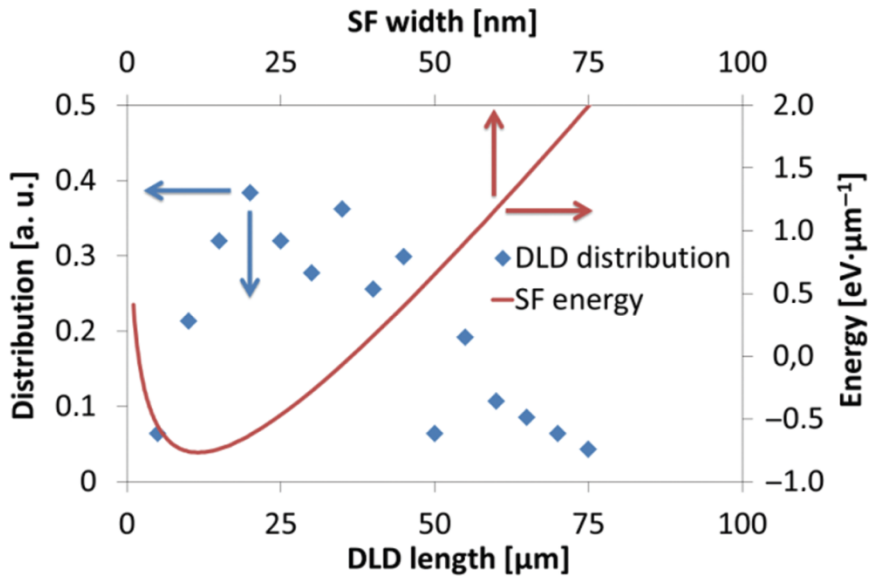


Figure 5-7. Normalized distribution of DLDs with respect to DLD width extracted from sample K with layer thickness of $100\mu\text{m}$. The crystal energy/unit length of SF with respect to SF width is included for comparison. The arrows indicate on which scale the data is plotted on [21].

The length of the DLDs was extracted from room temperature PCL maps for samples of InP SAG on Si substrate and is shown in Figures 5-7 and 5-8. As has been previously observed, the SF width is not constant but increases with layer thickness. The reason for this is not quite clear but is probably a consequence of the growth mechanism rather than force equilibrium as it is determined by the directions of the bounding partials [22]. The distribution function of these, i.e., the frequency with which certain lengths occurs,

appears to be neither random nor monotonically decreasing with increasing length; distribution sharply increases and then decays exponentially with increasing length, having a maximum towards lower lengths. The average length was around 3 μm in the case of sample with a layer thickness of 10 μm , and around 30 μm for sample with a layer thickness of 100 μm , respectively.

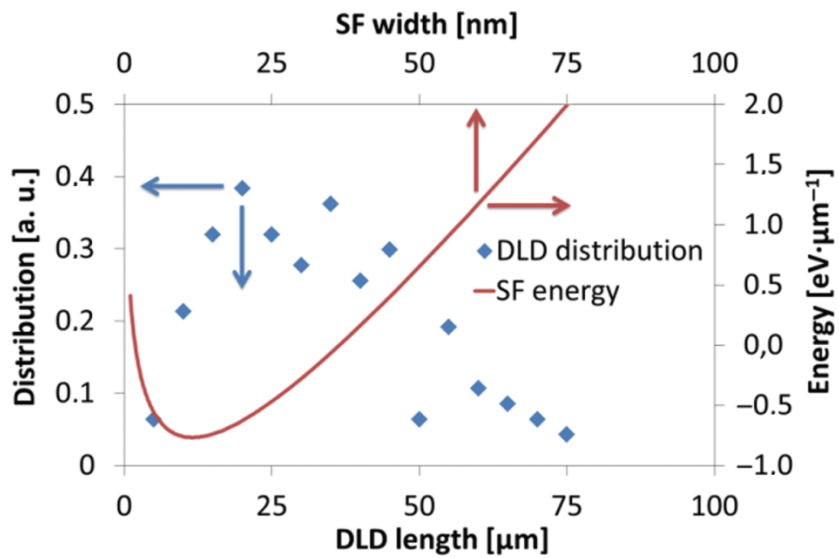


Figure 5-8. Normalized distribution of DLDs with respect to DLD width extracted from sample K with layer thickness of 100 μm . The crystal energy/unit length of SF with respect to SF width is included for comparison. The arrows indicate on which scale the data is plotted on [21].

Since the length of the DLDs corresponds to the width of the SFs as they intersect the layer surface, the observed distribution reflects the surface width distribution of the faults. An interesting conclusion that can be drawn from comparing Figures 5-7 and 5-8 [21] is a perpetual formation of new SFs do not occur throughout the growth of the ELOG layer but primarily in the earlier stages of growth, since for thinner layers most SFs have widths less than 10 μm , whereas for thicker layers only a few SFs have a width of 10 μm or less. Contrarily, if SFs were continuously forming, the occurrence frequency of SFs less than 10 μm would be more or less constant regardless of the layer thickness.

The SF energy/unit length as a function of SF width calculated from Eq. (5.3) is also shown in Figures 5-7 and 8. It first decreases sharply since the crystal energy is lowered when the separation between the bounding dislocations increases, but eventually reaches a minimum as the energy from the repulsive force becomes equal to the attractive force of the SF which increases with increasing width. The minimum crystal energy corresponds to the most energetically favorable SF width, referred to as equilibrium width which is given by Eq. (13):[20]

$$F = \frac{Gb^2}{4\pi d} - \gamma = 0 \Leftrightarrow d = \frac{Gb^2}{4\pi\gamma} \quad (5.4)$$

Using $G = 46 \text{ GPa}$ [23] and $\gamma = 17 \text{ m J m}^{-2}$ [24], for InP this translates into an equilibrium width of 12 nm in the case of Shockley partials with $b = 24 \text{ \AA}$. However, as shown in Figures 5-7 and 5-8, the DLD length, which corresponds to the stacking fault width, is generally considerably larger than this and increases significantly with increasing layer thickness. Assuming a linear increase of the average width with thickness (which is reasonable considering that the bounding dislocations appear to be straight lines as observed in Figure 5-4 & 5-7), the SF (surface) width w can be described by the following function:

$$w = Bh + w_0 \quad (5.5)$$

where h is the layer thickness, w_0 , the SF width at $h = 0$ and B a constant. Using the average DLD lengths of 3 and 30 μm at thicknesses of 10 and 101 μm respectively, B becomes ~ 0.3 and $w_0 \sim 0 \mu\text{m}$. Assuming that the SFs formed at a thickness of the order of magnitude 100 nm, this corresponds to an average initial width of around 30 nm, which is of the same order of magnitude as the theoretical equilibrium width of 12 nm. Furthermore, the incorporation of sulfur has been shown to decrease the SF energy [25-26], thereby possibly increasing the SF density and SF equilibrium width. The latter effect however will be counteracted by the strain in the ELOG layer; Dissociation of a 60° dislocation into Shockley partials will always result in

one 30° and one 90° dislocation which will not experience forces of equal magnitude in a strain field [27-29]. In compressively strained (001) films, the 90° dislocation will nucleate first and will experience a lower force than the 30° dislocation, thus leading to a contracted stacking fault. Since the ELOG layer is as previously discussed compressively strained during growth, a shorter equilibrium width would be expected on account of the strain if the SFs were bounded by Shockley partials.

5.4. Summary

We investigated SAG of InP layers on patterned Si substrates with InP/GaP buffer layers at various growth temperatures ranging from 500°C to 650°C . In order to grow high quality InP, a thin GaP buffer layer was grown on stepped sidewall surfaces of etched Si. The different growth temperature resulted in different top surfaces. The high quality InP layer with smooth surface can be attributed to the dislocation necking effect together with the formation of void. Finally, we demonstrated the formation of InGaAs/InP heterostructures using the suggested InP templates, which can be used in applications of electronic devices.

As to the origin of the SFs, there are a number of possible mechanisms: first, SFs present in the seed layer evidently can propagate through the mask openings. Secondly, they may form by random deposition errors during early SAG prior to coalescence on $\{111\}$ planes since these planes have a much lower SF energy than (001). They may also form by dissociation of TDs. Finally, SFs may form by incorrect deposition due to bond distortion because of strain in SAG islands. Presently, the latter formation mechanism of SFs appear to offer the most plausible explanation, possibly enhanced by roughness in the SiN_x mask which during lateral growth makes formation of stacking faults more energetically favorable, although dissociation of perfect dislocations into Shockley partial dislocations and random deposition errors cannot be ruled out completely. Finally, we postulate that it is possible to remove the SFs if not completely then at least decrease their density by annealing at a higher temperature, since their removal would result in a lower total crystal energy.

5.5. References

- [1] H. Ito, S. Kodama, Y. Muramoto, T. Furuta, T. Nagatuma, and T. Ishibashi, *IEEE J. Selected Topics in Quantum Electronics*, **10**, 709 (2004).
- [2] I. Németha, B. Kunertb, W. Stolza, K. Volza, *J. Cryst. Growth*, **310**, 1595 (2008).
- [3] A. Bakin, D. Piester, I. Behrens, H.-H. Wehmann, E. Peiner, A. Ivanov, D. Fehly, and A. Schlachetzki, *Crystal Growth & Design*, **3**, 89 (2002).
- [4] W.K. Liu, D. Lubyshev, J.M. Fastenau, Y. Wu, M.T. Bulsara, E.A. Fitzgerald, M. Urteaga, W. Ha, J. Bergman, B. Brar, W.E. Hoke, J.R. LaRoche, K.J. Herrick, T.E. Kazior, D. Clark, D. Smith, R.F. Thompson, C. Drazek, N. Daval. *J. Cryst. Growth*, **311**, 1979 (2009)
- [5] G. Wang, M. Leys, R. Loo, O. Richard, H. Bender, G. Brammertz, N. Waldron, W.-E. Wang, J. Dekoster, M. Caymax, M. Seefeldt, and M. Heyns, *J. Electrochemical Soc.* **158**, H645 (2011).
- [6] G. Wang, M.R. Leys, N.D. Nguyen, R. Loo, G. Brammertz, O. Richard, H. Bender, J. Dekoster, M. Meuris, M.M. Heyns, M. Caymax, *J. Cryst. Growth* **315**, 32 (2011).
- [7] G. Wang, M. R. Leys, R. Loo, O. Richard, H. Bender, N. Waldron, G. Brammertz, J. Dekoster, W. Wang, M. Seefeldt, M. Caymax, and M. M. Heyns, *Appl. Phys. Lett.* **97**, 121913 (2010).

- [8] C. Junesand, C. Hu, Z. Wang, W. Metaferia, P. Dagur, G. Pozina, L. Hultman, S. Lourdudoss, *J. Electron. Mat.* **41**, 2345 (2012).
- [9] G. Saint-Girons, P. Regreny, L. Largeau, G. Patriarche, and G. Hollinger, *Appl. Phys. Lett.* **91**, 241912 (2007).
- [10] K. Volz, A. Beyer, W. Witte, J. Ohlmann, I. Ne ´meth, B. Kunert, and W. Stolz, *J. Cryst. Growth*, **315**, 37 (2011).
- [11] H. Hasegawa, T. Shimoi, H. Asahi, *J. Cryst. Growth*, **378**, 47 (2013)
- [12] Y. Kobayashi, K. Ikeda, and Y. Shinoda, *Electron. Lett.* **23**, 242 (1987)
- [13] E. M. Vogel, *Nat. Nanotechnol.* **2**, 25 (2007).
- [14] N. Dupuis, J. Decobert, P-Y Lagree, N. Lagay, D. Carpentier, F. Alexandre, *J. Cryst. Growth*, **310**, 4795 (2008).
- [15] H. Hirayama, M. Hiroi, T. Ide, *Phys. Rev.* **B 48**, 17331 (1993).
- [16] D. Hwang, T. Yasuda, K. Ikuta, S. Yamasaki, K. Tanaka, *Jpn. J. Appl. Phys.* **37** 4204 (1998).
- [17] G. Zhou, Y. Lu, Q. Zhang, *IEEE Electron. Dev. Lett.* **33**, 782 (2012).
- [18] J. W. Matthews; Accommodation of misfit across the interface between crystals of semiconducting elements or compounds; *J. Appl. Phys.* **41**, 3800 (1970)
- [19] E. A. Fitzgerald; Dislocations in strained-layer epitaxy: Theory, experiment, and applications; *Mater. Sci. Reports* **7**, 87 (1991).

- [20] D. Hull and D. J. Bacon; Introduction to Dislocations; Butterworth-Heinemann, Oxford (2001).
- [21] D. Hull and D. J. Bacon, *Mater. Express*, **4**, 1, (2014).
- [22] F. Ernst and P. Pirouz; The formation mechanism of planar defects in compound semiconductors grown epitaxially on {100} silicon substrates; *J. Mater. Res.* **4**, 834 (1989).
- [23] D. N. Nichols, D. S. Rimai, and R. J. Sladek; Elastic anharmonicity of InP: Its relationship to the high pressure transition; *Solid State Commun.* **36**, 667 (1980).
- [24] H. Gottschalk, G. Patzer, and H. Alexander; Stacking fault energy and ionicity of cubic III–V compounds; *Phys. Status Solidi* **45**, 207 (1978).
- [25] H. Suzuki; Chemical interaction of solute atoms with dislocations; *Sci. reports Res. Institutes, Tohoku Univ.* **A4**, 455 (1952).
- [26] R. DeWit and R. E. Howard, *Acta Metall.* **13**, 655 (1965).
- [27] P. M. J. Marée, J. C. Barbour, J. F. van der Veen, K. L. Kavanagh, C. W. T. Bulle-Lieuwma, and M. P. A. Vieggers, *J. Appl. Phys.* **62**, 4413 (1987).
- [28] J. Zou and D. J. H. Cockayne, *J. Appl. Phys.* **74**, 925 (1993).
- [29] J. Petruzzello and M. R. Leys, *Appl. Phys. Lett.* **53**, 2414 (1988).

Chapter 6

Summary and conclusions

In this PhD work, the selective epitaxial growth of InP on Si (001) substrates has been studied and high-quality InP layers with extremely flat surface using a thin GaP buffer layer have been obtained. The main focus of this work is to study the defect formation mechanism during epitaxial growth and to develop solutions to reduce the defect density so that device-quality III-V virtual substrates can be realized on large-scale Si substrates. This work offers the required knowledge to fabricate InP virtual substrates with SiNx trench by using selective area growth (SAG).

Chapter 3 demonstrated that high quality GaP growth on exact (001) Si substrates is an important prerequisite for integrating III/V-based device layers with Si-based nanoelectronics. The present chapter summarizes a multi-step MOCVD process to achieve such high quality GaP/Si (001) template substrates after the growth of only 100nm Ga layer thickness.

We have investigated the generation process of low defects in GaP layers grown on Si substrates by FME. It was found that the APBs could be annihilated during the growth, and there were optimized growth condition as growth temperature, V/III ratio and growth rate. RMS roughness is 2.8 nm from the optimized growth conditions. Moreover, it was clarified that a few stacking faults and threading dislocations were detected during the lattice relaxation process in the MOCVD grown GaP/Si. It is considered that the

generation of stacking faults in the MOCVD growth would be attributed to the coalescence or expansion of isolated islands at the initial growth stage. The presence of stacking faults would result in the generation of threading dislocations during the lattice relaxation process.

Chapter 4 provides that InP epilayers were grown on Si substrates using buffer layers of GaP. AFM, SEM and TEM examination results showed that GaP is a proper material as a buffer layer, and that its optimum thickness is about 3~5nm. TEM observation showed that the inserted InGaAs strained layers were very helpful to reduce the surface roughness and defect reduction. It also confirmed that GaP acted as a buffer to alleviate the lattice mismatch between InP and Si. The best AFM roughness obtained from inserted InGaAs strained layers was 2.1nm for $5 \times 5 \mu\text{m}^2$.

In chapter 5, we investigated SAG of InP layers on patterned Si substrates with InP/GaP buffer layers at various growth temperatures ranging from 500 °C to 650 °C. In order to grow high quality InP, a thin GaP buffer layer was grown on stepped sidewall surfaces of etched Si. The different growth temperature resulted in different top surfaces. The high quality InP layer with smooth surface can be attributed to the dislocation necking effect together with the formation of void. Finally, we demonstrated the formation of InGaAs/InP heterostructures using the suggested InP templates, which can

be used in applications of electronic devices.

Cross-section TEM images furthermore that the TDDs corresponded to intersections between the SAG layer surface and SFs lying on the {111} planes. The SFs were generally blocked by the mask but at some points propagated through the mask openings. In addition, new SFs seemed to form, most likely early in the growth process during lateral growth rather than continuously during the growth since thicker layers exhibited fewer SFs with short width.

Abstract (in Korean)

고품질 III-V층을 Si 기판 위에 성장하는 방법은 Si 위에 CMOS 소자를 집적 하는 것과 고성능, 저전력 로직 소자 적용에 대한 기대로 여러 해 동안 많은 관심을 받아 왔다. 뿐만 아니라 Si 기판 위에 III-V 물질이 적층이 될 경우 테라헤르쯔 전자 소자, 광전 소자, 통신 소자 적층 등의 새로운 기능을 가지는 소자에 적용될 수 있기 때문에 더욱 주요 연구 기관들의 관심을 받아 왔다.

본 연구에서는 그러한 소자 응용에 적용시킬 수 있도록 선택 영역 성장 방법을 이용하여 Si (001) 기판 위에 InP 층을 에피텍셜로 성장시키는 것이다. Si (001) 기판 위에 SiNx 마스크를 사용하여 먼저 얇은 GaP층을 핵생성과 버퍼층으로 성장하고 InP층을 그 위에 성장하였다. 이러한 선택 영역 성장 방법으로 고품질의 에피층을 성장하는 데 있어 몇 가지 극복해야 될 장애물들이 존재한다. 가장 먼저 InP 층과 Si 기판 사이의 격자 상수 차이가 8% 이상 나기 때문에 에피 성장하면서 발생하는 결함이다. 이러한 격자 상수 차이에 의한 물질 특성 차이는 계면에서 많은 전위와 면결함을 발생시키고 이는 최종 디바이스의 누전 전류 통로로 작용하기 때문에 반드시 극복되어야 되는

문제이다. 두 번째는 InP와 Si 기판 또는 InP와 SiNx 물질의 열팽창 계수 차이에 의한 stress 발생과 그에 따른 추가 결함이 있다. 특히 각각의 계면에서 적층 결함 (Stacking faults) 및 쌍극면(Twin)이 주로 발생 되며 이것 또한 디바이스의 특성을 저하시키게 된다. 마지막으로 III-V 물질이 극성을 가지는 물질로서 비극성인 Si 기판 위에 성장할 때 APBs(Anti-phase boundaries) 면 결함을 발생 시키는 것이다.

본 학위 논문에서는 그러한 결함의 발생 메커니즘을 규명하고 그 결함을 최소화 시킬 수 있는 마스크 디자인과 성장 조건을 확인하였다. 그리고 Si CMOS 공정에 호환될 수 있도록 CMP 공정이 필요 없는 매우 평평한 표면층을 가지는 InP를 성장시키기 위한 방법을 연구 하였다.

먼저 패턴이 없는 평면 Si 기판 위에 핵 생성층으로 GaP 층의 최적 성장 조건을 확인하였다. 성장 온도, 성장 속도, V/III 비 등의 조합으로 Si (001) 기판 위에 표면 거칠기가 2nm 수준의 고품의 GaP 층을 형성할 수 있었으며 성장 온도를 2단계로 나뉘어 성장하는 방법과 FME 모드 방법을 사용하여 XRD FWHM 값이 133 arcsec으로 좋은 결과를 얻었다. 또한 그 GaP 버퍼층 위에 고품위 InP를 성장시켰으며 두 층 사이에 In_{0.6}Ga_{0.4}As의 strain 인가 층을 삽입하여 표면 거칠기가 2.3nm인 좋은 결과를 얻었다.

다음으로 선택 영역 성장에 영향을 가장 큰 영향을 줄 수 있는 마스크 물질과 디자인의 변수를 여러가지 마스크 모양으로 만들어 변수를 확인 하였다. 최종적으로 평탄한 버퍼층을 얻기 위해서는 SiO₂ 보다 SiN_x로 마스크를 사용하는 것이 유리하며 이것은 에피텍셀 성장 전에 전처리 공정에서 마스크 모양 변화가 없도록 하는 데에도 매우 성공적으로 작용한다. 또한 SiN_x 뿐만 아니라 Si 층도 일부 에칭을 하여 만들어진 트랜치에서 aspect ratio 값이 약 2정도 될 때 가장 평탄하고 고품위의 InP가 성장되는 것을 확인하였다. 그리고 SiN_x의 맨 위 부분의 모양이 사각으로 날카롭게 만들어지는 것보다 둥근 형태로 될 때 버퍼의 최종 층이 균일하고 평탄하게 자란다는 것을 확인하였다.

마지막으로 그러한 SiN_x 마스크 트랜치 내부에 InP 기판을 성장할 때 변수들을 확인하였고 최적의 성장 조건을 확인하였다. 성장 온도가 500°C에서 650°C로 높아지면 최종 InP 층의 모양은 {111}면을 가지면서 뾰족한 삼각형 모양이 되고 550°C에서는 평탄한 InP 버퍼층이 성장되었다. 균일하고 평탄한 InP 버퍼층은 디바이스를 제작할 때 CMP 공정을 생략할 수 있으므로 비용 절감 측면에서도 매우 좋은 방향이며 추가 공정을 하지 않아 활성층의 품질도 높일 수 있는 방법이 된다. 이렇게 성장된 InP 버퍼층 위에 최종 채널 물질이 되는 In_{0.53}Ga_{0.47}As층을

형성하여 동일하게 평탄하고 고품위의 채널 물질이 형성되는 것을 확인하였다.

Keywords: 인듐 포스파이드, 갈륨 포스파이드, 선택 영역 성장, APB, 금속 유기 화학 증착법, 표면 거칠기, 결함 제거

Student Number: 2011-30192

Research achievements

SCI Publication lists

1. **Sang-Moon Lee**, Euijoon Yoon and Jinsub Park, "High quality InP growth on exact Si (001) substrates" (In preparation)
2. Keun Wook Shin, **Sang-Moon Lee**, Sung Hyun Park, Sewoung Oh, Yongjo Park, and Euijoon Yoon, "Heteroepitaxial InP growth on Si(001) and Ge(001) substrates by metalorganic chemical vapor deposition" (In preparation)
3. **Sang-Moon Lee**, Young Jin Cho, Jong-Bong Park, Keun Wook Shin, Euichul Hwang, Sunghun Lee, Myoung-Jae Lee, Seong-Ho Cho, Dong Soo Shin, Jinsub Park and Euijoon Yoon, "Effects of growth temperature on surface morphology of InP grown on patterned Si (001) substrates" , J. Cryst. Growth (Accepted), 2014.
4. Hyun Soo Jin, Young Jin Cho, **Sang-Moon Lee**, Dae Hyun Kim, Dae Woong Kim, Dongsoo Lee, Jong-Bong Park, Jeong Yeon Won, Myoung-Jae Lee, Seong-Ho Cho, Cheol Seong Hwang and Tae Joo Park,

"Interface Sulfur Passivation Using H₂S Annealing for Atomic-layer-deposited Al₂O₃ Films on an Ultrathin-Body In_{0.53}Ga_{0.47}As-on-Insulator", App. Surf. Sci, (accepted), (2014).

5. Myoung-Jae Lee, Dongsoo Lee, Seong-Ho Cho, Ji Hyun Hur, **Sang-Moon Lee**, BokKi Min, David H. Seo, Dong-Sik Kim, Moon-Seung Yang, Sunghun Lee, Euichul Hwang, Mohammad Rakib Uddin, U-In Chung, Youngsoo Park, and In-Kyeong Yoo, "Integrated Chalcogenide Switch Device by Reactive Nitrogen and Plasma Treatment for Stackable Scalable 3D Nanoscale Memory", Nature Communications, 2013, 4, 2629

International conference presentations

1. **Sang-Moon Lee**, Myeong-Jae Lee, Youngjin Cho, Jongbong Park, Seung-Hoon Lee, Mun-Seoung Yang, Dongsoo Lee, Euichul Hwang, Jihyun Hur, Bokki Min, Hyungsuk Seo, Mohammad Rakib Uddin, Seong-Ho Cho, Youngsoo Park, Euijoon Yoon, "Selective Area Growth

of High Quality III-V Materials on Si (001) by MOCVD”, MRS fall meeting 2013, T4.04 (2013)

2. Keun Wook Shin, **Sang-Moon Lee**, Daeyoung Moon, Sewoung Oh, Changjae Yang, Youngjin Cho, Gun-Do Lee, Yasushi Nanishi, and Euijoon Yoon, “The effects of growth temperature and V/III ratio on InP heteroepitaxial growth on Si(001) substrates using metalorganic chemical vapor deposition”, 16th International Conference on Metal Organic Vapor Phase Epitaxy (2012)
3. Keun Wook Shin, **Sang-Moon Lee**, Sewoung Oh, Daeyoung Moon, Sung Hyun Park, Changjae Yang, Youngjin Cho, Yasushi Nanishi, and Euijoon Yoon, “Heteroepitaxial InP growth on Si(001) using MOCVD”, 9th SNU-Ritsumeikan joint workshop (2012)
4. Keun Wook Shin, **Sang-Moon Lee**, Sewoung Oh, Daeyoung Moon, Sung Hyun Park, Changjae Yang, Youngjin Cho, Yasushi Nanishi, and Euijoon Yoon, “Heteroepitaxial InP growth on Si(001) using MOCVD”, 4th International Symposium on Advanced Plasma Science and its Applications for Nitrides and Nanomaterials (2012)
5. **Sang-Moon Lee**, Youngjin Cho, Keunwook Shin, Jongbong Park, Euijoon Yoon and U-In Chung, “Heteroepitaxial Growth of GaP on

Exact Si (100) Substrates for III/V nano device integration”, Nano Korea
2012 (2012)

6. **Sang-Moon Lee**, YoungJin Cho, Seongho Jeon, Jae-Gwang Shin,
Youngsoo Park, Euijoon Yoon, and U-In Chung, " Heteroepitaxial
Growth of GaP on Exact Si (100) Substrates by Metalorganic Chemical
Vapor Deposition", MRS fall meeting 2011 (2011)

감사의 글

먼저 이 모든 과정을 끝까지 이끌어 주신 주 나의 하나님께 감사를 드립니다.

나에게도 박사 학위의 마지막 감사의 글을 작성하는 날이 올 수 있을까를 생각해 본 적이 있었던 것 같습니다. 다른 사람들과는 조금 달리 바쁜 회사 생활 가운데 학교 수업 따라가기도 벅차다고 생각되는 그 때, 논문자격시험을 준비하면서 회사와 도서관에서 밤늦게까지 시험 준비를 하던 그 때 그리고 마지막 졸업 논문 준비와 디펜스를 준비하던 그 때, 바로 이 순간을 바라보며 달려 온 것 같습니다. 하지만 막상 마지막 페이지를 마무리하려는 지금 이 순간 뿌듯한 마음보다는 지난 날 부족했던 순간들에 대한 아쉬움이 더 크게 다가 옵니다. 회사와 가정 그리고 학교 생활 그 모든 것에 좀 더 잘하지 못했던, 특히 처음 학위를 시작하며 가졌던 다짐과 목표들에 지금 내가 얼마나 이뤘나를 바라보면 부끄러운 마음까지 듭니다. 그래도 순간 순간 최선을 다해 열심으로 노력했던 자신을 바라보며 위안으로 삼고 그 과정에서 소홀했던 모든 것들에 대해 오늘 다시 한번 반성하면서 앞으로의 더 멋진 삶을 다짐해 봅니다.

처음 학회에서 만나 파트 타임 박사학위를 요청 드렸을 때 기꺼이 허락해 주시고 지난 4 년 동안 많은 조언들로 이끌어 주신, 저의 지도 교수님이신 윤의준 교수님께 진심으로 감사를 드립니다. 또한 부족한 저의 박사학위 논문을 심사하여 주신 김미영 교수님, 박용조 교수님, 고대홍 교수님 그리고 조성호 전문님께도 다시 한번 감사의 말씀을 전합니다. 모든 교수님들께서 남겨주신 조언과 격려들은 잊지 않고 앞으로의 회사 연구 활동에 주춧돌이 될 수 있도록 노력하겠습니다. 그리고 저의 고향 선배님이자 이 논문의 시작과 끝을 끝까지 도와주신 박진섭 교수님께 한없는 감사를 표현하고 싶습니다.

학위를 처음 시작할 수 있도록 기회를 주신 박영수 전무님, 김택 부장님을 비롯하여 삼성종합기술원에서 같이 III-V 연구를 진행했던 팀원들 조영진 전문님, 이명재 박사님, 허지현 수석님, 최영문 수석님, 이성훈 박사, 양문승 책임, 황의철 책임, 이동수 책임, 서형석 책임, 라킵 박사 모두에게 감사를 드립니다. 또한 반도체 연구소로 옮긴 후 지난 1 년여동안 많은 조언을 아끼지 않으신 구본영 부장님을 비롯하여 우리 III-V 팀원들 김철 책임, 윤지언 책임에게도 감사를 전합니다. 그리고 비록 짧은 박사학위 기간이었지만 학교 생활과 논문 준비에 많은 도움을 준 건축이와 상수, 세훈, 세웅이를 비롯하여 여러 CSEL 선후배 학생들에게도 고마움을 전합니다. 또한 어렵고 힘들어할 때 늘 옆에서 기도로 용기를 북돋아 준 수영이형과 일범 집사를 비롯하여 수원화산교회 및 생명샘 교회 목사님, 집사님들께도 감사의 마음을 전합니다. 이 논문을 준비하기까지 도움을 주신 모든 분들의 이름을 한 분 한 분 다 적지는 못하지만 이 글을 읽고 계시는 모든 분들이 바로 저에게는 더 없는 고마움을 전하고 싶은 분들입니다. 지금까지 저에게 주셨던 격려와 조언들 그리고 아낌없는 성원들을 잊지 않고 보답할 수 있도록 더 노력하고 더 매진하는 삶을 보여 드릴 것입니다.

마지막으로 항상 멀리서 묵묵히 저를 응원해 주신 어머니와 형, 누나들, 형수, 매형들, 처형, 형님들 그리고 이제는 천국에서 바라보며 미소 지으실 장모님을 비롯하여 마지막 이 순간까지도 새벽을 깨워 기도하며 그 어려웠던 순간들을 함께 인내하고 웃어 준 사랑하는 아내와 세상 그 어떤 것과도 바꿀 수 없는 귀한 세 선물 정민이, 현민이, 석현이에게 이 논문을 두 손 모아 바칩니다.

2015년 1월
이 상 문 拜上