A High-Speed Range-Matching TCAM for Storage-Efficient Packet Classification

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***Abstract*—A critical issue in the use of TCAMs for packet classification is how to efficiently represent rules with ranges, known as range matching. A range-matching ternary content addressable memory (RM-TCAM) including a highly functional range-matching cell (RMC) is presented in this paper. By offering various range operators, the RM-TCAM can reduce storage expansion ratio from 4.21 to 1.01 compared with conventional TCAMs, under real-world packet classification rule sets, which results in reduced power consumption and die area. A new pre-discharging match-line scheme is used to realize high-speed searching in a dynamic match-line structure. An additional charge-recycling driver further reduces the power consumption of search lines. Simulation results of a 256×64-bit range-matching TCAM, when implemented in the 0.13-μm CMOS technology, achieves a 1.99-ns search time with an energy efficiency of 1.26 fJ/bit/search. While a TCAM including range encoding approach requires an additional SRAM or DRAM, the RM-TCAM can improve storage efficiency without any extra components as well as reduce the die area.**

***Index Terms*—Content addressable memory (CAM), dynamic match-line scheme, packet classification, range matching cell.**

I. Introduction

As NETWORK transmission rates grow rapidly and complicated packet filtering is required to guarantee the quality of services (QoS), packet classification becomes a critical operation in networking devices such as routers [1], [2] and network intrusion detection systems (NIDS) [3]. In a typical Layer-4 switching application on IPv4, a packet classification rule is generally composed of the following five fields: 1) source IP address; 2) destination IP address; 3) source port; 4) destination port; and 5) protocol number, as shown in Table I. Generally, packet classification requires a longest prefix matching for the IP address field and a range matching for the TCP port field. Many software-based methods, including hierarchical tries and heuristic algorithms [4], have been proposed to support these various matching operations. However, software-based implementations of range matching have difficulty in keeping up with the speed requirement of the high-speed networks, such as SONET OC-768 (40 Gbps).

A content-addressable memory (CAM) [5], [6] is a more viable approach to the packet classification in high-speed network applications. To provide longest prefix matching and range matching, ternary CAM (TCAM) is widely employed rather than binary CAM. However, TCAMs have a serious limitation in range matching on TCP port fields, because they only allow ternary matching with a masking operator. Since TCAM cells store one of three states [0, 1 and 'X' (don't care)], a range has to be expanded into a set of sub-prefixes, thereby requiring multiple entries. For example, the range of 1024-65535 has to be expanded into 6 entries, as shown in Fig. 1. In the worst case, the number of entries required to represent a range in a single k-bit field is $2(k-1)$. Furthermore, a range with two fields may require as many as $4(k-1)^2$ prefixes. So a typical Layer-4 rule with a range that includes 16-bit source and destination port fields might have to be expanded into $4\times(16-1)^2 = 900$ entries in the worst case [7]. Indeed, utilization efficiency of conventional TCAMs can be further eroded with an increasing number of ranges in source and destination port fields used in real-world databases [7]. Consequently, the expansion of TCAM entries for range matching dissipates extra power and increases the die area. Although the existing dynamic range encoding scheme (DRES) [8] can significantly improve TCAM storage expansion ratio for range matching, it requires extra bits and an external DRAM or SRAM to support its complicated range-encoding process. In addition, the storage efficiency of the TCAM using DRES can be deteriorated with an increasing various ranges.

In this paper, we present a range-matching TCAM (RM-TCAM) that includes a novel range-matching cell

TABLE I
AN EXAMPLE OF PACKET CLASSIFICATION RULES ('X' MEANS A DON'T CARE BYTE)

Rule Index	Source IP (32bit)	Destination IP (32bit)	Source Port (16bit)	Destination Port (16bit)	Protocol (8bit)
1	192.168.1.X	147.46.10.X	> 1023	X.X	6
2	192.168.X.X	222.23.X.X	2047	6000-6064	17
3	192.X.X.X	10.10.X.X	256-512	768-2047	4
4	10.X.X.X	10.X.X.X	512-15536	256-512	X

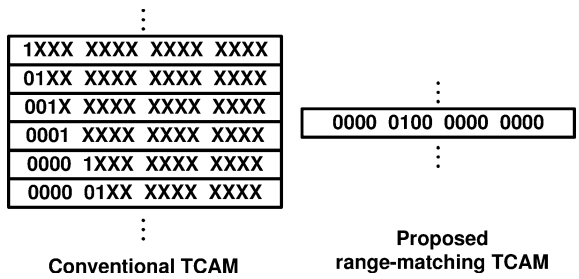

Fig. 1. Range mapping of the range 1024-65535 on a conventional TCAM and on a range-matching TCAM.

Manuscript received January 26, 2007; revised February 05, 2008 and May 24, 2008. First published October 31, 2008; current version published June 19, 2009. This paper was recommended by Associate Editor I. Verbauwhede.

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Digital Object Identifier 10.1109/TCSI.2008.2008512

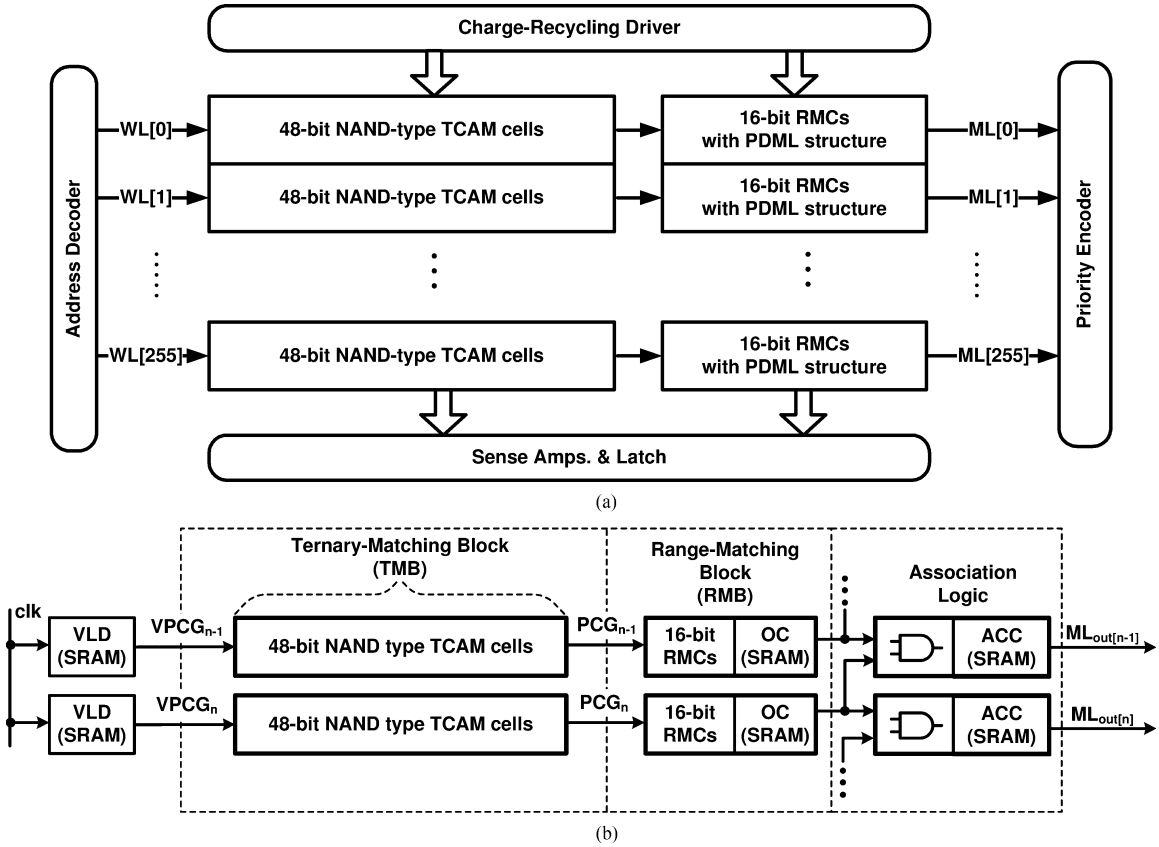


Fig. 2. (a) Block diagram of the range-matching TCAM. (b) 64-bit match-line structure of each entry.

TABLE II
STORAGE EXPANSION RATIO UNDER REAL-WORLD RULE SETS [8] OF THE PROPOSED RANGE-MATCHING TCAM COMPARED WITH A CONVENTIONAL TCAM AND A TCAM USING DRES [8]

Rule Set	A	B	C	Avg
Number of Rules	279	183	264	242
Rule with range (%)	9.3	7.7	54.9	24.0
Conventional TCAM (#Entries)	3.40 (949)	3.02 (553)	6.20 (1638)	4.21
TCAM with DRES [8]	1.22	1.33	1.23	1.26
RM-TCAM (This work)	1.01	1.01	1.02	1.01

(RMC). The RM-TCAM can directly represent a range with only one or two entries without any encoding process and external devices, which can greatly improve storage efficiency as well as reduce power consumption and die area. Table II (refer to [8] and [9]) shows the relative storage expansion ratio, defined as the number of rule entries divided by the number of rules in a TCAM, of the RM-TCAM for three real-world rule sets in [8]. On the average, the RM-TCAM can reduce the storage expansion ratio from 4.21 to 1.01, compared with a conventional TCAM. Moreover, the RM-TCAM is more efficient than a TCAM using DRES which requires additional bits for range encoding.

Range matching in a RM-TCAM is performed by an RMC which incorporates a range comparator within each cell. The proposed RMC can be implemented in two different ways, known as static or dynamic match-line structures, depending on their application. The RMC with static match-line structure is suitable for a low-power operation while the RMC with the dynamic match-line structure is more appropriate for a high-speed operation.

We also present a dynamic match-line scheme suitable for a dynamic RMC. Since the RMC has similar characteristics to a NAND-type TCAM cell [10], the bit width of each memory entry is limited by speed considerations. We propose a pre-discharging match-line (PDML) scheme for a fast searching operation, which can easily be adapted to include a charge-recycling driver so as to save more power.

In Section II, we describe the RM-TCAM architecture. In Section III, we present the RMC and the PDML scheme. Section IV details the charge recycling driver. Section V presents comparative simulation results and storage efficiency. Finally, Section VI summarizes the paper.

II. RM-TCAM ARCHITECTURE

The proposed RM-TCAM is composed of 48-bit typical TCAM cells for longest prefix matching [11] and 16-bit RMCs for range matching. In the following discussion, we focus on storage-efficient range matching using the new RMC and on the speed of operation achieved by the proposed PDML architecture.

Fig. 2(a) is a block diagram that shows how our RM-TCAM is composed of TCAM cells, RMCs, charge recycling drivers,

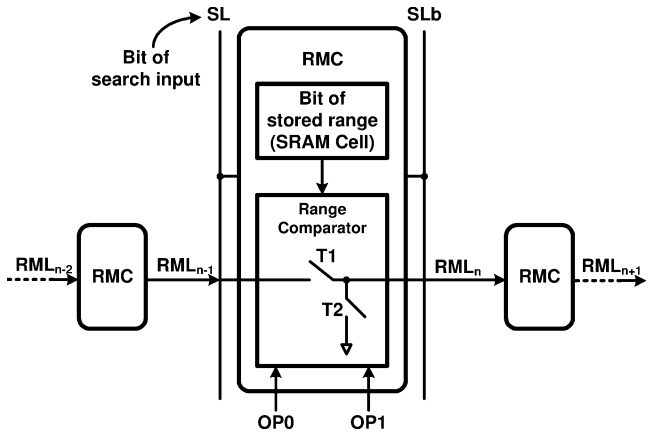


Fig. 3. Simplified symbolic diagram of the RMC.

sense amplifiers, and a priority encoder which includes the association logic. Each entry is divided into a ternary-matching block (TMB) for longest prefix matching that is necessary in searching IP address fields and a range-matching block (RMB) which matches TCP port fields, as shown in Fig. 2(b). The TMB is implemented with NAND-type TCAM cells to achieve low power operation. However, when high speed operation is preferred, it can alternatively be implemented with NOR-type TCAM cells without any extra circuitry.

To save power, the RMB is enabled only when the TMB has found a match. Since the IP address field which is stored in the TMB has various values generally [1], this TMB and RMB configuration has the advantage of saving power. When the range rule includes two inequalities, for example $\{512 \leq$ TCP port $\leq 1023\}$, the association logic combines two neighboring entries to achieve a logical AND operation between the two inequalities: in this case one entry expresses ($512 \leq$ TCP port) and the other expresses (TCP port ≤ 1023) in this example. Such a combination is indicated by setting the association control cell [ACC in Fig. 2(b)]. Otherwise, entries are matched independently. A VLD cell indicates the validity of the entry. If the entry is invalid, its match line is deactivated by holding the pre-charge signal VPCG to ground. Each 16-bit RMC in the RMB has a 2-bit operator cell OC which indicates the type of operator to be applied to the search-input data. In the next section, we will explain the operation of the RMC and the role of the OC in more detail.

III. Range-Matching Cell (RMC)

A. Operation of the RMC

The proposed RMC is composed of an SRAM cell which stores one bit of range data and a range comparator to match the incoming search-input data, whereas a typical TCAM cell has two SRAM cells which store a bit of data and a mask indicating 'X' (don't care).

Fig. 3 shows a simplified symbolic diagram of the RMC which illustrates its operation and function. The $\{\mathrm{OP0}, \mathrm{OP1}\}$ signals come from the OC, which is shared by all the RMCs in the same entry. Although the additional OC, composed of 2-bit SRAM cells, is required to store the operation type in the RM-TCAM, its impact on the cost of increased die area is offset by the improved storage expansion ratio. Also, the $\{\mathrm{OP0}, \mathrm{OP1}\}$ signals can easily be routed, because they do not need to operate at high speed. Section V will describe this aspect in detail. Depending on the logical operation that is required, the $\{\mathrm{OP0}, \mathrm{OP1}\}$ signals are statically set to one of three combinations: {1, 0}, {0, 1} or {0, 0}, which correspond respectively to the "greater than or equal to (GE)", "less than or equal to (LE)" and "equal to (EQ)" operators. If a bit of the stored range is equal to the corresponding bit of the search-input data, then T1 is turned on regardless of the state of the signals $\{\mathrm{OP0}, \mathrm{OP1}\}$, thereby connecting the nth node of the match line, RML_n, to the preceding node, RML_{n-1}. This operation is similar to that of a typical NAND-type TCAM cell. Otherwise, T1 is turned off and T2 is turned on or off depending on the range-matching result. When a bit of the search-input data matches a range condition, T2 is turned on and RML_n is connected to ground. Table III summarizes the matching results for each case.

Fig. 4 shows examples of 4-bit range-matching, which should help to explain the operation of the RMC. Range matching is achieved by bit-to-bit comparison, processing from the MSB to the LSB. Prior to evaluation, the RML_3 node of the

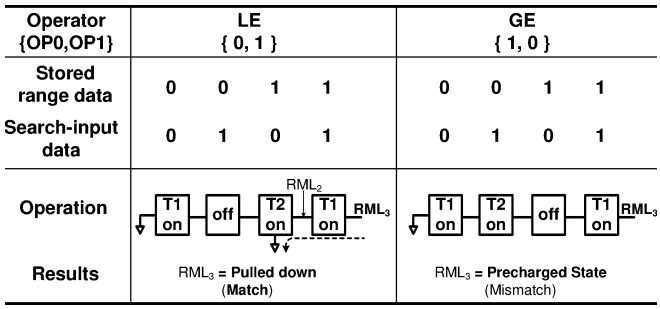


Fig. 4. Example of range matching using the RMC. In this example, the search-input data is 1010 (0xA) and the stored range data is 1100 (0xC).

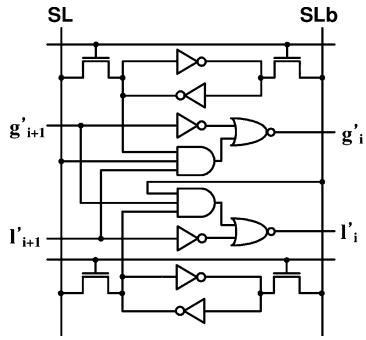


Fig. 5. Range-check cell of an Extended TCAM [9].

TABLE III
Matching Results of the RMC

Operator {OP0, OP1} / {bit of stored range, bit of search-input}	EQ {0, 0}	GE {1, 0}	LE {0, 1}
{ 0, 1 }	T1 : off T2 : off	T1 : off **T2 : on**	T1 : off T2 : off
{ 1, 0 }	T1 : off T2 : off	T1 : off T2 : off	T1 : off **T2 : on**
{ 0, 0 } or { 1, 1 }	**T1 : on** T2 : off	**T1 : on** T2 : off	**T1 : on** T2 : off

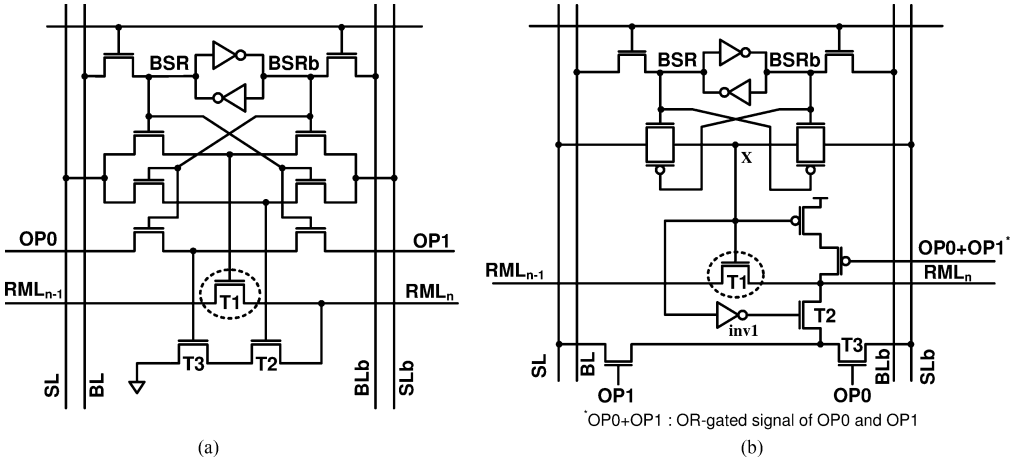


Fig. 6. (a) RMC with a dynamic match-line structure. (b) RMC with a static match-line structure.

RMC is precharged. When the search-input data is matched with the stored range data, the output RML_3 is discharged to indicate a match in this example. Otherwise, RML_3 remains in its precharged state. For example, if the stored range data is 1100 (0xC), the searched-input data is 1010 (0xA), and the $\{\mathrm{OP0}, \mathrm{OP1}\}$ signals are $\{0, 1\}$, corresponding to the "less than or equal to (LE)" operator, then the RMC corresponding to the MSB connects its RML_3 node to its RML_2 node. The second RMC discharges its RML_2 node to indicate a match and the results from its RML_0 and RML_1 nodes are overridden, because T1 is turned off and T2 is turned on in the second RMC. The matching result conforms to Table III. Fig. 4 shows another example of the "greater than or equal to (GE)" operator. In this case, RML_3 remains in its precharged state to indicate a mismatch. As these examples demonstrate, we can efficiently represent a range by using the proposed RMC which conforms to Table III.

B. Implementation of the RMC

The previously reported extended TCAM [9] uses a range-check cell to reduce the impact of the expansion of TCAM entries for range matching. As shown in Fig. 5, this range-check cell is composed of SRAM cells and general CMOS logic gates. Although the Extended TCAM can represent a range without an encoding scheme, there are two implementation problems. First, the range-check cell requires a large number of transistors, twice as many as a typical TCAM cell. Second, range matching is too slow, because the matching result must pass along a carry-ripple structure consisting of CMOS gates.

The RMC is designed to avoid these problems. An RMC can be implemented with a dynamic or a static [12] match-line structure, respectively, as shown in Fig. 6. The dynamic and static match-line RMCs function in the same way, except that the static match-line RMC pulls its match line up or down by itself. In a dynamic match-line RMC, the RML_n is connected to the RML_{n-1} by turning on transistor T1, when a bit of the stored range (BSR in Fig. 6) equals the bit of the search input (SL). Otherwise, the RML_n is discharged or remains in its precharged state, depending on the matching result. For example, if the BSR is 0, the SL is 1, and the {OP0, OP1} signals are {1, 0}, then T2 and T3 are turned on and T1 is turned off. This connects RML_n to ground, indicating that the search-input bit SL is greater than the BSR, which conforms to Table III. If the $\{\mathrm{OP0}, \mathrm{OP1}\}$ signals are $\{0, 1\}$ in this case, the RML_n remains in precharged state, which means that the search-input bit SL does not match the range condition corresponding to "less than or equal to (LE)."

To improve noise immunity and increase the evaluation speed, full CMOS pass gates are used in the static match-line RMC. These CMOS pass gates allow a full voltage swing on the internal node X, which makes it easier to stack RMCs in series and to drive the internal inverter [inv1 in Fig. 6(b)]. Since the static match-line structure does not require precharging of the match line, it consumes less power than the dynamic counterpart. However, the requirements for CMOS pass gates and an inverter in the static match-line version break the cell symmetry as well as increase the cell area. On the other hand, a dynamic match-line RMC can be more symmetrical and smaller than the static match-line RMC. However, a disadvantage of the dynamic match-line RMC is the difficulty of stacking cells without affecting the overall speed. Therefore, we now go on to describe a novel match-line scheme, a development of the typical domino scheme, which improves the speed of the dynamic match-line structure. This will be followed in Section V by a comparison between the static and dynamic match-line RMC.

C. Pre-Discharging Match-Line (PDML) Scheme

In a typical dynamic match-line structure which uses NAND-type TCAM cells, a search operation is divided into two phases: precharge and evaluation. During the precharge phase, all $\mathrm{RML}_{0,1,\ldots,n}$ nodes are precharged by driving all their complementary search lines (SL and SLb) to VDD in the typical dynamic match-line scheme [1]. However, this increases the power consumption of the search lines and degrades the matching speed when the cells are stacked in a serial fashion [10]. To resolve these problems, an AND-type match-line scheme with a pseudo-footless clock-and-data precharged dynamic (PF-CDPD) gate has been introduced [13]. The internal nodes C_1 and C_2 in Fig. 7(a) are precharged instead of all $\mathrm{RML}_{0,1,\ldots,n}$, and the PF-CDPD does not require a search-line transition to precharge the RML nodes. Therefore, search data can be simultaneously driven during the precharge phase in the PF-CDPD scheme, which allows increased matching speed and

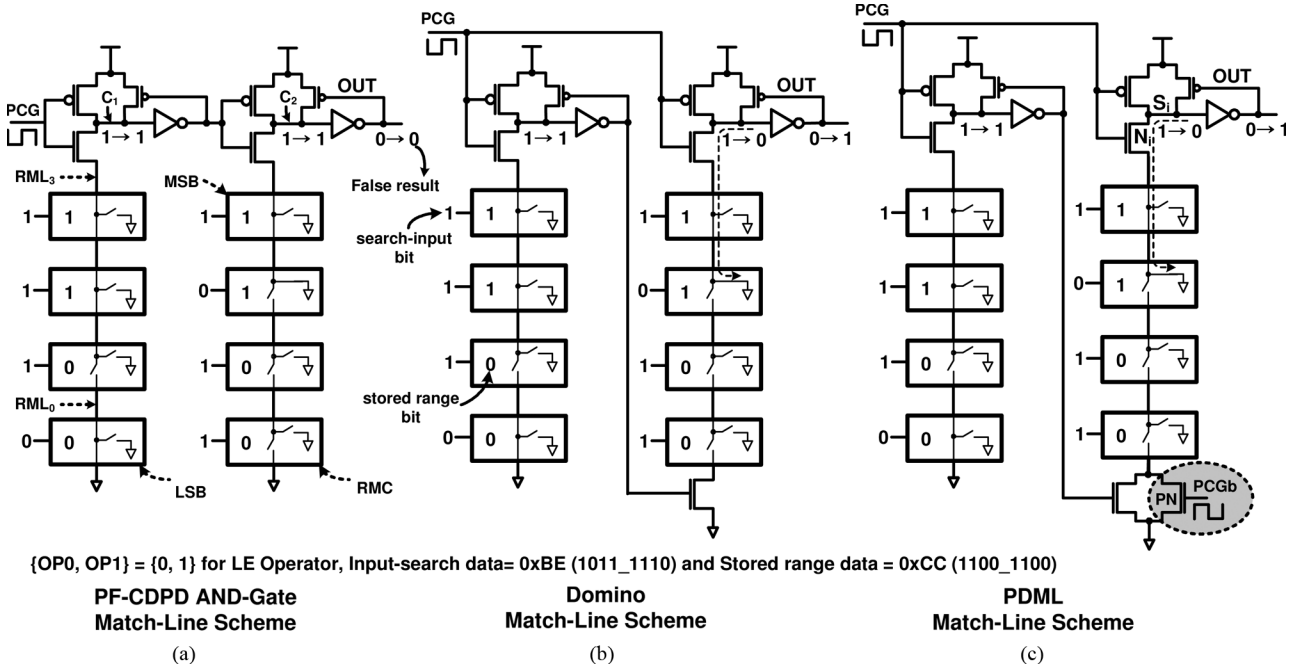


Fig. 7. Examples of range-matching in: (a) PF-CDPD, (b) domino, and (c) PDML match-line structures.

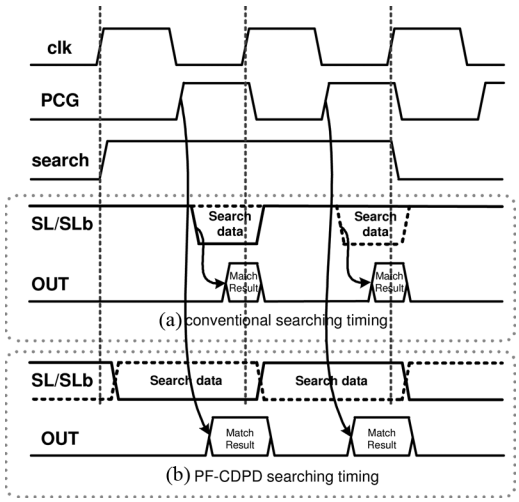


Fig. 8. Timing diagram of the search line. (a) Conventional method with search-line transition for precharging. (b) PF-CDPD method without search-line transition.

reduces the power consumption in the search lines by eliminating the search-line transition, as shown in Fig. 8. However, the PF-CDPD gates cannot be directly applied to a dynamic match-line RMC, because they are only effective in exact or ternary matching, in which they perform a logical AND at each match-line node. Unlike exact or ternary matching, a range matching is complete when the bit of the search-input data closest to the MSB is found which satisfies the range condition.

Fig. 7 shows an example of the operation of each match-line scheme with stacked RMCs, when the $\{\mathrm{OP0}, \mathrm{OP1}\}$ signals are $\{0, 1\}$, corresponding to a "less than or equal to (LE)" operation. The PF-CDPD match-line scheme produces a false result due to the characteristic of the RMCs, as shown in Fig. 7(a). A domino match-line scheme gives correct results as shown in Fig. 7(b), but it is too slow in a stacked configuration, because the matching result has to pass through all the stacked NMOS when all the search-input data and the stored range data are exactly equal.

To speed up matching, we propose a pre-discharging match-line (PDML) scheme with the structure shown in Fig. 7(c). During the match-line precharge phase, the PCG signal goes low and the search-input data is loaded into each RMC at the same time. Then the internal node Si is precharged. The transistor Ni prevents the node Si from connecting to the ground through the range-matched RMC during the precharge phase. During precharge phase, each RMCs evaluate the search-input data with the stored range data. After precharge phase, the PCG signal goes high and the matching result outputs on the node OUT in Fig. 7(c).

When all the search-input data are equal to the stored data, the evaluation result passes through the longest path. In the PF-CDPD match-line scheme, each match-line node reaches ground level in this case. This phenomenon, which has been called the pseudo-ground effect [13], enables the PF-CDPD match-line scheme to achieve a reduced discharging time and faster matching, as shown in Fig. 9.

In order to take advantage of the PF-CDPD match-line scheme, an additional NMOS transistor PN is attached in parallel to the bottom of the NMOS stack in the PDML match-line scheme, as shown in Fig. 7(c). During the precharge phase, PN is turned on by the signal PCGb which is the inverse of PCG. If the search-input data is exactly equal to the stored range data, all the RML nodes are discharged to the ground during the precharge phase. By pre-discharging the RML nodes, the matching speed can be reduced dramatically. The critical issue of the PDML scheme is charge-sharing problem when the RMCs are stacked in the PDML scheme. By following a design procedure in [13], we can determine the maximal number of stacked RMCs as 6 with the 0.13-μm process.

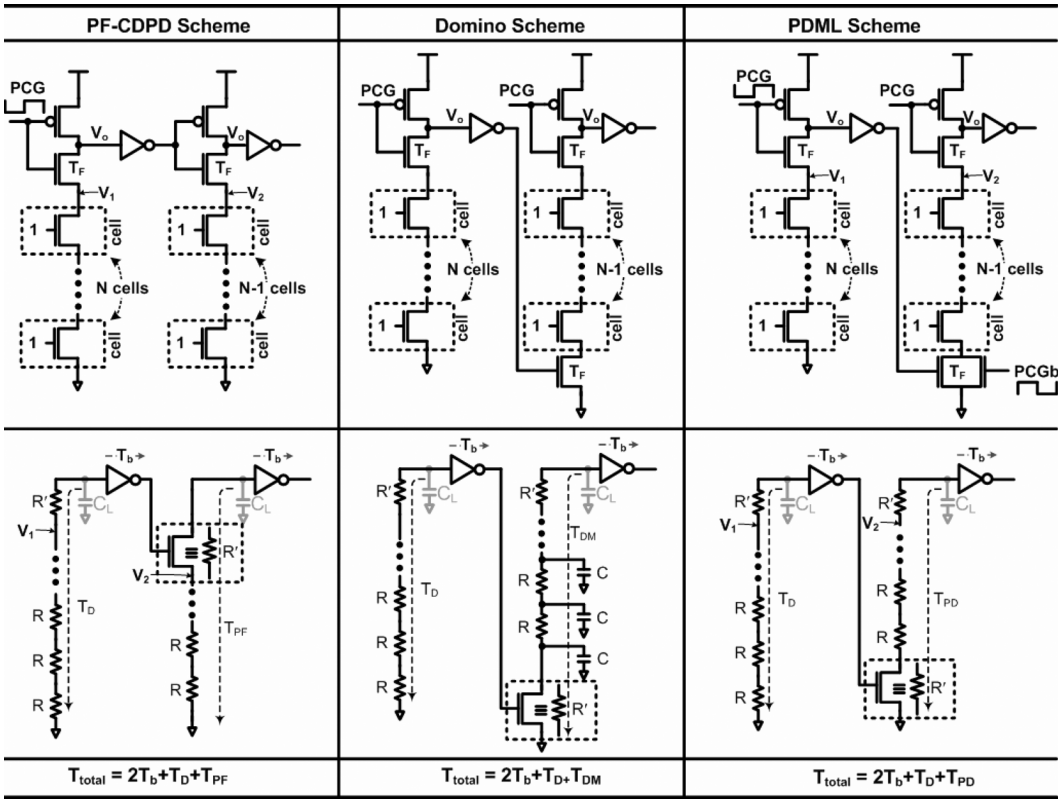


Fig. 9. Match-case evaluation and calculated delays of the PF-CDPD, the Domino, and the PDML schemes.

To facilitate the analysis of the match-line schemes, our analysis is based on the model shown in Fig. 9, which is composed of 2 stages, each with N RMCs and $N-1$ RMCs. The worst-case evaluating time in the model occurs when all the stored data of RMCs are matched with search-input data, regardless of range operators. Since all the RML nodes, in the PF-CDPD scheme and the PDML scheme, are discharged during precharge phase in this case, the nodes $V_{1,2}$ are being pulled toward ground. Therefore, this results in pseudo ground during precharge phase [13]. In contrast, charge of each RML nodes is held in the second stage of the Domino scheme, as shown in Fig. 9. The charge degrades the evaluating speed due to discharging time of each RML node. In this model, the stacked NMOS transistors are sized with equal width. Therefore, the discharging-delay time T_D, T_{PF}, T_{DM}, and T_{PD} for evaluation can be easily calculated using the Elmore delay rules [14], [15] as follows

$$T_D = 0.69 \times (NR + R') \times C_L \tag{1}$$

$$T_{PF} = 0.69 \times [(N-1)R + R'] \times C_L \tag{2}$$

$$T_{DM} = 0.69 \times \left[NR'C + \frac{N(N-1)}{2}RC + [2R' + (N-1)R] \times C_L\right] \tag{3}$$

$$T_{PD} = 0.69 \times [(N-1)R + 2R'] \times C_L = T_{PF} + 0.69R'C_L \tag{4}$$

where C_L equals the total capacitance at V_o in Fig. 9 and C is drain/source capacitance of the stacked NMOS transistors. Since stacked NMOS transistors have reduced gate overdrive with $V_{DD} - V_t$, their turn-on resistance is larger than that of transistor T_F which is fully turned on. Therefore, the resistance of stacked NMOS transistors is modeled as R while the resistance of T_F is modeled as R'. In this configuration, delay of the PDML scheme is increased by as much as $0.69R'C_L$, compared with the PF-CDPD scheme. Because the delay term of $R'C$ is small, our PDML match-line scheme enhances the matching speed just like the PF-CDPD scheme. When we compose M stages, first stage with N RMCs and others with $N-1$ RMCs, delays calculated from this equation are given in Table IV.

TABLE IV
MATCHING DELAY CALCULATED FROM FIG. 9

Match-Line Scheme	Matching delay
PF-CDPD	$T = MT_b + T_D + (M-1)T_{PF}$
Domino	$T = MT_b + T_D + (M-1)T_{DM}$
PDML	$T = MT_b + T_D + (M-1)T_{PD}$

Fig. 10 shows the post-layout simulated waveform for each match-line scheme, consisting of 16-bit cells, in fully exact matching and range matching. The PF-CDPD scheme is simulated with conventional TCAM cells for correct operation. The 16-bit RMCs or TCAM cells are divided into 3 cascaded stages, consisting of 6, 5 and 5 cells, respectively. In this case, the evaluating times of the PF-CDPD scheme, the Domino scheme, and the PDML can be calculated as follows:

$$T_{PF-CDPD} = 3T_b + T_D + 2T_{PF} \tag{5}$$

$$T_{\text{Domino}} = 3T_b + T_D + 2T_{DM} \tag{6}$$

$$T_{PDML} = T_{PF-CDPD} + 1.38R'C_L. \tag{7}$$

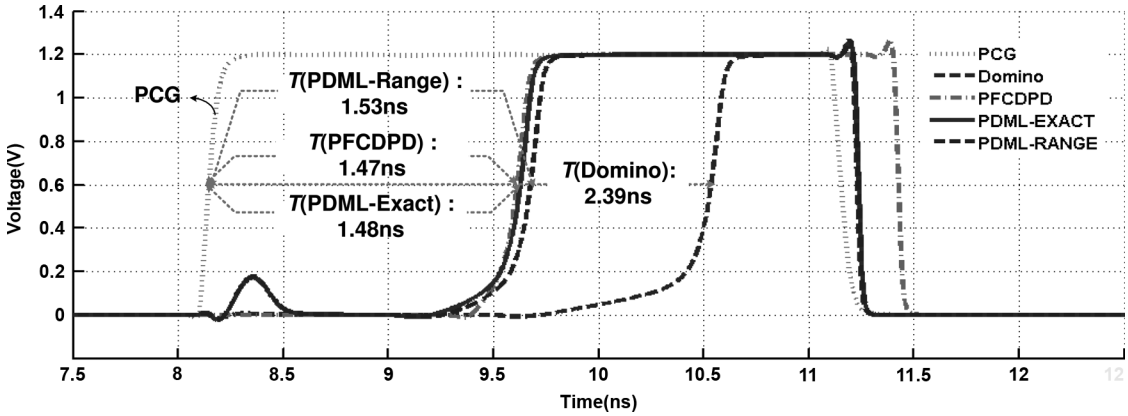
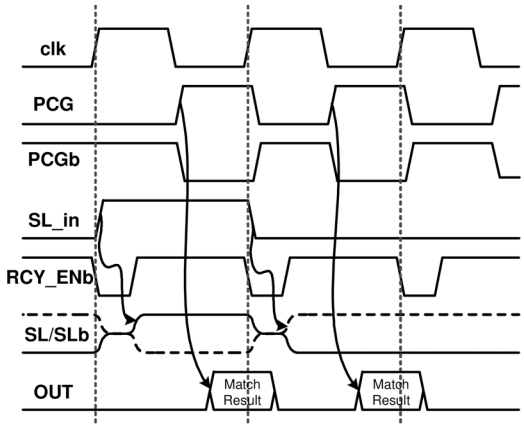


Fig. 10. Post-layout simulated waveform for full exact matching and RM in the worst case.

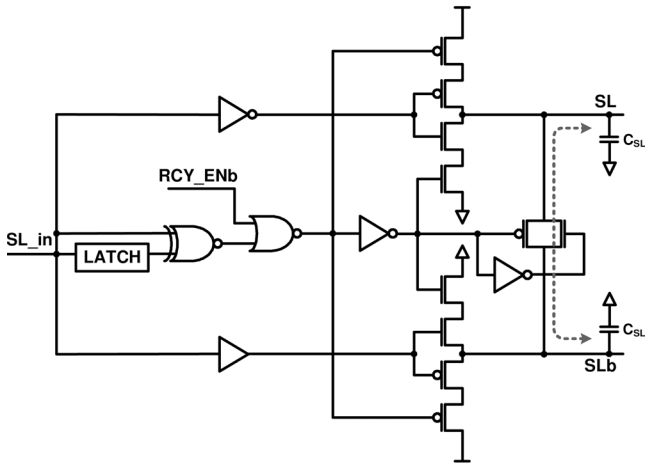
TABLE V
SIMULATED MATCHING DELAY AND ENERGY

Match-Line Scheme	Matching delay (ns)	Energy (fJ/bit/search)
Domino	*2.39*	*1.05*
PF-CDPD	*1.47*	*0.73*
PDML(Exact)	*1.48*	*1.53*
PDML(Range)	*1.53*	*1.58*

Although the PDML scheme is slower by $1.38\mathrm{R}'C_L$ compared with the PF-CDPD scheme in this case, it is still a dramatic improvement compared with the Domino scheme. As a different worst case, we can consider a range match case when the LSB has a range match and the others have an exact match, for example, a search-input data is 0xFFFF and a stored data is 0xFFFE when the operator is GE. In this case, the calculated delay T_{PDML} is not changed because the operation of discharging is same with the case of exact match. However, the simulated results show that the range-match case is lagged because the pseudo ground effect becomes weaker due to an increased series resistance by the transistor T3 in Fig. 6(a). In addition, the worst-case range matching more consumes power in the exact match case. Nevertheless, the PDML scheme achieves a similar matching speed as the PF-CDPD scheme, whereas the domino scheme is much slower. However, the PDML scheme consumes more power than the other types of match-line schemes. Table V shows the measured worst-case matching delay and energy of 16-bit RMCs on a 256×64-bit macro, in case of exact and range matching, respectively.



(a)



(b)

Fig. 11. (a) Timing diagram of the charge-recycling driver and (b) Circuit diagram of the charge-recycling driver.

IV. CHARGE RECYCLING SEARCH-LINE DRIVER

Conventional TCAMs consume a lot of power in their highly capacitive search lines, since they require precharging at every lookup [16]. The pulsed NAND–NOR CAM (PNN-CAM) [17] uses a charge-recycling driver with a replica entry which controls the precharging timing and minimizes static power consumption.

However, the PDML scheme with RMCs can be directly applied to the charge recycling driver without employing any extra circuits, such as a replica entry [17]. The PDML match-line scheme decouples match-line precharging from the setup of the search-input data. During the precharge phase, the Ni in Fig. 7 is turned off by the PCG signal and the search-input data is loaded into each cell by the charge-recycling driver. Only when the search data changes, the charge-recycling driver draws current from the supply after recycling, as shown in the timing diagram of Fig. 11(a). Assuming that the transition probability of the search line is 0.5, the power consumption of the search lines

TABLE VI
PERFORMANCE SUMMARIES OF DIFFERENT TCAM MACROS

Approaches	PF-CDPD	PF-CDPD (DRES)	RM-TCAM
Reference	[13]	[8], [13]	this work
Macro capacity	256×64	256×72	256×64
Configuration	64-bit NAND cells	72-bit NAND cells	48-bit NAND cells + 16-bit RMCs
Cell area (μm^2)	20.1	20.1	20.1 (NAND) 16.6 (RMC) 15.0 (OC) 9.1 (ACC)
Entry area (μm^2) (cells + precharge circuit)	1,382.4	1,561.2	1,361.0
Macro area (μm^2) (*normalization*)	355,180.3 (*1.02*)	401,119.4 (*1.15*)	349,292.3 (*1.0*)
Match-line energy (match case) (fJ/bit/search)	0.73	0.73	0.73 (NAND) 1.58 (RMC)
Match-line energy (mismatch case) (fJ/bit/search)	0.49	0.49	0.49 (NAND) 1.09 (RMC)
Search-line energy (fJ/bit/search)	0.31	0.31	0.31 (NAND) 0.33 (RMC)
Per-Entry Energy (match case) (fJ/entry/search)	66.56	74.88	80.48
Per-Entry Energy (mismatch case) (fJ/entry/search)	51.20	57.60	61.12
Search time (ns)	1.93	2.11	1.99

is theoretically 50% of that of a non-precharged TCAM [16]. But the saving is actually reduced to 40% by the control overhead of the driver. Fig. 11(b) shows the circuit diagram of the charge recycling driver.

V. PERFORMANCE COMPARISONS

Previous works [18] and [8] report the average storage expansion ratio of conventional TCAMs as 2.32 and 4.21 in real-world routers, respectively. The RM-TCAM with RMC can improve the storage expansion ratio of 1.01 for the rule sets of [8], as already set out in Table II.

To make a fair comparison in terms of the die area and power consumption, we implement three types of TCAMs, including our new design, using 0.13-μm process, as shown in Table VI. All the TCAMs have a charge-recycling driver. To support prefix matching and range matching, an entry of RM-TCAM is composed of 48-bit NAND-TCAM cells and 16-bit RMCs. The PF-CDPD TCAM with DRES has an additional 8-bit TCAM cells, because it needs extra bits for range encoding. The RM-TCAM is more efficient in die area and searching speed than the PF-CDPD TCAM with DRES, although the former uses more power for the same capacity, as shown in Table VI. The improved storage expansion ratio allows more favorable view of the power consumption. To see how the improved effect of the storage expansion ratio affects in power consumption and die area, we apply the implemented TCAMs to the real-world rule sets in [8] and we measure the total

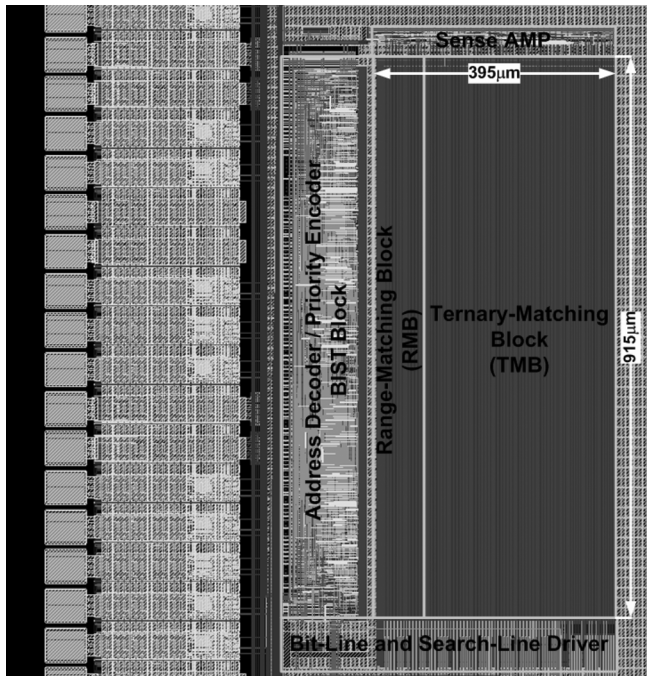


Fig. 12. A 256×64-bit layout of the proposed range-matching TCAM with dynamic match-line RMC and charge recycling-driver.

energy consumption. In this case, the storage expansion ratio can directly affect the search-line power consumption and the required die area. For example, the PF-CDPD TCAM with DRES requires 341 entries to support rule set A due to range expansion. When only an entry is matched with search data and 340 entries are mismatched, the PF-CDPD TCAM consumes $[74.88 + 57.60 \times 340] = 19{,}658.9$-fJ/search energy with 531,401.3-μm^2 die area. However, the RM-TCAM can support rule set A with 282 entries. Therefore, RM-TCAM consumes $[80.48 + 61.12 \times 281] = 17{,}255.2$-fJ/search energy with 383,510.2-μm^2 die area. Since the increased number of entry results in increasing power consumption in the search line and expanded entry, the total power of the PF-CDPD TCAM using DRES is increased, as shown in Table VII. The RM-TCAM can increase the efficiency in terms of power consumption and die area, on the average, by factors of 1.16 and 1.27 compared with the PF-CDPD TCAM using DRES, respectively. In addition, the RM-TCAM can directly store and update the rule sets without any additional devices, whereas the DRES approach uses an additional DRAM or SRAM for range encoding, and requires a complicated update algorithm.

The RMB of the RM-TCAM can be implemented as a static or dynamic RMC, depending whether low power consumption or small area is more important. We performed post-layout simulations to compare these structures. To provide a fair comparison, only a range-matching block, consisting of 256×16-bit entries with RMCs, was evaluated. Table VIII shows the trade-off in terms of energy, matching speed, and die area.

The dynamic RM-TCAM achieves 1.99-ns search times, and its energy requirement is 80.48 fJ/entry/search in the range matching case. Fig. 12 shows the layout of the 256×64-bit

TABLE VII
PERFORMANCE COMPARIOSNS ON THE REAL-WORLD RULE SETS IN [8]

Rule Set (Area : μm^2) (Energy : fJ/search)	A		B		C		Average *(normalized)*	
	Area	Energy	Area	Energy	Area	Energy	Area	Energy
PF-CDPD [13]	1,311,897.6	48,604.2	764,467.2	28,329.0	2,264,371.2	83,881.0	1,446,912.0 *(3.900)*	53,604.7 *(3.565)*
PF-CDPD (DRES) [8], [13]	531,401.3	19,658.9	379,980.5	14,071.7	506,952.9	18,737.3	472,778.2 *(1.274)*	17,489.3 *(1.163)*
RM-TCAM (Dynamic RMC)	383,510.2	17,255.2	362,891.4	11,326.6	366,484.4	16,521.8	370,962.0 *(1.000)*	15,034.5 *(1.000)*

TABLE VIII
COMPARISONS BETWEEN STATIC AND AND DYNAMIC MATCH-LINE RMCS

Statistic	Static RMC	Dynamic RMC
Configuration (256×16b)	*1 stage (16-b stacked RMCs)*	*3 stages (6, 5 & 5-b stacked RMCs)*
Macro Area(μm^2) (normalized)	*50,810 (1.00)*	*38,100 (0.75)*
Energy(fJ/bit/search) (normalized)	*1.02 (1.00)*	*1.58 (1.55)*
Search Time (ns) (normalized)	*1.85 (1.00)*	*1.53 (0.83)*

RM-TCAM with its charge-recycling driver and dynamic match-line RMCs.

VI. CONCLUSIONS

We have proposed a novel range-matching TCAM (RM-TCAM) with a dynamic range-matching cell (RMC), which provides range operators that allow the die area to be reduced by factors of 3.90 and 1.27, on average, compared with a PF-CDPD TCAM as a conventional method without range encoding scheme and a PF-CDPD TCAM with DRES, respectively. In addition, the RM-TCAM uses 3.57 and 1.16 less power, on average, than a PF-CDPD TCAM and a PF-CDPD TCAM with DRES, respectively. Furthermore, the RM-TCAM requires no external devices, whereas the TCAM using DRES uses an external DRAM or SRAM for range encoding. A novel pre-discharging match-line (PDML) scheme has also been proposed to increase the speed of operation. Combining this scheme with a dynamic RMC the matching speed can be improved by up to 17% as well as occupy a 25% less die area than the static match-line scheme. A prototype RM-TCAM, constructed using RMCs and the PDML scheme, has been designed as a 256×64-bit macro in a 0.13-μm 1.2-V CMOS process. The RM-TCAM achieves a 1.99-ns search time and its energy consumption is 1.26 fJ/bit/search, with the range-matching block achieving a 1.58-ns search time.

ACKNOWLEDGMENT

The authors would like to thank anonymous reviewers for providing constructive comments to improve the quality of this paper. Also, we wish to acknowledge the insightful discussions on this work to J.-Y. Park, H.-S. Song, and J.-H. Lee. The support of IDEC (IC Design Education Center), by the provision of CAD tools, and the support of ISRC (Inter-university Semiconductor Research Center) are gratefully acknowledged.

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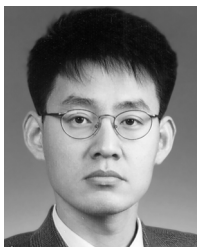

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