Fully Ion-Implanted InP JFET with Buried p-Layer

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***Abstract*—A buried p-layer has been successfully implemented in a fully ion implanted InP JFET for the first time. Using Be co-implanted with Si, a sharp channel profile is obtained. The saturation current has been reduced and the pinch-off characteristic has been improved with a slight decrease in transconductance and cutoff frequency. The equivalent circuits for the JFET with and without the buried p-layer are compared.**

I. Introduction

In GaAs MESFET fabrication, buried p-layers have been introduced to improve the threshold-voltage uniformity [1], [2], to alleviate the short-channel effects [3], to suppress the drain conductance transients [4], and to enhance the immunity to radiation [5].

The fabrication of fully implanted InP JFET's [6] requires a higher energy channel implant than that of GaAs MESFET's, because the channel exists under the p^+-gate rather than under the gate metal. The higher energy implant results in larger channeling tails which are further broadened by diffusion during the high-temperature activation cycle.

While higher channel doping can be effective in enhancing device characteristics [7], it also raises the saturation current and makes the pinch-off voltage of the depletion-mode device more negative. These changes are undesirable for low-power analog or digital switching applications.

In this paper, we report on the first application of the buried p-layer to the fabrication of a fully implanted InP JFET to obtain devices with low saturation current and small pinch-off voltage without affecting other aspects of them.

II. Buried P-Implant

First the channel doping profile was evaluated. A deep Be implant was used to form the buried p-layer under a Si channel implant. Fig. 1 shows the doping profiles obtained from a Polaron electrochemical profiler. When the 220-keV Si implant was used alone with a dose of 1×10^{13} cm^{-2}, the profile had a broadened tail as in curve (*a*). When a 150-keV Be was co-implanted, the profile became abrupt. For a dose of 5×10^{12} cm^{-2} (shown by curve (*b*)), a p-doped layer was detected under the n-channel. For a reduced dose of 1×10^{12} cm^{-2} (shown by curve (*c*)), however, the p-layer was absent through compensation and carrier depletion by the built-in junction potential.

In fabricating the JFET, a procedure identical to that described in [6] has been used except that the buried Be implant was added during the channel implant step. Fig. 2 shows a schematic cross-sectional view of the buried p-layer InP JFET. The p-layer is dotted to show that all the charges there are depleted.

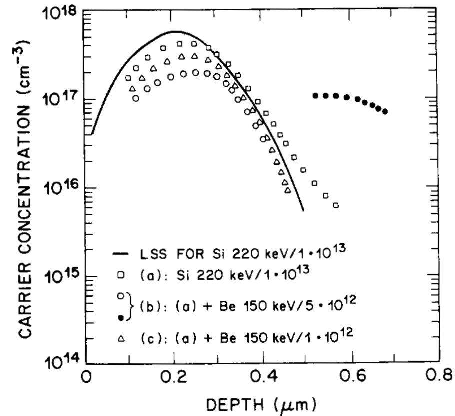

Fig. 1. Channel doping profiles measured using Polaron profiler: (*a*) when Si 220 keV/1 × 10^{13} cm^{-2} implant was used alone; (*b*) when Be 150 keV/5 × 10^{12} cm^{-2} was co-implanted; and (*c*) when Be 150 keV/1 × 10^{12} cm^{-2} was co-implanted. The filled circles represent the p-type buried doping found in (*b*). Also shown is the LSS profile for (*a*).

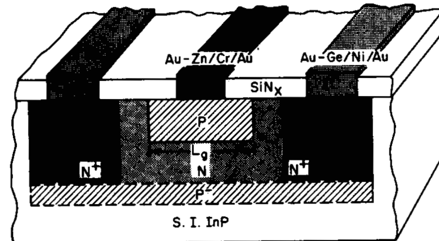

Fig. 2. Cross-sectional view of the InP JFET fabricated with buried p-layer.

III. Device Results

Fig. 3(a) and (b) shows the typical current–voltage characteristics of the FET's fabricated without and with the buried p-layer, respectively. The FET's had a gate of 1.5 μm length and 100 μm width. The standard (without buried p-layer) FET had a saturation current of 150 mA/mm and a pinch-off voltage of −3.2 V, while those of the buried p FET were 65 mA/mm and −1.7 V, respectively. The transconductance g_m, however, has been degraded slightly from 90 to 70 mS/mm. This may be due to the slight decrease in doping concentration (Fig. 1). Our Hall measurement showed little change in the channel electron mobility with the buried p-implant. The degradation

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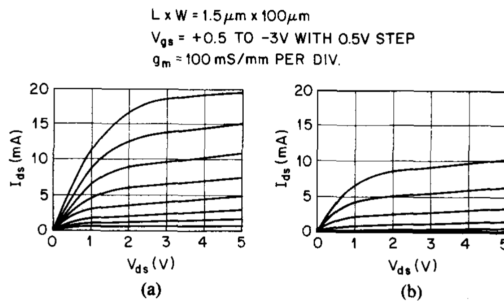

Fig. 3. FET I-V characteristics for JFET's (a) without and (b) with buried p-layer. The FET had a gate width of 100 μm.

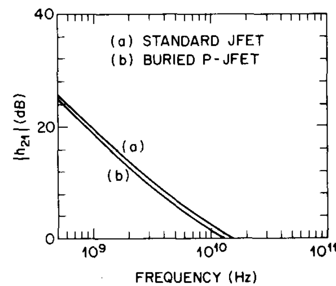

Fig. 4. Short-circuit current gain (h_{21}) of the JFET's (a) without and (b) with buried p-layer. The unity gain frequency is 10 GHz for (a), and 8 GHz for (b).

of g_m is responsible for the small reduction in the unity gain cutoff frequency f_T from 10 to 8 GHz as can be seen in Fig. 4. The short-circuit current gain (h_{21}) was calculated from microwave S-parameter measurements using a wafer prober from Cascade Microtech connected to a HP 8510 network analyzer.

From the same set of data, the parameters for the equivalent circuit of the JFET in Fig. 5 were derived using an optimization program [8] and tabulated in Table I. Except for g_m, the two equivalent circuits are very similar to each other, with the difference within the measurement error. The gate resistance R_g in both devices is relatively large because of high p-contact resistance in the gate. The p-ohmic metal and p-layer itself add extra gate resistance, but these are much smaller than contact resistance. It should also be noted that the parasitic capacitances are basically unchanged, which confirms that the buried p-layer is totally depleted.

IV. Conclusions

A fully implanted InP JFET has been fabricated for the first time with a buried p-layer. The saturation current and the pinch-off voltage have been drastically reduced, beneficial for low-power applications. The transconductance and the cutoff frequency have been slightly degraded with the equivalent circuit basically unchanged otherwise.

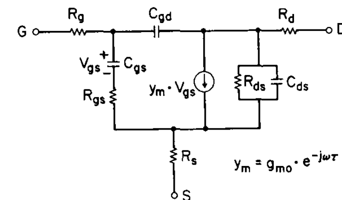

Fig. 5. Equivalent circuit for the JFET's.

TABLE I
Equivalent Circuit (in Fig. 5) Parameters for the Standard JFET and the JFET with Buried p-Layer. The Widths of the JFET's were 100 μm.

	C_{gs} [fF]	C_{gd} [fF]	C_{ds} [fF]	R_g [Ω]	R_d [Ω]	R_s [Ω]	R_{gs} [Ω]	R_{ds} [Ω]	g_m [mS]	τ [ps]
Standard	106	23	30	137	15	22	11	651	9.4	6.7
Buried p	90	28	20	146	20	29	13	752	7.3	8.1

Acknowledgment

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