Three-Stage InP JFET Amplifier for Receiver Optoelectronic Integrated Circuits

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Abstract—**Three-stage InP JFET amplifiers have been fabricated on semi-insulating InP using ion implantation. The amplifiers show dc gain of 43–65 calculated from amplifier transfer characteristics. From high-frequency measurements, a 3-dB bandwidth of 400 MHz and a gain of 38 have been measured from the amplifiers.**

InP JFET's have been integrated with InGaAs p-i-n diode for receiver optoelectronic integrated circuits (OEIC's) [1], [2] since JFETs offer the potential of high performance for long wavelength OEIC's. These receiver OEIC's used single stage amplifiers and were limited in performance because of the relatively low voltage gain. Using multistage high gain amplifiers, performance comparable with that of hybrid receivers is expected. In this letter, we report dc and ac performance of three-stage InP JFET amplifiers fabricated on semi-insulating InP substrates. The amplifiers utilized fully ion-implanted InP JFET and were designed to have a gain $>$ 30 and a bandwidth $>$ 350 MHz, making them suitable for use in 600 Mb/s receiver OEIC's.

The processing steps of InP JFET's were described in an earlier paper [3]. Si was implanted at 220 keV with a dose of 8×10^{12} cm^{-2} for the channel and 130 keV with a dose of 10^{13} cm^{-2} for the ohmic contact layer. For p^+ gate, As/Be coimplantation was performed. The wafers were activated at 850°C for 15 s using a capping layer of borosilicate glass. Ohmic contacts were made using Au-Ge/Ni/Au for n-InP and Au/Au-Zn/Cr/Au for p-InP and then alloyed at 440°C for 40 s.

Fig. 1 shows current-voltage characteristics of a typical 1.6 μm gate InP JFET for the gate width of 100 μm. A maximum transconductance of 90 mS/mm and an output conductance of 4–5 mS/mm were obtained. A cutoff frequency of unity current gain of 10 GHz was measured in InP JFET's with the same gate size [4]. The drain saturation voltage at zero gate voltage was approximately 2 V which is greater than the typical value for GaAs MESFET's. This difference is ascribed to the fact that InP needs a higher electric field to reach the saturation velocity than GaAs. Low gate leakage current of less than 10 nA was observed for gate voltage of -5 V. A turn-on voltage of 1.5 V and a series resistance of 50 Ω were

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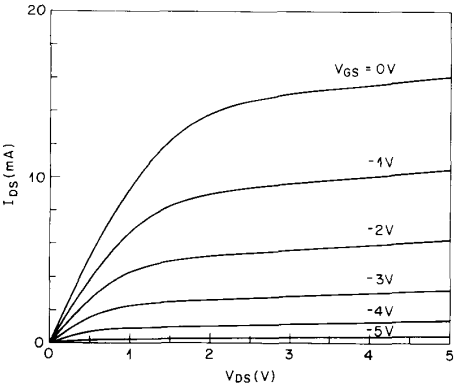

Fig. 1. Drain current-voltage characteristics of a typical InP JFET with a drain saturation current of 150 mA/mm.

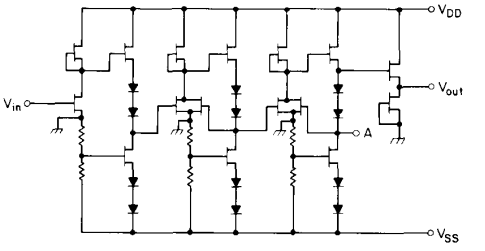

Fig. 2. Circuit diagram of three stage amplifier.

measured in the diode having a dimension of 5 $\times$ 50 μm. This diode was used for the level shifting stages of the amplifier.

The circuit diagram of the three stage InP JFET amplifier is shown in Fig. 2. Each stage consists of a gain stage and a level shifting buffer stage, which is similar to the previously reported symmetrical amplifier [3]. In this circuit, two resistors were used for a voltage divider instead of using FET's and localized negative feedback was added to the second and third stages to make the overall gain less dependent on the JFET characteristics and to minimize phase shifts. Wide InP JFET's were added for an output buffer stage capable of driving a 50 Ω load. In addition to the buffered output, a second output is available at node A. Since the quiescent voltage at this node is zero, it can be connected to the input through a feedback resistor to convert the amplifier to a transimpedance receiver. While all InP JFET's have 1.6 μm gate length, different gate widths were used from 30 to 300 μm. All diodes in the level shifting stages have the same size of 5 $\times$ 30 μm. A gain of 5–7 in the first stage can be expected from [3]. In the second and the third stage, an expected gain of

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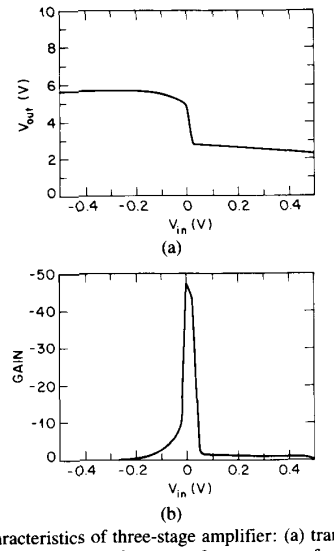

Fig. 3. DC characteristics of three-stage amplifier: (a) transfer characteristics and (b) gain calculated from transfer curve as a function of V_{in}.

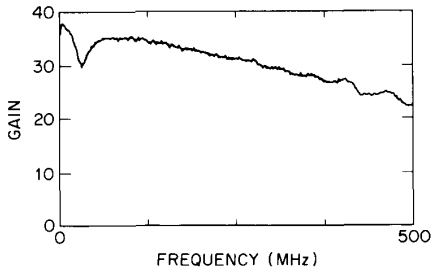

Fig. 4. Frequency response of a typical three-stage amplifier.

each stage was 2.5–3. Therefore, a total gain of the three stage amplifier will be 31–63. The additional gain afforded by a three stage over single stage amplifier is expected to improve the optical sensitivity by ~3 dB [5]. Although lower noise operation can be achieved with HEMT's than with JFET's, the increased material and processing complexity is not warranted for many applications.

The measured transfer characteristics and the gain of a typical three stage amplifier are shown in Fig. 3 for $V_{DD} = 8$ V and $V_{SS} = -11$ V. Amplifiers could be operated with symmetrical power supply voltages larger than 7 V, which is consistent with the turn-on voltage of two diodes and the drain saturation voltage. The total gain measured in the fabricated amplifiers was in the range of 43–65. These values are close to the expected total gain by simple calculation. The maximum gain did not occur at zero input voltage for symmetrical supply voltage ($V_{DD} = -V_{SS}$). This asymmetry is due to some resistance being inadvertently present in the source-ground connection of the first stage inverter and it has been corrected in a subsequent redesign. Nonetheless, high gain centered around $V_{in} = 0$ V can be obtained by using asymmetrical supply voltages.

The packaged amplifiers were mounted into a microwave fixture for the measurement of frequency response using an HP 4195A network analyzer. Capacitors of 2000 pF were mounted on the same package for power supply decoupling. From the measured frequency response shown in Fig. 4, a 3 dB bandwidth of 400 MHz is deduced with $V_{DD} = 10$ V and $V_{SS} = -9$ V (the dip in the gain at ~35 MHz is an artifact due to inadequate power supply decoupling).

In conclusion, three-stage amplifiers have been successfully demonstrated using fully ion-implanted InP JFET's. The measured total gain is in the range of 43–65. A 3 dB bandwidth of 400 MHz was measured in the packaged amplifier. High performance receiver OEIC's can be realized using this three stage amplifier.

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