High-Speed Signal Switching with a Monolithic Integrated p-i-n/Amp/ Switch on Indium Phosphide

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Abstract—Operation of an optoelectronic integrated circuit which includes two p-i-ns, preamplifiers, 2 × 2 crosspoint switch, and output buffers has been demonstrated. These circuits have been fabricated in semi-insulating InP:Fe substrates by vapor phase epitaxy and ion implantation using a planar horizontally integrated technology. Signals modulated at 150 MHz are shown to be switched at 15 MHz, with the circuits capable of detecting and passing data modulated at ~1 GHz.

INTRODUCTION

MODERN optical communication systems, in order to make full use of available bandwidth, multiplex information from many sources onto a single fiber. High-speed signals must then be switched for routing to and from their various original sources and final destinations. Switching rates may vary, from the duration of the connection, to a bit wise interleave. Monolithic integration of multiple network functions becomes a desirable goal as bit rates exceed 1 Gb/s or system complexity requires many simple optical and electrical operations be performed on data streams [1]. To address these applications we have monolithically integrated two InGaAs p-i-n photodetectors, JFET preamplifiers, a 2 × 2 crosspoint switch and output buffers on an InP substrate. This device allows an optical data stream to be detected, converted to an electrical data stream, amplified and dynamically directed to one of two buffered outputs capable of driving a 50 Ω load. InP is a desirable material system for high speed OEIC's because of its superior saturated electron velocity relative to Si and GaAs, and also its position as the material of choice for long wavelength photonic devices. Previous front end OEIC receivers based in InP typically are comprised of detectors with amplifiers [2]. We have developed a circuit which includes other functional elements capable of being connected to additional high-speed circuitry.

DESIGN

Fig. 1 shows a schematic of the circuit. Each input channel consists of a single InGaAs p-i-n diode biased in series with a
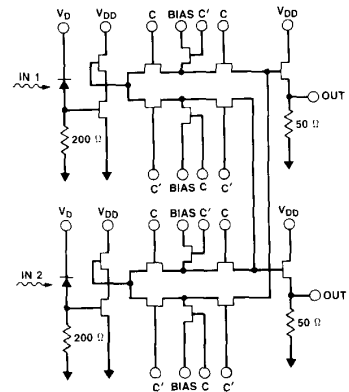
Fig. 1. Schematic of p-i-n/AMP/2 × 2 crosspoint switch–buffer circuit.

200 Ω load resistor and connected to a single-stage FET amplifier inverter. In order to optimize voltage gain, the preamplifier uses a matched pair of JFET's, one of which has the gate shorted to the source so as to act as an active load. The preamplifier output has a nominal output voltage of $V_{dd}/2$. Allowing for the capacitance of the p-i-n and FET gate junctions this input stage has an RC limit of approximately 5 GHz.

The output of each preamplifier is split into two alternate signal paths to output one and output two. Each path includes a series shunt switch [3]. This is a three-transistor cell made up of a series pass transistor to switch the signal transmission, a shunt transistor to reduce any capacitively coupled signal, and a second series pass transistor to prevent the shunt from loading the output. All three transistors are biased in the linear regime and act as variable impedances. With the shunt bias (V_{Bias}) set at $V_{dd}/2$, nominal values for the control voltage (V_c) and its complement (V_c') are $V_{dd}/2$ and 0 V/s, respectively. These values put the switch in the through state (input one goes to output one and input two goes to output two). In the crossed state (input one to output two and input two to output one) $V_c = 0$, $V_c' = V_{dd}/2$.

The output buffer consists of a single transistor source follower with a 50 Ω load. This is designed to have unity gain and give a nominal output voltage of $V_{dd}/2$ into a 50 Ω load.

FABRICATION

To minimize parasitic capacitance and allow for effective device isolation, the entire circuit is fabricated on a semi-insulating InP:Fe substrate. A cross section of the integrated p-i-n/FET structure is shown in Fig. 2. The p-i-ns are grown in recessed
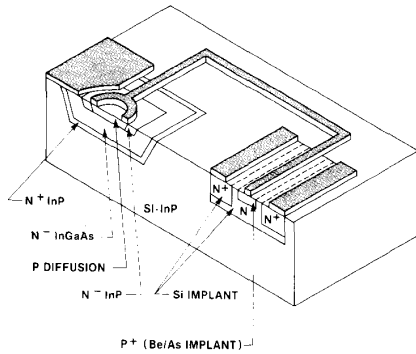
Fig. 2. Crossection of integrated p-i-n and FET structure. This illustrates both the p-i-n and FET technologies used.

wells using chloride vapor phase epitaxy. Epitaxial material outside the wells is subsequently removed and the wafer is planarized using reactive ion etching. The p-i-n structure includes a 1.5 μm multistep InP buffer including a heavily doped n^+ layer to facilitate n-side contacting, a 3 μm undoped InGaAs absorbing layer and a 0.5 μm undoped InP cap. A 75 μm diameter p-n junction is formed by zinc diffusion through the InP cap. Both p and n contacts are made to the top side of the wafer using Au-Zn and Au-Ge alloys, respectively.

FET's are formed directly on the semi-insulating substrate using nonself-aligned, patterned ion implantation [4]-[6]. Source and drain regions are Si implants of 3×10^{13} cm^{-2} at 220 keV. Gates are formed using 6×10^{13} cm^{-2} Be implanted at 80 keV, with an As coimplant at approximately the same depth. Because of their different functions, the amplifier/buffer FET's and the switch FET's receive different channel implants. The amplifier FET's are optimized for high transconductance and receive a high Si dose for the channel, 220 keV, 8×10^{12}. The switch FET's require a low pinchoff voltage and therefore the implant dose is lowered to 6×10^{12} cm^{-2}. Implants are activated with a dielectric cap using a rapid thermal anneal cycle of 850°C for 30 s. Resulting sheet resistances for the amplifier and switch channels are typically 500 and 700 Ω/sq, respectively. The integrated input and output load resistors are also formed by ion implantation.

The preamplifier FET's switch FET's, and buffer FET's have gate widths of 200, 100, and 400 μm, respectively. The input capacitance of the receivers and switches, including the p-i-n is still less than 2 pF which gives an RC limited bandwidth above 2 GHz. The output buffers are capable of driving a 50 Ω load as required for connecting to additional conventional high speed circuitry.

RESULTS

DC parametric component measurements were made on discrete devices processed on the same wafer as the actual circuits. Fig. 3 shows the characteristics of the amplifier-like and switch-like test FET's. Amplifier FET's have a transconductance (g_m) of 60 to 80 ms/mm at a source to drain saturation current (I_{dss}) of 190 mA/mm and have a cutoff frequency (f_T) of approximately 7 GHz. The switch transistors have a g_m of 35 ms/mm for an I_{dss} of 65 mA/mm with a f_T of 5 GHz. More importantly, the switch FET's had a source-drain impedance of 200 Ω in the on state and > 100 K Ω with the channel pinched off.

The preamplifiers have dc differential gains of as high as ≈ 10 for bias voltages (Vdd) between +5 and +10 V. However
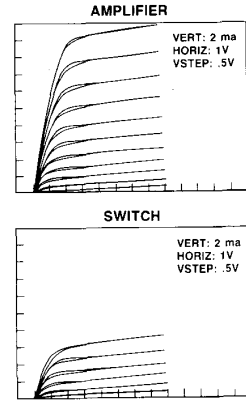

Fig. 3. Electronic characteristics of FET's used for switch and amplifier functions. The difference in saturation current is a result of different channel implants, chosen to optimize the different functional elements of the circuit.
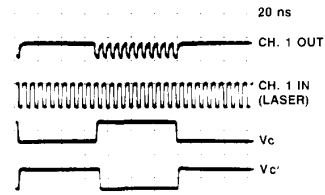

Fig. 4. Demonstration of the circuit switching capability. The output at channel 1 is shown while the signal from an optical input to p-i-n 1 is switched between channels 1 and 2.

voltage attenuation through the switch and buffer gives a net small signal gain of ≈ 4.5. The switching on-off ratio and crosstalk rejection was better than -20 dB using electrical probing of the inputs.

High-speed optical measurements were made on chips mounted in a high-speed test package. Bypass capacitors internal to the package were used to stabilize all dc lines. The optical input was a 1.3 μm AT&T Astrotek laser. Light from the single mode pigtail was focussed to a 50 μm diameter spot on the p-i-n. 50 Ω termination was not used for the control voltages V_c and V_c'.

Fig. 4 shows the switched output of channel 1 with a 150 MHz digital optical input to p-i-n 1. For a modulated light input of -20 dBm, the output is inverted with an amplitude of ≈ 8 mV with only slight distortion. The control voltages are switched at 15 MHz. For higher speed optical signals, the output becomes somewhat attenuated with a 3 dB roll-off by 1 GHz. The switching transition time is approximately 5 ns. For optical signals faster than 150 MHz there is some clipping of the first pulse after switching. At higher switching speeds, there is additional distortion and resonant-like behavior. This may be partly due to the lack of proper termination of the control voltage lines. Fifty Ω terminating resistors could easily be incorporated into the design of these circuits. In addition, on-board bypass capacitors for the dc bias and ground lines would be expected to improve the stability of these voltages under high speed operation.

CONCLUSION

In conclusion we have demonstrated monolithic integration of a two-channel optical receiver with an electronic crosspoint switch. The circuits showed relatively high speed switching of

high-speed signals. Photodetectors, resistors, and two function-ally different transistor designs were processed on a single semi-insulating substrate. This level of integration, 24 optical and electrical components, represents, to best of our knowledge, the highest level of integration in InP reported in the literature to date. Thus, ion-implanted InP JFET's appear to be a technology which can be engineered to produce devices optimized for specific applications. We expect that such functional elements and circuits can become building blocks for more complex switching systems.

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