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Edge Breakdown Suppression of 10 Gbps Avalanche Photodiode

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We have demonstrated a high-speed avalanche photodiode (APD) for a 10 Gbps optical communication system. To achieve a high gain-bandwidth product and reliable operation, the reduction of the multiplication layer thickness and an optimum design of the internal electric field distribution are essential. One- and two-dimensional analysis were done for this purpose. The suppression of edge breakdown can be achieved by precise control of the thickness of the multiplication layer and charge densities of the field control layer. Furthermore we suggest a junction curvature shape having negative curvature of the equi-potential line at the device edge. This new design successfully suppressed edge breakdown. The fabricated APD shows high current gain without premature edge breakdown, and a gain-bandwidth of above 80 GHz has been obtained.

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I. INTRODUCTION

InP-based avalanche photodiodes (APD) have been widely used for fiber optic communications because of their advantages of high current gain and high sensitivity. Much recent research has been focused on improving operational reliability [1,2] and a gain-bandwidth product [3], and reducing the excess noise factor [4,5].

In the early stages of long wavelength optical fiber communications, a Ge APD was widely used because of well-developed fabrication technologies. However the light absorption properties of germanium at 1550 nm are poor, and the rate of ionization coefficients is nearly equal to unity. The high electric field region is required to achieve avalanche multiplication, but the InGaAs material used for light absorption suffers from intolerably large tunneling leakage currents at high electric fields. For this reason, an InP/InGaAs APD with a separated absorption and multiplication (SAM) structure [6] has been proposed, to obtain higher gain and reduce tunneling current in the lower bandgap material of InGaAs. In this structure, an optical signal is converted into an electrical signal in the InGaAs absorption layer and goes through avalanche multiplication in the InP multiplication layer. A field control layer of moderately doped InP is inserted to maintain a low electric field in the InGaAs absorption layer while supporting a high field in the InP multiplication layer. Since the ionization coefficient of a hole is larger than that of an electron in an InP, the hole is usually chosen to be the type of injection carrier in order to reduce the excess noise factor. When photo-generated holes are injected from the absorption layer into the multiplication layer, a hole pile-up phenomenon has been found at the InGaAs-InP hetero-interface, which causes slow response and limits high-speed response of the APD device. This originates from valance band discontinuity and can be avoided by inserting mid-bandgap material nGaAsP, called the "grading layer" [7,8].

There are two critical issues for high speed APD. One is the reliability issue, and the other is how to obtain a high gain-bandwidth product. To solve the reliability issue, one must consider a planar structure. Due to finite-size planar positive-negative (p-n) junctions, there is a tendency toward enhancement of electric fields at the edge of the active area. These enhanced edge fields lead to larger gain at the device edges and premature "edge breakdown". The key to avoiding edge breakdown is to reduce the electric field intensity at the device edge. There have been many efforts to solve this problem. One of them is low doping density at the device edge to reduce the electric field. This can be done by ion implantation or diffusion of different dopant materials at the device edge, but it is difficult to control the maximum electric

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field in the n-InP layer and the hetero-interface. The second method is the regrowth of the epitaxial layer after selective etching of the field control layer at the device edge [9]. During the etching and regrowth process, there is some charge accumulation in the regrown interface, identified by silicon acting as a donor. This interface charge makes it difficult to fabricate APD devices reproducibly and reliably.

In the third approach, a junction of constant doping density is shaped to create a wider multiplication region with consequently lower electric fields in the peripheral region of the device. A floating guard ring is a similar concept to realize the planar structure [10,11]. Floating guard rings have the same doping as the central active region but are electrically isolated, which tends to lower the surface electric fields when the junction is biased. The widely used method for the planar type APD for higher gigabit systems is the use of a floating guard ring structure.

Itzler [12] proposed InP/InGaAs APDs manufacturable by using a multiple Zn diffusion process. In this scheme, the floating guard ring and the shaped junction profile created by double Zn diffusion are combined. An attractive aspect of this method is that the device can be fabricated by using a simple, mature diffusion process without regrowth or ion implantation, but the guard ring fabrication is very difficult for an APD having a high gain-bandwidth product. To obtain a high gain-bandwidth product, the multiplication layer has to be very thin, so that formation of the floating guard ring is very difficult. We can form the floating guard ring and the shaped junction profile simultaneously by recess etching and a single diffusion process. This makes the device more reliable and manufacturable. In this paper, we calculated electric fields and avalanche gain factors as a function of bias voltages and structural parameters. Two-dimensional analysis was done for the optimum floating guard ring structure design. Based on the results, an APD for 10 Gbps was fabricated and measured.

II. DESIGN AND SIMULATION RESULTS

A one-dimensional epitaxial layer structure and electric field model of APD are shown in Figure 1. An n-InGaAs absorption layer (region 3 in Figure 1), an n-InP field control layer (region 2 in Figure 1), an n-InP multiplication layer (region 1 in Figure 1), and a p^+ InP contact layer are assumed to be deposited on an n^+ InP substrate. Here, InGaAsP grading layers inserted between the absorption layer and the field control layer are assumed to be parts of the absorption layer. These p^+-i-n multiplication layer structures provide a uniform high electric field, which can increase the impact ionization collision rate of a hole. The ratio α/β even approaches unity, this could reduce the carrier running path length, transit time and avalanche build-up time in turn.

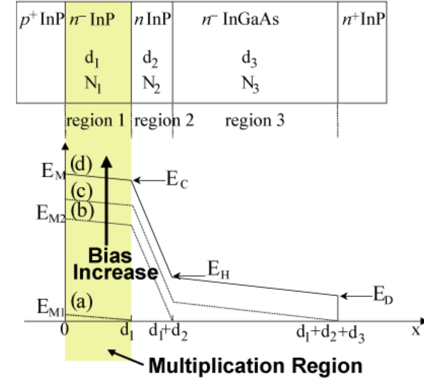

Fig. 1. Model of APD structure and electric field profiles.

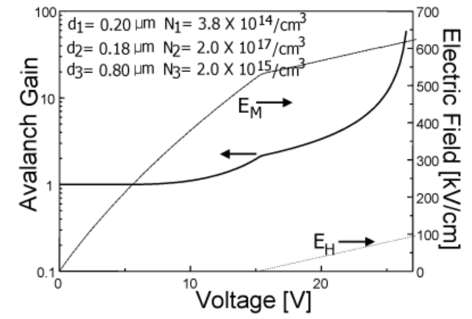

Fig. 2. Calculated E_M, E_H and avalanche gain factor as a function of bias voltages.

Let us assume that the x-coordinate is defined as shown in Figure 1, and a hole is injected at $x = d_1 + d_2$. Then the avalanche gain equation is given by

$$M = \frac{1}{1 - \int_0^W \beta \cdot exp\{\int_x^W (\alpha - \beta)dx\}dx}, \quad (1)$$

where $W = d_1 + d_2$.

It is our purpose to find a solution for the avalanche gain factor, M(V), as a function of bias voltage. The solution for the avalanche gain factor will provide the breakdown voltage (V_B) and other design parameters. Because the ionization coefficients are a function of the electric field, we must find the E(x)-V relation. To find the position-dependent electric field, the one-dimensional Poisson equation was solved and numerical calculation was carried out [13,14]. By using the parameters shown in Figure 1, the electric field has been successfully calculated as a function of bias voltage for a given layer structure. In the calculation, we used ionization coefficient data reported by Cook [15], and breakdown voltage defined as the voltage where gain exceeds 100. Figure 2 shows the calculated E_M, E_H and avalanche gain factor as a function of bias voltage.

Based on this model, we calculated breakdown voltages as a function of the multiplication layer width (d_1). Figure 3 shows the calculated breakdown voltages as a function of the multiplication layer width (MLW) for sev-

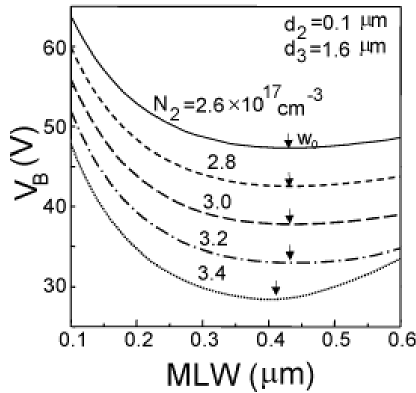

Fig. 3. Calculated breakdown voltages as a function of multiplication layer width and carrier densities of field control layer.

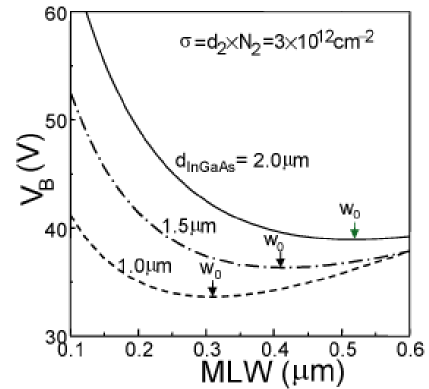

Fig. 5. Calculated breakdown voltages as a function of multiplication layer width for three cases of absorption layer thickness

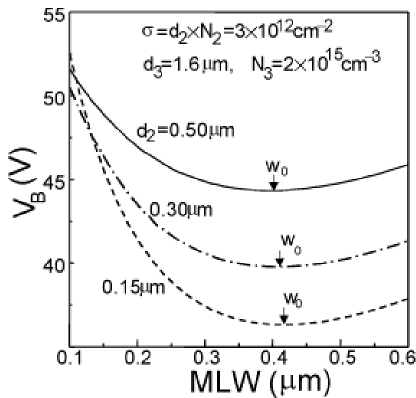

Fig. 4. Calculated breakdown voltages as a function of multiplication layer width and field control layer width.

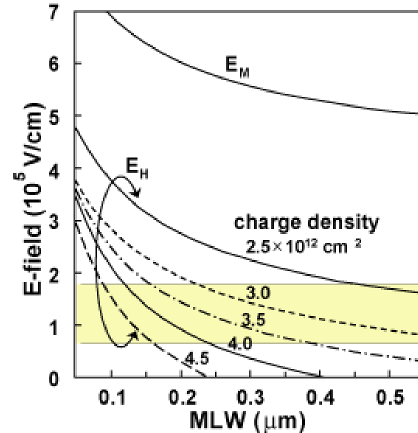

Fig. 6. E_M ad E_H curves at M = 100 as a function of MLW for different charge densities of field control layer.

eral carrier densities of the field control layer. Figure 4 shows the calculated breakdown voltages as a function of the multiplication layer width for three different cases of field control layer thickness. Breakdown voltage decreases as MLW increases from 0.1 μm to the minimum V_B, defined as w_0, while breakdown voltage increases as MLW increases in the region where MLW > w_0. Each curve has the minimum V_B marked with an arrow in the figure, and the minimum point w_0 is independent of the carrier density or the thickness of the field control layer.

In a design of APD with a shaped junction profile, the MLW at the active region is less than that at the device edge or periphery. Thus, if the MLW at the active region is less than w_0, then w_0 is always located between active region and device edge, where maximum gain is obtained. When the MLW at the device periphery is within w_0, the MLW at the device edge is greater than that at the device center in the active region, which means edge breakdown. Thus the MLW at the active region should be greater than w_0, to suppress the edge breakdown. Since a smaller MLW yields a higher gain-bandwidth product, we must find a structure having small w_0. As shown in Figure 3 and Figure 4, the minimum V_B depends neither on the carrier density nor on the thickness of the field control layer.

Figure 5 shows the breakdown voltage changes with the MLW for several cases of the InGaAs absorption layer thickness. The w_0 depends sharply on the InGaAs layer thickness. Figure 6 shows the E_M and E_H for M = 100 as a function of the MLW for several cases of charge densities of the field control layer. For stable operation and high performance, E_H should be sufficiently high to make photo-generated holes drift away, but should be low enough to suppress the tunneling and avalanche multiplication in the lower bandgap material InGaAs. This region is the shadowed band in Figure 6. For 10 Gbps operation, MLW should be less than 0.3 μm. From Figure 5, the InGaAs absorption layer thickness should be less than 1.0 μm, and charge density of the field control layer should be as high as 3.5×10^{12} /cm^2.

The effect of floating guard ring structure on the device performance was analyzed by solving the two-dimensional semiconductor equations. Figure 7 (a) shows the conventional floating guard ring, and Figure

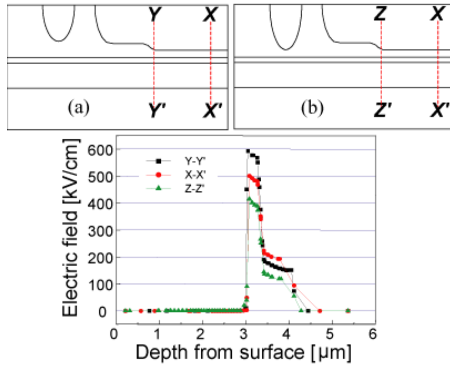

Fig. 7. (a) Conventional shallow floating guard ring and (b) proposed deep floating guard ring. (c) Electric field profile along the device.

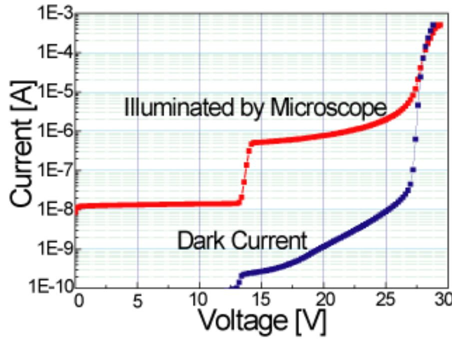

Fig. 8. Typical current-voltage characteristics of fabricated APD.

7 (b) shows the proposed deep floating guard ring. The deep floating guard ring has negative curvature of the equi-potential line at the device edge. Figure 7 (c) shows the simulated electric field profile over the device along the cross cut shown in Figure 7 (a) and (b). In the case of the deep floating guard ring, the electric field at the device edge is efficiently suppressed.

III. DEVICE FABRICATION AND MEASUREMENT

Metal-organic chemical vapor deposition (MOCVD) grown epitaxial wafers were used for the fabrication of the APD. An undoped InGaAs layer lattice-matched on an InP substrate was used for the absorption layer. Absorption layer thickness was reduced to 0.8 μm for 10 Gbps operation. The charge density of the field control layer was 3.5 $\times$ 10^{12} /cm^2 to increase the electric field in the InP multiplication layer for higher gain while maintaining a low electric field in the InGaAs absorption layer to avoid tunneling phenomena. InGaAsP grading layers are inserted to remove hole pile-up at the InGaAs-InP hetero-interface.

The p-junction is formed by the thin film deposition

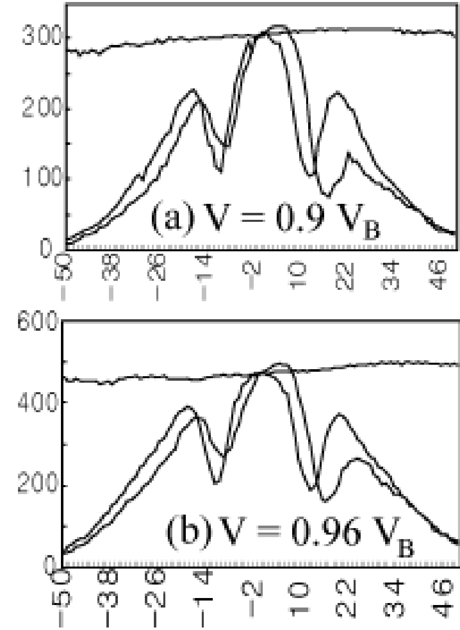

Fig. 9. two-dimensional gain profile across the devices.

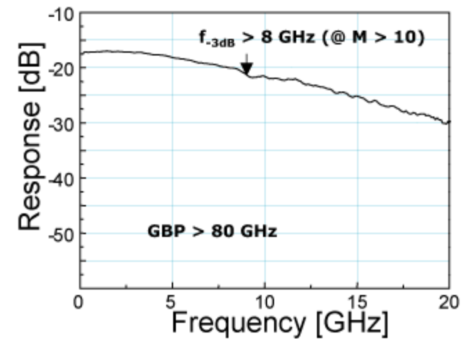

Fig. 10. Experimentally measured bandwidth of fabricated APD.

of ZnP composition followed by rapid thermal annealing. This process is the same as the method for manufacturing the reliable planar PIN photodiodes. The recessed junction profile was obtained by etching an InP top layer before Zn diffusion. This process needs no epitaxial regrowth or double-diffusion of Zn. The junction curvature can be obtained by well controlled reactive-ion etching (RIE) and single diffusion of Zn. The MLW of the center active region can be controlled to be less than 0.3 μm by adjusting the diffusion time, while the MLW of the device edge could be made greater than that of the center active region by RIE of the center active region. The difference of the MLW of the two regions can be controlled by RIE time. The floating guard ring region was also etched out to form a deep floating guard ring. To reduce the junction capacitance, back surface illumination geometry was introduced. Front p-metalization was made by using Ti/Pt/Au alloy. The Back surface of the device was thinned and polished. SiN$_x$ dielectric

layer was deposited on the back surface of the device to reduce the reflection of incident light from the air to the InP interface.

Typical current-voltage (I-V) curves of fabricated APD under dark condition and microscope lamp illumination are shown in Figure 8. The punchthrough voltage is 14 V and breakdown voltage is 27 V. From the I-V measurement we can expect that the MLW of the central active region is about 0.25 μm. Figure 9 shows the gain profiles measured across the fabricated APD. At 0.6 V_B, this device shows sufficient photocurrent and an avalanche gain factor higher than 2. Even M = 10 (V = 0.9 V_B) and M = 15 (V = 0.96 V_B) avalanche gain factors at the device edges are lower than those of the central active region. This is attributed to the strong guard ring structure of our new design and the exact analysis and tightly controlled fabrication process. The experimentally measured bandwidth of the devices shows that the APD has a gain-bandwidth product of above 80 GHz (Figure 10). Finally, 10 Gbps hybrid integrated receiver modules have been made by using this APD and pre-amplifier. The modules have shown a significant sensitivity improvement of at least 5 to 6 dB over similar receivers based on PIN photodiodes.

IV. CONCLUSIONS

In conclusion, we have demonstrated a high performance APD for 10 Gbps operation. One-dimensional electric field profile analysis was done for the optimum epitaxial layer design. From this analysis, optimum multiplication layer thickness and absorption layer thickness were found for stable operation. With this optimized epitaxial layer structure and the newly proposed deep floating guard ring structure, we have fabricated APD with high current gain without edge breakdown. The fabrication process needs only one growth and single diffusion of Zn, which makes the devices more reliable and reproducible. The fabricated APD shows a high gain-bandwidth product of above 80 GHz.

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