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Inkjet-Printed Silver Gate Electrode and Organic Dielectric Materials for Bottom-Gate Pentacene Thin-Film Transistors

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An inkjet-printed silver electrode and a spin-coated cross-linked poly(4-vinylphenol)(PVP) dielectric layer were used as a gate electrode and a gate insulator for a bottom-gate pentacene thin-film transistor (TFT), respectively. The printing and the curing conditions of the printed silver electrode were optimized and tested on various substrates, such as glass, silicon, silicon dioxide, polyethersulfone, polyethyleneterephthalate, polyimide and polyarylate, to produce a good sheet resistance of $0.2 \sim 0.4\ \Omega/\square$ and a good surface roughness of 2.38 nm in RMS value and 20.14 nm in peak-to-valley (P2V) value, which are very similar to those of conventionally-sputtered indium-tin-oxide (ITO) or thermally-evaporated silver electrodes. The coated PVP layer of metal/PVP/metal devices showed a good insulation property of 10.4 nA/cm^2 at 0.5 MV/cm. The PVP layer further reduced the surface roughness of the gate electrode to provide a good interface to the pentance layer. The pentacene TFT with a structure of glass/printed silver/PVP/pentacene/Au showed a good saturation region mobility of 0.13 cm^2/Vs and a good on/off ratio of larger than 10^5, which are similar to the performance of a pentacene TFT with a conventional ITO gate electrode.

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I. INTRODUCTION

Today, there are increasing demands for low-cost, rugged, thinner, lighter, bendable and/or possibly disposable electronic devices and circuits, which typically require development of low-cost, low-temperature fabrication processes that are compatible with flexible plastic substrates. Among many process methods, solution-based printing is one of the most promising ways to fabricate electronics at a very low cost and low temperature. Therefore, many researchers have studied materials and printing methods of solution-processable electrodes, insulators and semiconductors for all-printable thin-film transistors (TFTs) and TFT-based electronics applications [1–5].

Although many research groups have reported inkjet-based printable TFT results, the printed electrodes were used as gate electrodes in top-gate TFT structures [1,4, 6–8] or as source/drain electrodes in bottom-gate TFT structures having conventionally deposited and photolithographically patterned gate electrodes [9, 10] because the surface roughness of an inkjet-printed layer is generally too rough to be used for a gate electrode in the bottom-gate TFT structure [2, 6]. However, if the printing conditions are carefully optimized and/or a planarization gate insulator is used, a good TFT performance can be obtained from the bottom-gate TFT structure. All-printed bottom-gate TFTs having inkjet-printed gold gate electrodes have been reported and have shown a mobility of 0.002 cm^2/Vs [11]. In this case, a laser-based selective sintering method was used to improve the surface roughness of the gold electrode.

In this paper, we report a bottom-gate pentacene TFT fabricated on a glass substrate, which has an inkjet-printed silver gate electrode and a spin-coated cross-linked poly(4-vinylphenol)(PVP) gate insulator. With optimized jetting and thermal sintering conditions, the printed silver electrodes showed high conductivity and low surface roughness, which are key properties required for a good gate electrode in a bottom-gate TFT structure. The fabricated device showed a good performance that is comparable with that of the conventional TFT with an indium-tin-oxide (ITO) gate electrode [12,13].

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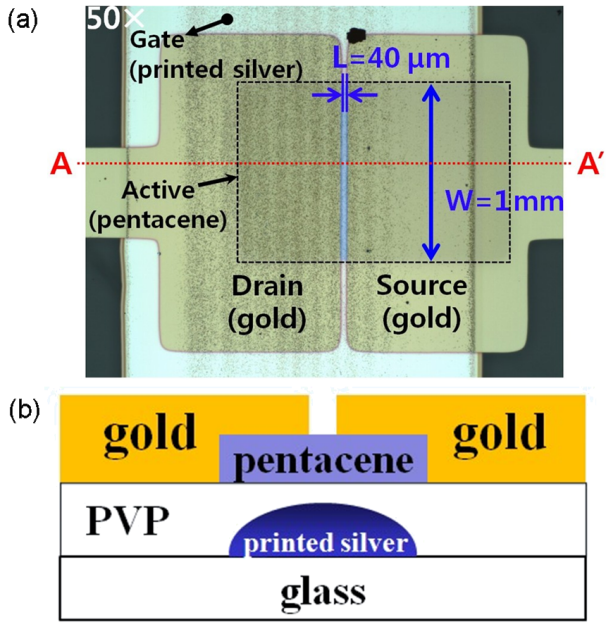

Fig. 1. (a) Top and (b) cross-sectional views of the fabricated bottom-gate pentacene TFT.

II. EXPERIMENTS

We fabricated bottom-gate pentacene TFTs with the printed silver gate electrodes on glass substrates. First, bare glass substrates were cleaned by using a tandard solvent cleaning process (acetone, isopropylalchol and deionized water sequentially in an ultrasonic bath). On the substrate, silver gate electrodes were printed and annealed at 150 °C for 30 minutes in an oven under an atmospheric environment. The thickness of the gate electrode was about 250 nm. Silver ink from INKTEC corp. (TEC-IJ-010) and an inkjet printer from DIMATIX corp. (DMP-2800 series) were used. After the gate electrode was formed, a PVP solution was spin-coated at 500 rpm for 5 seconds and then at 4000 rpm for 35 seconds and it was thermally cross-linked at temperatures of 100 °C for 10 minutes and then 200 °C for 10 minutes in an oven. The thickness of the PVP gate insulator was about 700 nm. The PVP solution was prepared by using the following procedure: 15 wt% of PVP and 3 wt% of poly (melamine-co-formaldehyde) as a cross-linking agent (CLA) were dissolved in propylene glycol monomethyl ether acetate (PGMEA). The solution was stirred using a magnetic spin bar at room temperature for 24 hours in air. PVP, CLA and PGMEA were purchased from Sigma-Aldrich Co. On the cross-linked PVP gate insulator, a pentacene active layer was thermally evaporated in a vacuum chamber at a pressure of 3×10^{-6} Torr at room temperature and a deposition rate of 0.5 Å/s. Finally, gold source/drain electrodes were thermally deposited without breaking the vacuum, with the same conditions as those for the pentacene evaporation, but with a deposition rate of 1.0 Å/s. The thicknesses

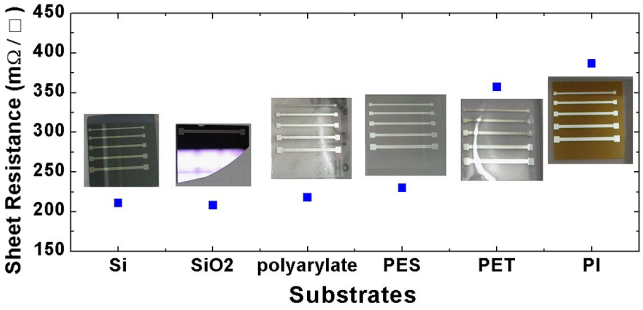

Fig. 2. Measured average sheet resistance of the printed silver electrodes on various substrates.

of the pentacene and the gold electrodes were 60 and 80 nm, respectively. The gate width (W) and length (L) of the fabricated TFT were 1000 and 40 μm, respectively, which were defined by the shadow masks for pentacene and the source/drain electrodes, respectively. Figure 1 shows optical microscope and cross-sectional schematic images of the bottom-gate TFT with the printed silver gate electrode.

To characterize the PVP insulation layer, metal/insulator/metal (MIM) capacitor structures were also fabricated on the same substrate, under the same conditions used for the pentacene TFT. The MIM capacitor of printed silver/PVP/gold had an area of 2 mm^2. We also fabricated a pentacene thin-film transistor with an ITO gate as a reference device. In this device, 150-nm-thick ITO-gate pre-patterned glass substrates were used. The device structure and the process conditions were the same as those for the TFTs with the printed silver gate, except for the thickness of the gate insulator, which was about 800 nm.

The transfer and the output characteristics of the fabricated TFTs and the capacitance-voltage (C-V) characteristics of the MIM capacitors were measured using a HP 4155C semiconductor parameter analyzer and a HP 4284 precision LCR meter, respectively. The thicknesses of the metal and the organic layers were measured using a TENCOR Alpha-step 500 system. The surface roughness of each layer and the grain size of the pentacene active layer were measured using an atomic force microscope (AFM). The scan area was 8×8 μm^2 for metal layers, 10×10 μm^2 for the PVP layer and 4×4 μm^2 for the pentacene layer. The contact mode was used for metal layers and the non-contact mode was used for organic layers to prevent the surface from scratching during the scanning process. All measurements were performed at room temperature in air.

III. RESULTS AND DISCUSSION

Figure 2 shows the sheet resistance of the printed silver electrodes on various substrates, such as silicon, silicon oxide, polyarylate, polyethersulfone (PES),

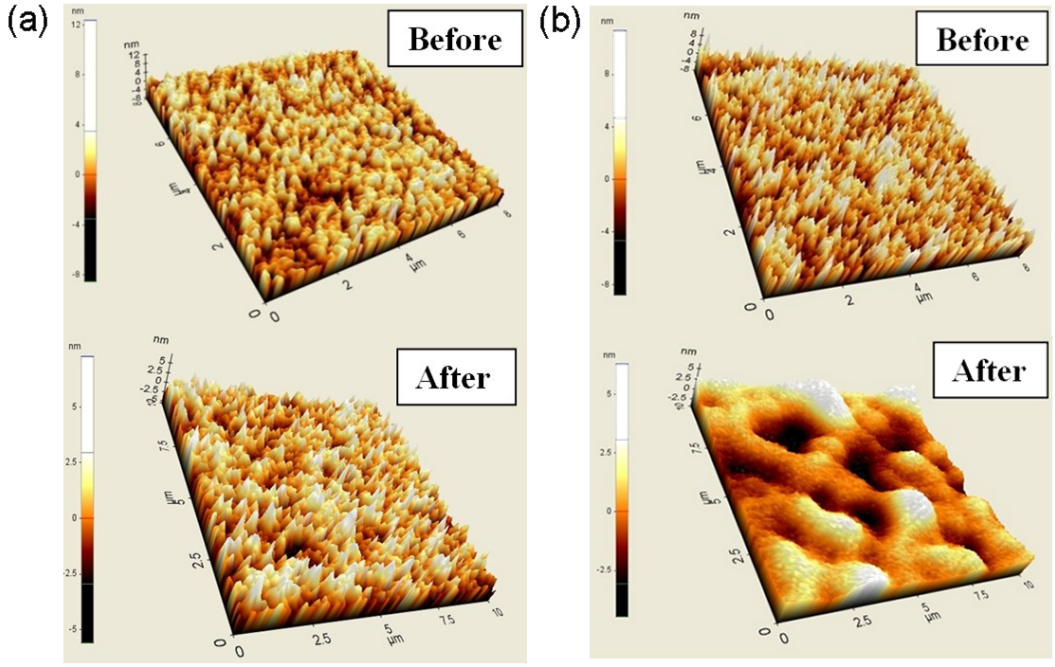

Fig. 3. Surface roughness of (a) ITO and (b) printed silver electrodes before and after PVP was coated.

Table 1. Peak-to-valley (P2V) and root-mean-square (RMS) values of the measured surface roughness.

	P2V (nm)		RMS (nm)		Thickness (nm)	
	Before	After	Before	After	Electrode	PVP
ITO	20.91	12.87	1.80	1.49	150	700
Printed Silver	20.14	10.77	2.38	1.57	250	700
Evaporated Silver	19.90	N/A	2.25	N/A	200	N/A

polyethyleneterephthalate (PET) and polyimide (PI). The thicknesses of the printed silver electrodes were 200 – 300 nm. The sheet resistance was measured for silver electrodes with widths of 0.5 – 1 mm by using a two-probe method. The average values of the measured sheet resistance were 0.2 – 0.4 Ω/□, as shown in Figure 2. This value is similar to that of the vacuum-deposited silver electrodes. The measurement error was within ±10 %.

Figure 3 shows the surface roughness of ITO and printed silver electrodes before and after the PVP layer was coated. The root-mean-square (RMS) and the peak-to-valley (P2V) values of the surface roughness are summarized in Table 1. The surface roughness data for the thermally evaporated silver electrode are also included for comparison. The surface roughness of the printed silver electrode was as good as that of the ITO and the thermally-evaporated silver electrodes. The P2V and the RMS values were further reduced from about 20 and 2 nm to about 10 and 1.5 nm, respectively, after the PVP layer was coated on both the ITO and the printed silver electrodes. The PVP gate insulator can behave as a good planarization layer and will improve the surface roughness of the channel area, leading to an improvement in the TFT electrical performance because it is well known that the surface roughness of the gate insulator in the channel area is closely related to the charge transport in TFTs [14,15]. The properties of the PVP gate insulator were also analyzed by measuring the leakage current and the high-frequency (1 kHz) capacitance of the printed silver/PVP/gold and ITO/PVP/gold MIM structures, where the thicknesses of the PVP were 700 and 800 nm, respectively. Unit area capacitances of 6.2 and 5.3 nF/cm^2 and leakage currents of 10.4 and 7.9 nA/cm^2 at 0.5 MV/cm were obtained for the former and the latter device, respectively.

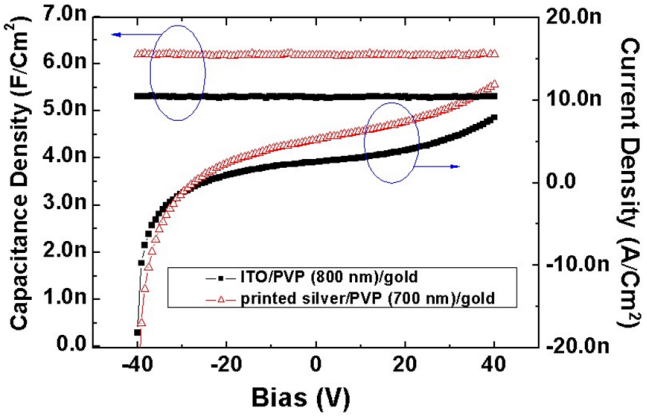

Fig. 4. I-V and C-V characteristics of printed silver/PVP/gold and ITO/PVP/gold structures.

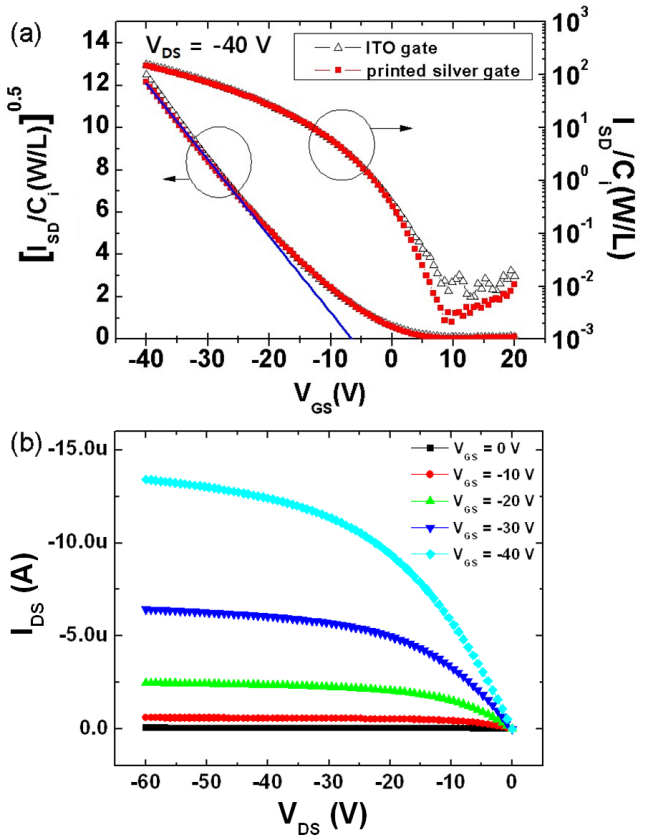

Fig. 5. (a) Normalized transfer curves for a TFT with printed silver and ITO gate and (b) output characteristic of a TFT with a printed silver gate.

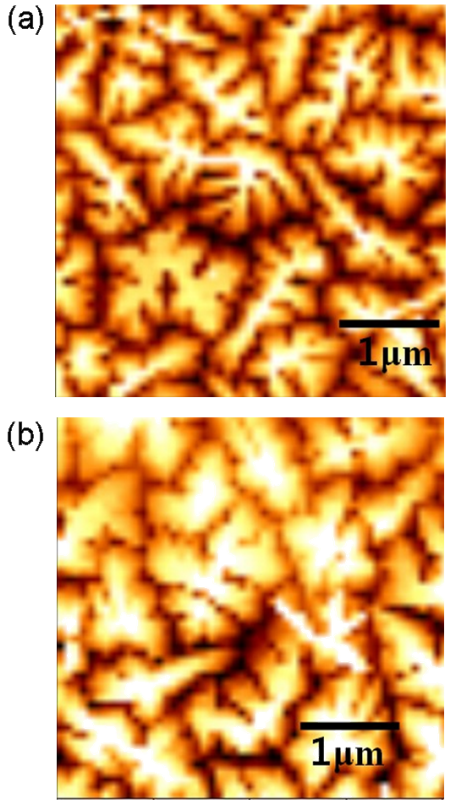

Fig. 6. AFM images of pentacene on (a) printed silver/PVP and (b) ITO/PVP structures.

Figure 5 shows saturation region transfer and output characteristics for the bottom-gate pentacene TFT with inkjet-printed silver gate. The saturation region transfer curve of our ITO gate reference device is also included. The channel length and width of the TFTs in both cases were 40 μm and 1000 μm, respectively. To compare the performances of both TFTs, we normalized the drain current by considering the measured unit-area gate dielectric capacitance (Ci) and the W/L of the TFTs. We extracted a field-effect mobility of 0.13 cm^2/Vs, a threshold voltage of -6.5 V and an on/off current ratio of about 10^5 for the printed silver gate TFT. Our reference device showed a field-effect mobility of 0.14 cm^2/Vs, a threshold voltage of -7.4 V and an on/off current ratio of greater than 10^4. This device performance is comparable with the reported values for pentacene TFTs with ITO gates [12,13,16]. The on/off current ratio increases by one order of magnitude when both TFTs are operated in their linear region ($V_{DS} = -5$ V), which is not shown in this paper. It is noted that based on the very similar TFT performances, the PVP organic insulator provides consistent surface and interface properties for the following pentacene layers for both ITO and printed silver gate electrodes. In addition to the surface and interface properties of the gate insulator, grain formation and the size of the pentacene layer are also important in improving TFT performances [13,16,17]. Therefore, we measured the grain sizes of the pentacene active layers for both devices. Figure 6 shows AFM images of the pentacene active layers, where grains are clearly observed. The sizes of the grains were $1 - 2$ μm for both devices, which is similar to previously reported values for pentacene TFTs with conventional ITO gate electrodes and PVP dielectric layers [16]. It is expected that when the pentacene layer is deposited at higher temperatures, the grain size will increase, resulting in a better TFT performance [12].

IV. CONCLUSIONS

We successfully fabricated a bottom-gate pentacene TFT with a printed silver gate electrode. The smooth surface of the printed silver gate electrode and the good insulation and planarization properties of the PVP gate insulator produced good TFT performances. This result shows that the printed silver electrode works well as a bottom-gate electrode, which enables low-cost, low-temperature, and maskless processes for TFT fabrication. We believe that the printing process of the PVP gate insulator and the solution process of the semiconducting layer are optimized, a high performance all-

printed bottom-gate TFT with a silver gate electrode can be obtained for printable electronics applications.

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