

A Tool for Fast Mismatch Analysis of Analog Circuits

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ABSTRACT

A tool is presented that evaluates statistical deviations in performance characteristics of analog circuits, starting from statistical deviations in the technological parameters of MOS transistors. Performance is demonstrated via the analysis of a Miller OTA in two different configurations and a linearized CMOS transconductor. The CPU time is reduced by a factor of 25 to 90 with respect to conventional Monte Carlo simulation, while maintaining similar accuracy in the computations.

I. Introduction

The performance of analog cells may be severely deteriorated due to random fluctuations in the electrical parameters of their components: transistors, resistors and capacitors. Crucial features like offset, common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), etc., are critically dependent on random-induced mismatches, and require careful design (equivalently sizing) to guarantee that specifications remain within tolerable margins for the largest possible number of circuit samples. However, due to the difficulties encountered in the modeling and evaluation of random fluctuations, this problem is usually handled by simply imposing conservative constraints in the design parameter space; e.g. the transistor area in a differential amplifier must be larger than say, $100 \mu\text{m}^2$. This leads to underexploitation of the performance potentials of the technologies. The optimization of the design procedure of analog cells under random fluctuations of the transistor parameters encompasses two different kinds of problems:

a) *Statistical modeling*, essentially the capture of statistical features of the components into parameterized models.

b) *Statistical simulation*, or the evaluation of the statistical features of the circuit performance induced by random variations of the electrical parameters.

The statistical modeling of MOS components has been covered by different authors in recent years [1-4]. Our contribution focuses not on the statistical modeling, but rather on statistical simulation. For modeling we rely on the proposal by Pelgrom [1] and more specifically, its further refinement as proposed in [2]. Such a

model provides the variances of the electrical parameters of MOS devices as a function of their geometry and distances and covers correlations among electrical parameters.

According to [2] variances of the electrical parameters of a given device can be evaluated from its layout as

$$\sigma^2(\Delta P) = \frac{A_p}{2WL} + S_p^2 D^2 \quad (1)$$

where D denotes the distance from the device to a common reference point (the coordinate center); WL , its area; and A_p and S_p are fitting constants, different for each technological parameter subject to variation.

Let us focus on statistical simulation. Most analog designers use Monte Carlo analysis for this purpose. However, for large analog cells described at the electrical level this is very costly in CPU time. This precludes its usage inside iterative analog design procedures [5,6] and motivates looking for more efficient solutions [7,8,9]. Especially significant is the technique proposed by [9], based on a two-step linearization of the circuit performance. Precise results are obtained using the Monte Carlo method with that linearization. However, it assumes that circuit performances do not change significantly. Thus, the examples presented have no node with voltage standard deviation larger than 0.1V.

Our contribution aims to use matrix methods to perform statistical analysis of analog integrated circuits starting from correlated electrical model parameters. These have been calculated according to the modeling technique in [4]. In particular, two different matrix techniques have been developed and included in a computer tool whose flowchart is shown in Fig.1. Some significant features of the proposed method are:

1) Statistical features of branch currents and node voltages of any circuit can be evaluated, allowing easy extension to any electrical, DC or AC, performance.

2) Results adequately fit those obtained with Monte Carlo analysis using an electrical simulator.

3) Analysis time is minimized so that the method can be included in an optimization-based design system.

II. Matrix-1 Technique

Variations in the transistor electrical parameters of a

given circuit induce changes in its node voltages and branch currents which can be calculated analytically. For a single transistor:

$$\sum_k \frac{\partial I}{\partial p_k} \Delta p_k + \frac{\partial I}{\partial V_G} \Delta V_G + \frac{\partial I}{\partial V_D} \Delta V_D + \frac{\partial I}{\partial V_S} \Delta V_S + \frac{\partial I}{\partial V_B} \Delta V_B = \Delta I \quad (2)$$

where p_k represents the k -th electrical model parameter.

Equation (2) is more conveniently written as,

$$\frac{\partial I}{\partial V_G} \Delta V_G + \frac{\partial I}{\partial V_D} \Delta V_D + \frac{\partial I}{\partial V_S} \Delta V_S + \frac{\partial I}{\partial V_B} \Delta V_B - \Delta I = - \sum_k \frac{\partial I}{\partial p_k} \Delta p_k \quad (3)$$

For a given circuit containing N transistors, and assuming that M node voltage variations and $N-M$ branch current variations are chosen as unknowns, the following linear equation system can be formulated:

$$A \cdot \Delta x = b \quad (4)$$

where

$$\Delta x_j = \begin{cases} \Delta V_j & \text{if } j \leq M \\ \Delta I_{j-M} & \text{if } j > M \end{cases} \quad b_i = - \sum_k \frac{\partial I_i}{\partial p_k} \Delta p_k$$

$$a_{ij} = \begin{cases} \frac{\partial I_i}{\partial V_D} \delta_{Dj} + \frac{\partial I_i}{\partial V_G} \delta_{Gj} + \frac{\partial I_i}{\partial V_B} \delta_{Bj} + \frac{\partial I_i}{\partial V_S} \delta_{Sj} & \text{if } j \leq M \\ -1 & \text{if } j > M \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

where δ_{xj} ($x=D,G,S,B$) is 1 if voltage V_x and voltage V_j correspond to the same physical node, or contrarily 0.

Cramer's rule is used to solve (4) and enables introducing correlations between transistors in the calculation. Hence, the j -th unknown is given by:

$$\Delta x_j = \frac{(A_{1j}b_1 + A_{2j}b_2 + \dots + A_{Nj}b_N)}{|A|} \quad (6)$$

where the coefficients A_{ij} are the cofactors of the elements in the j -th column.

Since we aim to determine variance, (6) must be multiplied by itself and integrated over the entire range of p_k parameters. Then, the variance results:

$$\sigma_{\Delta x_j}^2 = \frac{1}{|A|^2} \sum_{k=1}^N \sum_{l=1}^N A_{kj} A_{lj} \rho_{b_k b_l} \sigma_{b_k} \sigma_{b_l} \quad (7)$$

where σ_b is given by:

$$\sigma_{b_k} = \sqrt{\sum_r \sum_s \frac{\partial I_k}{\partial p_r} \frac{\partial I_k}{\partial p_s} \rho_{p_r p_s} \sigma_{p_r} \sigma_{p_s}} \quad (8)$$

and the correlation between two entries of vector b :

$$\rho_{b_k b_l} = \begin{cases} 1 & \text{if } k = l \\ \frac{Dist_{M_k} Dist_{M_l} \sum_r \sum_s \frac{\partial I_k}{\partial p_r} \frac{\partial I_l}{\partial p_s} \rho_{p_r p_s} \sigma_{p_r} \sigma_{p_s}}{\sigma_{b_k} \sigma_{b_l}} & \text{otherwise} \end{cases} \quad (9)$$

$Dist_{Mk}$ and $Dist_{Ml}$ represent distances to the coordinate center. The mean values are assumed equal to the nominal values.

The OTA Miller in Fig.2, configured as an unity-gain buffer, illustrates the performance of this method.

Table 1 shows the deviations in node voltages and branch currents obtained by Monte Carlo simulations (50 simulation instances) and those obtained by the Matrix-1 technique. As shown, the Matrix-1 technique reduces the CPU time by a factor of 90, without significant deviations in the analysis results as compared with those obtained by Monte Carlo simulations. The BSIM model was used considering variations of 16 parameters (and their correlations). Correlations of the electrical parameters in HSPICE simulations were calculated using the Principal Component Analysis technique [2].

However, the Matrix-1 method does not consider eventual excursions of the transistor operating points through different operating regions (i.e. ohmic, saturation, etc.) and thus, may obtain inaccurate results for circuits containing nodes which swing over wide voltage intervals. For example, consider the open loop OTA Miller of Fig.3. Table 2 shows the branch currents and node voltages obtained by Monte Carlo analysis and the Matrix-1 technique. Since the circuit is in open loop, the voltage V_{n3} changes over a wide range, taking transistors M_6 and M_7 out of their nominal operating regions and hence, introducing important analysis errors.

III. Monte Carlo analysis on the system matrix: Matrix-2 Technique

The Matrix-2 technique solves these problems by performing a Monte-Carlo analysis on vector b . Parameters are generated according to their distribution. A non-linear system is solved using the Newton-Raphson method and sensitivities are updated at each iteration.

Let us define a function F_i for each transistor:

$$F_i \equiv I_i - I_i(V, p_i) \quad i = 1, 2, \dots, N \quad (10)$$

Circuit analysis consists in determining the voltages and currents which annul all F_i . A Monte Carlo simulation consists in solving the system for a large number of vectors of electrical parameters p_i .

The time is reduced considerably by using the system solution at the nominal point as an initial solution of the Newton-Raphson method. The function F_i at the nominal point is:

$$F_{ni} \equiv I_{ni} - I_{ni}(V_n, p_{ni}) \quad i = 1, 2, \dots, N \quad (11)$$

For another vector of electrical parameters p_i transistor currents can be approximated as:

$$I_i = I_i(V, p_i) = I_i(V, p_{ni}) + \sum_k \left. \frac{\partial I_i}{\partial p_{ik}} \right|_{x_n} \Delta p_{ik} \quad (12)$$

where the derivative is evaluated at the nominal point. Its corresponding function F_i is then:

$$F_i \equiv I_i - I_i(V, p_{ni}) - \sum_k \left. \frac{\partial I_i}{\partial p_{ik}} \right|_{x_n} \Delta p_{ik} \quad (13)$$

Let us define a function G_i as the difference of F_i at the nominal point and F_i for another set of parameters p_i :

$$G_i \equiv F_i - F_{ni} = I_i - I_{ni} - I_i(\mathbf{V}, \mathbf{p}_{ni}) + I_{ni}(\mathbf{V}_n, \mathbf{p}_{ni}) - \sum_k \left. \frac{\partial I_i}{\partial p_{ik}} \right|_{x_n} \Delta p_{ik} \quad (14)$$

Expanding G_i in Taylor series (first order) and making it equal zero to apply the Newton-Raphson method:

$$G_i(X_o + \delta X) = G_i(X_o) + \sum_j \left. \frac{\partial G_i(X)}{\partial x_j} \right|_{x_o} \delta x_j = 0 \quad (15)$$

Applying (15) to (14) and reordering terms obtains in matrix notation:

$$\mathbf{A} \left[\delta (\Delta \mathbf{x}) \right] = \left[-\sum_k \left. \frac{\partial I_i}{\partial p_{ik}} \right|_{x_n} \Delta p_{ik} + I_i(\mathbf{V}_n + \Delta \mathbf{V}, \mathbf{p}_{ni}) - I_{ni}(\mathbf{V}_n, \mathbf{p}_{ni}) - \Delta I_i \right] \quad (16)$$

where \mathbf{A} is defined as in (5) and $\Delta \mathbf{x}$ is the vector of unknown variations in voltages and currents.

In every iteration of the Newton-Raphson method the equation system is solved by LU decomposition and $\Delta \mathbf{x}$ is updated summing the solution $\delta(\Delta \mathbf{x})$ to it. The iterative procedure continues until convergence.

Performing Monte Carlo analysis on the system matrix is more costly in CPU time than the Matrix-1 technique, but allows more accurate evaluation of variations, as shown in the OTA Miller results in Table 2. Moreover, a precise shape of the distribution is obtained.

IV. Statistical features of DC Characteristics

Interesting DC characteristics are functions of node voltages and branch currents at one or more operating points. As their relationships are known, their statistical features are easily obtained starting from the voltage and current deviations at the operating points needed for their evaluation. The variation in a DC performance Y_i is expressed as:

$$Y_i = Y_i(\Delta x_{11}, \dots, \Delta x_{1N}, \dots, \Delta x_{M1}, \dots, \Delta x_{MN}) \quad (17)$$

where Δx_{jk} is the increase in the k -th unknown at the j -th operating point. Performances are usually determined by only one unknown; so, (17) is simplified to:

$$Y_i = Y_i(\Delta x_r), \dots, \Delta x_{rN}) \quad (18)$$

Method-1 calculates performance sensitivities with respect to vector ΔX , and the variance is then given by:

$$\sigma^2(\Delta P_i) = \sum_k \left(\left. \frac{\partial P_i}{\partial x_r k} \right| \right)^2 \sigma_{\Delta x_r k}^2 + 2 \sum_k \sum_l \left. \frac{\partial P_i}{\partial x_r k} \right| \cdot \left. \frac{\partial P_i}{\partial x_r l} \right| \cdot \overline{\Delta x_r k \cdot \Delta x_r l} \quad (19)$$

where

$$\overline{\Delta x_r k \cdot \Delta x_r l} = \sum_j \sum_m A_{jr} A_{mr} \rho_{b_j b_m} \sigma_{b_j} \sigma_{b_m} \quad (20)$$

and $\rho_{b_j b_m}$ is defined similarly to (9).

If Method-2 is used, calculations are reduced to using conventional statistical estimators.

Table 3 shows experimental results for the linearized transconductor in Fig.4. The specifications considered are slope, linearity, input offset, and output offset. Methods 1 and 2 give similar results (except mean values which are assumed equal to the nominal ones in Method-1), because no node experiments large excursions. Speed with respect to Monte Carlo analysis is increased by a factor of around 25 with Method-2 and a factor of 80 using Method-1.

V. References

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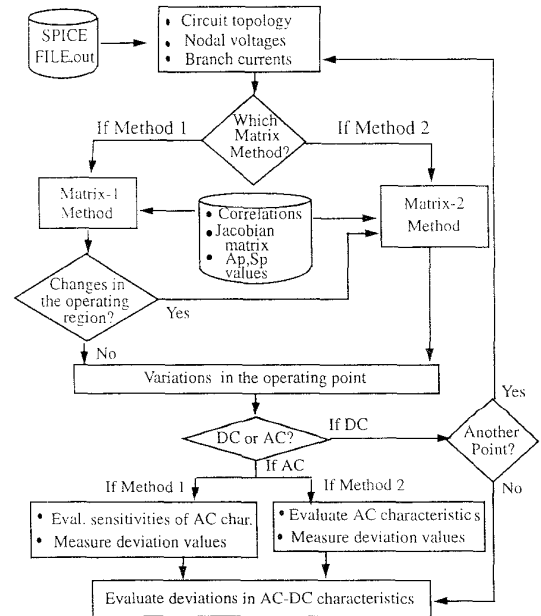


Figure 1: Flow diagram of the tool

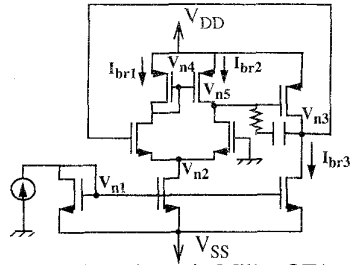


Figure 2: Unity-gain Miller OTA

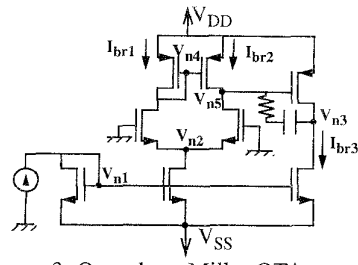


Figure 3: Open-loop Miller OTA

Node voltages & branch currents	MonteCarlo (50 samples)	Matrix-1 technique
	std dev	std dev
V_{n1}	5.29mV	4.39mV
V_{n2}	6.24mV	5.26mV
V_{n3}	4.94mV	3.15mV
V_{n4}	4.23mV	3.40mV
V_{n5}	7.94mV	7.43mV
I_{br1}	0.22 μ A	0.22 μ A
I_{br2}	0.23 μ A	0.22 μ A
I_{br3}	1.28 μ A	1.18 μ A
CPU time	90s	1.0s

Table 1: Comparative results for Fig.2.

Node voltages & branch currents	Monte Carlo analysis (50 samples)		Matrix-1 technique	Matrix-2 technique (50 samples)	
	mean	std dev	std dev	mean	std dev
V_{n1}	-3.89V	5.29mV	4.39mv	-3.89V	4.95mV
V_{n2}	-1.27V	3.5mV	2.72mv	-1.27V	3.21mV
V_{n3}	-3.04V	3.11V	0.4V	-3.13V	3.18V
V_{n4}	4.11V	4.39mV	3.34mV	4.11V	3.86mV
V_{n5}	4.17V	0.31V	0.2V	3.91V	0.33V
I_{br1}	7.27 μ A	0.27 μ A	0.27 μ A	7.14 μ A	0.27 μ A
I_{br2}	7.24 μ A	0.29 μ A	0.27 μ A	7.28 μ A	0.29 μ A
I_{br3}	27.28 μ A	33.9 μ A	35.7 μ A	32.2 μ A	35.2 μ A
CPU time	50s		0.8s	2.0s	

Table 2: Comparative results for the circuit in Fig.3

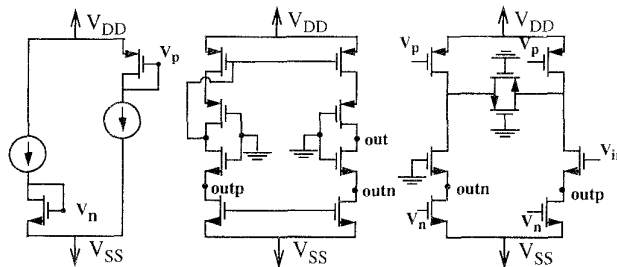


Figure 4: Linearized CMOS transconductor

Specifications	Monte-Carlo		New Tool	
	mean value	standard deviation	mean value	standard deviation
Slope ($V_{in}=0$)	5.5 μ A/V	0.21 μ A/V	5.4 μ A/V	0.21 μ A/V
Output offset	-0.1nA	0.5 μ A	-0.1nA	0.5 μ A
Input offset	-0.4mV	0.1V	-0.35mV	0.07V
Linearity: $V_{II}(V)=0.9*I(-2.5)$	-1.1V	20mV	-1.1V	21mV
CPU time	800s		Matrix-1 10s / Matrix-2 30s	

Table 3: Comparative results for the circuit in Fig.4 using Monte Carlo simulation and the new tool