

Nonlinear switched-current CMOS IC for random signal generation

M. Degaldo-Restituto, F. Medeiro, and A. Rodríguez-Vázquez

Indexing terms: Switched-current circuits, Oscillators, Chaos signal generators

A nonlinear switched-current circuit is presented that implements a chaotic algorithm for the generation of broadband, white analogue noise. The circuit has been fabricated in a double-metal, single-poly 1.6µm CMOS technology and uses a novel, highly accurate CMOS circuit strategy to realise piecewise-linear characteristics in the current-mode domain. Measurements from the silicon prototype show a flat spectrum from DC to ~30% of the clock frequency, for a clock frequency of 500kHz.

Introduction: During the last few years, the study of chaotic behaviour displayed by nonlinear deterministic systems has attracted an extraordinary amount of research attention in many different scientific and technologic disciplines. Today, there is renewed engineering interest in the topic, based on the expectations created by advanced signal processing [1] and computation paradigms [2] that operate in the context of chaos. In particular, deterministic chaos provides excellent algorithms for designing improved electronic random signal generators for white [3] and coloured [4] analogue noise, and for random number time series [5]. It is based on the extreme sensitivity of chaotic equations to initial conditions, that render their solutions (consequently, the waveforms provided by electronic circuits that implement these equations) stochastic-like [6].

Few of the previously reported chaotic circuits are realisable in monolithic form. To the best of our knowledge, the only monolithic chaos-based noise generator reported in the literature realises a piecewise-linear (PWL) discrete-time system employing switched-capacitor (SC) circuit techniques [3] which are very well suited to double-poly technologies. The circuit proposed in this Letter uses switched-current (SI) techniques for compatibility with standard, single-poly VLSI technologies. Measurements from a silicon prototype show faster operation than for the previously reported SC circuit [3], with much less silicon area occupation. Also, the proposed circuit is much simpler than digital noise generator structures composed of feedback shift register and lowpass filters, and provides fully aperiodic waveforms.

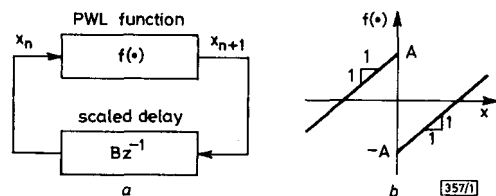


Fig. 1 Analogue computer concept for noise generation algorithm, and nonlinear function characteristic

a Analogue computer
b Nonlinear function characteristic

Noise generation algorithm and circuit concept: Fig. 1a shows a block diagram of the proposed circuit, consisting of a PWL function transformation, shown in Fig. 1b, whose output is fed back to the input through a delay block with scaling parameter B . Thus, the following PWL discrete-time system is implemented:

$$x_{n+1} = \begin{cases} Bx_n + A & x_n < 0 \\ Bx_n - A & x_n > 0 \end{cases} \quad n = 0, 1, 2, \dots \quad (1)$$

where x_n denotes the value of x at the n th discrete time instance.

We may consider eqn. 1 as a signal generator, providing a sequence $\{x_n\}$ for a given initial value x_0 . Parameter B determines the dynamic properties of the generated signal (also called orbit or trajectory), while parameter A acts only as a scale factor. For $1 \leq B \leq 2$, all steady-state orbits starting within interval $J = [-A, A]$, are aperiodic and remain confined inside J ; the system is in the

chaotic regime. In this regime, slight differences in the initial conditions are greatly amplified in a few iterations: the system has a sensitive dependence on initial conditions [6]. Also, for $B > \sqrt{2}$, and with the exception of a countable set of periodic points, any arbitrarily small subinterval inside J is reached regardless of the initial point: the map is ergodic in the range $B \in [\sqrt{2}, 2]$. Actually, for B near 2, the distribution of iterates is very uniform, allowing map exploitation for improved random number and white noise generators.

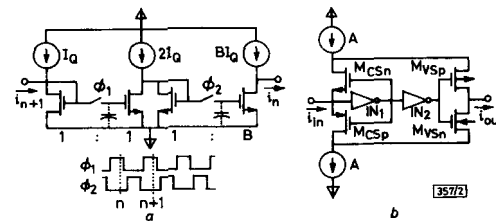


Fig. 2 Scaled delay block and schematic diagram for realisation of PWL characteristic

a Delay block
b Schematic diagram

Consider implementation of eqn. 1 in the current-mode domain, according to the concept of Fig. 1a. The scaled delay operation can be realised as a cascade of two track-and-hold switched-current stages, following the proposal by Hughes *et al.* [7]. Fig. 2a shows schematic diagrams for this block; parameter B is set by adjusting the geometry factors and bias current of the second track-and-hold stage. Fig. 2b, which consists of two current sources (realised in practice by current mirror output branches), four transistors and two digital inverters, shows a conceptual schematic diagram for the realisation of the PWL characteristics of Fig. 1b. Transistors M_{CSn} and M_{CSp} in Fig. 2b operate as a current-controlled-current-switch, and transistors M_{VSn} and M_{VSp} operate as voltage-controlled current switches. Any positive input current increases the input voltage, turning the M_{CSp} device on, and since both devices in the current switch have the same gate voltage, M_{CSn} off. Simultaneously, the voltage at the second inverter output evolves to the high logic state, turning M_{VSn} on and M_{VSp} off. Thus, a current $i_{in} - A$ (obtained by KCL at node N_1) is directed to the output node through transistor M_{VSn} ; the right-hand section of Fig. 1b is implemented in this manner. Similarly, negative input currents turn M_{CSn} and M_{VSp} on, so that a current $i_{in} + A$ circulates through M_{VSp} to the output node. Because current discrimination in the proposed circuit relies on the integration function performed at the input node, resolution is very high, and not influenced by transistor mismatches. Also, the feedback created by inverter IN_1 yields significant reduction of the dead zone exhibited by the driving point characteristics measured at the input node, that is proportional to $(V_{Tn} + |V_{Tp}|)/K$, where V_{Tn} and V_{Tp} are the threshold voltages for the transistors and K is the inverter DC gain. This is an appealing feature that enables reduction of inter-stage loading errors caused by finite equivalent MOS transistors Early voltages.

CMOS prototype and experimental results: A prototype of the proposed circuit has been fabricated in a 1.6µm CMOS doublemetal single-poly n -well technology. In this prototype, the output transistor of the second track-and-hold stage is a binary-weighted transistor array, thus allowing digital control of parameter B . Also, some extra miscellaneous circuitry has been added to enable testing of the output current and the possibility to either open or close the feedback loop. Bias current I_Q for the delay stages was set to 50 µA with $A = 20$ µA. Slopes of the characteristic, which correspond to the B parameter in eqn. 1, were set to a value slightly less than 2, to avoid divergent orbits that may arise as a consequence of non-ideal effects, such as clock feedthrough. Total area occupation, including miscellaneous circuitry, amounts to 0.096mm².

The characteristics of Fig. 3 have been measured in the open loop configuration. Fig. 3a ranges from -20 to 20 µA and shows the actual global PWL current transfer characteristics displayed by the prototype. Measured deviation from linearity in this range is less than 0.2%. Fig. 3b shows a detail of the global characteristics,

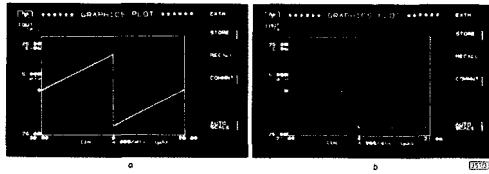


Fig. 3 Measured characteristic of nonlinear block, and detail of discrimination function

a Nonlinear block characteristic
b Discrimination function

where the input current changes from -21 to 21 pA. It is intended to illustrate resolution achieved in the current discrimination which amounts to few picoamps.

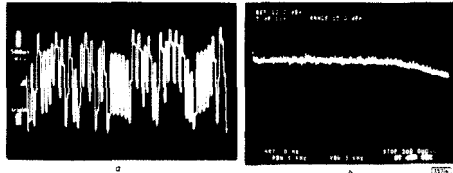


Fig. 4 Measured current waveform and power density spectrum

a Current waveform
b Power density spectrum

Fig. 4 illustrates the closed loop operation of the prototype for a clock frequency of 500 kHz. Fig. 4a shows the measured current waveform, and Fig. 4b its associated power density spectrum. The waveform of Fig. 4a shows that apparently coincident values of i_n result in quite different values after few iterations, thereby confirming the expected unpredictable feature. Regarding Fig. 4b, detailed measurements show a very flat spectrum from DC up to $\sim 30\%$ of the clock frequency (deviation was less than 1 dB).

It is useful to compare the performance of this circuit with that of the SC circuit reported previously for the same function [3]. Area occupation of the SI prototype is about one order of magnitude smaller than for the SC prototype. Also, for half the power consumption, the speed of the SI prototype is about three times greater than that obtained from the SC prototype.

Ideas in the Letter are directly extensible to the design of chaotic neural circuits, because signal aggregation is easily achieved in current-mode, by simply routing component currents to a common node. In particular, the Bernoulli circuit can be extended in this way to implement the chaotic neuron model proposed in [2], which models experimentally observed patterns of squid giant axons. Also, the circuit strategy used to implement the nonlinear function can be extended to support a systematic approach to high-accuracy function generation in the current domain. Such extensions will be reported in separate papers.

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1 September 1993

Electronics Letters Online No: 19931429

M. Degaldo-Restituto, F. Medeiro and A. Rodríguez-Vázquez (Centro Nacional de Microelectrónica-Universidad de Sevilla, Edificio CICA, C/ Tarfia s/n, 41012-Sevilla, Spain)

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ELECTRONICS LETTERS 9th December 1993 Vol. 29 No. 25

2191

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Settling time reduction technique for high speed DACs

O. Kim, G. Kim and W. Kim

Indexing terms: Digital to analogue conversion, Integrated circuits

The ringing mechanism of the high impedance output node was analysed. To reduce this ringing, a new compensation circuit was developed and implemented in a standard CMOS process. This circuit can be programmed to cover a range of parameters. It is effective in minimising the settling time of a DAC.

Introduction: There is an ever-increasing need for monolithic digital to analogue convertors (DACs) that have a resolution range of $8 - 10$ bits. The segmentation architecture with current output [1] is widely used to obtain both high speed and high resolution using a standard CMOS technology.

In this architecture, the output impedance needs to be high to obtain good linearity. This high output impedance coupled with the inductance of the packaging produces parasitic poles in the transfer function. These poles lead to ringing at the output node and an increase in the settling time.

The ringing mechanism was analysed and a new output compensation circuit was developed. This circuit effectively eliminates the ringing at the output node.

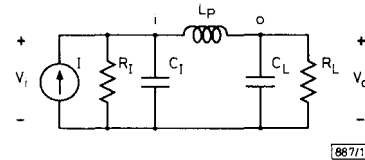


Fig. 1 Equivalent circuit of DAC output section

Modelling of output pad: Fig. 1a shows the equivalent circuit of a DAC output section. Node i is the internal node of the device. Node o is the external node like that on the printed circuit board. R_i is the output resistance of the device. C_i is the equivalent capacitance associated with node i which includes the parasitic capacitance of the current switch output, metal layout and bonding pad. L_p is the parasitic inductance between node i and o [2]. It comprises the parasitic inductance of a bonding wire and the lead frame of the package. C_o is the parasitic capacitance at node o , and R_L is the termination resistor. The effective value of R_L is 37.5Ω when the output node is doubly terminated with 75Ω .

Ideally, R_i is ∞ , C_i and L_p are 0. The step response at node o is given by

$$V_o = IR_L(1 - e^{-\frac{t}{T}}) \quad (1)$$

where $T = R_L C_L$. From this, the worst case settling time to within $1/2$ LSB of the target value is given by

$$T_{sett} = (n + 1)T \ln 2 \quad (2)$$

where n is the resolution of the device.

If C_i and L_p are included, the transfer impedance $Z(s)$ becomes

$$Z(s) = \frac{V_{out}(s)}{I(s)} \quad (3)$$

$$= \frac{R_i R_L}{R_i + R_L + (L_p + R_i R_L C_i + R_i R_L C_L)s + L_p(R_i C_i + R_L C_L)s^2 + L_p R_i R_L C_i C_L s^3} \quad (4)$$

If $R_i \gg R_L$ and $C_i \gg C_L$,

$$Z(s) \approx \frac{R_L}{(1 + R_L C_L s)(1 + L_p C_i s^2)} \quad (5)$$

The poles are