Switched-Current Chaotic Neurons

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Indexing terms: Switched-current circuits, Chaos, Neural networks

The Letter presents two nonlinear CMOS current-mode circuits that implement neuron soma equations for chaotic neural networks. They have been fabricated in a double-metal, single-poly 1.6μm CMOS technology. The neuron soma circuits use a novel, highly accurate CMOS circuit strategy to realise piecewise-linear characteristics in the current-mode domain. Their prototypes obtain reduced area and low voltage power supply (down to 3V) with a clock frequency of 500kHz.

Introduction: Most artificial neural networks use a simple neuron model where the processing realised by the soma involves a static nonlinear transformation, with either sigmoid or threshold characteristics. However, recent studies on real nerve membranes in neurophysiological experiments have shown that the dynamic behaviour of biological neurons is much more complex (including chaotic response) than that exhibited by simple models [1, 2]. Consequently new schemes of artificial neural networks have emerged to more realistically emulate the chaotic responses experimentally observed in biological systems. In particular, some remarkable chaotic neuron models have been reported by Nagumo and Sato [3], and Aihara *et al.* [4].

Many studies on chaotic neural networks in general, and using the previous models in particular, reveal that such networks serve not only as an experimental vehicle in the study of sensory nerve systems, but also lead to important engineering applications. In this sense, chaotic neural networks have been proposed to solve difficult optimisation problems [5], for dynamical associative pattern classification [6], and for signal detection and classification in noisy environments [7], and it is predictable that new applications will arise in the near future. Consequently, there is strong motivation to develop VLSI electronic implementations for these networks.

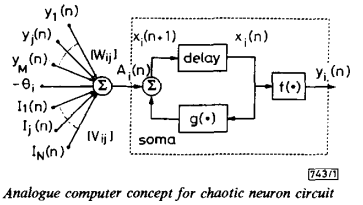

Fig. 1 *Analogue computer concept for chaotic neuron circuit*

Nonlinear block is given by $g(x) = kx - \alpha f(x)$, according to eqn. 1

Neuron models: Fig. 1 is a block diagram for a generic artificial neuron, where we can distinguish a dendritic/synaptic structure and a soma. The dendritic structure collects input signals (represented by vector **I**) and signals coming from other neurons (represented by vector **y**), so that the whole strength of the input is given by

$$A_i(n) = \sum_{j=1}^{M} W_{ij} y_j(n) + \sum_{j=1}^{N} V_{ij} I_j(n) - \theta_i \quad n = 0, 1, \ldots \tag{1}$$

where the first term corresponds to the M neurons driving the ith neuron, the second, to the excitation from the N external inputs, I_j; θ_i is the threshold, and n the discrete time variable.

Current-mode design techniques for the dendritic structure have been reported elsewhere [8]. Here we focus on the soma. In a conventional artificial neuron, processing performed at the soma is a simple nonlinear transformation. In the Nagumo–Sato model, that processing also involves dynamic operators,

$$\begin{aligned} x_i(n+1) &= kx_i(n) - \alpha u(x_i(n)) + A_i(n) \\ y_i(n+1) &= u(x_i(n+1)) \end{aligned} \quad n = 0, 1, \ldots \tag{2}$$

where α and k are the scaling and damping factors of refractoriness (residual effect of a neuron once fired), respectively, and $u(.)$ is a unit-step function. Numerical studies realised with this model show that chaotic responses occur only for a set of parameters with zero measure.

To extend the range of parameters for which chaotic behaviour can be observed, the chaotic neural network reported in [4] constitutes a modification of the Nagumo–Sato model [5], where instead of following an all-or-none law for the action potential (modelled by $u(.)$), the neuron shows a continuous stimulus-response curve (represented by $f(.)$). The model in [4] is defined by the following finite-difference equations:

$$\begin{aligned} x_i(n+1) &= kx_i(n) - \alpha f(x_i(n)) + A_i(n) \\ y_i(n+1) &= f(x_i(n+1)) \end{aligned} \quad n = 0, 1, \ldots \tag{3}$$

where $f(.)$ constitutes the neuron output function and can be represented by the piecewise-linear model,

$$f(x) = \frac{|x+\varepsilon| - |x-\varepsilon|}{2\varepsilon} \tag{4}$$

where ε is a positive number defining the steepness of the function.

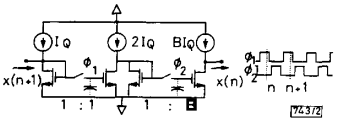

Fig. 2 *Current-mode track-and-hold circuit*

Current-mode implementations: Current-mode techniques have been employed in order to implement eqns. 2 and 3, following the conceptual diagram enclosed in the broken-line box shown in Fig. 1. Summation is easily realised exploiting KCL. The delay operation can be realised as a cascade of two track-and-hold switched-current stages [8] (see Fig. 2). Nonlinearities have been achieved using a novel, highly accurate CMOS circuit strategy to realise piecewise-linear (PWL) characteristics in the current-mode domain, which provides very high resolution and virtually zero current offset, not influenced by transistor mismatches (indeed, minimum size transistors were used in both prototypes) [9]. Fig. 3 shows the corresponding schematic diagrams for both PWL functions. Current amplifiers can be implemented by properly ratioed bilateral current mirrors.

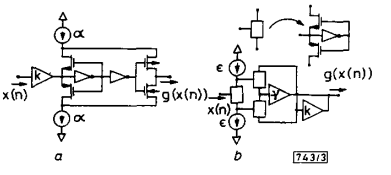

Fig. 3 *Piecewise-linear mapping circuits for neurons*

a Ngumo–Saito model
b Aihara model

Both neurons have been fabricated in a double-metal, single-poly 1.6μm CMOS technology. Fig. 4 shows the corresponding microphotographs. Some extra miscellaneous circuitry has been added to both circuits to enable testing of the output current and the possibility to either open or close the feedback loop. All current amplifiers were binary-weighted for reasons of programmability. Bias current I_Q for the delay stages was set to 50μA. The total area occupation is 0.096mm² for the Nagumo–Sato neuron, and 0.225mm² for the Aihara neuron.

Fig. 4 *Microphotographs of prototypes*

Fig. 5 shows the characteristics measured in an open loop for both circuits, using the HP4145 semiconductor analyser, with a rail-to-rail power supply of only 3V. For the Nagumo–Sato neuron (Fig. 5*a*), $\alpha = 20\mu A$, $k = 1$ and the input ranges from $-20\mu A$ to $20\mu A$. For the Aihara neuron (Fig. 5*b*), $\varepsilon = 2\mu A$, $\gamma = 10$, $k = 1$ and the input sweeps from $-10\mu A$ to $10\mu A$, where $\gamma = \alpha/\varepsilon$–$k$, according to eqns. 1 and 3. In both prototypes, deviation from linearity is less than 0.2%, and the measured current offset amounts to few picoamps.

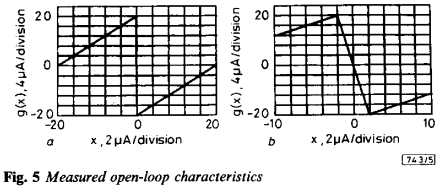

Fig. 5 *Measured open-loop characteristics*

Fig. 6 shows the experimental bifurcation trees for both neurons, when the damping factor $k = 0.5$ and the neuron excitation A, taken as the bifurcation parameter, varies from $-20\mu A$ to $20\mu A$. All other parameters were fixed to the values previously cited. The clock frequency was set to 500kHz.

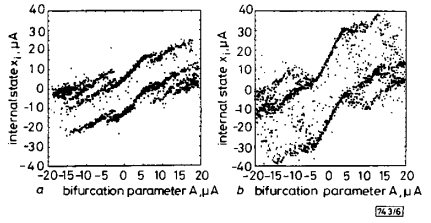

Fig. 6 *Bifurcation diagrams*

The full accordance observed between theory and measurements supports the development of future analogue VLSI chaotic neural networks to emulate biological systems and advanced computation.

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155Mbit/s optical wireless link using a bootstrapped silicon APD receiver

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Indexing terms: Space communication links, Optical communication, Local area networks

A 155Mbit/s optical wireless link has been implemented using a large-area silicon APD, bootstrapped, transimpedance receiver and a hologram-based laser transmitter. The receiver gives high sensitivity and high transimpedance while providing a large photodiode collection area.

Introduction: With the rise in popularity of mobile computers such as laptops and personal digital assistants, there is a growing demand for wireless access to fixed broadband networks. Optical wireless transmission has the potential to meet the dual requirement for broadband services and wireless access. One system option uses a ceiling-mounted access point to define optical cells of operation within a given area [1]. The link detailed in this paper could form a 155Mbit/s broadband downlink for a optical cell and is depicted in Fig. 1.

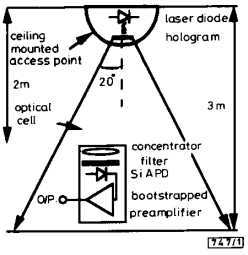

Fig. 1 *Schematic diagram of optical cell based link*

Bootstrapped Si APD receiver: The overall receiver circuit has a transimpedance topology (Fig. 2) to provide the large dynamic range required to accommodate the changing power levels in an optical wireless system. A large-area, commercially available Si APP (diameter = 5mm) was used as a photodetector and had an associated capacitance of close to 100pF. The bootstrapped input stage minimises the effective photodiode capacitance which is seen by the signal. This allows the feedback resistor value to be maximised for a given bandwidth requirement. The thermal noise power associated with this component is then reduced to an insignificant amount compared with other circuit noise sources [2].

The optimum APD gain is achieved when the amplified shot noise, which is generated by the ambient light generated current, device dark current and mean signal current, is equal to the total thermal noise. With bootstrapping, the thermal noise is signifi