Double-Sampling Single-Loop ΣΔ Modulator Topologies for Broad-band Applications

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***Abstract*—This paper presents novel double sampling high-order single loop sigma–delta modulator structures for wide-band applications. To alleviate the quantization noise folding into the inband frequency region, two previously reported techniques are used. The digital-to-analog converter's sampling paths are implemented with the single-capacitor approach and an additional zero is placed at the half of the sampling frequency of the modulator's noise transfer function (NTF). The detrimental effect of this additional zero on both the NTF and signal transfer function is also resolved through the proposed modulator architectures with a low additional circuit requirement.**

***Index Terms*—Double sampling, sigma–delta (ΣΔ) modulators, switched-capacitor circuits.**

I. Introduction

SIGMA–DELTA (ΣΔ) analog-to-digital converters (ADCs) are the main candidates for high resolution applications due to their inherent immunity to the circuit nonidealities [1]. In order to employ them in broad-band applications, a low oversampling ratio (OSR) should be used. But, the modulator accuracy is reduced by lowering the OSR, drastically. So, novel modulator structures are needed to alleviate the reduction of resolution in low OSR applications.

A useful approach in switched-capacitor realizations of the modulators is to employ the double-sampling technique [2]–[5]. In this method, the circuit operates during both phases of the clock. Hence, the effective sampling frequency of the system is twice that of the clock frequency. This results in doubling the OSR or the available time for settling of the integrators if the OSR and input signal bandwidth are fixed. Fig. 1 shows a single-ended double-sampling integrator. In this circuit, two distinct capacitors are used to sample the input signal. The capacitor C_{S1} is used to sample the input signal at the phase ϕ_1 while at this interval the stored charge on C_{S2} is transferred into the integrating capacitor, C_I. At the next phase, ϕ_2, C_{S2} samples the input signal and C_{S1} transfers its stored charge into C_I. Hence, in both phases of the clock, the sampling and integrating is performed resulting in doubling the effective sampling rate of the system.

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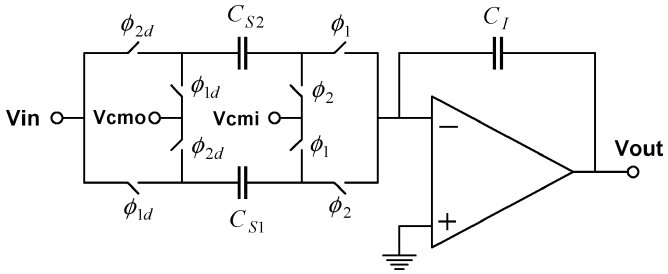

Fig. 1. Single-ended double-sampling integrator.

The signal transfer function of the double sampling integrator with an ideal opamp can be written as

$$V_{\text{out}}[n] = V_{\text{out}}[n-1] + \frac{C_S}{C_I} V_{\text{in}}[n-1] + \frac{(-1)^n \Delta C_S}{2C_I} V_{\text{in}}[n-1] \quad (1)$$

where $C_S = (C_{S1} + C_{S2})/2$, $\Delta C_S = (C_{S1} - C_{S2})$, and time $n = 0$ occurs when ϕ_2 is high [2]. The first two terms of the right side in (1) implements an ideal sample delaying integrator. But, the last term in (1) is the product of the input signal and $(-1)^n$, which indicates a modulation between the input signal and a sampled cosine at the half of the sampling frequency $(f_s/2)$ through any mismatch between the sampling capacitors. If the input is a low frequency signal, this mismatch does not affect the inband frequencies. However, since the digital-to-analog converter (DAC) output has a large high frequency quantization noise, this noise is folded into the inband frequencies if any mismatch exists between the DAC sampling capacitors. Therefore, the signal-to-noise ratio (SNR) is degraded. This is the main drawback of the double sampling modulators.

Several techniques have been proposed to alleviate the quantization noise folding such as the fully floating implementation of the critical sampling paths [3], placing a zero at $f_s/2$ of the noise transfer function (NTF) [4], and the single capacitor realization of DAC paths [5], etc. However, the first two techniques affect both the modulator's NTF and STF. Their effect is not considerable in first and second-order modulators. But, the NTF of high-order structures employing these techniques should be synthesized in a way to avoid the instability and more performance degradation. The last technique can only be used in the feedback DAC sampling paths. Also in this technique the opamp common mode input voltage like the fully floating method cannot be defined.

In [6] a systematic procedure has been proposed to design the stable double-sampling modulators with additional zeros of NTF at $f_s/2$. In this technique, the NTF poles are placed in two Butterworth configurations: one around dc zeros and the other

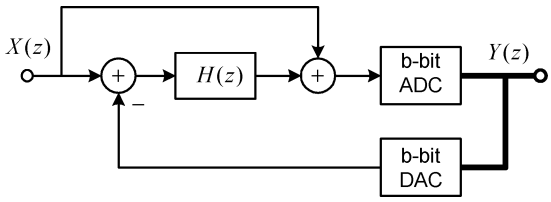

Fig. 2. General structure of a ΣΔ modulator.

around additional zeros at $f_s/2$. The bandwidth of the associated Butterworth filters are optimized for both the stability and noise shaping. However, with this technique it is not possible to achieve the efficient structures with unity gain STF.

In this paper, novel ΣΔ modulator topologies employing the double-sampling technique are proposed. The proposed modulator structures employ a finite-impulse response (FIR) NTF with an additional zero at $f_s/2$. Also to remove the quantization noise folding of the first integrator in high-order structures, the DAC sampling paths are realized using the single capacitor approach. The paper is organized as follows. Section II describes the derivations of the proposed modulator structures. Section III provides the simulation results. The conclusions are given in Section IV.

II. Proposed Modulator Topologies

A. General Structure

The general structure of the proposed ΣΔ modulators is shown in Fig. 2 where $H(z)$ is the loop transfer function. In this structure the STF is unity. Unity gain STF in a ΣΔ ADC has many advantages such as the followings. First, the effects of the circuit nonidealities such as the limited opamp dc gain and nonlinearities are reduced since only the quantization noise is processed by the integrators [7]. Second, the dynamic range is increased because the only elements that have to accommodate the full-input signal swing are the switches and the quantizer and the output swing of the opamps does not limit the input signal amplitude. Third, the integrators need small output swings.

The loop transfer function $H(z)$ can be obtained in term of the NTF as follows:

$$H(z) = \frac{1 - \mathrm{NTF}(z)}{\mathrm{NTF}(z)}. \tag{2}$$

The NTF of the proposed ΣΔ modulators is considered as FIR filter as follows:

$$\mathrm{NTF}(z) = \begin{cases} (1-z^{-1})(1+z^{-1}) \\ \quad \times \prod_{i=1}^{M}(1-\alpha_i z^{-1}+z^{-2}), & \text{if } L \text{ is odd} \\ (1-z^{-1})^2(1+z^{-1}) \\ \quad \times \prod_{i=1}^{M-1}(1-\alpha_i z^{-1}+z^{-2}), & \text{if } L \text{ is even} \end{cases} \tag{3}$$

where $M = [L/2]$ and L is the order of the modulator and is considered greater than two. It should be noted that the FIR NTF was selected in order to achieve the efficient double sampled modulator structures with unity gain STF. Of course, this is a limitation to put all of NTF poles at $z = 0$.

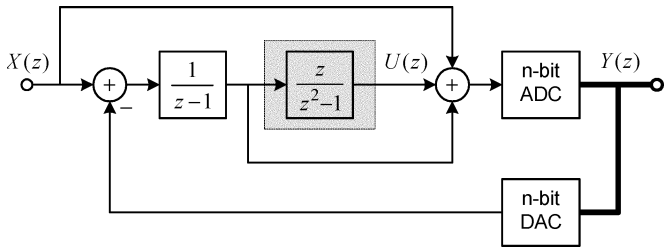

Fig. 3. Proposed second-order double-sampling modulator.

For the second-order structure only the first two terms of the NTF is assumed. A zero is placed at $f_s/2$ of the NTF through the term of $(1+z^{-1})$ to reduce the folding effect of the quantization noise into the signal band. The term $(1-z^{-1})$ is needed to realize the input stage of the modulator as an integrator without any local feedback DAC. For odd-order modulators only one zero of the NTF is placed at dc and the other zeros are located at the inband frequencies to shape out the quantization noise aggressively. For even-order structures, two zeros of the NTF are located at dc and the others at the inband frequencies. Another zero at dc is needed in even-order modulators compared to the odd-order structures in order to remove the requirement of the local feedback DAC around first pair of integrators.

It is worth mentioning that although placing a zero at $f_s/2$ of the NTF increases the quantization noise at the inband low frequencies about 6-dB, and hence degrades SNR by the same amount, but it avoids the quantization noise folding. It is also possible to achieve the aggressive noise shaping with an additional zero of NTF at $f_s/2$ since it relaxes the stability condition by reducing the NTF's out-of-band gain around the $f_s/2$. Therefore, with considering the mismatch between the DAC sampling paths that is not avoidable in a real implementation we can get a net benefit in SNR.

The loop transfer function, $H(z)$, of the proposed modulators is obtained with relations (2) and (3). For example, $H(z)$ of the second and third-order modulators is as follows, respectively:

$$\begin{aligned} H_2(z) &= \frac{z^{-1}}{1-z^{-1}}\frac{1+z^{-1}-z^{-2}}{1-z^{-2}} \\ &= \frac{z^{-1}}{1-z^{-1}}\left(1+\frac{z^{-1}}{1-z^{-2}}\right) \end{aligned} \tag{4}$$

$$\begin{aligned} H_3(z) &= \frac{z^{-1}}{1-z^{-1}} \\ &\quad \times\left(\alpha+\frac{\alpha(\alpha-1)z^{-1}+\alpha(\alpha-2)z^{-2}+(1-\alpha)z^{-3}}{1+(1-\alpha)z^{-1}+(1-\alpha)z^{-2}+z^{-3}}\right). \end{aligned} \tag{5}$$

As it is seen, the loop transfer function, $H(z)$, of the proposed modulators can be realized as an integrator and an infinite-impulse response (IIR) filter. For example, the realization of the proposed second-order modulator is shown in Fig. 3.

The proposed second-order double sampling modulator can be realized using a delaying integrator and a simple one sample delaying resonator. The double-sampling resonator with a unit delay can be implemented using only one opamp. So, only two opamps like the conventional second-order modulator are needed to realize the circuit of the proposed second-order double sampling modulator. The paths terminating at the input

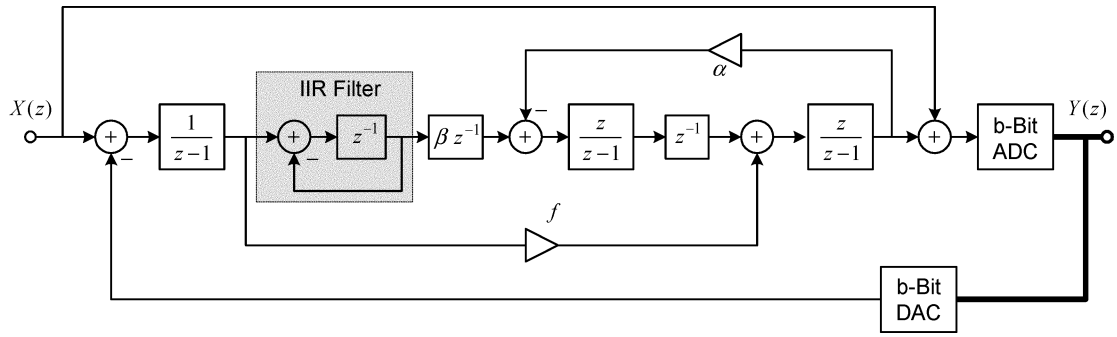

Fig. 4. Proposed third-order double-sampling $\Sigma\Delta$ modulator.

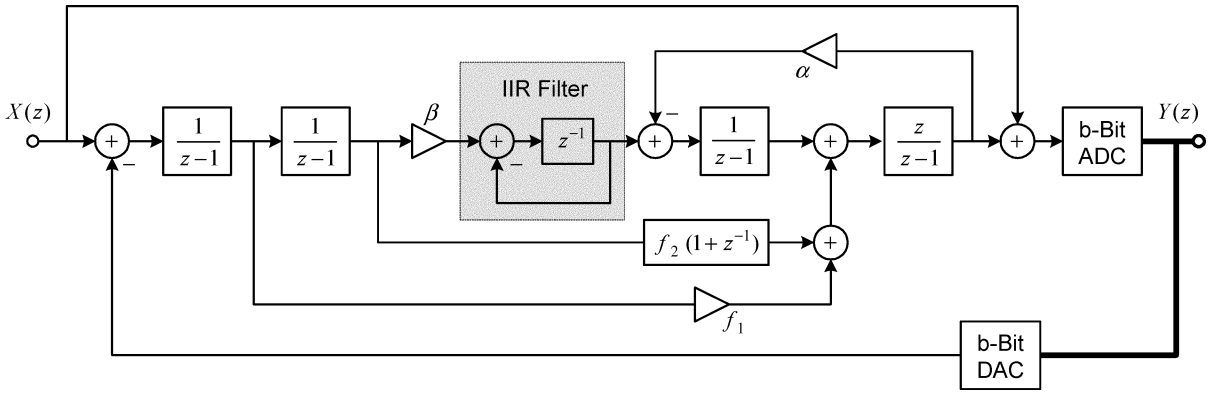

Fig. 5. Proposed fourth-order double-sampling $\Sigma\Delta$ modulator.

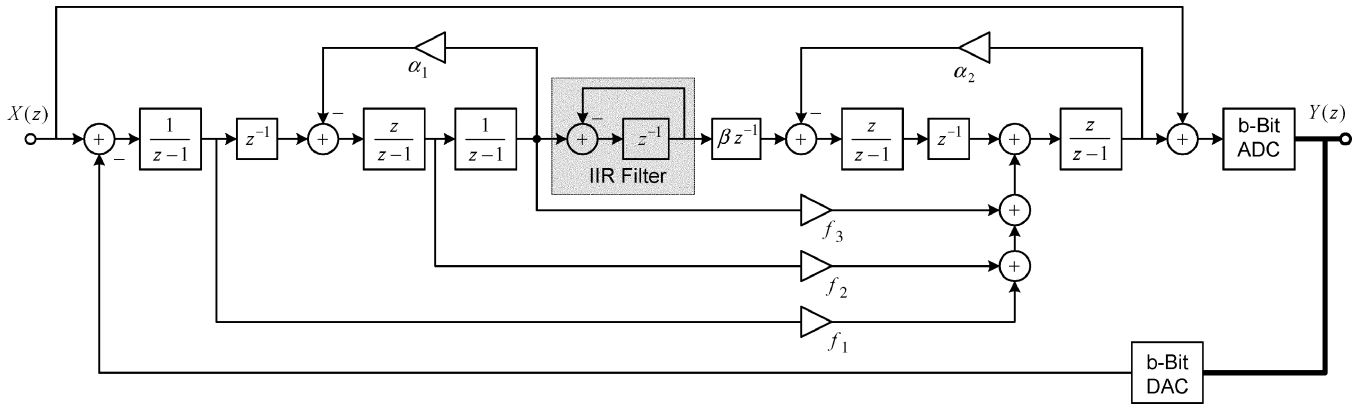

Fig. 6. Proposed fifth-order double-sampling $\Sigma\Delta$ modulator.

of the quantizer can be realized using a passive switched-capacitor circuit. The cascading of the proposed double sampling second-order modulator is very simple since the output of the resonator is only a function of the quantization noise.

Although, the realization of the proposed FIR NTF double-sampling modulators can be performed efficiently, the number of the modulator coefficients becomes large for high-order structures as is seen in (5) for the third-order structure. So, this realization will be more sensitive to the mismatch between the coefficients when the modulator's order becomes large. The other drawback of this realization is the existence of three paths terminating to the input of the quantizer that complicates the passive implementation in low voltage applications. So, more efficient structures that need lower number of coefficients and minimum terminating paths to the quantizer input are proposed in the next subsection.

B. *Efficient Structures*

The proposed NTF for double-sampling modulators can also be implemented efficiently as the combination of the integrators and only one first-order IIR filter as shown for the third, fourth and fifth-order modulators in Figs. 4–6, respectively.

The realization of high-order modulators can be obtained with a straight forward extension of the proposed structures. However, since the proposed topologies have the NTF with large out-of-band gain, the stability of higher order ones with large input signal level can only be achieved by changing the FIR NTF to an IIR one and/or using a multibit quantizer. On the

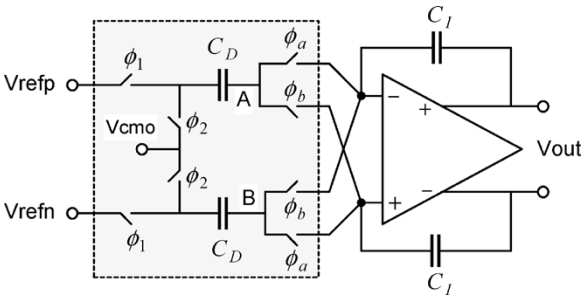

Fig. 7. Single capacitor implementation of DAC paths in a summing integrator.

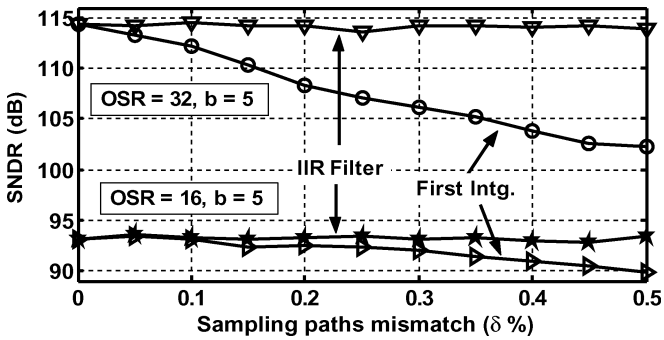

Fig. 8. Sampling paths mismatch effect of the third-order. $\delta = |(C_{S1} - C_{S2})|/(C_{S1} + C_{S2})$.

other hand, since we limited ourselves to NTF's of the form of (3), the modulators require a high-resolution quantizer in order to be stable. If this is not acceptable appropriate poles have to be added to the NTF. This is out of the scope of this paper and we will limit ourselves to modulators with a high-resolution quantizer.

The coefficients of the proposed modulators to obtain an FIR NTF as shown in (3) for the third-, fourth-, and fifth-order structures are as follows:

$$\beta = 1, \quad f = 2 - \alpha, \qquad \text{for } L = 3 \tag{6}$$

$$\beta = 1, \quad f_1 = 3 - \alpha, \quad f_2 = 1, \qquad \text{for } L = 4 \tag{7}$$

$$\beta = 1, \quad f_1 = 4 - \alpha_1 - \alpha_2$$
$$f_2 = f_3 = 3 - \alpha_1(4 - \alpha_1), \qquad \text{for } L = 5. \tag{8}$$

The coefficients α_i are needed to place some of NTF's zeros at the inband frequencies to shape out the quantization noise aggressively. The design method proposed by Schreier [8] can be used to obtain the values of α_i in order to place the inband zeros at the optimal points. The other coefficients are obtained such that the NTF becomes an FIR filter.

The single-capacitor realization of DAC paths is shown in Fig. 7 [5]. In phase ϕ_1, the charge of $C_D \times (\pm\text{Vref})$ is transferred by the capacitors C_D directly. Also the same amount of charge is stored on these capacitors that are used in the next phase, ϕ_2. Depending on the quantizer output bits the switches ϕ_a and ϕ_b connect the nodes A and B to the opamp inverting and noninverting inputs in order to realize the negative feedback operation of the summing integrator. However, this technique can only be used in the DAC paths and the opamp common-mode input voltage cannot be defined like the fully floating approach.

Implementation of the proposed modulators is like the conventional single loop structures. To realize the IIR filters, the generic low-Q biquad structure can be used. The fully differential double sampling implementation of $z^{-1}/(1+z^{-1})$ (IIR filters of Figs. 4–6) can also be performed efficiently using the switched-capacitor structure proposed in [6] with an extra opamp. The unit delays of the feedforward paths can be implemented with appropriate designing of the clock phases in switched-capacitor circuits without any extra circuit. The term $(1 + z^{-1})$ in the even-order structures can be realized using the fully floating technique and/or the bilinear sampling integrator without any effective extra circuit requirement. It should be noted that since the charge transfer of the DAC sampling capacitors is performed without any delay, the unit feedback delay of the first integrator is devoted to the quantizer and DAC linearization technique.

III. Simulation Results

To show the usefulness of the proposed modulator topologies, their system level architectures taken into account the circuit nonidealities were simulated. To get the optimal location of the inband zeros, MATLAB with Schreier's method [8] was used. The other coefficients of the modulators were determined from relations (6)–(8). Then, signal scaling was performed to limit the output swing of the integrators and IIR filters for a real implementation.

The circuit requirements of the proposed architectures such as the amplifier finite dc gain are more relaxed and simulation results show that about 40 dB dc gain for the first integrator is sufficient to prevent any signal-to-noise-plus-distortion ratio (SNDR) degradation with an enough margin (about 10 dB). The proposed architectures have small output swings compared to the conventional distributed feedback and weighted feedforward architectures due to the unity-gain STF and also feedforward paths. The proposed modulators are also stable for an input signal with amplitude slightly greater than that of the feedback reference level. This is mainly due to the unity gain STF and feedforward paths resulting in a wide input signal range and hence large dynamic range.

Fig. 8 shows SNDR versus the sampling paths mismatch of the first integrator and IIR filter of the proposed third-order modulator. As it is seen the SNDR degradation is negligible and the first integrator DAC paths can also be implemented with conventional double sampling integrators.

In Fig. 9 the sampling paths mismatch effect of the fourth-order modulator is shown. In this structure, the SNDR degradation due to the first integrator DAC sampling paths is noticeable. So, the DAC paths are realized using the single capacitor approach. The sampling paths of the remaining integrators and IIR filter are realized employing the conventional double sampled integrators without any considerable performance degradation.

The proposed fifth-order structure is more sensitive to the sampling paths mismatch as it is seen in Fig. 10. But, with single-capacitor realization of DAC paths of the first integrator the performance degradation due to its mismatch is avoided. The second integrator sampling paths capacitors are large due to kT/C noise considerations in a low OSR application. So, a

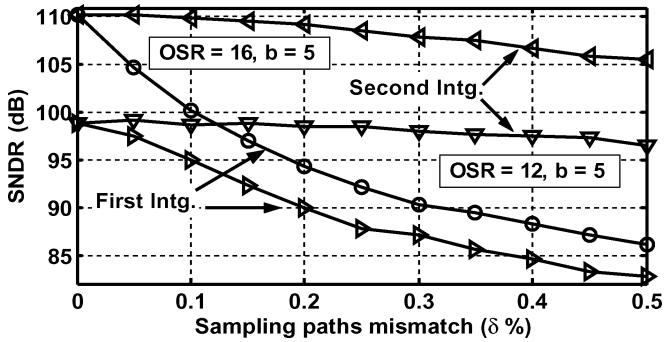

Fig. 9. Sampling paths mismatch effect of the fourth order.

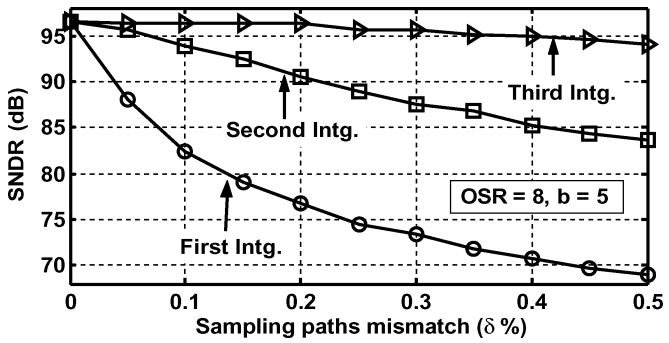

Fig. 10. Sampling paths mismatch effect of the fifth order.

matching better than 0.1% can be obtained that limits the SNDR degradation to less than a few decibels.

The proposed fifth-order structure is more sensitive to the sampling paths mismatch compared to the third and fourth-order structures. This is because in fifth-order structure the out-of-band quantization noise is larger with a lower OSR.

In general, it can readily be shown that the sampling paths mismatch of the integrators and IIR filters in the proposed architectures is shaped with order equal to their standing location in the modulator. For example, the mismatch of the first and second integrators is shaped first and second order, respectively. This is because one order shaping is achieved by placing a zero at $f_s/2$ of the NTF. So, it is possible to get higher order mismatch shaping with placing more zeros of NTF at $f_s/2$. But, any additional zero at $f_s/2$ degrades SNR about 6-dB and needs an extra opamp for its realization.

Another note, if only the single capacitor technique is employed and any additional zero of NTF is not placed at $f_s/2$, the mismatch between the sampling paths of the remaining integrators can degrade the SNR because in this case the mismatch of the second integrator is only first-order shaped like the first integrator in the proposed structures. So, placing a zero at $f_s/2$ of the NTF and using the single capacitor method for realization of the feedback DAC paths of the first integrator is a very efficient structure for the proposed fourth and fifth-order double sampling modulators.

In the simulations, the dc gain and output swing of the integrators, IIR blocks and resonators were 40-dB and 40% of the feedback reference level, respectively and ideal DAC unit elements have been assumed. However, in the real implementations, dynamic element matching (DEM) such as data weighted averaging (DWA) and calibration or correction techniques can be used to correct the DAC errors [1].

IV. Conclusion

In this paper, novel single loop double sampling sigma delta modulator topologies were proposed. To alleviate the quantization noise folding effect into the signal band, an FIR NTF with an additional zero at $f_s/2$ was used. Unity-gain STF was employed to decrease the modulator's sensitivity to the circuit nonidealities. We limited ourselves to the NTF's of the form of (3). However in broad-band applications where the OSR is small, such aggressive NTF's are often needed. Most of the NTF zeros are placed at the inband frequencies to shape out the quantization noise aggressively. In the proposed structures, only one multibit DAC is needed in the feedback loop which greatly decreases the circuit implementation complexity. The DAC implementation is performed using the single capacitor approach in higher order structures to completely remove the noise folding effect. The proposed modulators are suitable for high speed and low voltage applications because they demand more relaxed analog circuit requirements.

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