Characterisation of a Reconfigurable Free Space Optical Interconnect System for Parallel Computing Applications and Experimental Validation Using Rapid Prototyping Technology

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ABSTRACT

Free-space optical interconnects (FSOIs) are widely seen as a potential solution to present and future bandwidth bottlenecks for parallel processing applications.

This thesis will be focused on the study of a particular FSOI system called Optical Highway (OH). The OH is a polarised beam routing system which uses Polarising Beam Splitters and Liquid Crystals (PBS/LC) assemblies to perform reconfigurable interconnection networks. The properties of the OH make it suitable for implementing different passive static networks.

A technology known as Rapid Prototyping (RP) will be employed for the first time in order to create optomechanical structures at low cost and low production times. Off-the-shelf optical components will also be characterised in order to implement the OH. Additionally, properties such as reconfigurability, scalability, tolerance to misalignment and polarisation losses will be analysed. The OH will be modelled at three levels: node, optical stage and architecture. Different designs will be proposed and a particular architecture, Optimised Cut-Through Ring (OCTR), will be experimentally implemented. Finally, based on this architecture, a new set of properties will be defined in order to optimise the efficiency of the optical channels.

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PUBLICATIONS AND PRESENTATIONS

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2. C. J. Moir, R. Gil-Otero, G. Russel and J. F. Snowdon, "Architecture and Tolerancing for Matrix Operations on the Optical Highway", *Optical Engineering,* 45(9), 095401, September 2006.

3. R. Gil-Otero, Craig J. Moir, Gordon Russell, T. Lim, and John F. Snowdon, "Free-Space Optical Interconnected Topologies for Parallel Computer Application and Experimental Implementation using Rapid Prototyping Techniques", *Optical Engineering,* 45(8), 085402, August 2006.

4. R. Gil-Otero, J. Snowdon, "Characterization of a reconfigurable Free-space optical channel", Poster presentation at the Scottish Universities Alliance, SUPA Photonics in Strathclyde University, Glasgow, UK, July 2006.

5. R. Gil-Otero, C.J Moir, T.Lim, G A Russell, J F Snowdon, "Rapid Prototyping for Free-Space optical interconnects", Poster presentation at ECOC Conference in Scottish Exhibition Conference Centre, Glasgow, UK, September 2005.

6. S Kumpatla, R. Gil-Otero, G A Russell, J J Casswell, C J Moir, J F Snowdon, "Optically Interconnected Computing (OIC) Group", Poster presentation at the Scottish Universities Alliance, SUPA Conference in Strathclyde University ,Glasgow, UK, May 2005.

7. Rafael Gil-Otero, G. A. Russell, T.Lim, K. J. Symington, J. Snowdon, "Design of a 3 dimensional optical interconnect architecture based on free space", Oral presentation in PREP Conference, Lancaster, UK, March 2005.

Chapter 1
Introduction

1.1 Introduction and Thesis Outline

The world's Information Technology industry is moving a step closer towards incorporating photonics with the aim of overcoming bandwidth bottlenecks. The recent development of the first electrically driven Hybrid Silicon Laser for Intel at the University of Santa Barbara [1] is a good example of technological advancements toward standard high-volume, low-cost silicon manufacture techniques available for integrating silicon photonic chips.

For communication technology, fiber-based optical interconnects have already proven their advantages over electrical interconnects over long distances. However, for the new era of parallel computing applications where high bandwidth is required over relatively short distances (<1m), the utilisation of fiber becomes difficult and costly.

Free-Space Optical Interconnection (FSOI) networks are particularly attractive for connecting many nodes in a complex topology, where a node may be a board or a chip. Potential applications occur both in multiprocessor computing systems and switching systems. Several architectures exploiting this technology have been designed. These systems are generally based on an optical system, often referred to as an optical bus which comprises several image relay stages in a linear (or ring) topology [2], [3], [4].

This thesis is focused on the study of a particular FSOI system called Optical Highway (OH) [2],[5]. OH is a polarised beam routing system which provides a very high spatial and temporal bandwidth to which a large number of nodes (processors with associated memory) can be connected. The objective of the research is to analyse and characterise devices and technologies that can be useful for implementing the OH. A diverse number of OH architectures is proposed and different properties of the OH such as reconfigurability, scalability, tolerance to misalignment and polarisation losses will also be under research.

This first chapter, will present a general overview of the limitations of current electrical interconnects and computer technologies. It will also analyse the influence of these limitations on new computer architectures based on parallel processing that are being employed to fulfil the requirements for present and future computers. The last part of the chapter will present the advantages of optoelectronic systems over electronics for solving communication problems.

Chapter 2 will show the advantages of FSOI systems over other optical communication systems. The state-of-the-art in FSOI technology will also be analysed and the OH will be presented as the FSOI system under study in this thesis. The last part of this chapter will propose a novel design of the OH that exploits the properties of FSOIs such as reconfigurability, which is achieved by using Liquid Crystals (LC).

In Chapter 3, new 'off-the-shelf' optical components will be proposed and tested for using as optical stages of the OH. A technology known as Rapid Prototyping (RP) will also be employed for the first time in order to implement optomechanical structures at low cost and low production times. Then, the optomechanical system will be used to undertake a first estimation of the scalability of the system, which will be compared theoretically.

Chapter 4 will characterise a more suitable set of optical components including 90° Twisted Nematic Liquid Crystals (TNLC) which will allow us to achieve more optimum results. Then, the reconfigurable properties of one channel of the OH will be tested using Eye Diagrams (ED) as an analysing technique. The chapter will conclude with the analysis of a second method used to estimate the scalability of the system.

Chapter 5 will analyse the requirements for designing efficient OH architectures. Different designs of the OH at different levels will also be presented and characteristics such as performance, cost, efficiency and redundancy will be taken into account.

Chapter 6 will focus on the construction, assembly and proof-of-work of a particular architecture, the Optimised Cut-Through Ring (OCTR) architecture, proposed in Chapter 5. This architecture will be used to interconnect 8 nodes and different properties of free space optical signals in general and the OH in particular will be tested.

Finally, Chapter 7 concludes this dissertation and outlines some potential areas of future research.

1.2 Motivation

The motivation for this research comes from the need to find a solution to the limitations of the use of electrical interconnects for short, high-bandwidth links such as input/output (I/O) buses and memory buses links. We will show how electrical interconnects slow down the performance of computer system components such as processors, memories and I/Os and increase the gap in performance between them.
This thesis is also motivated by the bigger role that computer manufacturers are giving to parallel processing as the main solution for maintaining Moore's law. One of the major challenges of multiprocessor systems is the communication data between processors, symmetric multiprocessors (SMP) or system buses where, currently very high bandwidth and low latency are required.

1.2.1 Electrical Interconnect Limitations.

Current technology in CMOS electronics operates chip speeds in multi-GHz clock rates and transistor gates down to 90 nm. Thus Moore's Law does not seem to be slowing down in the near future according to the 2003 ITRS Roadmap [6]. Yet, electrical interconnects do not seem poised to keep up. Metal wires are currently being used to connect chips to boards (links ~10-cm long), boards to boards (~50 cm), router linecards to each other (~3 m) and so on. Unfortunately, at frequencies above 5 GHz, a copper wire along an internet router backplane fails to act as a simple electrical signal channel [7]. The many imperfections of the metallic interconnect such as frequency-dependent loss, impedance mismatching and skin depth, complicate the transmitter circuitry. To some extent, these problems can be overcome at a cost of electrical power consumption. However, since the heat extraction from CMOS chips has recently become a serious problem ([6], [8]) reducing electrical power consumption has developed into a high-priority design issue.

In the following sections, we take a closer look at each of the major issues with electrical interconnects.

Frequency-Dependent Loss

Mohammed et al. at Intel [9] simulated a 20-inch electrical interconnect on a standard printed circuit board using parameters for the material FR4. Their results, shown in their Figure 1.1, indicate that there is an insertion loss of about -25 dB at 5 GHz and about -45 dB at 10 GHz. At higher signal frequencies, the losses in the electrical interconnect gets even worse. In absolute terms, this amount of loss is severe, and the variation in loss with respect to frequency causes signal distortion.

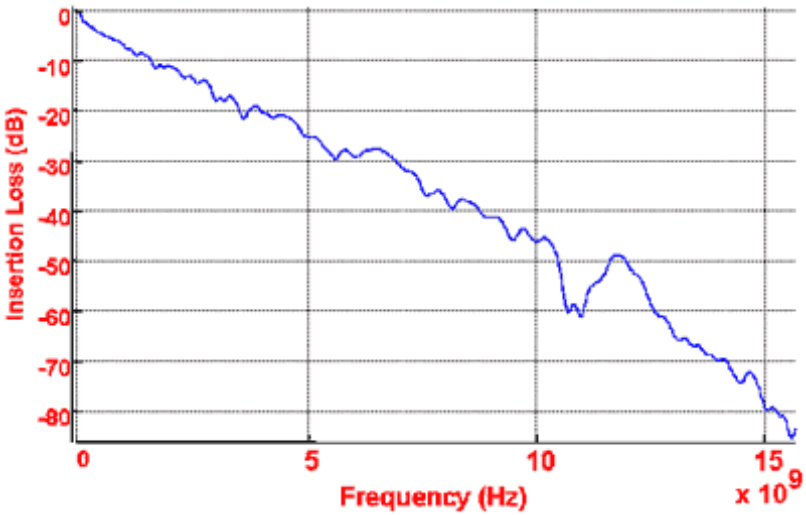


Figure 1.1. Simulation of 20" channel transmitter [9].

A process called equalization can compensate for this aspect of the channel by amplifying frequency components that are more strongly attenuated during the transmission. Equalization, however, requires previous knowledge of the data transfer rate and of the channel characteristics (or at least some active method of determining the characteristics) and consumes valuable chip area and electrical power [9]. As the bit rates increase, the loss of the electrical channel gets worse and equalization schemes will only become less practical.

A second consequence of the frequency-dependent loss of the electrical channel is the so-called "aspect-ratio limit" of electrical lines [10], [11]. The capacity of an electrical interconnect system, B_{MAX}, is essentially limited by the total cross-section, A, and the length, L:

$$B_{MAX} = B_0 \times \frac{A}{L^2} \qquad \text{Equation 1.1}$$

The constant B_0 is related to the resistivity of the interconnect and is only weakly dependent on the fabrication technique. For copper, it is about 10^{14}bits^{-1} in a co-axial cable, 10^{15}bits^{-1} in a multi-chip module (MCM) and 10^{16}bits^{-1} in cross-chip lines.
Since the distance that must be traveled by the signal and the size of the chips are usually fixed in a system, the maximum aspect-ratio can be calculated and thus, the maximum aggregate data rate is known. In other words, it does not matter what specific architecture is implemented (many small wires or a few large wires) as filling a particular volume with information-carrying wires will result in the ability to transmit only a certain amount of data per second. Advanced techniques such as multilevel coding and repeatering can be used to extend this limit, but these techniques consume additional power [7].

Impedance Mismatching

Another major problem is to construct electronic transmission lines (board-to-board interconnects) with uniform characteristic impedance.

In a practical computer or router system, the electronic boards are plugged into a backplane which connects the many boards to each other. A signal generated on one board, for example, must pass through the ball grid array on the transmitter chip onto the printed circuit board, travel along a metal trace on the board, cross over to the backplane through a connector, along the backplane, through another connector, along another board, and through another ball grid array in order to arrive at the receiver circuit. At each interface, two traces come together in a way that is likely to contain some discontinuities in the size and shape of the joint between them. Electrical signals passing through such discontinuities generate reflections due to the impedance mismatch at the interface [7], [12]. It is essential to minimised these reflections because they can cause intersymbol interference (ISI). ISI means the information in one bit is corrupted by the energy or information in some other bit(s) in the data stream. ISI, in this case, is essentially an ‘echo’ – the first part of a signal tries to pass these interfaces but some of the energy is reflected, and when it comes back in the same direction a split second later this ‘echo’ gets superimposed with the signal that is currently trying to pass the interface for the first time. Note that reflections are not the only cause of ISI. Other channel imperfections such as dispersion can lead to ISI as the energy from one bit corrupts the adjacent bits in time.

Crosstalk

As the highest frequency in an electrical signal approaches 5-10 GHz, a wire with an oscillating electric field at that frequency will be emitting radiation that will affect the nearby wires. Thus, a signal that is supposed to be confined to one wire will actually be contributing to the energy or signal carried on another. This "crosstalk" is obviously noise on the receiving signal that degrades the ability of the receiver circuit to properly distinguish the digital levels. The large amount of data that must pass through a chip's I/O, requires a dense array of interconnects. If an electrical interconnect scheme is utilised, each line must be well protected in order to avoid any possibility of crosstalk

Power

A major problem with electronic interconnects is the power dissipated in terminating resistors, especially in conventional complimentary metal oxide semiconductor (CMOS) signalling. Complex architectures such as rack and blade systems are crowded with copper lines which drain power, generate heat, and force system designers into placing the hottest components right next to each other. The result is that some blade servers can not be fully populated with the latest processors and workloads may have to be offloaded to cooler systems to avoid overheating.

Reducing electrical power consumption has developed into a high-priority design issue. Thus, the growth in power consumption must be stopped whilst still gaining performance. Voltage scaling techniques will help spread out the thermal management problem. However, electrical noise will become an issue limiting voltage scaling and also device performance since at very low VCC voltages, reduced signal to noise ratios will lead to increases in bit errors and thus frequent transient processor failure.

Pin Density

The exponential growth in transistor densities, as predicted by Moore in 1965, has lead to smaller faster chips. However, the number of I/O pins connecting the chips to the outside world is not improving at the same rate as transistor performance.

Higher clock speeds have increased the amount of data required to keep the chips 'fed' with data. To avoid increasing the frequency of the I/O pins operation, increasingly more pins are required. At the same time the chips are reducing in size and, because of the planar nature of electronic design, the space available around the chip for

connections is shrinking. The size of the I/O pins cannot be reduced much further because of bandwidth limitation imposed by reducing the cross-sectional area and by increasing difficulties in working with very fine metal wire. According to the 2004 ITRS roadmap [13], the number of pins available per chip will increase at a rate of approximately 11% per year over the next fifteen years. This is a much lower rate than the predicted rate of increase in the number of transistors per chip, which is projected at 26% per year in the same period.

Even though pins are expected to run at a higher frequency thus increasing the effective bandwidth, the on-chip frequency will increase at the same rate [13], which will offset the increase in pin frequency. In addition, the cost per pin is predicted to decrease at a lower rate (~5%) than that of the increase in the number of pins [13]. This means that the overall cost of packaging will increase at a rate of approximately 5% a year. If no effort is made to reduce the cost further (or reduce the rate of increase in the number of pins), the total packaging cost will double in the next fifteen years, a trend that is opposite to other design cost trends.

1.2.2 Influence of Electrical Interconnects on Memory Performance.

Over the past few decades, transistor performance has been improving at a much faster rate compared to memory performance. Figure 1.2 plots the evolution of CPU performance against the historical performance improvement in time to access main memory.

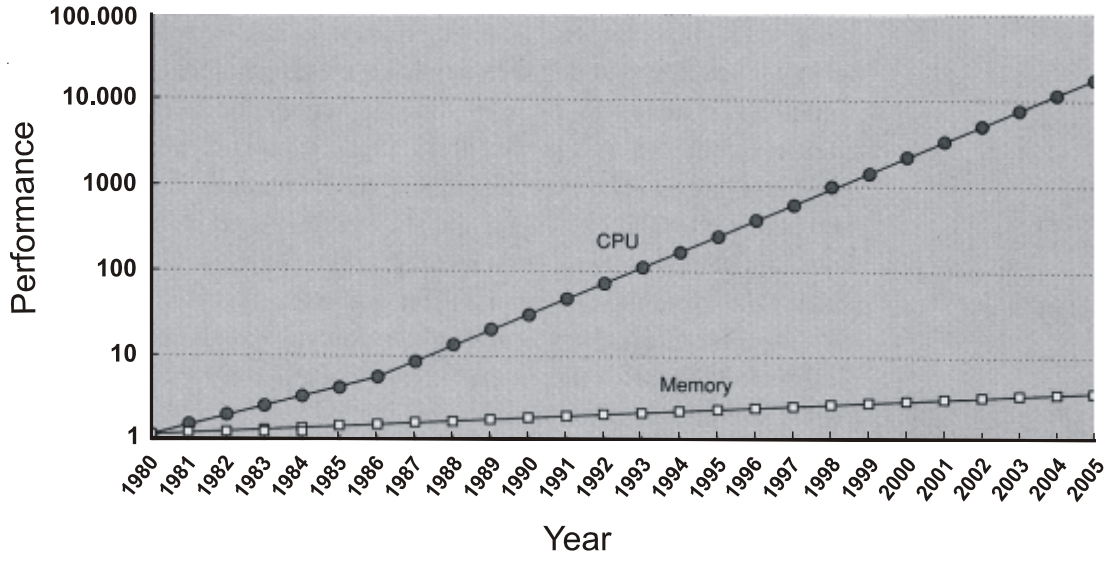


Figure 1.2. Evolution of Memory and CPU Performance [14].

DRAM is the memory technology that is used almost exclusively for direct communication with the CPU. Therefore, it is a key technology to the overall performance of electronic computing systems because memory deployed in its current form is significantly slower that the microprocessor. For example, while leading edge processors are now operating at 4 GHz, present generation memory is only capable of a 400 MHz performance. This disparity results in a condition generally referred to as the 'memory wall'. In such conditions, the CPU must remain in a wait state until the memory data is written or retrieved.

The 2004 ITRS Roadmap [13] predicts that transistor speed will continue to improve at a much faster annual rate (21%) over the next fifteen years compared to the rate of improvement in DRAM latency (10%). Thus, even though each is improving exponentially, the exponent for the microprocessor is substantially larger than that for the DRAMs. The difference between diverging exponentials also grows exponentially, so although the disparity between processor and memory speed is already an issue, it will become a much bigger one. Therefore, computer designers are faced with an increasing processor - memory performance gap, which now is the primary obstacle to improve computer system performance. Part of this disparity is due to the limits of current interconnection design, the memory bus, which often results, particularly at higher frequencies, in disturbances that contribute to signal distortion.

In addition, because of the growing memory access latencies (measured in processor cycles), any request that misses in the caches may eventually take hundred of cycles to satisfy. Thus, system speed will now be dominated by memory performance. This problem can be solved by reducing the average memory access time, which depend on three factors; Hit time, Miss penalty and Miss rate. In reference [14] different latency tolerances (or reduction) techniques are presented. However, these techniques increase the processor's memory bandwidth needs by causing the processor to request the same stream of operands in less time or by causing the processor to request more data from memory. Thus, the two factors of memory latency and memory bandwidth are closely related. Improvement in memory bandwidth is critically necessary to support novel memory latency techniques. There are a wide range of techniques to improve effective memory bandwidth. One of the most important includes the use of wider and faster connection to memory [15].

Traditional approaches to improving the memory bandwidth include the speeding up of the memory clock (this is to reduce the access latencies), increasing the bus width, or both. For conventional DRAMs, these approaches are reaching their practical limits. While clock rate scaling causes tight system timing requirements, which dictate precise component and PCB modelling, the increase of bus width comes at the expense of increasing the pin count, increasing I/O power, and creating multitude of mechanical and PCB layout problems.

1.2.3 Influence of Electrical Interconnects on Processor Performance and the New Era of Parallel Processing.

When compared with the original bus interface on the Intel 8088 processor used by IBM in the first IBM PC, we find that available bus performance has increased significantly. The original 8088 processor had an 8 bit wide data bus operating at 4.77 MHz. The peak data bandwidth, product of the bus frequency and the data bus width, was therefore 419 Mbit/s or 4.77 Mbyte/s. When compared with this bus, the current highest performance general purpose peripheral bus available (the PCI-Express) has widened by a factor of 8 and its signaling speed has increased by a factor of 28 for an overall improvement in peak bandwidth of approximately 2000% [14]. Owing to improvements in bus utilization the improvement of actual bandwidth over the last 20 years has been even more dramatic than this, as has the improvement in actual processor performance. While the growth in bus performance over the last several years has been impressive there are many indications that a new approach must be taken for it to continue.

Figure 1.3, [16], shows the exponential growth of processor performance over the last 30 years compared to the slower growth of processor bus frequency over that same period of time. The MHz scale of the chart is logarithmic and the difference between the core CPU performance, represented by the clock frequency, and the available bandwidth to the CPU, represented by the bus frequency, continues to grow.

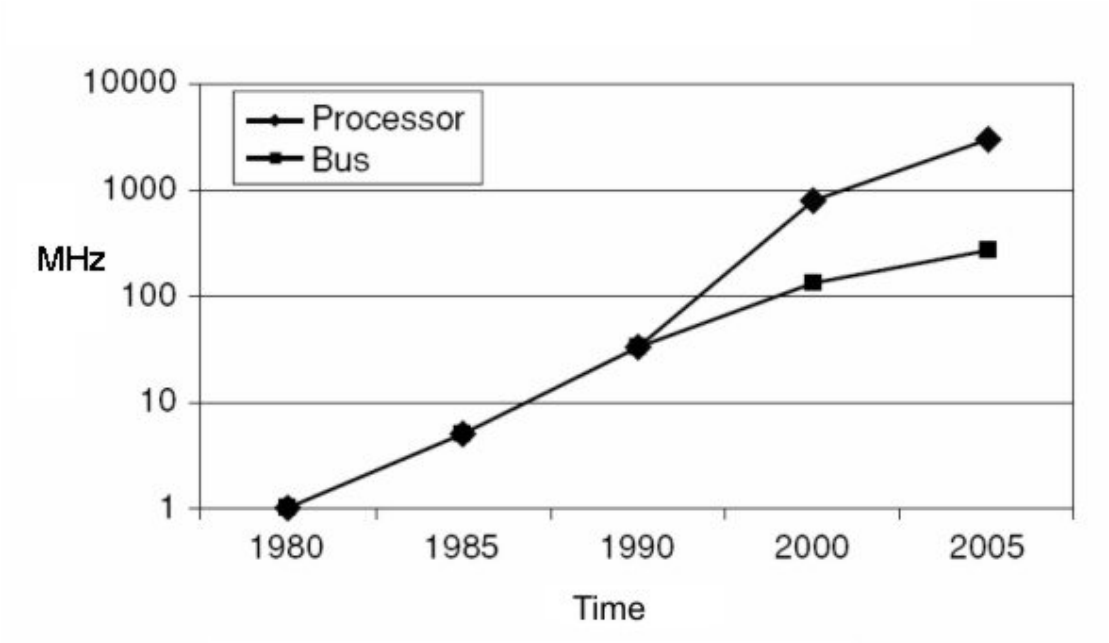


Figure 1.3. Frequency and bandwidth growth [16].

The connections between processors and peripherals have been traditionally, shared buses and often a hierarchy of buses. Devices are placed at the appropriate level in the hierarchy according to the performance level they require. Low-performance devices are placed on lower-performance buses, which are bridged to the higher-performance buses so they do not overload the higher-performance devices.

Traditional external buses used on more complex semiconductor processing devices such as microprocessors are made up of three sets of pins, which are soldered to wire traces on printed circuit boards. These three categories of pins or traces are address, data and control. The address pins provide unique context information that identifies the data. The data is the information that is being transferred and the control pins are used to manage the transfer of data across the bus. For a very typical bus on a mainstream processor there will be 64 pins dedicated to data, with an additional eight pins for parity protection on the data pins. There will be 32–40 pins dedicated to address with 4 or 5 pins of parity protection on the address pins and there will be approximately another 30 pins for control signaling between the various devices sharing the bus. This will bring the pin count for a typical bus interface to approximately 150. Due to of the way that semiconductor devices are built; there will also be a large complement of additional power and ground pins associated with the bus. These additional pins might add another 50 pins to the bus interface pin requirement, raising the total pin count attributed to the bus alone to 200. This 200 pin interface might add several dollars to the packaging and

testing cost of a semiconductor device. The 200 wires traces that would be required on the circuit board would add cost and complexity as well. If the bus is needed to cross a backplane to another board, connectors would need to be found that would bridge the signals between two boards without introducing unwanted noise, signal degradation and cost. Then, if it is assumed that the system will require the connection of 20 devices to achieve the desired functionality, we begin to understand the role that the bus can play in limiting the functionality and feasibility of complex embedded systems.

The use of cache memory and more advanced processor microarchitectures has helped to reduce the growing gap between CPU performance and available bus bandwidth. Increasingly, processors are being developed with large integrated cache memories and directly integrated memory controllers. However, multiple levels of on- and off-chip cache memory and directly integrated memory controllers, while useful for reducing the gap between a processor's data demands and the ability of its buses to provide the data, does little to support the connection of the processor to external peripheral devices or the connection of multiple processors together in multiprocessing (MP) systems.
In addition to the increasing performance of processors, the need for higher levels of bus performance is also driven by two other key factors: First, the need for higher raw data bandwidth to support higher peripheral device performance requirements. Second the need for more system concurrency. The overall system bandwidth requirements have also increased because of the increasing use of Direct Memory Access (DMA) smart processor-based peripherals and multiprocessing in systems.

Parallel Processing

Multiprocessing is increasingly seen as a viable approach to adding more processing capability to a system. Historically, multiprocessing was used only in the very highest end computing systems and typically at great cost. However, the continuing advance of semiconductor process technology has made multi-processing a more dominant technology and its use can offer advantages beyond higher processing performance. It is believed that parallel processors will definitely have a bigger role in the future. This view is driven by three observations [14]. First, there appears to be slow but steady progress in one of the major obstacles to widespread use of parallel processors, software. This progress is probably faster in server and embedded applications, which exhibit natural parallelism and currently can be exploited without the trouble of rewriting a gigantic software base. Second, it is unclear whether architectural innovation

that has been based for more than 15 years on increased exploitation of instruction-level parallelism (ILP) can be sustained indefinitely. Modern multiple-issue processors have become incredibly complex, and the performance achieved through increasing complexity, silicon technology and power seem to be decreasing. Third, since microprocessors are likely to remain the dominant uniprocessor technology, the logical way to improve performance beyond a single processor is by connecting multiple microprocessors together. This combination is likely to be more cost-effective than designing a custom processor. The use of multiprocessing may also reduce the total system power dissipation at a given performance point. This occurs because it is often possible to operate a processor at a reduced frequency and achieve greatly reduced power dissipation.

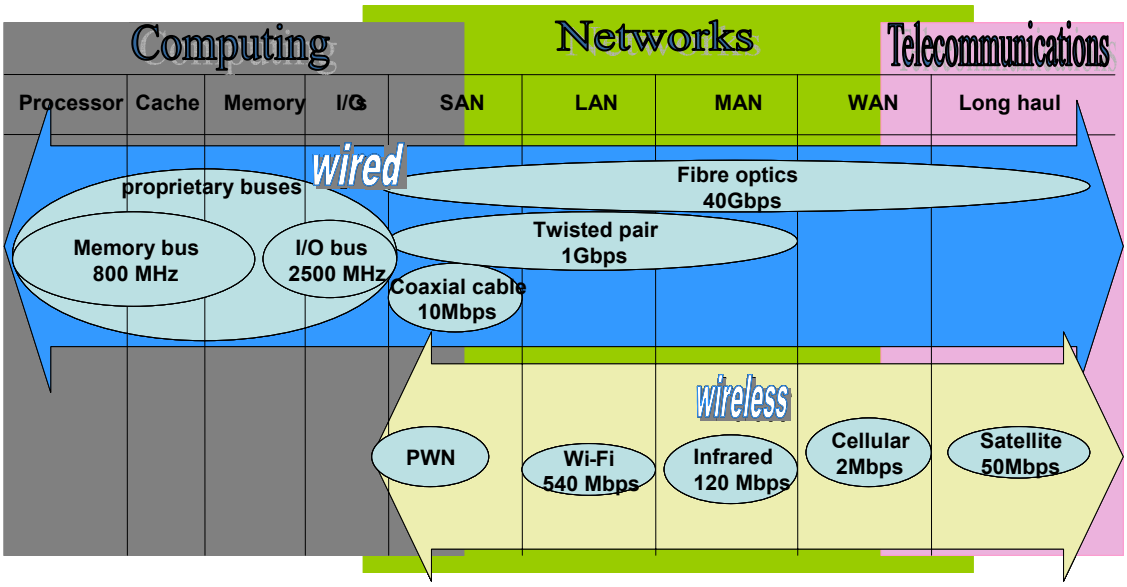
While many obstacles to multiprocessing have been reduced or removed, the processor interconnect has increasingly become the main limiting factor in the development of multiprocessing systems. Existing multiprocessor bus technologies restrict the shared bandwidth for a group of processors. For example, in existing multiprocessors systems, communication of data between processors may cost anywhere from 100 clock cycles to over 1000 clock cycles, depending on the communication mechanism, the type of interconnect, and the scale of the multiprocessor. For multiprocessing to be effective, the processors in a system must be able to communicate with each other at high bandwidth and low latency.

1.3 Using Optics in Computers

The use of optical interconnects is often cited as having potentially great advantages over the use of electronic technology. In fact, optical communication has already transformed the telecommunications industry, Figure 1.4. Today, Wide Area Networks (WANs) based on fiber-optics have permeated every aspect of terrestrial communication. The success of fiber-optic insertion in telephone systems and the promise of economies of scale from a larger component market resulted in adoption of optics for Metropolitan Area Networks (MAN) and Local Area Network (LAN) connectivity where low-cost is a dominant factor. The Gigabit Ethernet standard (IEE 802.3z) of 1998 and the 10 Gigabit Ethernet standard (IEEE 802.3ae) in progress since 2001 are representative of the adoption of fiber-optics for the LAN environment.

Recently, optics has been used to solve a different class of problems in Store Area Networks. In these networks the link distance is less than 300m, so the advantage of optics for long-distance transmission is not important. However, electrical interconnections simply can not provide the needed bandwidth density and this is where optics has another distinct advantage.

The use of optics in computers is oriented to tackle the electronics and architectural problems presented in the previous section. However, before considering new computer architectures based in optics we should be sure that it must be nearly impossible to build an equivalent system with pure electronics within a prolonged future. Therefore, it is important to know the advantages and a disadvantage of optics over electronics for interconnects.



Figue 1.4 Nowadays, optics is used for both wired and wireless communications in the networks and telecommunications world. Because of the low attenuation and less need for repeaters than twisted pair and coaxial cables, fibre is the most economic choice for telecommunication and WAN's. For smaller networks fibre optics is employed when high bandwidth is required, and for wireless communications, optics (infrared) is a commercial solution for low cost and quick installation MAN's. The many advantages of optics can also be used in the near future for solving the interconnect problems of the computing world.

1.3.1 Optical Interconnects

The difference between electronics and optics is essentially the difference between the electron and the photon. Since electrons carry mass and charge they interact very strongly with each other making them ideally suited for switching. Photons, on the other hand, do not carry mass or charge and are therefore non-interacting in free-space. This makes them ideally suited for interconnection since, as we will see optics can avoid complex problems of electrical interconnect bus design such as signal and clock distortion, high-frequency attenuation, temperature dependence, wave reflection and impedance matching phenomena. In addition, the optics itself does not need to be redesigned, in contrast to electrical bus, as the clock rate on the bus is increased.

Frequency-Dependent Loss

The information channel in the case of optical interconnects is either free space (air or glass) or optical fiber (glass). The frequency-dependent distortion for an optical signal in either material does not have any comparable limit with that of an electrical signal because it does not have the resistive loss physics. Optics does not rely on wires with their associated resistance and capacitance. Therefore, it can avoid problems such as signal and clock distortion and high-frequency attenuation. Moreover, at the relevant frequencies, neither material absorbs or scatters much of the energy over a large range of frequencies. The attenuation of optical fiber is around 0.2dB/km at the optimum wavelength of 1550 nm. Thus, almost all the energy sent into the fiber reaches the receiver. For free space optical communication the attenuation highly depends on weather conditions. However, for the distances dealt with in this thesis (generally indoor and <1m) weather conditions are not taken into account and attenuation of 0.43 dB/km (in clear air conditions for infrared wavelength) can be considered. This implies that a short-distance optical system would have little or no need for equalisation or repeaters, saving power and reducing the thermal load.

Impedance Mismatching

Impedance matching in optical systems is achieved simply by utilising antireflection coatings [11]. Because the refractive index of the materials remain relatively constant over the optical frequency range of interest, an impedance matching layer is sufficient for all signals. The simplest anti-reflection coating between media with refractive

indices n_1 and n_2 is a single layer of material with a properly chosen thickness ($t = \lambda/(2n)$) and index of refraction ($n = \sqrt{(n_1 n_2)}$).

Crosstalk

Reduced crosstalk due to electromagnetic interference is another significant advantage of optical systems [11]. The short wavelength of optical waves (~ 1μm) allows the energy in the beam to be focused down to a small spot at the detector. Thousands of individual beams can be imaged simultaneously using a single lens without significant cross-talk.

Pin Density

Optics can provide a potential solution to this problem. It is quite easy to manufacture arrays of optoelectronic devices with their optical I/Os normal to the chip. It is also feasible to have the I/O connected across the whole area of the chip by placing electronic I/O pads across the chip on top [17]. This has the advantage of allowing the surface area and not the edges of the chip to be used for I/O. In this case, the solder links between the electronic chip and the optoelectronic chip would be very short so the bandwidth can remain very high.

Other Factors

Optical technologies have also other advantages over electronics for interconnections. These are as follows:

- *Larger number of fan-ins and fan-outs*

  As a single beam of light can be sent to many detectors, by using a DOE for example, (fan-out) and many beams can reach one detector (fan-in). The power losses and lack of I/Os limit the electronics fan-ins and fan-outs.

- *Lower signal and clock skew*

  The narrow band nature of light, compared with the broad band nature of an electronic signal, means lower dispersion when the signal travels through an interconnection media and, therefore, less spreading of signals.

- *Potential for reconfigurable interconnect*

  Optical interconnects can make use of the greater number of available degrees of freedom optically available (such as polarisation and wavelength) to create multiple paths, which can be taken dependent on a controllable property of the carrier beam.

Table 1.1 summarises the most significant difference between electronic and optics for interconnect applications.

	Electronic	Optics
Transmission	▪ Wires	▪ Fiber, Free Space and Guide Wave
Attributes of Signal	▪ Amplitude-phase ▪ Signal spectrum ▪ Modulation ▪ Pulse width/spectrum ▪ Power	▪ Amplitude-phase ▪ Signal spectrum ▪ Modulation ▪ Pulse width/spectrum ▪ Power ▪ Coherence ▪ Light spectrum ▪ Polarisation ▪ Spatial distribution ▪ Spatial mode content
Density	▪ Overlapping or crossing of lines not allowed ▪ Size of the signal limited by the wire ▪ Planar technology	▪ Overlapping and crossing allowed (free-space) ▪ Size of the beam limited by diffraction ▪ 3D allowed. Ideal for parallel computer
Delay	▪ Max. signal propagation speed ~ 0.1mm/ps ▪ Signal propagation speed ~1/C' ~ interconnection density	▪ Max. signal propagation speed ~ 0.3mm/ps ▪ The signal propagation speed does not depend on the interconnection density
Bandwidth	▪ The density of electrical interconnections is affected by the bandwidth carried by each connection (because of parasitic C' and L' effects) ▪ Max bandwidth limit of any electrical system	▪ The density of optical interconnections is not affected by the bandwidth carried by each connection. ▪ The bandwidth depends primarily on thermal and real state considerations.
Power	▪ Matching impedance needed at the end of the line to avoid reflections => large power expenditure	▪ Power requirements mainly limited by the sensitivity of the photodectors, the efficiency of the conversions and the transmission efficiencies
Noise	▪ High noise features	▪ Low noise features
Technology & Material	▪ Easy (CMOS), low cost. All Si possible	▪ Complicated (III-V materials, hybrid integration). High cost.
heat	▪ Electrical wires generate heat	▪ Optical interconnects do not generate heat
Alignment	▪ Low sensitivity to misalignment	▪ Extremely sensitive to misalignment

Table 1.1 Electronics versus Optics for interconnect applications.

From Table 1.1, it is clear that optics has potential advantages over electronics for interconnection. However, it also outlines the main problem for the implementation of optics over short distances, which is the cost.

The primary barrier to extensive use of optics at short ranges is the cost of conversion from electrical to optical and back again. Silicon photonics holds the potential to create low-cost, highly integrated optical components using the same CMOS-based manufacturing techniques that have revolutionised the electronics industry over the past 40 years. Unfortunately, silicon's indirect bandgap makes light emission in the bulk material highly inefficient. Thus, it is extremely difficult to fabricate any kind of light emitter with this material. A high effort has been made to overcome this problem. However, to date, an electrically pumped pure silicon laser has not been demonstrated. Until an electrically pumped silicon laser is demonstrated, III-V semiconductor materials will continue to be necessary to produce communication lasers. The question then is to determine how these optical sources can be integrated cost-effectively onto a silicon photonic chip.

As mentioned at the beginning of the chapter, a breakthrough has been made by Intel at the University of Santa Barbara [1] with the recent development of the first electrically driven Hybrid Silicon Laser which has overcome many problems inherent in the previous integration by employing a volume-manufacturable wafer-bonding process which allows the fabrication of multiple hybrid lasers without the need for alignment, which is a critical costly step.

This is an example of how the world's Information Technology industry is moving a step closer towards incorporating photonics, and Figure 1.5 shows the prediction made by Intel where the transition period for changing from electronic to optics depend on how long Cu technology can hold with the high demand of bandwidth and when optical interconnect will be costly effective.

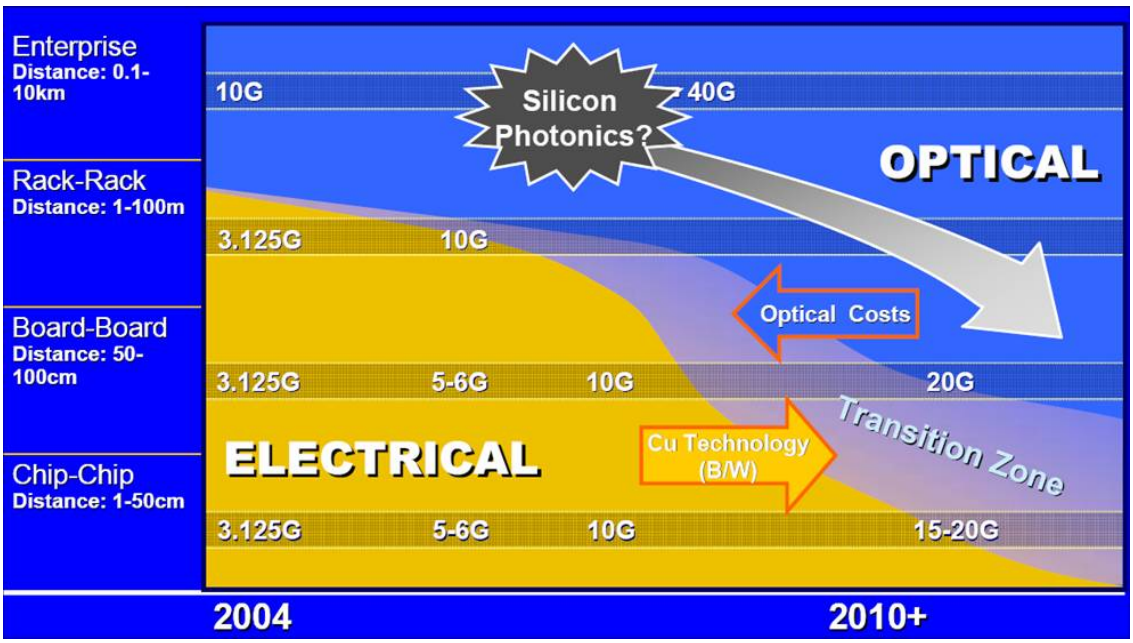


Figure 1.5. Prediction of interconnect technology evolution [18].

For the distances dealt with in this thesis (on card and multi-chip-level <1m) a cost effective solution will not be available in the near future. However, sometime after 2015 the interconnect industry based on electronic technology does not have any known solution for feeding the terabits of information needed for future multiprocessors architectures [19]. Therefore, it is believed that between 2015 and 2020, optics can start to be employed at this level [18].

1.4 Conclusion

This introductory chapter has analysed the physical limitations of electrical interconnects and their effects on memory and processor performance. The interconnect requirements for the new era of parallel processing and how the advantages of optics over electronics can fulfil these requirements have also been analysed. Although, cost is currently the main factor that impedes a wide acceptance of optics, we believe that faster increase of optics over electronics technology will lead in the future to the use of optics for short distances.

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Chapter 2
Free Space Optical Interconnects for Parallel Computer Applications

2.1 Introduction

The previous chapter demonstrated the problems of electronic interconnects and the potential of optics, especially for communication technology where fiber-based optical interconnects have already proven its advantage over electrical interconnects over long distances.

This chapter introduces FSOI technology for short distance communications. The advantages of FSOIs over other interconnect technologies and the current state-of-the-art in this field will be analysed. A particular FSOI system known as Optical Highway (OH) will also be examined. This system, proposed by the OIC group at Heriot-Watt University, provides a very high spatial and temporal bandwidth to which a large number of nodes can be connected in an arbitrary topology. This section will propose for first time new concepts and ways of improve the OH.

2.2 Free Space Optical Interconnect Networks and Current State-of-the-Art

Optics has been discussed as a future technology in computers in many articles which describe a wide variation of non-pure electronic systems [1],[2],[3],[4]. Despite this, optics has still not reached its full impact. As it was said in the previous chapter, cost is a major drawback that impedes the wide acceptance of optics. However, there are other factors such as misalignment, losses and crosstalk that also contribute to the slow development of this field. In any case, it seems clear that the key to success will not just consist of replacing electrical wires since many properties of optics will be wasted using that strategy. Instead, new computer architectures based on the best characteristics of both optics and electronics should be developed. If solutions could be found that utilise properties of optics such as transmission in all spatial dimension (an extra dimension compared to two dimensional electrical planes), light coherence, high bandwidth,

multiple wavelengths, immunity to electro-magnetic interference [1], together with the complementary characteristics of electronics, then we could also build new competitive systems.

This thesis focuses on parallel computer systems rather than processor design. Parallel computer systems have to deal with extreme bandwidths. Therefore it is natural to replace the information highways with optoelectronic interconnects, and thus utilise optical properties.

In Figure 2.1 we describe the ideas of Ozaktas' Tree [2],[3] where a systematic method (an architecture tree) is used to find the most promising parallel computer architecture by weighing the pros and cons of many design possibilities and removing the idea that is considered to be inferior to another.

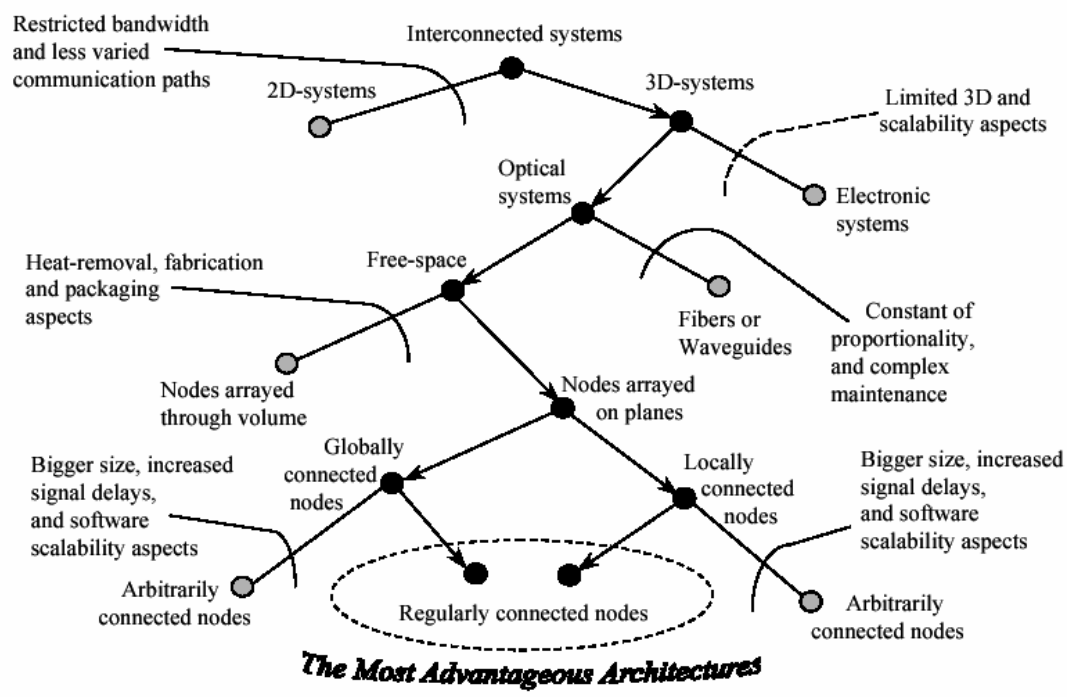

Figure 2.1. Ozaktas' Tree. Description of the most advantageous architectures [4].

Note that the result of the architecture tree seems to favour regular, globally or locally interconnected 3D-systems using free space communication between nodes arrayed through planes. Ozaktas' Tree differs from Figure 2.1, however, since all locally connected systems are also pruned in favour of globally connected systems. He argues that these systems will use fewer time steps to complete a certain operation, and that the system growth rate will not increase compared to locally connected systems due to the requirement to have large distances between nodes to remove the heat. On the other

hand, H. Forsberg [4] argues that complex global architectures also suggest that we should use micro-optical systems and this could be a problem in reference to bisection bandwidth because of diffraction effects. Thus, he decides to keep the locally connected systems branch in order to allow the possibility of using macro-optic systems.

A significant point of Ozaktas' scheme is the election of free space over fiber optics. For communication technology fiber-based optical interconnects have already proven their advantage over electrical interconnects over long distances. However, for parallel computing applications where high bandwidth is required over short distances (mm-m) the utilisation of fiber becomes difficult and costly, and it would limit the possibilities of optics over electronics [2],[3],[4].

2.2.1 Technology and Integration of Free Space Optical Interconnected Systems

This section examines the device technologies that enable FSOIs and its integration. It will illustrate some of today's key technologies paying particular attention to 2D arrays of devices such as transmitters, detectors, lenses and interconnects that allow spatial parallelism and, therefore, the creation of high-density optical interconnect or buses used to construct FSOI systems.

Transmitter

Optoelectronic computing systems combine electronic circuits with optical interconnects. Compared with all-electronic systems, an additional subsystem is necessary to provide electro-optical signal conversion and proper optical signal routing. This additional subsystem begins at the transmitter driver input and ends at the detector-amplified output. The transmitter can be either light modulators or light emitters. Modulators differ from emitters in that they transfer information onto an incident optical channel either by changing transmission, reflection or re-routing the beam of an external laser source. Most of the modulators used in FSOI systems are based on multiple quantum well (MQW) structures [5] which, depending on the potential difference across its active region, either absorb any input signal or reflect it along the modulated output path.

The fact that modulators are not subject to carrier photons allows them, under certain circumstances [6], to be used at higher speeds than emitters. Unfortunately, this is also the principal drawback of modulators which rely on an external optical source. Manufacturers generally wish to construct systems as efficiently as possible using a single process technology and, if feasible, on a single chip. The requirement of separate modulators and emitters, plus associated alignment, may add unnecessary complexity.

The other transmitter technology, emitters, can either be light emitting diodes (LED) [7], laser diodes (LD) [8] or, more frequently, vertical cavity surface emitting laser (VCSEL) [9]. The VCSEL has an optical cavity axis along the direction of current flow rather than perpendicular to the current flow as in conventional LDs. The active region length is very short compared with the lateral dimensions so that the radiation emerges from the surface of the cavity rather than from its edge. This simplifies fabrication and lowers production costs.

Although some typical drawbacks associated with VCSELs such as the high threshold current and voltage have been solved [6], there are a number of problems that are still subject to ongoing research. For example, the power consumption and heat generation associated with biasing and modulation of a VCSEL can change the properties of the lasers in large arrays [6]. In spite of this, VCSEL technology can be considered a relatively mature technology. At present there are commercially available 1x4 and 1x12 VCSEL arrays with modulation rates up to 10 Gbps [10]. Additionally different experiments ([11], [12], [13], [14]) have managed to integrate large number of VCSELs (64, 256 and 540) with maximum channel packaging density of 6800 channels/cm^2. Therefore this technology is currently the best candidate for implementing FSOI systems.

Detectors

The two commonly used devices for OE conversion are PIN diodes and metal-semiconductor-metal (MSM) diodes. In both types of diodes, an electrical field in a semiconductor material drives the electrons and holes which are generated by the incident photons to the terminals. The result is a current which is proportional to the number of photons absorbed per second. They are Si compatible devices that convert any incident light into a current. They can be easily fabricated in large arrays using existing technology, offering fast response times [15].

A number of different designs have been used for optical receivers on chip. These include transimpedance amplifier [16], [17] and clocked sense-amplifiers [18]. See reference [19] for a discussion of development and results of state-of-the-art in photoreceivers technology.

Smart Pixel Array

The definition of a Smart Pixel Array (SPA) is, according to Liu et al. [20], an array consisting of optical transmitters and receivers with resident intelligence built into each element in the array. Transmitters and photodetectors can be fabricated on the same substrate which is usually different from the silicon substrate devoted to electronic processing. As a result some interfacing technique is needed to connect the optoelectronic inputs to their electronic counterparts. These techniques, which are reviewed by Desmulliez [21] and Miller [22], allow photodetectors and transmitters to be hybrid-integrated to CMOS chips after the chip is manufactured. The advantage of hybrid integration is that the material and design of the transmitter and photodetector are independent of the transistor technology. The most mature hybridisation techniques are wire bonding and flip-chip bonding. Flip-chip bonding is a manufactureable technology enabling the integration of large device arrays. The performance tradeoffs between these two techniques are evaluated in [23]. Wire bonding has greater parasitic inductance and capacitance which reduces performance at high bit-rates as compared to flip-chip bonding. Hence, flip-chip bonding is more suitable for high-performance applications requiring minimum front-end capacitance.

The integration of dense two-dimensional (2D) arrays of optical devices with standard CMOS ICs has been demonstrated, and allows a huge chip-to-chip interconnection bandwidth [11], [14], [17].

Lenses

When using FSOIs, we can, almost freely, utilise all three dimensions. Actually, the architecture can be extended to four dimensions if we consider the use of different wavelengths as an extra dimension [24]. However, due to the large far-field divergence of the transmitters it is necessary to employ lenses in order to collimate the beam and reduce loss and crosstalk [29]. The discussion is then whether it is best to use macrolenses, -lenses that cover many transmitters and receivers, or microlenses, which cover only one transmitter or receiver each. Over a shorter interconnection distance, a

microchannel configuration offers many advantages [25] [26]. In such systems each channel is relayed by a pair of microlenses. The design complexity is low and is independent of the number of channels. However, the interconnection distance is limited by diffraction. Longer interconnection distances require either cascade relays (thus increasing assembly complexity) or increasing lens apertures (which reduce channel density). An alternative to this approach is to use a single (macro) lens pair to image all of the source elements to the detectors' array allowing therefore longer interconnection distances [17] [27]. Then in order to minimise the aberrations, multiple-elements lenses are typically used [28] which increases the cost and complexity of the system. Although longer interconnect distance can be achieved with this configuration, the number of channels is limited by the field of view of the lenses. There is a third configuration known as clustered interconnect configuration [12] which is an intermediate compromise to the previous two extremes, consisting of grouping the channels within a cluster, each of which is imaged by a single lens pair. A study of the optimum design parameters that maximise the density of channels for different interconnect length can be found in reference [29].

Independent of the chosen lens configuration, another important factor is the development of low divergence, single mode, VCSELs [30] in order to achieve large interconnection densities at longer interconnection length and lower assembly complexity.

Optical Interconnect Elements

This subsection examines different optical components that can be used to create static or dynamic two-dimensional interconnect patterns in free space.

The first component considered is the diffractive optic element (DOE). In the same way that a diffraction grating divides an incident beam in one dimension, the DOE shapes a beam in two dimensions to create a desired intensity profile in the far field of a Fourier lens. These passive devices are planar elements consisting of areas which retard incident light. They can perform complex optical functions which may have previously required several optical components. DOEs are compact, can be constructed using robust materials such as silica and are simple to manufacture using existing VLSI fabrication techniques. Complex and large scale interconnection patterns can be created using a DOE, which obviously are limited by input beam intensity since every fanned-out

channel must have a large enough fraction of the input beam power to make it detectable. In reference [31] and [32], Taghizadeh et al. present the use of DOEs as free-space interconnection elements in optical computing.

The second component examined is the Spatial Light Modulator (SLM) [33], based on liquid crystal displays (LCD) technology, and which contain a large number of individually addressable voltage controlled pixels. These devices can be used to modulate amplitude by controlling the routing of a specific transmission channel. It can also be used as a phase retarder allowing an SLM to be used as a programmable DOE.
The use of SLMs tends to be limited by their relative expense, complex control logic and slow refresh rates. If used to control phase, configurations need to be stored in memory as a computation of a new configuration, requiring a large amount of processing power and therefore they are not feasible in real time. SLMs do not particularly suffer from fabrication limitations. Indeed, megapixel devices already exist [34] However, commercial SLMs are addressed in a serial manner and larger arrays require longer reconfiguration times which, consequently, reduce the refresh rate of the entire array. These disadvantages mean that SLMs rarely have frame refresh rates of greater than a few kilohertz.

Apart from these components there are a wide range of passive optical devices such as beam splitters, polarising beam splitters (PBS), mirrors, prisms, filters, quarter wave plates (QWP) and half wave plates (HWP) which have been successfully employed in multiple FSOI systems [24], [35], [36]. The most important advantages of these components are their simplicity and mature technology which offers a wide variety of characteristics and performances.

2.2.2 Simulation Tools for Modelling Free Space Optical Networks

Systems using optical interconnects belong to the mixed domain of optoelectronics. In the electrical domain, simulation tools have been used in all areas from analog circuits such as SPICE to digital tools such as VHDL. The same happens in the optics domain where powerful design tools such as CODE V and ZEMAX have been developed and are commercially available. Systems using optoelectronic devices so far have been

developed in an unplanned manner, and the performance of the system has been estimated on empirical characterisation of components [37].

During the later years, however, at least two computer-aided tools have been developed to assist optoelectronic architecture designers in their work to create high-performance systems. These two tools are Chatoyant [37], [38] developed by Levitan et al. at University of Pittsburgh and HADLOP [39], [40] developed by G. Grimm et al. at Friedrich-Schiller Universitat, Jena.

Chatoyant is a tool for simulation and analysis of heterogeneous free space optoelectronic architectures. It is capable of modelling digital and analog electronic signals and optical signal propagation with mechanical tolerancing at the system level. It is capable of presenting models for a variety of optoelectronic devices and produces results that demonstrate the system's ability to predict the effects of various component parameters, such as detector geometry, and system parameters such as alignment.

HADLOP (Hardware Description Language for Optical Processing) is a simulation system for parallel digital optoelectronic and optical architectures. It was designed in order to verify the logical behaviour of algorithms working on two-dimensional data planes. These planes are manipulated by optical or optoelectronic devices which are connected optically, for example, Smart Pixel Array and SEED-Systems [4].

2.2.3 Classification of Optical Networks

Interconnection networks can be classified as static or dynamic [4]. Static networks consist of point-to-point communication links among processors and are also referred to as direct networks. Static networks are typically used to construct message-passing computers. Dynamic networks are built using switches and communication links. Communication links are connected to one another dynamically by the switching elements to establish paths among processor and memory banks.

Additionally, optically interconnected networks can also be divided in two subgroups, passive or active [4]. A passive network does not process any data or any buffering electronically outside the processing elements. In other words, all advanced address

recognition, adding or extracting optical packets to or from streams must be performed inside the processing elements. On the other hand, an active network has intermediate active nodes that process data electronically.

In the following three subsections, three out of four possible subgroups are described. The fourth group -passive dynamic networks- is removed due to the difficulty in optically processing the data.

Active Static Networks

The active elements in the network are only allowed to do non-dynamic routing such as data manipulation and buffering. Instead of using elementary transmitters and receivers, and leaving all processing of information to the nodes, one could add some logic to the elementary components. With this kind of intelligent transmitters and receivers, high fan-in and fan-out could be utilized. In [41], Guilfoyle et al. describes the DANE optoelectronic intelligent logic cell, where the information is detected, amplified, negated and emitted (DANE).

Active Dynamic Networks

Active dynamic networks, also known as switching systems, are very common in computer networks and telecommunication systems such as asynchronous transfer mode (ATM) networks. Crossbar Switch is a common type of switch system and several architectures exploiting the properties of FSOI have been proposed [42], [32]. For example, in reference [11], A.C. Walker et al. presents the construction of an optoelectronic crossbar system that includes a 64x64 switch matrix with optical inputs and outputs permitting 1 Tb/s of internal interconnect capacity for achieving non-blocking one-to-one or unrestricted broadcast connectivity.

Passive Static Networks

The passive static group represents one of the most advantageous optically interconnected networks for parallel computers. No additional optical-electrical-optical conversion is made in the network, and all communication is made in the more favourable optical domain with help of passive optical devices such as beam splitters. Also, all computational power is uniformly distributed throughout the whole system.

FSOIs have been identified as a potentially important technology for future passive static networks and a lot of theoretical systems have been proposed using FSOI's [24], [36], [43], [44], [45]. These works propose the utilisation of different optic properties such as wavelength-division and polarisation-based beam combination for interconnecting a lot of processors using architectures such as Completely Connected or Hypercube topology.

Experimental studies have also been proposed using simple architectures, generally based on an optical system, often referred to as an optical bus that comprises several image relay stages in a linear (or ring) topology. Despite their architectural simplicity theses systems have show up many engineering problems. For example, reference [35] aims at the design of a system that interconnects four multiprocessor nodes using a high density optical ring interconnect. However, the system was not fully functional because modulators were used as optical sources which required an optical power supply (OPS) of approximately 2W which was not available at the time.

Alternatively, reference [12] makes use of the other type of source available, VCSELs. In this case, 512 VCSELs channels are used to interconnect two CMOS chips. However, the optical bus presents an efficiency of only 9%, and an optical crosstalk of -9.6dB. The main contributions to excess loss were both the leakage from the prisms used to route the signal into and out of the chip, and the beam clipping within the relay system that was necessary to collimate the high divergence of the VCSEL beams.

2.3 Optical Highway

The concept of Optical Highway (OH) was introduced in [46], [47], [48] as a FSOI system and explored in depth in the AMOS project [36], [49], [50] jointly carried out by Heriot-Watt and Leeds Universities.

2.3.1 Previous Work on the Optical Highway

The OH is a FSOI polarised beam routing system (passive static network) which provides a very high spatial and temporal bandwidth to which a large number of nodes can be connected in an arbitrary topology. Figure 2.2 schematically shows an OH in a linear configuration-a highway.

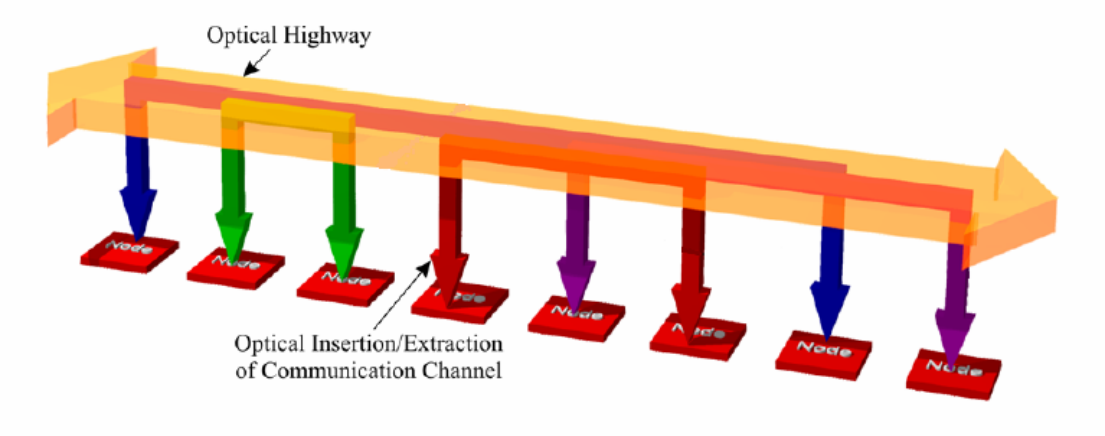

Figure 2.2. The Optical Highway. Free space optical highways interconnect multiple nodes through a series of relays that are used to add or drop several optical channels at a time.

A node consists of a processing system and a custom optoelectronic interface chip such as an SPA. The SPA gathers two different structures: the reconfigurable chip and the optical interface. The reconfigurable chip is an FPGA (Field Programmable Gate Array) which allows setting different connection patterns on identical chips. This chip designed has been part of POCA project [51], [52] also at Heriot-Watt University. The optical interface communicates the different processing units and is set by arrays of VCSELs and photodiodes which are directly flip-chip bonded on the FPGA to form altogether the SPA, also called OFPG.

OH is a passive static network where optical hardware is based on a polarising beam routing system. This system can be implemented in many different ways. Figure 2.3 and 2.4 show the first two designs proposed in AMOS. In Figure 2.3, two polarising beam splitters (PBS) are used to deflect optical channels of a specific polarisation to a node with each channel's polarisation state determined by patterned half wave plates (HWP). In Figure 2.4 a single PBS is used and a QWP (quarter wave plate) is used to route the optical signal in different directions.

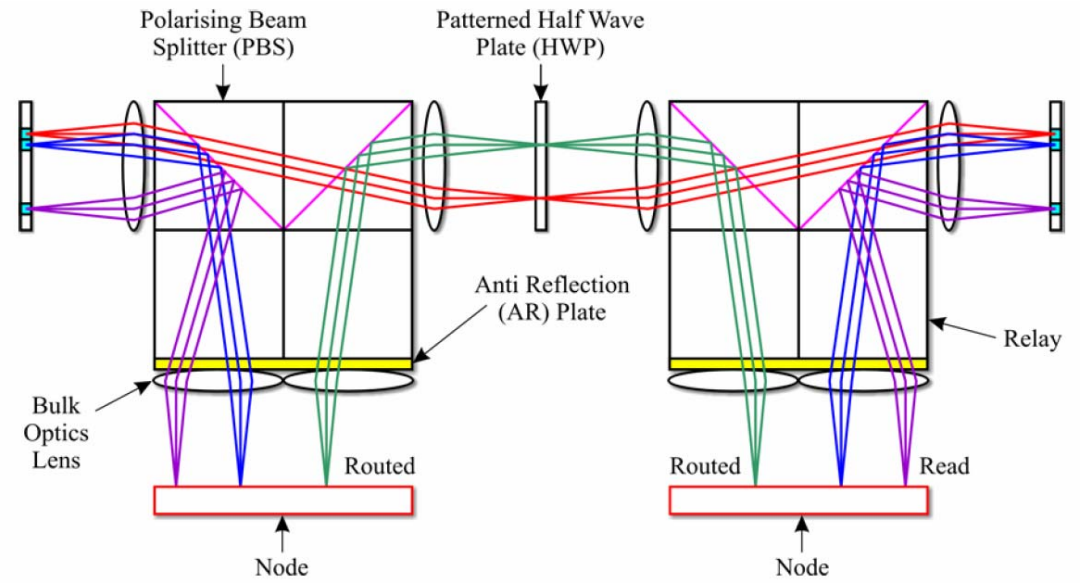

Figure 2.3. A dual PBS optical highway construction where the polarising optics define a fixed network topology.

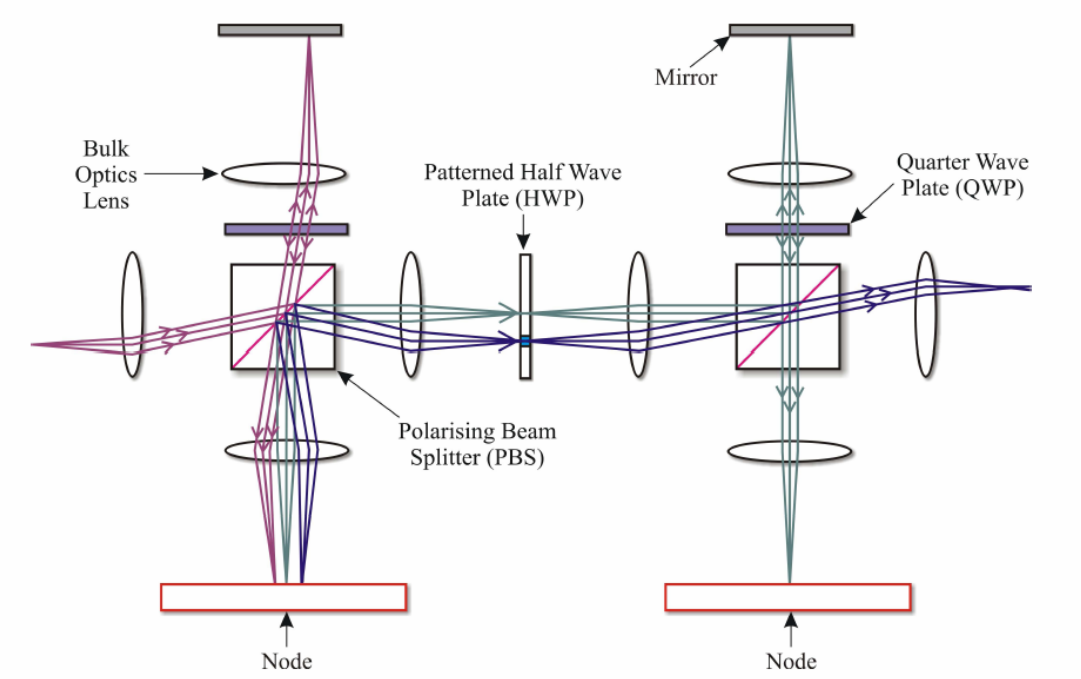

Figure 2.4. A single PBS optical highway construction using QWP for routing the signal in different directions.

The AMOS project also proposed the use of Liquid Crystals (LCs) as phase retarder SLM instead of the patterned HWP in order to make the OH a reconfigurable static passive network. The idea of a reconfigurable passive static network introduces an advantage over general passive static networks since, in this case, multiple interconnect topologies can be implemented.

LCs are slow for packet switching but can be used to reconfigure topology for fault tolerance and algorithm reasons.

In order to maintain efficiency, run-time reconfiguration cannot be performed since it requires a reconfiguration controller with associated hardware reconfiguration delays. Compile time reconfiguration is desirable but not necessarily a requirement. Regardless of when reconfiguration occurs, most algorithms will need to be adjusted for computation on a multiprocessor system. It would therefore be simpler to fit the algorithm to a fixed topology OH. Thus, complex reconfiguration control hardware can be eliminated, including potential run time issues such as determination of the entire OH's current state.

Based on the AMOS project, a group of different experiments have been carried to further develop of the concept of the OH. In [54], G. Russell proposes a set of parameters necessary to define the optoelectronic interface of the OH. He also analyses the optical limitations of the OH in terms of aberration and makes a first estimation of attenuation and maximum number of stages that the optical signal can pass through the system before it becomes too weak.

In [53], Tissot presents the design and mapping of receivers and VCSEL arrays for the OH. Properties such as redundancy and efficiency are analysed. He also proposes the implementation of two topologies (Completely Connected and Hypercube) and carries out a first simple experiment as a proof of work of the OH based on LC.

Finally, C. Moir in [55] proposes the implementation of a concrete algorithm, matrix multiplication, using a particular architecture of the OH.

2.3.2 Improvements and Limitations of the Optical Highway

As shown in the previous section the concept of OH has been deeply analysed. This section examines the area, both experimental and theoretical, that require further analysis.

The first chapter indicated that one of the major problems for impeding the widespread acceptance of the FSOI system in general was relative to the cost and manufacturability of optics and optomechanics used in such systems [56], [57]. This thesis will explore the use of a low cost and fast technique known Rapid Prototyping for implementing different architectures of the OH and carrying out experiments.

Another problem to be tackled in this thesis is the study of polarisation losses on the OH since there is little literature available on polarisation losses in FSOI [57]. The OH is a polarization beam routing system. Therefore, it is important to analyse the influence of these losses on the different components that gather the OH. Special attention will be given to the optical reconfigurable switching and the liquid crystal, since little study on this component has been carried out in this environment.

The analysis of polarisation losses will help us to understand the influence of these losses on the estimation of the maximum number of stages the signal will be available to pass through the OH before it becomes too weak.

One important choice in the implementation of an optical interconnect is the manner in which each logical network link is supported. One approach is to form such links from multiple hops between physically adjacent nodes. This has the advantage of simplifying the optical system design and assembly [35]. The disadvantage is that the entire bandwidth of the bus passes through the optoelectronic interface at each node. An alternative approach is to use a single hop to form each long-distance link with the signal remaining in the optical domain throughout. Since a high-performance free space optical system can carry more parallel signals than the optoelectronic interface, this method has the potential to fully exploit the capacity of the optical system. However, as the signal beams travel further through the optics, beam quality degenerates and aberration occurs. Thus the channel bit rate must be lowered. In reference [58], these two approaches for implementing FSOI networks were compared and it was found that the single-hop approach could provide a higher bandwidth per link. However, this higher bandwidth varies depending on the type of networks and number of nodes connected. For the single-hop approach, the maximum number of nodes connected depends on the physical architecture of the network and the maximum number of stages that the optical signal can pass through in the network.

In order to minimise the optical losses and increase the efficiency of the architecture, this chapter proposes a basic design of the OH shown in Figure 2.5, where a reduced number of different optical components are used (PBSs and LCs) which significantly simplify the design. The design of the proposed optical stage will be used in this thesis and supposes a more efficient design in terms of losses and connectivity than the designs proposed originally in the AMOS project (Figure 2.3 and Figure 2.4).

The basic operation is that a linear polarised signal from a node will be routed to a Twisted Nematic LC, which can either rotate the polarised light by 90°, if switched Off, or leave the light unchanged if switched On. The signal then travels towards a PBS, which can route the signal in two different directions (transmission or reflection) depending on how the LC has set the linear polarisation of the signal. This structure, the LC/PBS assembly, constitutes what we call an optical stage of the OH, and in Figure 2.5 two of these stages are represented.

The OH utilises multiple imaging stages constituting a flexible architecture on to which multiple interconnect topologies can be dynamically implemented. Note that although a signal may pass through multiple optical stages to travel from the source to destination nodes, these optical stages are passive components and do not involve any optoelectronic conversion of the signal. Therefore, the latency associated with routing can be reduced to the minimum - conversion from electrical to optical in source node and optical to electrical in the destination node.

Figure 2.5 also shows some unique properties of FSOI systems. For example, due to the non-interaction of light, the optical signal that communicates node 2 with node 4 can cross the optical signal that communicates node 2 with node 5. Another characteristic is that the same channel (PBS point) can be used for routing different signals at the same time. In Figure 2.5 we can see how node 1 and node 5 can communicate at the same time as node 2 and node 3 using the same PBS point. These properties are important in order to increase the efficiency of an optical channel in terms of the number of different optical signals from different nodes that can use the same, or at least part of the same, optical channel. These properties and others, together with some of their main limitations such as crosstalk, will also be analysed in the following chapters.

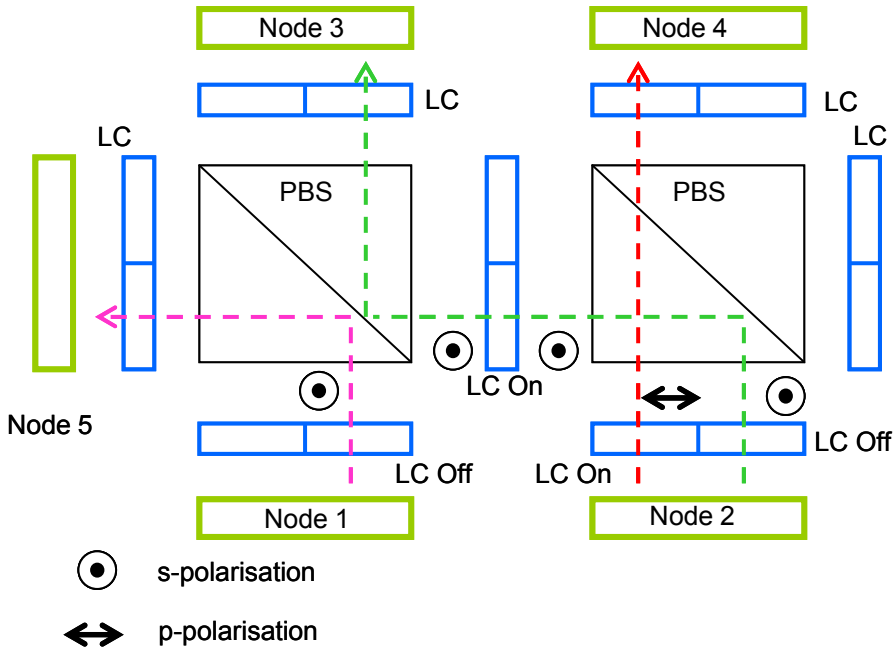

Figure 2.5. Example of an implementation of two optical stages of the OH. When LC is Off, the linear polarisation is twisted. In On state, the LC keeps the same initial polarisation.

2.4 Conclusion

This chapter has overviewed FSOI networks and the current state-of-the-art in technology, integration, simulation tools and classification of such networks has been analysed. Additionally, a particular FSOI network was introduced, known as the Optical Highway, which will undergo further analysis in this thesis.

This chapter concludes by proposing a basic design of an optical stage of the OH, which increases the efficiency of optical stage, allowing the signal to be route in one extra direction. The design increases also the efficiency optical channel by using the same channel to route more than one the signal. Therefore, this design makes more feasible the use of FSOI for parallel computing applications.

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Chapter 3
Experimental Validation of the Optical Highway using Rapid Prototyping Technique

3.1 Introduction

In this chapter the concept of the optical stage of the OH based on the LC/PBS assembly is tested experimentally.

The first section analyses the optical components, such as wire grid plates and 'off-the-shelf' LCs, which will be specially optimised for new roles within the OH.
The second section of the chapter analyses the feasibility of a novel, low cost and fast technique known as Rapid Prototyping (RP) for implementing the optomechanical structures of the OH.

In the last section, a model is proposed in order to estimate the maximum number of stages that an optical signal can pass through within the OH. This model is validated experimentally using the optomechanical structure designed in the previous section.

3.2 Optical Components used for Implementing an Optical Highway Demonstrator

This section will present a set of off-the-shelf optical components used for building the first demonstrator designed to analyse different properties of the OH, focusing especially on reconfigurability properties.

Some limitations are taken into account at this point. Firstly, only one optical channel of the OH is going to be simulated at this time. Therefore, we eliminate the possible contribution of crosstalk from other channels and simplify the alignment of the system.
Secondly, in order to simplify the system, only an analysis in Continuous Wave mode (CW) will be carried out for the study of the reconfiguration properties of the optical channel.

These simplifications allow us to employ off-the-shelf optical components such as simple 630 nm, CW diode lasers, low cost Wired Grid Plates (WGP) used as broadband Polarising Beam Splitter (PBS) and off-the-shelf LC.

3.2.1 Description and Characterisation of Wire Grid Polarising Beam Splitter Plates

There are different varieties of polarising beam splitters. However, only two are viable alternatives for use with FSOIs. The PBS cube, or MacNeille PBS, is the most common variety and is based upon achieving Brewster's angle behavior at the thin film interface along the diagonal of the high refractive index cube in which it is constructed. This device is currently the most favoured since its performance is marginally acceptable. However, it does carry a significant cost in both weight and price.

The WGP are simple one-dimensional, dielectric or metallic grating (Figure 3.1). They have been in use for some time in the microwave region where the longer wavelengths make its construction easier. However, the first commercially available device for the visible spectrum based on the technology of nanometer-scale wire-grids has only recently been released by Moxtek [1].

The function of the wire grid is to allow the wave incident on the parallel conductors with polarization, perpendicular to the length of the conductors to pass through the structure. This occurs because the electric field of the wave can generate no significant current in the conductors in this direction. The polarisation parallel to the conductors, however, generates a current in the conductors and imparts energy to them due to their inherent resistance.

The accelerating electrons in the conductors radiate in both the forward and rearward directions. The forward radiation cancels the wave moving in the forward direction, and the rearward radiation appears to be a reflected wave [2]. In other words, for one polarisation the wire grid acts as a lossless metal, while for the other polarisation, it acts as a dielectric.

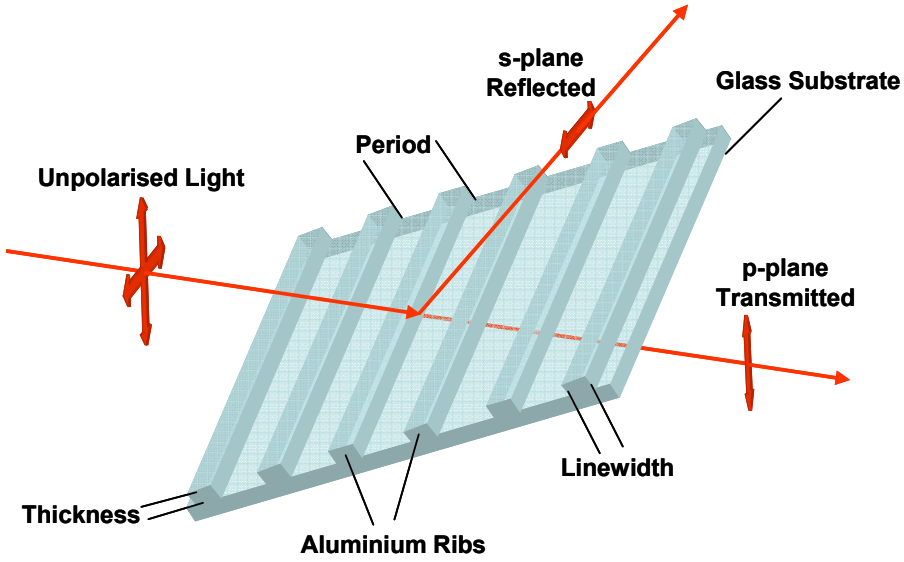

Figure 3.1. Wire Grid Plate. The grating period must be smaller than the wavelength of the source used in order to work as a PBS. The thickness and linewidth of the grating are free parameters used for optimising the extinction ratio and the diffraction efficiencies of the p and s polarisations.

WGP performance is a trade-off between competing concerns. For example, the best transmission performance requires consideration of thin plate behavior as well as polariser behavior. These two constraints may not be compatible with achieving the optimum contrast at the same time. In general, WGPs have transmission performance ranging from approximately 85% to 92%, whilst the contrast ratio will range from 100:1 to over 1000:1. The highest contrast requires a trade-off in transmission and vice versa.

WGPs offer advantages in projection display architectures over traditional cube PBS, such as less sensitivity to angular aperture, high system contrast and simplified designs when implemented in the appropriate architecture. They constitute a technology critical to the continued progress of LC projection technology [3].

The use of WGP for FSOI systems was suggested in reference [4]. However, this chapter will, for the first time, fully analyse and experiment with this component. WGPs are attractive due to their one-dimensional nature because they can solve problems of compactness inherent to the use of PBS cubes. The one-dimensional nature of the WGP also permits more architectural flexibility to route the signal, allowing the beam to pass not just through the plate but also parallel to it without being attenuated or modified as shown in Figure 3.2.

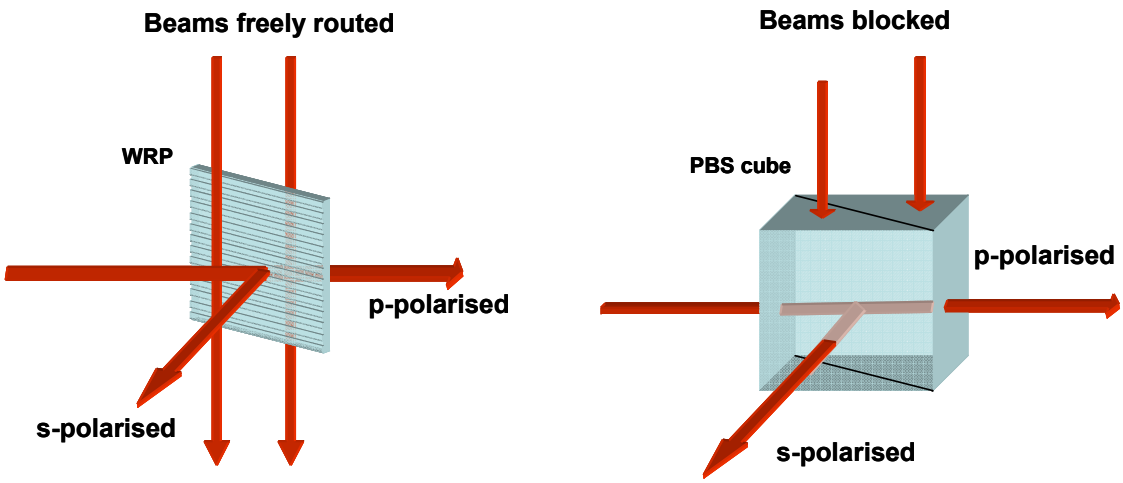

Figure 3.2. WGP vs PBS cube.

WGPs are also adapted to mass production since their manufacture is based on lithography technology. Therefore, the cost associated with this component is considerably lower than for PBS cubes.

Another important advantage of WGPs is that they can offer a better thermal management solution than PBS cubes, allowing more airflow through the system. Thus, temperature sensitive components such as VCSELs can be easily controlled.

Finally, the fact that the WGP has a relatively low sensitivity to angular aperture compared with PBS cubes can also offer an important benefit for FSOI systems, since WGPs do not suffer from polarisation losses under tilt and rotational misalignment where typical PBS cubes do.

A custom-made WGP (30 mm x 18 mm) has been specially designed by Moxtek for testing within the OH. In order to obtain the best transmission and contrast, the beamsplitter has been used to transmit the p-polarisation. It is possible to use the beam splitter in the orthogonal orientation (transmission of the s-polarisation), but with reduced efficiency and contrast.

3.2.2 Liquid Crystal

In this section an off-the-shelf LC is fully characterised and optimised in combination with the WGP in order to achieve good switching performance of an optical stage of the OH.

Figure 3.3 shows the diagram of the conventional operation of a 90° twisted nematic structure, TNLC, working as a light valve, which consists of a thin film of a nematic LC contained between parallel glass plates and sandwiched between two crossed polarisers. The surfaces of these plates are treated so that the time-averaged molecular axis or director in the film is parallel to these surfaces but undergo a 90° rotation through the film thickness. The material used in these devices is birefringent and has positive dielectric constant anisotropy.

An important optical property of this structure is that it will rotate the plane of polarisation of light transmitted through the film. If polarised light is incident on the film in such a way that the plane of polarisation is parallel (or perpendicular) to the director at the entrance surface, then the plane of polarisation is rotated 90° as the light traverses the film.

If an electric field is applied across the film, by means of transparent electrodes on the inner surfaces of the glass plates, the molecules realign parallel to the field to form the homeotropic state which has no optical activity. Therefore, to make a practical device, the twisted structure is placed between parallel or crossed polarisers as shown in Figure 3.3 where the structure gives transmittance and can be switched to an extinction state when applying a voltage. A more detailed analysis on the LC operation will be analysed in the next chapter.

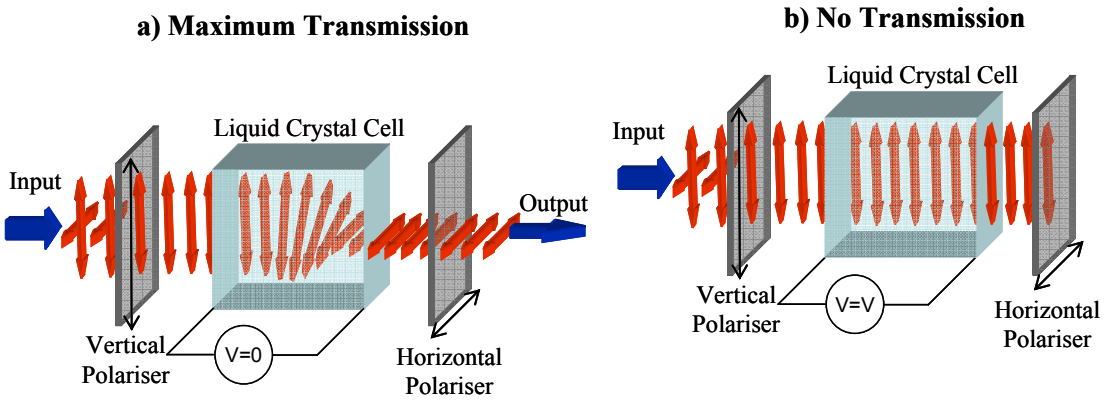

Figure 3.3. Operation of an LC. Input light follows the director of the LC. When voltage is applied the light passes through with no twist and when the voltage is not applied, the polarisation light is twisted through 90°. In practise, LCs can be manufactured with various degrees of twist.

The LC employed in this chapter has been obtained for a fraction of the price of a custom made LC plate from commercially available, mass-produced, stereostropic viewing glasses developed for the PC gaming industry [5]. These glasses consist of two TNLC plates sandwiched between crossed polarisers. In order to obtain the LC the cross-polarisers have to be removed from the glasses, which proved to be easy to dismantle.

Preliminary characterisation of this LC [6] shows that they need to be powered at least at 6V in order to perform the twisting of polarisation.

Error! Reference source not found. shows the setup of the experiment carried out in order to analyse the switching behaviour of the LC-WGP assembly. In this experiment an s-polarised beam is launched into the LC that can be oriented at any rotational position. The LC is placed behind the WGP which will transmit the p-polarised component and reflect the s-polarised component for different rotational positions of the LC.

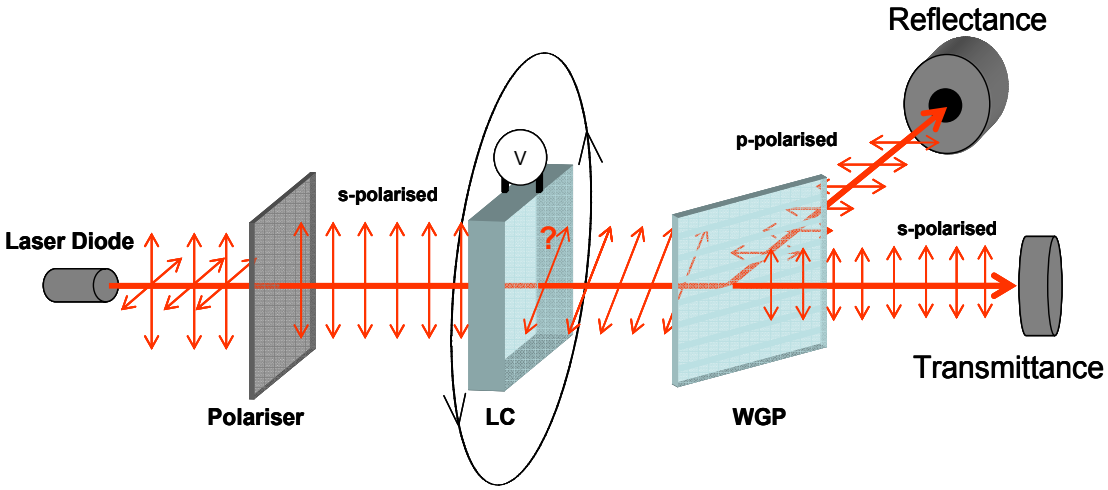

Figure 3.4. Set up experiment for analysing switching properties of LC-WGP assembly.

Figure 3.5 presents the values of transmittance and reflectance at different rotational positions of LC when it is in Off and On states. It must be pointed out that in order to achieve an optimum switching performance of the LC the transmittance and reflectance values must differ as much as possible for each state, On or Off, of the LC. When the LC is On, it becomes not birefringent and, therefore, no change of phase is produced and the input s-polarised beam remains unaltered. This allows the WGP to reflect most of the light, keeping the transmittance low for any rotational position of the LC. On the other hand, when the LC is Off, the value of the transmittance-reflectance difference is low and variable with the orientation of the LC. In this case, the maximum difference is achieved when the LC is rotated between 45° and 50° with respect to its original position. However, the result is still significantly worse than when the LC is On. The reason for this is because the molecular twist angle of the TNLC is different from 90°.

The twisting angle varies from 45° to 70° depending on the orientation of the input polarised beam in regard to the director of the LC.

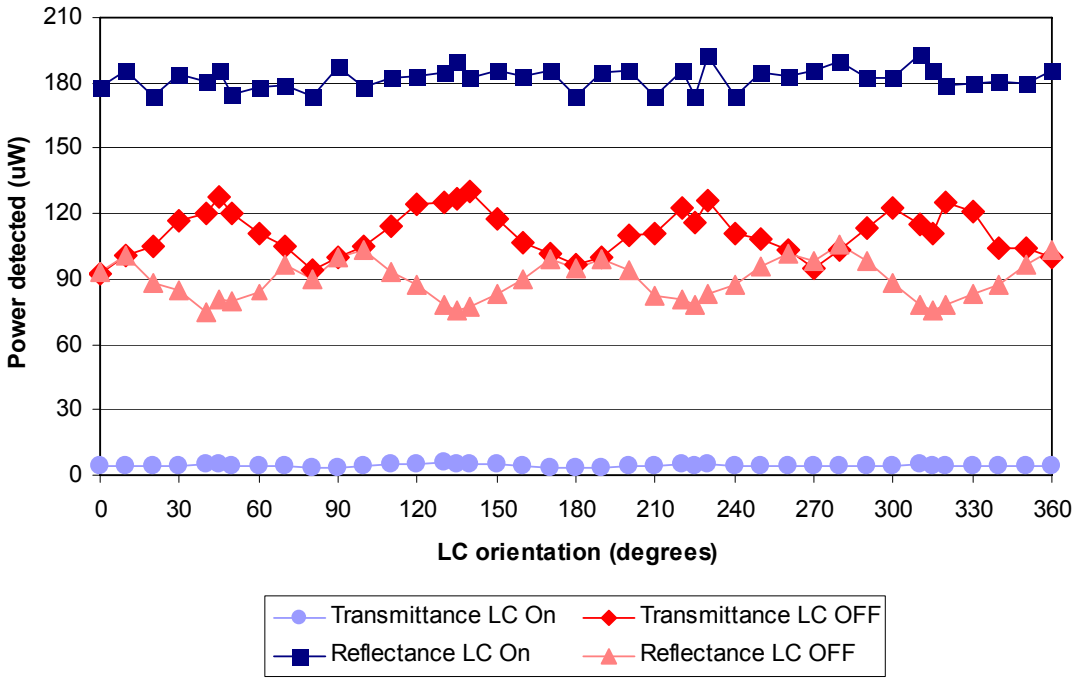

Figure 3.5. Transmittance and Reflectance obtained after s-polarised light goes through the assemble LC-WGP.

In order to obtain a 90° twisting angle of the input s-polarised beam, a second LC must be used and properly oriented with respect to the first LC as shown in Figure 3.4. In this case the first LC (LC1) is fixed in position and the second LC (LC2) is rotated.

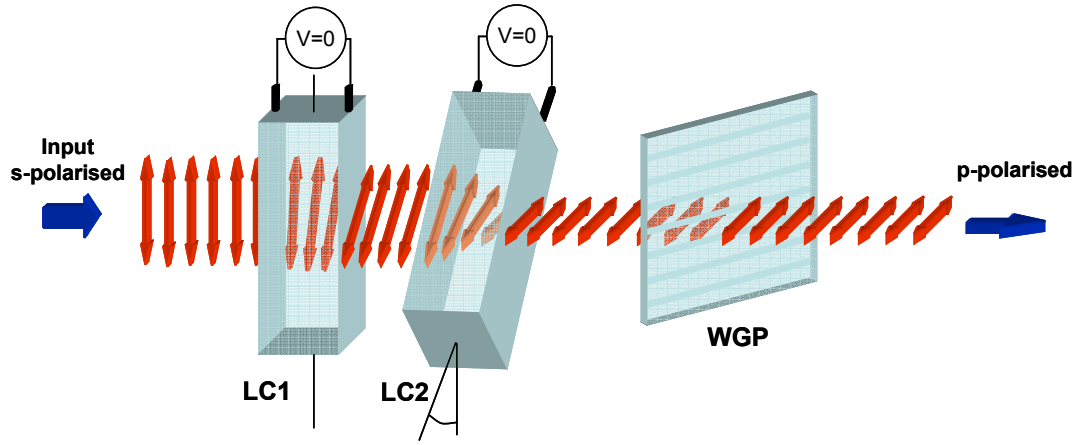

Figure 3.4. Configuration of two LCs (LC1, LC2) in order to achieve 90° twisting angles of the polarisation in Off state.

Figure 3.5 shows the values of transmittance and reflectance at the outputs of the WGP when two LCs are employed. It can be observed that in Off state there are two windows for the position of the LC2, 90°-140° and 260°-330° where the input s-polarised beam is

mostly converted into a p-polarised beam and then transmitted by the WGP, resulting in a high value of transmittance and low value of reflectance. Therefore, these windows are suitable for using the LC-WGP assembly as an optical stage of the OH, where the signal can be efficiently reconfigured from transmission into reflection and vice verse.

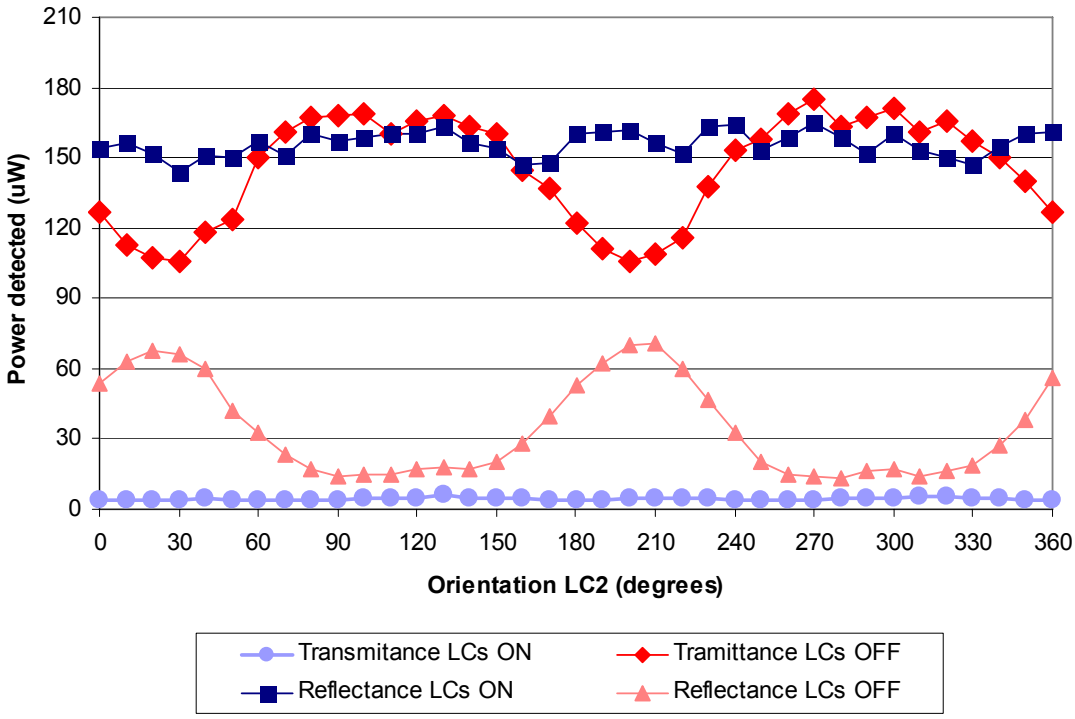

Figure 3.5. Values of Transmittance and Reflectance for different orientation of LC2 with respect to LC1.

3.3 Rapid Prototyping

The cost of implementing a new optical design using traditional laboratory equipment is high and any mistake in the initial design or specification of such equipment makes the process even more costly.

Rapid Prototyping (RP), also known as solid freedom fabrication or layered manufacturing, combines various methods, materials and technologies to fabricate three dimensional objects directly from a Computer-Aided-Design (CAD) data source, eliminating the need for tooling [7].

This has advantages over traditional methods of fabricating physical objects in that objects can be formed with any geometric or intricacy without the need for elaborate

machine set-up or final assembly. This is also achievable in a relatively fast and cheap process.

RP was introduced in the 1980s as a tool that allowed the designers to improve their product and shorten the time it took to bring new products to market. However, today the introduction of new materials and lower-cost systems are pushing these same processes out of the design lab and into the manufacturing world where they are being used to create custom parts that are production quality and not just prototype quality.
Most rapid-prototyping processes are additive, building parts one layer at a time from a powder or liquid that is bonded, meted, or fused together, often with the aid of a laser. Current laser-based prototyping methods include stereolithography (SLA), selective laser sintering (SLS), and direct metal deposition (DMD) [7].

This chapter will propose the use of RP as a fast and low cost technique for experimentally testing the LCs-WGP assembly presented in Section 2. It is believed this technique can be a solution to the current problems of cost and manufacturability relative to the optomechanic implementation of FSOI systems.

RP can be used for the first steps of the optomechanic design where many modifications of the initial design are required. Moreover, RP allows integrating the associated electronics much more closely with the optical components creating more compact optomechanic structures. The resulting system will be self-contained where with off-the-shelf optical stages, this was not possible.

The Digital Tools Manufacturing Group (DTMG) at Heriot-Watt University recently acquired a 3D printer machine, the ZPrinter 310 Plus from Z Corporation [8], Figure 3.6, which has been used to explore the capabilities of this technique. It works in a way analogous to 3D printing. Each layer of an object is written much like a laser printer. The object is moved down, a new layer of powder is created and laser-written, and this process is continued until all the layers are written.

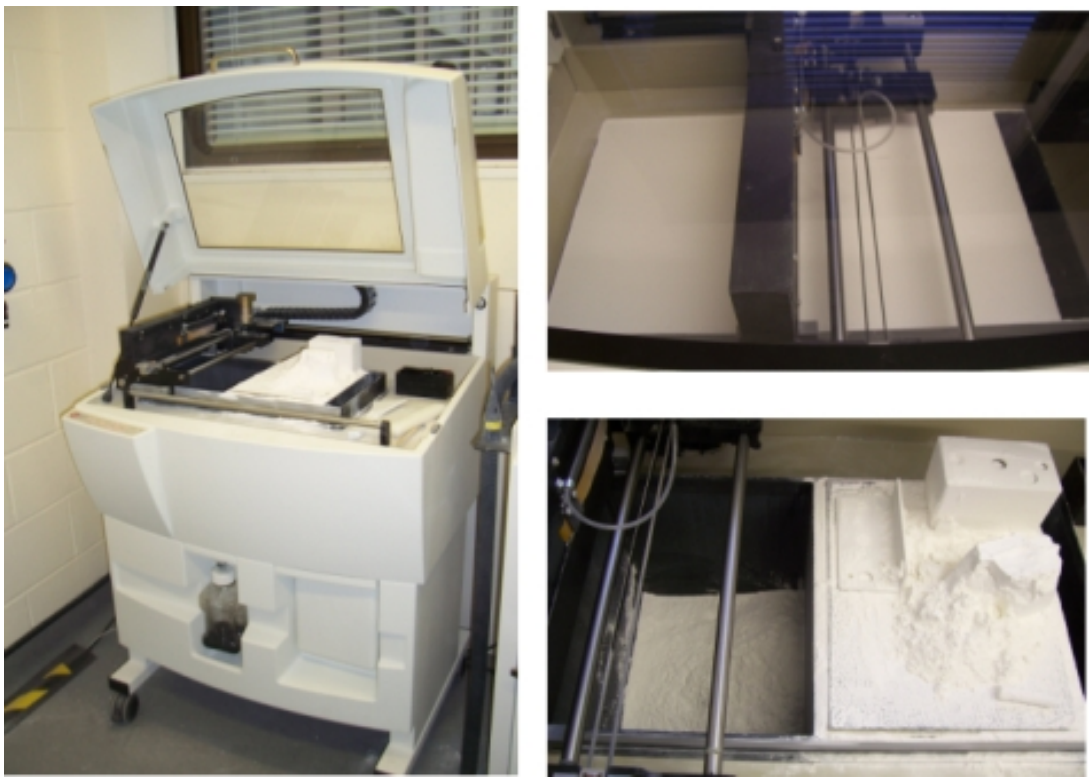

Figure 3.6. ZPrinter 310 Plus from Z Corporation at Heriot-Watt University.

Using the CAD software tool known as Solid Edge, three different frames were designed to hold the optical parts: the PBS plate; the LCs; and the laser diode module, Figure 3.9.

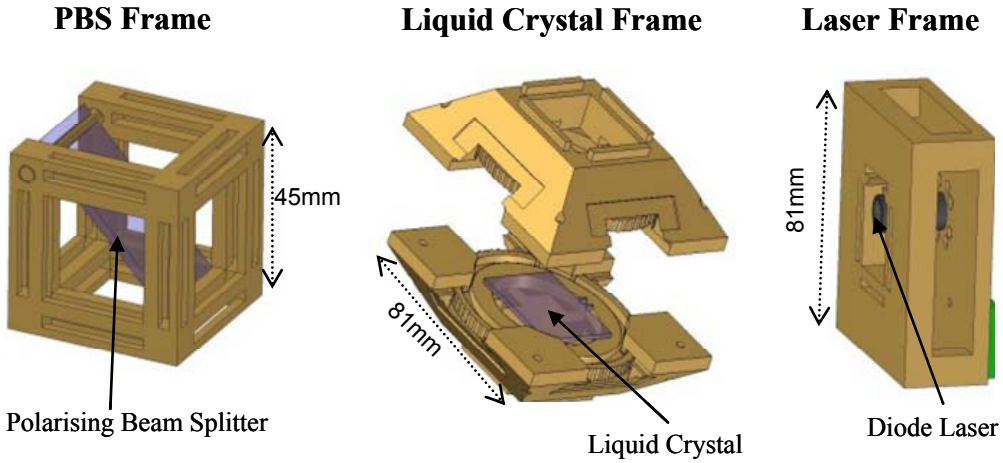

Figure 3.9. Three Designs using SolidEdge showing different frames necessary for implementing the stages of the OH.

The printer took 1-2 hours to complete the design depending on the complexity and quantity of the parts. Figure 3.10 shows the PBS frame with the PBS plate placed on it. The PBS frame has been designed to allow the signal to pass through all six faces of the

cube. In addition, the frame has been provided with a movable part to allow the PBS to be oriented at different degree. Although the usual position of the PBS plate is 0° and 45° with respect to the input signal, the moveable part also allows the active alignment of the system for fault tolerance.

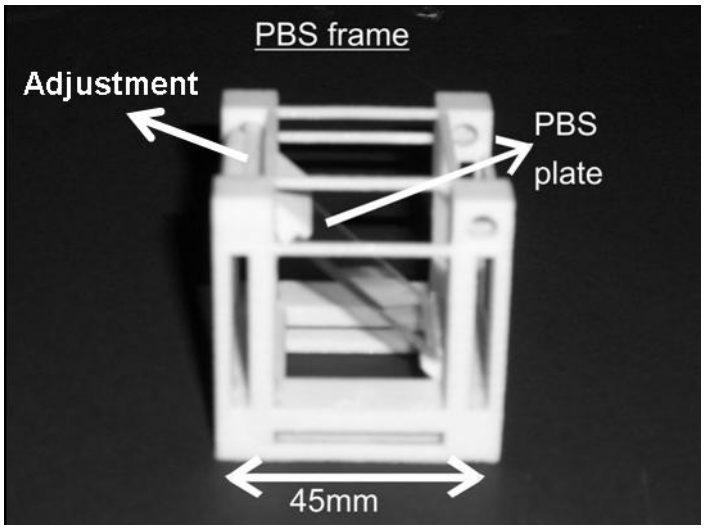

Figure 3.10. Implementation of the WGP onto its rapid prototyping frame.

Figure 3.7 shows the liquid crystal frames and the two LCs used. It has also been fabricated with a moveable part to allow the LC to rotate in order to place it in the correct position from where they can twist the polarisation angle of the light exactly at 90°.

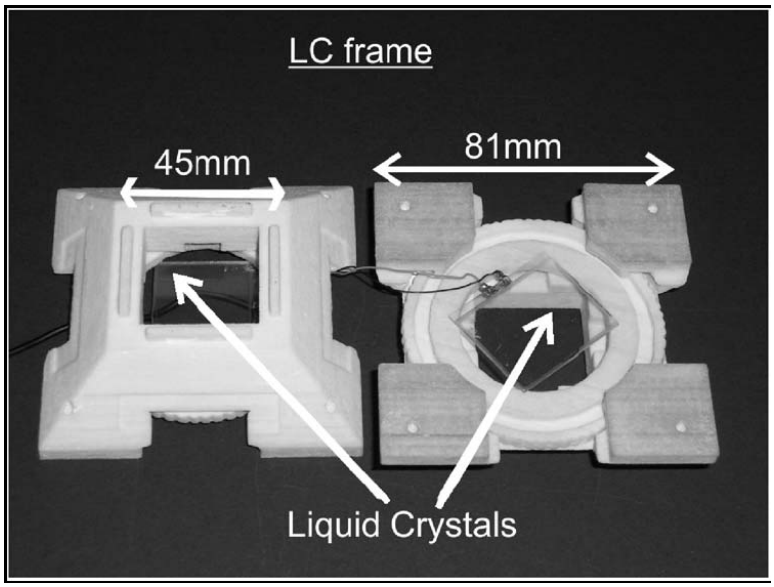

Figure 3.7. Implementation of the LCs onto its rapid prototyping moveable frame.

Finally, Figure 3.8 shows the laser frame which contains the laser module and its driver controller.

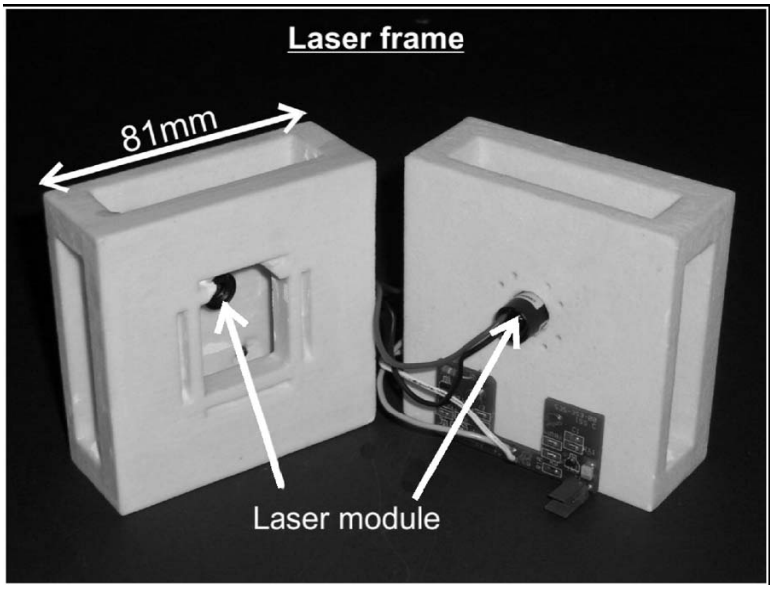

Figure 3.8. Implementation of the laser diode module and its driver controller onto the rapid prototyping frame.

As we can see, each frame has been used to test different capabilities of the 3D printer machine. All the frames were created using a cost effective powder which allows an accuracy of 1mm. However, once the final design is decided, a metalised powder can be used which has an accuracy of 100 μm. It has been estimated that the rotational tolerance is 5°. Although this tolerance is bigger than that of traditional techniques, it is good enough to study the properties of the topologies such as attenuation per stage, polarisation losses, crosstalk and maximum number of stages that the signal can pass through. These properties will be studied in the next section. However, the most important advantage of using RP is the amount of time that can be saved during the design process where multiple corrections have to be made before a definitive design. The design of laser frame required two iterations while the LC frame and PBS frame required both three iterations due to problems producing the moveable parts. All these iterations were made in less than five days.

This section proposes a design where the system is made up of different blocks or cells. Each cell routes the incoming signal in two different directions. As they work like 'lego' pieces they can be reconfigured in many ways to create different architectures as shown in Figure 3.13.

Apart from this design there are two other generations of RP structures used for implemented the OH. The second generation presented in chapter 4 supposes a

reduction in size and complexity compared with the first design presented in this chapter. The last generation is presented in chapter 6 and is used for implemented a particular architecture which implies the used of a large quantity of structures.

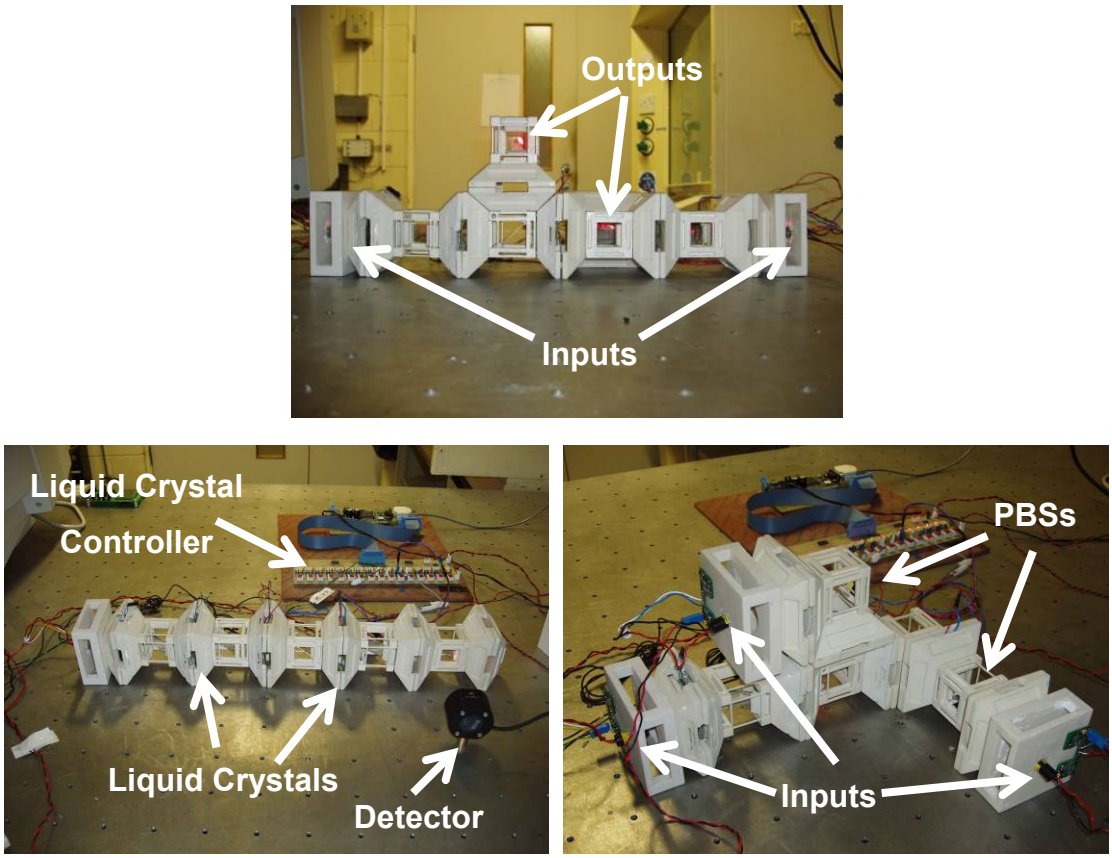

Figure 3.9. Pictures of different assembled of the same RP cells that shows the flexibility of the final cell design.

3.4 Crosstalk-Attenuation Model

The optomechanic system designed in the previous section has been used experimentally to demonstrate the equation that establishes a first estimation of the maximum number of stages the optical signal can go through. The determination of this maximum enables us to define important characteristics of the different topologies that can be implemented using the OH such as scalability and latency.

The maximum number of stages is obtained by the worst case scenario. This is where the attenuated signal between the two farthest points on the network arrives at the

detector at the same time as the misdirected signal coming from the nearest source (maximum crosstalk). In this first estimation, we assume that a medium spatial density of optical channels is employed in the OH. This implies that there are enough channels to ensure that in the worst case scenario only very few signals use the same optical channel. These assumption will be analysed in chapter 5.

A medium spatial density also ensures that there is no contribution to crosstalk from other optical channels since there is enough distance between them.

Figure 3.10 shows the experimental setup carried out where the source and detector 1 are placed at a distance of one optical stage. In this case, a misdirected signal is reflected directly by the PBS into detector 1 when any other port is selected by the LCs as output.

The objective of this section is to find out how crosstalk and attenuation can be reduced to maximize the number of stages, N. We proposed a model based on the matrix approach [9] that enables exploring the polarization nature of the crosstalk and attenuated signal.

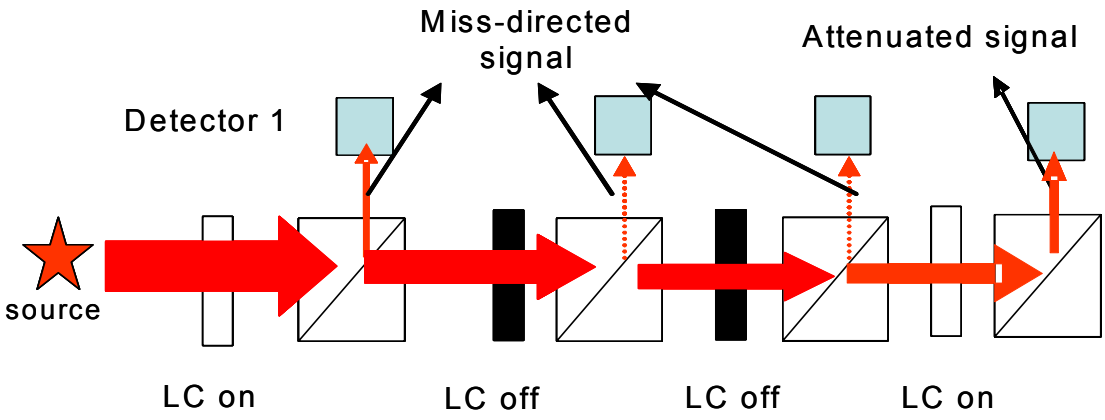

Figure 3.10. Experimental setup. Polarized light enters the system travels through up to N assemble LC-PBS stages before being output.

In order to apply this model in this particular case, a set of 2x2 matrices describing the crosstalk between vertical polarised and horizontal polarised light for each optical element and their correspondent attenuation is defined. In this model we consider four sources of crosstalk: crosstalk at each state of the liquid crystal polarisation rotators, ε_0 (LC On) and ε_1 (LC Off), and crosstalk in the reflected path ε_r and transmitted path ε_t of the polarising beam splitter.

The model also considers two sources of attenuation: attenuation caused by the LC, α, and attenuation caused by the WGP, β.

The LC can be described as a polarisation rotator by a pair of matrices: P_0, which denotes the LC when it does not rotate the polarisation of the incident light in the On state; and the matrix P_1, denoting the LC when it rotates the polarisation of the incident light in the Off state:

$$P_0 = \begin{bmatrix} \alpha & \varepsilon_0 \\ \varepsilon_0 & \alpha \end{bmatrix}, \quad P_1 = \begin{bmatrix} \varepsilon_1 & \alpha \\ \alpha & \varepsilon_1 \end{bmatrix}.$$

Note that no information concerning the relative phase of the two polarisations is included in these matrices. This information is not needed because in this switch each LC polarisation rotator is followed by a polarising beam splitter that spatially separates the polarisations. As we said before, ε0 and ε1 characterise the crosstalk of the LC so that the lower these values are the better the LC. On the other hand, α represents the attenuation of the LC and ideally has to be as low as possible.

The WGP, working as polarising beam splitters, can also be described by a pair of matrices: T, which describes the transmitted beams, and R, which describes the reflected beams:

$$T = \begin{bmatrix} \beta & 0 \\ 0 & \varepsilon_t \end{bmatrix}, \qquad R = \begin{bmatrix} \varepsilon_r & 0 \\ 0 & \beta \end{bmatrix}.$$

Where $\varepsilon_r = \frac{R_p}{R_s} << 1$ is the reflection extinction ratio, $\varepsilon_t = \frac{T_s}{T_p}$ is the transmission extinction ratio and β ~ 1 is the average loss through the PBS.

To complete the first stage of the matrix model an additional matrix is needed which represents the vertical polarisation of the input light I_v.

$$I_v = \begin{bmatrix} 0 \\ 1 \end{bmatrix}.$$

Figure 3.11 shows the different parameters associated with each optical component used in the experiment: This is to measure the attenuation and the crosstalk when the optical signal passes through many stages and therefore allows the evaluation of the matrix model.

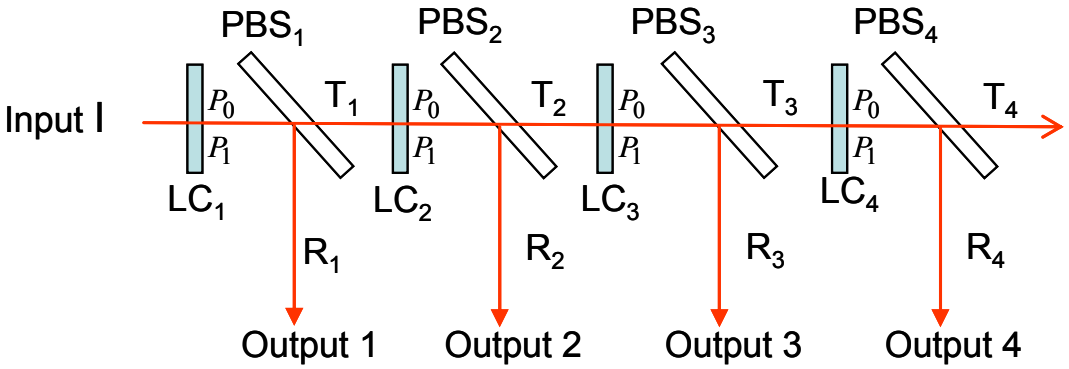

Figure 3.11. Matrices associated with each optical component.

This general architecture routes the input signal to any of the four outputs by switching the appropriate LCs. Table 3.1 shows the states of the LCs in order to route the input s-polarised signal to the different outputs.

Input I=[0 1]	Output 1 Selected	Output 1 Selected	Output 1 Selected	Output 1 Selected
LC1	ON	OFF	OFF	OFF
LC2	ON	OFF	ON	ON
LC3	ON	OFF	OFF	ON
LC4	ON	OFF	OFF	OFF

Table 3.1. Configuration of the LCs for enabling the different outputs.

This model provides us with five matrices that are used to calculate the power detected at all the ports for any output. The results are given in Table 3.2 where the diagonal elements are the insertion loss for each output port, and the off- diagonal elements are measurements of crosstalk. For example, if Output 3 is selected, the power detected at this output is $\mathbf{R}P_1\mathbf{T}P_0\mathbf{T}\ P_1I = [0, 3\alpha\beta]$, which is the expected insertion loss when the optical signal goes through three stages. The other three powers obtained correspond with the crosstalk expected at Outputs 1, 2 and 4.

Input I=[0 1]	Output 1 Selected	Output 2 Selected	Output 3 Selected	Output 4 Selected
Output 1	$\mathbf{R}\,P_0\,\mathbf{I}$	$\mathrm{R}\,P_1\,\mathrm{I}$	$\mathrm{R}\,P_1\,\mathrm{I}$	$\mathrm{R}\,P_1\,\mathrm{I}$
Output 2	$\mathrm{R}\,P_0\,\mathrm{T}\,P_0\,\mathrm{I}$	$\mathbf{R}\,P_1\,\mathbf{T}\,P_1\,\mathbf{I}$	$\mathrm{R}\,P_0\,\mathrm{T}\,P_1\,\mathrm{I}$	$\mathrm{R}\,P_0\,\mathrm{T}\,P_1\,\mathrm{I}$
Output 3	$\mathrm{R}\,P_0\,\mathrm{T}\,P_0\,\mathrm{T}\,P_0\,\mathrm{I}$	$\mathrm{R}\,P_1\,\mathrm{T}\,P_1\,\mathrm{T}\,P_1\,\mathrm{I}$	$\mathbf{R}\,P_1\,\mathbf{T}\,P_0\,\mathbf{T}\,P_1\,\mathbf{I}$	$\mathrm{R}\,P_0\,\mathrm{T}\,P_0\,\mathrm{T}\,P_1\,\mathrm{I}$
Output 4	$\mathrm{R}\,P_0\,\mathrm{T}\,P_0\,\mathrm{T}\,P_0\,\mathrm{T}\,P_0\,\mathrm{I}$	$\mathrm{R}\,P_1\,\mathrm{T}\,P_1\,\mathrm{T}\,P_1\,\mathrm{T}\,P_1\,\mathrm{I}$	$\mathrm{R}\,P_1\,\mathrm{T}\,P_1\,\mathrm{T}\,P_0\,\mathrm{T}\,P_1\,\mathrm{I}$	$\mathbf{R}\,P_1\,\mathbf{T}\,P_0\,\mathbf{T}\,P_0\,\mathbf{T}\,P_1$

Table 3.2. Matrix approach model applied at each output for each configuration.

The accuracy of this theoretical analysis can be determined by comparing it with experimental results. The six parameters necessary to characterise the LCs and the PBSs used for this experiment are listed in Table 3.3.

	Crosstalk		Attenuation
Liquid Crystal	ε_0 (LC On) = 0.025= -16dB	ε_1 (LC Off) = 0.020= -17dB	α = 0.75= -1.2dB
PBS	$\varepsilon_r = \frac{R_p}{R_s}$ =0.001= -30dB	$\varepsilon_r = \frac{R_p}{R_s}$ =0.033= -14.8dB	β = 0.8= -0.96dB

Table 3.3. Matrix approach parameters of the LC and PBS used.

By introducing these values on Table 3.2, we obtain the theoretical Table 3.4. It can be observed that by introducing a vertical polarised light [0,1] as input signal, the attenuated signal detected at each stage is also going to be a vertical polarised signal of value [0,n$\alpha\beta$] where n is the number of stages that the signal goes through. On the other hand, the value for the maximum crosstalk detected corresponds to an elliptically polarised light of value [$\alpha\varepsilon_r$, $\beta\varepsilon_1$].

	Output 1 Selected	Output 2 Selected	Output 3 Selected	Output 4 Selected
Output 1	$\begin{bmatrix} 8\cdot10^{-4} \\ 0.6 \end{bmatrix} = -2.2dB \approx \alpha$	$\begin{bmatrix} 2.5\cdot10^{-2} \\ 1.6\cdot10^{-2} \end{bmatrix} = -13.86dB$	$\begin{bmatrix} 2.5\cdot10^{-2} \\ 1.6\cdot10^{-2} \end{bmatrix} = -13.86dB$	$\begin{bmatrix} 2.5\cdot10^{-2} \\ 1.6\cdot10^{-2} \end{bmatrix} = -13.86dB$
Output 2	$\begin{bmatrix} 0.5\cdot10^{-3} \\ 0.86\cdot10^{-3} \end{bmatrix} = -28.6dB$	$\begin{bmatrix} 4\cdot10^{-4} \\ 0.36 \end{bmatrix} = -4.4dB \approx 2\alpha$	$\begin{bmatrix} 1.5\cdot10^{-2} \\ 1.2\cdot10^{-2} \end{bmatrix} = -15.65dB$	$\begin{bmatrix} 1.5\cdot10^{-2} \\ 1.2\cdot10^{-2} \end{bmatrix} = -15.65dB$
Output 3	$\begin{bmatrix} 0.30\cdot10^{-3} \\ 0.25\cdot10^{-3} \end{bmatrix} = -32.5dB$	$\begin{bmatrix} 0 \\ 5.9\cdot10^{-3} \end{bmatrix} = -22.3dB$	$\begin{bmatrix} 2\cdot10^{-4} \\ 0.216 \end{bmatrix} = -6.6dB \approx 3\alpha$	$\begin{bmatrix} 8.9\cdot10^{-3} \\ 7.4\cdot10^{-3} \end{bmatrix} = -17.8dB$
Output 4	$\begin{bmatrix} 0.18\cdot10^{-3} \\ 0.15\cdot10^{-3} \end{bmatrix} = -34.8dB$	$\begin{bmatrix} 10.6\cdot10^{-6} \\ 13.2\cdot10^{-6} \end{bmatrix} = -46dB$	$\begin{bmatrix} 1.5\cdot10^{-4} \\ 2.4\cdot10^{-4} \end{bmatrix} = -33.6dB$	$\begin{bmatrix} 1\cdot10^{-4} \\ 0.1296 \end{bmatrix} = -8.9dB \approx 4\alpha$

Table 3.4. Theoretical results obtained by substituting the parameters of Table 3.3 on Table 3.2 when an input s-polarised light, I= [0, 1] = [0.4, 400] uW is used.

From Table 3.4 a value of −2.16 dB is obtained for the attenuation per stage and −13.89 dB for the maximum crosstalk. It can be observed that the value of the maximum misdirected signal detected is approximately 2 dB higher than the contribution of any other source placed at a further distance.

These results agree with the experimental values presented in Table 3.5 where it can be observed an average attenuation per stage is of −2.28 dB and a maximum crosstalk of −13.63 dB. The differences of 0.12 dB for the attenuation and 0.26 dB for the maximum crosstalk can be attributed to the misalignment between the LC and the incoming vertical polarised signal.

Input [0.4, 400]uW	Selected #1	Selected #2	Selected #3	Selected #4
Output 1	-2.4dB	-13.9dB	-13.4dB	-13.6dB
Output 2	-30dB	-4.6dB	-15.6dB	-15.7dB
Output 3	-31dB	-25dB	-6.7dB	-17.5dB
Output 4	-33dB	-40dB	-35dB	-8.9dB

Table 3.5. Results obtained experimentally.

Therefore, by comparing both tables it can be concluded that the matrix model is applicable to this architecture and it can be used theoretically to explore the maximum number of stages that the system can support in terms of attenuation and crosstalk.

Equation 3.1 shows the relation between the maximum number of stages the signal can pass through, N, the attenuation at each stage, A, the minimum Contrast Ratio, CR = 1/ [maximum crosstalk], and the optical signal-to-noise ratio (OSNR) required to obtain a certain bit error rate.

$$CR\ (dB) = OSNR(dB) + N \times A\ (dB) \qquad \text{Equation 3.1}$$

Equation 3.1 also assumes that crosstalk is the dominant noise. In [54], it was probed that if the use of detectors sufficiently sensitive with a noise-equivalent power (NEP) of around 10^{-12} $WxHz^{-1}$ and sufficiently powerful emitters (1 mW), then it could be concluded that other noise sources such as thermal noise and shot noise could be neglected.

The minimum CR achieved in the system which is inversely proportional to the maximum crosstalk, occurs at Output 1 when any other port is selected for routing the signal out of the system. This value is given by the expression, $RP_1I = [\varepsilon_r\alpha, \beta\varepsilon_1]$. The attenuation per stage A is given by the expression $[0, \alpha\beta]$. For the OSNR a value of 12 is assumed, which is the minimum value to achieve a bit-error rate (BER) of at least 10^{-9}. By solving N in Equation 3.1, we obtain;

$$N = \frac{CR(dB) - SNR}{A(dB)} = \frac{-10\log(\varepsilon_r\alpha + \varepsilon_1\beta) - 10\log 12}{-10\log(\alpha\beta)} = \frac{\log(12(\varepsilon_r\alpha + \varepsilon_1\beta))}{\log(\alpha\beta)} \qquad \text{Equation 3.2}$$

Ideally, low attenuation and low crosstalk are desirable. This result can be achieved by using high-quality optical devices with low attenuation and high contrast ratio as can be deduced from Equation 3.2. However, having analysed the polarised nature of attenuation and crosstalk, it is found that there are other ways of achieving better results. As mentioned previously, the attenuated signal is vertically polarised light and the maximum crosstalk is an elliptic, almost circular light. Therefore, if a high-transmission cleanup polariser is used at the end of each port, orientated to vertical polarisation [0,1], the first component of the crosstalk ε_r can be extinguished. Using the matrix approach model we can characterise the cleanup polariser as $P_{cleanup} = \begin{bmatrix} \varepsilon_p & 1 \\ 1 & \alpha_p \end{bmatrix}$, where ε_p is the extinction ratio and α_p is the attenuation of the polariser. This attenuation contributes only once at the end of the system and therefore the signal attenuated is now $[0, n\alpha\beta + \alpha_p]$ and the maximum crosstalk signal is $[0, \alpha_p\beta\varepsilon_1]$.

These results were demonstrated experimentally using a polariser with $\alpha_p = -1.1$ dB. The maximum crosstalk signal decreased from −13.63 dB to −20 dB, while the attenuated signal decreased from −2.28 dB to −3.38 dB. Therefore, the introduction of cleanup polarisers at the end of each port increased the optical budget by 5.27 dB.

Following from this, it can concluded that the use of both cleanup polarisers and high quality optical devices can contribute to considerable increases in the maximum number of stages that the signal can pass through before it becomes too weak.

As an example, below is a calculation of the maximum number of stages using cleanup polarisers and high-quality optical elements such as that reported in Table 3.6.

	Crosstalk		Attenuation
Liquid Crystal [9]	ε_0 (LC On)=0.013=-19dB	ε_1 (LC Off)=0.013=-18dB	α =0.93=-0.3dB
PBS [10]	$\varepsilon_r = \frac{R_p}{R_s}$ =0.02=-17dB	$\varepsilon_r = \frac{R_p}{R_s}$ =0.01=-20dB	β =0.98=-0.1dB
Polarizer [11]	ε_p =0.001=-30dB		α_p =0.9=-0.4dB

Table 3.6. High-quality values of PBS, LC and high-transmission polariser.

Equation 3.2 was modified to include the effect of the cleanup polariser and the relation between N and the quality of the parameters. The result is shown in Equation 3.3, where the values of the Table 3.6 can be substituted to obtain N =20.

$$N = \frac{CR(dB) - SNR(dB) - A_{Pcleanup}(dB)}{A(dB)} = \frac{\log\left(\frac{12(\alpha\varepsilon_p\varepsilon_r + \alpha_p\varepsilon_1\beta)}{\alpha_p}\right)}{\log(\alpha\beta)} \qquad \text{Equation 3.3}$$

Figure 3.12 shows more clearly the relation expressed in Equation 3.3 between attenuation, crosstalk, and OSNR when high quality optical elements and cleanup polarisers are used.

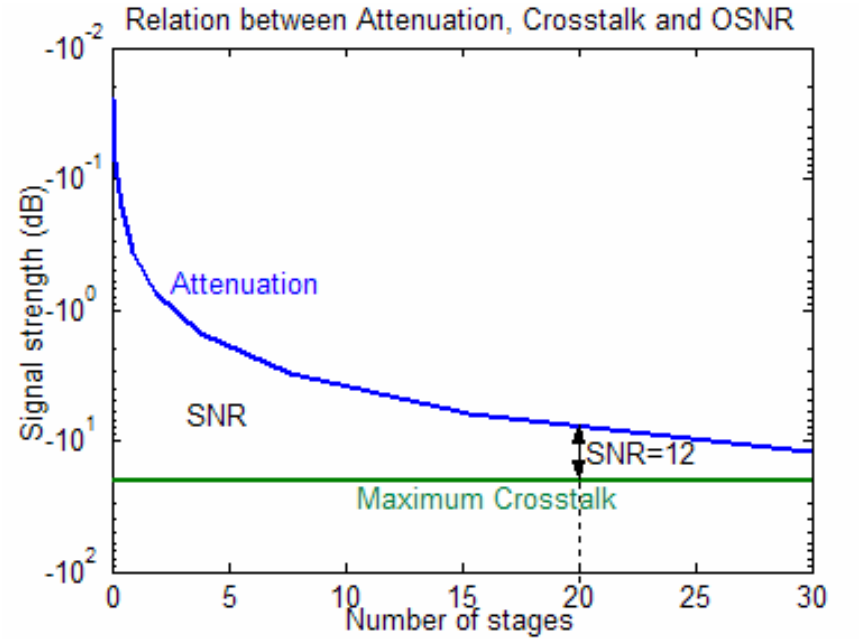

Figure 3.12. Maximum number of stages that can be achieved using high-quality optical elements and cleanup polarisers.

3.5 Conclusion

This chapter has shown the optimal use of WGP and off-the-shelf LC for implementing the stages of the OH. The use of RP as a fast and low cost fabrication technique for implementing the different architectures of the OH has also been proposed. Additionally, the scalability of the OH has been analysed by studying the maximum number of stages that the optical signal can pass through when the maximum crosstalk of the system is caused by misdirected signals. It has been proved that by combining both high-quality optical elements and cleanup polarisers, the crosstalk can be decreased without significantly increasing the attenuation in the system. Therefore, the optical signal could pass through more stages without the necessity of being regenerated.

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Chapter 4
Characterisation of a Reconfigurable Free Space Optical Channel

4.1 Introduction

This chapter will show different experiments that characterise the properties of a reconfigurable free space optical signal that goes through the OH.

For this purpose, a modulated optical signal will be employed instead of a CW optical signal used in the previous chapter. This will allow us to use Eye Diagrams (ED) as an analysing technique for characterising the OH.

Moreover, a completely new set of optical components will be used: diode laser, optical collimators, polarisers, Si photodetectors and most importantly, a new transmissive 90° TN-LC. This off-the-shelf LC obtained from Excel Display allows twisting the linear polarisation more accurately and has less losses than the one used in chapter 3, where two 45° TN-LCs were needed and carefully aligned in order to perform the 90° twisting.

The first section of this chapter will be focused on the individual characterisation and optimisation of each new component.

The second section will characterise an optical stage, LC/PBS assembly, of the OH. Polarisation tolerance of the system will also be analysed.

The last section will characterise and optimise three stages of the OH. For this purpose, a new mechanical structure is designed using the RP technique once again.

4.2 Characterisation of Optical Signal and Components

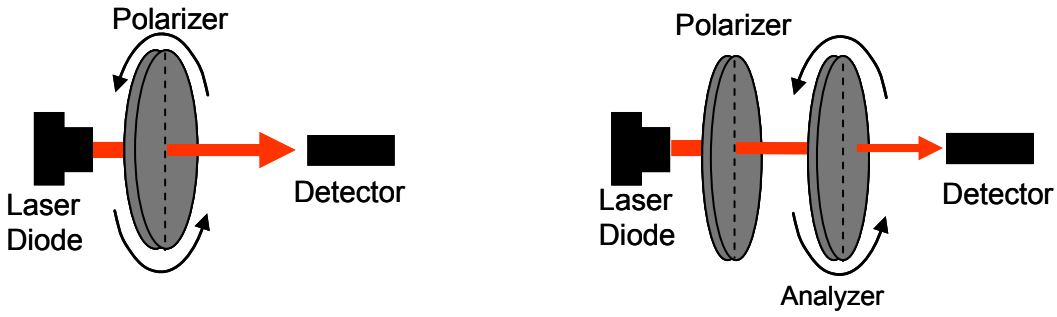
This section will show a series of experiments oriented to characterise and optimise the polarisation nature of the optical source used, the eye diagram of the electrical signal used to drive the source, and the eye diagram of the free-space optical signal obtained. Finally, the new LCs obtained from LCDisplay will be characterised and optimised as well.

4.2.1 Polarisation Characteristics of Diode Laser and Polariser

Since the switching of the optical input to the different optical outputs is achieved by using polarised light rotated with the LC, the polarisation nature of the optical source becomes crucial.

This experiment involves the use of a Hitachi AlGaInP Laser Diode (630nm, 3mW CW) as a source, a Thorlabs LD collimating tube with precision lens mount and adjustable focus to produce a parallel output beam, a linear polariser film (25% transmission, 99% polarisation efficiency) and a 917 NewPort Optical Power detector.

Figure 4.1 shows the set up of the experiment that was carried out. The optical signal from the Laser Diode (LD) was analysed rotating a polariser at different angles. The properties of the polariser was analysed using a second polariser, namely an analyser. In this case, the polariser was fixed to the position of maximum transmission and the analyser was rotated.



(a) (b)

Figure 4.1. a) Characterisation LD output. b) Characterisation polariser output.

Figure 4.2 shows the results obtained when a polariser is rotated in front of the LD and when an analyser is rotated in front of the previous polariser. The output from the LD (first graph) is linearly polarised with a polarisation extinction ratio, 160:1. However a higher polarisation extinction ratio 1000:1 is achieved in the second graph. Therefore, for this set up a polariser will be placed in front of the LD in order to increase the extinction ratio of the polarised light generated by the LD.

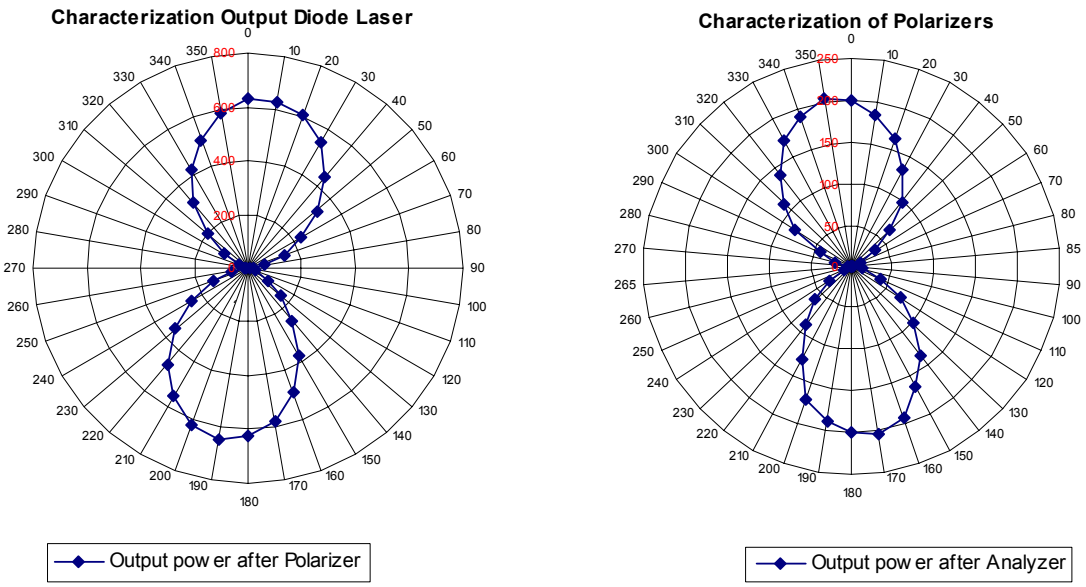


Figure 4.2. Output characteristic of the LD and polariser for an initial output power of the LD is 1.62 mW, a background of 0.07 uW and at 19 °C.

4.2.2 Characterisation of the Electrical Signal used to Drive the Laser Diode

This experiment was carried out in order to characterise and determine the electrical signal generated by the Tektronic Stimulus System that has been used to drive the LD.

Optical communication is mostly done in binary format, i.e., the messages are put into a sequence of zeros (0) and ones (1). At the physical level, 1s can be encoded in at least two ways, while for a 0, no light beam is transmitted. One way to encode a 1 is to send a constant light intensity for the entire bit period: The other method is to send a pulse shorter than the bit period. The first method of encoding is called non-return-to-zero (NRZ) and the second method is termed as return-to-zero (RZ). When the pulse duration

is much shorter than the bit period, the pulses are referred to as short pulses (Figure 4.3).

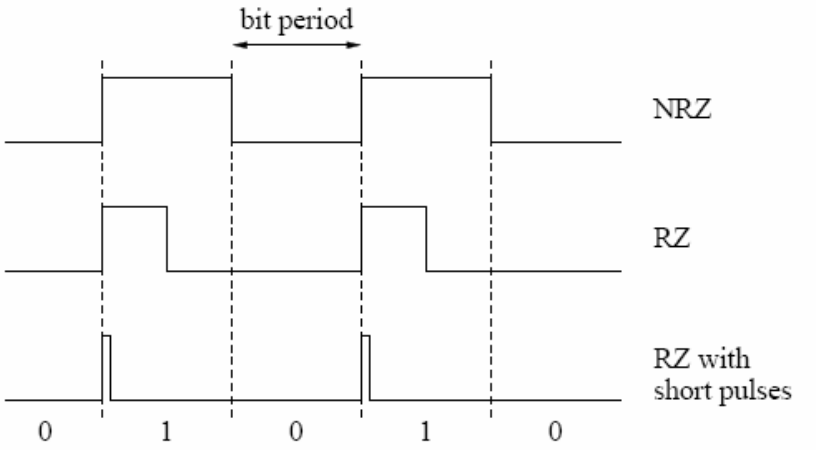


Figure 4.3. Schematic demonstration of NRZ and RZ coding.

The use of the symbol P1 represents the high power level and the symbol P0 represents the low power level. These symbols will be used to mathematically define a number of useful terms and relationships.

Optical Modulation Amplitude (OMA) is the difference between the logic high power level and logic low power level.

$$OMA = P1 - P0 \qquad \text{Equation 4.1}$$

Extinction Ratio (r_e) is the ratio of the logic high power level to the logic low power level.

$$r_e = P1/P0 \qquad \text{Equation 4.2}$$

BER is determined entirely by the optical signal-to-noise ratio, which is commonly called the Q-factor [1] .

$$Q = \frac{OMA}{\sigma_1 + \sigma_0}\left(\frac{r_e - 1}{r_e + 1}\right) \qquad \text{Equation 4.3}$$

The Q-factor is defined as the OMA divided by the sum of the rms noise on the high and low optical levels. The term $(1- r_e)/(1+ r_e)$, known as power penalty, is due to the difference between P0 and 0.

Up to this point in the discussion, it may seem apparent that OMA and r_e are basically equivalent. Either can be calculated with knowledge of the other and one reference point. Both can be quantified when the values of P1 and P0 are known. However, there are important differences. One particularly interesting point is how OMA and r_e change as the signal propagates through the optical system.

Assuming a system with a linear attenuation between two points, the r_e will stay constant even though the signal is attenuated, while the OMA will change by a factor equal to the attenuation.

A technique known as eye diagram was used to evaluate optical transmitters and digital signals in general. Eye diagrams are a very successful way of assessing the quality of a digital signal [2]. A properly constructed eye should contain every possible bit sequence from simple 101s and 010s, through to isolated 1s after long runs of consecutive 0s and other sequences that often show up weaknesses present in system designs.

Eye diagrams show parametric information about the signal and effects deriving from physics such as health of system bandwidth. It will not show protocol or logical problems. If a logic 1 is healthy on the eye, this does not reveal the fact that the system meant to be 1. However, if the physics of the system means that a logic 1 becomes so distorted while passing through the system that the receiver at the far end mistakes it for a zero, this should be shown in the eye diagram. In this experiment, the eye diagram will be used to measure and compare the OMA, r_e and Q of the optical signal at different stages of the system.

In order to obtain an eye diagram of a free space optical signal, a Tektronix Programmable Stimulus System HFS9009 was used for generating the following data signals: On-Off-Key (OOK) code, Non-Return-to-Zero (NRZ) data stream with <20ps rise and fall times. For driving the LD within the specifications, the amplitude of the digital signal was set at 400mV and offset at 2.5 V. The pulse generator had a bandwidth from 50 KHz to 630 MHz. With the use of the Infimun Agilent 6 GHz Real Time Scope, the eye diagram of the raw electrical signal was analysed for this range of frequencies. The scope was triggered with an external signal obtained from the pulse generator.

Figure 4.4 shows both the pulse signal used as trigger at 50 KHz (yellow) and the NRZ pseudo-random sequence of bits generated by the pulse generator (red) at 25 Kb/s.

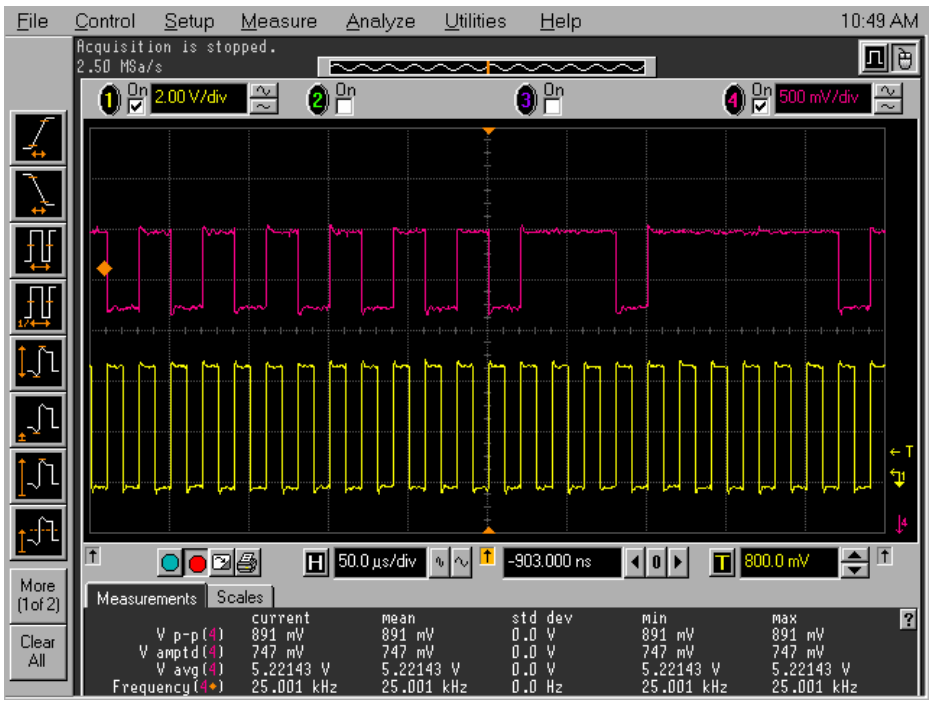


Figure 4.4 Pulse signal (yellow) used as trigger and pseudo-random sequence of bits (red) at 50 KHz, 25 Kb/s, generated by Tektronix Stimulus System.

In Figure 4.5 we can see the ED of the electrical signal for different frequencies. It can be observed that the electrical signal achieves excellent performance from 50 KHz to 5 MHz.

Since the objective of this experiment is to study the polarisation efficiency of a free space optical signal that passes through the OH, data rate is not crucial. Therefore, a low data rate will be selected in order to prevent the electrical signal from affecting the quality of the optical signal.

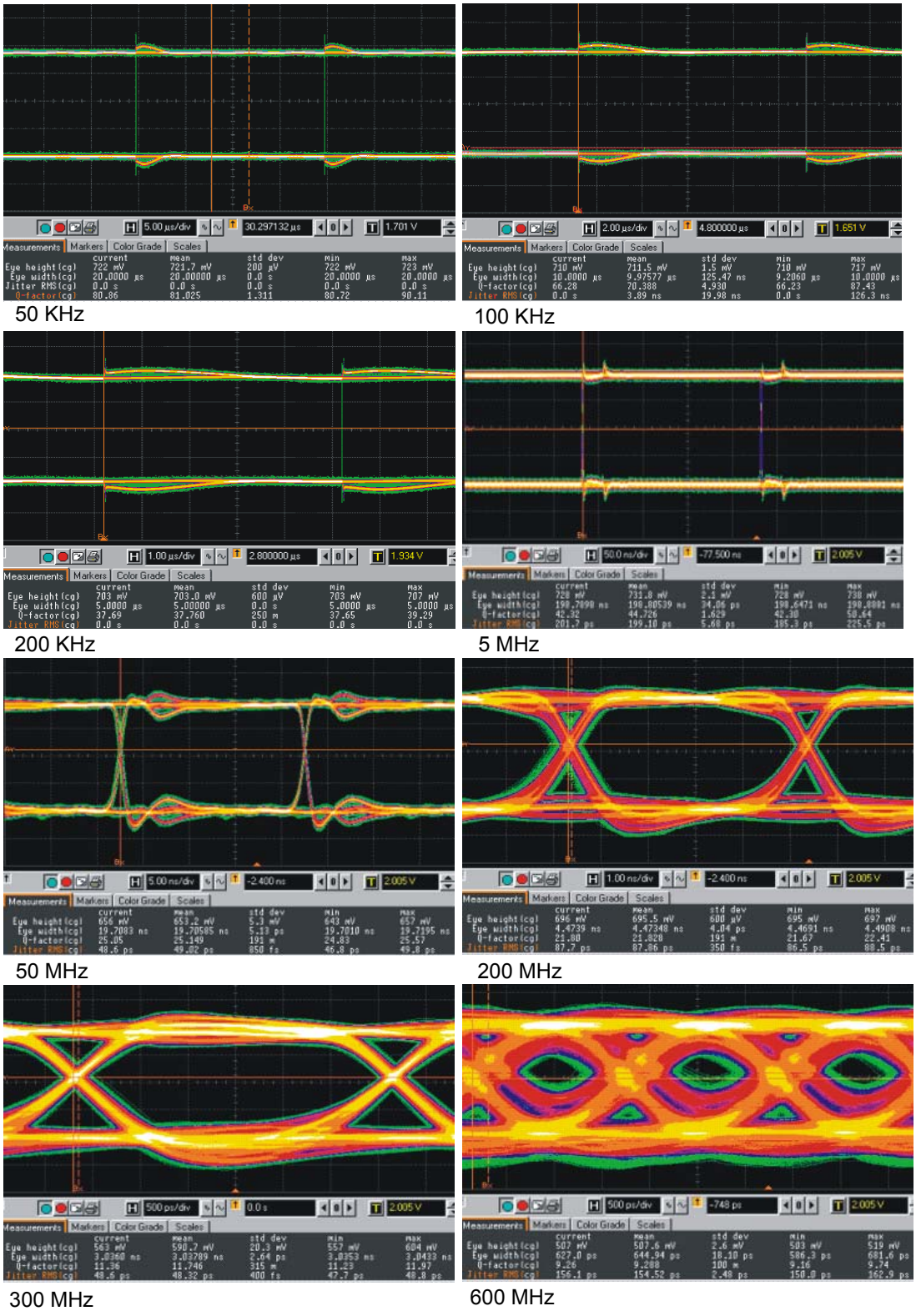


Figure 4.5. Eye Diagram of the electrical signal at different frequencies of operation.

4.2.3 Eye Diagram of the Optical Signal

This section will analyse the ED of a free-space optical signal for different frequencies. The experiment carried out will provide the information necessary to decide which data rate will be set up in the system for the rest of the experiment.

In order to obtain a stable optical output power the LD is contained in a small transistor-like metal case fitted with a window. This is held in a metal block that is temperature controlled by using a Peltier cooler to transfer heat to the heat sink under electronic control. The LD has to be driven at an operating voltage of 2.7 V and an operating current of 20-55 mA. In so doing, a resistance of 65.5 ohm is placed in series with the stimulus system as shown in Figure 4.6.

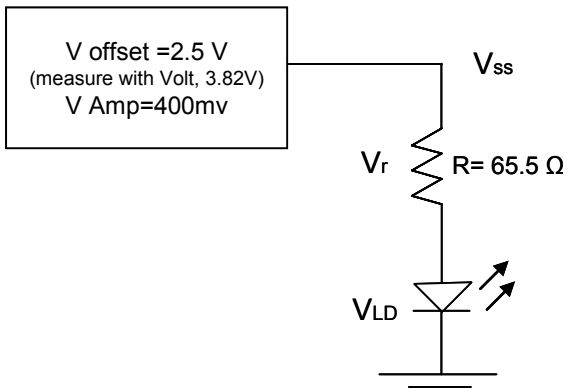


Figure 4.6. Driving the LD. It has been experimentally obtained that Vss=3.82 V, Vr= 1.6 V and V_{LD}=2.225 V. The current the simulus system generates is: Ir x R =Vr, Ir= 1.6V/65.5=24.4mA. Therefore, the LD is working within the specifications, V_{LD}=2.225 V, I_{LD}=24.4 mA.

Figure 4.7 shows the set up for recovering the optical signal propagated around 15 cm in free space and recovered by a Thorlabs free space amplified, switchable-gain, silicon detector designed for detection of light signals from DC to 10 MHz.

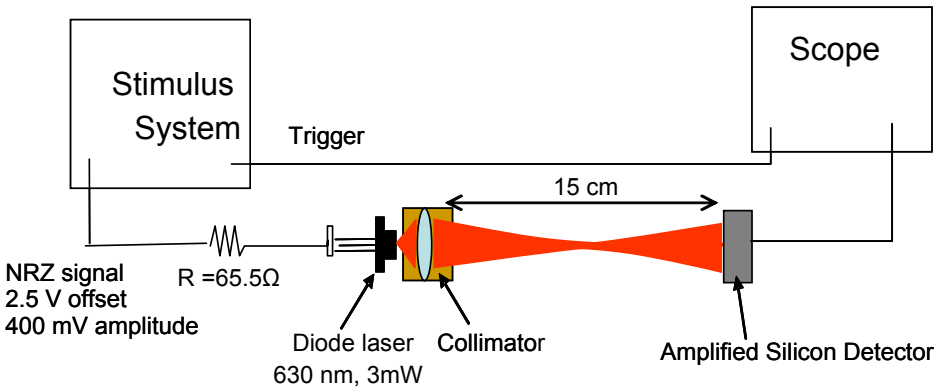
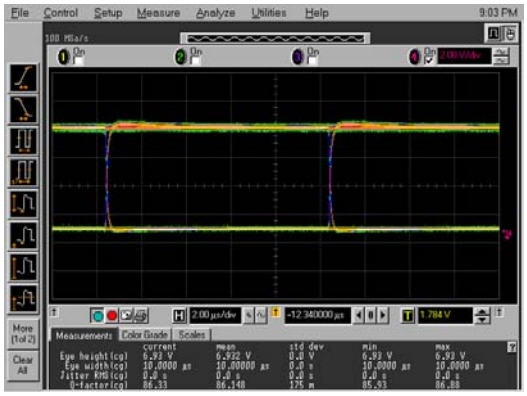


Figure 4.7. Set up for characterising the free-space optical signal at different frequencies.

The ED of the free space optical signal obtained with the scope at different frequencies is presented in Figure 4.8. It can be observed that at half the maximum operation frequency of the amplified detector (5 MHz) the EDs of the optical signal starts to close. As said before, speed is not under examination in this experiment. Thus a slow frequency is chosen, (50 KHz) as an operating frequency, where the ED of the optical signal can be considered as ideal, the jitter RMS (deviation from real time event) is 0, and the quality factor is 80, which is much bigger than Q=6, the minimum value for achieving a BER of 10^{-9}.

50KHz

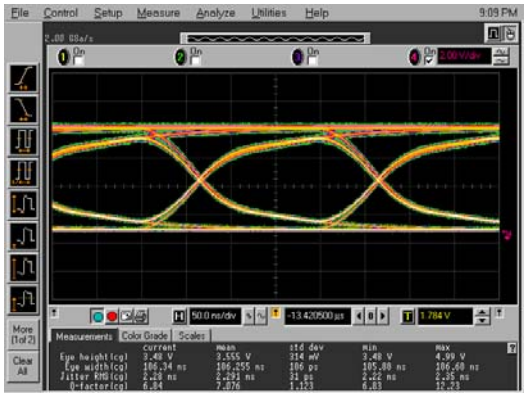


100KHz

500 KHz

1 MHz

2 MHz



5 MHz

Figure 4.8. Eye Diagrams of the free space optical signal at different frequencies.

4.2.4 Characterisation of the 90° Twisted Nematic Liquid Crystal

In this section, the LV00S liquid crystal obtained from Excel Display [2] will be characterised and optimised. These LCs are transmissive, 90° twisted nematic and consist in only one pixel of an area of 2.5 cm x 2.5 cm. They are off-the-shelf components that were originally designed to be used as optical shutters. However, for this purpose Excel Display supplied us with LCs without input and output polarisers typical in these types of devices.

Parameters of the LC

Before continuing the discussion of the results obtained, it is worth mentioning again the parameters defined in the previous chapter used to measure the quality of the LC; The contrast ratio of the LC at each state is ε_0 (LC On) and ε_1 (LC Off), and the attenuation of the LC, α. The contrast ratio ε_0 measures how well the LC twists polarised light by 90°. This is achieved by measuring the intensity detected after a polariser; Po is placed at the output of the system which is oriented parallel or perpendicular to the input polariser, Pi. When the LC is Off, the polarised light is supposed to twist by 90°. Therefore, the intensity detected when Pi and Po are perpendicular has to be as high as possible and when they are parallel they have to be as low as possible. The parameter ε_1 measures how well the LC keeps the polarised light untwisted. In this case, the maximum power is detected when both polarisers, Pi and Po, are parallel to each other and the minimum power is detected when they are perpendicular to each other.

$$\varepsilon_0 = -10\log\left(\frac{I_{Po\perp Pi}}{I_{Po\,//\,Pi}}\right)_{LC\ On} \qquad \text{Equation 4.4}$$

$$\varepsilon_1 = -10\log\left(\frac{I_{Po\,//\,Pi}}{I_{Po\perp Pi}}\right)_{LC\ Off} \qquad \text{Equation 4.5}$$

From equations 4.4 and 4.5 we can see that the lower the values of ε0 and ε1 in dB are, the better the LCs work.

Figure 4.9 shows the set up of the experiment carried out in order to obtain these two parameters.

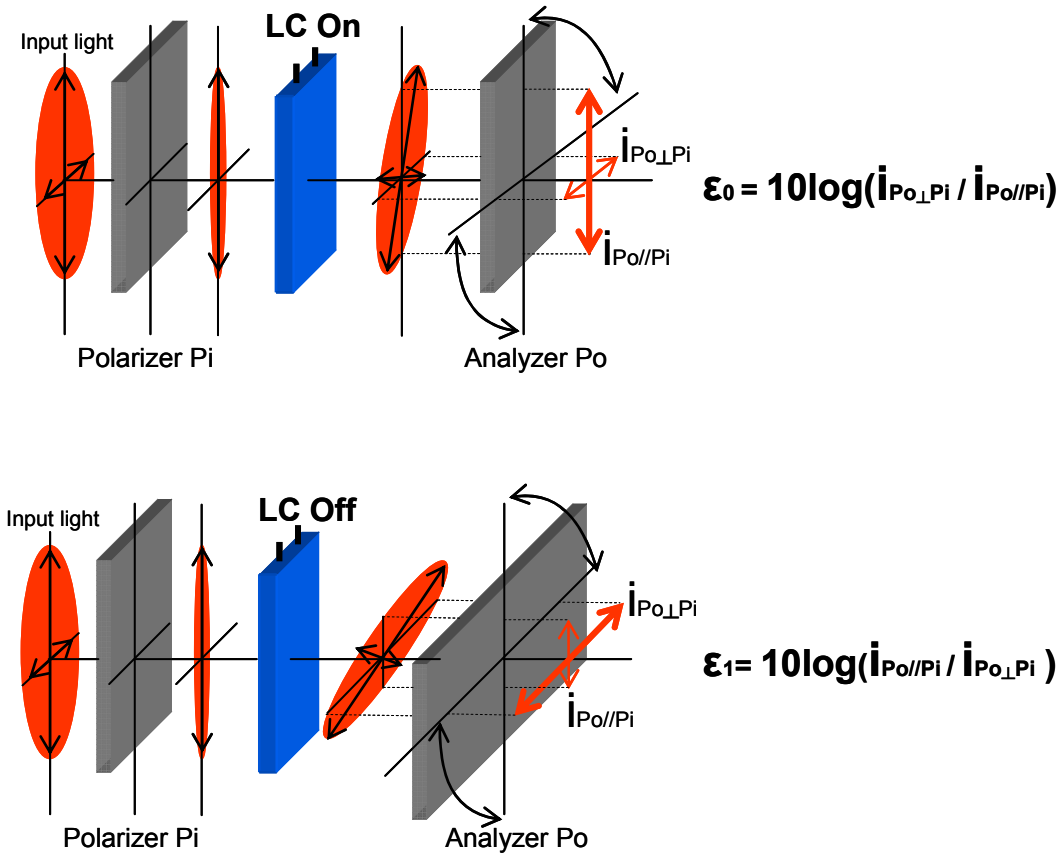


Figure 4.9. Experimental set up for determining ε_0 and ε_1.

It has been proven experimentally that the attenuation does not change significantly for different voltages and the value is α = -0.7dB. On the other hand, the contrast ratios ε_0 and ε_1 vary depending on different factors.

Voltage Characterisation

The set up shown in Figure 4.9 has been used for finding ε_0 and ε_1 when different voltages are applied to the LC.

As observed in Figure 4.10 the LC starts to work as desired at around 7 V. At this voltage, the LC starts to keep the initial polarised light almost invariable, while in the Off state the polarised light is twisted. Therefore, it has been decided to set the LC at a safe voltage value of 8 V (far from the maximum 10 V), and where both ε_0 and ε_1 have similar values.

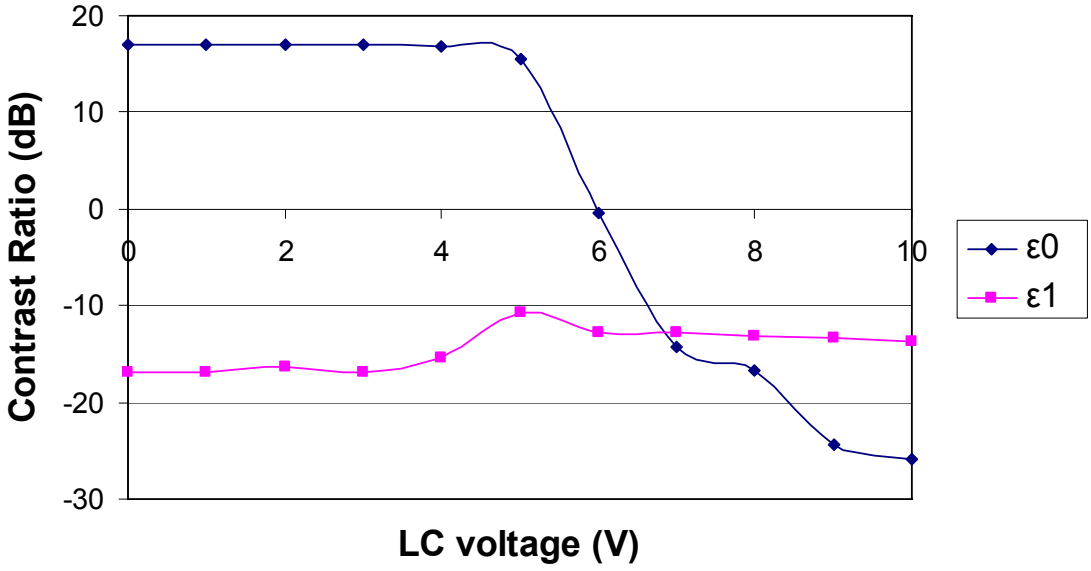


Figure 4.10. Contrast ratios ε_0 and ε_1 for different LC voltages.

Characterisation under Translational Displacement

The following experiment consists of the study of ε_0 and ε_1 for different positions of the LC with respect to the optical beam.

Since the area of the LC (484mm^2) is approximately 30 times bigger than the area of the beam spot (7mm ^{2}) it is useful to check if there is any difference in pointing the laser beam to different positions of the LC, Figure 4.11.

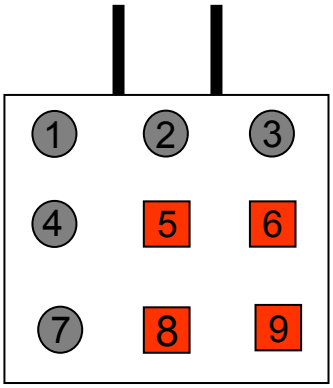


Figure 4.11. Different positions of the LC where the laser beam has been pointed. The grey circular spots show the places that have achieved low contrast ratios, while the square red spots represent the places where good contrast ratios have been achieved.

Figure 4.12 shows the different values for ε_0 and ε_1 obtained for the nine different positions where the LC was placed with respect to the beam spot. For the value of ε_0, the LC was set to 8 V, as we concluded previously.

It can be observed that although both contrast ratios are negative for all the positions, only positions 5, 6, 8 and 9 present very high negative values. Similar experiments were carried out with other LV00S LCs supplied by Excel Display. It was found that some of the good positions change from one LC to another. However, the central position, 5, always achieves similar good contrast ratios. The positions where the contrast ratio, ε_1, is a low value may not be able to support many stages but would however be adequate for its intended use as a cost effective shutter.

Different explanations have been suggested for justifying such a big discrepancy. For example, the lack of reproducibility in a process called rubbing which causes surface alignment of liquid crystal molecules, or the difficulty to fill large-sized LC cells with such materials using state of the art techniques without suffering some degree of phase separation between the components as well as inducing possible inhomogeneous variations in the anchoring-energy between the cell alignment-layers and said liquid crystal materials [4]. Another problem may be electrostatic problems caused due to the use of DC voltage during long time to drive the LCs. However, it is beyond this thesis to analyse the reason of this behaviour. The objective is to optimise the LC in order to obtain the minimum stable values for the contrast ratios ε_0 and ε_1, and it has been found that pointing the beam to the centre of the LC these good values can be achieved.

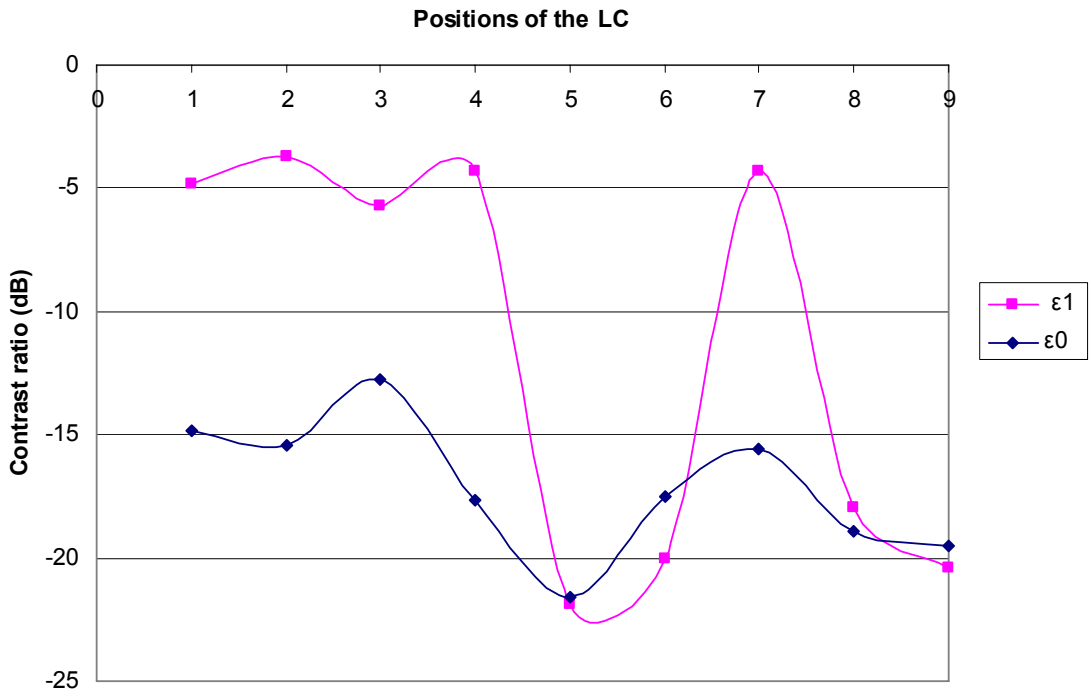


Figure 4.12. Contrast ratios under translational displacement with respect to the beam spot.

LC Characterisation under Rotational Displacement

The characterisation of the LC is completed with a final experiment which consists in studying how the contrast ratios ε_0 and ε_1 change for different rotational positions of the LC. As we have seen previously, the LC has an active axis which must be aligned with the input linear polarisation in order to twist it as we desire.

Figure 4.13 shows the results obtained when the LC is rotated from 0° to 90° and the spot beam is pointed at the centre of the LC. From these results we can conclude that the optical axis of the LC is oriented at 45°. However, it can be seen that the dependence of ε_0 and ε_1 respect to the rotational orientation of the LC is not as important as the voltage or translational dependence. Therefore, in order to simplify the design of the mechanical structure and the set up of the three stage experiment that will be carried out, the LC will be placed at 0º. In other words, in a vertical position, with the connectors on the top and the light beam pointing to the centre of the LC.

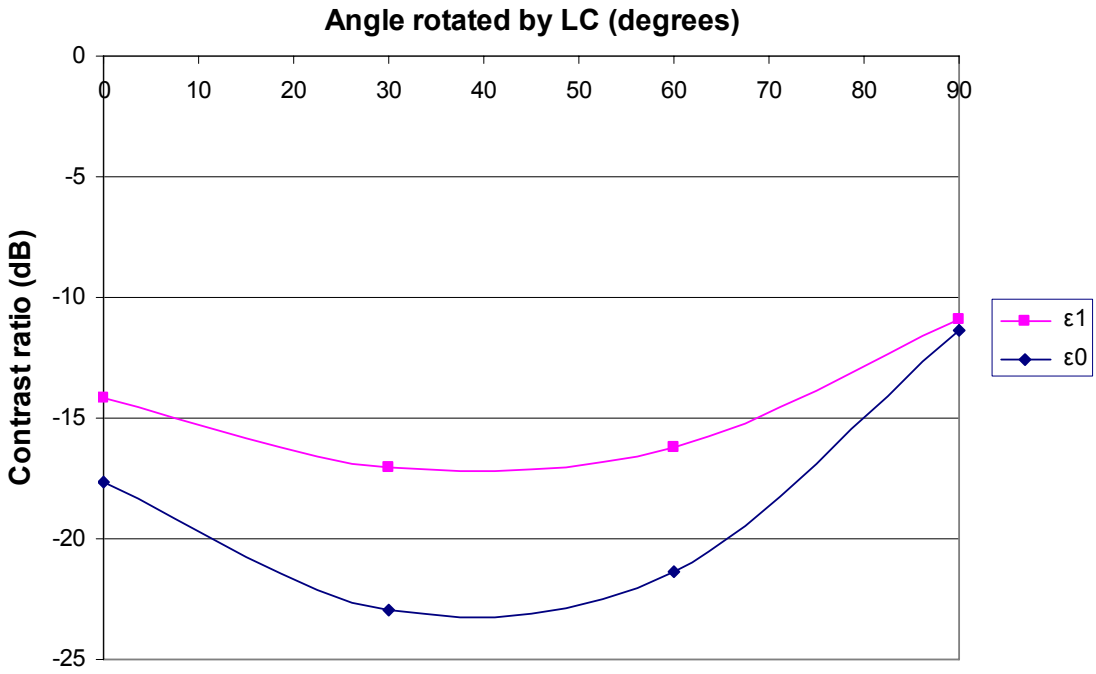


Figure 4.13. Contrast ratios ε_0 and ε_1 for different orientations of the LC.

Achieving Large Contrast Ratios

Based on the experiments carried out with the Excel Display LC it was concluded that the most convenient configuration for this purpose is when the LC is set at a voltage of 8 V and oriented at 0º. Figure 4.14 shows how a linear polarised beam, which was characterised at the beginning of this chapter, is affected by the LC. An analyser at the output of the LC was used in order to obtain the polarisation characteristic of the beam after passing through the LC.

The first thing that can be observed is that when either vertical, p-polarised, or horizontal, s-polarised, light is used as initial input, the LC keeps the linearity of the polarised light for both states of the LC, On and Off. Secondly, it can be observed that by switching the LC On-Off or Off-On the polarised light is twisted by 90°, which is the result that was sought in order to use an efficient polarised beam router system. Under these conditions the parameters for the contrast ratios ε_0 and ε_1 and the attenuation are -19 dB, -19 dB and -0.7 dB respectively.

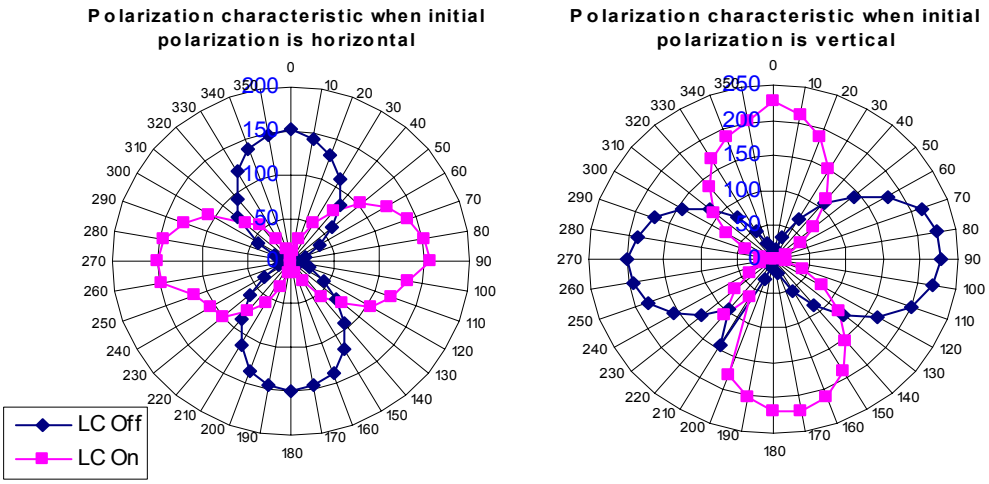


Figure 4.14. Characterisation of p-polarised and s-polarised light when the LC is Off and On.

Figure 4.15 shows the eye diagrams obtained when the modulated optical signal characterised in section 4.2.3 (50 KHz, NRZ data stream) is routed through the set up shown in Figure 4.9 and the LC is set at the values discussed above.

From Figure 4.15 we can see that the LC is working as desired. When the LC is Off, the linear polarised light is twisted 90°, and a clear open eye can be observed when an analyser Po is placed perpendicular to the input linear polarised light. On the other hand, no eye diagram is formed when the analyser is placed parallel to the input linear polarised light. Similar results are achieved when the LC is On. In this case, a clear open eye is obtained placing the analyser parallel to the input linear polarised light, and no eye is formed when Po is placed perpendicular.

It is worth noting that the values of the optical signal detected when no eye is obtained are lower than the minimum value that represents bit 0 when an eye is generated. Therefore, it can be considered that in this condition there is no crosstalk due to miss-directed signal.

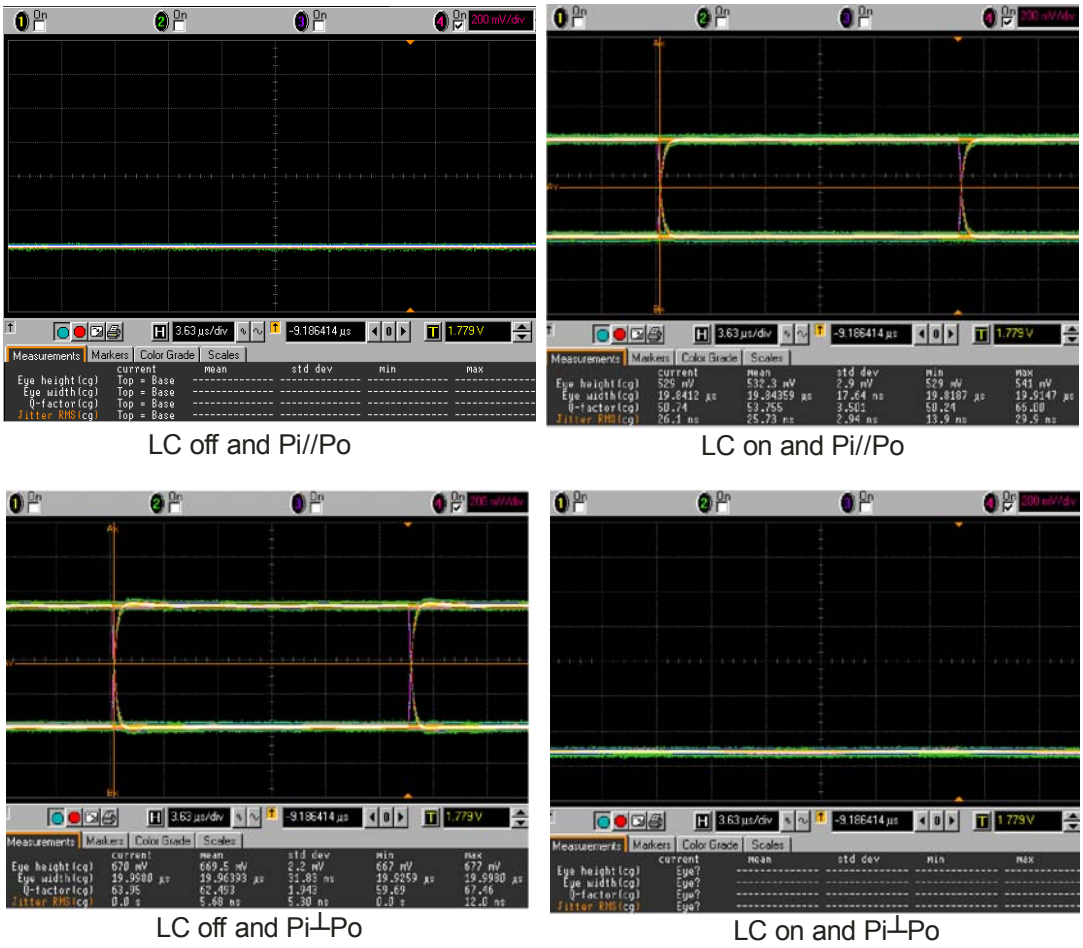


Figure 4.15. Eye Diagram obtained after the optical signal goes through the LC, which is set at 8 V, oriented at 0° and the light beam is pointed to the centre of the LC.

4.3 Eye Diagram Characterisation of One Stage of the Optical Highway

In this section, one stage of the OH (LC/PBS assembly) will be characterised. As defined previously, an optical stage is the smallest optical system necessary for reconfiguring the optical signal, Figure 4.16.

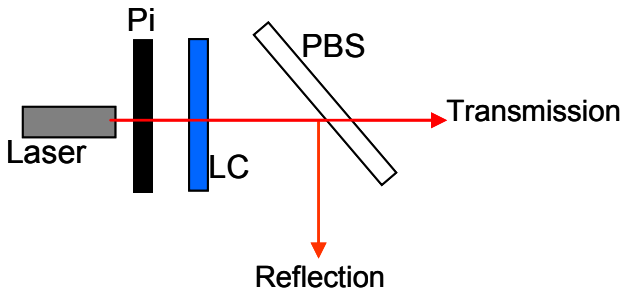


Figure 4.16. Set up for characterising one optical stage.

The PBS used in this experiment is the same characterised in the previous chapter, a broadband WGP. Therefore, all the individual elements that constitute one stage have already been characterised and optimised.

First of all, it has been found that the attenuation of one optical stage is 1.4 dB, 72.24% of the input optical power is transmitted. Secondly, Figure 4.17 shows the EDs obtained from the two outputs of the optical stage, reflection and transmission. From this figure we can observe two clear EDs: the first one, with an eye height of 1.664 V is obtained on the reflection output when the LC is Off; and the second one, with an eye height of 1.530 V at transmission output when the LC is On. On the other hand, minimum outputs considered as mis-directed signals, are obtained for transmission when LC is Off and for reflection when LC is On. In the last case, because of the relatively high crosstalk in the reflected path, $\varepsilon_r \approx -14{,}8\,dB$ of the WGP, a closed ED can be observed. However, even in this worst case, the mis-directed signal is lower than the minimum value that represents the bit 0 when the LC is Off and the desired signal is routed to the reflection output.

We can conclude that the reconfigurability efficiency of the optical stage is approximately 95%. This means that 95% of 72.24% of the input optical power that is

transmitted through the optical stage is re-routed satisfactorily from one output to the other. It is worth noting that the 5% that is not re-routed does not really contribute as a misdirected signal and therefore it does not increase the crosstalk of the system.

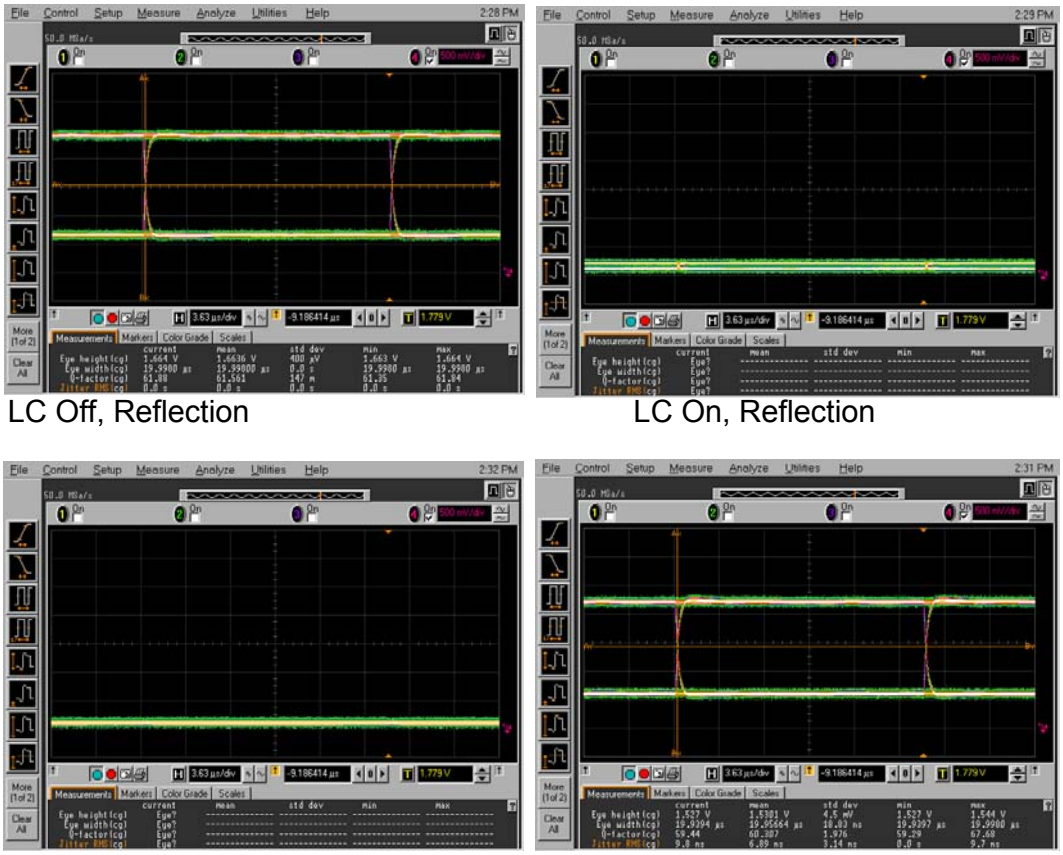


Figure 4.17. Eye Diagram of the optical signal obtained at the reflected and transmitted outputs of the optical stage, when the LC is switched Off and On.

4.3.1 Tolerancing of Polarisation Losses in the Optical Highway

We can consider the result obtained previously as spectacular, mainly because no microalignment systems have been used to achieve such good results. In fact, the 95% of polarisation efficiency has been obtained using tolerances to rotational misalignment of the LC and the WGP of 45°.

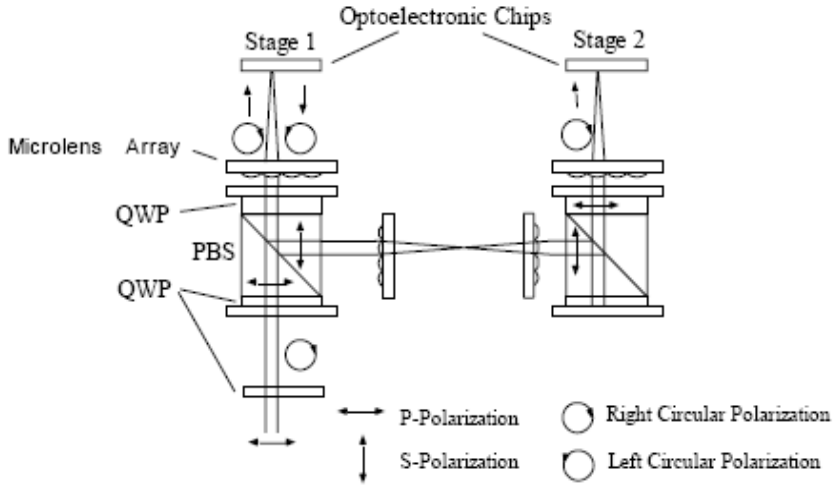
Whilst some effort has been spent on the analysis on tolerancing of the optomechanical aspects of optical interconnects [5],[6] and [7], little information and literature is

available on the tolerancing of other aspects. In particular, polarisation losses in optical interconnects have rarely drawn much attention, [8],[9]. Reference [8] uses a Monte-Carlo analysis for modelling polarisation losses caused by rotational misalignment in a free space optical interconnect system based on a cascade of PBS/QWP assemblies Figure 4.18.a. This work concludes that very restrictive tolerances (1%) are needed in order to achieve a polarisation efficiency of 95%. The 1% tolerances imply that the QWP can not exceed a rotational misalignment higher than 6°, and for the PBS cube, which polarisation efficiency strongly depends on the angle of the incident radiation [10], the rotational misalignment can not exceed 5°.

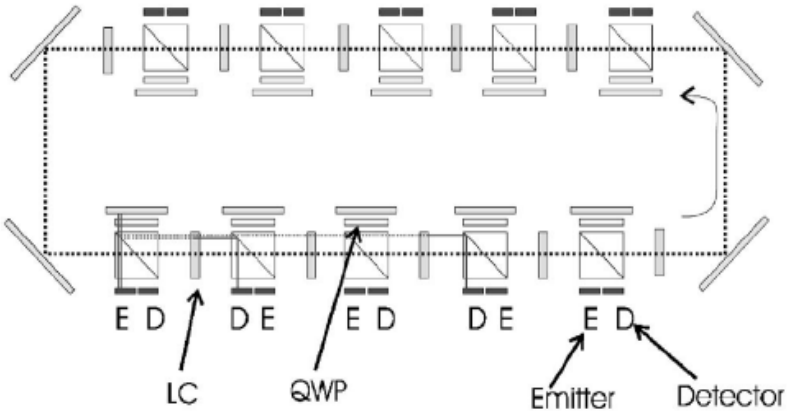
Reference [9] proposes a Monte-Carlo analysis for modelling polarisation losses caused by rotational misalignment of a particular architecture of the OH. The architecture, Figure 4.18.b, is based on a cascade of QWP/LC/PBS and the analysis concludes that the polarisation loss is relative to Malus' Law, which means that a polarisation efficiency of 95% for one optical stage is achieved when the rotational misalignment of the QWP, LC and PBS do not exceed 8°. This simulation also shows that for one optical stage there are several outliers with large deviations from the angular mean that have high polarisation efficiencies due to a combination of angles that have moved in such a way that their relative misalignment is low. However, this advantage is lost when more optical stages are simulated. In order to achieve less than 2dB losses through 15 optical stages the tolerances for rotational misalignment are reduced to 2° for each optical component.

The question, now, is to explain the difference between the systems described in [8] and [9] and the one proposed here. It can be distinguished that there are three main differences: The first one is that for the systems simulated in [8] and [9] one stage is achieved using more optical components than in the system proposed here. In [8] the optical stage is achieved using two QWPs and one PBS. In [9] there is one QWP, one PBS and one LC. On the other hand, in this thesis just one PBS and one LC are used. Therefore, there are fewer components that contribute to the rotational misalignment.
The second difference is that in this system, a WGP is used in place of a traditional PBS cube. It has been analysed previously that the typical performance specifications of the PBS cube are Tp =99% Ts=4% Rp=0.5% Rs=96%. For the WGP the typical performance specifications are Tp =90% Ts=0.13% Rp=0.5% Rs=90%.

As seen, the WGP suffers from more attenuation than the PBS cube. This is one of the reasons for a transmission per stage of only 72.24%. On the other hand, the polarisation leakage of the WGP is less than the PBS cube. Therefore, the polarisation efficiency is greater. Another important advantage of the WGP over the PBS cube is that its performance is not affected by rotational misalignment [11].



a)



b)

Figure 4.18. Architectures used to analysed polarisation losses in FSOI systems.a) Architecture based on cascade of PBS/QWP [8] and b) Architecture based on cascade of QWP/LC/PBS [9].

The third and last difference is the use of good quality 90° TNLCs. Following this, it will be explained how the characteristics of the TNLC can affect its tolerances to rotational misalignment. In order to do this, the transmission properties of a general TNLC presented in [12] are described.

Referring to Figure 4.19, the transmission of a beam of polarised light is investigated through a general TNLC and placed between two polarisers. According to Figure 4.19, the input and output polarisation states, as determined by the orientation angles of the polariser transmission axes, are given by:-

$$\begin{pmatrix} V_x \\ V_y \end{pmatrix} = \begin{pmatrix} \cos\phi_{ent} \\ \sin\phi_{ent} \end{pmatrix}, \qquad \begin{pmatrix} V_x' \\ V_y' \end{pmatrix} = \begin{pmatrix} \cos\phi_{exit} \\ \sin\phi_{exit} \end{pmatrix} \qquad \text{Equation 4.6}$$

Where Φ_{ent}, Φ_{exit} are the angles of the plane of polarisation of the input and output beams respectively.

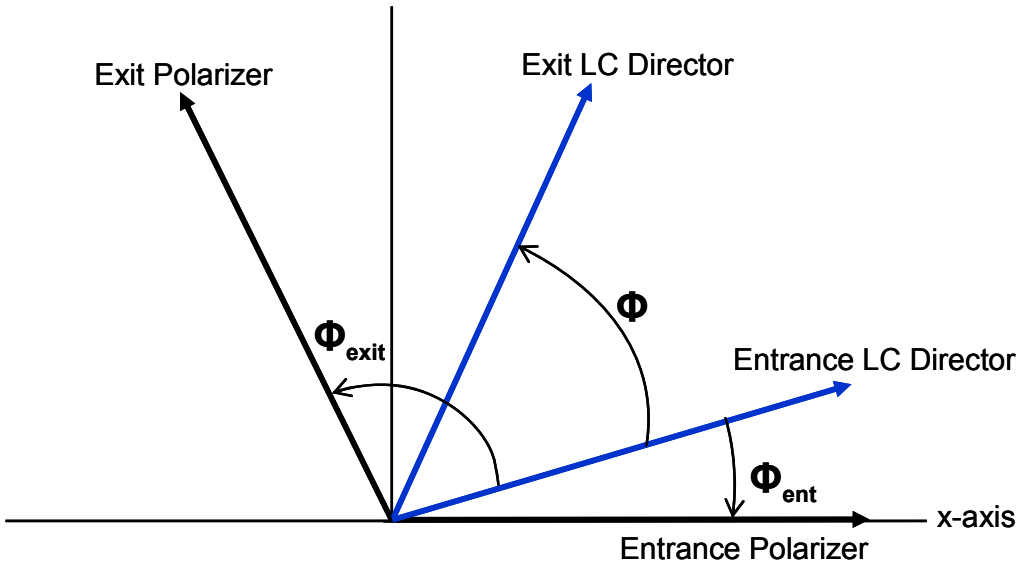


Figure 4.19. Schematic drawing showing the orientation of the polariser axes, LC director of a general TNLC display in the xy plane. All angles are measured from the Entrance LC Director axis.

The intensity transmission of the system is given by, according to Jones matrix method

$$I = \left| V'^{*} \cdot M \cdot V \right|^2 \qquad \text{Equation 4.7}$$

Where V and V' are the input and output Jones vectors respectively. Here, we assume an incident beam of polarised light. M is the matrix that, in x-y coordinates, describes the TNLC assuming that it is used in waveguiding mode [13]. Waveguiding mode occurs when the polarisation vector of the incident beam follows the twist of the liquid crystal director.

$$M = \begin{pmatrix} \cos\phi & -\sin\phi \\ \sin\phi & \cos\phi \end{pmatrix} \begin{pmatrix} \cos \mathrm{X} - i\frac{\Gamma}{2}\frac{\sin \mathrm{X}}{\mathrm{X}} & \phi\frac{\sin \mathrm{X}}{\mathrm{X}} \\ -\phi\frac{\sin \mathrm{X}}{\mathrm{X}} & \cos \mathrm{X} + i\frac{\Gamma}{2}\frac{\sin \mathrm{X}}{\mathrm{X}} \end{pmatrix} \qquad \text{Equation 4.8}$$

Equations 4.9 and 4.10 give the values for X and Γ. ϕ is the absolute change in phase caused by the LC cell - the total twist angle. Γ is a measure of the relative change in phase as a result of the propagation, not the absolute change.

$$\mathrm{X} = \sqrt{\phi^2 + \left(\frac{\Gamma}{2}\right)^2} \qquad \text{Equation 4.9}$$

$$\Gamma = \frac{2\pi}{\lambda}(n_e - n_o)d \qquad \text{Equation 4.10}$$

λ is the wavelength of the polarised light used. (n_e- n_o) is the value of the birefringence and d is the thickness of the LC cell.

Now that all the parameters of Equation 4.7 have been defined, the transmission, I, can now be obtained which after few steps of matrix multiplication shows:-

$$I = \cos^2(\alpha - \beta) - \sin^2 \mathrm{X} \sin 2\beta \sin 2\alpha + \frac{\phi}{2\mathrm{X}} \sin 2\mathrm{X} \sin 2(\alpha - \beta) - \phi^2 \frac{\sin^2 \mathrm{X}}{\mathrm{X}} \cos 2\alpha \cos 2\beta \qquad \text{Equation 4.11}$$

Where

$\alpha = \Phi_{ent}$

$\beta = \Phi_{exit} - \Phi$

Equation 4.11 gives us a general expression for the transmission of polarised light that passes through a TNLC which is arbitrarily oriented at the Off state and placed between polarisers that are also arbitrarily oriented.

However, this work is interested in the particular case where a 90° TNLC is arbitrarily placed between polarisers whose relative positions are perpendicular or parallel. This configuration is similar to the experiment carried out in the previous section, LC Characterisation under Rotational Displacement. Therefore, for this particular case;

$\phi = 90°$

$\Phi_{ent} - \Phi_{exit} = 90°$ when polarisers are perpendicular

$\Phi_{ent} - \Phi_{exit} = 0°$ when polarisers are parallel.

Substituting these values in Equation 4.11 and for Γ = 4.78, given by the LC supplier, two values for the transmission, T, are obtained and plotted in Figure 4.20.

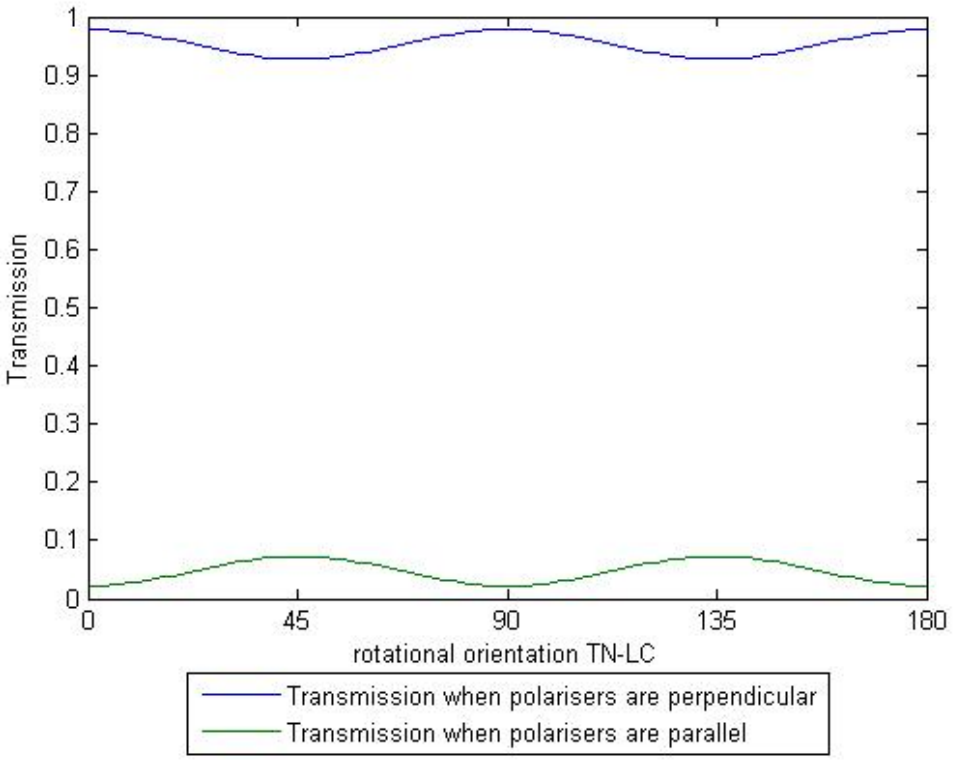


Figure 4.20. Two different values for the transmission of a polarised light after going through a 90° TNLC, Γ = 4.78, arbitrarily oriented and placed between polarises in crossed and parallel configuration. It can be seen that both transmissions remain relatively constant for different rotational orientations of the LC.

The high transmission value corresponds to the case where the two polarisers are placed perpendicular to each other. As the LC is Off the polarised light is supposed to twist 90° and a high transmission is expected when polarisers are crossed. The low transmission value corresponds to the case where the two polarisers are parallel and therefore a minimum of transmission is obtained.

It can be observed that both transmission values keep relatively constant when the LC is rotated. These results agree with the experimental results obtained in the previous section and explain the wide range in the rotational misalignment tolerances of the TNLC. However, it is worth noting that this tolerance strongly depends on both the phase birefringence (n_e- n_o) and the twist angle ϕ, [14]. This would also explain also

why the transmittance of the 45° TNLC used in chapter 3 is more sensitive to rotational misalignment orientation.

4.4 Characterisation of the Three Stage System

After characterising one optical stage, in this section we are going to analyse a cascade of three stages (LC/PBS assembly) of the OH.

RP technology will be used once again for implementing the optomechanical system suitable for studying the reconfigurable characteristics of the free space optical channel. Additionally, how the limited contrast ratio of the optical components can affect the attenuation of the optical signal and the crosstalk caused by misdirected signals will be reported. Different techniques will also be proposed in order to increase the optical modulation amplitude (OMA) of the system.

Figure 4.21 shows the scheme of the optical system where a polarised optical signal is routed through the OH. Then, selecting the appropriate LCs, the optical signal can be routed to any of the three outputs

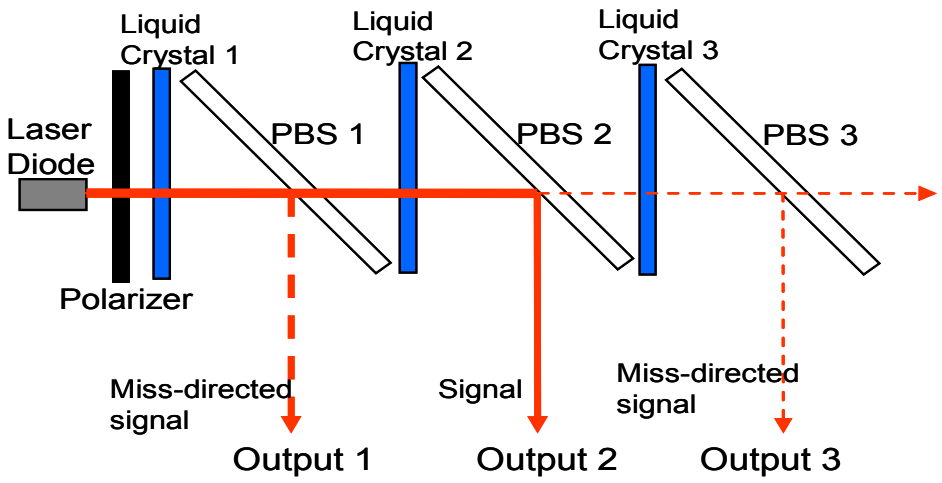


Figure 4.21. Experimental design of a cascade of three stages (LC/PBS assembly) of the Optical Highway.

Figure 4.21 shows also the effect of residual polarisation at the optical surfaces of the PBSs resulting in misdirected signals being routed to the wrong output causing a source of noise.

In reference [3] it is suggested that rather than aberration, the fact that the misdirected signal accidentally routes from a node to the nearest neighbour is the main factor which limits the size of the network. For this reason, an experiment was proposed where the problem of the misdirected signal is isolated and studied independently from other sources such as aberration and crosstalk caused by misalignment and high spatial bandwidth (number of physical layers). Only one optical channel will be routed through the system and ED of the optical signal and the misdirected signal will be analyzed at each output.

4.4.1 Design of the Mechanical Structure using Rapid Prototyping Technology

A mechanical structure has been built for this particular experiment to hold four different optical components, the transmissive 90° TNLC from Excel Display, WGP, an AlGaInP Laser Diode 3mW CW used as a source with its collimator, and polarisers.
In chapter 3, a mechanical structure was designed also using the same technique in order to hold different optical components. Three structures were designed to hold the LD modules, the WGPs and the LCs. The use of 45º TNLC required the design of a structure with a mobile part in order to align two 45º LCs. The acquisition of new 90° TNLCs allows the design of the structure to reduce in size. Additionally, In order to achieve better alignment of the optical components only one block has been designed where the optical components that constitute the three stage system can be slotted.

Figure 4.22 shows the design using the CAD software tool Solidedge17. The structure is made of three different parts: one that holds the collimators where the LD is placed. The structure has been designed to hold a maximum of two LDs and their collimators. Another structure has been designed to hold the PBS plates. The third structure has been designed in order to slot all the optical components necessary for constituting the three stage system.

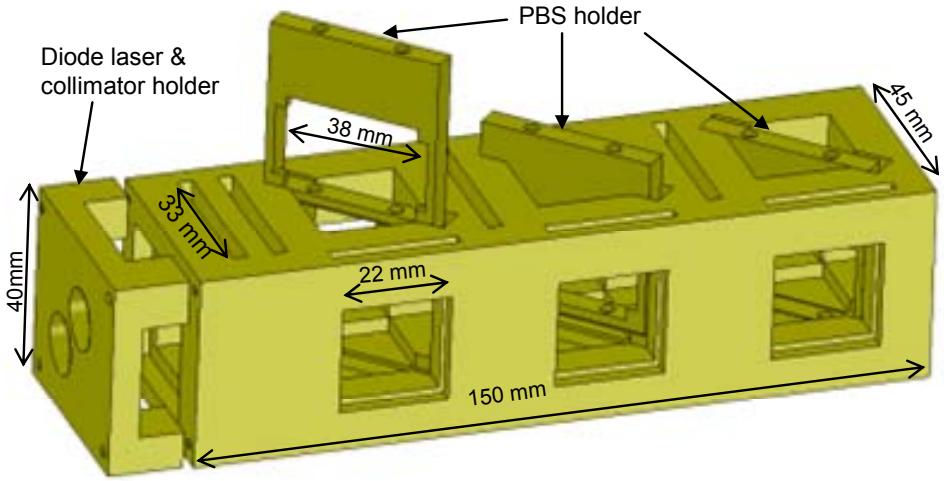


Figure 4.22. Design using Solidedge17 CAD software of the mechanical structure for supporting three optical stages of the OH.

The dimension of the structure (150mm x 40mm x 45mm) is half the size of the previous model and is designed to support more optical components such as input polariser at the entry of the system and out polarisers at each output of the system. The most critical point of the design was the PBS holder since the minimum active area of the PBS had to be taken up for attaching it to the frame. The solution was to add small corners (0.89% of the active area) to the PBS holder and use screws for fixing the edges of the PBS to the frame.

Using the RP machine from the Mechanical Engineering department at Heriot-Watt University the model was made in one hour.

Figure 4.23 shows a picture of the mechanical structure and all the optical components used for this experiment. All the optical components were slotted and removed easily from the top of the structure thanks to tolerances of 0.5 mm which the RP machine achieved without problem.

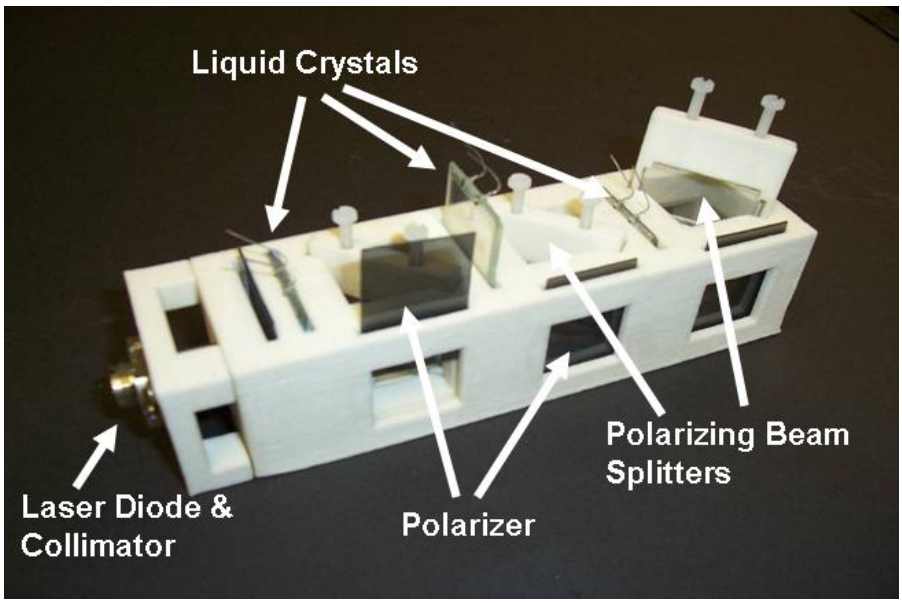


Figure 4.23. Optomechanical structure built using rapid prototyping techniques.

4.4.2 Experimental Setup

Figure 4.24 shows the experimental setup carried out where the LD used was controlled by the Tektronix Stimulus System, the three LCs are controlled by a Digital Signal Processor (DSP) and a custom made PCB regulates the amplified voltage that drives them. The optical signal is detected using a 10MHz amplified silicon detector which is connected to the scope. Four power supplies are necessary for powering all the components.

In previous sections, the optimisation of the optical components that are used for this experiment have been carried out. The results are summarised here and used for setting up this experiment.

The Tektronix Programmable Stimulus System is configured for generating 50 Kb/s Non-Return-to-Zero (NRZ) data stream with rise and fall times lower than 20ps. The amplitude of the digital signal is 400mV and the offset 2.5 V. The LCs are set at 8.5 V and the optical signal is pointed to the centre of the LCs where it has previously been seen that the contrast ratio is higher.

Finally, the LC was placed in a stable position with the connectors on the top and its wider edge resting on the mechanical structure. Although, for this configuration the

entrance of the LC director is oriented at a 45° horizontal position, it has been proven that the LC continuous the twisting of the polarised light as desired.

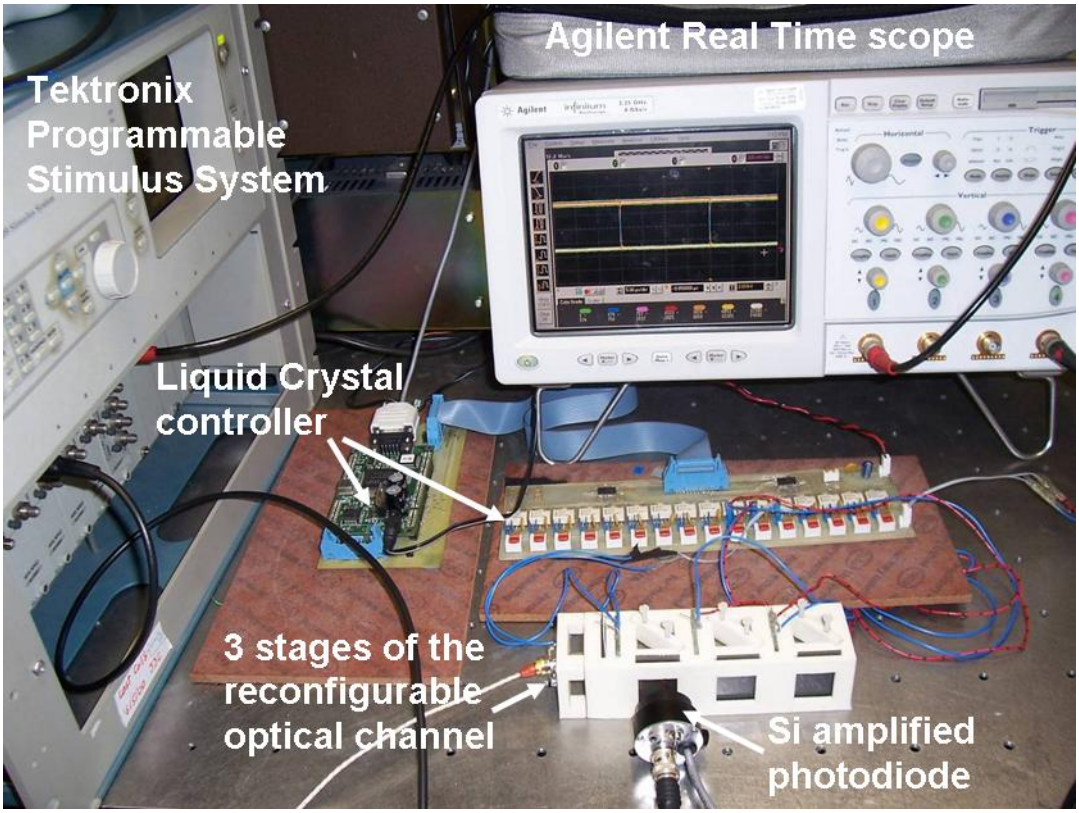


Figure 4.24. Se-up of experiment carried out in order to characterise the 3 optical stage structure.

4.4.3 Three Stage System Characterisation

This section studies the attenuation of the optical signal and the crosstalk at each output caused by misdirected signals. In order to analyse the optical signals, two different EDs at each output have been obtained: one when the signal is directed to this output, and the other when the signal is directed to any other output but a misdirected signal is routed into the output under testing.

Figure 4.25 shows the ED at the three outputs of the system. The On and Off states of the LC are represented by the scalar 1 and 0 respectively. In this demonstrator three LCs have been used. Therefore, a vector of three elements determines their states. The vector [0,0,0] means that all the LCs are off and the signal is routed to the first output

R1. When the LCs are selected [1,0,0] and [1,1,0] the optical signal is routed to the outputs R2 and R3 respectively.

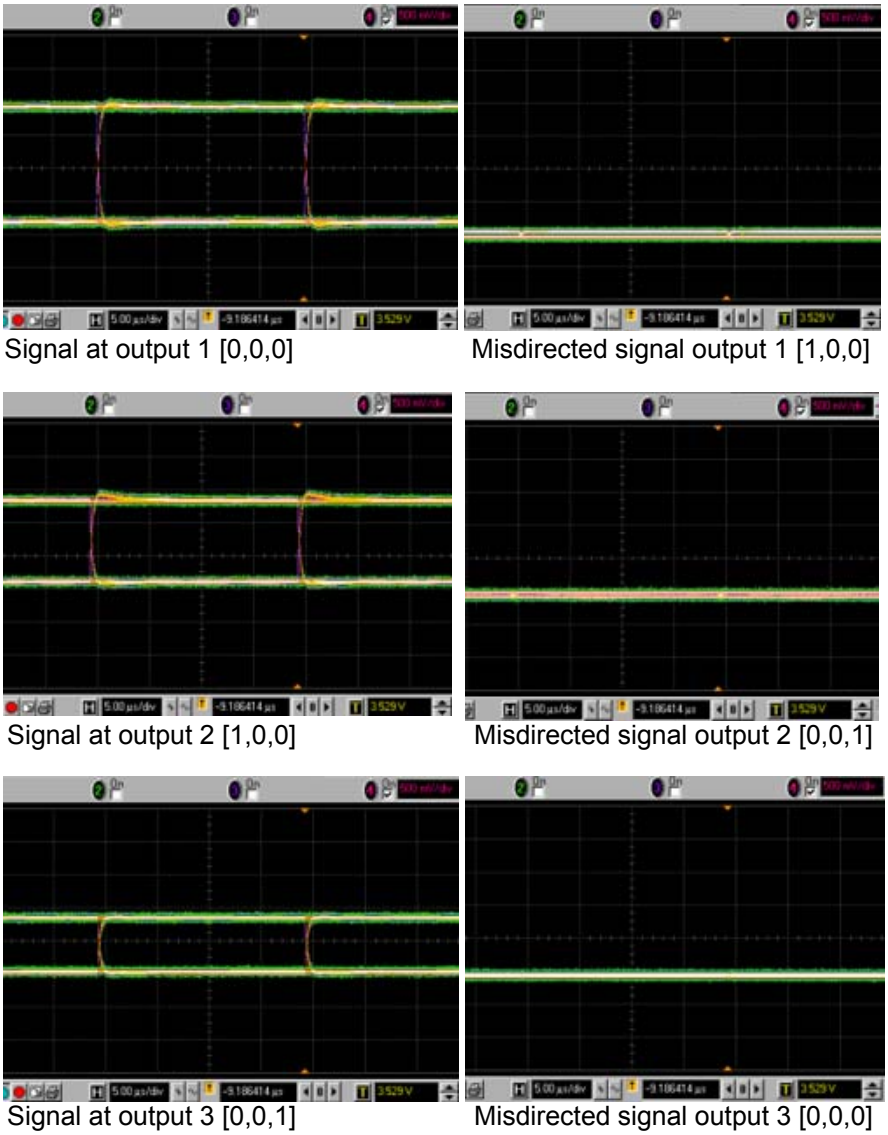


Figure 4.25. Eye Diagrams at the three outputs of the optomechanical system. The three dimension vector indicates the state, On or Off, of each one of the three LCs.

Table 4.1 summarises the ED parameters obtained when the optical signal is routed into each output. As can be seen from the table the eye height decreases by 1.4 dB per stage. As a result, the quality factor, Q, also decreases. However, after three stages the value of Q is still far from the value of 6 which is the minimum necessary to achieve a BER of 10^{-9} [15]. On the other hand, the signal level after three stages is high enough not to degenerate the eye width and the Jitter RMS parameters.

	Output 1	Output 2	Output 3
Eye height (mV)	1655	1146	751
Eye width (us)	20	20	20
Q-factor	62.07	44.09	35.74
Jitter RMS(ns)	0	0	0

Table 4.1. Eye Diagram parameters when no clean up polarisers are used. These values are obtained at each output when the optical signal is directed to each output.

As can be observed in Figure 4.25, no ED and, therefore, no eye parameters can be obtained for the misdirected signals at each output. This means that the misdirected signals detected are too weak when compared with the desired signal that was routed to that output.

As a consequence of these results, the misdirected signals at each output can be considered as a CW value when it is compared with the directed signal detected where two clear values (the logic 0 and logic 1) can be distinguished.

Secondly, the value of the misdirected signal at each output is inferior to the value, at each output, of the logic 0 of the directed signal.

These conclusions prove that, as result of the optimisation of each component, the system worked as required. A more detailed analysis has been proven in order to compare the value of the misdirected signal at any output with the value of the digital 0 at any output. It has also been analysed how the optical signal is affected in terms of polarisation losses and attenuation when the signal passes through the optical stages.

Figure 4.26 shows the optical power value of the logic 1, P1, logic 0, P0, and the crosstalk, $P_{crosstalk}$, at each output. As seen, $P_{crosstalk}$ at each output is lower than P0 at the same output. In fact, the extinction ratio of the optical signal defined as $r_e = P1/P0=8.8$ at the first output is lower than the extinction ratio of the misdirected signal defined as $r_{crosstalk}=P1/P_{crosstalk}= 12.7$ at the first output. From Figure 4.26 we can see that the optical quality of the signals in the three stage system is determined by Optical Modulation Amplitude of the system defined as OMA_{system} = P1 min – P0 max, where

P1 min is the value of P1 at the third output and P0 max is the value of P0 at first output.

We can conclude that, in spite of using off-the-shelf LCs after correct optimisation and without the need of precise systems of alignment, the limiting factor in the optical budget of the OH system is not crosstalk, but P0.

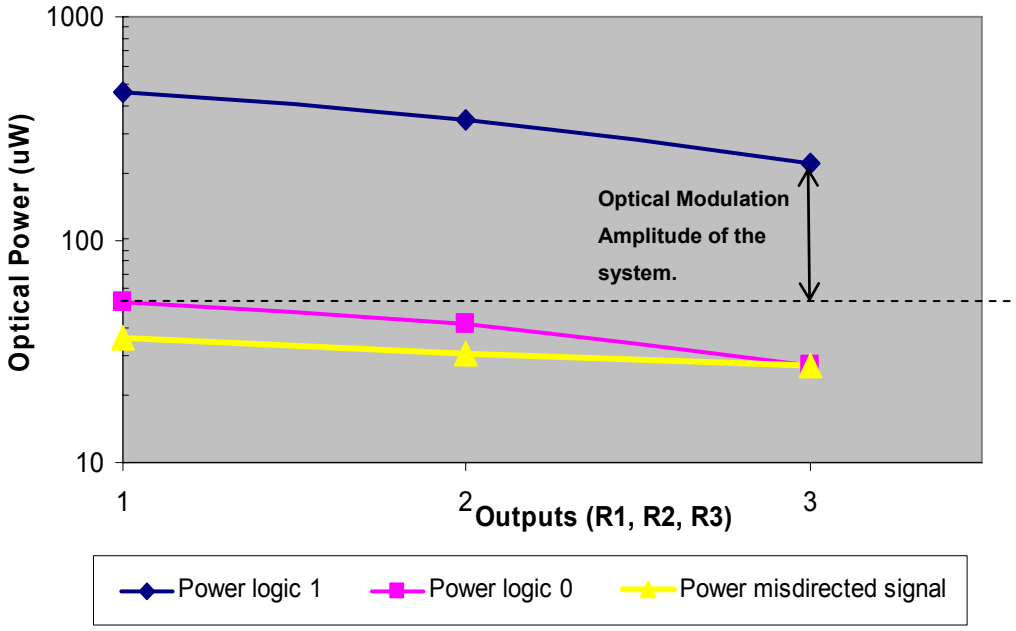


Figure 4.26. Characterisation of three stages (assemblies PBS/LC). Values in uW of the logic 1, logic 0 and the crosstalk.

Since $r_e < r_{crosstalk}$ the Bit Error Rate (BER) of the optical signal can be analysed without the need of having to take into account the influence of crosstalk. BER is determined entirely by the optical signal-to-noise ratio, which is commonly called the Q-factor which was defined previously in Equation 4.3 as $Q = \frac{OMA}{\sigma_1 + \sigma_0}\left(\frac{r_e - 1}{r_e + 1}\right)$.

The Q-factor has been defined as the optical modulation amplitude OMA=P1-P0, divided by the sum of the rms noise on the high and low optical levels. The term $(1-r_e)/(1+r_e)$, known as power penalty is due to the difference between P0 and 0.

In order to minimise the power penalty r_e is required to be as high as possible. However, very high extinction ratios cause many problems for the transmitter such as turn-on delay and relaxation oscillation. In general, the practical limit on r_e for a transmitter is in the range of 10 to 12 [1] which corresponds to power penalties of 1.22 and 1.18 respectively.

Before continuing, it is worth noting that if P0 is assumed to be 0 or low enough to become $r_e > r_{crosstalk}$, then $P_{crosstalk}$ can be considered as the main source of noise. In this situation Equation 4.3 is simplified as follows:

$$Q = \frac{OMA}{\sigma_1 + \sigma_0}\left(\frac{r_e - 1}{r_e + 1}\right) \quad \Rightarrow \quad Q = \frac{P_1}{P_{crosstalk}}$$

At the same time, this simplified expression is equivalent to Equation 3.1 obtained in the previous chapter as CR (dB) = OSNR (dB) + N x A (dB), where OSNR (dB) = log(Q), N x A (dB) = -log (P_1) and CR (dB) = -log ($P_{crosstalk}$). Therefore, we can conclude that Chapter 3 studies the case where $r_e > r_{crosstalk}$ and in this chapter it is discovered that the case $r_e < r_{crosstalk}$ must also be analysed. In conjunction with this a new expression to determine the maximum number of stages that the system can support under this condition must also be found.

Returning to Equation 4.3, it is important to note that when it is applied to this particular system where there are different outputs with different values of P0 and P1, it is necessary to consider the worst case scenario. In this case the OMA_{system} and r_e of the system are determined using the minimum value of P1 obtained at the last stage of the system, and the maximum value of P0, which occurs at the first output. Based on Equation 4.3 (assuming that the noise is a fixed quantity and $r_e < r_{crosstalk}$) it is clear that the system BER performance is directly controlled by the OMA. Therefore, in order to optimise BER performance, the OMA should be as large as possible.

From the optical receiver point of view, there is an upper limit on the optical power that can be received called the overload level. When the power exceeds this level, saturation effects degrade the performance.

Equation 4.3 can be used to work out the maximum number of stages the optical signal can pass through in the system. In order to do this, P1 minimum can be expressed in terms of P1 maximum which is equal to P1 at the first output of the system by using the relationship; $P1\min = \alpha^N \times P1\max$, where α is the attenuation per stage -1.40 dB or 0.72, and N the maximum number of stages. Then, the maximum number of stages, N, can be obtained by substituting in Equation 4.3 the value of P1 min in the OMA and r_e:

$$N = \frac{\log\left(\frac{(2P_0 + Q\sigma) + \sqrt{(2P_0 + Q\sigma)^2 + 4(P_0 Q\sigma - P_0^2)}}{2P_1 \text{ max}}\right)}{\log \alpha} \qquad \text{Equation 4.12}$$

In Equation 4.12, the value of Q is fixed to achieve a certain BER. For example, to achieve a BER of 10^{-9}, Q has to be at least 6. The noise $\sigma = \sigma_1 + \sigma_2$ is obtained experimentally and is also assumed to be a fixed value in this experiment, 6 uW.

4.4.4 Increasing the Optical Quality in the System

From the discussion in the previous section it has been concluded that for optimum BER performance the maximum P1 in the system has to be as large as possible while avoiding the overload of the detector. In addition to this, the maximum P0 of the system should be kept as low as possible without becoming so low that either it causes problems with the laser, or becomes lower than $P_{crosstalk}$. In order to achieve these results different techniques have been used:

Table 4.2 summarises the techniques used for increasing the optical quality of the system. The first column represents the values obtained without using any technique. Substituting these values on Equation 4.11, the maximum number of stages the system can support is four.

	Initial condition (4 Optical Stages)	Increase of transmitter power	Use of RZ signal	Use of cleanup polariser and increase of transmitter power (8 Optical Stages)
P1 max	457 uW	1923 uW	1998 uW	1826 uW
P0 max	52 uW	306 uW	65 uW	65 uW
$P_{crosstalk}$	36 uW	109 uW	109 uW	37 uW

Table 4.2. Techniques used for increasing the optical budget of the system.The table shows the cumulative effects of the different techniques that allow increasing the maximum number of optical stages from 4 to 8.

Figure 4.27 helps to understand graphically how the techniques proposed increase the optical quality of the system.

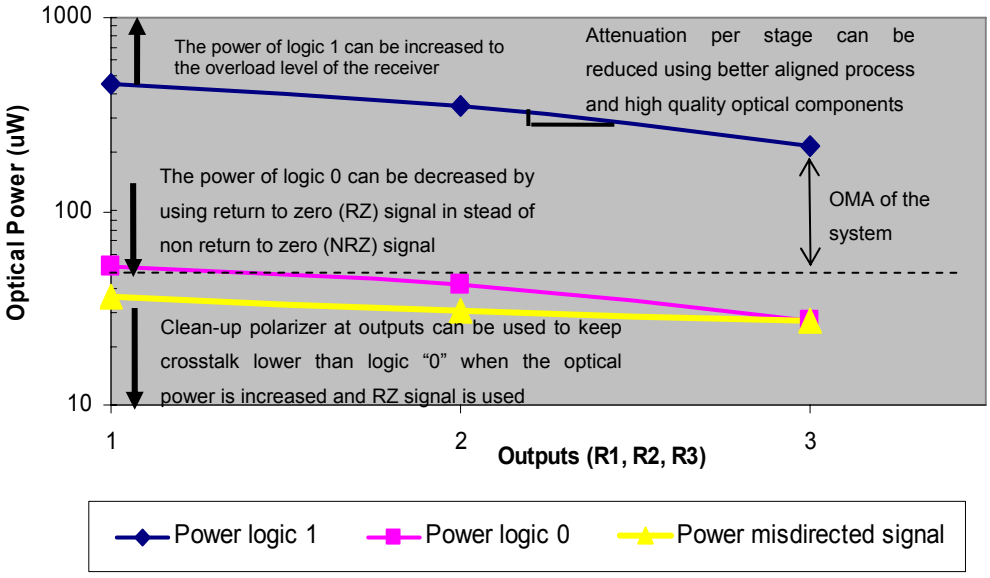


Figure 4.27. Characterisation of three PBS/LC assembly stages.

In order to increase the number of stages, the first technique is to increase the power of the transmitter to a value where the maximum P1 is close to the overload level of the detector. By doing this, the P1 max of the system has increased by a factor of 4.20, from 457 µW to 1923 µW. On the other hand, P min has increased by a factor of 5.88, from 52 µW to 306 µW. Although the maximum $P_{crosstalk}$ has also increased from 36 µW to 109 µW, this is lower than the P0 max, and therefore the system is still under conditions for applying Equation 4.3. Due to the high value of P0 max, the maximum number of stages, N, has not improved and is still four. Therefore, in order to decrease the value of P0 max a second technique has been used which consists in using Return-to-Zero (RZ) code signal instead of NRZ. The difference between these codes is that while NRZ encodes the logic 1 by sending a constant light intensity for the entire bit period, RZ code sends a pulse shorter than the bit period. Due to its basic pulse nature, an RZ signal has many more transitions than a NRZ signal, and less direct current (DC) content. Although RZ signals are more difficult to produce and require more signal bandwidth, these are being used for high bit rates (40 Gb/s) because they cause less chromatic and polarisation mode dispersion than the NRZ signal. In our experiment the use of the RZ signal causes a decrease in the power of the logic 0 from 306 µW to 65 µW and keeps the value of the logic 1 practically at the same value than before. However, the $P_{crosstalk}$ has not decreased and becomes higher than P0 max. Therefore, Equation 4.12 cannot be used to determine the value of N and a third technique consisting in the utilisation of a

cleanup polariser at each output of the system is used. This technique proposed in the previous chapter improves the $r_{crosstalk}$= P1/ $P_{crosstalk}$ of the system. Although, the use of cleanup polarisers decreases P1 max, this value can be raised again to the overload level of the detector by increasing the power of the laser. As can be seen in Table 2, the combination of the three techniques used has increased the value of P1 minimum to 1826 μW, while the P0 maximum and $P_{crosstalk}$ have been kept practically to the same values as in the initial conditions. Consequently, the maximum number of stages (N) the optical signal can go through this system has increased from four to eight. Equation 4.12 also shows that the attenuation per stage is a key factor and as it was suggested in chapter 3, high quality optical component can improve significantly the results. For example, by decreasing the attenuation per stage just 7.5%, from 0.74 to 0.80 the maximum number of stages the optical signal can go through in the system increases to eleven.

4.5 Conclusion

In this chapter, new components have been used and characterised in order to complement the results obtained in chapter 3. Special attention has been focused on the new 90° TNLC which, through characterisation experiments, have revealed its inhomogeneous contrast ratio properties through its 30mm x 30mm surface. On the other hand, low contrast ratio dependence has been obtained for rotational misalignment. This important property has been proved theoretically to be general behaviour for this type of LC, and supposes an important advantage over other FSOI systems based on polarising beam routing systems that use components such as QWP for routing the signal which suffer far higher contrast ratio dependence to rotational misalignment.

Finally, a new design using RP has been successfully employed to implement three stages of the OH. The ED technique has been employed for analysing the reconfigurability properties of the system and it has shown that the crosstalk caused by misdirected signal is not a limiting factor of the optical budget. As a consequence, it has been possible to use simple techniques for increasing the OMA and the Extinction Ratio (r_e) of the system in order to increase the number of optical stages that an optical signal can pass through the system. These techniques consist in increasing the optical power of the transmitter to the overload level of the detector, using RZ modulation code instead of NRZ code and placing a cleanup polariser at each output of the system.

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Chapter 5

Design of the Optical Highway at Different Levels

5.1 Introduction

The previous chapters examined different components and techniques useful for implementing the OH, and also the efficiency of one optical channel of the OH in terms of reconfigurability and tolerance to misalignment. The scalability of the OH in terms of attenuation and crosstalk has been analysed both theoretically and experimentally. This chapter will examine the design of the OH at different levels. Figure 5.1 summarises the four physical levels: the Node level, the Optical Stage level, the OH Architecture level and the Parallel Computer Network level.

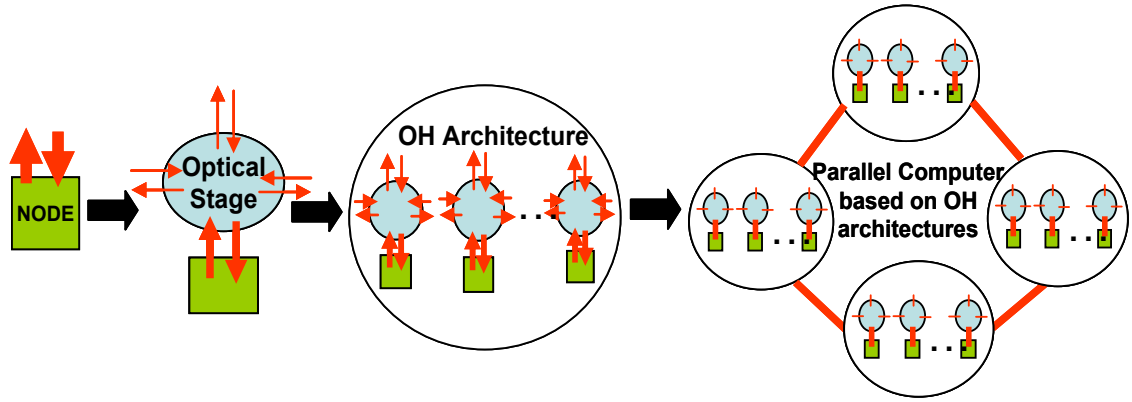


Figure 5.1. Levels of design of the OH: Node, Optical Stage, OH Architecture and Parallel Computer level.

At node level the mapping of emitters and receivers onto the node will be analysed. As we mentioned previously, a node is a general O/E-E/O computational unit available to process information, which could be a processor, memory or simply a recovery point where the weak signal can be regenerated.

At the optical stage level it will be proposed different designs of the basic unit of the OH - the assembly LC/PBS. Properties such as connectivity and complexity will be discussed at this level.

The architectural level defines different ways of assembling optical stages in order to achieve communication between different nodes using a single or low number of hops.

Thus, the importance of establishing the maximum number of stages that the optical signal can pass through in a single hop.

The highest level, the Parallel Computer Network based on OH Architectures, considers the interconnections of OH architectures in order to create large parallel computer systems.

This chapter will focus on the design of the first three levels only, as the Parallel Computer Network level is based on the use of either switching or repeater technology or both together which require future and extra analysis.

5.2 Design of a Node of the Optical Highway

As mentioned in Chapter 2, a node consists of a processing system and a custom optoelectronic interface chip such as an SPA (Figure 5.2) The SPA gathers two different structures: the reconfigurable chip and the optical interface, which includes the emitters (VCSELs) and the receivers (PDs). The reconfigurable chip is an FPGA (Field Programmable Gate Array) and allows any pin of the chip to connect to any emitter or receiver without changing the design of the processing unit. By using the FPGA, any connection pattern can be set on the processing unit and therefore it is possible to specify the node where the signal comes from.

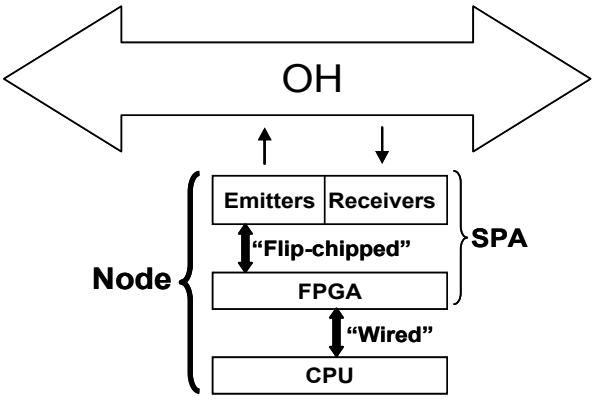


Figure 5.2. Technologies used for the design of a node [1].

5.2.1 Optical Requirements

Before proceeding with the design of the node of the OH, it is convenient to point out some considerations and assumptions about the optical requirements of the system in order to validate the design of the node and also the models presented in the previous chapters.

To summarise, the previous chapters established the maximum number of stages that the signal can pass through in a single hop. It was supposed that one stage of the OH is constituted by the LC/PBS assembly. No other components were considered and, therefore, no other contribution to the attenuation or crosstalk was taken into account. The use of optical relays throughout the system was omitted in the theoretical analysis and avoided in the experiments by using collimators at the input, a low number of channels and a large active area of the LC and PBS. However, it is obvious that when the system is scaled to a large number of channels, a network of lenses is required in order to focus the signal and keep it collimated through the system.

In addition to its original function as a polarisation switcher, the LC is proposed to act as a lens. This idea is based on the development of a new technology known LC-lens [2]. LC-lens technology makes use of the controllable voltage and frequency of the LC for changing the focal length.

Lenses with electronically controllable focal lengths for making variable focus lenses are currently producing considerable interest in both technical and commercial literature. Technologies include electro-wetting [3], [4], acousto-optics [5] and fluid-filled lenses [6].

Therefore, the LC in this system can perform two functions: polarisation twisting of the input beam and focusing of the signal. Since the focal distance is not necessary to be modified in the OH, the fixed focus length can be achieved by simply manipulating the transparent wall substrate containing the LC cell.

However, it is worth mentioning that, for future FSOI applications, the possibility of using voltage and frequency, applies to the LC-lens for controlling both polarisation and focal distance.

The design of the node will be based on the use of a microchannel configuration. In this configuration each channel is relayed by a pair of microlenses (Figure 5.3). The design complexity is low and independent of the number of channels. However, the interconnection distance is limited by diffraction and cascade relay is required for long interconnection distance. The high number of LC-lenses used in this system provides this cascade relay.

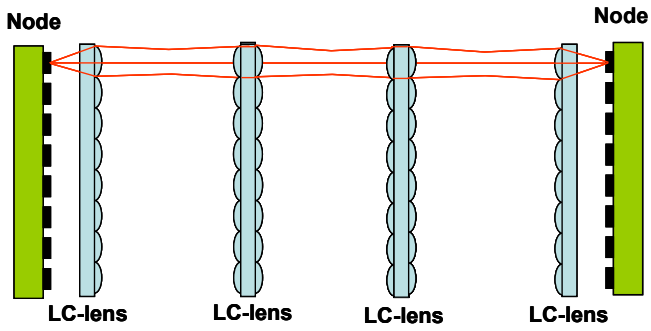


Figure 5.3. The use of LC-lenses as microchannels simplify the design of the node with respect to previous designs [7] where macrochannel configuration was proposed.

One important advantage of the microchannel configuration is that the image of a node has the same orientation as the "object-node" independent of the number of lenses that the signal passes through (Figure 5.4). This offers an advantage over previous designs [7] because each emitter of an object-node has associated the same receiver of an image-node independently of the position of the node, therefore simplifying the mapping problem.

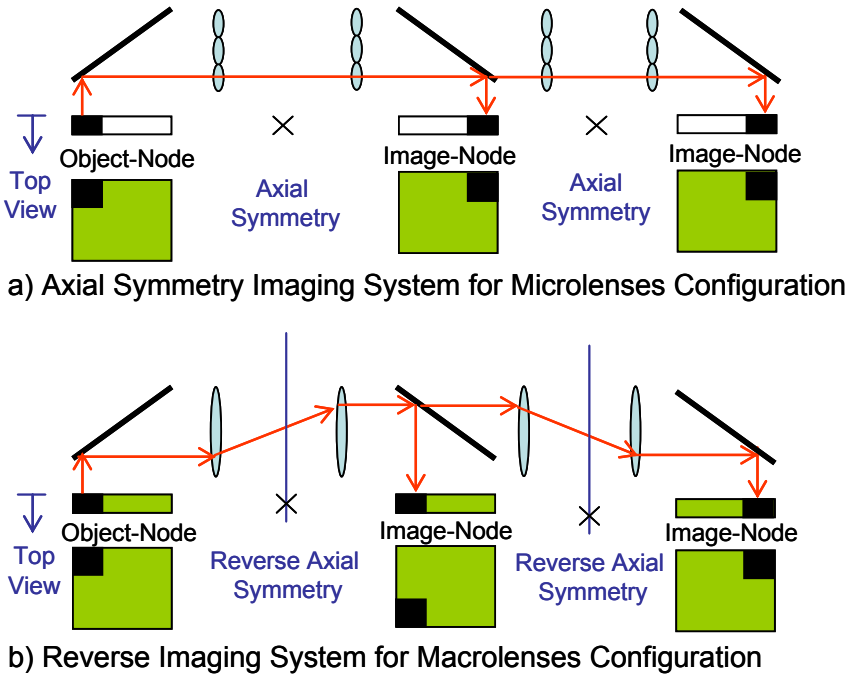


Figure 5.4. Using Microlens Configuration a) each emitter of the object-node has associated the same receiver of an image-node independent of the position of the node. On the other hand, using the Macrolens configuration b) the associated receiver depends on the position of the image-node.

5.2.2 Design Requirements

Apart from the optical requirements, there are other factors that must be considered which are summarised as follows [7];

- *Computing Versatility Requirements*. The main "computing" requirement for the mapping of the nodes is that it must be as versatile as possible in order to implement network topologies which could be totally opposite. For example, the Completely Connected Topology (CCT) uses the largest number of links among all the existing network topologies when the Hypercube Topology (HT) uses fewer numbers.
- *Packaging Requirements*. Two main requirements regarding the use of CMOS technology have been identified. First of all, all the nodes must be the same. This is linked to the cost associated to the design and use of several masks. The more replicable the node is, the cheaper the system will be. Secondly, all the nodes must be square due to the fact that both processing and FPGA systems are also square, and it would be difficult to imagine an optical interface which does not fit the underlay architecture..

- *Node Efficiency*. We refer to node efficiency as the percentage of working structures, i.e. emitters-receivers that can be employed at the same time. The design and mapping of the nodes must take into account the limit case where all the emitters-detectors on a chip are working at the same time.
- *Redundancy* of emitters and receivers mapped on the nodes are used mainly for two reasons. The first is to increase the bandwidth between nodes. Given the reconfigurable characteristics of the OH it is possible to create a bidirectional optical link between two nodes using a variable number of emitters and receivers depending on the bandwidth requirements. The second reason for using redundancy is to avoid the crosstalk caused by misdirected signals. In the OH, several optical signals can potentially be used in the same optical channel for interconnecting different nodes. This is ideal in order to increase the efficiency of the nodes. However, due to crosstalk, the misdirected signals are routed to the same destination-node. Thus, receivers and the processor cannot identify the origin of the signal.

5.2.3 Mapping Emitters and Receivers on the Node

The design of the optical interface must fulfil all the requirements that have been discussed previously.

Regarding the packaging requirements, a square chip with an array of 4x4 optoelectronics I/O will be used. Then the first emitter will be placed in position 1, on the upper left corner (Figure 5.5(a)) and, considering the optical requirements, the system will provide an axially reversed image (mirror symmetry) in position 4 at each output that is allowed by the OH architecture. A second emitter placed next to the first one (position 2) will be imaged in the position 3 and so on. Furthermore, as each link must be bidirectional we have to do the same operation with the emitters of the "Image-Node", Figure 5.5 (b). Therefore, the emitter in position 1 and 2 on the Image-Node, which is now the "Object-Node", will be imaged in the position 3 and 4 of the old Object-Node, which is now Image-Node.

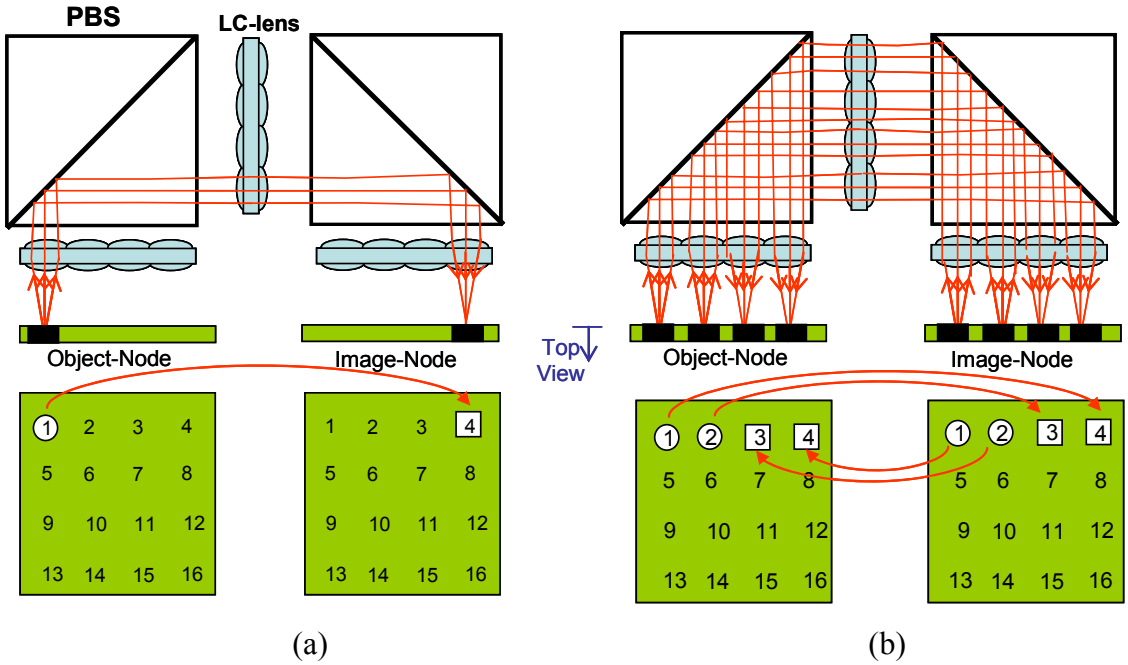


Figure 5.5. Mapping of Nodes.

Figure 5.6 shows two possible designs that we call Simple and Versatile Configurations for the mapping of emitters and receivers into the Object and Image Node allowing bidirectional communication. Both designs fulfil the packaging and versatility requirement since all the nodes can be identical and make imaged emitters meet with physical receivers for different configurations. However, each design has a particular property.

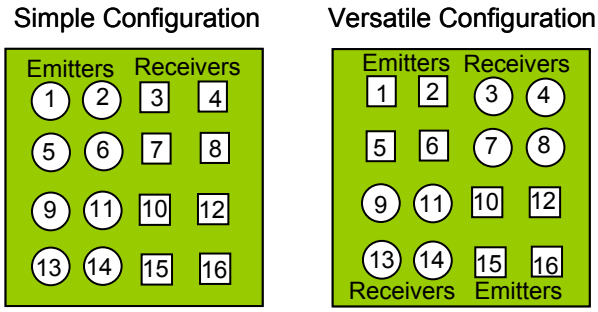


Figure 5.6. Different Node configurations. (a) Shows the Simple Configuration where the emitters and receivers are grouped in two separated parts. (b) Presents the Versatile Configuration where the array of emitters and detectors are both split in two parts and placed diagonally to each other. This configuration allows the use of both microchannel and macrochannel configuration and, as it will be seen in the next section, increases the connectivity of the optical stage.

The Simple Configuration (Figure 5.6 (a)) is the simplest in terms of packaging requirements since the emitters and receivers are separated in just two different groups. This configuration has already been used experimentally and has proven its viability [8]. On the other hand, the Versatile Configuration (Figure 5.6(b)) offers a more versatile design since it can be used with both microlens and macrolens configuration [7] irrespective of the position of the node and, as we will see in the next section, can increase connectivity between nodes. However, the Versatile Configuration implies a higher packing complexity and has not been experimentally implemented yet.

5.3 Design of Optical stage and Optical Highway Architectures

This section will focus on the design and analysis of the Optical Stage level and the OH architecture level. Different designs of the optical stage and the way it is assembled are proposed in order to achieve a particular interconnection network between nodes in a single or low number of hops.

5.3.1 Design Requirements

At this level, as at node level, some design requirements and parameters must be taken into account.

- *Ozaktas' Tree Requirements*. In Chapter 2, we summarised the ideas of Ozaktas [9] in order to design an optoelectronic parallel computer. Ozaktas' Tree concludes that FSOI systems must be used locally and globally for communicating 3D nodes arranged regularly in planes.
- *Low Complexity Requirements*. The complexity of the OH architecture in terms of quantity and variety of the optical components used should be kept as low as possible in order to simplify the packaging of the system, reducing costs and misalignment problems.
- *Heat Dissipation Requirements*. One of the main issues associated with traditional parallel computer systems is the dissipation of heat generated by the processor's units or nodes. Parallel computers based on FSOI systems are not free from this issue. Therefore, heat dissipation must be considered when designing OH architectures.

- *Architectural Efficiency*. This term includes the parameters used to evaluate the performance of the OH such as connectivity, cost, bisection bandwidth, diameter and maximum losses.

5.3.2 Design of the Optical Stage and Optical Highway Architectures

In order to obtain optimal complex architectures based on the OH, it is believed that it is necessary to analyse the simplest FSOI structure, which is the optical stage. In Chapter 2, the importance of an efficient design of the optical stage was already discussed and the LC/PBS assembly was defined, which has been used to carry out the research. Based on the LC/PBS assembly four designs will be proposed which will be compared and analysed.

Unidirectional Optical Stage

Figure 5.7 shows the Unidirectional Optical Stage, based on the original design of the OH [1]. In this structure, the polarised light passes through a PBS to a quarter wave-plate (QWP). On reflection at the mirror, the signal then passes again through the QWP and is reflected from the PBS to the LC, which controls the polarisation of the signal, and then is passed to the left optical stage. This link is unidirectional. In other words it is available to send and receive information in one direction. One important drawback of this design is that it requires four different components which make the structure complex. Another disadvantage of this design is the use of a mirror which blocks part of the path that could be used for the node to communicate with other stages, thereby reducing the efficiency of the architecture.

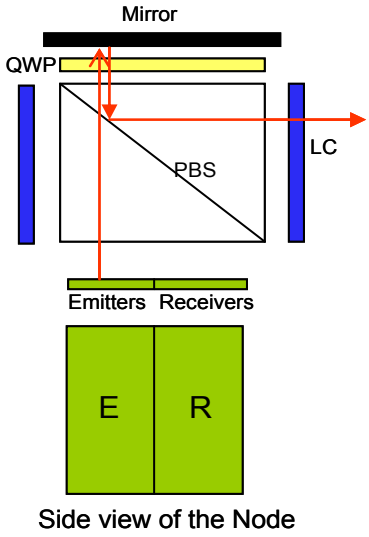


Figure 5.7. Unidirectional Optical Stage and a side view of the Simple Configuration node employed.

However, using this design, simple OH architectures such as the Ring architecture Figure 5.8, can be easily implemented. The ring architecture allows interconnecting nodes in a traditional ring configuration. Each node has been placed outside of the architectures in order to allow adequate heat dissipation and airflow. In fact, the placement of nodes outside of the architecture will be a general criterion for all the designs that will be proposed in this chapter.

It can be observed that the system makes use of the QWP and mirror only at the beginning of the optical link communication in order to route the signal into the OH. Therefore, the optical signal contributes to an extra power loss when compared to the use of a LC/PBS assembly. The Ring Architecture uses the Simple Configuration for the mapping of emitters-receivers into the node. However, due to the use of the mirror the orientation of the mapped emitter-receiver depends on the position of the node on the architecture. Therefore the node, i, can communicates only with half of the nodes of the architecture, $i + (2n-1)$ with $n \in [1, N]$, N being the number of stages. Therefore, the efficiency of this architecture in terms of connectivity is low.

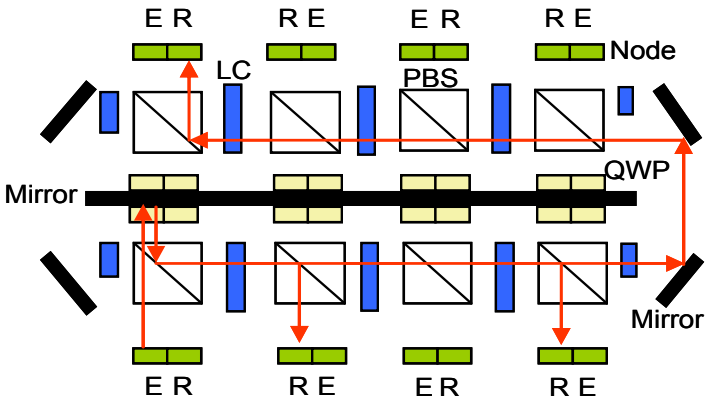


Figure 5.8. The Ring Architecture based on the Unidirectional Optical Stage.

The Ring Architecture has been proposed in reference [10] for mapping matrix-vector multiplication algorithms [11]. Parallel algorithms involving matrices and vectors are applied in several numerical and non-numerical contexts and the Ring Architecture was proven to be more efficient in terms of communication costs rather than traditional architectures based on electronic interconnects.

Bidirectional Optical Stage

The second design proposed will be named Bidirectional Optical Stage (Figure 5.9). This has already been introduced in Chapter 2 as a simpler and more efficient design than the Unidirectional Optical Stage since it is available to transmit and receive optical signals in and from two different directions. In addition to this, the Bidirectional Stage does not use a QWP or a mirror and, therefore the complexity and power losses are lower. Observe also that the node uses a Simple Configuration for mapping the emitters and detectors. Note that there is no need for placing LCs at the input of the detectors of the node since the optical signal at this point can only be routed in towards the detectors. Therefore, there is no need for controlling the polarisation of the light.

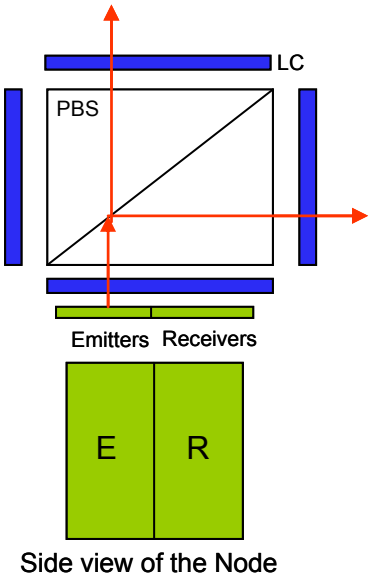
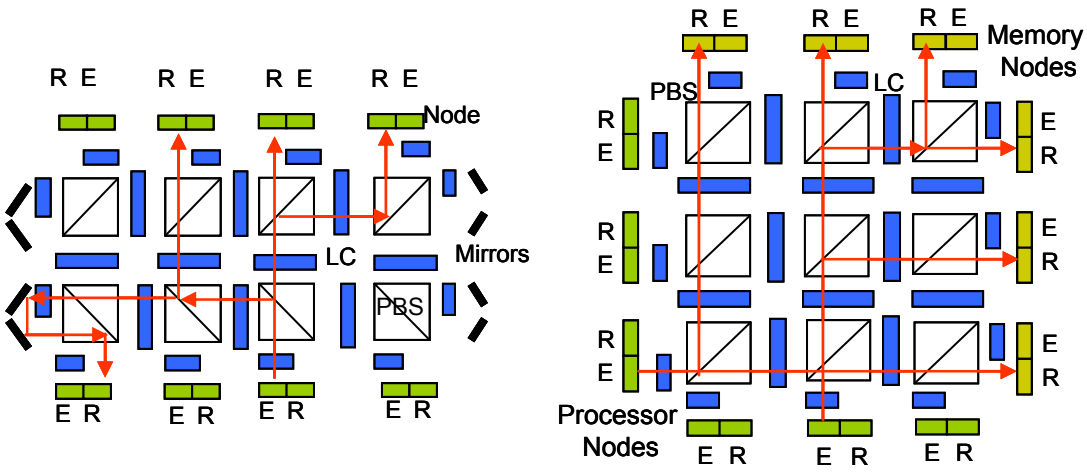


Figure 5.9. Bidirectional Optical Stage. This design requires the use of Simple nodes shown in the side view.

Based on the Bidirectional Optical Stage, two architectures, namely the Cut-Through Ring and the Matrix, have been proposed in Figure 5.10. The Cut-Through Ring is a more efficient architecture in terms of connectivity than the Ring architecture. As we can see in Figure 5.10 (a) from the simplified ray tracing, any node placed on one side of the architecture can easily communicate with any other node of the other side of the architecture using a low number of optical stages. Additionally, the mirrors placed at the laterals of the architecture allow the communication between nodes on the same side. These mirrors can be replaced by WGPs allowing also communication with the exterior.

Figure 5.10 (b) shows the Matrix Architecture which consists of a dense matrix of optical stages that allows the interconnection of nodes using a high number of different routes. This makes this architecture ideal for implementing non-blocking topologies.
The symmetry of this design allows interconnecting half of the nodes with the other half using a single hop and all nodes in just two hops.
Figure 5.10 (b) also shows a possible application where half of the nodes are used as processor units and the other half memory units. Any processor will be able to communicate in a single hop with any memory and vice versa.



(a) Cut-Through Ring Architecture *(b) Matrix Architecture.*

Figure 5.10. Architectures based on the Bidirectional Optical Stage.

Three-Directional Optical Stage

The next optical stage presented is the Three-Directional Optical Stage, Figure 5.11. This is a novel design where as its name indicates, allows the transmission and reception of optical signals in and from three different directions. The increment of directions is achieved by placing two PBSs in front of the node, one on top of another and crossed over each other. This design requires the use of the Versatile Configuration design for mapping the I/Os on the node and therefore the complexity of this optical stage is higher than in previous designs. On the other hand, the efficiency in terms of connectivity is higher.

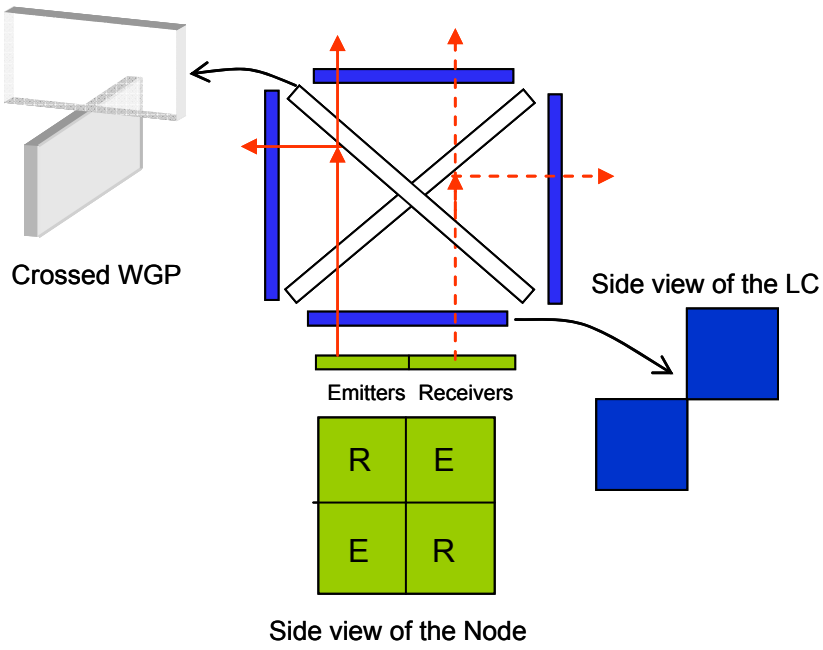


Figure 5.11. Three-Directional Optical Stage. The design requires the use of Versatile Configuration nodes, Implementation can be achieved by PBS cubes or WGP. However, WGP can offer advantages in term of connectivity (Chapter 3) over PBS cubes.

Figure 5.12 shows the Optimised Cut-Through Ring (OCTR) architecture. As its name indicates, the OCTR is an optimised design in terms of power loss of the Cut-Through Ring presented previously. Both architectures can support the same routing operations. However, the OCTR only requires half of the optical stages than the Cut-Through Ring architecture which increases its compactness and also its complexity. On the other hand, the bisection bandwidth is lower.

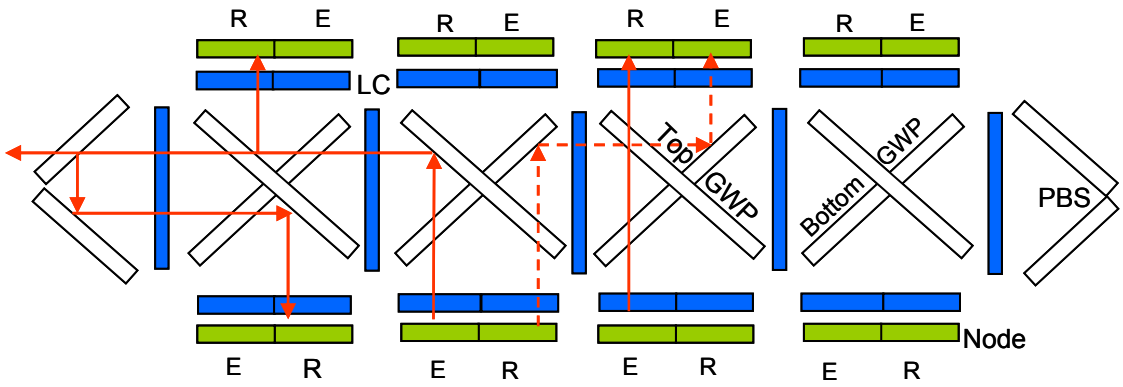


Figure 5.12. Optimised Cut-Through Ring (OCTR) Architecture. This design allows the communication between eight nodes and also other architectures connected to this architecture.

As an example of the real application of these architectures in parallel computing, the use the ORCT for implementing a hybrid distributed shared memory architecture is proposed. A set of nodes arranged in the OCRT can constitute shared memory architecture. From Figure 5.12 we can observe that if local memories are placed on one side of the architecture and only processors are placed on other side, then any processor can communicate with any memory and vice-versa. Moreover, the corners of the topology allow both the communication between processors themselves and the communication of this network to other architectures.

Multidirectional Optical Stage

Figure 5.13 shows the last design proposed in this chapter, the Multidirectional Optical Stage, which allows routing signal in and out of the node using four different directions. This multidirectional property is achieved by placing two crossed WGPs in front of the node and a total of six LCs as shown in Figure 5.13. Thus, a high number of components and, therefore, a high complexity is required. As can be observed, this design also used versatile nodes.

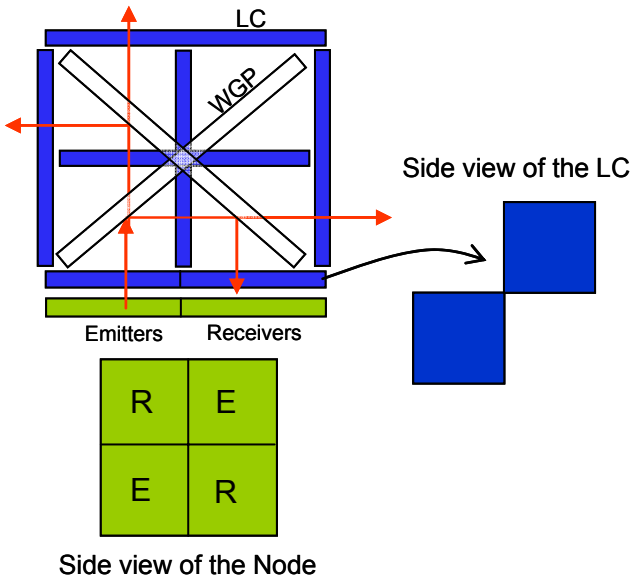


Figure 5.13. Multidirectional Optical Stage design. High complexity design using high number of components and versatile nodes. The side view of the LC shows that there are only LCs at the output of emitters.

Figure 5.14 shows the Multidirectional architecture where eight nodes are connected using four Multidirectional Optical Stages. This architecture is suitable for implementing very 'demanding' topologies such as the completely connected topology where any node can communicate with any other node in a single hop.

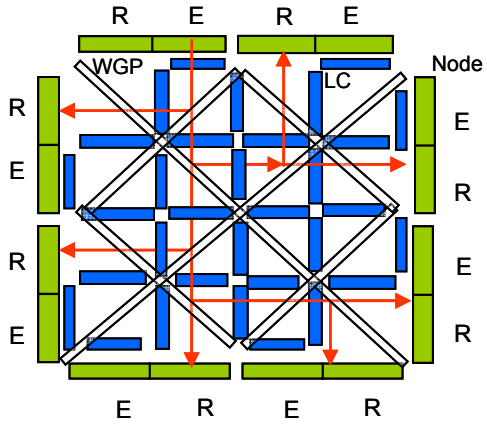


Figure 5.14. Multidirectional Architecture.

5.3.3 Performance of the Optical Highway Architectures

This section examines and compares the cost and performance of the architectures previously proposed. The cost is analysed in terms of the number of switching elements (LCs) and links (PBSs) and the performance, in terms of power losses, diameter and bisection bandwidth.

In order to estimate the cost of the design, the PBSs and LCs are numbered depending on the area they are covering rather than the number of individual structures used by the design. In other words, it is considered that one optical component (PBS or LC) covers all the emitters and detectors of a node. For example, in most of the architectures proposed, the first LC placed in front of a node covers just half of the node since the polarisation of the signal does not require twisting when arriving at the receivers. Therefore, this LC is counted as half of a LC.

On the other hand, in order to measure the diameter (maximum optical distance between any two processors) and Bisection bandwidth (measure of the maximum volume of communication between two halves of the network) is considered as one step counter the PBS/LC assembly since it is the basic optical stage for all designs

Having defined the properties in a way that allows the comparison of the architectures possible, Table 5.1 presents the results obtained, where P represents the number of nodes that the architecture supports, β attenuation of PBS, α is the attenuation of LC and γ and δ the attenuation associated with the QWP and the mirror respectively in the Ring architecture.

	Ring	**Ring Cut-Trough**	**Matrix**	**ORCT**	**Multidirectional**
# Switching, LCs	P	3P/2+2	2P	P+1	2P
# Links PBSs	$3P^*$	P	P	P/2+2	P
Diameter	P+2	P-1	P	P-2	P-2
Bisection bandwidth	2	2	P/4	1	P/4
Maximum Losses	$\delta\cdot\gamma^2\cdot(\alpha\cdot\beta)^{P+2}$	$(\alpha\cdot\beta)^{P-1}$	$(\alpha\cdot\beta)^{P}$	$(\alpha\cdot\beta)^{P-2}$	$(\alpha\cdot\beta)^{(P-2)}$

Table 5.1. Characteristics of the OH architectures. In the Ring Architecture the number of links 3P makes reference not only to the number of PBSs but also to the number of QWP and mirrors employed.*

It can be observed that the Ring Architecture presents both high cost and low performance, especially in terms of maximum losses. Therefore it is not a good option for being implemented in FSOI systems. The Ring Cut-Through architecture is a simple alternative that makes use of the FSOI properties more effectively.

The Matrix and Multidirectional architectures present similar properties: high connectivity, high cost, and similar attenuation. However, the complexity in terms of packaging of the Multidirectional architecture is higher since it requires far more individual components.

It can also be observed in the table that the ORCT architecture is a compromise design that combines low cost, relatively low complexity and good performance in terms of diameter and maximum losses associated. The drawback of this design is the bisection

bandwidth, which is only 1. That means that it is only necessary to remove one optical component to split the architecture in two symmetrical halves [11]. This is a measure of the volume of communication between the two halves of the architecture. However, the fact that the connectivity of this design is high (three directions per optical stage) means that it uses the bandwidth more efficiently than the other design which has more bisection bandwidth but less connectivity.

5.4 Conclusion

This chapter has presented the design and analysis of the OH at different levels. At Node level, requirements for the mapping of the emitters and receivers have been established and two designs have been proposed - the Simple and Versatile configurations.

Four structures have been designed at the Optical Stage level: Unidirectional, Bidirectional, Three-directional and Multidirectional. Their names make reference to the number of directions that the optical signals can be routed in and out of the node.
Additionally, different OH architectures based on the four optical stages designed have been proposed and their properties in terms of cost and performance have been analysed.

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Chapter 6
Experimental Implementation of an Optical Highway Architecture

6.1 Introduction

The last experimental chapter of the thesis focuses on the construction and first proof-of-work of a particular architecture: the Optimised Cut-Through Ring (OCTR) architecture, which has been proposed in Chapter 5. To prove the reconfigurability properties of this architecture, eight nodes will be connected to each other.

Custom LCs have been especially designed for this experiment. Due to the high number of LCs –around 30- and their new driving specification, it has been also designed new PCB circuits.

Another important innovation is the use of a Field programmable gate array (FPGA) board for controlling both the LCs and the sources. In previous chapters the LCs and sources were controlled using different devices: DSP for the LCs and Signal Pulse Generator for the sources.

6.2 System Overview

To aid understanding, it is convenient to first examine the system as a whole. Subsequent sections break the demonstrator down into its component modules while detailing both their construction and performance. This process follows data flow through the demonstrator with results presented as appropriate either during the description or in the results section at the end.

An image of the whole system can be seen in Figure 6.1. The FPGA board has been programmed for controlling the LCs and the lasers which requires different frequencies. Manual switches have also been programmed to allow the implementation of different topologies by controlling the appropriate LCs. Two PCBs, with a total number of 30 outputs, have been designed to amplify the signal from the FPGA and supply the LCs

with the right voltage level. The optomechanical structure on the right has been designed to interconnect 8 nodes and allows the implementation of multiple topologies. The Rapid Prototyping technology has been used again to build the mechanical structure. In this case, the system consists of two large structures where many smaller parts holding the optical components are slotted or attached. In total there are 12 PBSs using three different types of holders depending on the position given; 8 laser holders, each one designed to slot two laser collimators tubes; and 13 liquid crystal holders capable of holding 4 new custom-made liquid crystals each.

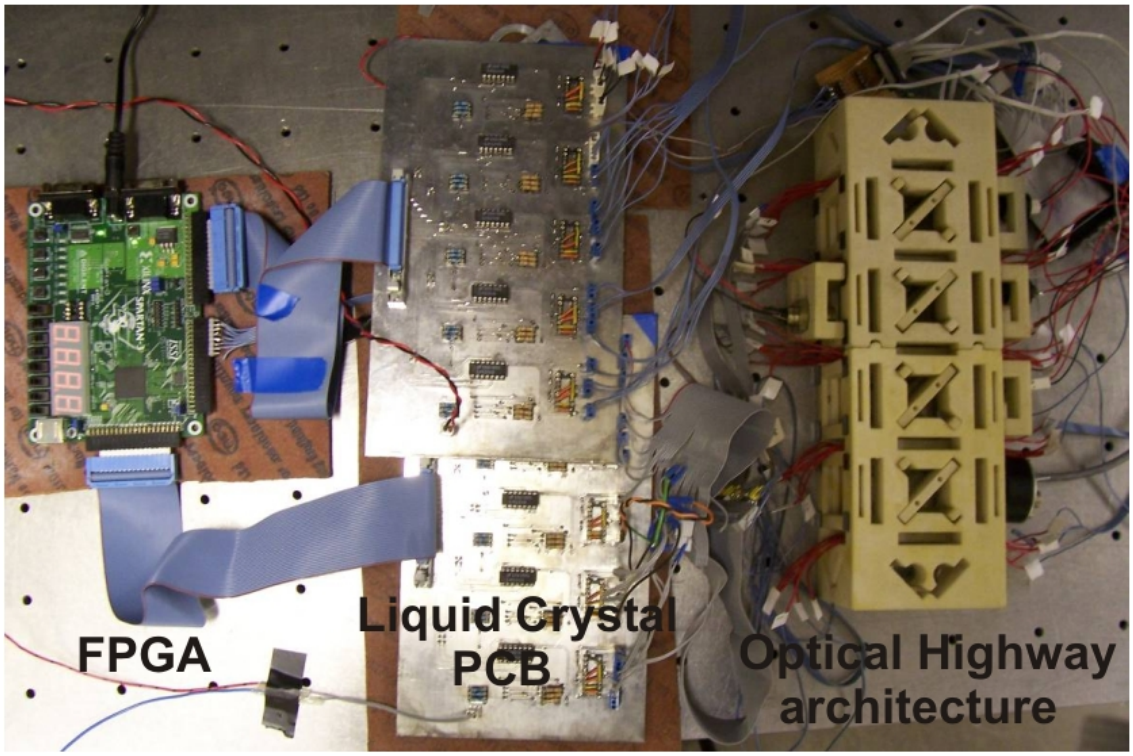


Figure 6.1. Overview of the system. FPGA used to control the LCs and the sources. A PCB has been designed to amplify the signals from the FPGA board and supply the LCs with the right voltage. The optomechanical structure on the right has been designed to support multiple topologies for interconnecting 8 nodes with two sources and two detectors at each node.

The size of the architecture has been determined by two factors: the maximum number of components that we have managed to obtain and the maximum number of stages that the optical signal can pass through.

For this experiment we have a limited number of components: 5 laser collimators, 2 amplifying Si detectors and 10 PBS plates.

Although the design can support more components, only 5 out of the 16 possible sources and 2 out of the 16 possible detectors can be employed at this stage of the experiment.

The system can also hold a maximum of 12 PBS. This does not prevent us from conducting the first set of experiments which consist of testing the electronic devices -FPGA and PCBs-, system alignment, crosstalk and attenuation of the optical signals; implementing elementary configurations and analysing some important properties of the architecture. It is expected to fully exploit the potential of the structure in future experiments.

6.3 Optimised Cut-Through Ring Architecture

We have chosen the OCTR architecture for the experiment because as shown in the previous chapter is an optimal architecture in terms of cost, number of components and performance i.e. symmetry and the possibility of implementing different topologies.
Figure 6.2 shows one optical stage of the OCTR architecture. Note that crossing PBS plates allows routing the signals from a node in three different directions: front, right and left. The arrays of sources attached to the node are split in two groups and arranged in diagonal allowing half of the sources to be routed towards the front and the left and the other half towards the front and the right. The detectors, same as emitters, are separated in two groups and placed in diagonal, allowing a complete symmetry of the outputs and inputs of the node. In addition, pixelated LCs can be employed allowing individual control of each signal coming out from each emitter. These characteristics make this architecture ideal for interconnecting a high number of nodes using a relatively low number of optical stages.

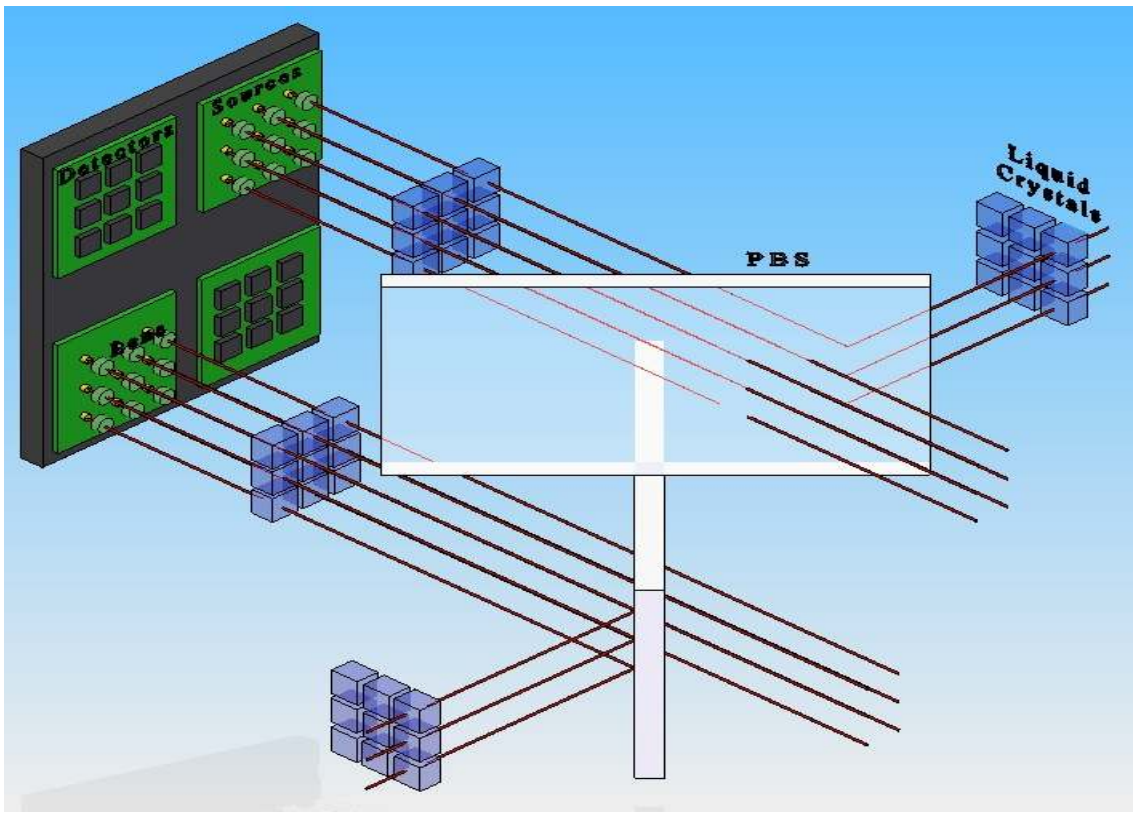


Figure 6.2. One stage of a OCTR architecture based on the three-directional optical stage. Two PBS are cross placed one on top of each other in front of a node, which is attached with 18 detectors and 18 sources emitting in three different directions: front, right and left. The pixelated liquid crystals allow the reconfiguration of each optical channel.

For this first design some restrictions have been adopted. We have used a minimum number of sources and LC's per node in order to simplify the architecture and minimise costs and alignment problems. The group of sources and detectors associated with one node have been reduced to two sources and two detectors, and instead of the pixelated LCs, only 2 LC's are used to route the signal out of the emitters.

Figure 6.3 shows two nodes placed in parallel and the use of the simplified configuration described previously. This scheme shows that despite the limited number of sources and LCs employed, the architecture is able to interconnect dynamically both nodes and their respective right and left directions. Note that in front of each detector there is no LC. The reason for this is that there is no need to control the polarisation of the signal at this stage of the interconnection and its use will only contribute to the attenuation.

A drawback in the configuration is that it is not possible to use clean up polarisers at the input of the detectors to prevent the crosstalk becoming too high. Therefore it is paramount that the LCs perform as ideally as possible in order to keep the misdirected signals as low as possible.

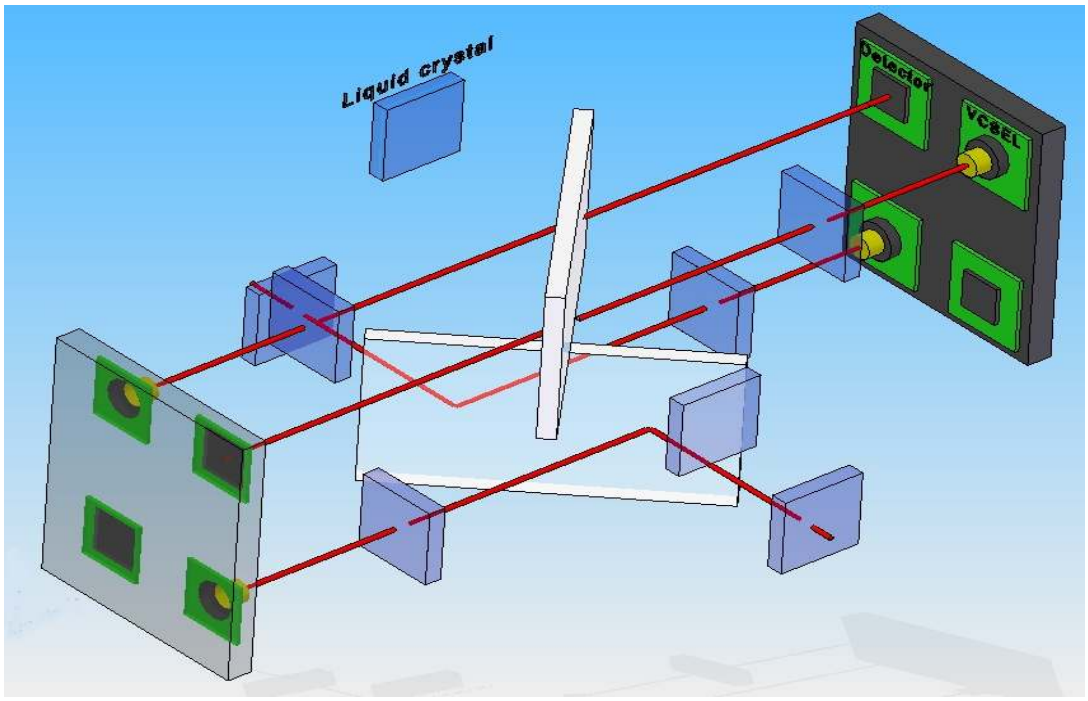


Figure 6.3. Practical implementation of OCTR architecture where two nodes are interconnected using limited components; two emitting sources, two detectors and two liquid crystals per node.

Due to its symmetry, this architecture is easily scalable since it allows the addition of either more stages or nodes at both sides of the stage. For example, placing two other nodes at both sides of the stage leave us a four node architecture system interconnected by using only one optical stage. Even the simplified configuration with only two sources, two detectors and two LC's per node has the potential of allowing the optical communication of each node with any of the other three nodes. In fact, it is possible for any node to communicate with any other two at the same time. What is more, by simply increasing the number of sources, detectors and LCs to three per node we would have a completely connected topology with all the nodes communicating with each other at the same time.

However, at this moment we are going to escalate to a higher number of stages keeping as low as possible the number of optical components used.

In order to do this, more stages must be placed at the sides of the two nodes as shown in Figure 6.4. This will leave two arrays of nodes parallel to each other and the optical interconnect stages in the middle allowing the communication of the nodes. Therefore, using this scaling configuration, the interconnection of eight nodes require four optical stages.

Figure 6.4 shows the four stages of the optical system that have been implemented experimentally. The corners of the architecture have been terminated using two PBS which have been placed vertically and oriented 45° each other. This allows routing the signal back into the system or out of the system depending on the set up of the corresponding LCs. This architecture allows direct communication of each node with any other node and the exterior. However, it is more suitable for implementing other topologies that require only direct communication between nodes placed on different sides of the architecture.

For interconnecting nodes on the same side, it is necessary to route the signal to the nearest corner and send it back into the system using another optical channel.

The use of only two sources and two LCs per node limits the number of channels in the system and therefore the number of different topologies that can be implemented. For example, it is not possible to implement a completely connected topology, which requires a least 7 sources-detectors and 7 pixelated LCs.

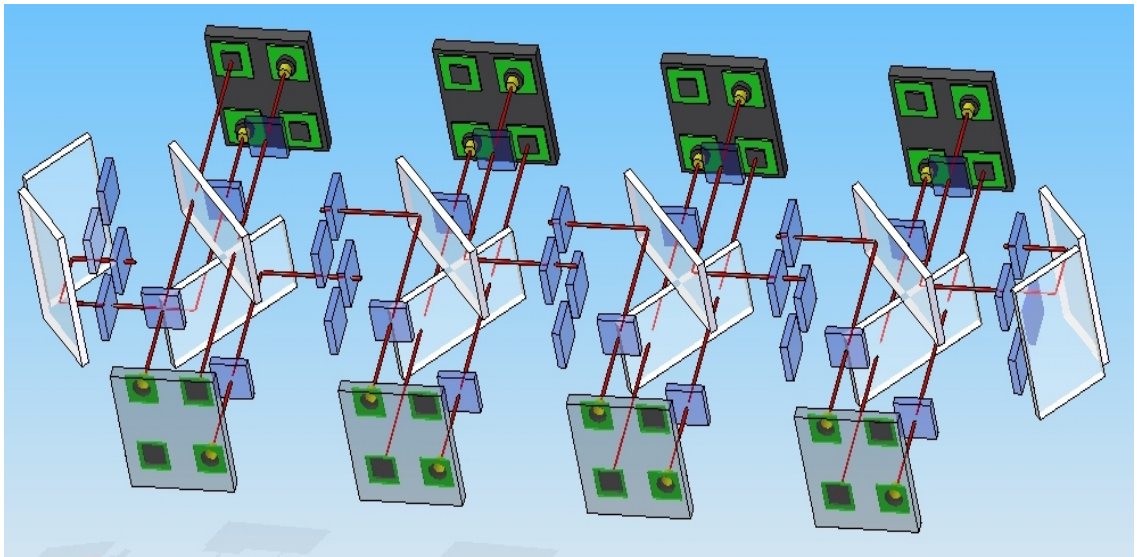


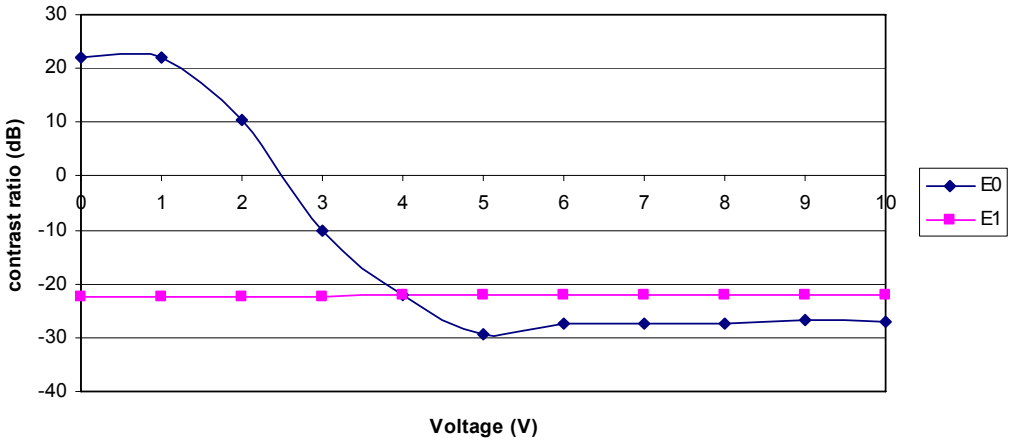
Figure 6.4. Interconnection of eight nodes using four stages in the OCTR architecture. The PBSs on the corners allow the nodes placed on the same side to be interconnected directly.

6.4 Optical Components

Most of the optical components used in this experiment, 2mW CW Diode Laser, Si 10 MHz amplify detector and 32 x 18 mm wires plates working as PBS have been used previously. The only two new optical components are two new lens collimator tubes and the custom made LCs. The two new lens collimator tubes together with the previous three make a total of five collimators that will allow us to carry out the first set of experiments of the OCTR architecture. The dimensions of these new collimators are slightly different from the older ones, therefore the structure must be designed asymmetrically in order to hold both types of collimators. Next we will analyse the new custom LC.

6.4.1 Liquid Crystal Characterisation

The implementation of the OCTR architecture requires new LCs of smaller dimensions and more uniformity and stable characteristics. LC-TEC DISPLAYS has manufactured for us a custom 90° twisted nematic LC that suits perfectly our purposes. The new LC has an active area of 10 x 9 mm^2 .From the graphs shown in Figure 6.5 we can observe that the values obtained for the parameters ε_0 and ε_1, in terms of best values obtained, are similar to the ones obtained in chapter 4 for the LV00S LC from Excel-Display. However, the new LC presents both a more uniform behaviour of the ε_0 and ε_1 parameters over its area and more stability due to its smaller dimensions and the use of a better driving control method. The driving control consists of a square-wave voltage with frequencies of around 500 Hz that prevent impurity ion migration from occurring within the liquid crystal material [1]. Another advantage of this custom-made LC is that it has been designed to achieve a better value of ε_1 for the 0° and 90° rotational positions, which are the positions that we are going to use.



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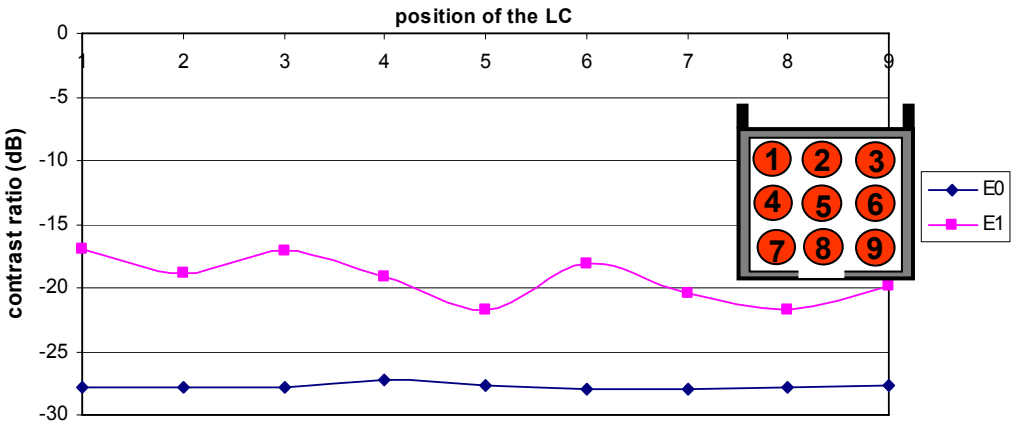

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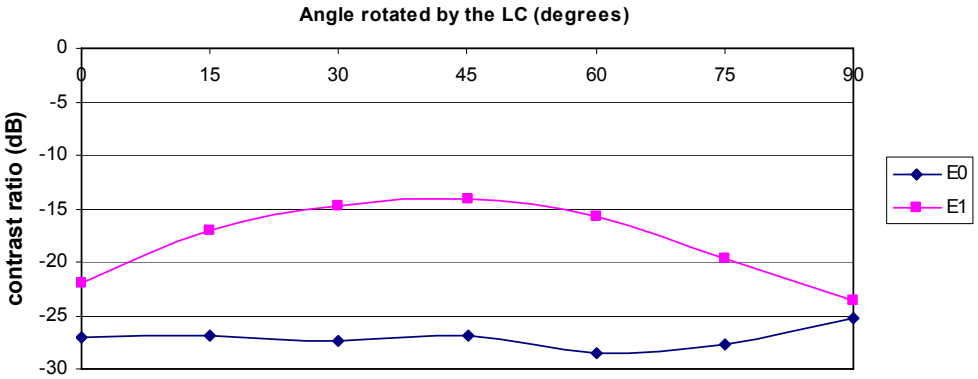


(c)

Figure 6.5. Characterisation of new custom LC from LC-TEC Display. In (a) the values of ε_0 and ε_1 are analysed for different voltages applied to the LCs. (b) Shows the LC characteristics under translational displacement of the LC with respect to the optical signal and (c) shows the variations under rotational displacement of the LC.

6.5 Design of the OCTR Architecture Using Rapid Prototyping Technology

Having analysed the requirements for implementing the OCTR architecture and the optical components that are going to be employed, we present in this section the mechanical design of the structure and the assembly of the optomechanical system.

6.5.1 Design and Implementation of the Structures

As it was mentioned at the beginning of the chapter rapid prototyping technology has been employed once again for implementing the mechanical structure. In this case, the rapid prototyping machine available at the Digital Tools Manufacturing Group (DTMG) at Heriot-Watt University has been pushed to its limits for producing both high quantity and good quality of components.

Figure 6.6 shows the design of the most complicate component; a large structure where the holders for the LCs and PBSs are slotted and the sources and detectors holders are attached to its sides. For designing this structure it has been necessary to take into account the design of all the other components in order to meet the alignment requirements. Due to the limited dimensions of the RP machine the structure has been split into two parts. This does not imply a drawback since the two-part structure allows an easier access for the assembling and can help to correct some alignment problems.
This structure has been designed in order to arrange the components as has been proposed in Figure 6.4. The LC holders are introduced through the sides of the structure. There are small slots on top of the structure that make the handling and alignment of the LCs holders easier. The PBSs are introduced from the top of the structure.

Additionally, a modification of the corner has been made in order to allow the routing of the signal in vertical direction. In order to do this, two extra slots, at 45° to each other, have been made at the end of the structure where the two PBS can be slotted. Holes have been also made on the top and bottom of the corners allowing the signal to go up or down.

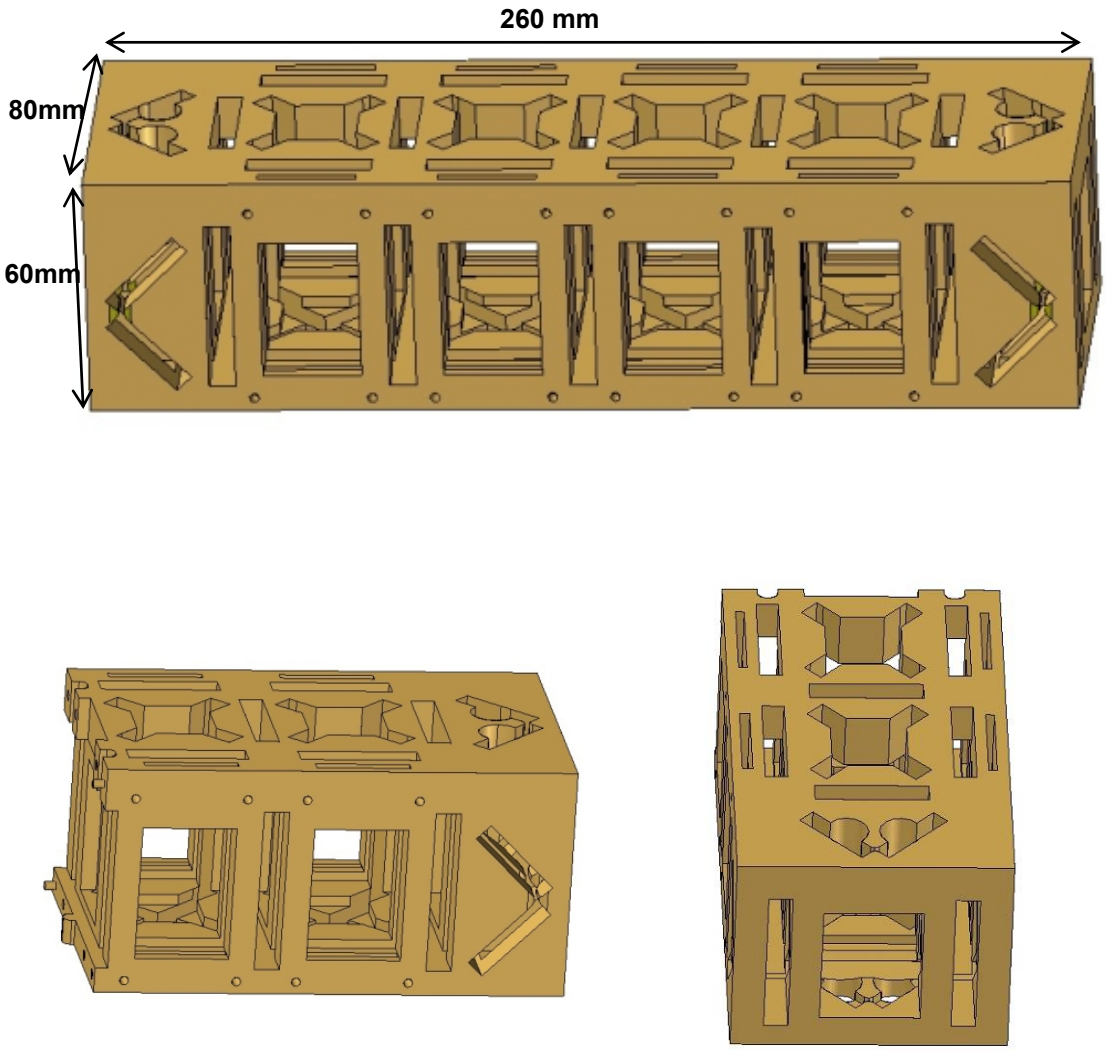


Figure 6.6. Large structure where LC and PBS holders are slotted and sources and detectors holders are attached.

Figure 6.7 shows the three different designs for the PBS holders. The holder shown on Figure 6.7 (a) is designed to place the PBS on the bottom of the structure; thanks to the long legs, these can be handled from the top of the structure. The holder on Figure 6.7 (b) goes on top of the first one and the crossing point of the holders has a wider contact surface ensuring more stability to the system.

The last PBS holder, Figure 6.7 (c), has been designed in order to place the PBS in the corners. It can be observed that one of the lateral parts that hold the PBS has been removed. This allows us to place the two PBSs in each corner as close as possible. Since all the PBSs have the same size and were obtained before the experiment, their dimension can be a limiting factor and therefore the design of the structures has to adapt to these dimensions.

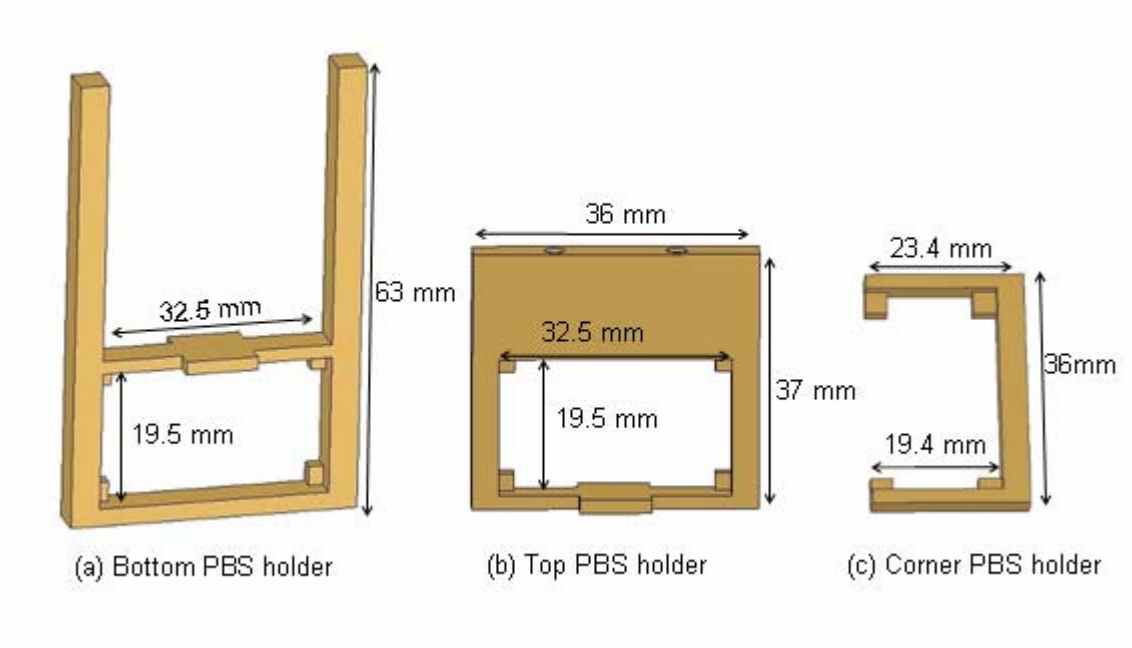


Figure 6.7. PBS holders design.

Finally, Figure 6.8 shows the design for the LC and Source holder. The LC holder, Figure 6.8 (a), holds a maximum of four LCs while the sources holder, Figure 6.8 (b) is designed to hold the two different types of lens collimator tube that are going to be employed.

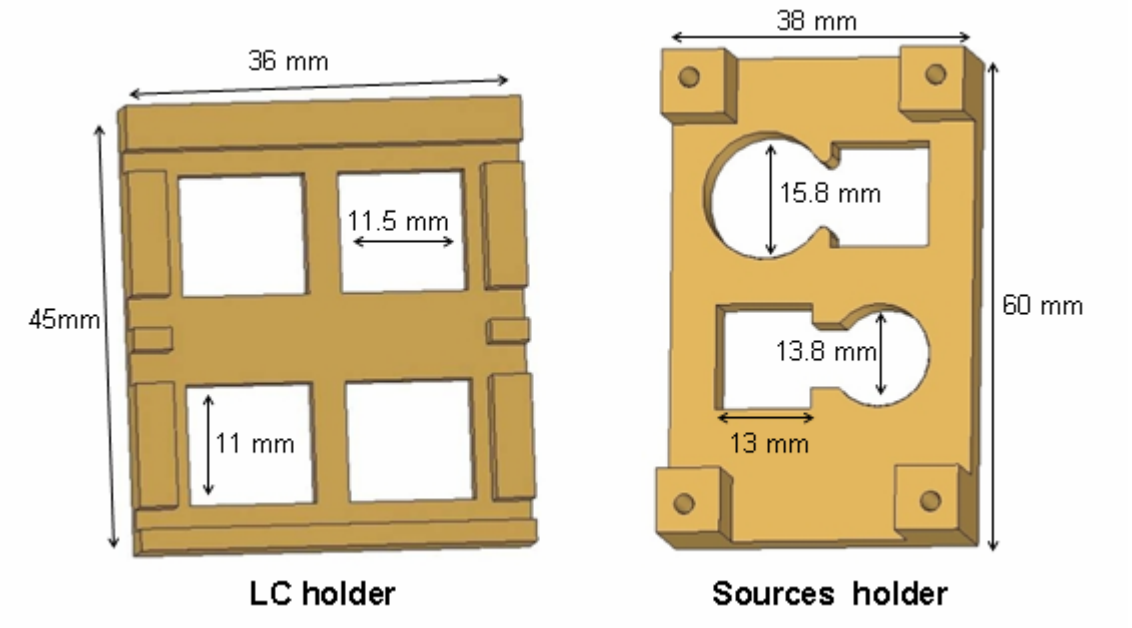


Figure 6.8. LC and Source holder.

We would like to point out the advantages of this design, which involves using many different small parts with the optical components attached to them. These parts are then introduced into a larger structure. This design is more convenient than others in which

only one structure is used and where all the optical components are directly attached to it. There are several reasons which support this criteria:

First of all, the handling of the optical components is safer. This is especially important for the wire grid plates where the tiny aluminium wires are easily damaged. Therefore, it is safer to make a frame for this component and handle the holder instead of the optical components.

The second advantage is the mechanical reconfigurability of the system. Due to the possibility of introducing the PBSs in different orientations at each stage of the structure it is possible to implement other architectures apart from the one proposed in Figure 6.4. For example, we could implement other architectures where some nodes of the same side are directly connected without the need to route the signal to the corners of the structure.

The third reason is that this design makes it possible to easily replace one optical component for a new one with different specifications by just modifying the design of its corresponding frame. For example, scaling the system to a higher number of sources per node would require just redesigning the source holder while the rest of the structures would be kept the same.

On the other hand, the use of many components increases the difficulty in the alignment process. This is aggravated by the low resolution of components (around 1mm) due to the low quality of materials used in the production of rapid prototyping structures.

The problem has been overcome using optical components requiring low positional tolerances; The LC has an active area of 10 mm x 9 mm, the optical beam is expected to be collimated to a spot size between 3 and 5 mm and the dimension of the PBS allows around 3 mm of misalignment. In addition, the detector with an active area of 3.5mm x 3.5mm can be manually aligned at each output of the system to capture all the optical signal power coming out from system.

6.5.2 Assembling the Optomechanical System

In this section we are going to describe the assembly process of the optomechanical system. In this process adhesive magnetic tape has been extensible used for attaching the optical components to the holders and also for making it easy to stabilise the alignment of the different components.

Figure 6.9 shows the assembly of all the optical components onto their corresponding holders. In this picture it can be observed four LCs attached to the holder using the adhesive part of the magnetic tape and the assembly of the PBSs onto the three different types of frames. The photo also shows the assembly of the two different laser collimators tubes. The production of the laser frame has required the tightest mechanical tolerance -0.5 mm- in order to keep the optical beam as straight as possible.

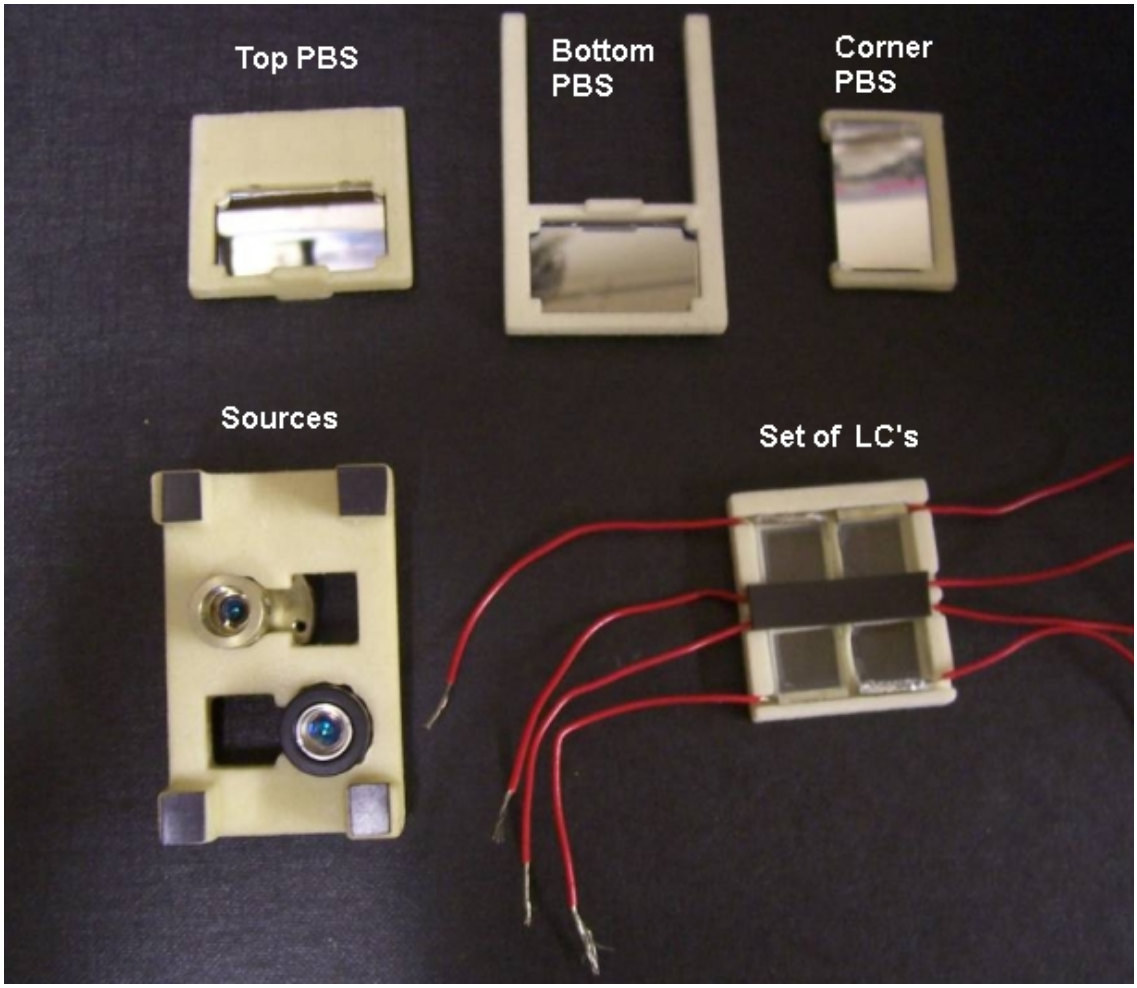
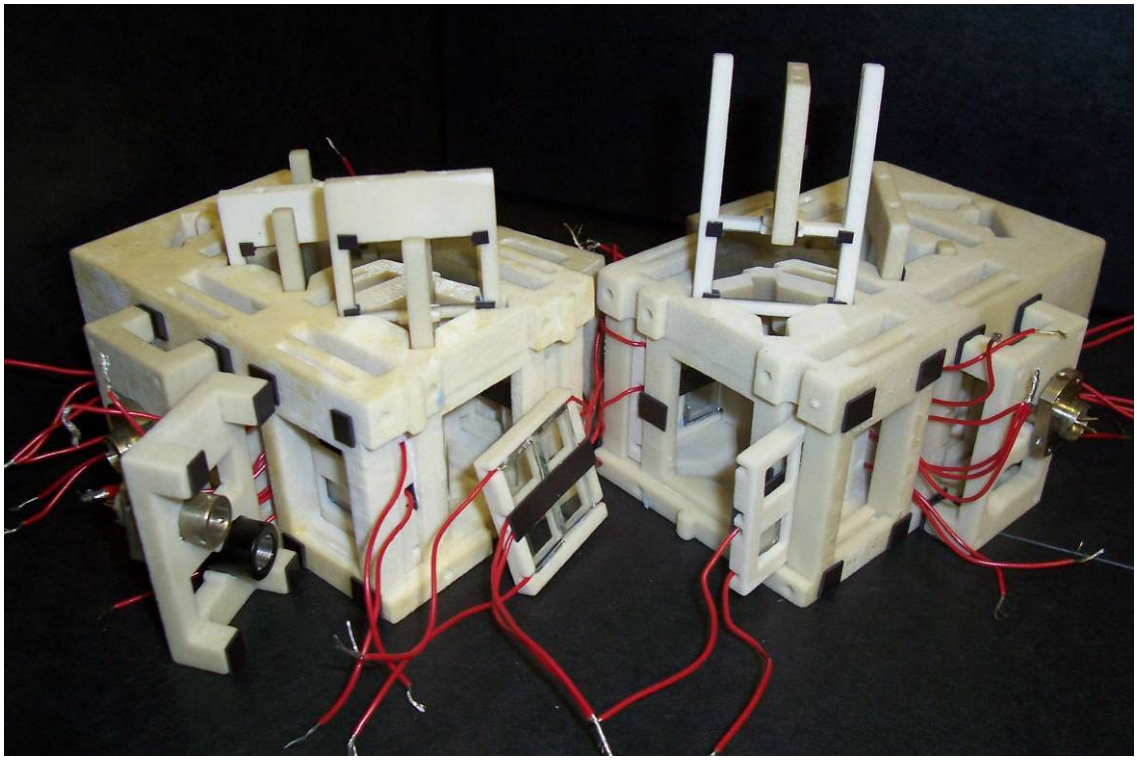


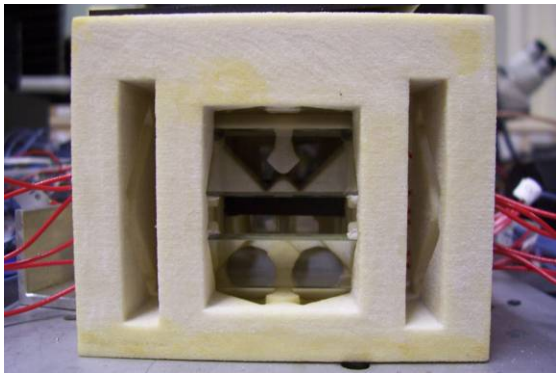
Figure 6.9. Assembly of PBSs, sources and LCs.

Figure 6.10 shows different views of the assembly of the components onto the two large structures. These photos help us understand how the different components are placed. It can be observed that the LCs can be introduced into the structure using many different slots which are placed on the sides and corners of the structure. All these slots are necessary since the wires of the LCs block them once they are placed inside.

It can be observed also how the PBSs are introduced from the top into the structure. Figures 6.10 (b) and (c) show the two different configurations for the PBSs that can be implemented on the corners of the structures allowing the routing in different directions.



(a)



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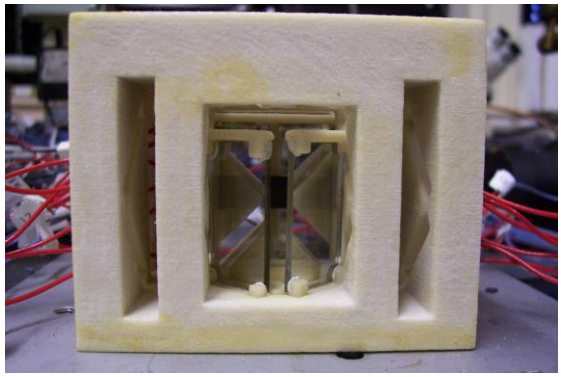


(c)

Figure 6.10. Assembly of components onto the two large rapid prototyping structures.

6.6 Programming the Field Programmable Gate Array Module

As mentioned in the introduction, the use of an FPGA entails an advantage over previous experiments where the LCs and sources were controlled by two different devices: a DSP and a Signal Pulse Generator. These devices were unsuitable for the purpose of this experiment because they could just control few components and only individually.

The use of FPGAs has been suggested [2] [3] for optoelectronic systems due to their intrinsic reconfigurable properties. An FPGA is a semiconductor device containing programmable logic components called "logic blocks" and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or simple mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memories. A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer. Once the FPGA is manufactured, logic blocks and interconnects can be programmed by the customer or designer in order to implement any logical function; hence the name "field-programmable". The role of the FPGA in this experiment is to centralise the control systems, optimising the communication and processing a wide range of topologies.

Figure 6.11 shows the FPGA Spartan 3 board from Xilinx that has been used and its main components; the core of the board, 200,000 gate Xilinx XC3S200 FPGA unit, three expansion connectors with 40 outputs each and a set of 12 switches of two different types: four momentary-contact push button and eight slide switches. The expansion connectors A1 and B1 are employed for connecting up to 15 LCs each and the expansion connector A2 is used to control a maximum of 8 sources. One slide switch is utilised for changing the type of signal applied to the sources, from a CW signal to a pseudo random pattern useful for generating eye diagrams. Four other slide switches are used in conjunction to set up the different topologies by controlling the respective LCs.

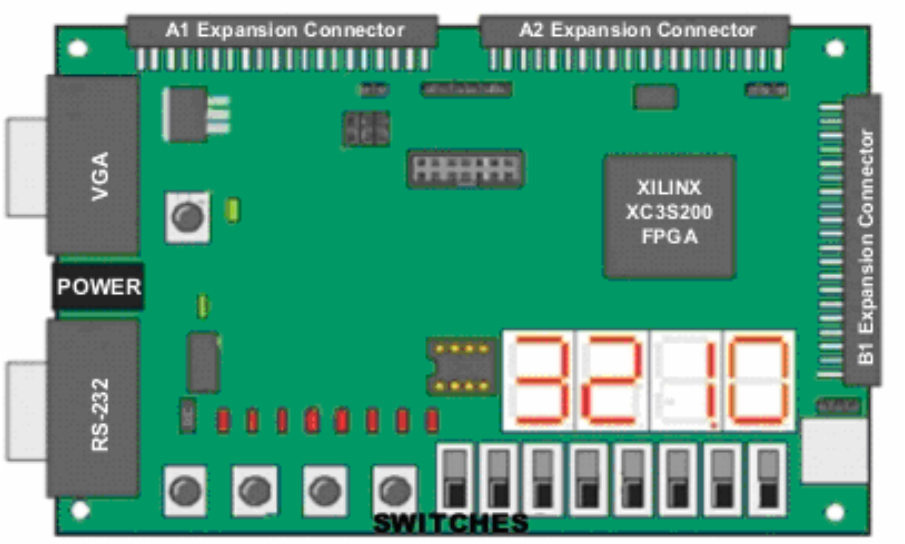


Figure 6.11. FPGA Spartan 3 board from Xilinx.

The four switches used in combination allow us to implement 16 different topologies within the same architecture. This means that the way in which 8 nodes are interconnected with each other can be modified in 16 different ways. This number can be easily increased to, for example, 32 by just employing one more switch. These configurations, rather than analysing complex topologies, are going to be used for the following: testing components, single optical channels and the interaction between optical channels. Complex topologies will be left for future work.

A hardware design language –VHDL- has been used for programming the FPGA board. The ISE Software developed by Xilinx turns then the VHDL code into a netlist and runs a place and route program specific to the target FPGA.

The VHDL code has defined 6 input addresses to control the sources and LCs and 38 output signals; 30 for LCs and 8 for sources. The code also includes clock dividers to reduce the internal clock signal of the FPGA from 50 MHz to 600Hz for the clock signals applied to the LCs, and to 13 Khz for the signals applied to the laser diodes.
A Linear Feedback Shift Register (LFSR) has also been added in order to modulate the laser diodes with a pseudo random pattern.

Figure 6.12 shows the simulation of the code on ModelSim where all the input addresses and output signals are presented. Note that the same pseudo random pattern is generated for the 8 output lasers signals after the reset address input is activated. This

figure also shows four different configurations for the 30 LC output signals set by the four input address.

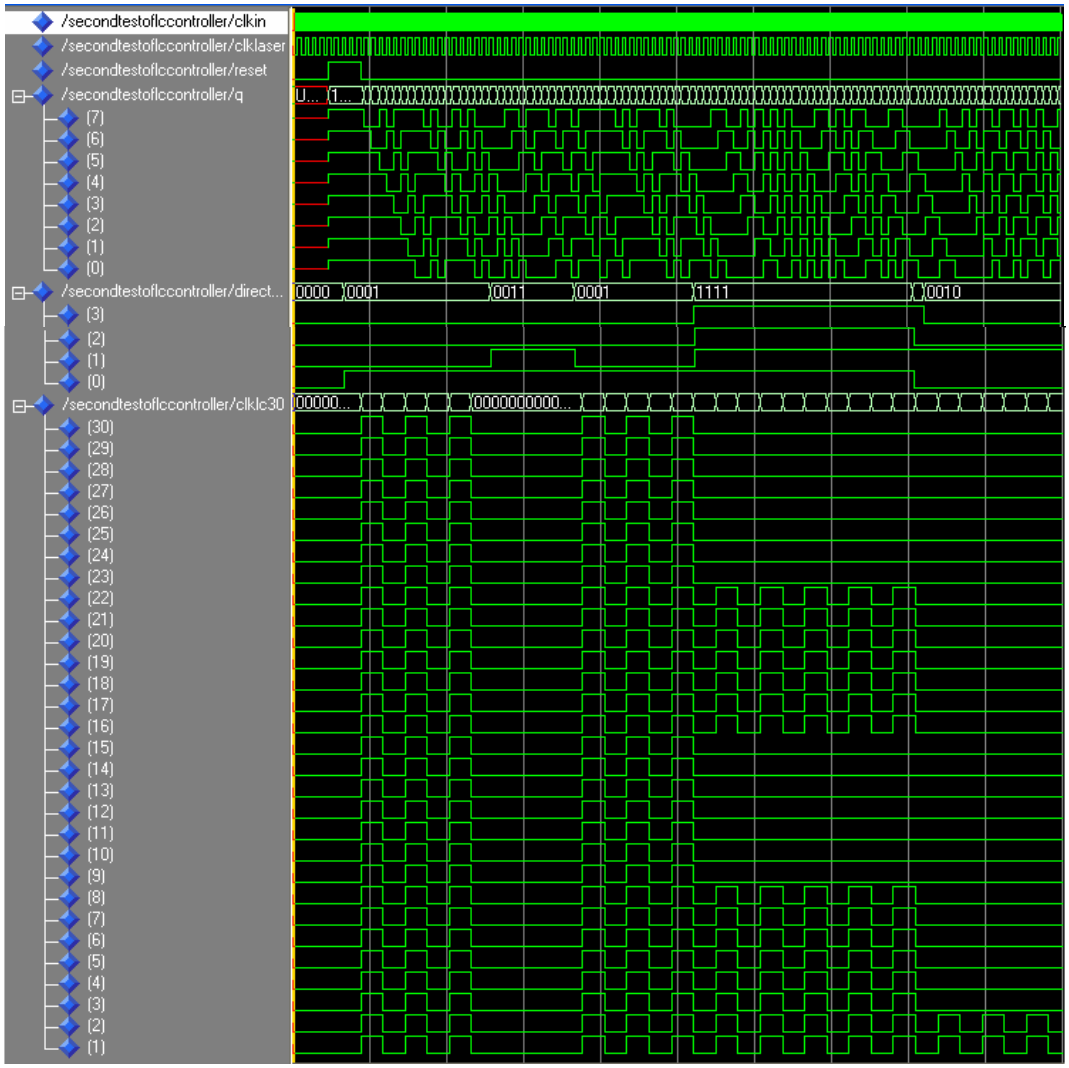


Figure 6.12. Pseudo random pattern that drives 8 laser outputs. Four input address control output of the 30 LCs.

Once the code is written, the ISE software creates and edits timing and area constrains. Thus the input address is linked to the switches of the Spartan board and the output signals to the pins at the expansion connectors.

6.6.1 PCB Design

The Spartan-3 Board uses a 3.3V regulator to feed all the voltage supply inputs –Vcco- to the I/O expansion connector banks. Custom circuit modules must be designed in order to supply the LCs and sources with the right driving voltage.

From the LC voltage characteristic graph obtained previously in Figure 6.5 (a) we can observe that the LC requires up to 6 V driving voltage. A simple amplifier circuit as shown in Figure 6.13 is used for amplifying the 3.3 V FPGA outputs up to 6 V.

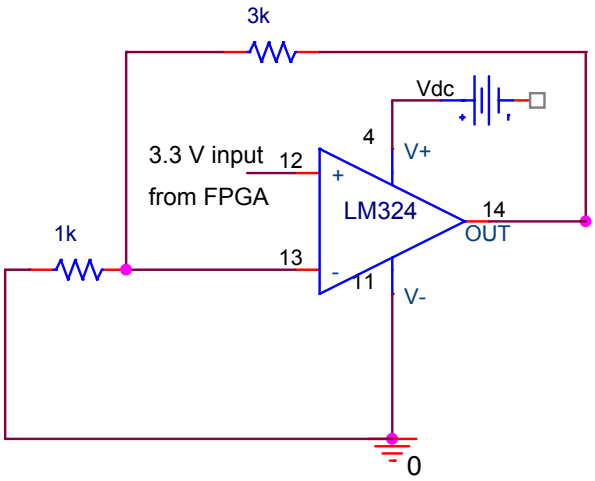


Figure 6.13. Amplifier circuit employed to convert the 3.3 V of the FPGA output up to 6V.

As shown in Figure 6.14, two PCBs have been designed for driving the LCs. Each PCB can support 15 LCs. Instead of soldering the electronic components directly to the board, we have used sockets. This way the electronic components can be easily replaced by others in case the input or output specifications change.

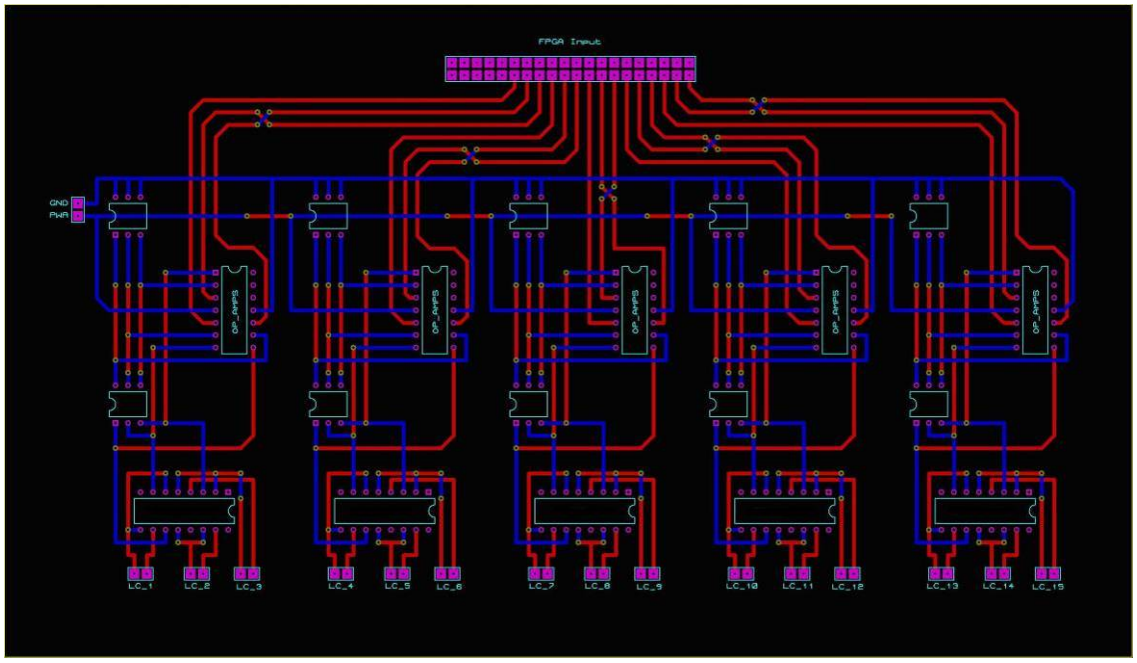


Figure 6.14. PCB module layout for driving 15 LCs. The blue is the upper layer and red is the lower.

Another PCB has been designed for driving the five diode lasers at a current of 20-55 mA and at an operating voltage of 2.7 V. In order to do this, five resistances of 20 ohms have been placed in series with the FPGA outputs.

6.7 Results

In this section we will present a set of experiments which involve testing the FPGA and PCBs, and the properties of the OCTR architecture. We will implement some basic topologies in order to analyse the connectivity properties of the system, alignment, signal attenuation and crosstalk caused by misdirected signal. Future work will be focused on fully exploiting the OCTR architecture by implementing more complex topologies.

Figure 6.15 shows three signals taken at the FPGA and LC PCB outputs; The 3.3 Vp-p pseudo random pattern (purple) obtained from the FPGA output used to drive the sources, and the 3.3 Vp-p and 8 Vp-p signals (green and yellow) correspond to signals taken from FPGA LC output and the amplify LC PCB respectively. It has been found that all the output signals (30 for driving the LCs and 5 for driving the laser) behave as expected.

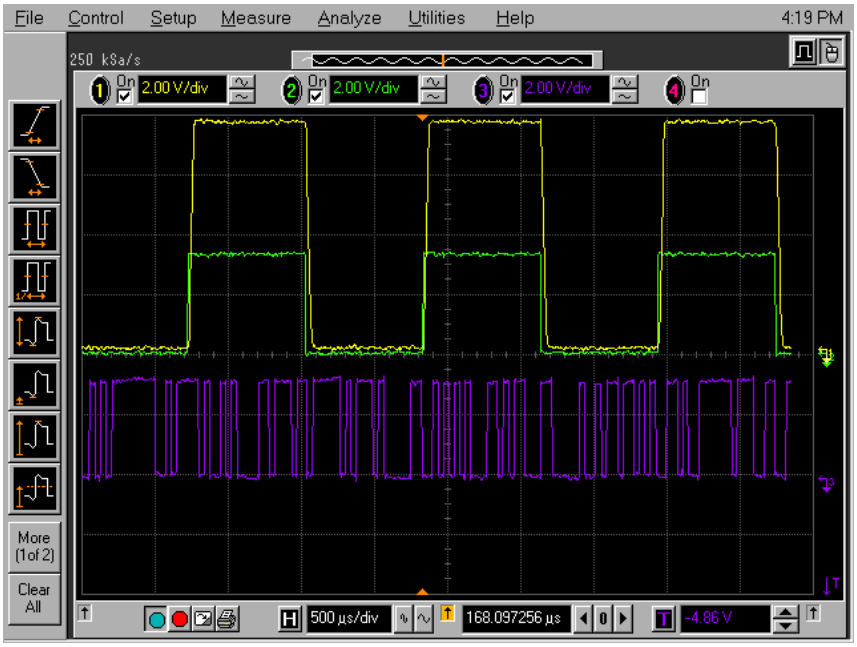


Figure 6.15. Output from FPGA of LC and laser, and from PCB of the amplified signal of the LC.

Figure 6.16 shows the eye diagram of a free space optical signal obtained from a detector of a source placed at a 20 cm. This signal is a maximum reference value since it is not affected by attenuation of optical components, misalignment or crosstalk.

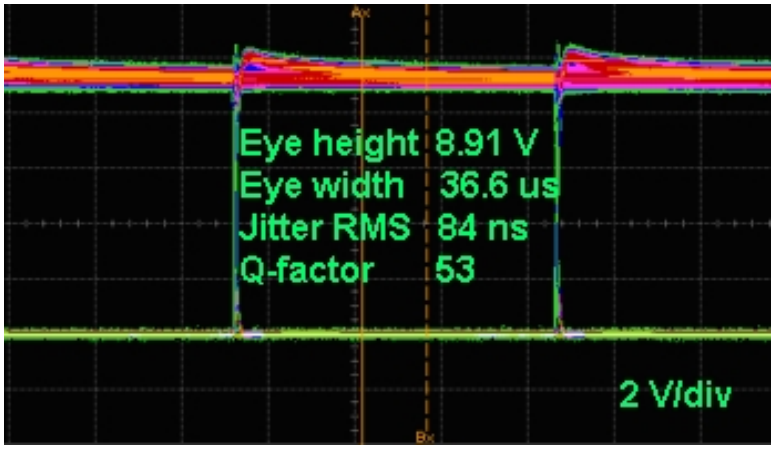


Figure 6.16. Eye diagram of a diode laser emitting at 14 Khz obtained by the amplifier detector.

In order to easily understand the relation between different components of the system we propose the scheme presented in Figure 6.17. In this figure the LCs, PBS and sources have been placed, named and linked. This two dimensional schema will also help us visualise the different configurations and topologies that can be implemented. Figure 6.17 can be interpreted as a top view photo of the OCTR architecture where the

LCs and nodes have been placed facing up while the PBSs have been kept in their original position. The colour criterion is important to establish the relation between the different components. The blue colour represents components that are placed in the top section of the architecture and the red is associated with all the components placed in the bottom section. Therefore, signals coming out of a blue source of any node can only be reflected by blue PBSs. their polarisation can only be modified by blue LCs placed on their way and they can only reach blue detectors at a node. The same happens with signals coming out of red sources. Note that the vertical PBSs placed on the corners are black. This is done to point out that they can reflect both signals coming out from blue and red sections. This scheme does not contemplate the possibility of using lateral slots on the corner of the structure for connecting top and bottom levels. Therefore signals using blue and red components do not mix with each other.

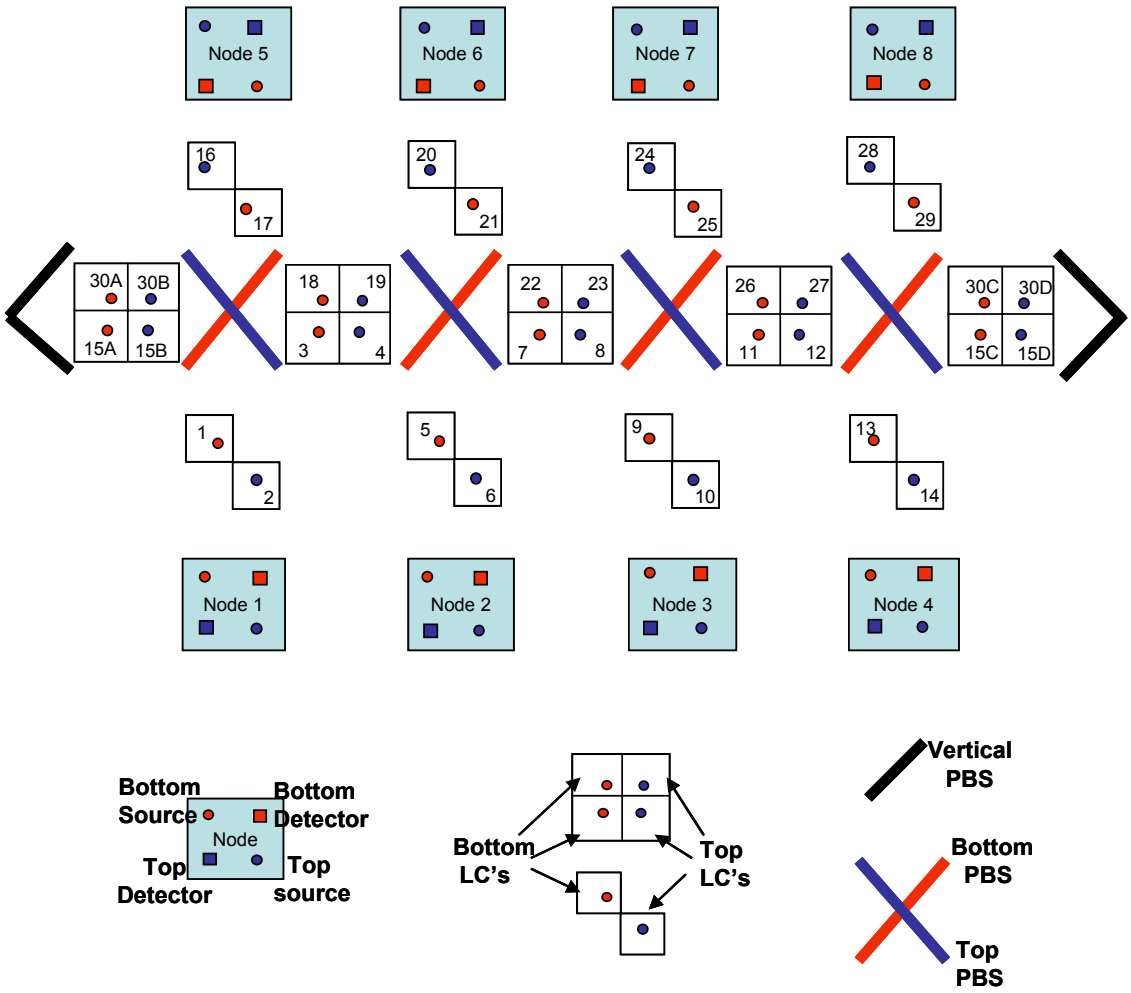


Figure 6.17. Two dimensional schema of the Multidimensional OH.

Before explaining the different configurations implemented it is worth remembering how the assembly LC-PBS routes the optical signal; Independent of the polarisation

state of the signal, p-polarised or s-polarised, the LC twists the polarisation 90° when it is Off, and keeps the polarisation untwisted when it is On. Then the PBS reflects or transmits the signal depending on how the LC has modified the polarisation.

Next, a set of three experiments is presented. These experiments are carried out in order to analyse the feasibility of the system. The first two experiments are oriented to test the connectivity of one node with the rest of nodes and outputs by studying the attenuation and alignment at different stages. The first one will analyse the connectivity of Node 1, N1, and the second one will study Node 2, N2. Due to the symmetry of the architecture, by connecting N1 and N2 with the rest of nodes and outputs all different configurations that one node can support are covered. Therefore, the analysis of N1 is equivalent -in terms of number LCs employed and their states- to the analysis of Nodes 5, 8 and 4. And the Nodes 3, 6 and 7 are equivalent to N2.

In the last experiment, multiple sources will be used from different nodes in order to show some of the unique properties of FSOIs such as signal contact, overlapping, crossing, and broadcasting. This way the efficiency of the optical channel with respect to previous demonstrators will increase.

6.7.1 Experiment 1 - Connectivity of Node 1

In this experiment different configurations are proposed to connect N1 to the other nodes and Outputs. Figure 6.18 shows the connectivity of N1 using the bottom red source and top blue source. It can be seen that the blue source is used to connect N1 to the Left Output and N1, N2, N3, N4 and N5. Similarly, the red source connects to N5, N6, N7, N8 and the Right Output. Although this architecture allows other configurations, the ones mentioned above are the optimal configurations in terms of minimum number of stages required.

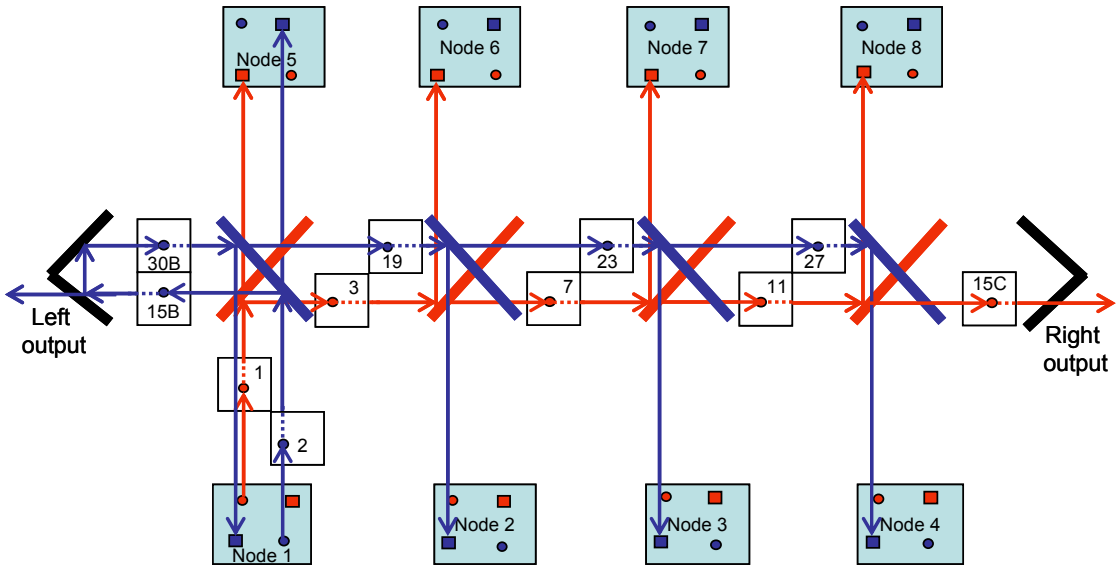


Figure 6.18. Connectivity of N1. This diagram shows the LCs employed for connecting N1 to the rest of nodes and outputs. Note that the bottom red source of N1 uses the LCs 1, 3, 7, 11 and 15C for connecting to N5, N6, N7, N8 and the Right Output. At the same time the top blue source can use LCs 2, 15B, 30B, 19, 23 and 27 for connecting N1 to the left Output and N5, N1, N2, N3 and N4.

Table 6.1 is proposed in order to see the function of each LC and make the programming of the FPGA easier. Table 6.1 (a) shows the state of the LCs 1, 3, 7, 11 and 15C employed by the bottom red source of Node 1 in order to connect it to other nodes. And Table 6.1 (b) shows the state of LC 2, 15B, 30B, 19, 23 and 27 in order to connect N1 to N5, Left Output, N1, N2, N3 and N4. Note that as well as indicating the state of each LC (On or Off), we also show the effect, transmission or reflection that the LC causes on the next PBS.

N1 bottom Red Source	N1→N5	N1→N6	N1→N7	N1→N8	N1→Right
LC#1	ON(Trans)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)
LC#3		ON (Reflex)	OFF (Trans)	OFF (Trans)	OFF (Trans)
LC#7			OFF (Reflex)	ON (Trans)	ON (Trans)
LC#11				OFF (Reflex)	ON (Trans)
LC#15C					OFF (Trans)

(a) Connectivity N1 using the bottom red source.

N1 top Blue Source	N1→N5	N1→Left	N1→N1	N1→N2	N1→N3	N1→N4
LC#2	ON(Trans)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)
LC#15B		ON (Trans)	OFF (Reflex)	OFF (Reflex)	OFF(Reflex)	OFF(Reflex)
LC#30B			OFF(Reflex)	ON(Trans)	ON(Trans)	ON(Trans)
LC#19				OFF(Reflex)	ON(Trans)	ON(Trans)
LC#23					OFF(Reflex)	ON(Trans)
LC#27						OFF(Reflex)

(b) Connectivity N1 using the top blue source.

Table 6.1. Experiment 1, N1 is connected to all the other nodes and outputs. Table 6.1 (a) shows the state of the LCs employed in order to connect the bottom red source of N1 to N5, N6, N7, N8 and Right Output. Table 6.1 (b) shows the state of LC 2, 15B, 30B, 19, 23 and 27 for connecting N1 to N5, Left Output, N1, N2, N3 and N4.

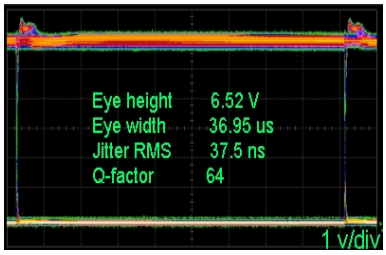
From Table 6.1 it can be observed that this first experiment requires eleven different configurations for the set of LCs. However, since each source of the N1 uses different sets of LCs, the eleven configurations can be grouped into six, by putting together one configuration from Table 6.1 (a) with another from Table 6.1 (b). Thus the number of different configurations programmed on the FPGA can be minimised.

After programming the FPGA and aligning the system, Experiment 1 analyses the eye diagram of the signals obtained at each node-output of the system.

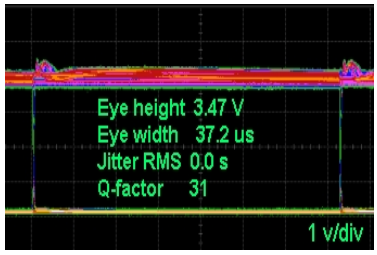
Figure 6.19 shows the eye diagram obtained from the signal coming out from the bottom red source of N1 at each node-output described in Table 6.1(a). The diagrams are presented in powered order i.e. from the interconnection that requires the minimum

number of optical stages, N1→N5, to the one that requires the maximum number, N1→Right Output.

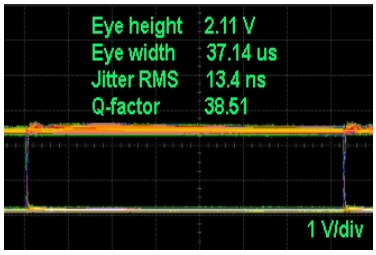
We can observe a readable eye diagram at all the outputs, which confirms the successful alignment of the system and the correct programming of the FPGA. However, though the power is reduced as the number of stages increases, the fact that the power loss at each stage is higher and more irregular than expected suggests that the system could perform better. For example, the attenuation at the second stage (N1→N6) is 2.7 dB, at the third stage (N1→N7), 2.16 dB and at the fourth stage (N1→N8), 3.4 dB. In previous experiments an attenuation of around 1.4 dB was achieved in similar conditions. This discrepancy is due to degradation of the PBSs whose wires of aluminium are easily handling damaged. The degradation of the PBSs together with problems of alignment and collimation due to the long distance interconnection explain the results obtained.



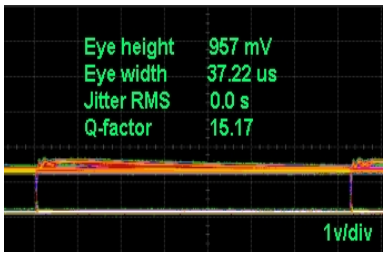
N1→N5



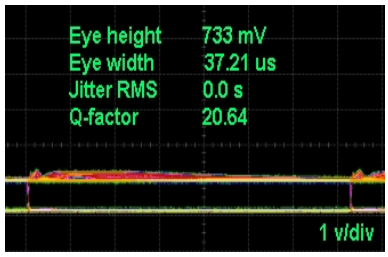
N1→N6



N1→N7



N1→N8

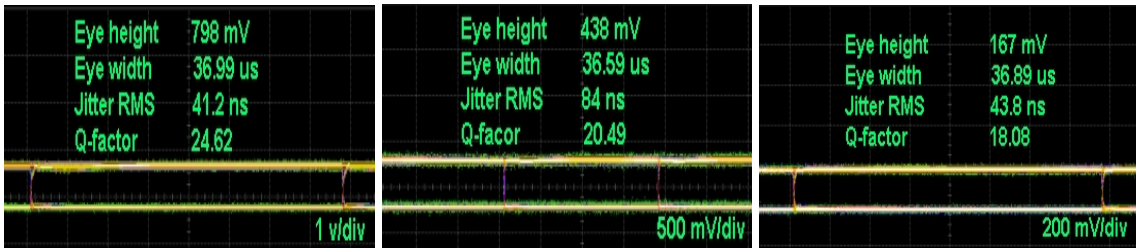


N1→Right Output

Figure 6.19. Eye diagrams obtained at the node-outputs of the signal coming from the bottom red source of N1 and using the set of configurations from Table 6.1 (a).

Figure 6.20 shows the eye diagram obtained from the signal coming from the top blue source of N1 at each node-output described in Table 6.1(a). As in the previous experiment, clear eye diagrams at each output have been successfully obtained. However, as has occurred previously and for the same reasons suggested the attenuation per stage is slightly higher and irregular than expected.

N1→N5 *N1→Left output* *N1→N1*



N1→N2 *N1→N3* *N1→N4*

Figure 6.20. Results of Experiment 1 corresponding to the set of configurations of Table 6.1 (b).

Additionally, Figure 6.21 shows the maximum crosstalk obtained in the system at the output of Node 6 when the signal was routed from N1 to N7, N8 or the Right Output. This crosstalk is low for most of the configurations, except after 5 stages, where the crosstalk and signal have similar values. The techniques proposed in chapter 4 in order to increase the Optical Modulation Amplitude of the signal at each output and decrease the crosstalk are also applicable in this case. However, it is considered that before using these techniques it would be necessary replace the damaged wire grid plates and solve the problems of collimation and alignment.

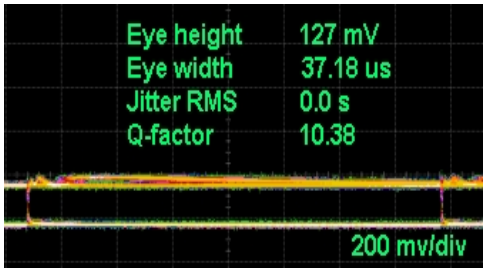


Figure 6.21. Maximum crosstalk obtained at the output of Node 6 when the signal is routed from N1 to N7, N8 or the Left Output.

6.7.2 Experiment 2 - Connectivity of Node 2

In this section a new set of configurations will be analysed. These configurations will allow the interconnection of N2 with the rest of the nodes and outputs. This experiment

will cover all the different possibilities of connectivity for one node. The tables obtained with the state of the LCs will be useful when implementing more complex topologies which are a combination of these simple configurations.

Figure 6.22 shows the connectivity of N2 using the bottom red source and the top blue source. It can be seen that the blue source is used to connect N2 to N6, N5, N1, N2 and Left Output. Additionally, the red source connects to N6, N7, N8, N4 and N3 and Right Output. As with experiment 1, this set of configurations has been chosen because it is the optimal design in terms of minimum number of stages required.

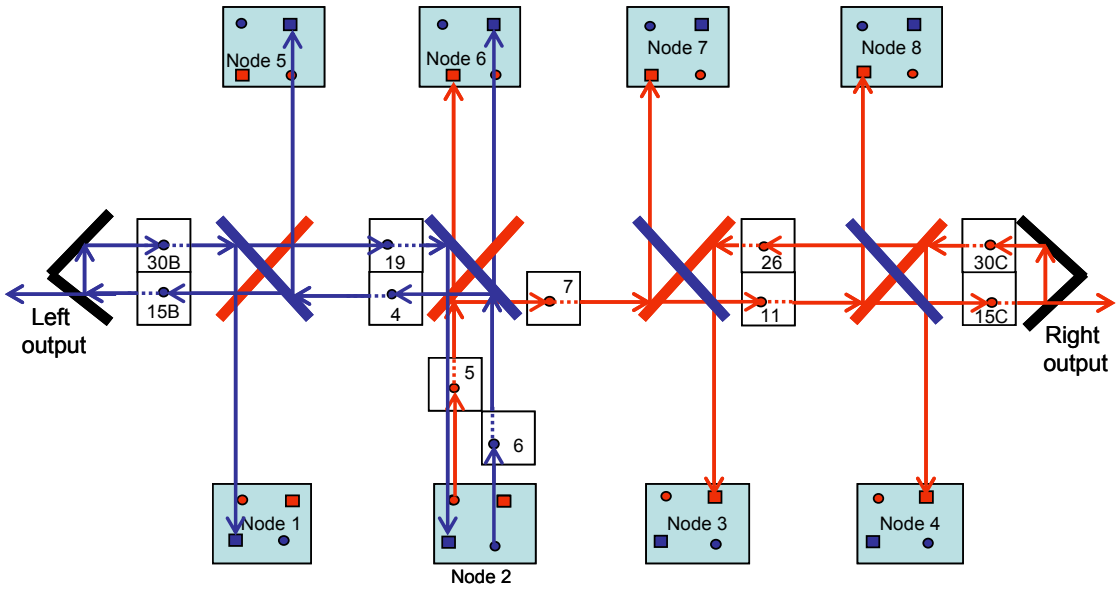


Figure 6.22. Scheme of experiment 2, where the connectivity of N2 is analysed. This diagram shows the LCs employed to connect Node 2 to the rest of nodes and outputs. The bottom red source of N2 uses LCs 5, 7, 11, 15C, 30C and 26 to connect to Nodes 5, 6, 7 and 8 and the Right Output. At the same time the top blue source can use LCs 6, 4, 15B, 30B and 19 to connect N2 to N6, N5, N1, N2 and the Left Output.

Table 6.2 summarises the state and function of the LCs involved in the connection of N2 to the rest of nodes and outputs. Table 6.2 (a) shows the state of the LCs 5, 7, 11, 15C, 30C and 26 employed by the bottom red source of N2 to connect to the other different nodes. And Table 6.2 (b) shows the state of LCs 6, 4, 15B, 30B and 19 employed to connect N2 to N6, the Left Output, N5, N1 and N2.

N2 red source	N2→N6	N2→N7	N2→N8	N2→Right	N2→N4	N2→N3
LC#5	ON (Trans)	OFF (Reflex)	OFF (Reflex)	OFF (Reflex)	OFF (Reflex)	OFF (Reflex)
LC#7		ON(Reflex)	OFF (trans)	OFF (Trans)	OFF (Trans)	OFF (Trans)
LC#11			OFF (Reflex)	ON (Trans)	ON (Trans)	ON (Trans)
LC#15C				OFF (Trans)	ON (Reflex)	ON (Reflex)
LC#30C					ON(Reflex)	OFF (Trans)
LC#26						OFF (Reflex)

(a) Connectivity N2 using the bottom red source.

N2 blue source	N2→N6	N2→N5	N2→Left	N2→N1	N2→N2
LC#6	ON (Trans)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)	OFF(Reflex)
LC#4		ON(Reflex)	OFF (Trans)	OFF (Trans)	OFF (Trans)
LC#15B			OFF (Trans)	ON (Reflex)	ON (Reflex)
LC#30B				OFF (Reflex)	ON (Trans)
LC#19					OFF(Reflex)

(b) Connectivity N2 using the top blue source.

Table 6.2. Experiment 2. N2 is connected to all the other nodes and outputs. Table 6.2 (a) shows the state of the LCs in order to connect the bottom red source of N2 to N6, N 7, N8, N4, N3 and Right Output. Table 6.1 (b) shows the state of the LCs used to connect N2 to N6, N5, Left Output, N1 and N2.

In this case there are also eleven different configurations for the LCs, grouped into six and optimizing, therefore, the number of different configurations employed by the FPGA.

Figure 6.23 and Figure 6.24 show the eye diagrams obtained from the signal coming out from the sources of N2 at each node-output and corresponding to the configuration in Table 6.2 (a) and Table 6.2 (b) respectively.

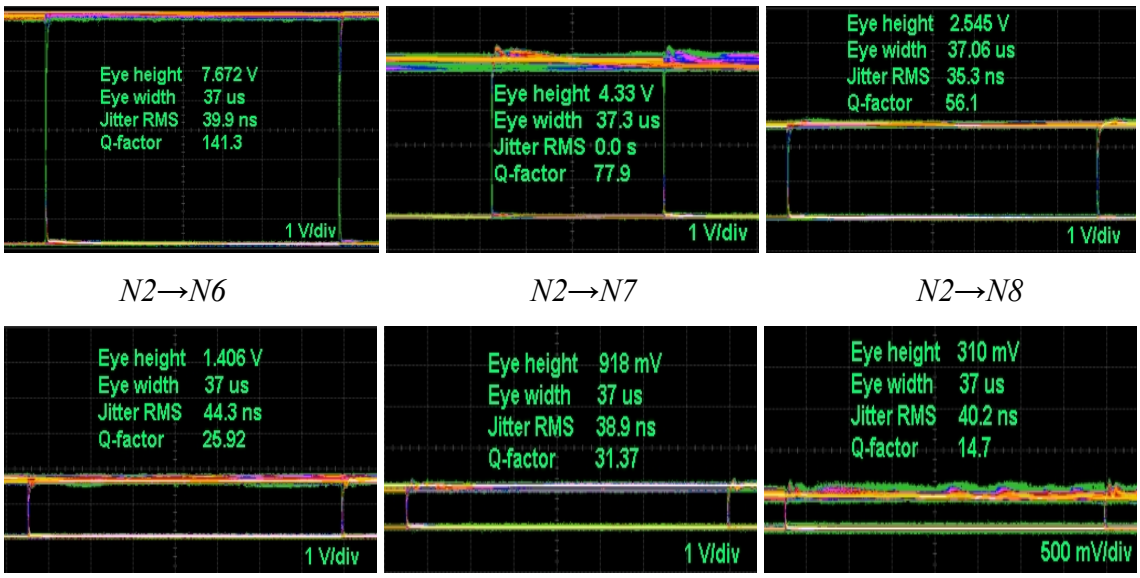


Figure 6.23. Results of Experiment 2 corresponding to the set of configurations in Table 6.2 (a).

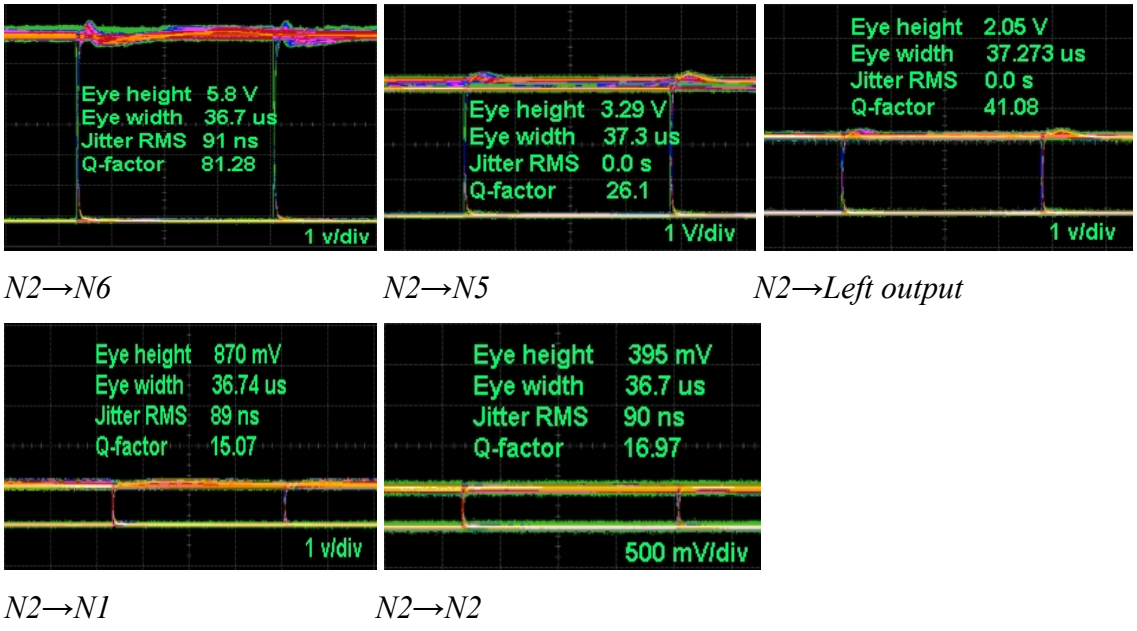


Figure 6.24. Results of Experiment 2 corresponding to the set of configurations in Table 6.2 (b).

Figure 6.25 shows the maximum crosstalk obtained in the system at the output of Node 5 when the signal was routed from N2 to the Left Output, N1 or N2. This result coincides with Experiment 1 and after 5 stages the value of the crosstalk becomes similar to the attenuated signal. Therefore, in these conditions, five would be the maximum number of stages that a signal could go through without the need to be regenerated.

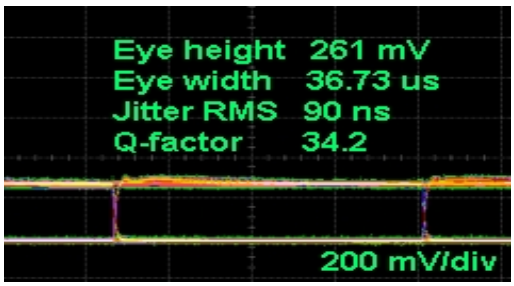


Figure 6.25. Maximum crosstalk obtained at the output of Node 5 when the signal is routed from N2 to the Left Output, N1 or N2.

These results prove that the FPGA has been programmed correctly and that, apart from the problems pointed out in Experiment 1, the optomechanical structure can be used for implementing a high variety of topologies.

6.7.3 Experiment 3 - Optical Channels Efficiency and Properties of the OCTR Architecture

In the two previous experiments we have analysed the connectivity of two different nodes individually. In this section it will be studied how various nodes can interact together. We will present different properties of the Multidirectional OH architecture that will allow us to use the same optical channel by different nodes.

These properties increase the efficiency of an optical channel and take advantage of the free space optical interconnects. Most of the free space optical interconnect systems use one optical channel for each communication link, which implies that if the communication link is not required at a certain moment or for a concrete topology, the corresponding optical channel is wasted. In our system one optical channel has the potential to be used by different communication links, increasing therefore its utility.

Signals Contact and Crossing

The first properties to be analysed are what we call signals contact and crossing. These properties allow two signals to use the same section of the PBS as there is no interaction between the optical signals. Signal Crossing occurs when two signals with different directions and coming from different sources are transmitted by the PBS using the same section of the optical material. Signal Contact occurs when the two signals are reflected by the same section of a PBS. The fact that two signals use the same section of a PBS

means that they are sharing part of the same optical channel to interconnect different nodes, increasing then the efficiency of the optical channel.

It is in these situations when the problem of a misdirected signal can become a limiting factor. Figure 6.26 shows the experiment carried out in order to analyse these properties. In this case, the five sources available in the system have been used at the same time by three nodes; N1 using two sources, N2 using two sources and N3 using the source in the top blue position.

Signal Contact has been achieved twice; the first time at the top PBS that shares the signals connecting N1 to Left Output and N2 to N5, and the second time, at the top PBS sharing the signals connecting N2 to N5 and N3 to N6. We have obtained clear eye diagrams of the three signals at the outputs of N5, N6 and Left Output. Note that there is no degradation of the eye diagrams caused by the misdirected signal. The reason for this is that for these configurations the value of the crosstalk is negligible. It is also worth pointing out how different sections of the same free space optical channel have been employed by three different signals to connect three different nodes.

The property of crossing signals, which has also been obtained in Figure 6.26, can be observed in the PBS used simultaneously by the signal that connects N1 to N7 and the signal connecting N2 to N6. In this occasion, although readable eye diagrams have been obtained, the effect of crosstalk caused by misdirected signal is clear. These configurations coincide with situations where the misdirected signal is the highest in the system.

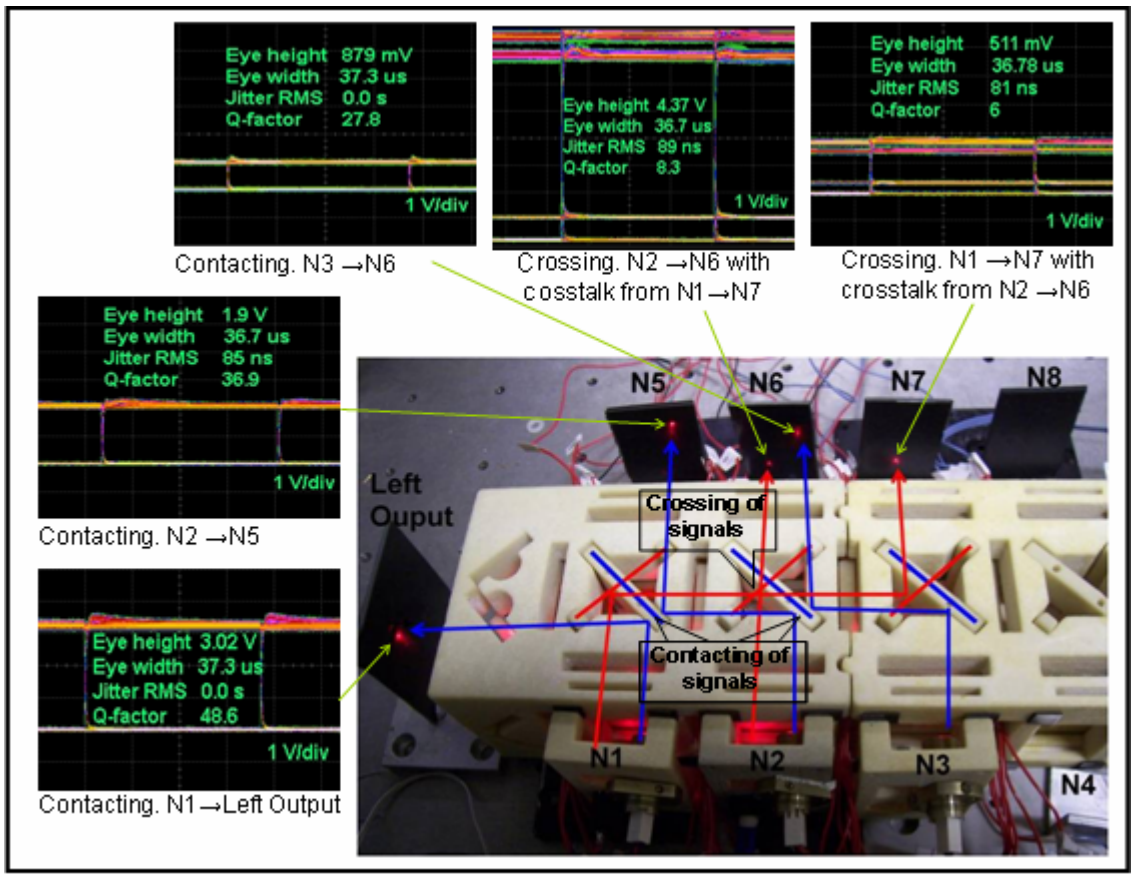


Figure 6.26. Properties of Signal Contact and Crossing. In order to understand better these two properties, the different connections established have been highlighted over the photo. For the signal showing the contacting property it has been used blue colour; N1→Left, N2→N5 and N3→N6. For the signal showing the crossing property, N2→N6 and N1→N7, it has been used red colour.

Signals Overlapping

The next property to be analysed is what we call Signals Overlapping. This property takes advantage of the polarisation characteristics of FSOI and the particular design of the multidirectional OH architecture. Thus this allows us to use not only common points of the optical channel by different signals -as the properties presented previously- but also sections of the optical channel.

In order to understand better this property Figure 6.27 shows the experiment carried out and the results obtained. The phenomenon of Signal Overlapping can be observed when two signals -one connecting N1 to N8 and another connecting N2 to N7- use the same section of the optical channel corresponding to the path situated between the two PBSs in which LC 7 is sandwiched. In this section the two signals can travel together without interfering with each other due to the fact that they arrive at the section with a different

polarisation. Irrespective of its state, LC 7 keeps both signals with a different polarisation; both polarisations untwisted, if LC 7 is On, or both polarisations twisted, if the LC 7 is Off. Finally, the two signals with different polarisations are split by the next PBS.

Figure 6.27 shows four eye diagrams (obtained by deliberately misaligning the signals) corresponding to the two signals being tested and two misdirected signals that contribute to the crosstalk. It can be observed that the value of the misdirected signal is negligible compared with the signal.

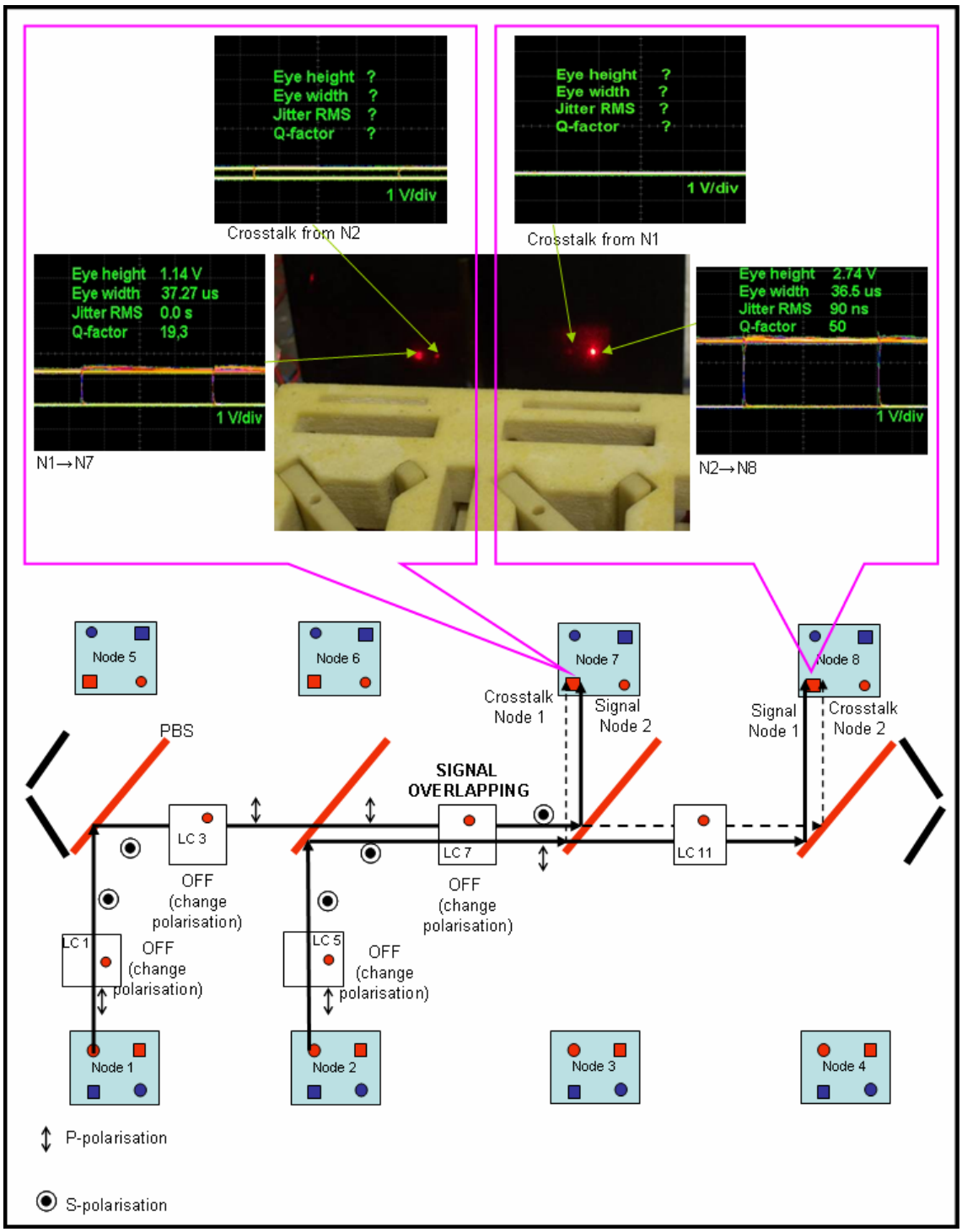


Figure 6.27. The property of overlapping is achieved using the signals that connect N1→N8 and N2→N7. The system has been deliberately misaligned in order to analyse the contribution of crosstalk to the normal signal, which in this case, is negligible.

Signal Broadcasting

Finally, we have analysed a property of slightly different nature than the previous ones but very powerful for parallel computing application. This property will be called Signal Broadcasting and allows the source of a node to be connected to different nodes at the same time by controlling the voltage of the LC employed for the interconnection. Up until now, the LC has been used only for two different states; LC Off, 0 V, and LC On, over 6 V. The LC works as a switcher, routing the signal in one direction or another. However, using intermediate values of voltage for the LC would allow us to route signal in two directions. This property is important because parallel algorithms often require a single processor to send identical data to different processors. This operation is known as one-to-all broadcasting or single-node broadcast.

By using intermediate values of voltage the LC will keep the polarisation untwisted just partially. Figure 6.28 shows the graph obtained by measuring the signal power at two different outputs. Initially, a signal coming from N2 can be reconfigured by LC 5 to connect with N8 when it is Off, or to connect with N6 when it is On. From this graph, it can also be observed how we could control the power obtained at the output of each node by manipulating the driving voltage of the LC.

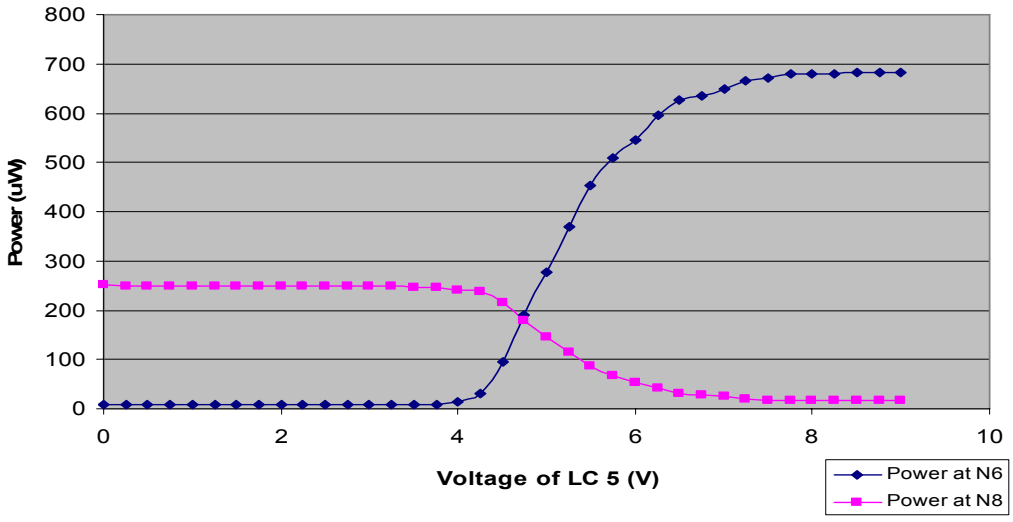


Figure 6.28. Property of Broadcasting. The difference in the maximum power obtained at each output is due to the difference in the number of stages that each signal goes through. Whilst the signal connecting N2 to N6 only uses one optical stage, the signal connecting N2 to N8 employs three optical stages. It can be observed that at about 4.75 V the value of the signal at each output is similar. However, the distribution of power at each output can be distributed as we desire.

6.8 Application of the ORCT Architecture

This section will analyse an example of an interconnect network mapped into the OCTR where some of the properties previously studied increase the efficiency of the architecture.

Figure 6.29 proposes an interconnection network where any node on one side of the architecture bidirectionally communicates with any node on the other side.

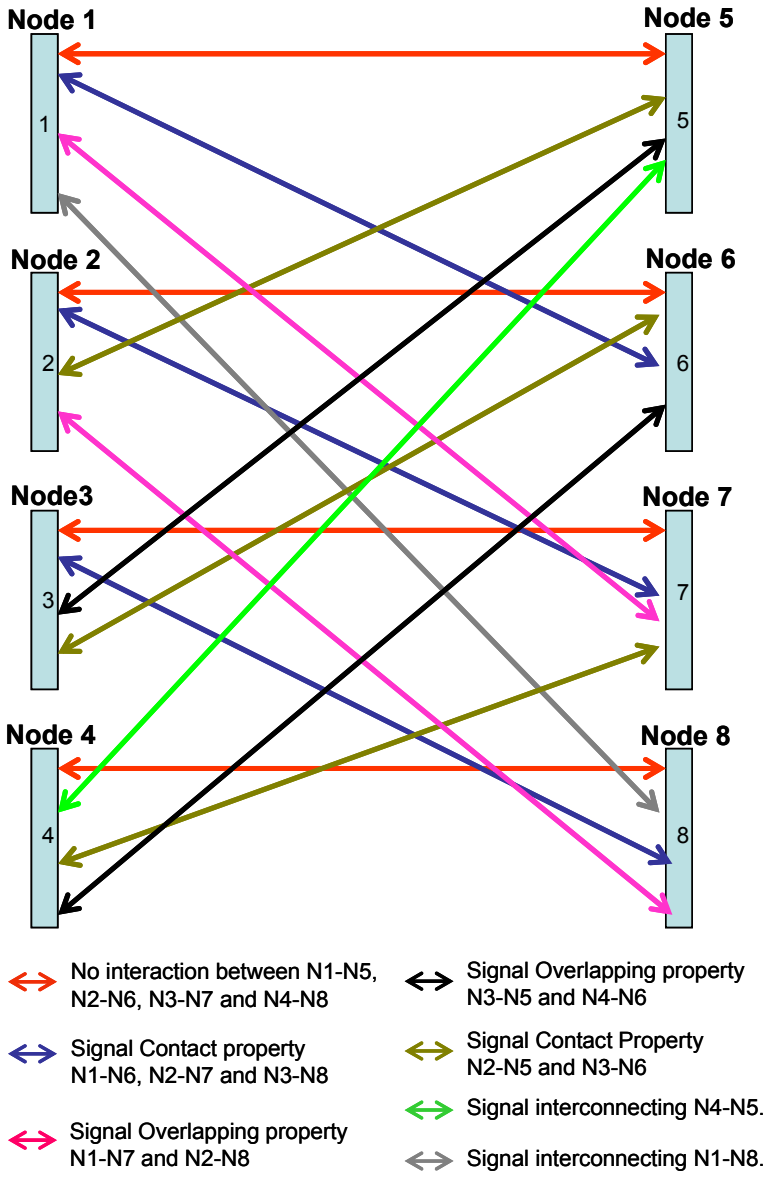


Figure 6.29. Bidirectional interconnection between the four nodes on one side and the four nodes on the other side.

Figure 6.29 shows the number of bidirectional optical signals required in order to obtain a non blocking interconnection network. A bidirectional signal is physically constituted by a pair of emitters and receivers. The signals using the same colour share the same optical channel. Thus, the number of optical channels employed in the network is determined by the number of emitters-receivers mapped into the symmetric nodes.

It can be observed that only seven channels are employed (seven emitters-receivers per node). This is due to the fact that the emitters and receivers for parallel signals are placed in the same position in their respective nodes. Such low number of optical channels can be achieved thanks the symmetry of the ORCT and the properties previously described. Another important characteristic is that, based on the analysis in the previous section, a set of rules can be created in order to establish a relationship between these properties and the schema shown in Figure 6.29:

The first rule refers to the signals that interconnect those nodes placed in front of each other. In this case the signals do not interfere with each other and therefore those emitters and receivers which have the same position can be used at the same time in different nodes. The four in red can benefit from this rule and therefore the number of different optical channels can be reduced from four to only one.

The second rule establishes a relationship between the Signal Contact property and the parallel signals in diagonal direction that are interconnecting each node on the right side of the architecture with a node on the left side, placed immediately below or above the node directly in front of the node of the right side where the signal is coming from. Thus, regarding this rule the blue signals that interconnect N1-N6, N2-N7 and N3-N8 and the brown signals interconnecting N2-N5, N3-N6 and N4-N7 employ emitters and receivers with the same position at each node.

Finally, the Signal Overlapping property applies to parallel-diagonal signals interconnecting each node on the right side with a node on the left side, placed at a distance of one node below or above the one directly in front of the node on the right side where the signal is coming from. This condition is satisfied by the pink signals, N1-N7, N2-N8, and the black signals N3-N5, N4-N6.

As a general rule it can be concluded that all parallel signals can be grouped within the same channel in the ORCT architecture.

Chapter 5 proposed the use of symmetric and square nodes, therefore a minimum of 8 emitters and receivers will be necessary in this topology in order to fulfil the packaging requirements. Figure 6.30 shows the mapping of the emitters and receivers in the nodes and an example of a possible signal configuration linking each emitter and receiver. In order to simplify the scheme only the signals going in one direction has been indicated. The mapping of the emitters and receivers of the signals going in opposite direction will be symmetric to those shown in the scheme.

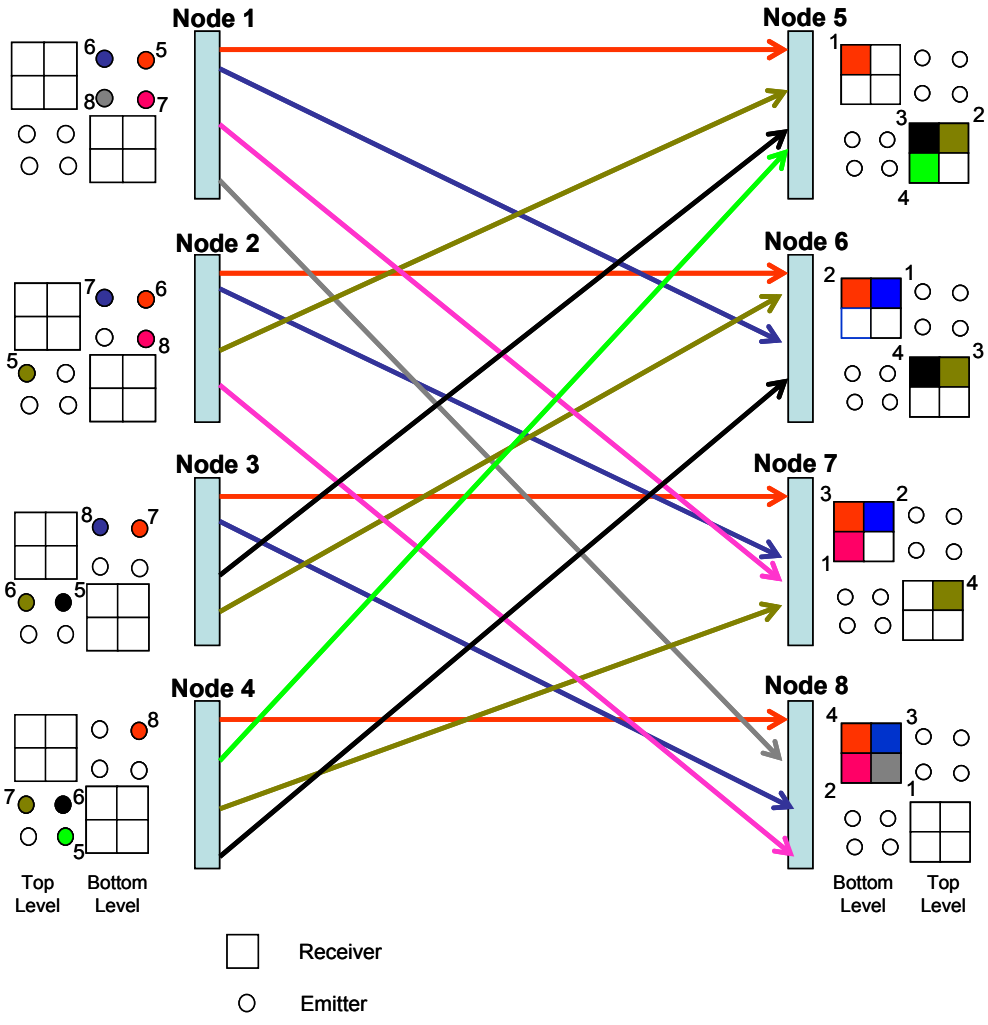


Figure 6.30 Mapping of emitters and receivers and signal configuration in one direction.

This configuration has a node efficiency of at least 50% since half of the emitters and receivers mapped are required for this interconnection network. However, the efficiency increases if the additional emitters and receivers at each node are used in order to solve problems of failure, increase the bandwidth between nodes that are already linked or create new interconnections between nodes that are not connected. In these cases the use of the Signal Crossing property can be very useful.

Other well known topologies such as the Hypercube can be easily embedded into the ORCT architecture as shown in Figure 30. However, the interconnection network previously proposed shows better performance in terms of connectivity and is relatively easy to implement in the ORCT. Regardless the topology, the same set of rules which have been defined in order to optimise the number of optical channels can be applied.

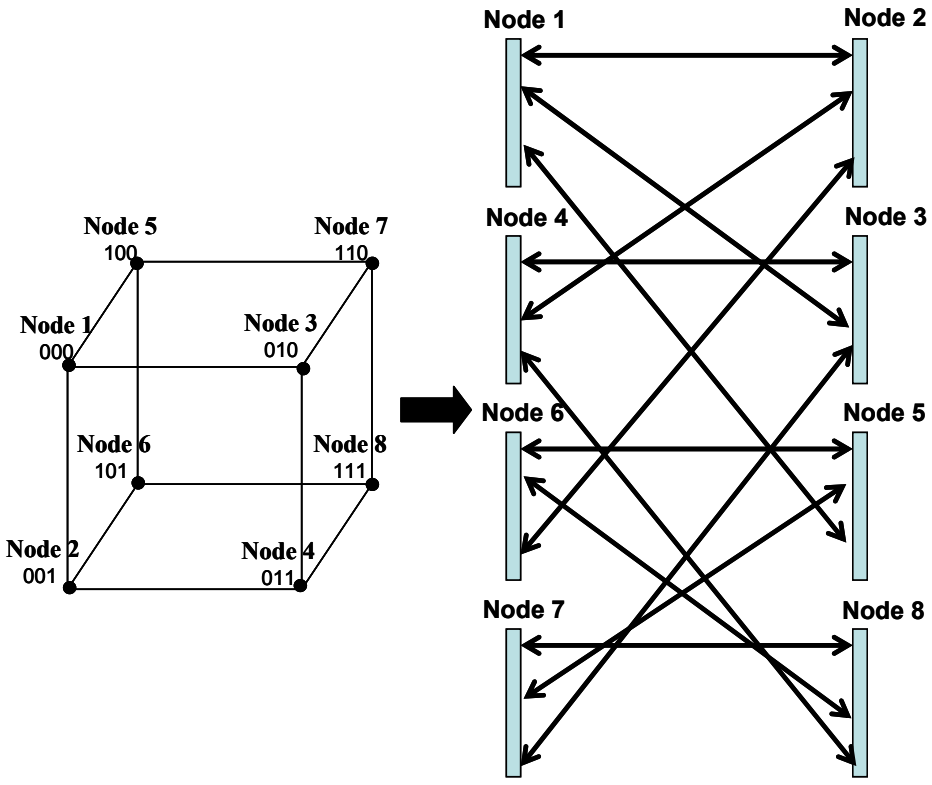


Figure 6.30. Hypercube Network mapped into the ORCT.

6.9 Conclusion

In this chapter we have presented the design, assembly and proof of work of the OCTR architecture using the RP.

The different advantages of the design using RP have also been discussed. These advantages include the easy alignment and replacement of each optical component and the possibility of scaling the number of sources and detectors per node -currently two- by just modifying the design of the source holder.

Additionally, new custom LCs have been characterised and used in order to fulfil the requirements of the architecture. Since a high number of LCs are used, a FPGA has been employed in order to control them and make the reconfiguration of channels easier. The FPGA has also been used to control the sources and thus allow the centralisation of the different components. Given the large number of reconfigurable I/Os, the FPGA can be employed for more scalable designs.

A set of experiments have been carried out in order to perform a complete proof of work of the system. The first two experiments have also provided us with the tables that indicate the states of the LCs necessary for achieving different interconnect configurations. This will be very useful for the design of future complex topologies. The last set of experiments has tested some unique properties of FSOI in general and of the OCTR architecture in particular. These properties allow us to use many interconnect configurations at the same time and thus increase the efficiency of the optical channel.

The chapter has concluded with an example of an interconnect network mapped into the OCTR where some of the properties previously presented were shown and characteristics such as efficiency and connectivity were analysed.

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Chapter 7

Conclusions and Future Work

7.1 Summary

Computer Systems will start running up against interconnection bottlenecks in 10-15 years (2015 – 2020). Optical interconnection systems have the fundamental advantages to solve this problem, but will only be used if the architectures proposed are provably impossible to build with pure electronics. FSOIs were identified as a potential solution over other optical interconnect systems and this thesis has dealt with a particular polarized beam routing system, the Optical Highway (OH), which allows the implementation of different passive networks by using LCs as reconfigurable devices.

Chapter 3 and 4 characterised in terms of polarization efficiency off-the-shelf and low cost components such as Twisted Nematic Liquid Crystals (TNLC) and Wired Grid Plates (WGP) proposed for implementing the OH. These components have proved to have more tolerance to rotational misalignment than traditional components such as PBS and QWP. A technique known as Rapid Prototyping was also used for first time as a low-cost and low time consuming tool for implementing different demonstrators of the OH. In addition to this, a matrix model based on the attenuation and crosstalk associated with each optical component was used in order to make a first estimation of the scalability of the OH in terms of maximum number of stages that the optical signal can pass through the system before it becomes too weak. This model was experimentally validated and it was proven also that the use of clean-up polarisers at the output of the system and RZ modulation code can reduce the crosstalk caused by misdirected signals and therefore increase the OSNR of the system.

In Chapter 5 the OH was designed at different levels: Node level, Optical Stage level and Architecture level. The design requirements were analysed in terms of complexity, packaging, efficiency and connectivity and different structures were then presented. The chapter concluded comparing the cost and performance of the different designs proposed.

In Chapter 6 a particular OH architecture was implemented, the Optimised Cut-Through Ring (OCTR) for interconnecting 8 nodes using four channels per node. A new set of custom TNLCs was used and a FPGA was employed in order to reconfigurate the high number of channels. The experiment carried out provided tables with the values for the LCs that defined the basic routing interconnects.

Finally, different properties of FSOI such as Signals Contacting, Crossing, Overlapping and Broadcasting were analysed and an example interconnection network was proposed.

7.2 Conclusions

In this project we have successfully built three generations of the Optical Highway using rapid prototyping technology. As a result, and based on the subsequent experiments carried out, we can conclude that rapid prototyping is a feasible technology for implementing optomechanical systems at low cost and low production time.

By using off-the-shelf twisted nematic liquid crystals and wired grid plates as optical stages in the Optical Highway we have achieved high polarisation efficiency, 95%, and large tolerance to rotational misalignment, 45°. This results in a considerable improvement with respect to previous systems that required tighter rotational tolerances, 5°.

The scalability of the OH has also been thoroughly studied. We have managed to increase the maximum number of optical stages that the signal can pass through from four to eight. By doing this, it has been possible to study more realistic designs and to implement the first OH architecture, Optimised Cut-Through Ring. This particular architecture has been employed to identify different properties of the optical channels which allow us to use free space optical interconnects more efficiently than in previous systems.

7.3 Future Work

The future plan of research in the next years will focus on the improvement of the Optimised Cut-Through Ring architecture presented in chapter 6, the search and characterisation of new materials and technologies suitable for implementing the OH and the analysis of algorithms where the potential of FSOI based architectures can be proven.

The improvement of the Optimised Cut-Through Ring architecture will consist of scaling the number of emitters and detectors to at least an array of 4x4 per node in order to implement more complex topologies such as the Completely Connected Topology. The alignment of the system will also be considered by employing new materials for implementing the RP structures which will allow achieving accuracies of about 100μm-50μm.

Research in new devices called LC-lenses will be carried out, as suggested in Chapter 5, for implementing FSOI systems. The design of the OH at higher level, Parallel Computer level, will also be developed.

Currently a theoretical study on the applications of the OH in general and the OCTR in particular is being carried out. The research is focused on the implementation of Matrix-Multiplication algorithms [1] and optical algorithms for solving a variety of basic problems in computational geometry [2] [3].

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