The Behaviour and Analysis of a Three-Phase AC-DC Step-Down Unity Power Factor Converter

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Contents

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Abstract

This thesis provides a close examination of certain aspects of a three-switch, three-phase, step-down unity power factor ac-dc converter. A dead-band, look-up table type PWM scheme is used, operating at a switching frequency of 76.8kHz. This scheme generates sinusoidal input currents and a pure dc output voltage, given the assumptions of an undistorted three-phase mains supply and infinite dc-side inductance. If the two assumptions are not met, then this results in harmonic distortion of the ac and dc-side currents.

Average current-mode control of the dc-side current is examined in detail and found to reduce the harmonic distortion as well as damping the resonant dc-side filter. The current loop can become unstable as a result of adding an input filter to the converter. This instability can be alleviated by adding passive damping components to the filter.

Two SIMULINK™ models of the converter are examined and compared with each other as regards to their time and frequency domain responses. The two models are a switching, three-phase model and an equivalent dc-dc converter model.

Mathematical expressions for the input current and output voltage and current spectra are derived for different PWM schemes. These expressions predict the locations and magnitudes of the harmonics successfully compared to a PSpice™ simulation.

A soft-switching PWM scheme is developed that theoretically reduces the total switching losses by 42%. This scheme is simulated using PSpice™ and implemented practically, where it is found to reduce the semiconductor devices' temperature rises.

Two converters are connected in parallel to drive the same load and operate from a common input filter. The PWM schemes of the converters are interleaved to reduce the switching harmonics of the ac-side input current.

Principle Abbreviations and Symbols

a_0	dc coefficient of Fourier series
A/D	analogue to digital converter
AM	amplitude modulation
a_n, a_q	n^{th}, q^{th} even coefficients of Fourier series
b_n, b_q	n^{th}, q^{th} odd coefficients of Fourier series
C_{ac}	ac-side filter capacitance (F)
CAPWM	centre aligned pulse width modulation
C_d	damping capacitance (F)
C_{dc}	dc-side filter capacitance (F)
c_n	n^{th} complex Fourier coefficients
DSBM	double side-band modulation
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPROM	erasable programmable read-only memory
E_t	total switching energy of IGBT (J)
f_e	effective switching frequency (Hz)
f_m	modulating frequency (Hz)
FM	frequency modulation
FPGA	field programmable gate array
f_s	switching frequency (Hz)
FTJ	Fourier theory of jumps
I_a, I_b, I_c	phases 'a', 'b', 'c' input ac currents (A)
I_{ac}	input current of converter and input filter (A)
I_{Cac}	current flowing in ac-side filter capacitor (A)
I_d	average diode current (A)

I_{dc}	average dc output current (A)
I_{df}	average freewheel current (A)
IGBT	insulated gate bipolar junction transistor
I_s	average switch current (A)
I_{st}	average total switch current (A)
J_n, J_q	n^{th}, q^{th} Bessel function
j_s	sign and magnitude of s^{th} jump
k	depth of flat-topping
k_{for}	forward gain of converter
k_b	bridge gain of converter
k_c	controller gain
k_f	feedback gain of controller
k_p	proportional gain of current controller
k_i	integral gain of current controller (rad/s)
k_{s1}	constant of turn-on switching loss (As)
k_{s2}	constant of turn-off switching loss (As)
L_{ac}	ac-side filter inductance (H)
L_{dc}	dc-side filter inductance (H)
m	number of jumps over waveform period
M	modulation depth
n	harmonic number
P_d	conduction power loss of diode (W)
P_{df}	conduction power loss of freewheel diode (W)
PF	power factor
PLL	phase locked loop
P_s	conduction power loss of switch (W)

P_{sw}	switching power loss of switch (W)
PWM	pulse width modulation
Q_d	series quality factor due to current feedback
Q_e	series quality factor of dc filter
Q_L	parallel quality factor of dc filter
R	load resistance (Ω)
R_d	damping resistance (Ω)
R_e	series resistance of dc filter (Ω)
r_c	series resistance of ac capacitor (Ω)
r_{cdc}	series resistance of dc capacitor (Ω)
r_l	winding resistance of ac inductor (Ω)
r_{ldc}	winding resistance of dc inductor (Ω)
rms	root-mean-square
S_a, S_b, S_c	switches a, b and c
SSPWM	soft switching pulse width modulation
SVC	static VAr compensator
$t_{c(off)}$	turn-off switching cross-over time (s)
$t_{c(on)}$	turn-on switching cross-over time (s)
t_f	fall time of PWM pulse edge (s)
t_r	rise time of PWM pulse edge (s)
T_o	overlap duration (s)
T_s	switching frequency period (s)
UPF	unity power factor
x	argument of Bessel function
x_p	angular position of p^{th} rising jump (radians)
y_p	angular position of p^{th} falling jump (radians)

V	peak phase voltage (V)
V_{ab}	phases 'a' to 'b' line voltage (V)
V_{ac}	phases 'a' to 'c' line voltage (V)
V_{bc}	phases 'b' to 'c' line voltage (V)
V_c	magnitude of carrier signal (V)
V_{dc}	average dc output voltage (V)
$V_l(\theta)$	line voltage as a function of angular position, θ (V)
V_m	magnitude of modulating signal (V)
$W_{c(off)}$	turn-off switching energy (J)
$W_{c(on)}$	turn-on switching energy (J)
z_0	characteristic impedance of output filter (Ω)
α	phase shift due to ac-side input filter capacitors (radians)
ΔI_{dc}	dc-side inductor ripple current (A)
ΔI_{dcmax}	dc-side maximum inductor ripple current (A)
Δt_{on}	on-time of a switch (s)
ΔV_c	ac-side capacitor ripple voltage (V)
ΔV_{cmax}	ac-side capacitor ripple voltage (V)
θ_p	second carrier's angular position of p^{th} rising/falling edges (radians)
θ	point of beginning of flat-top section (radians)
ϕ_p	first carrier's angular position of p^{th} rising/falling edges (radians)
ψ_p	interleaved carrier's angular position of p^{th} rising/falling edges (radians)
ω_m	modulating frequency (rad/s)
ω_s	switching frequency (rad/s)
ω_0	resonant frequency of dc filter (rad/s)

Preface

Scope of the Thesis

The thesis presents a close look at some of the practical and theoretical issues surrounding a three-phase, step-down, unity power factor ac-dc converter. The converter topology is that of a three-switch, twelve (or thirteen) diode voltage source type. New converter topologies are constantly being invented and analysed, especially resonant types, without an emphasis on the practical problems faced. This thesis attempts to examine an existing, hard-switched converter, in terms of the practical problems encountered in trying to produce a commercially viable product. To this extent, a simple controller is considered and analysed in depth using the approach that it is best to understand the problems posed by a simple control scheme in order to justify using a more complex one, should it be needed. Some of the practical problems faced include; non-sinusoidal mains voltages, a finite size dc inductor and an input filter where the input inductance is dominated by the mains inductance. Theoretical aspects considered include; average current-mode control and harmonic transfer and production.

Structure of the Thesis

The thesis consists of seven chapters. **Chapter 1** introduces the need for converters of the type considered in this thesis and looks at the question of power supply harmonics. **Chapter 2** details the hardware used to implement the converter and produces some design equations and a PSpice™ simulation that describe its steady-state behaviour. **Chapter 3** is concerned with obtaining mathematical expressions for the converter input and output harmonics for the cases of; a single converter, parallel connected converters and a soft-switching converter. These expressions are compared with PSpice™ simulation results. Also considered in this chapter are the effects of; supply voltage flat-topping harmonic production, finite dc inductor harmonic production

and transfer of harmonics from the ac/dc and dc/ac sides of the converter. **Chapter 4** is about the average, current-mode control of the converter and its modelling. A three-phase switching model and dc-dc simple average model are developed. A number of frequency and time responses are considered and explained, especially the effect the input filter has on stability. Damping the converter dc filter and reducing the harmonics produced by flat-topping are both advantageous effects of closed-loop average current-mode control that are examined. The input filter is passively damped and this is modelled successfully when compared with the practical results. **Chapter 5** considers the practical results and issues in the parallel connection of two converters to drive a common load. **Chapter 6** introduces a new soft-switching PWM technique that reduces switching losses and describes the implementation of it on the practical test-rig and via a simulation. **Chapter 7** details the overall conclusions of the thesis, scope for further work and the author's contribution.

CHAPTER 1 - Introduction

1.1 The Power Quality Problem and its Background

Power Quality

Power quality is a measure of how stable, reliable and distortion-free the utility voltage is. Power quality in electrical distribution networks has, in recent years, become an issue of ever-increasing importance. It is the proliferation of non-linear loads connected to the mains that reduces the power quality of the supply. Examples of power electronic non-linear loads are; computers, mill drives, locomotives, arc furnaces and electrochemical plants. Power quality affects the user, supplier and electronic equipment designer. A key paper [1.1] provides an overview of the situation, lists some problems and remedies and provides an extensive bibliography.

Power, Distortion and Displacement Factors

The power factor (PF) of a load fed from an ac supply is defined by [1.2]

$$PF = \frac{\overline{P}}{V_{rms} I_{rms}} \tag{1.1}$$

where V_{rms} is the root-mean-square (rms) supply voltage, I_{rms} is the rms supply current and $\overline{P}$ is the mean power drawn from the supply. It is insufficient to define the PF as the cosine of the displacement angle, as non-linear loads draw non-sinusoidal current from the supply. If the supply voltage is assumed to be sinusoidal, then there is no power associated with the harmonic currents and the mean power is therefore given by

$$\overline{P} = V_{1(rms)} I_{1(rms)} \cos\phi_1 \tag{1.2}$$

where $V_{1(rms)}$ is the fundamental supply voltage, $I_{1(rms)}$ is the fundamental supply current and ϕ_1 is the fundamental displacement angle. Substituting Equation (1.2) into (1.1) gives

$$PF = \frac{I_{1(rms)}}{I_{rms}} \cos\phi_1 \qquad (1.3)$$

where $I_{1(rms)}/I_{rms}$ is the distortion factor and $\cos\phi_1$ is the displacement factor.

To achieve unity power factor (UPF) operation, the supply current drawn should be a pure, sinusoidal waveform that is in-phase with the pure, sinusoidal voltage supply (i.e. $I_{1(rms)}/I_{rms}=\cos\phi_1=1$). A distortion factor of unity and a displacement factor of unity represents the most efficient use of the utility supply system. The displacement factor measures the amount of reactive power being consumed. A displacement factor of unity is the ideal case and corresponds to zero reactive power.

Harmonics

Harmonics are sinusoidal voltages or currents that are integer multiples of the fundamental frequency, which in this case is the 50Hz mains power supply system. Harmonics are a major cause of the distortion factor being less than unity and originate from the non-linear characteristics of power system loads. Harmonics cause various undesirable effects [1.3] including; heating of transformers, capacitors and electrical machines, failure of and disturbances to sensitive electronic equipment, telephone interference, performance deterioration in circuit breakers and protection circuits and torque pulsations and vibration in electrical machines.

Sub-cycle and High Frequency Distortion

Other distortion components include sub-cycle distortion, otherwise known as "flicker" and high frequency distortion called electromagnetic interference. Flicker is caused by high power dynamic loads generating unacceptable voltage drops across the power distribution network due to large, transient reactive current demand.

Electromagnetic interference (EMI) is often caused by the fast switching of large voltages and currents by power electronics devices.

1.2 Power Quality Regulations

Prior to 1996, a bewildering range of harmonic standards existed, from the British Standards (BS), to German VDE Standards, Military Standards (MIL), CISPR Standards for the telecommunications market and European (EN) Standards. Since the beginning of 1996, all electrical goods connected to the mains and sold in the European Union (EU) must carry the "CE" mark to show that the good meets certain harmonic emission and safety standards. The CE mark's function is stated in the EU directive 93/68/EEC. The reasoning behind introducing the mark is to unify the existing standards to enable EU electronic equipment manufacturers to sell their equipment in any EU country, with minimal changes to meet the different countries' regulations. The electromagnetic compatibility (EMC) emphasis behind the CE mark is to eliminate the susceptibility of the equipment to emissions of a certain level and to reduce the emissions of the equipment itself. The EMC directive is found in 89/336/EEC.

Certain items of equipment have their own dedicated EMC standards, e.g. uninterruptable power supplies are covered by EN 50091-2 and household appliances, such as electric tools, by EN 55014-1. The standards of greatest interest, from the general point of view of equipment connected to the utility are; EN 50081-1 for residential and light industry products and EN 50081-2 for equipment used in an industrial environment.

EMI Mechanisms

There are three fundamental coupling mechanisms for electromagnetic disturbances [1.4].

(i) Galvanic coupling, where the disturbing current flows in a common circuit impedance.

(ii) Coupling via the "near" field, i.e. capacitative or inductive coupling, where the distance between the two conductors is much less than $\lambda/2$ metres, where λ is the wavelength of the electromagnetic radiation.

(iii) Coupling via the "far" field, i.e. the distance between the two conductors is much greater than $\lambda/2$ metres.

For power electronics equipment, the first method of coupling is the most significant, followed by the second and lastly the third. CE marked equipment should not be susceptible to certain levels of these disturbances, nor should they generate disturbances above certain limits set out in the EMC standards.

1.3 The Improvement of Power Quality

There are four often-used methods by which power quality can be improved; tuned impedance filters, passive filters, dynamic filters and input waveshaping converters.

1.3.1 Tuned Impedance Filters

These filters take the form of a connection of an inductor, parallel capacitor and/or resistor to the mains lines, Figure 1.1.

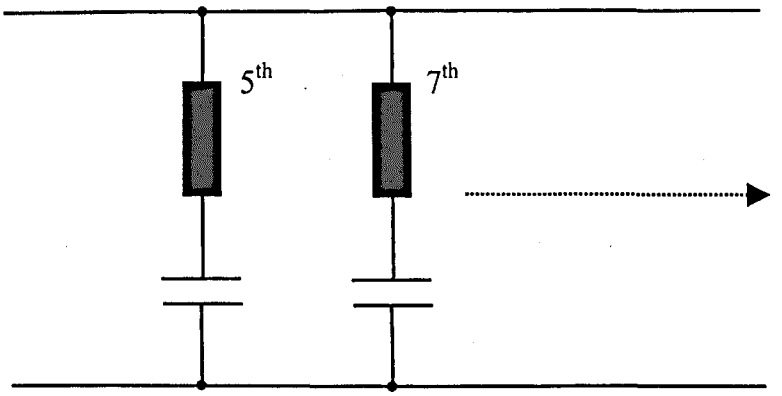

Figure 1.1 – Tuned Impedance Filters

Several of these tuned filters can be connected in series to the line, each filtering a different frequency e.g. 5^{th}, 7^{th} and 11^{th}, 13^{th} harmonics, etc. An example of an application is on an off-shore platform, where three tuned filters were added to provide low impedance paths for the current harmonics produced by thyristor drilling drives to prevent the harmonics from entering the subsea cable connected to the remotely located generators [1.5]. The tuned filters achieved their aim, but shifted the resonance problems to other locations in the frequency spectrum, potentially causing problems. In general, curing one resonance problem with a tuned harmonic filter may introduce another.

1.3.2 Passive Filters

A typical application would be an uncontrolled, single-phase ac-dc diode bridge rectifier, Figure 1.2.

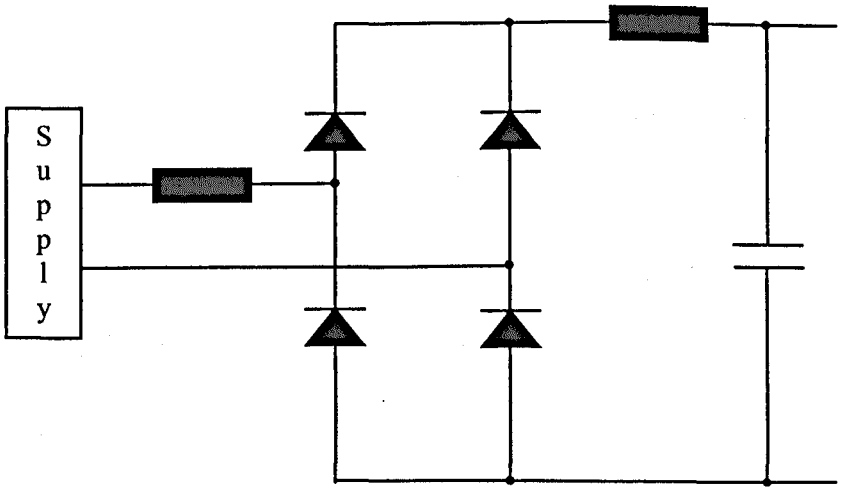

Figure 1.2 – Single Phase Rectifier with Passive Filters

With carefully chosen inductors and capacitors, the power factor is improved and the harmonic standards can be met [1.4, 1.6]. Passive solutions, when compared with active solutions, have the advantages of; simplicity, robustness and reduction of the high frequency EMI. The harmonic limits for high frequency EMI are much stricter compared with the low frequencies e.g. EN 6055 specifies that only 4μA at 500kHz can flow through the standard mains input impedance of 50Ω [1.6]. Active solutions, whilst reducing the low frequency harmonics, shift the problem to high frequencies at around the switching frequency and beyond. It is possible that a high cut-off frequency, multi-stage input filter will be needed to reduce the harmonics below the harmonic standard limits. The disadvantages of passive filters are that they are heavy and bulky and require range switching if both the 230V and 110V ac mains supplies used in different countries are to be catered for.

1.3.3 Dynamic Filters

Dynamic filters [1.7] are able to improve the power quality of a network affected by sub-cycle disturbances and/or harmonics. One such example is the static VAr compensator (SVC) which controls the flow of reactive power in an electrical system. Active SVC's feature inductors and/or capacitors in series with two back-to-back, parallel connected thyristors connected to the mains lines.

Figure 1.3 shows a thyristor switched capacitor (TSC) type SVC and a thyristor switched reactor (TSR) type SVC. (N.B. The TSC includes an inductor to limit the rate of rise of current through the thyrsitors.) The capacitor bank is seperated into smaller units and switched in and out to cancel the inductive (leading) power factor. A TCR is then used to cancel the surplus capacitive current in order to achieve unity power factor.

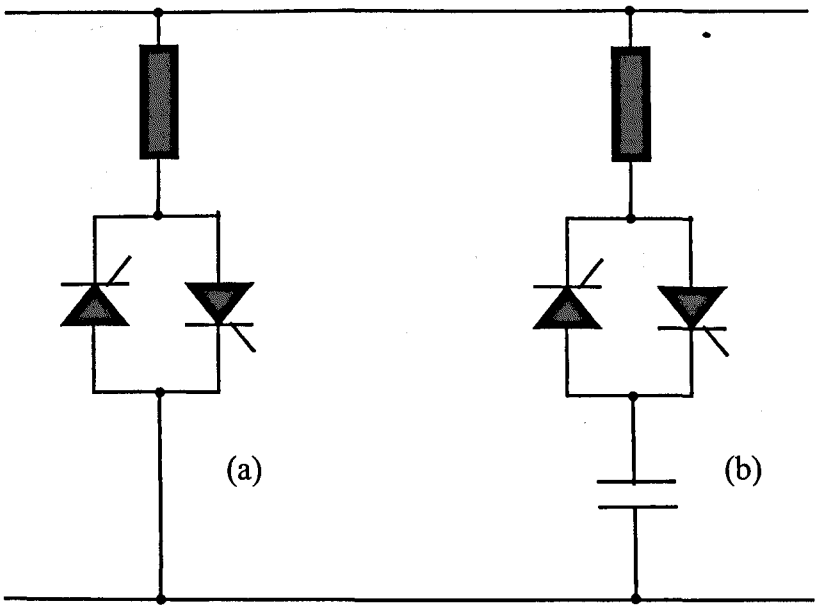

Figure 1.3 – (a) Basic TCR and (b) Basic TSC

For SVCs, altering the firing angle of the thyristors controls the reactive power flow. The disadvantage of these systems is their sub-cycle response times and the generation of thyristor-associated harmonics, which themselves have to be filtered.

Another type of SVC uses an inverter, where the dc-side is connected to a dc supply (provided by a capacitor) and the ac-side is connected to the mains lines. The output currents are controlled in such a way as to give the required reactive power compensation. By employing suitable detection circuitry, harmonics can also be compensated for, as this type of converter using fast transistor switches and high frequency PWM can respond quickly enough to cancel the harmonics. The advantage of these SVCs over input waveshaping converters is that only the harmonic power is processed, leading to lower power losses. The disadvantage of SVCs is that they do not provide an ac-dc conversion process and so if this is required another converter is needed.

1.4 Input Waveshaping Converters

Introduction

A large body of work exists on waveshaping converters. The idea behind the technology is to control the input current to be sinusoidal and in-phase with the ac supply voltage and provide a controllable ac-dc voltage conversion process. Some waveshaping converters provide a variable dc voltage output as well as waveshaping the input current. Other waveshaping converters provide the waveshaping, generate a constant dc voltage output and are followed downstream by a dc-dc converter to generate the required dc voltage/s.

1.4.1 Single-Phase Waveshaping Converters

One of the most popular topologies for single-phase supply systems is the UPF ac-dc boost converter followed by a dc-dc step-down converter [1.8], Figure 1.4.

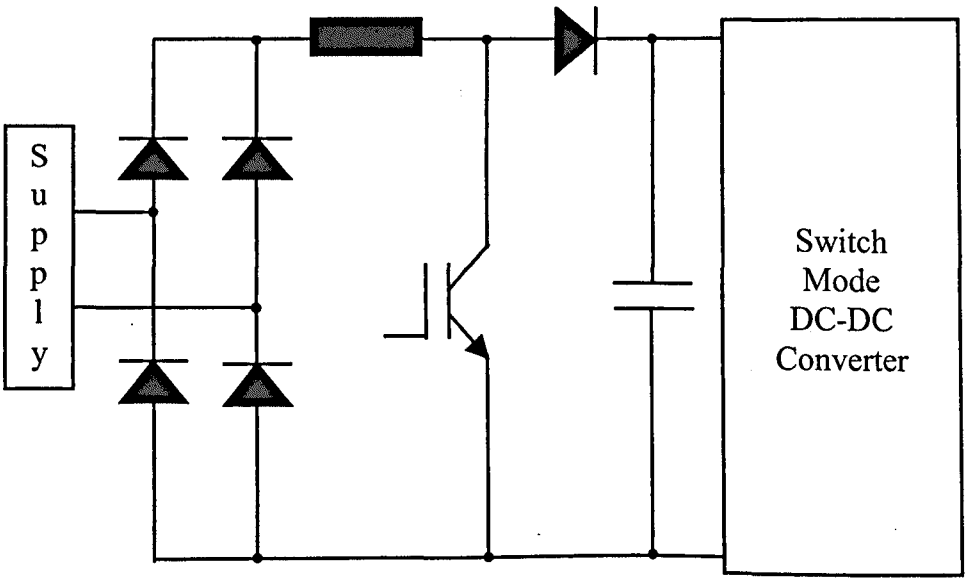

Figure 1.4 – Single Phase Boost UPF and DC-DC Converter

A study was carried out into using this technology in a typical office environment [1.9] in order to reduce the costs due to harmonic-related losses in the mains system. The study found that installing such converters within non-linear loads such as personal computers was cost effective, yielding a three-year payback period. At the present time, this

solution is not usually adopted due to the increased cost and complexity of the power supply. In the future this may change, as standards are enforced and increased device integration leads to lower costs. Researchers and power supply manufacturers are working on single-stage, single switch, UPF converters with isolated step-down outputs to make the technology commercially viable.

1.4.2 Three-Phase Waveshaping Converters

The emphasis of this thesis is on three-phase, ac-dc UPF converters and these are now briefly reviewed. The three basic converter types consist of; the boost converter, the flyback converter and the buck converter. Resonant-type converters are not considered, as the resonance is used to reduce switching losses and is not a fundamental requirement.

The Boost Converter

The standard three-phase boost converter uses a bridge of six switches connected to six anti-parallel diodes with large ac inductors and a capacitor connected to the dc output, Figure 1.5.

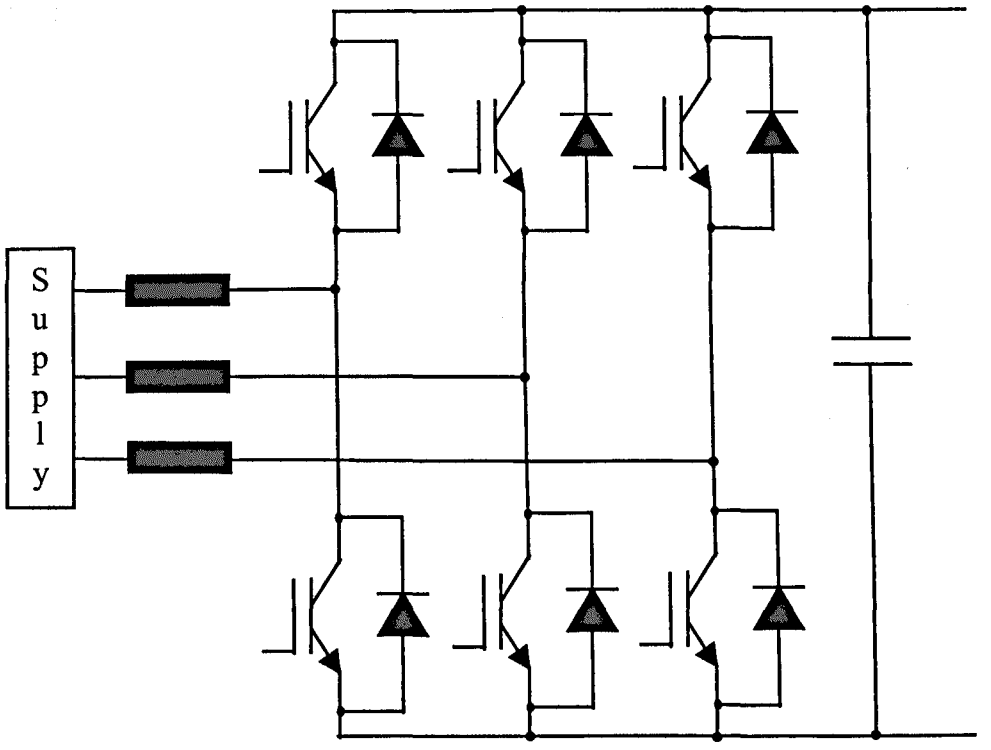

Figure 1.5 – Three-Phase Boost UPF Converter

It is capable of supplying leading or lagging power factor power over the full ±180° range of power angle [1.10]. An application of this topology would be in providing the dc link voltage for an induction motor drive. Using a sinusoidal PWM scheme, the input currents are capable of being high-quality sinusoids. The input current inherently has a low switching ripple-current component to it, making the filtering requirements lower than that of the buck or flyback converters. An change to this converter was made by the addition of one diode in series with the positive dc bus, between the bridge and output capacitor[1.11]. Adding this fast, soft recovery diode has the following effects; reduced anti parallel diode reverse recovery as the anti-parallel diodes often have poor reverse recovery characteristics, eliminating the shoot-through condition when two devices in the same bridge leg are turned on simultaneously and in the easy implementation of soft-switching. The disadvantage to adding this diode is that it prevents reversing of the load current for reverse power flow operation.

A one-switch version exists [1.12] which takes the same form as the single phase boost converter, Figure 1.4, only with a three-phase diode bridge rectifier front end.

The control scheme implemented reduced the dc-side voltage ripple, the compromises being that the input currents are not sinusoidal and the regenerative capability is lost. However, the harmonic content of the input current is reduced compared to that of a standard three-phase diode bridge rectifier. Another one-switch converter [1.13], generated sinusoidal input currents, but at the expense of increased stress of the switching device and an increase in the high frequency switching ripple of the ac input currents. Commercially, these one-switch converters have not found acceptance, with designers preferring the conventional six switch configuration.

The Flyback Converter

Flyback converters are capable of both step-up and step-down operation. Their operation is similar to that of the buck converter and the input current contains a large switching ripple-current component. The six-switch topology is shown in Figure 1.6.

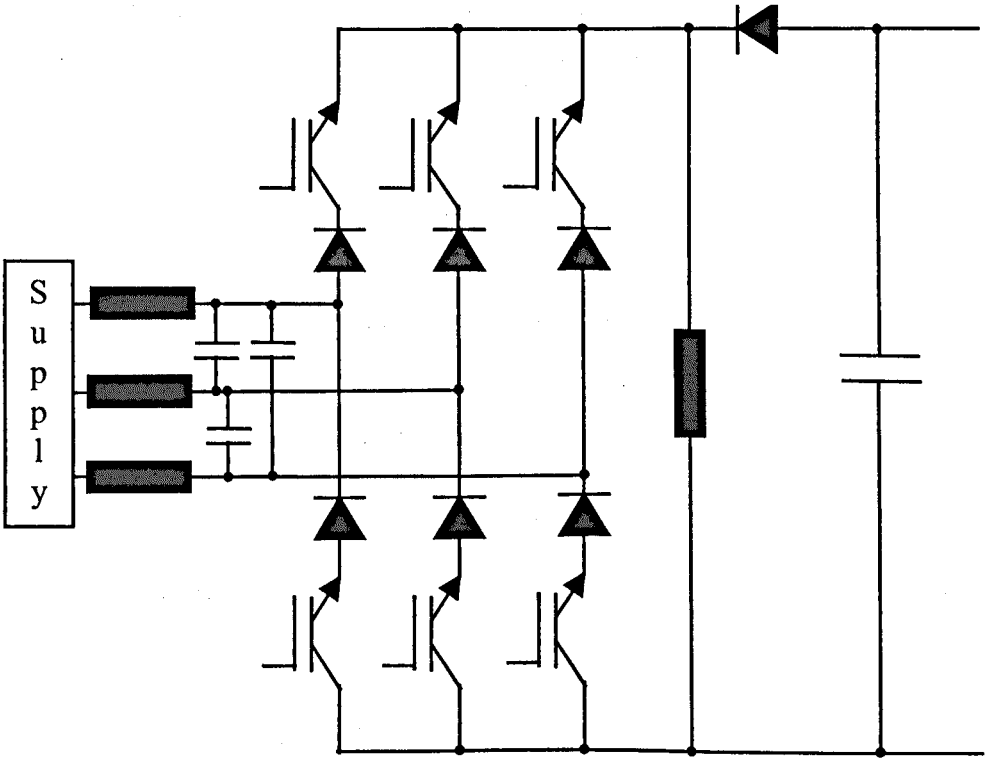

Figure 1.6 – Three-Phase Flyback UPF Converter

Little work has been performed on this topology for use in UPF converters. A four-switch converter was proposed [1.14] which has a simple control scheme to yield

sinusoidal input currents. A three-switch converter [1.15] utilising twelve diodes and featuring sinusoidal input currents was also reported.

The Buck Converter

The buck converter is used when a voltage output less than the input is required. A six-switch converter [1.16] was reported in the literature featuring modulation depth and angle control, Figure 1.7.

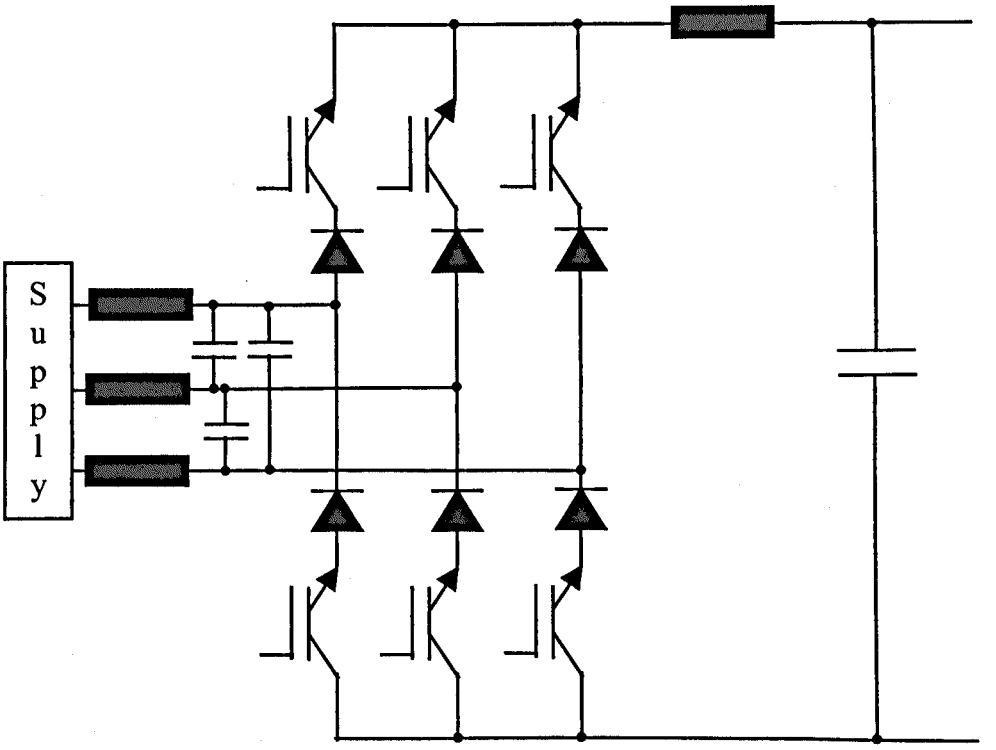

Figure 1.7 – Three-Phase Buck UPF Converter

The buck converter is only capable of reverse power flow if the output voltage reverses. The disadvantage of the buck compared to the boost converter is that the former requires an LC input filter as standard, as the input current is inherently discontinuous. This filter degrades the input power factor of the converter by producing a phase shift. The phase shift can be compensated for using the converter controller, by getting it to produce a power component of the opposite sign to cancel the input filter's effect. The input filter can also be responsible for an unstable or oscillatory transient response. This can be tackled by incorporating the filter state variables into a sophisticated control

scheme [1.17] to damp the oscillations, as well as controlling the active and reactive power flow.

A three-switch, ac-dc UPF buck converter capable of operating in one power quadrant (i.e. reverse power flow is not possible) was proposed [1.18] that can deliver pure sinusoidal input currents, Figure 2.1. This topology halves the number of active switches used, (and hence halves the number of gate-drive circuits employed) at the expense of doubling the number of diodes from six to twelve. A disadvantage is that the maximum phase displacement of the input current is reduced to ±30°, but this is probably enough to compensate for the phase shift of the input filter, if so desired. Investigation into this converter topology was continued [1.19] by using steady-state analysis and practical, step-change transient tests.

1.5 The Converter Topology Investigated in this Thesis

The research on the three-switch converter is continued because it looks like a promising topology. Halving the number of active switches whilst retaining the ability to deliver sinusoidal input current is an attractive feature. The aim of the forthcoming chapters is to provide a rigorous analysis of the converter's practical features such as the average current-mode control scheme, the effect of the input filter as regards system stability and converter harmonics.

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CHAPTER 2 – Converter Hardware and Basic Analysis

2.1 Hardware

Description of the Major Components

The hardware needed for the three phase converter can be summarised as follows; a three-phase ac-dc bridge consisting of thirteen diodes and three IGBTs, a digital PWM pulse generation circuit using a Xilinx™ FPGA, gate drive circuits, a synchronisation circuit to lock the PWM to the mains, a control circuit that implements analogue dc-side current control, a three-phase ac-side input filter and a dc-side filter. A schematic representation of the bridge, filters and resistive load is shown in Figure 2.1

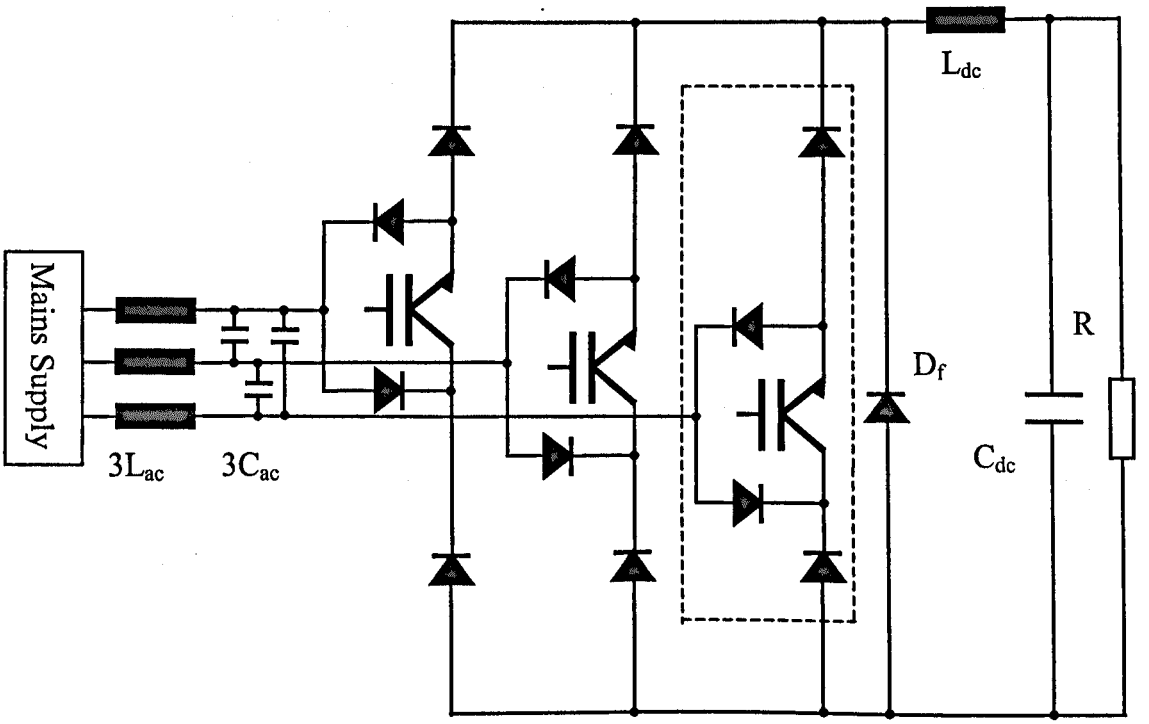

Figure 2.1 – Three-Phase AC-DC Step-Down Converter

The IGBTs used are the ultra fast type IRGP440U and the diodes are all the fast recovery type DSEI 30-06A. The dc filter has nominal values of L_{dc}=500μH and C_{dc}=4700μF whilst each component of the ac filter has nominal values of L_{ac}=50μH and

C_{ac}=3μF. The switching frequency used is as high as possible in order to minimise the size of the reactive components, i.e., f_s=76.8kHz when the mains frequency is f_m=50Hz.

Basic Converter Operation

The bridge is essentially made up from three controlled ac-dc converter blocks, one of these being shown dotted in Figure 2.1. These blocks allow the bi-directional flow of current through the input terminal (which is connected to the ac filter inductor) and unidirectional current in or out of the other two terminals. In terms of modelling the converter, the input to the bridge looks like a voltage source due to C_{ac} and the output of the bridge looks like a current sink because of the large inductor, L_{dc}. If the dc inductor is large enough, then the dc-side current is constant with no ripple. Every time two IGBT switches are closed, a pulse of constant amplitude current flows from the ac to the dc side. If no switches are closed then the current flows around the freewheel diode path provided by D_f. Whilst D_f is not strictly necessary, (an alternative freewheel path can be provided by holding on one of the IGBTs) it was added because it reduces the power loss and makes for a more robust freewheeling state that is independent of any active semiconductor devices. If the switches are switched using a sinusoidal PWM scheme, then the input current will be sinusoidal and a pure dc voltage is created at the bridge output containing no low frequency harmonics. The PWM scheme is an interleaved one, i.e. in one switching period, two on-off transitions are made by two different switches. It is possible to parallel converters to drive the same load and yet to share the same input filter and output capacitor. The PWM patterns of the two converters are interleaved, i.e. they are working in antiphase. This has the advantage of doubling the effective frequency seen by the input filter thereby allowing a decrease in its size.

2.2 Dead-Band Centre-Aligned PWM Scheme (CAPWM)

Operation of PWM Scheme

The PWM scheme used has to be able to deliver voltage pulses to the dc filter, that, when averaged, give a pure dc result and likewise the average of the current pulses drawn from each of the three phases must be sinusoidal and in-phase with the supply voltages to give unity power factor. The dual-carrier, centre-aligned, triangular modulation scheme employed belongs to the dead-band category of PWM methods and is shown in Figure 2.2 over one mains cycle. An advantage of such a scheme is that it reduces the effective switching frequency and hence switching loss by one third compared to sinusoidal PWM, because for one third of any device's conduction time it is held on, instead of being switched. This will also reduce the switching harmonics by one third [2.1]. Referring to Figure 2.2, the phase of the carrier for each PWM signal is periodically reversed so that the input current spectrum contains no component at the switching frequency, ω_s, but rather there are two carrier frequencies positioned at $\omega_s \pm 2\omega_m$, each of these having a reduced magnitude compared to the case when the pulses are not positioned in this way. For example, carrier signal "A" reverses at 120° and 300°.

Considering each 60° portion of the PWM pattern in turn it is seen that the same parts of the modulating waveforms are used repeatedly, namely, the 0-60° and the 120-180° portions of a sinusoid. The magnitude of the voltage phase that is largest is the phase whose IGBT is held on for that 60° period. The other two phases are switched and either push/draw current into/out of the highest voltage magnitude phase.

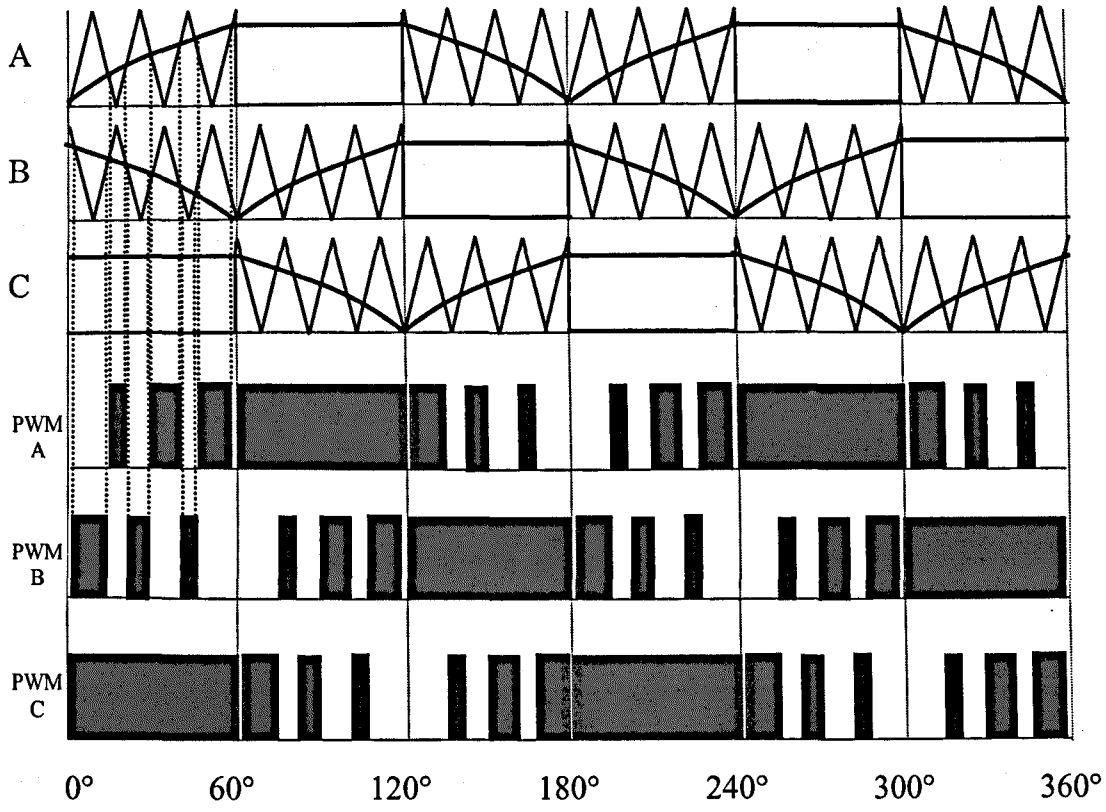

Figure 2.2 – Three Phase CAPWM Scheme

The PWM generation method used is that of comparing the triangular carriers to a sinusoidal modulating reference waveform. This comparison is performed off-line and the resultant pulse widths stored in an EPROM. The magnitude of the reference is termed the modulation index, M, where $0 \leq M \leq 1$. Only a 60° portion of PWM widths need to be stored because of the symmetry, each 60° portion being described by 128 PWM pulses. M is quantised into 256 discrete values, thus 256 tables each containing 128 bytes of information are stored on the EPROM, a total of 32kB. In order to describe a 50Hz sinusoid, each EPROM-stored sample must be addressed at a rate equal to the number of samples in 360° multiplied by 50Hz which is 128*6*50=38.4kHZ. This is illustrated in Figure 2.3, where each reference value is held for two carrier periods, where the triangular carriers have a frequency of 76.8kHz.

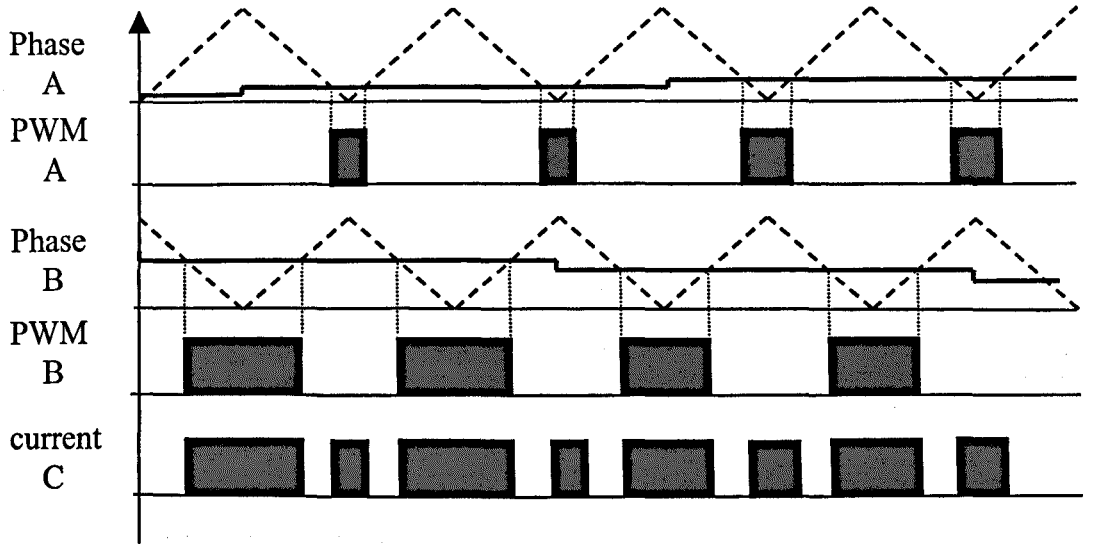

Figure 2.3 – Production of CAPWM pulses

Figure 2.3 shows the two references being compared to the two cophasal triangles resulting in two PWM patterns labelled "PWM A" and "PWM B". The pulsed waveform "current C" shows the resultant, interleaved current pulses pushed back into phase C, where phase C is the phase that is held on during this particular 60° cycle.

CAPWM Scheme Implementation

The CAPWM scheme is implemented using a Xilinx™ 3042 FPGA and is capable of controlling two separate converters. The modulation indices for each converter are determined by the 8-bit numbers read in using two A/D converters that sample the current demand signals from the analogue controllers. The operation of two converters, each 180° out of phase, driving a common load is considered in Chapter 5.

It is necessary that the PWM signals be locked to the 50Hz mains voltage so that the input currents are in-phase with the mains voltages. This is accomplished by generating a squarewave signal from the zero crossings of one of the mains voltage phases. This signal is then used to produce the clock signals for the PWM at 76.8kHz and for the Xilinx clock frequency at approximately 19.7MHz by using two phase

locked loops (PLL), as illustrated in Figure 2.4. N.B. The divide by 1536 counter was implemented by cascading a divide by 256 counter with a divide by 6 reset-counter.

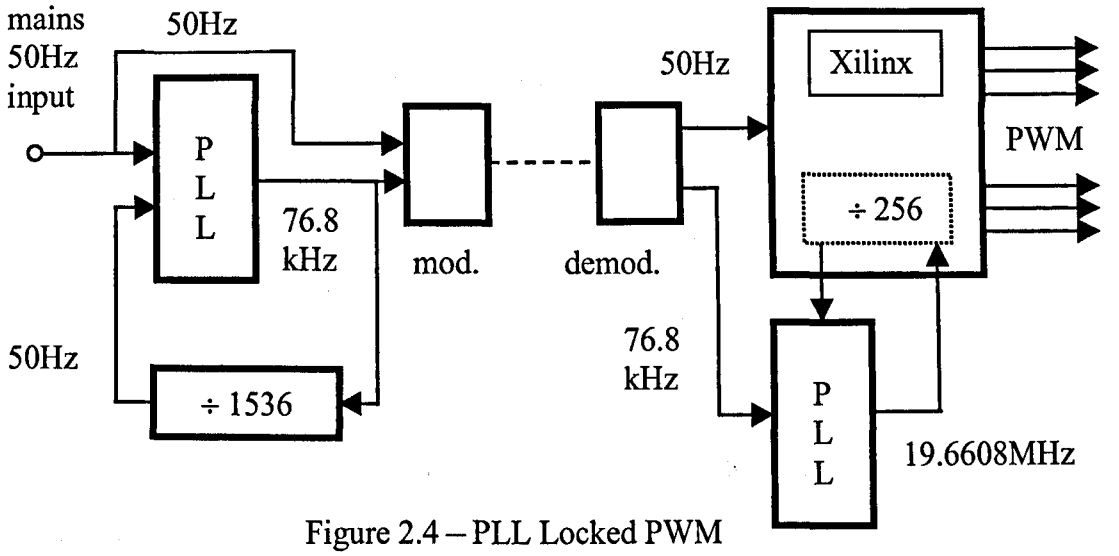

Figure 2.4 – PLL Locked PWM

The purpose of using PLLs is that the mains frequency can show some deviation from 50Hz, typically ±1%. The PLLs will keep the switching and clock frequencies locked to whatever the mains frequency is, thereby ensuring that all of one lookup table's pulses fit exactly into one mains cycle. At the end of every mains cycle the PWM signal is hard-synchronised to the start of the new mains cycle to prevent small errors from building up over time.

The function of the modulator (mod.) is to combine the two signals coming into it by removing a single pulse from the high frequency pulses every 20ms. Thus both signals can be transmitted along one wire to different converters all driving the same load. The demodulator (demod.) recovers this information by low pass filtering the modulated signal to get the 50Hz signal.

2.3 Average Current-Mode Control

Review of Converter Control

A wide range of control techniques have been applied to ac-dc converters. These include a state variable controller [2.2] which uses multiple processors and four sensors to

control input current and voltage and output current of a current source rectifier. However, no mention is made of the switching frequency used in the implementation of this method, which makes it difficult to assess its efficacy in the light of the large inductors and input capacitor used. Another state variable scheme [2.3] which monitors ten state variables in order to damp the input filter oscillation as well as programming the input currents to be sinusoidal suffers from being too complex and was later simplified to four sensors [2.4]. An indirect current control method was proposed [2.5] that eliminates two current sensors but degrades the transient step-change-in-demand performance, in that the input current has a significant dc term for the duration of the transient. For the step-down converter, [2.6] monitoring of the three-phase input currents and dc output voltage has been considered using a simple analogue PWM generator and controller. Programming the input currents is claimed to improve the transient response of the system by damping the oscillations due to the input filter, but the authors also state that resistors in series with the input capacitors are essential for stability of the closed loop system, making it unclear as to what contribution to the damping each method provides.

Current Control for this Converter

The control scheme used in this thesis is a simple, analogue, dc-side located, fast average-mode current loop and a slow dc-side voltage controller, a total of two sensors. The inner current loop is analysed in detail in Section 4.5, where a number of important effects due to this loop are examined. Because the switching frequency of this converter is high (76.8kHz) the corner frequency of the input filter can also be high resulting in negligible phase shift of the fundamental, which can be a problem when off-line stored PWM schemes are used with low switching frequency operation. A

simplified block diagram for just one operational converter driving the load appears in Figure 2.5.

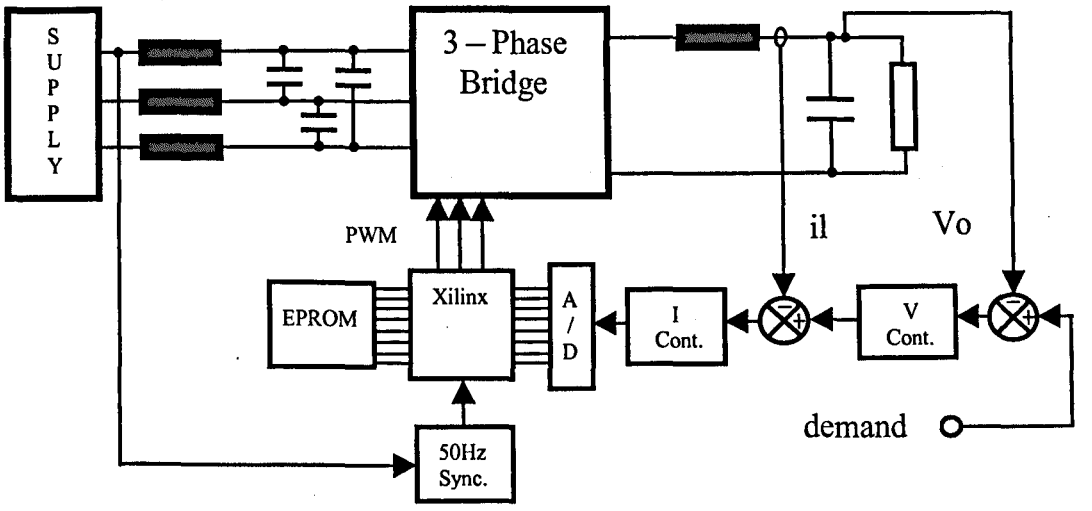

Figure 2.5 – System Block Diagram

2.4 Converter Steady-State Equations

DC Output Voltage and Current

The converter has 60° symmetry and so finding the dc voltage over this period is sufficient. Considering the 0-60° interval, the line-line voltages (V_{ac}, V_{bc}) are given by Equations (2.1a) and (2.1b), where V is the peak phase voltage

$$V_{ac} = \sqrt{3}V\sin\left(\omega_m t + \frac{\pi}{6}\right) \tag{2.1a}$$

$$V_{bc} = \sqrt{3}V\cos(\omega_m t) \tag{2.1b}$$

Averaging on a per switching cycle basis, the modulating functions (m_1, m_2) are given by Equations (2.2a) and (2.2b), where M is the modulation depth, $0 \le M \le 1$. The modulating functions can be phase shifted by an amount equal to $-\pi/3 \le \phi \le \pi/3$ in order to compensate for the input filter reactive power.

$$m_1 = M\sin(\omega_m t + \phi) \qquad 0 \le \omega_m t \le \pi/3 \tag{2.2a}$$

$$m_2 = M\sin\left(\omega_m t + \frac{2\pi}{3} + \phi\right) \qquad 0 \le \omega_m t \le \pi/3 \qquad (2.2b)$$

The per switching cycle averaged dc output voltage is given by the sum of the line voltages multiplied by their modulating functions

$$\overline{V_{dc}} = V_{ac}m_1 + V_{bc}m_2 \qquad (2.3)$$

Substituting Equations (2.1) and (2.2) into (2.3) and using trigonometric identities to simplify the result, results in most terms cancelling and finally yields Equation (2.4a). Equation (2.4b) gives the dc current that flows in the inductor as a result of a fixed resistive load, R.

$$\overline{V_{dc}} = \frac{3}{2}MV\cos\phi \qquad (2.4a)$$

$$\overline{I_{dc}} = \frac{1}{R}\frac{3}{2}MV\cos\phi \qquad (2.4b)$$

Note that this result is a pure dc term with no harmonics providing the input voltages are pure sinusoids. In this thesis cosϕ=1 as reactive power compensation of the input filter is not considered because the phase shift on the input current due to the filter is small for a high switching frequency converter using small filter capacitors. If simple ac-dc rectification with an infinite dc smoothing capacitor is used then approximately 13% more output volts can be obtained, but at the expense of non-sinusoidal input currents (unless a large inductor is used) and constant rather than variable dc output voltage.

Input AC Currents

The pure dc voltage produced will in turn produce a pure dc current. The input current in a phase will therefore be given by the dc current multiplied by that phase's modulation function. The third phase's current will be equal to the sum of the other two phases' currents. The three phase currents are given by

$$\overline{I_a} = \overline{I_{dc}}M\sin(\omega_m t + \phi) \qquad (2.5a)$$

$$\overline{I_b} = \overline{I_{dc}} M \sin\left(\omega_m t + \frac{2\pi}{3} + \phi\right) \tag{2.5b}$$

$$\overline{I_c} = \overline{I_{dc}} M \sin\left(\omega_m t + \frac{4\pi}{3} + \phi\right) \tag{2.5c}$$

Switch Currents

The average current flowing through a switch is found by integrating Equation (2.5a) between 0 and π radians and averaging over π radians to give

$$\overline{I_s} = \frac{2M\overline{I_{dc}}}{\pi} \tag{2.6}$$

Diode Currents

The average current flowing in any one of the diodes, except the freewheel diode, will be one half of the current flowing in one of the switches because pairs of diodes only conduct for either the positive or negative half cycles. The average diode current is given by

$$\overline{I_d} = \frac{M\overline{I_{dc}}}{\pi} \tag{2.7}$$

Freewheel Diode Current

The freewheel diode current can be found by first considering the total current flowing in the switches over any 60° period (because of the symmetry). During one switching cycle, two phases conduct and the total of these currents averaged over one switching cycle is given by

$$\overline{I_{st}} = \overline{I_{dc}} M\left[\sin(\omega_m t) + \sin\left(\omega_m t + \frac{2\pi}{3}\right)\right] \qquad 0 \le \omega_m t \le \pi/3 \tag{2.8}$$

The freewheeling current, when added to the total switch input current, will give the dc output current averaged on a per switching cycle basis. Therefore the freewheel current averaged over one switching cycle is given by

$$\overline{I_{df}} = \overline{I_{dc}} - \overline{I_{st}} \tag{2.9}$$

This can be simplified by substituting Equation (2.8) into Equation (2.9) to give

$$\overline{I_{df}} = \overline{I_{dc}}\left[1 + M\sin\left(\omega_m t + \frac{4\pi}{3}\right)\right] \qquad 0 \leq \omega_m t \leq \pi/3 \tag{2.10}$$

The average freewheel current over a 60° sextant is found by integrating and averaging Equation (2.10) from 0 to $\pi/3$ radians to give

$$\overline{\overline{I_{df}}} = \frac{\overline{I_{dc}}}{\pi}(\pi - 3M) \tag{2.11}$$

By inspection of Equation (2.11), it is seen that as $M \to 0$ so $I_{df} \to I_{dc}$ and so in the limit all of the load current is in the freewheel diode. Equations (2.4) to (2.11) were verified using the PSpice™ model described in Section 2.7.

DC Inductor Current Ripple

So far, the dc inductor ripple current has been ignored, but it is considered now as knowing this is a useful step in the design stage of a practical converter. Examining Figure 2.8 shows that the ripple current varies about a constant term where the minimum dc inductor current ripple occurs at 30° (two equal width pulses), whilst the maximum ripple occurs at the 0° and 60° points (one maximum width pulse produced) of each sextant. The voltage applied across the dc inductor is equal to the line voltage minus the voltage across the dc capacitor which is assumed to be constant as the capacitor is large. The ripple current is given by Equation (2.12), where Δt_{on} is the on-time of the switch at a certain point

$$\Delta I_{dc} = \frac{1}{L_{dc}}(V_{bc} - \overline{V_{dc}})\Delta t_{on} \tag{2.12}$$

By substituting Equations (2.1b) and (2.4a) into (2.12) and looking at the point of maximum ripple where $\omega_m t=0$ radians, then Equation (2.13) gives the maximum ripple current as a function of M.

$$\Delta I_{dc\max}(M) = \frac{V}{L_{dc}}\left(\sqrt{3} - \frac{3}{2}M\right)\Delta t_{on} \tag{2.13}$$

The on-time of the switch when phases 'b' to 'c' are conducting is given by Equation (2.14), where it is assumed that T_s, the switching period, is small in comparison with the modulating period.

$$\Delta t_{on} = T_s M \sin\left(\omega_m t + \frac{2\pi}{3}\right) \qquad 0 \le \omega_m t \le \pi/3 \tag{2.14}$$

The maximum on-time in Equation (2.14), Δt_{onmax}, occurs at $\omega_m t=0$ radians. Substituting $\Delta t_{on}=\Delta t_{onmax}$ into Equation (2.13), differentiating with respect to M and setting the result to zero gives the value of M for which the ripple is a maximum to be $M = 1/\sqrt{3}$, at which point the maximum value of the ripple current is given by

$$\Delta I_{dc\max} = \frac{\sqrt{3}VT_s}{4L_{dc}} \tag{2.15}$$

This result agrees with the PSpice™ simulation result. Likewise, the minimum ripple current can be shown to be a factor of $\sqrt{3}$ less than the maximum dc ripple current. As shown in Section 6.3, if the pulses are positioned back-to-back instead of interleaving them as we have here, then the ripple current is almost constant at the maximum value. Therefore as regards to losses in the dc inductor, interleaving is disadvantageous and will result in a greater temperature rise because the effective ripple frequency is twice the switching frequency, whilst the maximum ripple current is the same as in the non-interleaved case. The dc inductor still has to be designed to meet this maximum ripple current value.

AC Capacitor Ripple Voltage

The ripple voltage is computed at its maximum point. This occurs when the frequency of the pulses of current being drawn from the input capacitors is a minimum and when the width of the pulse is a maximum. This occurs at the 0° point for phase 'b' switching into 'c' and at the 60° point when phase 'a' is switching into 'c' of the 0 to 60° sextant. The ripple voltage is given by

$$\Delta V = \frac{1}{C_{ac}} I_c \Delta t_{on} \tag{2.16}$$

where $I_c\Delta t_{on}$ is the area of the current pulse. It is assumed that the low frequency harmonics are ignored, the 50Hz component of the current pulses is supplied entirely from the supply phase and the switching harmonics entirely from the capacitors. Considering the case when phase 'a' is switching into phase 'c' at the 60° point, then the current supplied by the phase is $I_a = I_{dc} M \sin \omega_m t = \frac{\sqrt{3}}{2} I_{dc} M$. The current demanded by the load is a trapezoidal pulse due to the finite dc inductor whose average magnitude can be approximated to a rectangular pulse of height I_{dc} and width $\Delta t_{on} = T_s M \sin \omega_m t = \frac{\sqrt{3}}{2} T_s M$. The current demanded from the capacitor is therefore $I_c=I_{dc}-I_a$. The total available capacitance from phases 'a' to 'c' is $3C_{ac}/2$. The maximum ripple voltage as a function of M is given by

$$\Delta V_{\max}(M) = \frac{I_{dc}}{\sqrt{3}} \frac{T_s M}{C_{ac}} \left(1 - \frac{\sqrt{3}}{2} M \right) \tag{2.17}$$

By differentiating this equation and setting the result equal to zero, the maximum ripple voltage is shown to occur at $M = 1/\sqrt{3}$ and is given by

$$\Delta V_{\max} = \frac{I_{dc} T_s}{6 C_{ac}} \tag{2.18}$$

This equation was verified against the PSpice™ model. The actual selection of C_{ac} depends on several factors; **(i)** the allowed reactive power that is to be drawn by the filter and the subsequent phase shift, **(ii)** the switching frequency, **(iii)** the maximum output dc current, **(iv)** the trade-off in the size of C_{ac} and L_{ac} (small C_{ac} will increase current ripple fed back into the supply and hence require L_{ac} to be larger) and **(v)** the allowed loss in output voltage due to the effective supply impedance seen by the bridge and output filter being greater than zero (this effect also has importance where current mode control feedback is used, see Sections 4.4 and 4.6).

2.4 Power Losses in the Converter

Conduction Power Loss

The conduction power losses in the converter can now be found easily using the equations previously developed. Excluding the freewheel diode, there are twelve diodes in the circuit. These diodes each have the same average current in them. Therefore the total diode conduction loss is given by Equation (2.19), where V_f is the forward conduction voltage of the DSEI 30-06A diode and is approximately 1.2V for a forward current of 13A @ 100°C

$$P_d = 12\overline{I_d}V_f \tag{2.19}$$

Likewise, the total of the three IGBT conduction losses is given by Equation (2.20) where V_s is the on-state voltage drop of the IRGP440U IGBT and is approximately 2V for a current of 13A @ 100°C.

$$P_s = 3\overline{I_s}V_s \tag{2.20}$$

The freewheel diode loss is given by

$$P_{df} = \overline{\overline{I_{df}}}V_f \tag{2.21}$$

In order to get an idea of the efficiency of this converter, the losses are calculated for a converter of output power 3kW and an input phase voltage of 110Vrms. Using Equation (2.4a), then the maximum dc output voltage will be approximately 230V @ M=1 and the dc current 13A. The maximum conduction loss will occur when M=1 and this information is used along with Equations (2.6), (2.7) and (2.11) to get $\overline{I_s} = 8A$, $\overline{I_d} = 4A$ and $\overline{\overline{I_{df}}} = 0.6A$. These numbers can then be substituted into Equations (2.19) to (2.21) to find the conduction power losses.

Switching Power Loss

The switching losses of the IGBTs are significant as the converter operates at high switching frequency. To a first order approximation, the reverse recovery power loss can be ignored. From the IRGP440U IGBT datasheet, the total switching energy at 11A and 400V @ 100°C is approximately 0.3mJ. However, the average voltage seen by one of the IGBTs over one sextant is less than 400V and is found by integrating and averaging the line voltage (Equation (2.1b)) over π/3 radians to give 222V. The switching losses are approximately proportional to the voltage and so the total switching energy is approximately halved to E_t=0.15mJ. The effective switching frequency of the converter is $f_e=2/3f_s$=51.2kHz, because during two sextants out of six the IGBTs are held on. Thus, the total IGBT switching power loss is given by

$$P_{sw} = 3E_t f_e \tag{2.22}$$

Total Power Loss and Efficiency

Using Equations (2.19) to (2.22), Table 2.1 was produced, which summarises the contribution each power loss makes to the total power loss. One interesting feature of the table is the fact that the ultrafast IGBTs are optimised for low switching loss at the expense of the on-state conduction voltage drop, so even if the more usual six IGBT

bridge configuration had been used, the saving on conduction losses would only be 10W for the same modulation scheme / switching loss, giving an efficiency of 96.1%.

Device / Type of Loss / Symbol	Power Loss (W)
Diodes / Conduction / P_d	58
Freewheel Diode / Conduction / P_{df}	0.7
IGBTs / Conduction / P_s	48
IGBTs / Switching / P_{sw}	24
	Total ≈ 131W, Efficiency≈95.8%

Table 2.1 – Summary of Device Losses

2.6 The Use of Computer Simulations

A number of different simulation approaches are possible, as outlined below

Saber™

Saber™ can simulate closed loop controlled power electronics systems effectively. The disadvantage is that it is expensive and more complex to use compared with other simulation software. The challenge is to simulate the power electronic converter circuit using cheaper, alternative software.

PSpice™

PSpice™ is a cheaper, popular choice for simulating a wide range of electronic circuits, including power electronics circuits. It can simulate down to the device level or at the system level, e.g. are the power transistors to be treated as ideal switches or not. The difficulty in power electronics is that if high frequency PWM schemes are used then the simulation time-step needs to be small. Results are often required over

time spans of several mains periods, thus making the simulation slow. Implementing closed loop control of a converter with sinusoidal dead-band PWM is also difficult.

MATLAB™ plus SIMULINK™

For the reason above, a MATLAB™ plus SIMULINK™ exact switching model was derived. This model has the advantage of easy implementation of closed loop control, as the software is primarily designed to do this. Also, in the case of this converter, the bridge can be treated as a mathematical 'black box', the currents and voltages of the devices being of no importance at the system level. For example, in place of a rectification process that would require diodes using PSpice™, the absolute value (abs) block in SIMULINK™ can be used. This improves the speed of the simulation. However, current flow in a converter modelled as an input filter followed by a black box bridge followed by a dc output filter does not function naturally as in PSpice™. Instead, the current in the input filter needs to be derived specially from the output filter current. See Section 4.2.6 for more details.

MathCAD™

Simulations are useful for simulating the system under a set of precisely controlled conditions (e.g. undistorted mains phase voltages) and for ease of changing component values. However, the use of simulations does not guarantee understanding as to why the converter is behaving in a certain way. For this reason, reducing the converter to a set of equations and applying the package MathCAD™ to solve them is also a valuable method that can give insight into the fundamental behaviour of a system. MathCAD™ is also useful for testing any equations developed that describe the system's behaviour.

As well as exact, switching simulations, average models are also useful. The average model reduces the non-linear, time-varying, discontinuous system to a time-invariant, continuous model. Such a model can then be linearised about an operating point and the powerful mathematical methods valid for linear systems can be applied e.g. frequency response plots. Stability of the closed loop system can then be examined. Such a model is developed in Section 4.4.

Comparing simulation against simulation and simulation against the real world in the laboratory is important in assessing the validity and limitations of a certain model as well as using the models to explain the operation of the converter.

2.7 PSpice™ Simulation of the Open-Loop Converter

In order to investigate the properties of the converter further, a simulation was designed using the PSpice™ software package. The circuit listing is given in Appendix A1 and represents the converter shown in Figure 2.1. Note the values of parallel capacitance and series resistance of the diode and series resistance of the switch are used to smooth the discontinuities due to switching and aid convergence. The IGBTs are modelled as ideal switches, as we are only concerned with system-level rather than device-level effects. The sources driving the IGBT gates have series and parallel resistors to aid simulation convergence.

The PWM waveforms supplied to the IGBT gates cannot be generated easily using PSpice™ and so a 'C' programme was used to produce three, piece-wise-linear (PWL) files of the PWM waveforms which can then be included in the listing as voltage sources by using the '.INC' command. These PWL files contain lists of off/on times that describe the magnitude of the PWM signal at the switching points. The 'C' programme is split into a main driving module and two other routines that are called by

this module which calculate the on/off times and write them to three files. Examples of the PWM signals generated, taken from the simulation itself, are shown in Figures 2.6a, 2.6b and 2.6c. The 'C' programme is given in Appendix A2.

All of the results from Figures 2.6a to 2.19 were taken using the following basic conditions: M=0.577, L_{dc}=160μH, C_{dc}=2000μF, L_{ac}=50μH, C_{ac}=3μF, V=240V, R=20Ω and f_s=76.8KHz. All other conditions can be found in the PSpice™ listing given in Appendix A1

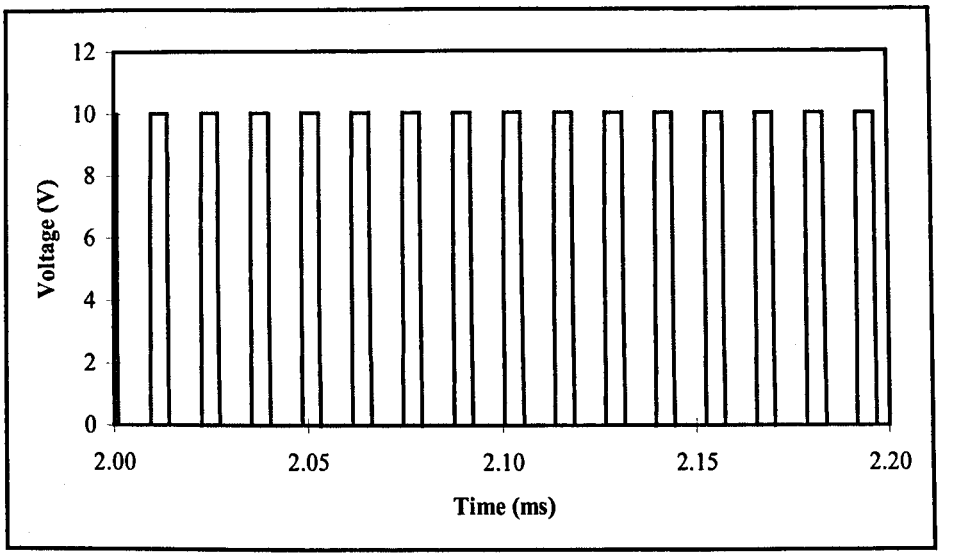

Figure 2.6a – Gate Drive Waveform for Phase A

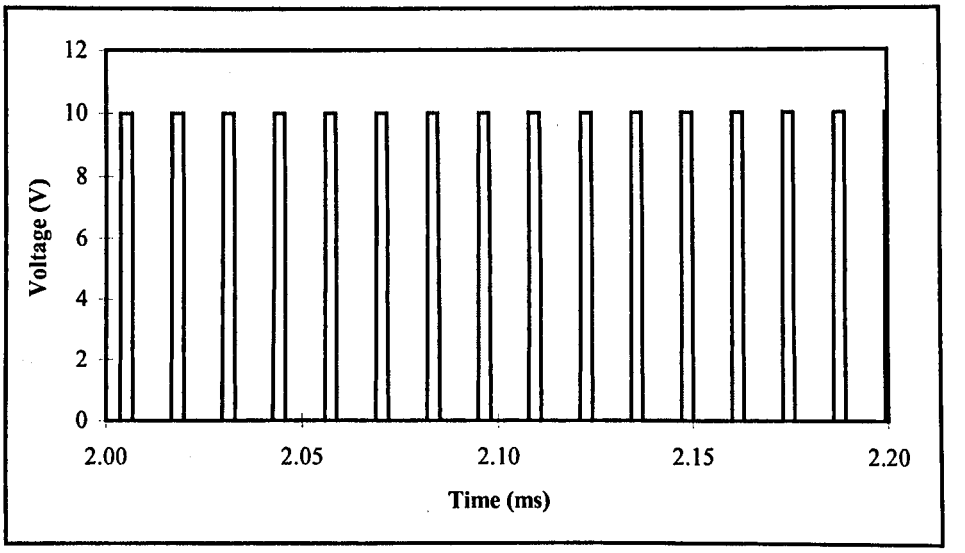

Figure 2.6b – Gate Drive Waveform for Phase B

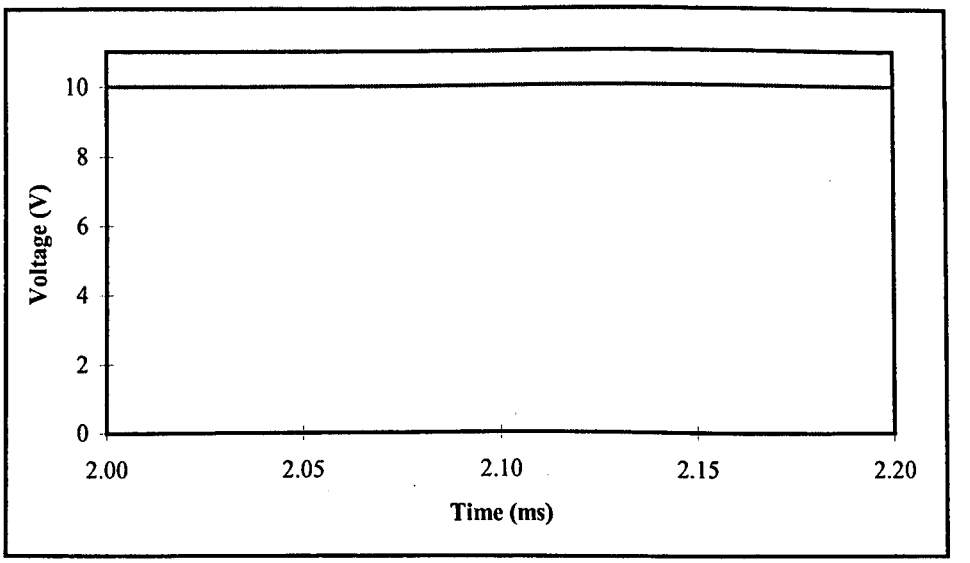

Figure 2.6c – Gate Drive Waveform for Phase C

Some of the characteristic waveforms of the converter are shown in Figures 2.7 and 2.8 over a 60° sextant. N.B. The 0-360° waveform (i.e. one mains cycle) consists of six repetitions of any 60° segment. The filtered input current waveforms for one mains period are shown in Figure 2.9. The distorted nature of these waveforms is due to the input filter drawing a reactive current and also the effect of using a finite dc inductor, see Section 3.7.

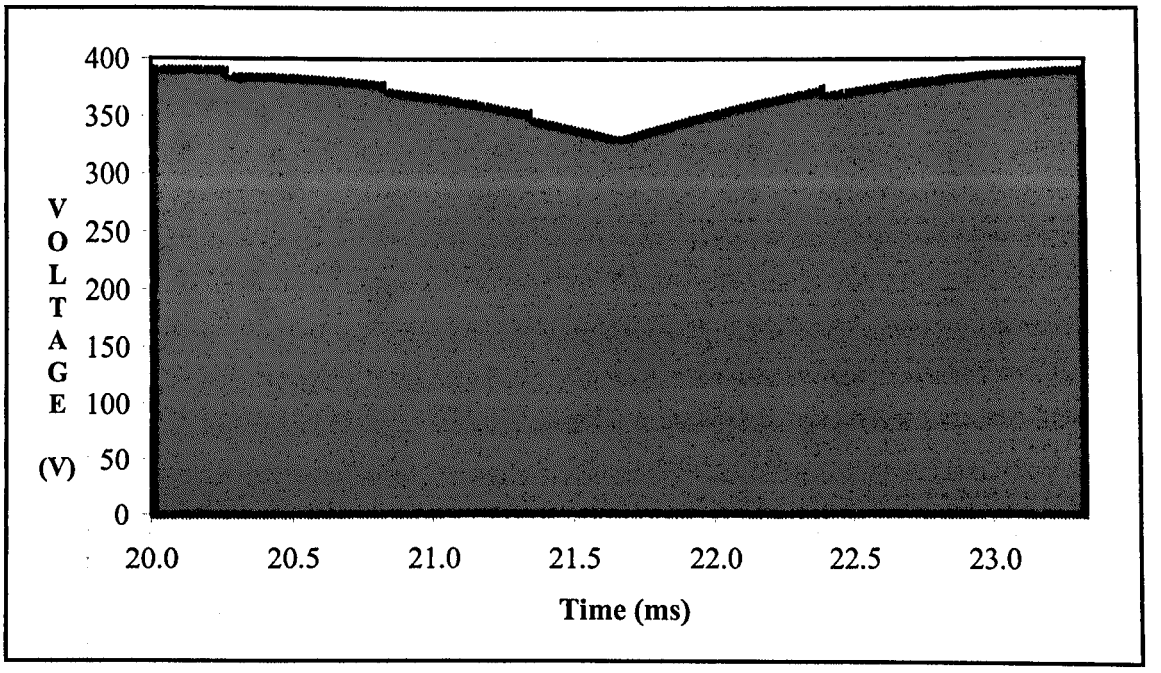

Figure 2.7 – Output Voltage From Rectifier Bridge 0-60°

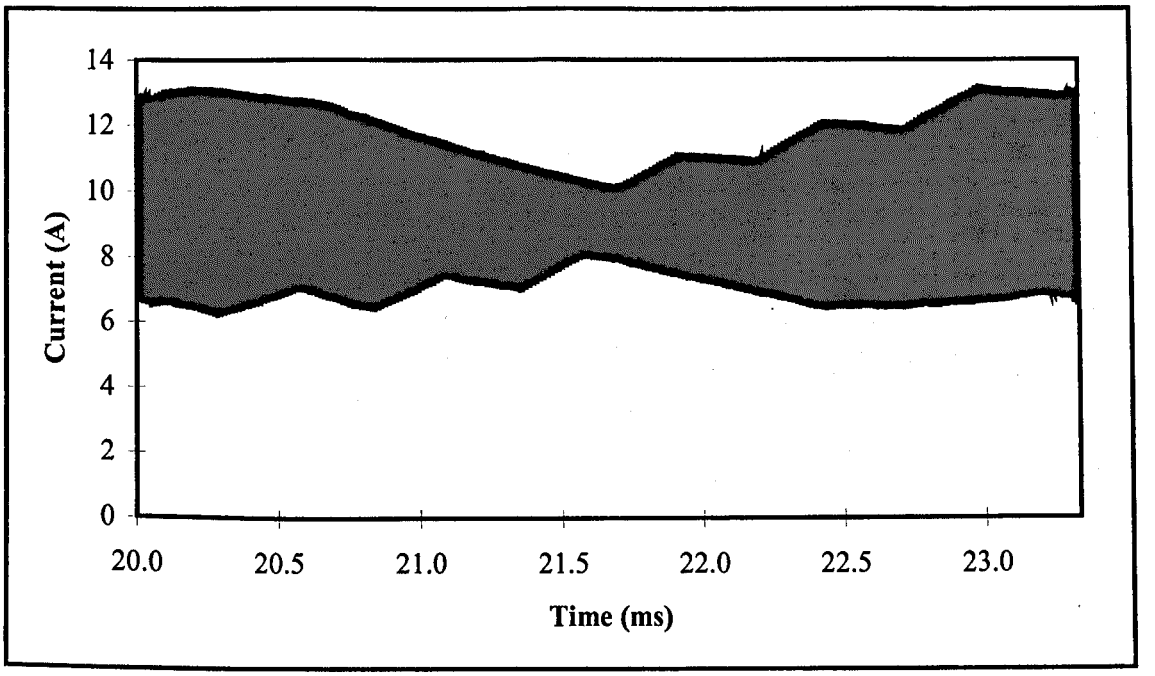

Figure 2.8 – The DC Inductor Current 0-60°, I_{dc}

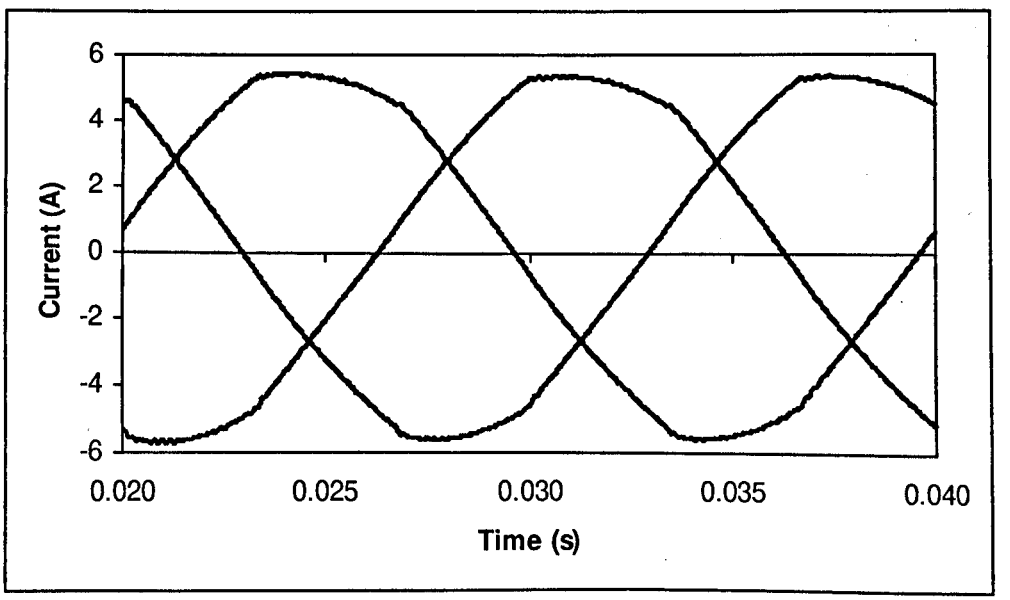

Figure 2.9 – Three Phase Input Mains Currents, I_a, I_b, I_c

Zoomed-in views of the bridge voltage and inductor current clearly show the nature of the interleaving of the pulses and are shown in Figures 2.10 and 2.11 for the same time interval as the PWM signals shown in Figures 2.6a to 2.6c.

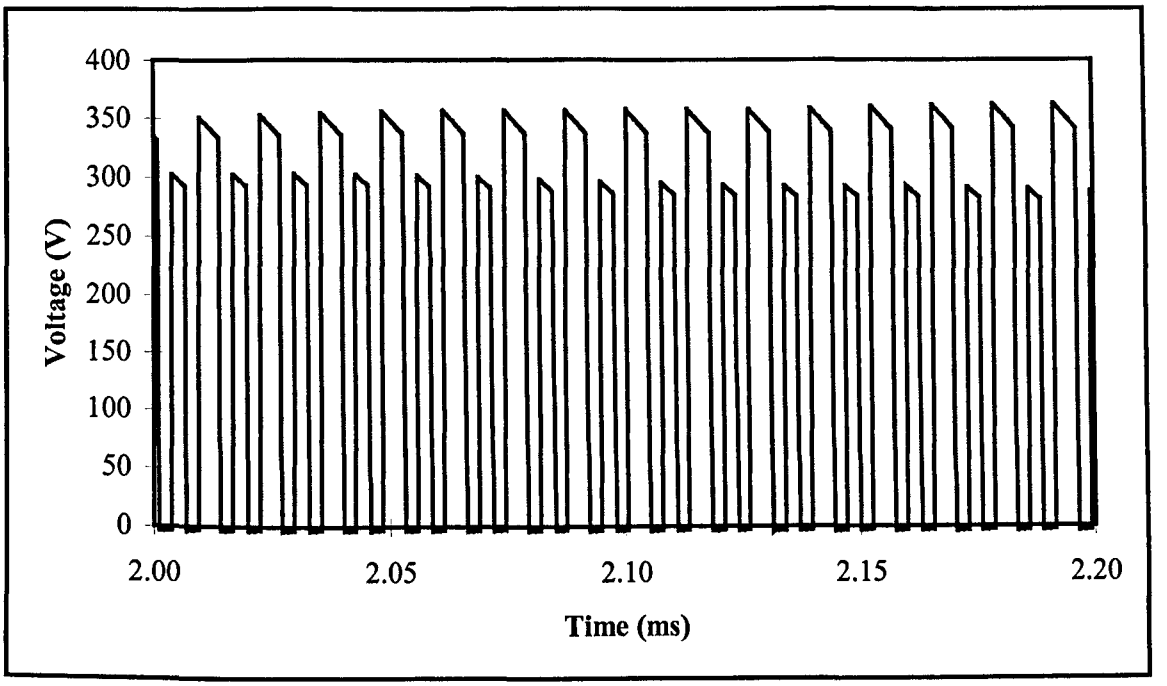

Figure 2.10 – Bridge Voltage Output

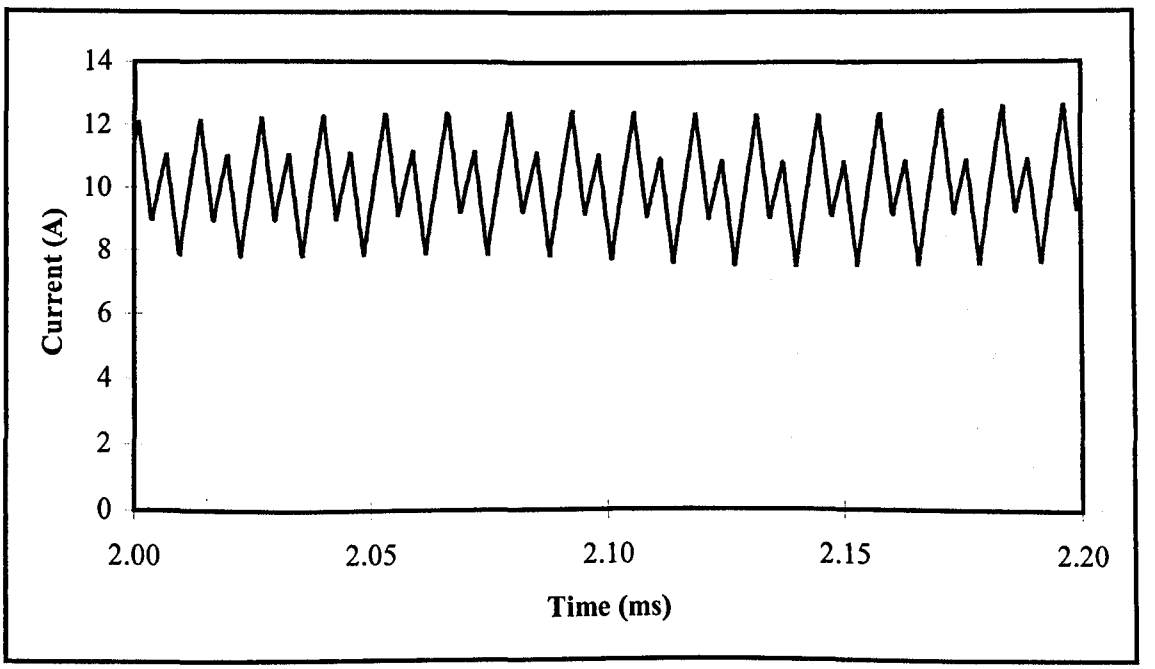

Figure 2.11 – DC Inductor Current

Other characteristic waveforms include the switch current, diode current and freewheel diode current and are shown in Figures 2.12, 2.13 and 2.14 respectively. Note that the gap around the 30ms mark in Figures 2.12 and 2.15 is caused by the deletion of narrow pulses that are less than the minimum allowed. These pulses are deleted as their width is less than the time it takes for an IGBT to turn on fully. If they were not deleted the IGBT would conduct current in a high loss state.

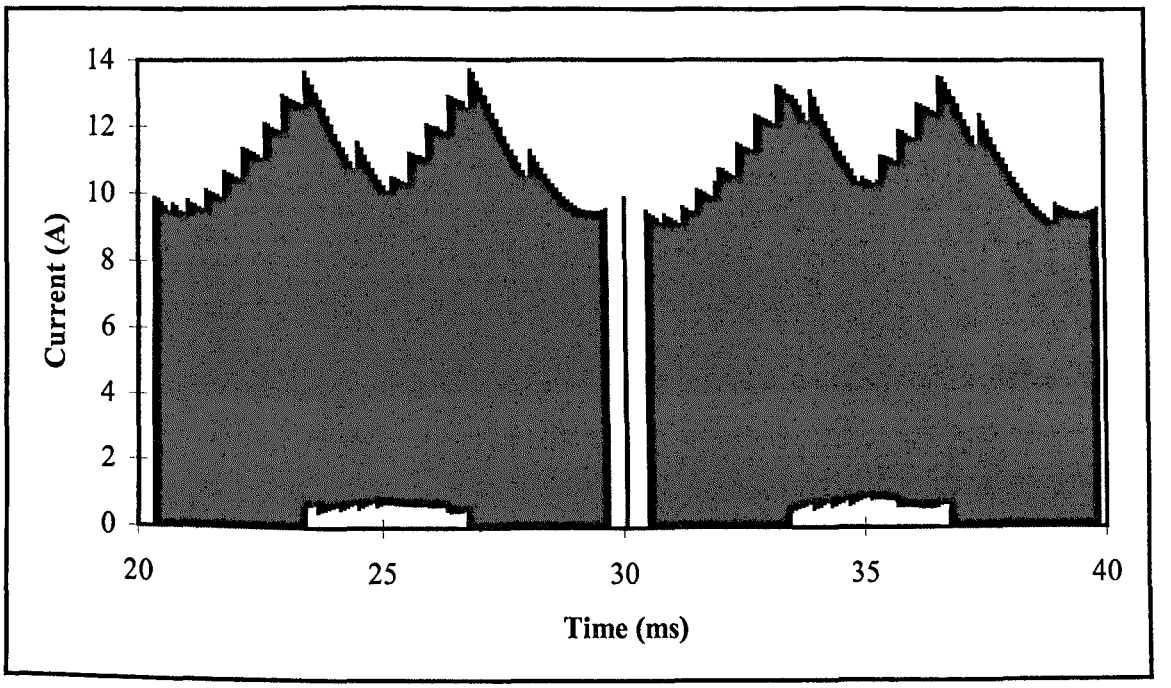

Figure 2.12 – Switch Current, I_s

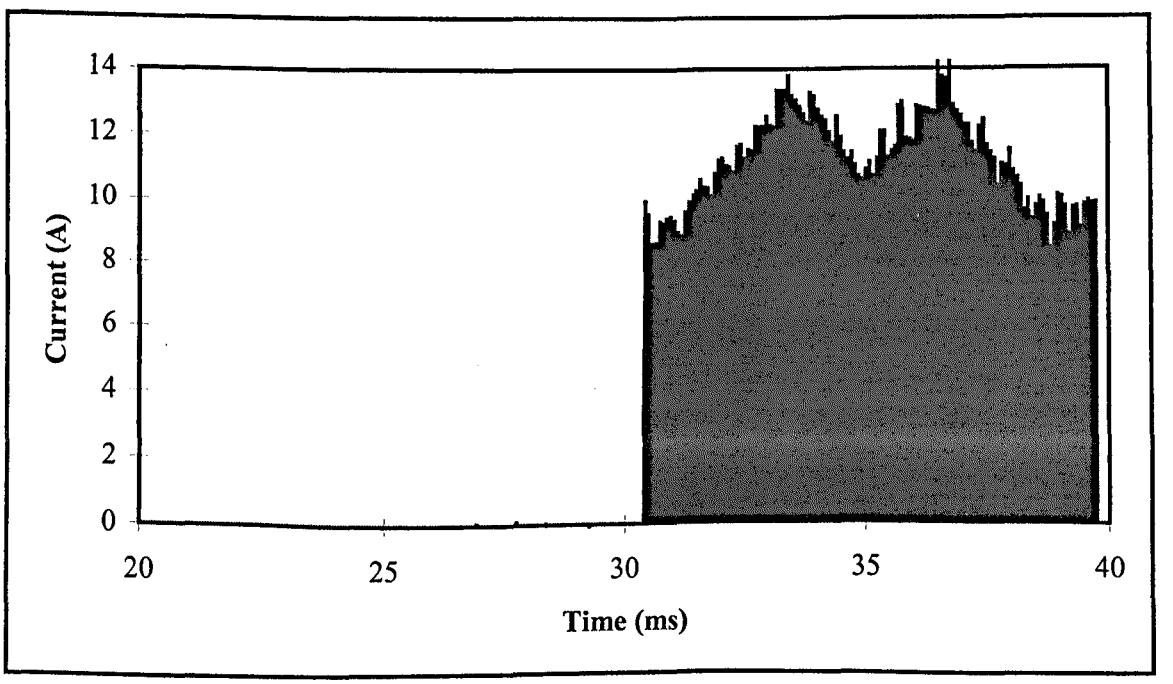

Figure 2.13 – Diode Current, I_d

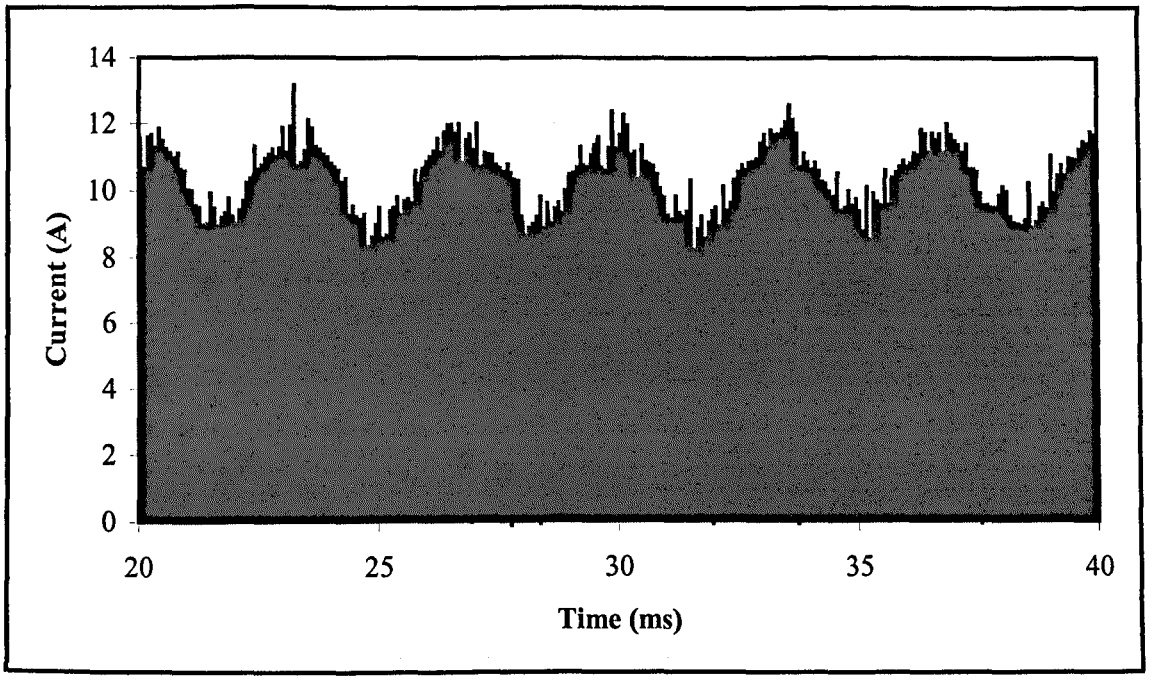

Figure 2.14 – Free-Wheel Diode Current, I_{df}

The dc output voltage waveform is not shown, but consists of a 185V dc component with a negligible amount of ripple riding on it. In practice, the dc ripple voltage will be dominated by the capacitor's equivalent series resistance (esr).

The unfiltered mains input current for one phase is shown in Figure 2.15 and the harmonic components of this waveform at low frequency are shown in Figure 2.16, those centred around ω_s in Figure 2.17, those around $2\omega_s$ in Figure 2.18 and those around $3\omega_s$ in Figure 2.19. The low frequency distortion is mainly 5^{th} and 7^{th} harmonics. The two carrier components are clearly seen in Figure 2.17. More analysis of these harmonics appears in Section 3.3, where their distribution and amplitude are shown to be controlled by Bessel functions. The harmonic components of the bridge output voltage are also computed using PSpice™ and are shown in Figures 2.20, 2.21 and 2.22.

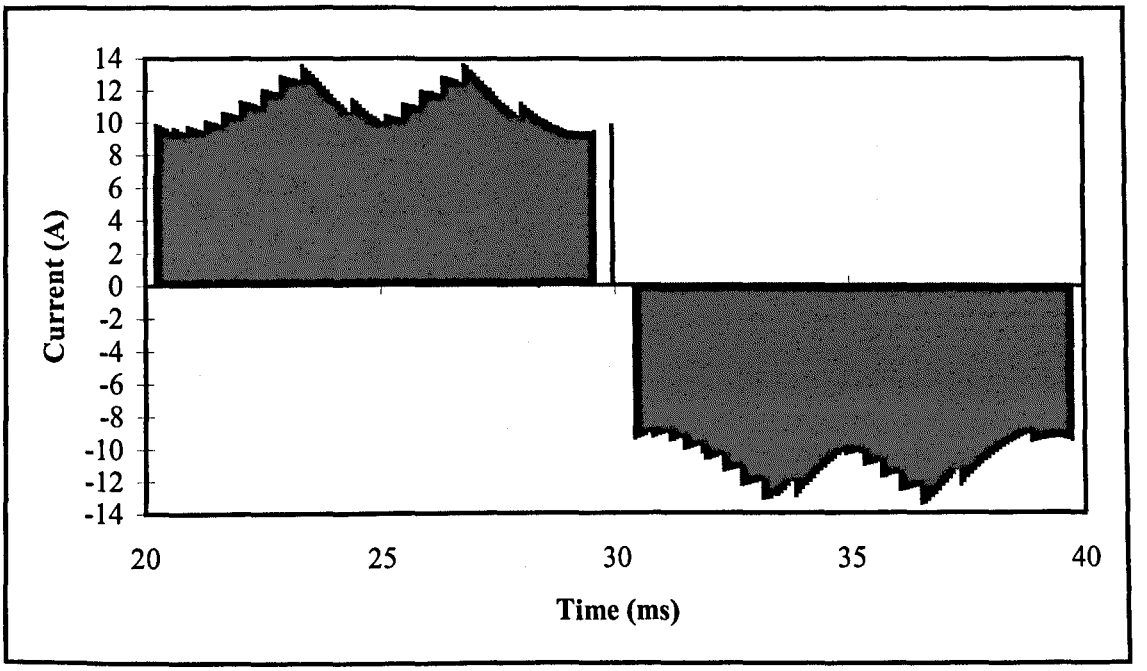

Figure 2.15 – Unfiltered Input AC Current

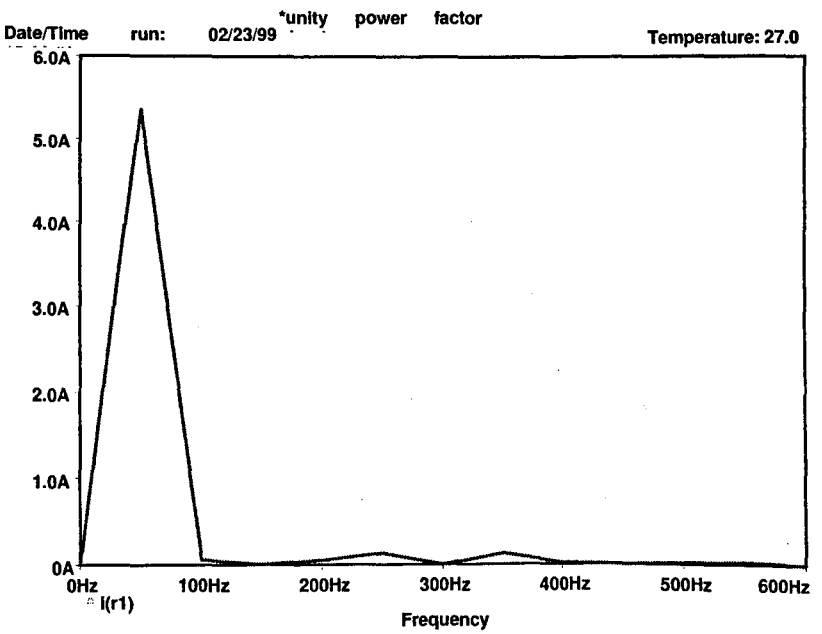

Figure 2.16 – Input Current Low Frequency Harmonics

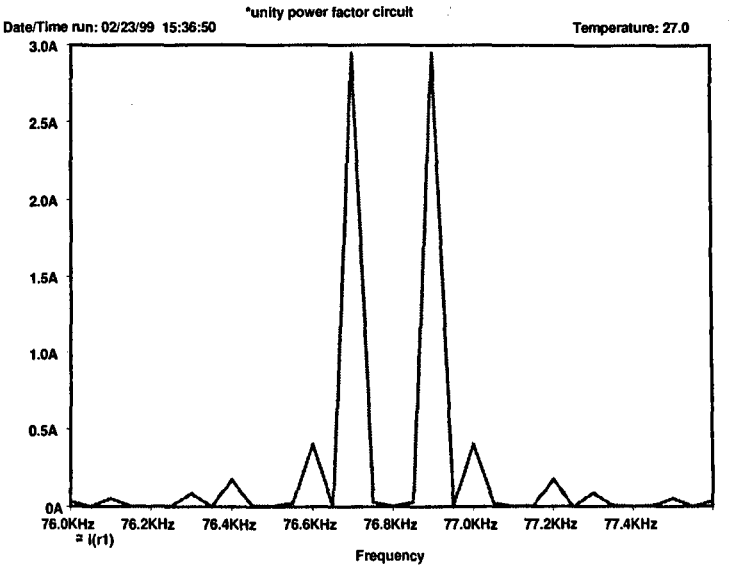

Figure 2.17 –Input Current Harmonics Centred About ω_s

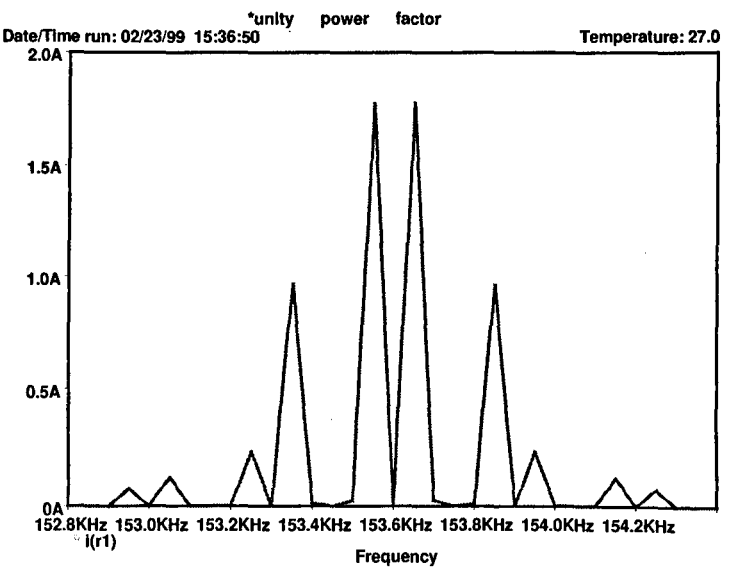

Figure 2.18 –Input Current Harmonics Centred About $2\omega_s$

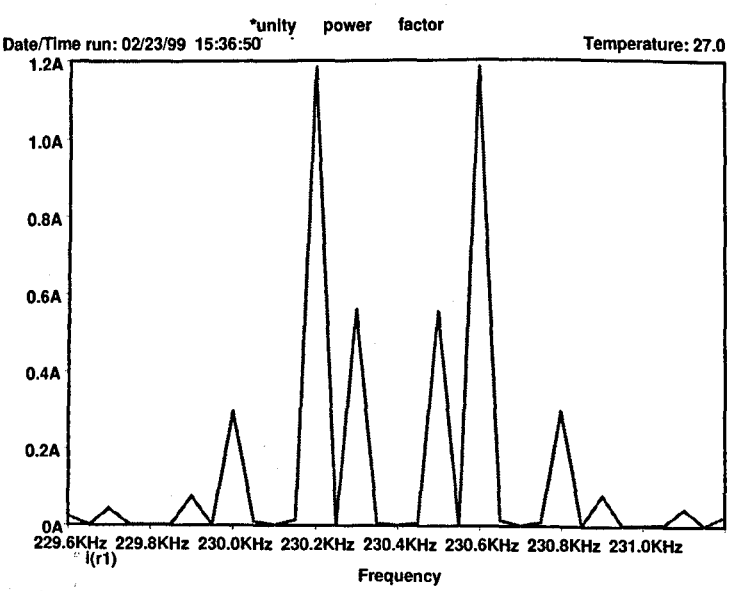

Figure 2.19 –Input Current Harmonics Centred About $3\omega_s$

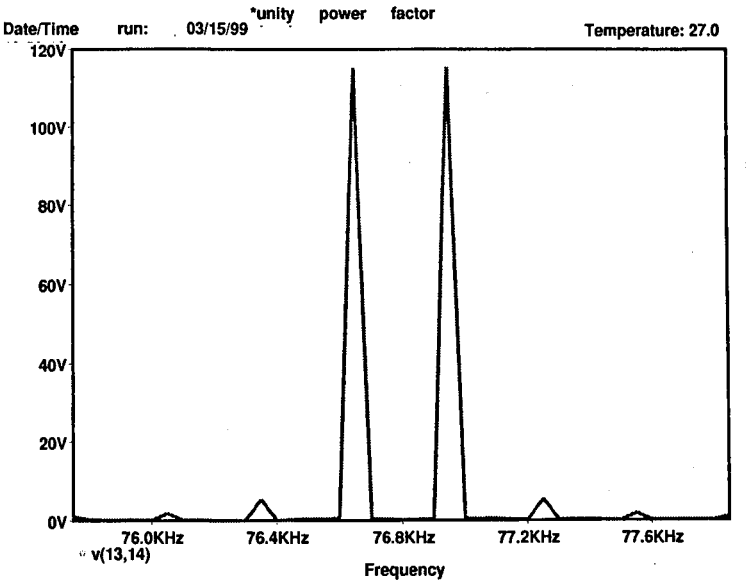

Figure 2.20 – Output Voltage Harmonics Centred About ω_s

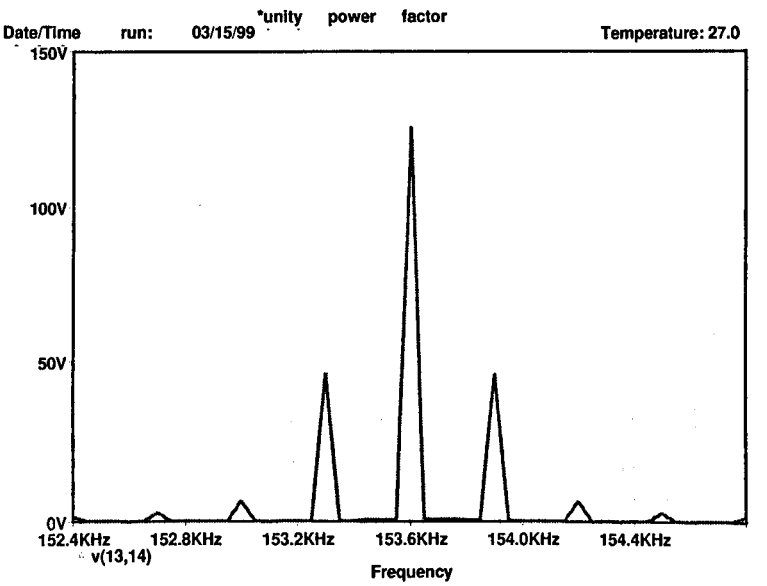

Figure 2.21 – Output Voltage Harmonics Centred About $2\omega_s$

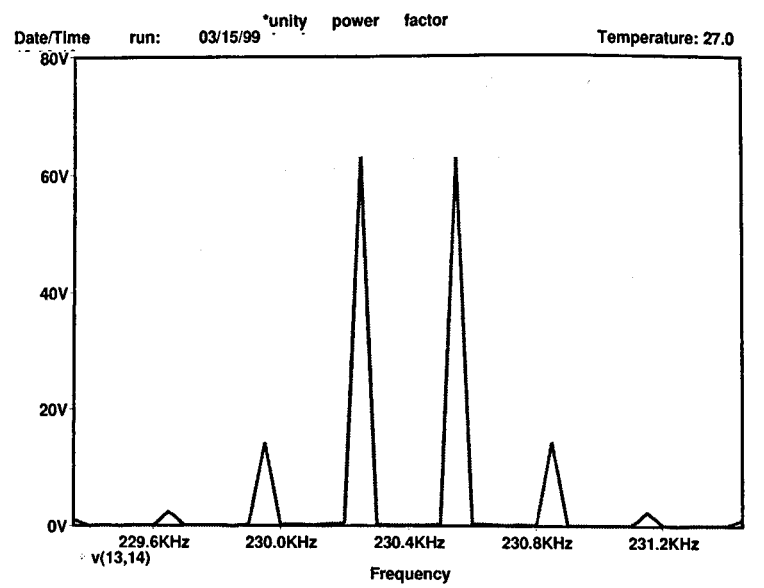

Figure 2.22 – Output Voltage Harmonics Centred About $3\omega_s$

2.8 Practical Results

Practical waveforms for the bridge output voltage and dc inductor current are shown in Figure 2.23. Open loop operation of the converter gives different waveforms to those generated by PSpice™ because the power supply phase voltages are not purely sinusoidal but rather have a "flat-top" appearance due to low frequency 5^{th} and 7^{th} harmonics causing harmonic currents to flow. This is investigated in detail in Section 3.6, which looks at the theory of harmonic transfer and Section 4.5.2 which investigates how closing a dc current feedback loop reduces the current harmonics' magnitudes.

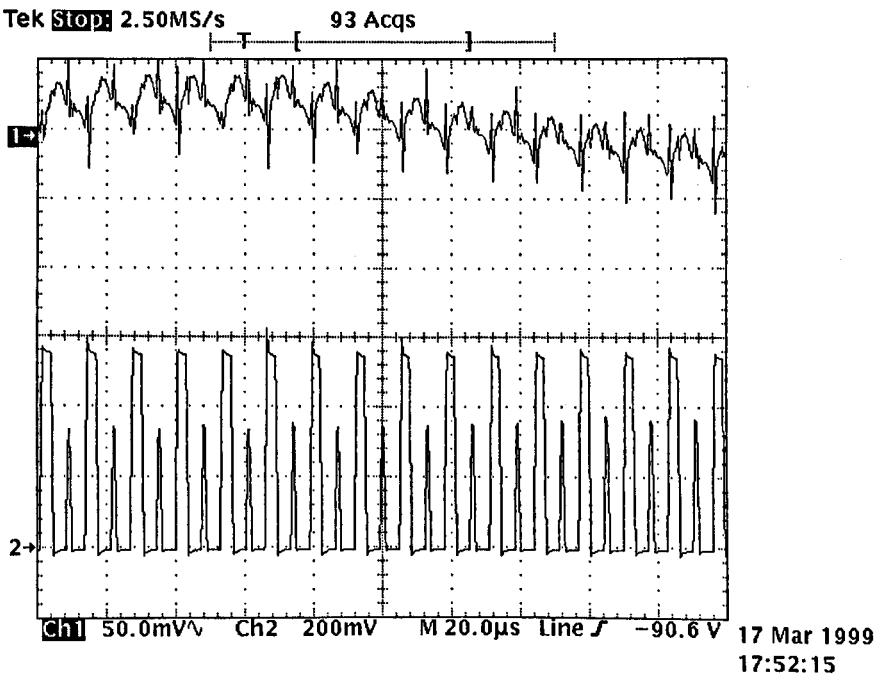

Figure 2.23 – Upper Trace : AC Inductor Current Ripple (0.5A/div)

Lower Trace : Bridge Output Voltage (40V/div)

Note that the dc inductor current contains low frequency harmonics of greater magnitude than the switching frequency.

2.9 References

2.1 V. G. Agelidis, P D Ziogas and G. Joos, "Dead Band PWM Switching Patterns", IEEE PESC Conf., pp. 427-434, 1992

2.2 X. Wang and B-T. Ooi, "Real Time Multi DSP Control of Three Phase Current Source Unity Power Factor PWM Rectifier", IEEE Trans. Power Elec. , Vol. 8, No. 3, pp. 295-300, 1993

2.3 A. Draou, Y. Sato and T. Kataoka, "A New State Feedback Based Transient Control of PWM AC to DC Voltage Type Converters", IEEE Trans. Power Elec., Vol. 10, No. 6, pp. 716-724, 1995

2.4 Y. Sato and T. Kataoka, "A Current Type PWM Rectifier with Active Damping Function", IEEE IAS Conf., Vol. 3, pp. 2333-2340, 1995

2.5 J. W. Dixon and B-T. Ooi, "Indirect Current Control of a Unity Power Factor Sinusoidal Current Boost Type Three-Phase Rectifier", IEEE Trans. Ind. Elec., Vol. 35, No. 4, pp. 508-515, 1988

2.6 N. R. Zargari and G. Joos, "A Current-Controlled Current Source Type Unity Power Factor PWM Rectifier", IEEE IAS Conf., Vol. 2, pp. 793-799, 1993

CHAPTER 3 – Harmonic Analysis

3.1 Introduction

A considerable amount of work has been done on the analysis of the spectra of switching converters and inverters. A double Fourier integral approach [3.1] is one method of analysing the complex PWM waveform and was applied to single and three-phase inverter systems using either natural or uniform (regular) sampling. This method suffers from being difficult to visualise (a 3D representation is given) and was only applied to sinusoidal PWM (SPWM). Another analytical technique [3.2] was developed to examine the spectra of space vector modulated inverters. It presents a general solution for both regularly sampled asynchronous PWM and regularly sampled synchronous PWM (the carrier frequency is a fixed integer multiple of the modulating frequency) by resolving the PWM waveform into a series of symmetrical waveforms. Fourier analysis is performed on each of these waveforms and the result is summed to give the analysis of the original waveform. Delta-Sigma modulated inverters were previously examined [3.3], a closed-form expression for the spectra produced and a set of conclusions drawn. Attention was given to the underlying amplitude modulation (AM) and frequency modulation (FM) processes present in the PWM. A novel and flexible simulation technique [3.4] was used to predict the spectra of digital asynchronous PWM based on double Fourier integration. This technique explained a number of observed spectra phenomena due to dead-time and minimum pulse deletion in inverters.

The modulation scheme used for the purpose of study in this thesis is of the dead-band variety and, as well as being discontinuous at the switching cycle level, is also discontinuous every 120° of the low frequency mains modulating period. The PWM scheme used is regular-sampled synchronous PWM. Thus a method of analysis is needed that can cope with the low frequency discontinuity and take advantage of the synchronicity.

3.2 Introduction to Harmonic Analysis

A review of some of the harmonic analysis techniques and examples relevant to the future derivations (Section 3.3) is made.

3.2.1 Standard Fourier Series and Fourier Theory of Jumps (FTJ)

Standard Fourier Series Integrals

The standard Fourier series integral equations for the coefficients, a_0, a_n and b_n and the series itself, are given by Equations (3.1) to (3.4)

$$a_0 = \frac{1}{2\pi}\int_{-\pi}^{\pi} f(x)dx \tag{3.1}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\cos nxdx \qquad n = 1,2...\infty \tag{3.2}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin nxdx \qquad n = 1,2...\infty \tag{3.3}$$

$$f(x) = a_0 + \sum_{n=1}^{\infty}\left(a_n \cos nx + b_n \sin nx\right) \tag{3.4}$$

The Fourier Theory of Jumps (FTJ)

The FTJ is a little known method [3.5] that produces the a_n and b_n Fourier series coefficients whilst avoiding doing integration. The original theory of the method [3.13, 3.14] and its application to several power electronics cases [3.15, 3.16] seems to have been largely forgotten. The FTJ relies on analysing the waveform, for which the Fourier coefficients a_n and b_n are to be determined, by resolving the waveform into a series of 'jumps', at which points the derivatives are taken and summed according to Equations (3.5) and (3.6). Where n is the n^{th} harmonic, j_s is the sign and magnitude of the s^{th} jump, x_s is the angle at which the s^{th} jump occurs, m is the number of jumps over the period of the

waveform and $\dot{j}_s, \ddot{j}_s$ etc. are the derivatives of the s[th] jump. For a further explanation of the FTJ see Appendix A18. The value of the dc component, a_0, of the series is calculated by using the usual method of integration given by Equation (3.1).

$$a_n = \frac{1}{n\pi}\left[-\sum_{s=1}^{m} j_s \sin nx_s - \frac{1}{n}\sum_{s=1}^{m} \dot{j}_s \cos nx_s + \frac{1}{n^2}\sum_{s=1}^{m} \ddot{j}_s \sin nx_s + ...\right] \tag{3.5}$$

$$b_n = \frac{1}{n\pi}\left[\sum_{s=1}^{m} j_s \cos nx_s - \frac{1}{n}\sum_{s=1}^{m} \dot{j}_s \sin nx_s - \frac{1}{n^2}\sum_{s=1}^{m} \ddot{j}_s \cos nx_s + ...\right] \tag{3.6}$$

For a pulsed PWM type waveform, Equations (3.5) and (3.6) can be further simplified by realising that the components of these equations involving the derivatives of the jumps are all zero. Also, most of the waveforms to be analysed here demonstrate either "odd" or "even" symmetry and so the summation need only be carried out over m/2 and the result doubled, see Equations (3.7) and (3.8). (The definition of a 'jump' being the point at which the waveform to be analysed experiences a discontinuity).

$$a_n = \frac{-2}{n\pi}\sum_{s=1}^{m/2} j_s \sin nx_s \tag{3.7}$$

$$b_n = \frac{2}{n\pi}\sum_{s=1}^{m/2} j_s \cos nx_s \tag{3.8}$$

3.2.2 Bessel Functions and Amplitude, Double Side Band and Frequency Modulation

Bessel Functions

The Bessel functions, $J_n(x)$, are solutions to the integral Equation (3.9) and have found applications in such diverse fields as; loudspeaker design, analysis of heat flow and analysis of electromagnetic wave propagation. Where n is the n[th] Bessel function and x is called the argument of the Bessel function.

$$J_n(x) = \frac{1}{2\pi}\int_0^{2\pi} \cos(n\theta - x\sin\theta)\,d\theta \tag{3.9}$$

This equation can be expanded in a Fourier series [3.6] to give Equations (3.10), (3.11) and (3.12).

$$a_0(x) = J_0(x) = \frac{1}{2\pi}\int_0^{2\pi} \cos(x\sin\theta)d\theta \tag{3.10}$$

$$\frac{1}{2}a_n(x) = J_n(x) = \frac{1}{2\pi}\int_0^{2\pi} \cos(x\sin\theta)\cos(n\theta)d\theta \qquad \text{n=even} \tag{3.11}$$

$$\frac{1}{2}b_n(x) = J_n(x) = \frac{1}{2\pi}\int_0^{2\pi} \sin(x\sin\theta)\sin(n\theta)d\theta \qquad \text{n=odd} \tag{3.12}$$

Frequency Modulation (FM)

Another application where Bessel functions occur is in Frequency Modulation (FM). A typical FM signal has the form of

$$FM(t) = V_c\cos(\omega_c t + x\sin\omega_m t) \tag{3.13}$$

Where V_c is the peak of the carrier voltage, ω_c is the angular carrier frequency, ω_m the angular modulating frequency and the argument of the Bessel functions is the depth of modulation, $x=\Delta\omega/\omega_m$, where $\Delta\omega$ is the maximum deviation of the carrier frequency. Equation (3.13) can be expanded using a trigonometric identity and further expanded as a Fourier series to give

$$FM(t) = J_0(x)\cos(\omega_c t) + \sum_{n=even}^{\infty} J_n(x)\left[\cos(n\omega_c t + n\omega_m t) + \cos(n\omega_c t - n\omega_m t)\right]$$

$$+ \sum_{n=odd}^{\infty} J_n(x)\left[\cos(n\omega_c t + n\omega_m t) - \cos(n\omega_c t - n\omega_m t)\right] \tag{3.14}$$

Equation (3.14) shows that a carrier component varying like the $J_0(x)$ Bessel function is produced and also sidebands at $\pm n\omega_c$ either side of the carrier which vary in amplitude like the $J_n(x)$ Bessel functions, where $n = 1,2,3....\infty$.

Amplitude and Double Side Band Modulation

Amplitude Modulation (AM) and Double Side Band Modulation (DSBM) are produced when a high frequency carrier is multiplied by a low frequency modulating signal. If the modulating signal contains a dc term, then the result is AM and the spectrum has a component at the carrier frequency, ω_c, if not then the result is DSBM and there is no carrier component. Both schemes have frequency components in their spectrums situated at $\omega_c \pm \omega_m$. See Equations (3.15) and (3.16), where ω_m and ω_c are the modulating and carrier frequencies respectively, V_m and V_c are the magnitudes of the modulating and carrier waveforms respectively and V_{dc} is the magnitude of the dc component of the modulating signal in AM.

$$DSBM(t) = V_m \sin(\omega_m t) V_c \sin(\omega_c t) = \frac{V_m V_c}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right] \quad (3.15)$$

and

$$AM(t) = \left[V_m \sin(\omega_m t) + V_{dc}\right] V_c \sin(\omega_c t) = \frac{V_m V_c}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right] + V_{dc} V_c \sin(\omega_c t) \quad (3.16)$$

3.1 Closed-Form Expressions for Converter Harmonics

Most of the work on switching harmonics presented has been carried out on inverters. This section will develop closed form expressions for the harmonics of this thesis' converter using the novel and simple method of FTJ, which can cope with the complexity of three-phase dead-band PWM schemes.

3.2.3 Analysis of Converter Input Current Harmonics Using the CAPWM Scheme

A number of assumptions are made at the outset :-

1. Practically, only synchronous PWM schemes are used with these converters as it has been shown that low frequency harmonics are removed if synchronous schemes are used. Thus the equations used assume the switching frequency is a fixed integer multiple of the phase voltages' frequency.
2. The PWM scheme exhibits "odd" symmetry about the 180° (π rad) point for the input current and so a_n=0. (In fact, if the pulses for 'a' phase are drawn at around the mains cycle crossover point, then it is seen that the exact point of symmetry is actually π-$\omega_s T_s/4$ radians).
3. The modulating frequency, ω_m, is chosen to be 1 rad/s, thus $f_m=1/2\pi$ Hz and this will satisfy the Fourier equations which are valid for waveforms of period 2π seconds. The switching frequency, ω_s, is an integer multiple of ω_m.
4. There is no dc component to the ac sinusoidal input current, thus a_0=0.
5. The magnitude of a rising edge jump =I_{dc} and for a falling edge jump =-I_{dc} i.e. we assume the dc inductor is infinite.
6. The principle of superposition applies, so that the harmonic contributions of different parts of the PWM waveform can be found separately and the results summed to give the overall harmonic expression.

The positions of the rising and falling edges of a certain pulse in a stream of PWM pulses are given by Equations (3.17) and (3.18) and are illustrated in Figure 3.1.

$$t_r = \frac{T_s}{2}(1 - M\sin\omega_m t) \tag{3.17}$$

$$t_f = \frac{T_s}{2}(1 + M\sin\omega_m t) \tag{3.18}$$

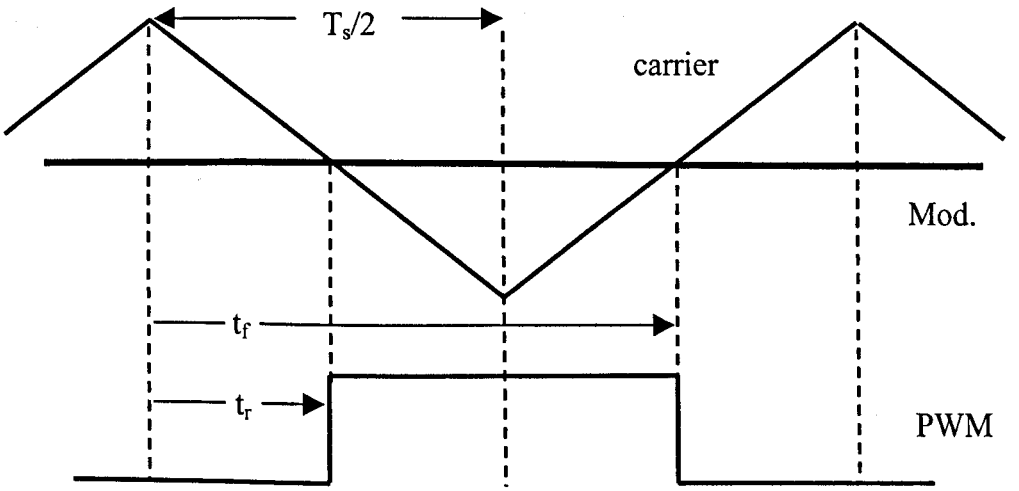

Figure 3.1 – Rising and Falling Edge Times

The PWM pulses in the 0-60° sextant are considered. Two general equations are developed that describe the angular position of the p^{th} rising and the p^{th} falling edges of a pulse, where p=1, 2, 3 ...$(f_s-3)/6$. See Equations (3.19) and (3.20). (By referring to Figure 2.2, we see that the number of edges in 60° is $(f_s-3)/6$).

$$x_p = \phi_p - \frac{M\phi_p}{2p}\sin(\phi_p) \tag{3.19}$$

$$y_p = \phi_p + \frac{M\phi_p}{2p}\sin(\phi_p) \tag{3.20}$$

x_p and y_p are the angular positions of the p^{th} rising and p^{th} falling edges respectively, M is the modulation index and $\phi_p=\omega_m T_s p$. Note that these equations are for the first PWM carrier where the pulses are sampled and centred about T_s, $2T_s$, $3T_s$...$(f_s-3)T_s/6$ and the modulating function is given by Equation (2.2a).

Considering only the rising edges, Equation (3.19) can be substituted into Equation (3.8) to give

$$b_n = \frac{2}{n\pi}\sum_{p=1}^{\frac{fs-3}{6}} j_p \cos\left(n\phi_p - \frac{nM\phi_p}{2p}\sin\phi_p\right) \tag{3.21}$$

This equation can be compared with the Bessel Equation (3.9) and the FM Equation (3.13).

The cosine term in Equation (3.21) can be expanded using the identity cos(A-B)=cosAcosB+sinAsinB, where $A = n\phi_p$ and $B = \frac{nM\phi_p}{2p}\sin\phi_p$. The cosAcosB term is an "even" function whilst the sinAsinB term is "odd". The cosAcosB term can be discarded, as it is known that the only terms of interest are "odd". Thus using Equation (3.21) and the "odd" part of the identity we get

$$\sin A \sin B = \sin(n\phi_p)\sin\left(\frac{nM\phi_p}{2p}\sin\phi_p\right) = \sin(n\phi_p)e(\phi_p) \qquad (3.22)$$

The second term in Equation (3.22), $e(\phi_p)$, is now itself expanded in a Fourier series in q by using the standard integral form of the Fourier expansion for odd coefficients, Equation (3.3), to give

$$b_q = \frac{1}{\pi}\int_0^{2\pi}\sin\left(\frac{nM\phi_p}{2p}\sin\phi_p\right)\sin(q\phi_p)dt \qquad \text{q=odd} \qquad (3.23)$$

Comparing Equation (3.23) to the Bessel Equation (3.12) we can reduce Equation (3.23) to Equation (3.24) which contains only odd Bessel functions

$$b_q = 2J_q(x) \qquad \text{q=odd} \qquad (3.24)$$

where x, the argument of the Bessel function, is given by $x=nM\phi_p/2p$. The Fourier series is found by substituting Equation (3.24) into Equation (3.4), where $a_0=a_q=0$, to give

$$\sin(n\phi_p)e(\phi_p) = 2\sin(n\phi_p)\sum_{q=odd}^{\infty}J_q(x)\sin(q\phi_p) \qquad (3.25)$$

In practice, the series will not need to be summed over infinity as it will converge before this point. Back-substituting Equation (3.25) into Equation (3.21) we get Equation (3.26) which is the contribution of the rising edges of the PWM scheme to the total harmonic spectrum from 0-60° of the input current.

$$b_n = \frac{4I_{dc}}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x)\sin(q\phi_p)\sin(n\phi_p) \tag{3.26}$$

Where the jumps, j_p, in Equation (3.21) are all constant and equal to the dc current, I_{dc}, as pulses of constant height are drawn out of / pushed into the supply phases.

We now consider the contribution made by the falling edges in the 0-60° sextant to the total harmonic spectrum. The b_n coefficient expression for the falling edges will be similar to that of the rising edges because the only difference between Equations (3.19) and (3.20) is the sign of the second term. Also, the sign of the jumps is now $-I_{dc}$ instead of I_{dc}. Repeating the method by which Equation (3.26) was found (the identity cos(A+B)=cosAcosB-sinAsinB is used and only the –sinAsinB terms kept) yields the fact that the falling edge expression is identical to the rising edge expression. Thus by superposition, the combined rising and falling edge contribution to the total spectrum is simply twice that of Equation (3.26), to give Equation (3.27), where the identity $\sin\left(\frac{A+B}{2}\right)\sin\left(\frac{A-B}{2}\right) = -\frac{1}{2}(\cos A - \cos B)$ has also been used ($A=n\phi_p+q\phi_p$ and $B=n\phi_p-q\phi_p$) to transform the equation into sums of sideband pairs.

$$b_n = \frac{4I_{dc}}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x)\left[\cos(n-q)\phi_p - \cos(n+q)\phi_p\right] \tag{3.27}$$

The 120-180° sextant is considered next. These pulses use the second carrier (see Figure 2.2) and are sampled and centred about $T_s/2$, $3T_s/2$, $5T_s/2$....$(f_s-3)T_s/6$. The sinusoidal modulating signal is given by Equation (2.2b). The actual form of the final equation for this sextant's contribution will be similar to Equation (3.27), only with the following transformations

$$\phi_p \rightarrow \theta_p = \omega_m \frac{T_s}{2}(2p-1)$$

$$\sin(q\phi_p) \rightarrow \sin\left(q\theta_p + q\frac{2\pi}{3}\right)$$

$$\sin(n\phi_p) \rightarrow \sin\left(n\theta_p + n\frac{2\pi}{3}\right)$$

The sextant 60-120° is more complicated, as the current flowing is made up of the combined interleaved current pulses from two phases. When phases 'a' to 'b' are switching then carrier one is used, when phases 'a' to 'c' are switching then carrier two is used instead. Thus for phases 'a' to 'b', the following transformation only is made to Equation (3.27)

$$\sin(n\phi_p) \rightarrow \sin\left(n\phi_p + n\frac{\pi}{3}\right)$$

For the case when phases 'a' to 'c' are switching, the following transformations are made to Equation (3.27)

$$\phi_p \rightarrow \theta_p = \omega_m \frac{T_s}{2}(2p-1)$$

$$\sin(q\phi_p) \rightarrow \sin\left(q\theta_p + q\frac{2\pi}{3}\right)$$

$$\sin(n\phi_p) \rightarrow \sin\left(n\theta_p + n\frac{\pi}{3}\right)$$

These four contributions are summed to give Equation (3.28) and this equation completely describes the coefficients of the ac input current harmonics, b_n.

$$b_n = \frac{4I_{dc}}{n\pi}\sum_{p}^{\frac{fs-3}{6}}\sum_{q=odd}^{\infty} J_q(x)\left[\cos(n-q)\phi_p - \cos(n+q)\phi_p\right.$$

$$+\cos\left((n-q)\phi_p + n\frac{\pi}{3}\right) - \cos\left((n+q)\phi_p + n\frac{\pi}{3}\right)$$

$$+\cos\left((n-q)\theta_p + (n-2q)\frac{\pi}{3}\right) - \cos\left((n+q)\theta_p + (n+2q)\frac{\pi}{3}\right)$$

$$\left.+\cos\left((n-q)\theta_p + (n-q)\frac{2\pi}{3}\right) - \cos\left((n+q)\theta_p + (n+q)\frac{2\pi}{3}\right)\right] \qquad (3.28)$$

An explanation of the meaning of this equation would be that the harmonic contribution of each edge of the PWM signal over one mains cycle is considered individually. Thus the PWM signal is resolved into a sum of odd, symmetrical squarewaves, where there are as many squarewaves as there are positive (or negative) edges. By superposition, the sums of the coefficients of these individual series give the Fourier coefficients of the overall PWM waveform.

In summary, for each p^{th} pulse, the odd Fourier coefficients are found in n, Equation (3.21). These coefficients are found by making use of the FTJ which focuses on the jumps of the pulses. Equation (3.21) is simplified by expanding it in an odd Fourier series in q and making use of the Bessel functions in order to simplify it.

Equation (3.28) was processed using MathCAD™ (see Appendix A3 for the listing) and Figures 3.2 to 3.5 show the harmonics centred around ω_s, centred around $2\omega_s$, centred around $3\omega_s$ and the harmonics up to $3\omega_s$ for the same conditions as those shown in the PSpice™ plots, Figures 2.16 to 2.19. A further check can be made on Equation (3.28) by plotting the series. Using Equation (3.4) and (3.28) the series sum equation is given by Equation (3.29) and the result is plotted in Figure 3.6.

$$I_a(t) = \sum_{n=odd}^{\infty} b_n \sin(n\omega_m t) \tag{3.29}$$

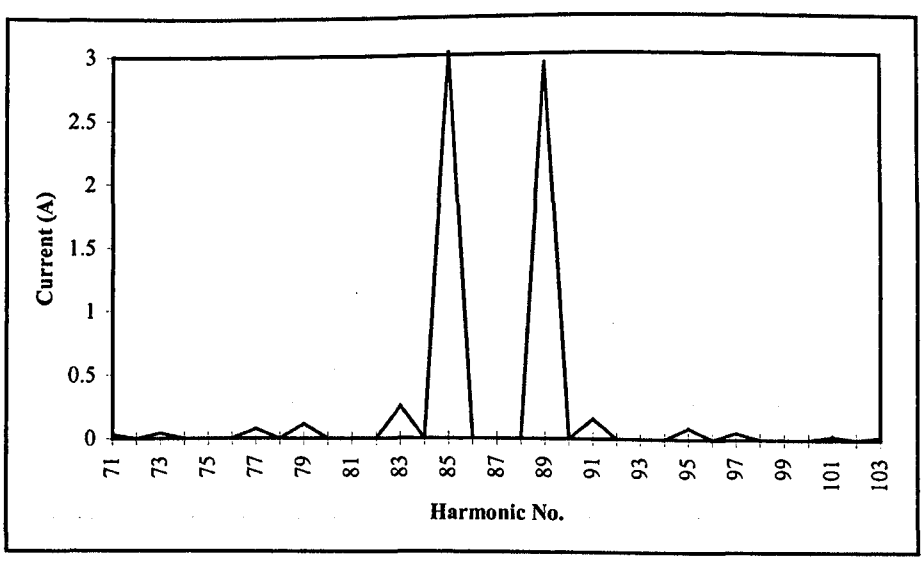

Figure 3.2 – Input Current Harmonics Centred About ω_s

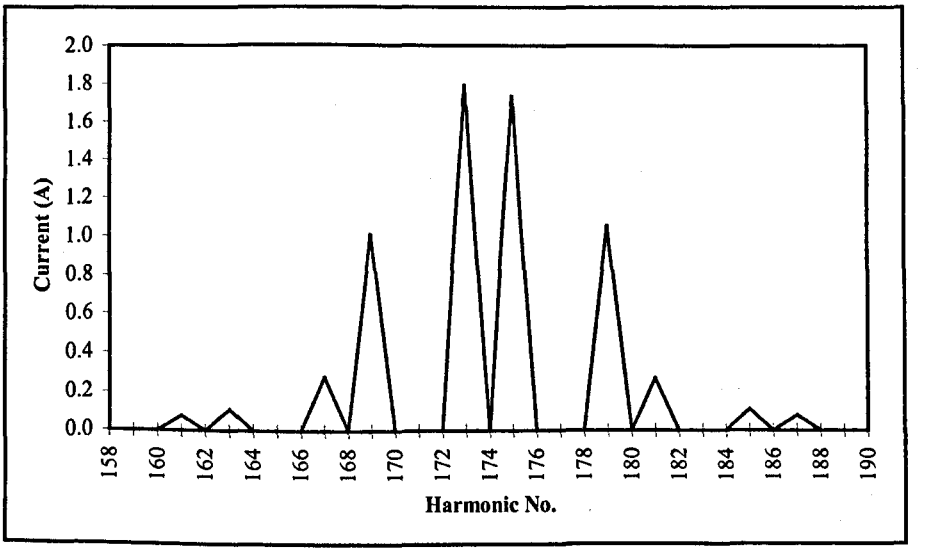

Figure 3.3 – Input Current Harmonics Centred About $2\omega_s$

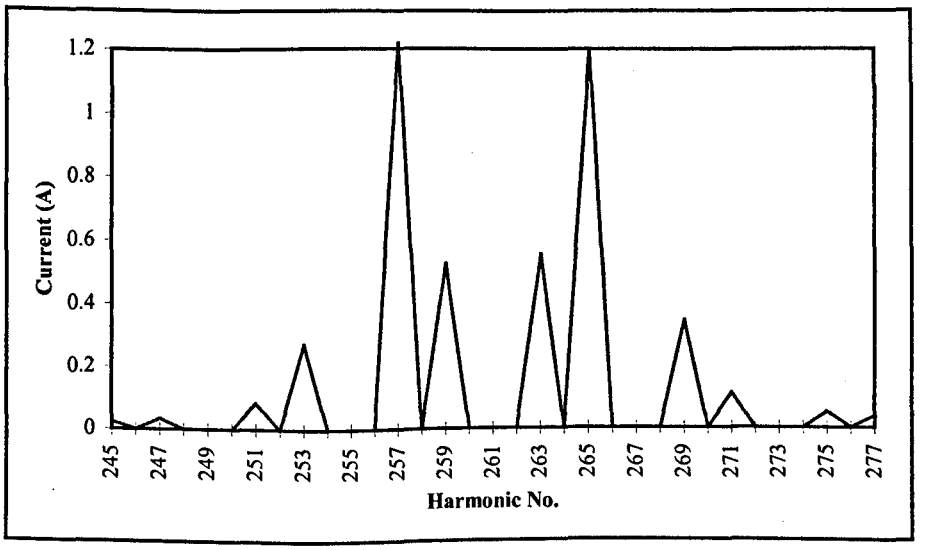

Figure 3.4 – Input Current Harmonics Centred About $3\omega_s$

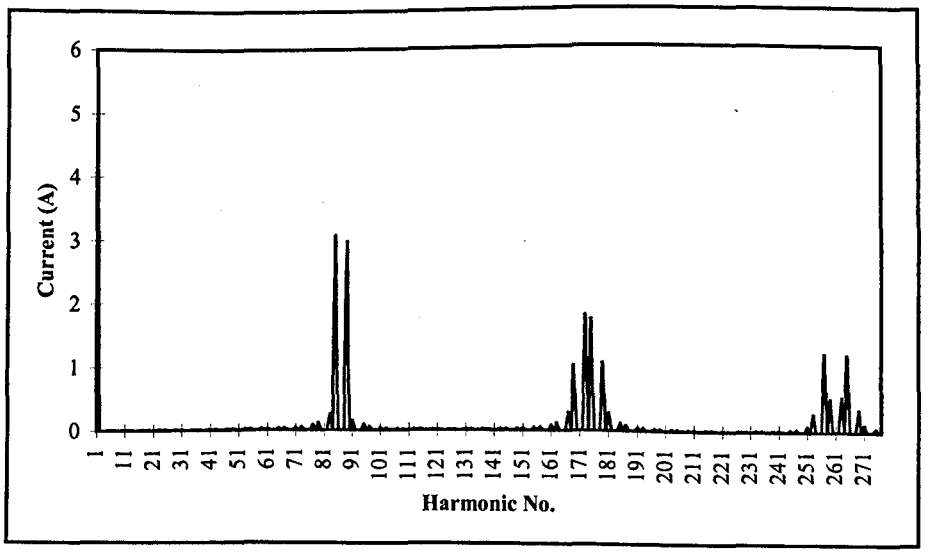

Figure 3.5 – Input Current Harmonic Spectrum Up To $3\omega_s$

Comparison of these four figures with the PSpice™ plots (Figures 2.16 to 2.19) demonstrates excellent agreement in terms of position and magnitude of the sidebands; $I(\omega_m)$=5.5A, $I(\omega_s \pm 2\omega_m)$=3A, $I(2\omega_s \pm \omega_m)$=1.7A, $I(2\omega_s \pm 5\omega_m)$=1A, $I(3\omega_s \pm 2\omega_m)$=0.5A, $I(3\omega_s \pm 4\omega_m)$=1.2A for the conditions M=0.577 and I_{dc}=9.5A.

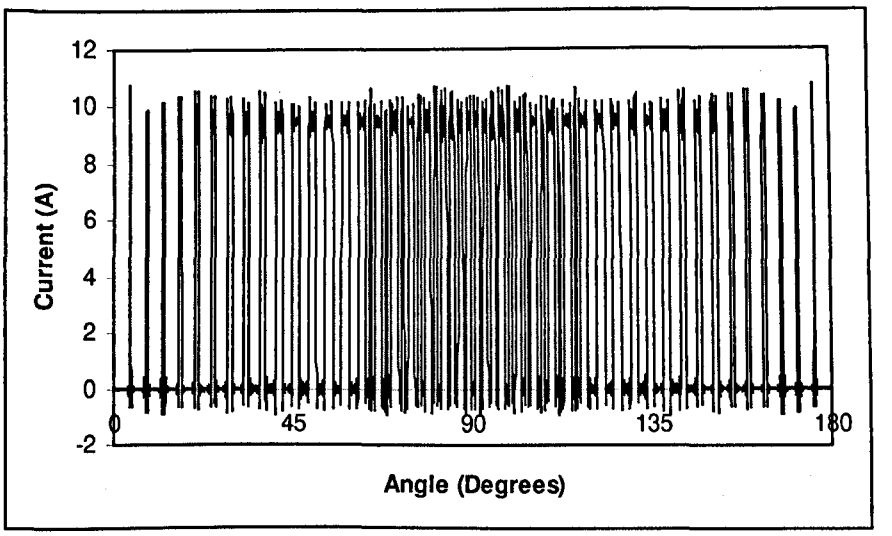

Figure 3.6 – Input Current Series Sum

Figure 3.6 shows the first half cycle of the mains phase current. Note that the 'ringing' on the edges of the pulses is due to Gibbs' phenomenon which states that the Fourier series cannot converge uniformly around a discontinuity and so we get spikes that tend to zero in width but not in height. A number of observations concerning the harmonic spectra of the input current are noted:-

1. The harmonics occur in "combs" made up of sideband pairs around multiples of the switching frequency, where each harmonic is a multiple of the modulating frequency
2. There are no low frequency components apart from the fundamental and no ω_s component. Instead, the power around ω_s is concentrated in two sidebands at $\omega_s \pm 2\omega_m$.
3. As the frequency is increased from ω_s, $2\omega_s$, $3\omega_s$ etc., so the harmonic sideband pairs become more distant from these central frequencies. Around ω_s, the dominant sidebands are positioned at $\omega_s \pm 2\omega_m$ whilst around $3\omega_s$ they are at

$3\omega_s \pm 4\omega_m$ and this trend continues with greater power being concentrated in the more distant sidebands. Also, as M is increased the same effect occurs, so that around $3\omega_s$ (for example), for M increasing from 0.5 to 1.0, power is concentrated at $(3\omega_s \pm 4\omega_m)$ then $(3\omega_s \pm 2\omega_m$ and $3\omega_s \pm 4\omega_m)$ then $(3\omega_s \pm 2\omega_m$, $3\omega_s \pm 4\omega_m$ and $3\omega_s \pm 8\omega_m)$ and finally just at $(3\omega_s \pm 8\omega_m)$. For M decreasing from 0.5 to 0 the power is concentrated at $(3\omega_s \pm 4\omega_m)$ then $(3\omega_s \pm 4\omega_m$ and $3\omega_s \pm 2\omega_m)$ and finally just $(3\omega_s \pm 2\omega_m)$. Both of these effects are due to the nature of the behaviour of Bessel functions. As the arguments of the Bessel functions, $x=nM\phi_p/2p$, increase, so greater power becomes concentrated in more distant sidebands.

4. The positioning of the sidebands themselves follow certain rules. Considering those sidebands around ω_s (for example), then it is noted that no even harmonics occur because the input current has been assumed a priori to be an odd function. There are no harmonics positioned at frequencies like ω_s, $\omega_s \pm 6\omega_m$ and $\omega_s \pm 12\omega_m$ etc. because these are triplen frequencies and for a balanced three-phase supply no triplen currents flow.

5. There is an underlying FM process in the input current harmonics, c.f. Equation (3.14) with (3.28)

3.3.2 Analysis of the Converter Output Voltage Harmonics Using the CAPWM Scheme

The assumptions made for carrying out the analysis are as follows:

1. The PWM scheme is synchronous where $\omega_m=1$ rad/s

2. "Even" symmetry exists about the 180° point of the output voltage, therefore $b_n=0$

3. A dc component, a_0, exists whose magnitude is given by Equation (2.4a)

4. The magnitudes of the falling and rising edges of the voltage pulses are variable and depend on the instantaneous line voltages.

The 0-60° sextant is considered first. The position of the p^{th} rising and p^{th} falling edges are given by Equations (3.19) and (3.20). The output voltage is an "even" function so only the FTJ Equation (3.7) need be used. Considering the rising edges, then substituting Equation (3.19) into Equation (3.7) gives Equation (3.30), which is the contribution of the rising edges from 0-60°, $a1_n$, to the total "even" coefficients, a_n.

$$a1_n = \frac{-2}{n\pi}\sum_{p=1}^{\frac{fs-3}{6}} j_p \sin\left(n\phi_p - \frac{nM\phi_p}{2p}\sin\phi_p\right) \tag{3.30}$$

For the falling edges, substituting Equation (3.20) into Equation (3.7) gives Equation (3.31), where $a2_n$ is the contribution of the falling edges.

$$a2_n = \frac{-2}{n\pi}\sum_{p=1}^{\frac{fs-3}{6}} j_p \sin\left(n\phi_p + \frac{nM\phi_p}{2p}\sin\phi_p\right) \tag{3.31}$$

The sin(A±B) terms in Equations (3.30) and (3.31) can be expanded using the identities sin(A±B)=sinAcosB±sinBcosA, where $x=nM\phi_p/2p$, $A=n\phi_p$ and $B=x\sin\phi_p$. The magnitudes of the jumps, j_p, in Equations (3.30) and (3.31) are equal, but the signs of the j_p in Equation (3.31) are negative as they are falling edges. Substituting the identities and subtracting Equation (3.31) from (3.30) results in some terms cancelling and Equation (3.32), which is the total contribution of the "even" coefficients due to rising and falling edges over 0-60°.

$$a_n = a1_n - a2_n = \frac{4}{n\pi}\sum_{p=1}^{\frac{fs-3}{6}} j_p \cos(n\phi_p)\sin\left(x\sin(\phi_p)\right) \tag{3.32}$$

The $\sin(x\sin\phi_p)$ term in this equation can itself be expanded as an "odd" Fourier series in q (in a similar way to how Equation (3.25) was produced), to give

$$a_n = \frac{8}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x) j_p \cos(n\phi_p) \sin(q\phi_p) \tag{3.33}$$

During the 0-60° sextant, the line voltage for phases 'a' to 'c' is given by Equation (2.1a). Thus the p[th] jump value of the a-c line voltage is given by

$$j_p = \sqrt{3}V \sin\left(\phi_p + \frac{\pi}{3}\right) \tag{3.34}$$

Substituting Equation (3.34) into (3.33) we get Equation (3.35) which is the harmonic contribution of the rising and falling edges due to phases 'a' to 'c' being switched during the 0-60° sextant.

$$a_n(ac) = \frac{8\sqrt{3}V}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x) \sin\left(\phi_p + \frac{\pi}{3}\right) \cos(n\phi_p) \sin(q\phi_p) \tag{3.35}$$

Considering phases b-c switching during the 0-60° sextant, where carrier two is used, then the following transformations to Equation (3.35) are made

$$\phi_p \rightarrow \theta_p = \omega_m \frac{T_s}{2}(2p-1)$$

$$\sin\left(\phi_p + \frac{\pi}{3}\right) \rightarrow \cos(\theta_p)$$

$$\sin(q\phi_p) \rightarrow \sin\left(q\theta_p + q\frac{2\pi}{3}\right)$$

$$\cos(n\phi_p) \rightarrow \cos(n\theta_p)$$

This results in Equation (3.36), the contribution of phases 'b' to 'c' to the harmonic content of the output voltage.

$$a_n(bc) = \frac{8\sqrt{3}V}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x) \cos(\theta_p) \cos(n\theta_p) \sin\left(q\theta_p + q\frac{2\pi}{3}\right) \tag{3.36}$$

The output voltage harmonics also have 60° symmetry. Therefore the contributions of the 60-120° and 120-180° sextants will be the same as the 0-60° sextant. Therefore the total harmonic content will be three times the sum of Equations (3.35) and (3.36), and so $a_n = 3[a_n(ac) + a_n(bc)]$.

$$a_n = \frac{24\sqrt{3}V}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x) \left[\sin\left(\phi_p + \frac{\pi}{6}\right) \cos(n\phi_p) \sin(q\phi_p) \right.$$

$$\left. + \cos(\theta_p) \cos(n\theta_p) \sin\left(q\theta_p + q\frac{2\pi}{3}\right) \right] \qquad (3.37)$$

Equation (3.37) can be expanded using trigonometric identities. The sinAcosBsinC term can be expanded by using 2sinCcosB=sin(C-B)+sin(C+B) and then by using $2\sin A\sin(C \pm B) = \cos(A \pm C \mp B) - \cos(A \mp C \pm B)$. The cosDcosEsinF term is expanded in a similar manner and Equation (3.37) is transformed to give Equation (3.38)

$$a_n = \frac{6\sqrt{3}V}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x) \left\{ \cos\left[(n-q-1)\phi_p - \frac{\pi}{6}\right] - \cos\left[(n-q+1)\phi_p + \frac{\pi}{6}\right] \right.$$

$$+ \cos\left[(n+q-1)\phi_p - \frac{\pi}{6}\right] - \cos\left[(n+q+1)\phi_p + \frac{\pi}{6}\right]$$

$$- \sin\left[(n-q-1)\theta_p - q\frac{2\pi}{3}\right] + \sin\left[(n-q+1)\theta_p - q\frac{2\pi}{3}\right]$$

$$\left. - \sin\left[(n+q-1)\theta_p + q\frac{2\pi}{3}\right] + \sin\left[(n+q+1)\theta_p + q\frac{2\pi}{3}\right] \right\} \qquad (3.38)$$

Thus the two terms of Equation (3.37) each give rise to four sidebands. Equation (3.37) was processed using MathCAD™ (see Appendix A4 for the listing) and Figures 3.7 to 3.10 were plotted which show the harmonics centred around ω_s, centred around $2\omega_s$, centred around $3\omega_s$ and the harmonics up to $3\omega_s$ for the same conditions as those shown in Figures 2.20 to 2.22 which are the PSpice™ plots. A further check can be made on Equation (3.37) by plotting the series. Using Equation (3.4) and (3.37) the series sum equation is given by Equation (3.39) and the result is plotted in Figure 3.11.

$$V_{out}(t) = a_0 + \sum_{n=even}^{\infty} a_n \cos(n\omega_m t) \qquad (3.39)$$

The dc voltage, a_0=1.5MV. The series, $V_{out}(t)$, can be applied to an inductor in series with the parallel combination of a dc voltage source (to simulate the large capacitor) and resistive load. The characteristic dc side ripple current waveform results in Figure 3.12.

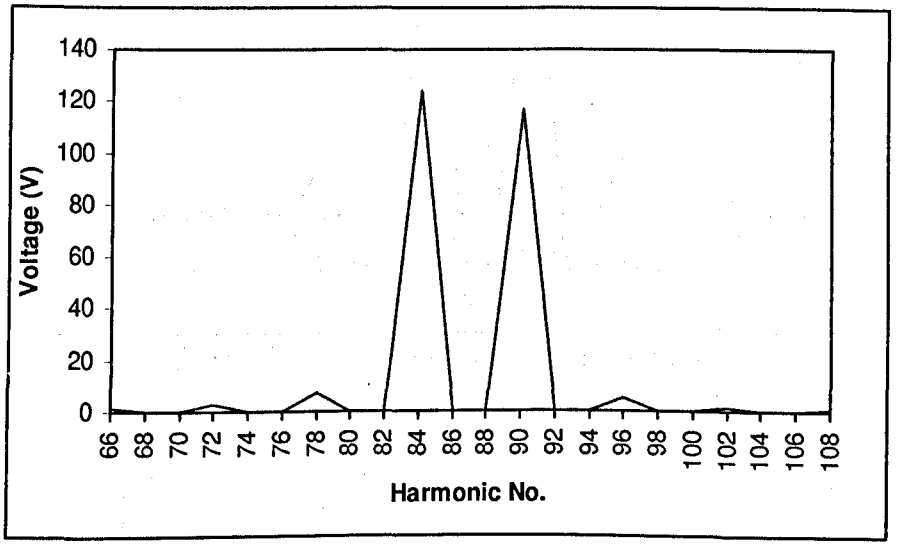

Figure 3.7 – Harmonics Centred About ω_s

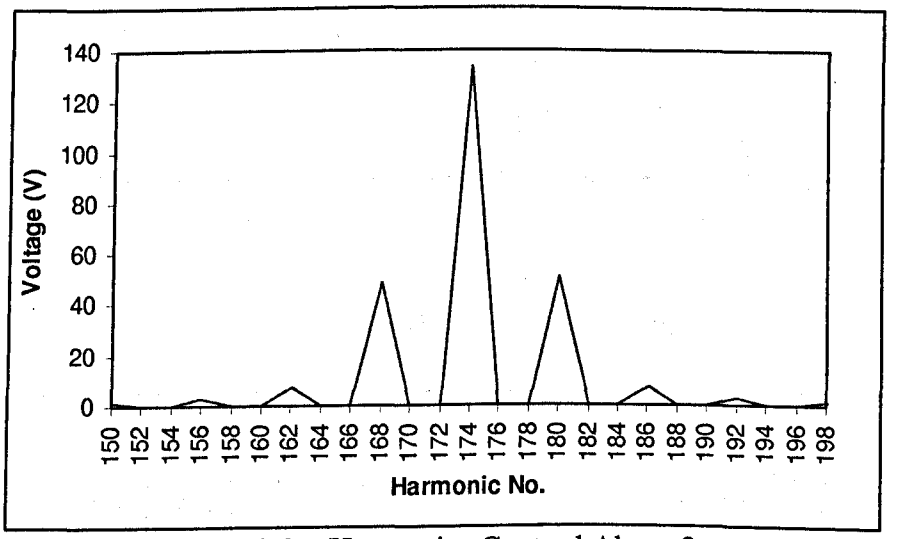

Figure 3.8 – Harmonics Centred About $2\omega_s$

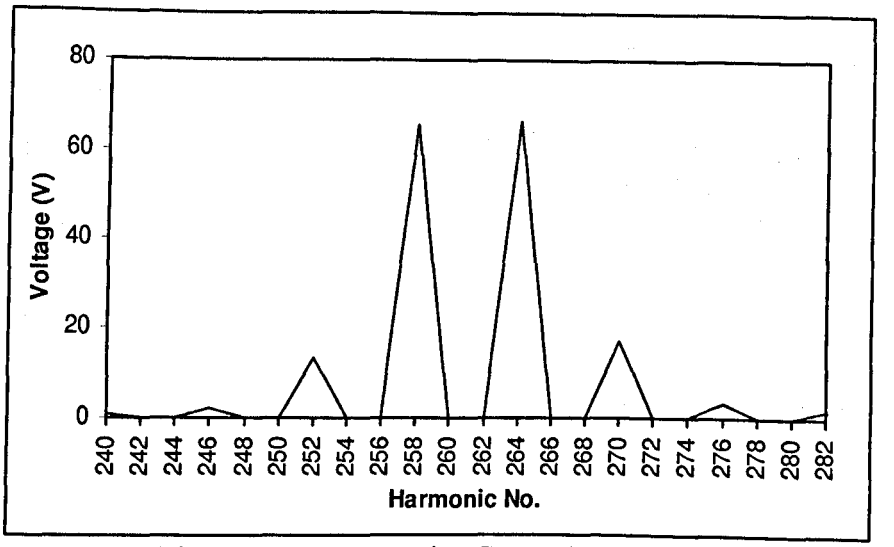

Figure 3.9 – Harmonics Centred About $3\omega_s$

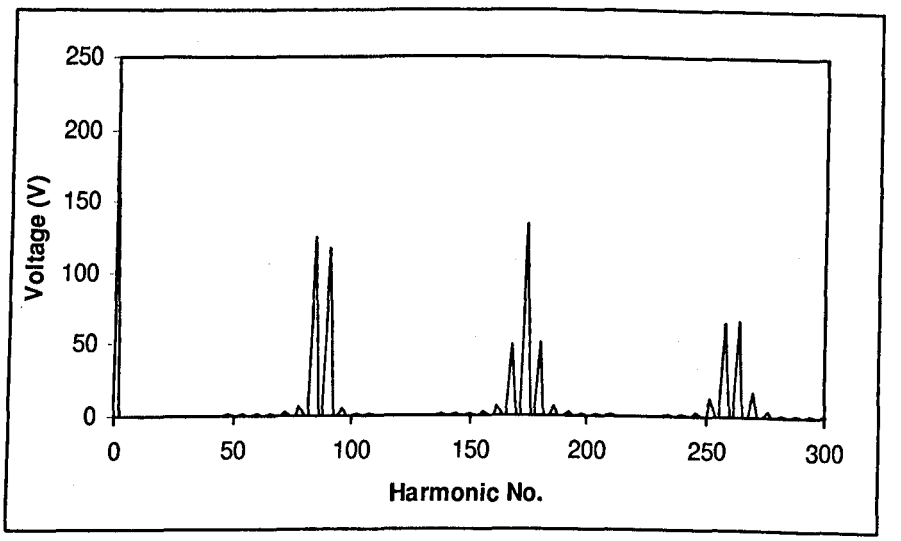

Figure 3.10 – Harmonics up to $3\omega_s$

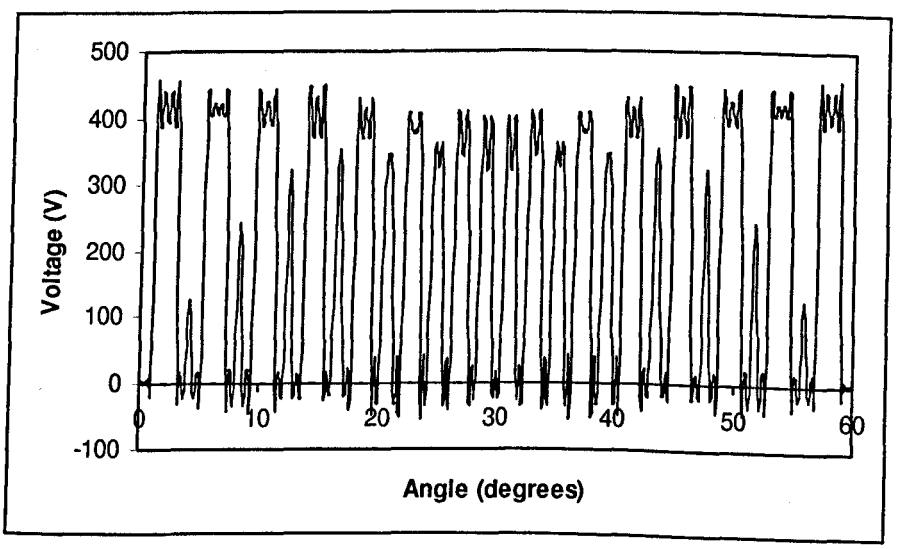

Figure 3.11 – The DC Output Voltage, $V_{out}(\omega_m t)$

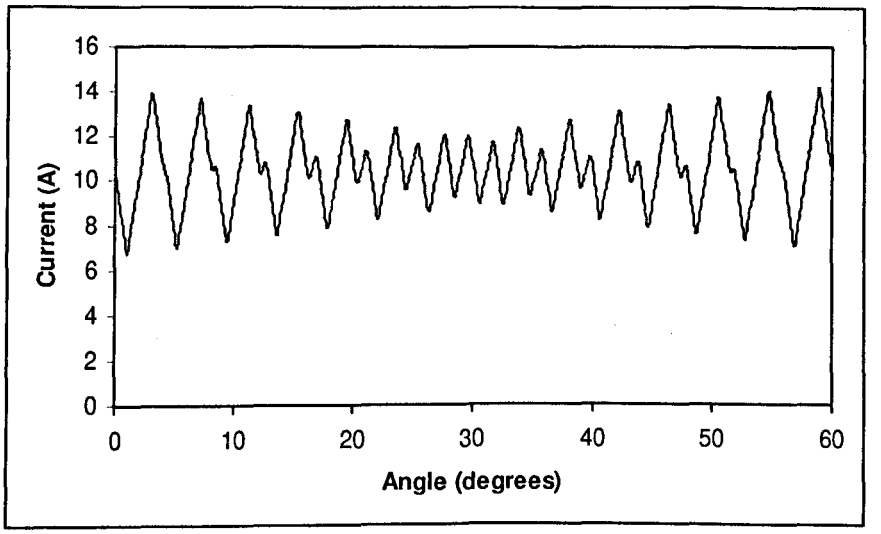

Figure 3.12 – DC Inductor Current $I_{dc}(\omega_m t)$

Figure 3.12 can also be produced by computing the dc current Fourier series from the voltage series. Each voltage harmonic is shifted by –90° when applied to the inductor and the harmonic voltages scaled by the impedance of the inductor at the frequency of each harmonic. The dc current series is found by using Equation (3.40) instead of (3.39), where L_{dc} is the dc inductance and R is the resistive load. This equation could also be used for the computation of the frequency dependant losses in the inductor core and windings. This computation would not include core gap effects and so these should be calculated separately.

$$I_{dc}(t) = \frac{a_0}{R} + \sum_{n=even}^{\infty} \frac{a_n}{n\omega_m L_{dc}} \cos\left(n\omega_m t - \frac{\pi}{2}\right) \tag{3.40}$$

A number of conclusions about the dc side harmonics are now stated:-

(1) The harmonics occur in "combs" in the same way as for the ac side harmonics.

(2) The low frequency content of the output only consists of a pure dc term

(3) The same argument given for the ac harmonics Bessel function behaviour applies here.

(4) The positioning of the dc side harmonics is such that only "even" harmonics are produced. A strong component at $2\omega_s$ is produced. The harmonics on the dc and ac sides are related and this relationship is explored in Section 3.6.

(5) The harmonics only occur at multiples of six of the modulating frequency. This is to be expected as the bridge output voltage has symmetry over each sextant (due to the basic three-phase rectification process).

(6) There are both FM and DSBM processes occurring in the output voltage harmonics. The DSBM is generated by the fact the FM process is multiplied by the sinusoidal jumps of the input voltages. Thus for every two FM produced sidebands, the DSBM process generates four sidebands.

3.3.3 Analysis of Two Converters Input Current Harmonics Using Dual Interleaved CAPWM Scheme

This arrangement consists of two converters driving a common load and sharing the same input filter, as examined in more detail in Chapter 5. The PWM scheme of the first converter is the same as the converter described previously. The second converter's PWM scheme (#2) places the pulses in antiphase with the first converter's PWM scheme (#1), as illustrated in Figure 3.13.

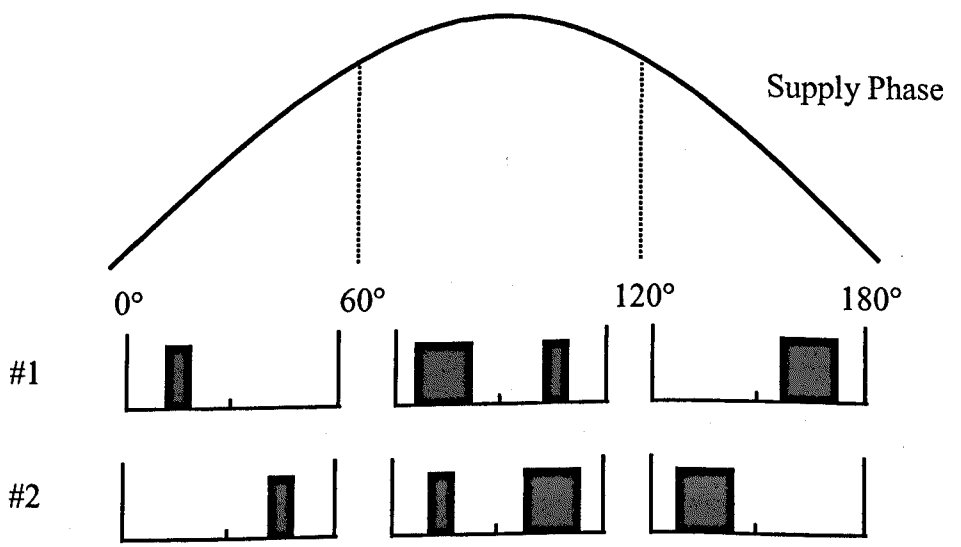

Figure 3.13 – Interleaving of PWM Pulses

The input current harmonic analysis of these interleaved converters will be the summation of Equation (3.28) with another similar equation with the position of the

relevant pulses moved by one angular switching cycle, i.e. ψ_p is used instead of ϕ_p to yield Equation (3.42), where ψ_p is given by Equation (3.41). In Equation (3.42) the first four terms are due to converter one and the last four due to converter two. Note that for a given value of M each converter now supplies half the current to the load, hence $I_{dc}/2$ instead of I_{dc} is used in Equation (3.42).

$$\psi_p = \omega_m \frac{T_s}{2}(2p-1) + \omega_m T_s \tag{3.41}$$

and

$$\begin{aligned} b_n = \frac{2I_{dc}}{n\pi} \sum_{p}^{\frac{fs-3}{6}} \sum_{q=odd}^{\infty} J_q(x) \Big[& \cos(n-q)\phi_p - \cos(n+q)\phi_p \\ & + \cos\left((n-q)\phi_p + n\frac{\pi}{3}\right) - \cos\left((n+q)\phi_p + n\frac{\pi}{3}\right) \\ & + \cos\left((n-q)\theta_p + (n-2q)\frac{\pi}{3}\right) - \cos\left((n+q)\theta_p + (n+2q)\frac{\pi}{3}\right) \\ & + \cos\left((n-q)\theta_p + (n-q)\frac{2\pi}{3}\right) - \cos\left((n+q)\theta_p + (n+q)\frac{2\pi}{3}\right) \\ & + \cos(n-q)\psi_p - \cos(n+q)\psi_p \\ & + \cos\left((n-q)\psi_p + n\frac{\pi}{3}\right) - \cos\left((n+q)\psi_p + n\frac{\pi}{3}\right) \\ & + \cos\left((n-q)\phi_p + (n-2q)\frac{\pi}{3}\right) - \cos\left((n+q)\phi_p + (n+2q)\frac{\pi}{3}\right) \\ & + \cos\left((n-q)\phi_p + (n-q)\frac{2\pi}{3}\right) - \cos\left((n+q)\phi_p + (n+q)\frac{2\pi}{3}\right) \Big] \end{aligned} \tag{3.42}$$

This equation is plotted using the MathCAD™ listing in Appendix A5. Note that the harmonics centred around ω_s, $3\omega_s$ ....etc. have been eliminated and the harmonics centred around $2\omega_s$, $4\omega_s$ ....etc. remain of the same magnitude and at the same position as in the case for a single converter.

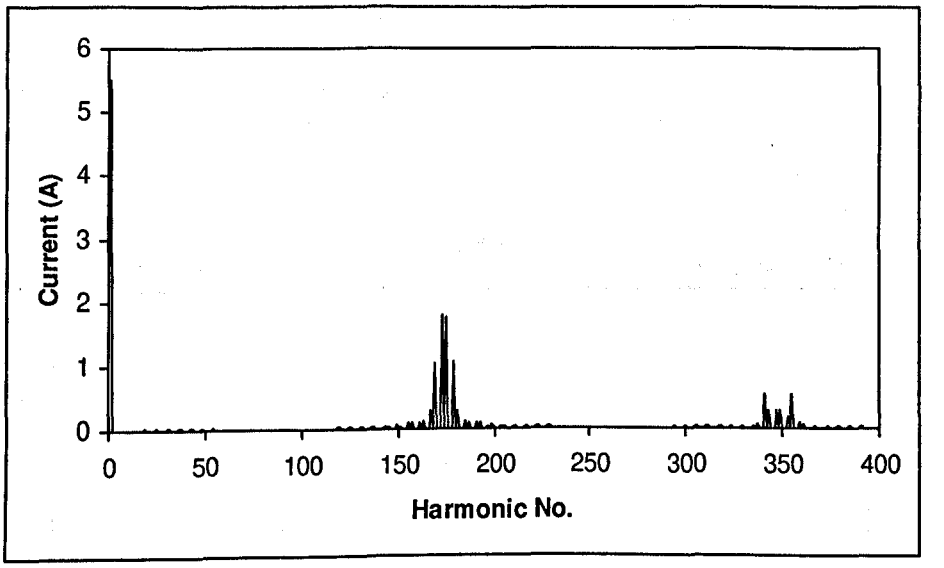

Figure 3.14 – Input Current Harmonics up to $4\omega_s$

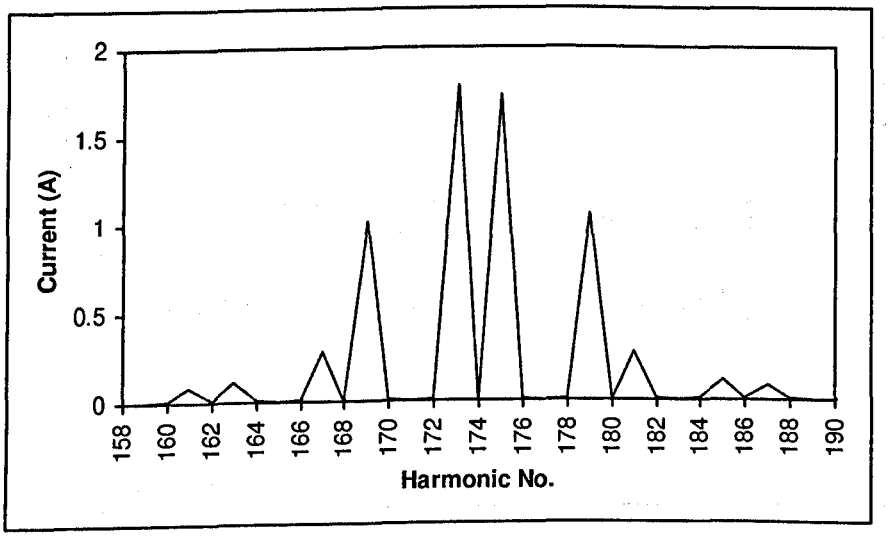

Figure 3.15 – Input Current Harmonics Centred Around $2\omega_s$

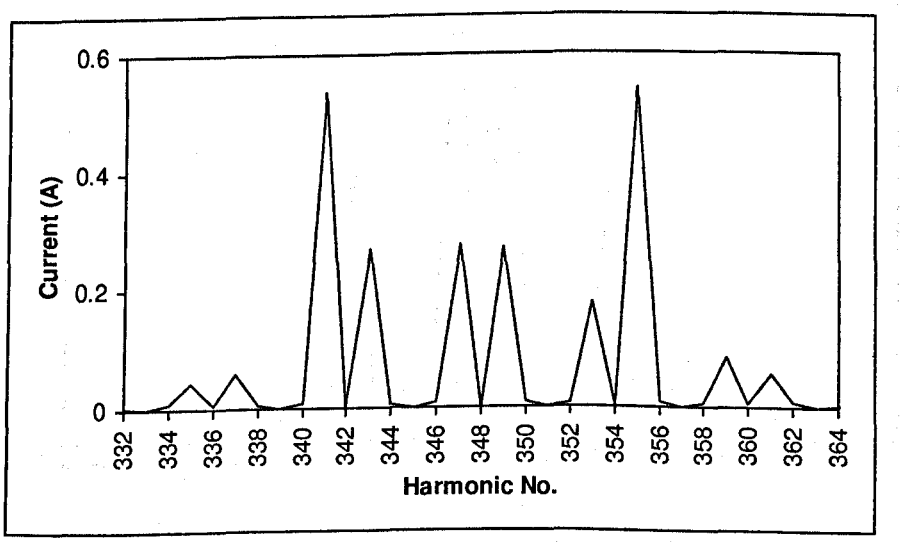

Figure 3.16 – Input Current Harmonics Centred Around $4\omega_s$

The PSpice™ simulation of two interleaved converters yielded similar results for the same conditions, see Figures 3.17 to 3.19.

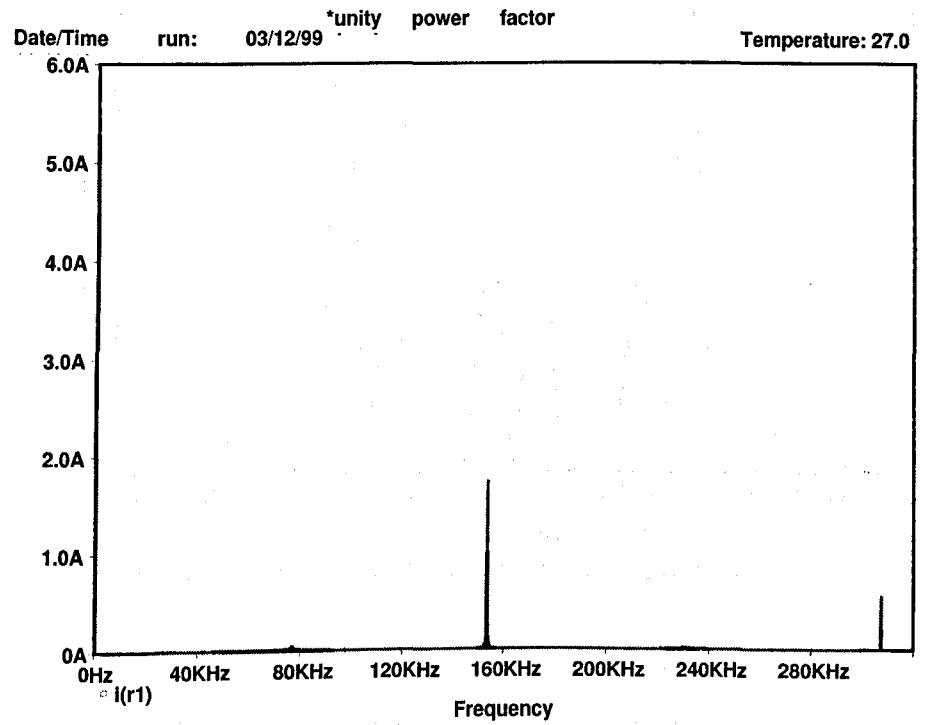

Figure 3.17 – Input Current Harmonics up to $4\omega_s$

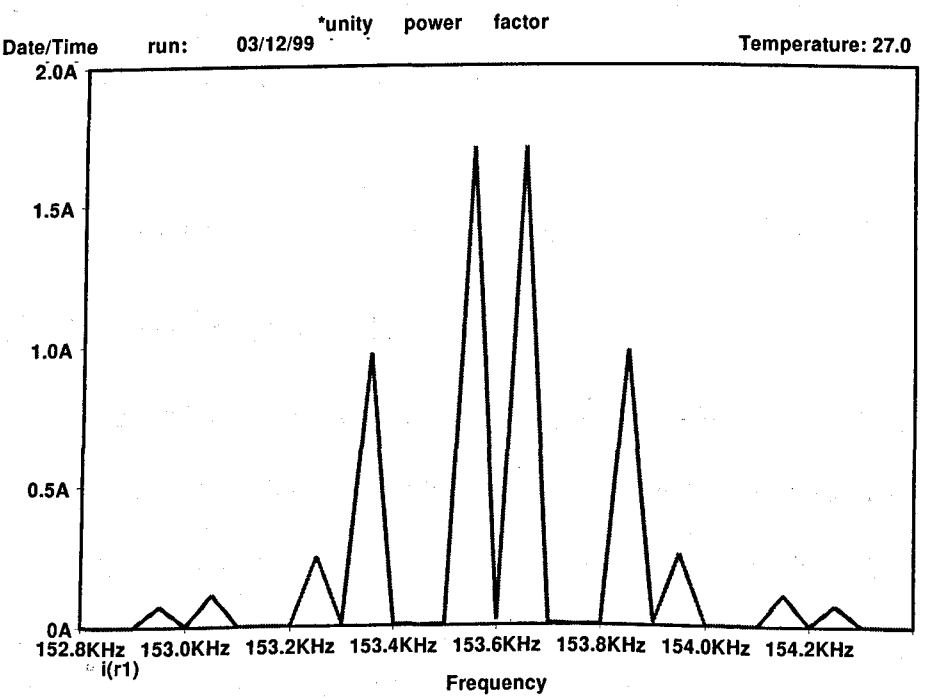

Figure 3.18 – Input Current Harmonics Centred Around $2\omega_s$

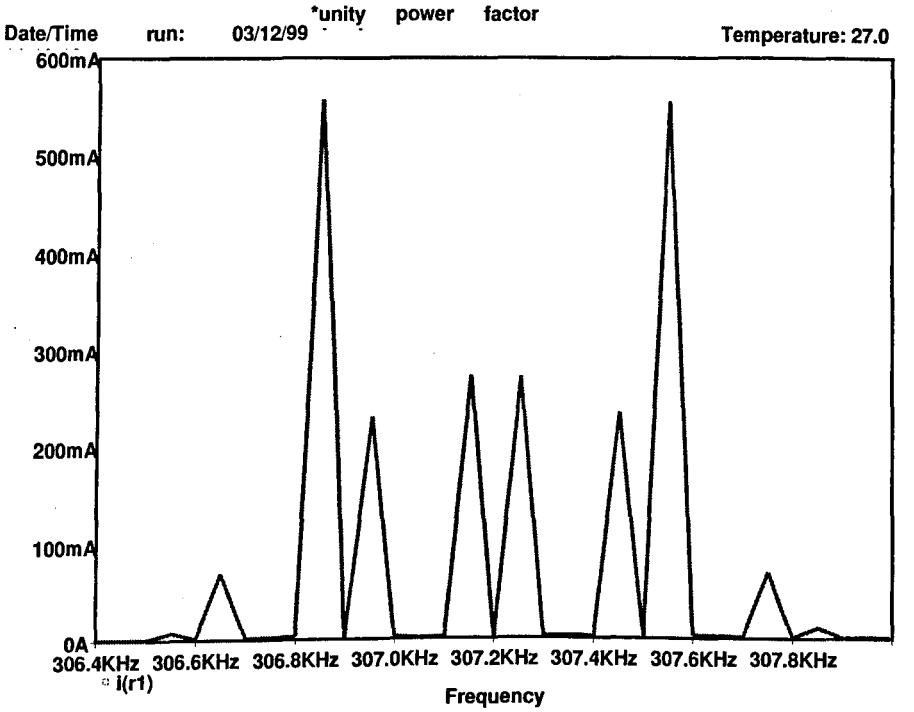

Figure 3.19 – Input Current Harmonics Centred Around $4\omega_s$

One possibility for extending this scheme for use in a single converter would be to operate the two different PWM schemes over alternate mains cycles in a multiplexing fashion. Over many mains cycles, the average magnitude of the harmonics around ω_s should be halved, so giving a reduction in harmonic distortion and input filter size without the need to use two paralleled converters.

3.4 Use of MathCAD™ to Analyse the Soft Switching Converter's Input Current Harmonics

The soft switching scheme is given in detail in Chapter 6. Analysis of the scheme could be carried out by hand by formulating equations as before. However, the scheme has an inherent lack of symmetry to it and the resultant formulae would be cumbersome and not yield much information about the nature of the harmonics. MathCAD™ can still be used to analyse these harmonics by using a piecewise FTJ approach, rather than trying to derive a closed form equation. A drawing of the PWM

scheme is shown in Figure 6.5 and from this each 30° section can be analysed using the FTJ. The input current, at the switching harmonic level, does not exhibit odd symmetry therefore both the a_n and b_n coefficients are found. The resulting magnitude of the n^{th} harmonic, c_n, is given by the vector sum

$$c_n = \sqrt{a_n^2 + b_n^2} \tag{3.43}$$

Considering the 0 to 30° portion then the position in time, x_p of the p^{th} rising edge is given by

$$x_p = pT_s - MT_s \sin(pT_s\omega_m) \tag{3.44}$$

where the magnitude of the jump is equal to the dc current, $j_p=I_{dc}$. The position in time, y_p, of the p^{th} falling edge is given by

$$y_p = pT_s \tag{3.45}$$

where the magnitude of the jump is $k_p=-I_{dc}$. This approach is repeated for each 30° section of the 360° waveform. From 60° to 120°, two pulses are present in each switching interval and so the length of each combined pulse is the sum of the individual lengths. See Appendix A6 for the listing. The coefficients are calculated using

$$a_n = \frac{-1}{n\pi}\sum_p \left(j_p \sin(nx_p\omega_m) + k_p \sin(ny_p\omega_m)\right) \tag{3.46}$$

and

$$b_n = \frac{1}{n\pi}\sum_p \left(j_p \cos(nx_p\omega_m) + k_p \cos(ny_p\omega_m)\right) \tag{3.47}$$

Input current harmonics are shown in Figures 3.20 to 3.23 where I_{dc}=10A, ω_s=90 rad/s and M=0.577. Note the presence of extra harmonics compared with the original PWM scheme. 5^{th}, 7^{th}, 11^{th} etc. harmonics exist due to the discontinuities at the 30° points in the modulation scheme where the leading and trailing PWM pulses swap positions to maintain the soft switching action. The positions of the switching harmonics have

changed to $\omega_s \pm \omega_m$, $\omega_s \pm 5\omega_m$, $2\omega_s \pm \omega_m$, $2\omega_s \pm 3\omega_m$ and $2\omega_s \pm 5\omega_m$ etc. compared with the original PWM scheme.

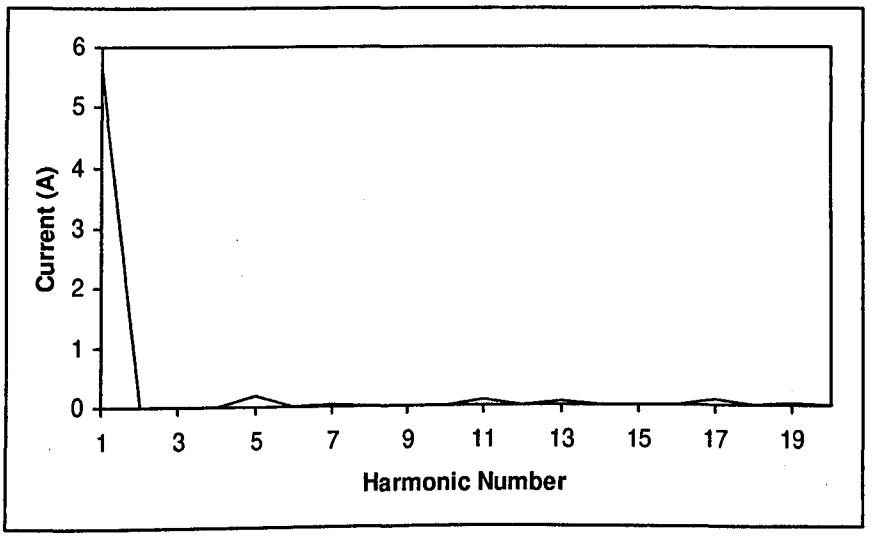

Figure 3.20 – Low Frequency Input Current Harmonics for Soft Switching

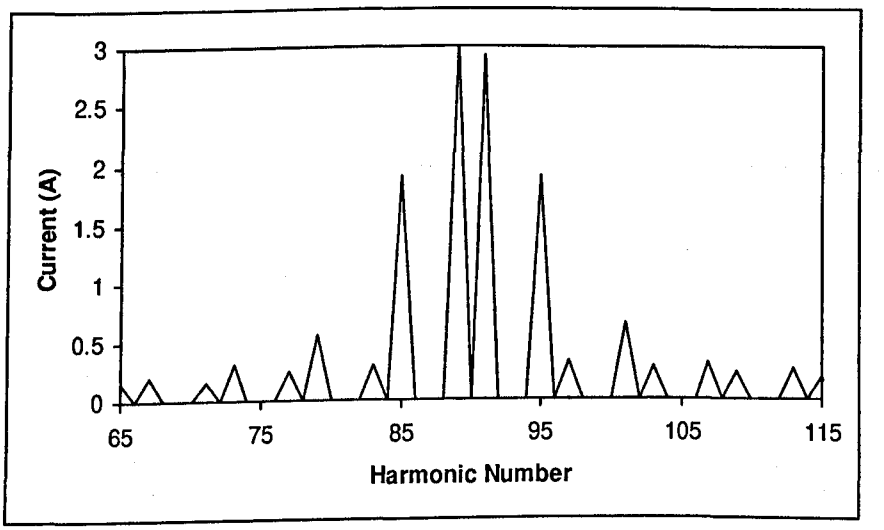

Figure 3.21 – Harmonics Centred Around ω_s for Soft Switching PWM

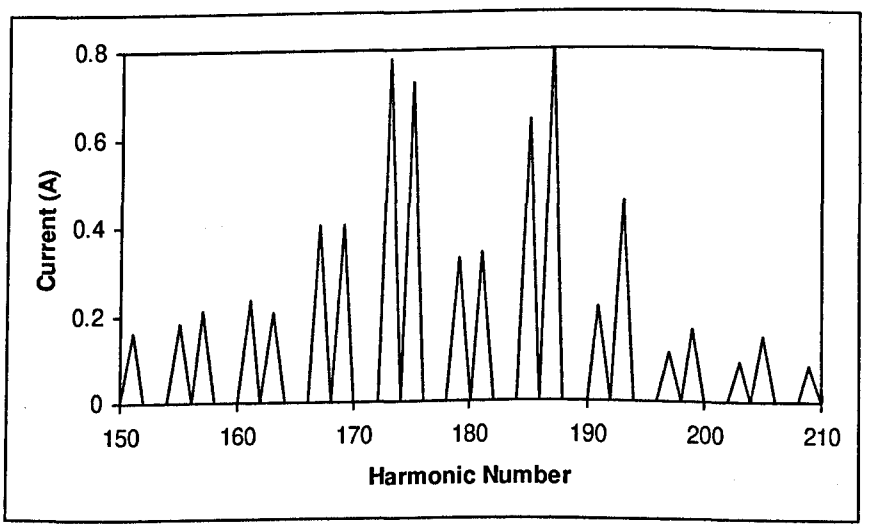

Figure 3.22 – Harmonics Centred Around $2\omega_s$ for Soft Switching PWM

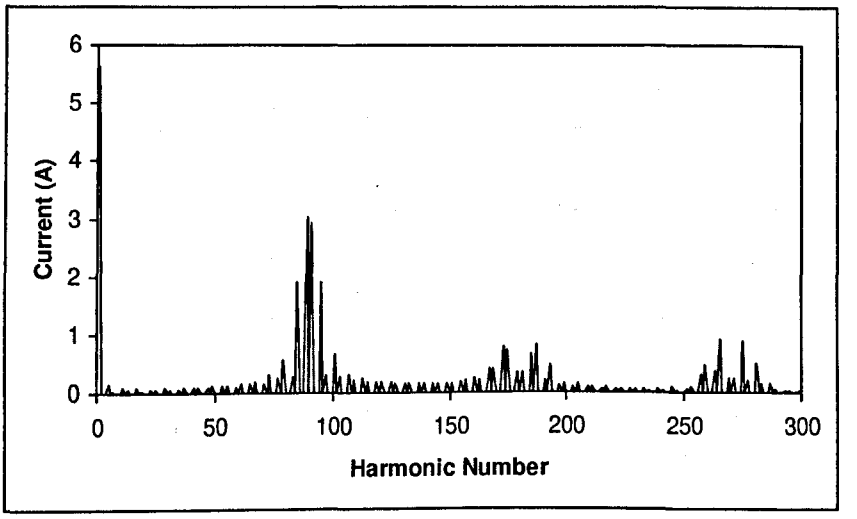

Figure (3.23)- Input Current Harmonics up to $3\omega_s$ for Soft Switching PWM

The series sum is given by Equation (3.48) and plotted in Figure 3.24 to prove the analysis

$$I_a(t) = \sum_{n=1}^{\infty} [a_n \cos(n\omega_m t) + b_n \sin(n\omega_m t)] \tag{3.48}$$

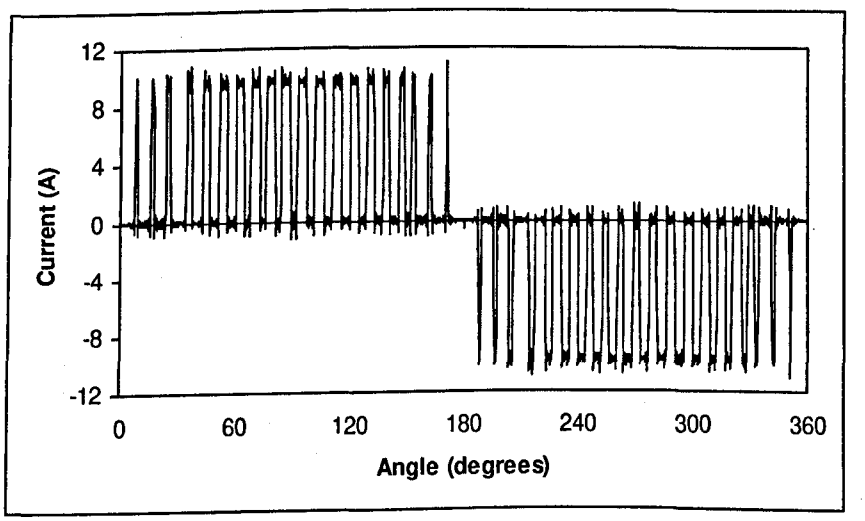

Figure 3.24 – Input Current for Soft Switching PWM

3.5 Practical Results

Practical results for one converter around ω_s are shown in Figure 3.25 and for two converters in Figure 3.26. Note the change in vertical scale showing that interleaving has reduced the harmonics around the switching frequency by a factor of approximately 2500.

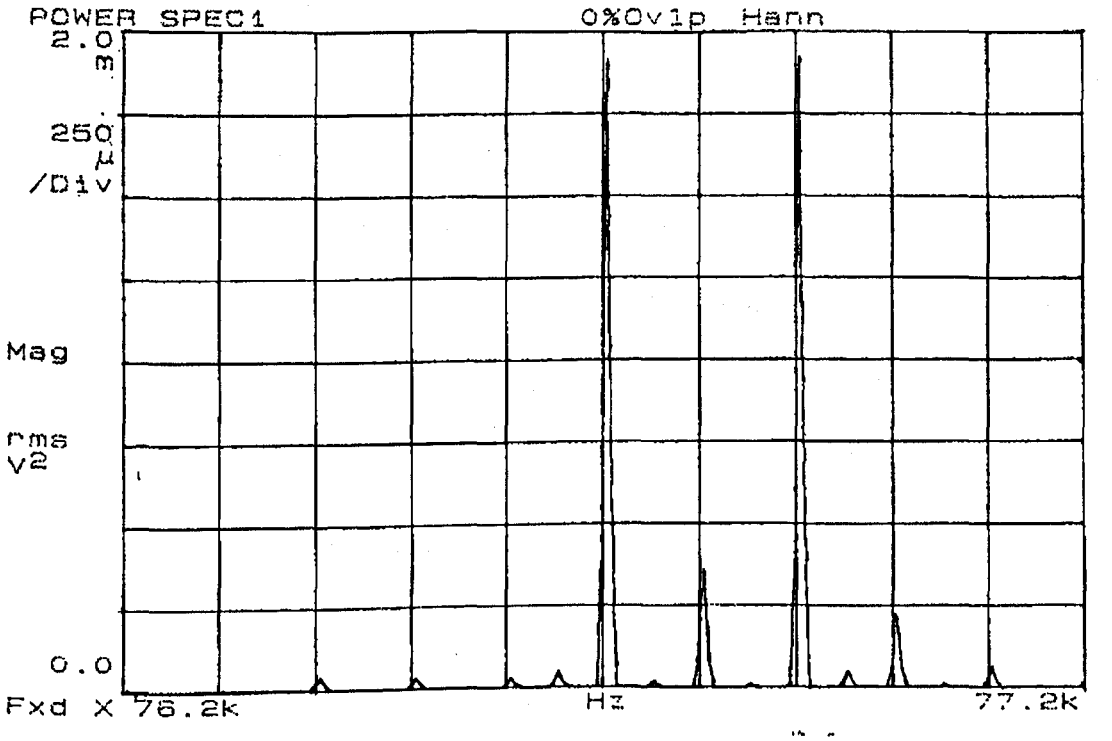

Figure 3.25 – Input Current Harmonics Around ω_s for One Converter

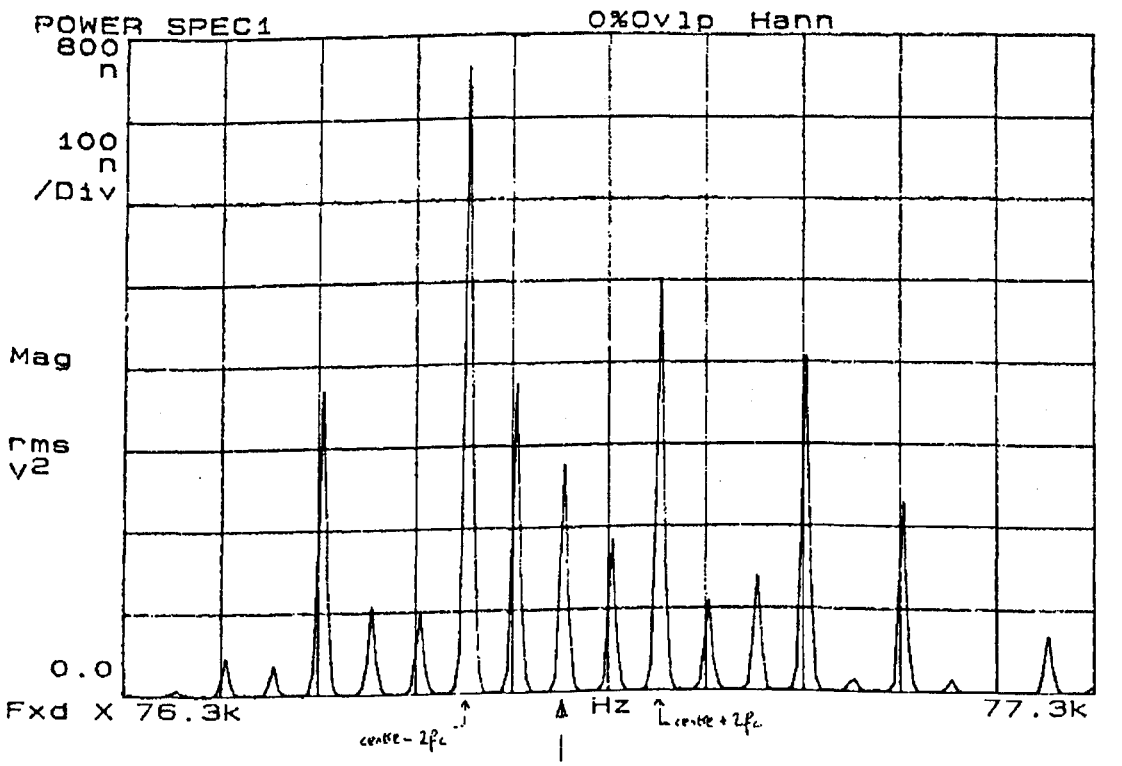

Figure 3.26 – Input Current Harmonics Around ω_s for Interleaved Converters

Switching Frequency Jitter

It is noted that the switching frequency production (from a mains frequency locked phase-locked-loop, PLL) is subject to jitter caused by the imperfect behaviour of

the PLL's voltage feedback loop. The feedback loop relies on a smoothing capacitor, which feeds a voltage controlled oscillator. Voltage ripple causes deviation of the output frequency and so the carrier frequency is not constant. This can have the beneficial effect of spreading the power seen in the main two sidebands around ω_s into several sidebands of smaller peak power, thereby reducing the filtering requirements. It is difficult to take frequency plot results as the requirements exceed the capability of the available instrumentation – i.e. the spectrum analyser must be capable of looking over at least a 20ms period and yet resolving up to at least ω_s.

3.6 The Effects of Distorted Phase Voltages and Harmonic Transfer

Distorted Phase Voltages

So far, all calculations have been carried out assuming purely sinusoidal phase voltages. In practice, the supplies have a certain amount of harmonic distortion, often caused by the distribution system supplying a significant non-linear/high crest factor load. A typical example of this would be personal computers, which almost universally feature a switched mode power supply utilising a bridge rectifier and large dc-smoothing capacitor front-end. As a result of this, current is only drawn at the peak of the phase voltages resulting in voltage drops in the system only for this time period, see Figure 3.25.

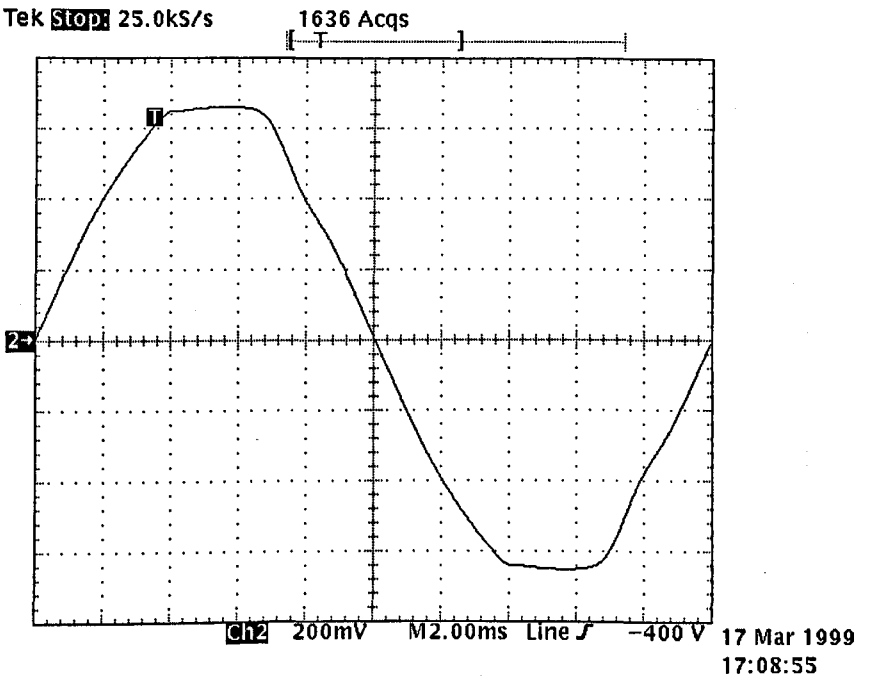

Figure 3.25 – Phase to Neutral Voltage (40V/div; 2ms/div)

This waveform was approximated to a flat-top sinusoid for the purpose of analysis in Figure 3.26. It has "odd" symmetry and is analysed using three Fourier series from 0 to θ, θ to π-θ and π-θ to π radians to gives the series sum by superposition in Equation (3.49). N.B. The fourth term in this equation is due to the n-1 factor in the denominators of one of the previous terms meaning that the case when n=1 needs to be derived separately. The equation is normalised to a peak supply voltage of unity and ω_m=1rad/s, where θ is the point at which the flat topped section begins.

$$f(t)=\frac{1}{\pi}\sum_{n=3,5..}^{\infty}\left[\frac{1}{n-1}\sin(n-1)\theta-\frac{1}{n+1}\sin(n+1)\theta\right.$$

$$-\frac{2\sin\theta}{n}[\cos(\pi-\theta)n-\cos(n\theta)]$$

$$\left.-\frac{1}{n-1}\sin[(n-1)\pi-(n-1)\theta]+\frac{1}{n+1}\sin[(n+1)\pi-(n+1)\theta]\right]\sin(nt)$$

$$+\frac{1}{\pi}[2\theta+\sin(2\theta)]\sin t \qquad (3.49)$$

For $\theta=\pi/3$ radians, the fundamental=94.2%, the 3rd harmonic=4.6%, the 5th harmonic=2.8% and the 7th harmonic=1%. The 9th harmonic is a factor of ten down on

the 7th. For θ=π/3 radians, Figure 3.26 shows how that even a relatively small amount of harmonic distortion can look worse than it actually is if these harmonics sum to act on the peak of the waveform.

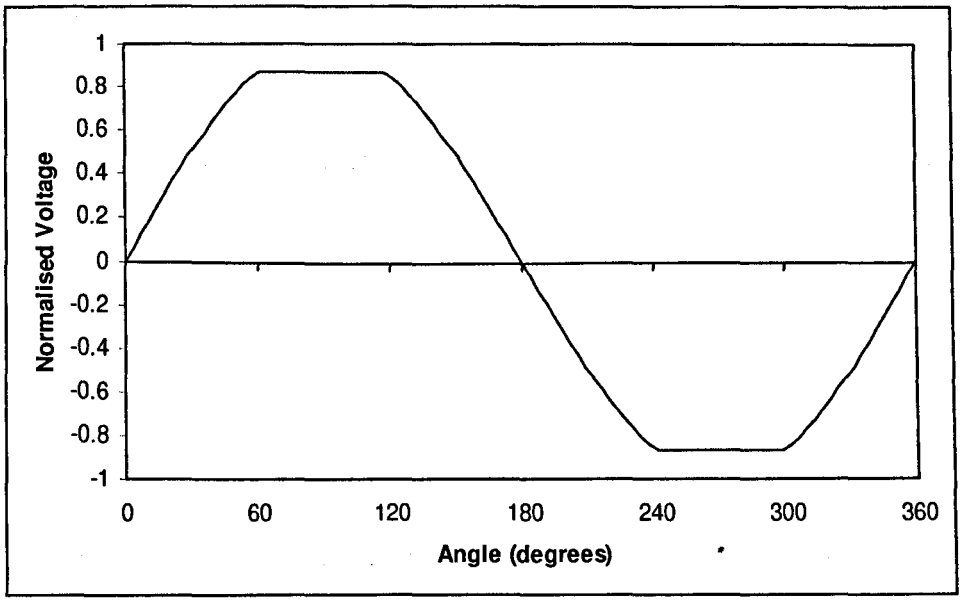

Figure 3.26 – Normalised Flat-Top Phase Voltage

In an ideal world, every non-linear load would feature a unity power factor stage at its front end and so there would be no mains voltage distortion. At the present moment in time this is not so and therefore the power converter used in this thesis that operates on the assumption of pure sinusoidal phase voltages will, in practice, draw harmonic currents. Previously, an over-sized dc inductor was used to improve the input current waveshape [3.12]. In Section 4.5.2 It is shown how that dc-side current feedback can accomplish the same task.

Harmonic Transfer

Previous work [3.7] investigated the general harmonic transfer process in power converters. It answered the question that if the ac mains voltages or currents contained certain harmonics, then which harmonics would be present on the dc side and vice versa. The converters analysed in this paper were the six-switch current source and six-switch voltage source type, using space vector PWM and it was stated that the rules

formulated applied generally. This statement is verified for the case of this thesis' converter and the harmonics produced by a flat-top phase voltage waveform examined. Whilst work has been done examining the effect of supply phase voltage unbalance [3.8, 3.9, 3.10] no work has been done looking at the specific and widespread problem of distorted (especially flat-topped) yet balanced mains voltages.

The switching cycle averaged operation of the converter was modelled using the software package MathCAD™ using the listing given in Appendix A7, where k is the amount of flat-topping in the phase voltages (k=1 implies no flat-topping), V=85V, R=15Ω, M=0.54, and L_{dc}=750μH. In the model, the modulating frequency is scaled by a factor of 1/50 to 1Hz and so the inductance is scaled to 37.5mH. For 10% flat top (k=0.9) the per switching cycle averaged bridge output voltage is given by Figure 3.27, where the dominant harmonic is clearly the 6^{th}. The other harmonics present are revealed using an FFT as being the 12^{th} and 18^{th} etc. Applying the voltage in Figure 3.27 to an inductor gives the dc side current, Figure 3.28, and then multiplying this current by the modulating functions yields the ac-side currents, Figure 3.29. An FFT reveals that the dominant harmonics are the 5^{th} and 7^{th} with small 11^{th} and 13^{th} components. These waveforms compare favourably with the practical results, taken under the same conditions, given by Figures 3.30 and 3.31.

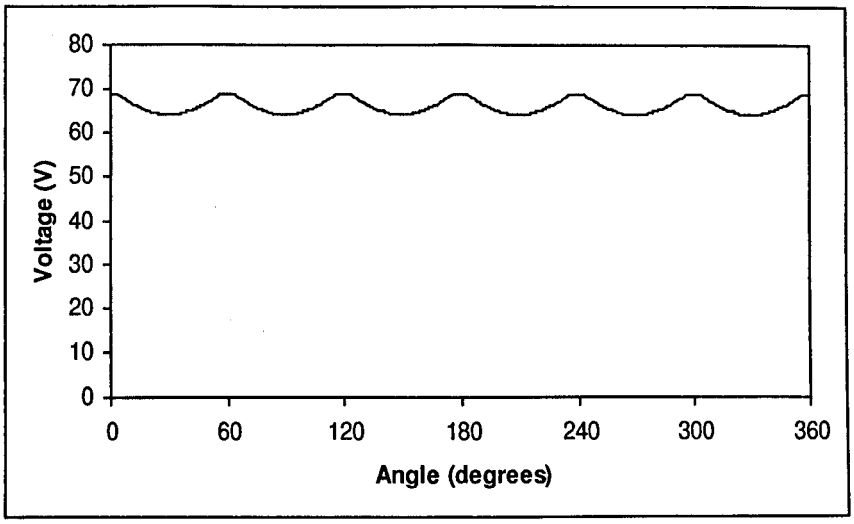

Figure 3.27 – Per Switching Cycle Averaged DC Bridge Output Voltage

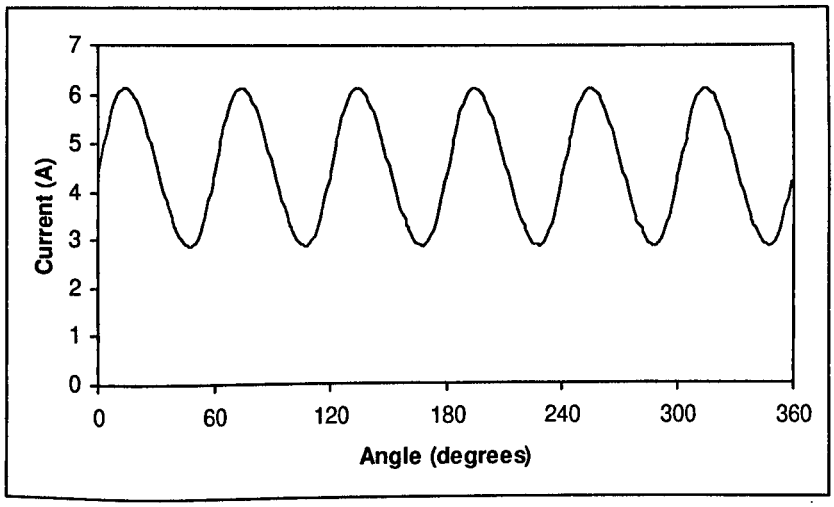

Figure 3.28 – DC Current

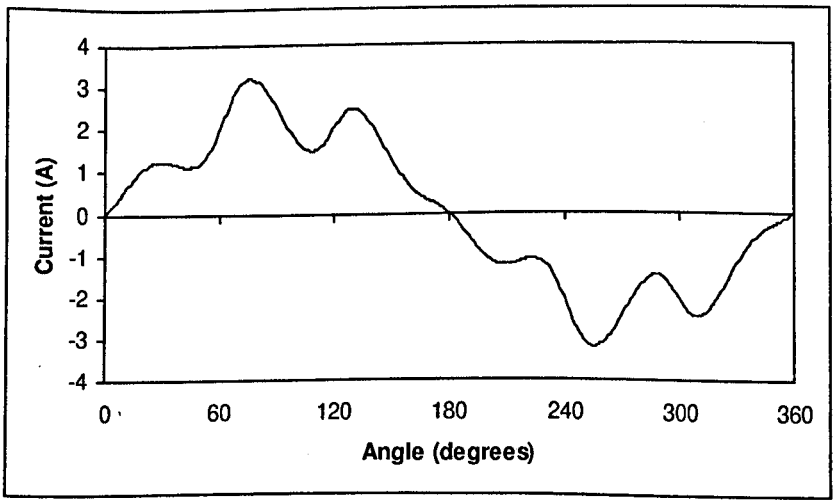

Figure 3.29 – AC Input Current

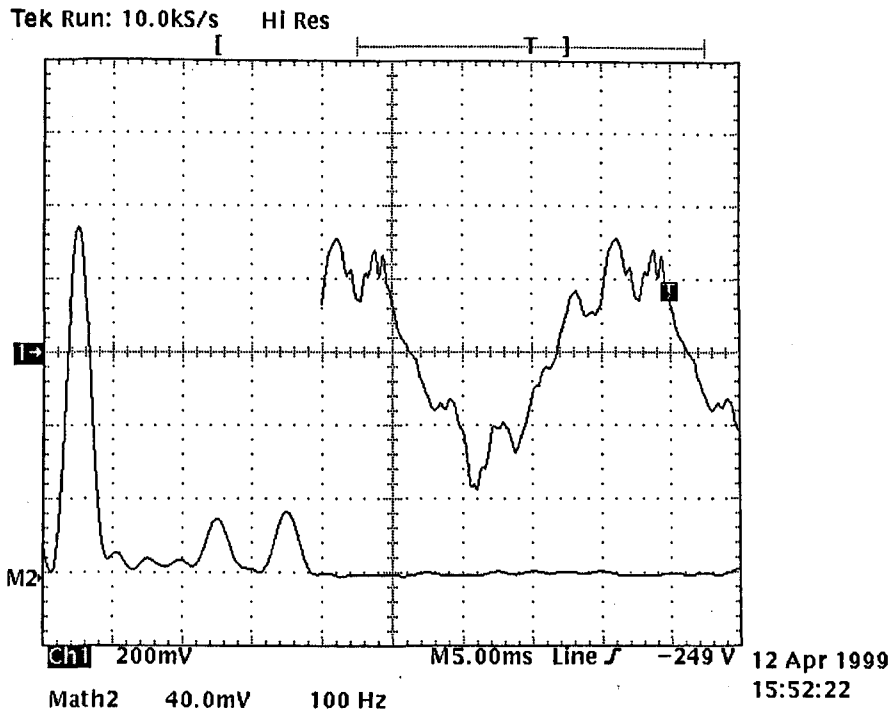

Figure 3.30 – Open-Loop Input Current (2A/div) and FFT Plot (0.4Arms.div)

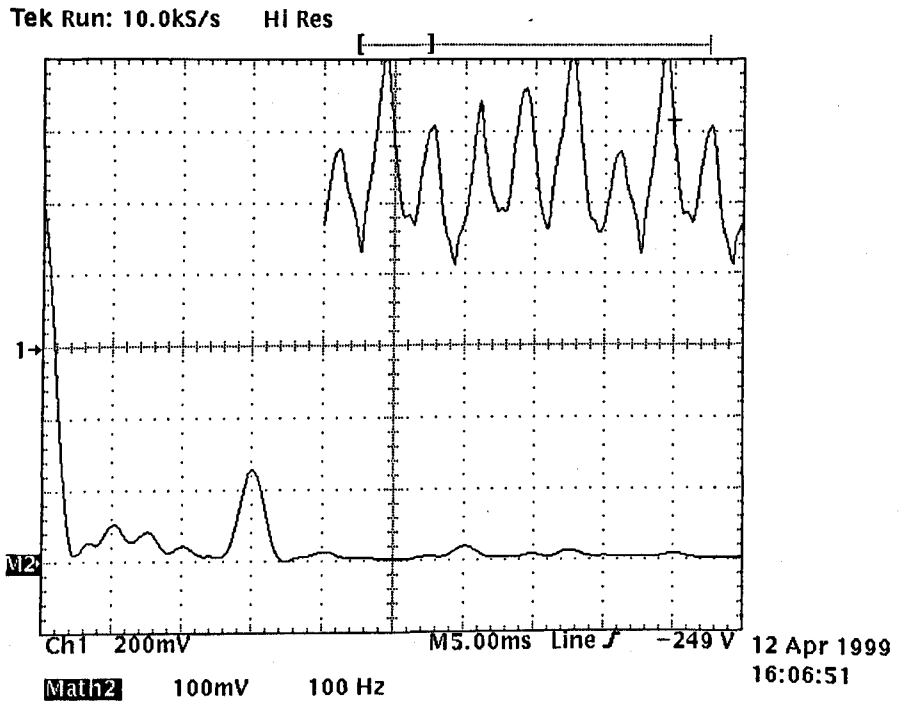

Figure 3.31 – Open-Loop Output Current (2A/div) and FFT Plot (1Arms/div)

From the results given from Equation (3.49) it is seen that the most significant ac voltage harmonic is the 3rd and yet this balanced harmonic results in no current flow as it is a triplen. Instead, the 5th and 7th both control production of the 6th voltage and current harmonics on the dc side and then this 6th harmonic is reflected back to the ac side as 5th and 7th current harmonics. The same argument applies for the 11th and 13th

ac-side voltage/current side harmonics that produce the 12th current harmonic on the dc side.

Production of Sidebands

It is intuitive that the n^{th} dc side harmonic will produce two ac side sidebands. The current in phase 'a' is given by

$$I_a(t) = I_{dc}(t)\sin(\omega_m t) \tag{3.50}$$

where $I_{dc}(t)=I_{dc}+I_n\cos(n\omega_m t)$ (n.b. it is cosine rather than sine as the dc side harmonics are "even"). Substitution of this into Equation (3.50) will give two ac-side sidebands; at $(n-1)\omega_m$ and $(n+1)\omega_m$ as well as the fundamental at ω_m and this is an example of an AM process in the converter. What is not so intuitive is why one ac side sideband gives only one dc side sideband. The reason for this is that the dc-side voltage is composed of two modulation processes due to the switching of two phases with a third phase. If the voltage phases contain the n^{th} harmonic of the fundamental, then four sidebands are produced, two at $(n-1)\omega_m$ and two at $(n+1)\omega_m$. If the n^{th} harmonic was added in a positive sequence manner then mathematically the $(n+1)\omega_m$ harmonics cancel and only the $(n-1)\omega_m$ harmonic is left and vice versa if the n^{th} harmonic was added in a negative sequence manner resulting in one dc side harmonic. The 5^{th} and 7^{th} harmonics involved in the ac side due to the flat-topped phase voltages are of negative and positive sequence respectively, so they both affect the dc side 6^{th} harmonic production.

Harmonic Transfer Applied to Switching Frequencies

The harmonic transfer rules also apply to switching frequency harmonics. For example, comparing Figures 3.2 and 3.7 (which show the harmonics around ω_s for the ac and dc sides respectively) then it is seen that $\omega_s \pm 3\omega_m$ on the dc side gives sidebands

either side at $\omega_s \pm 4\omega_m$ and $\omega_s \pm 2\omega_m$ on the ac side. This is true for harmonics centred around any multiple of ω_s for both ac-dc and dc-ac transfer.

3.7 Distortion Due to the AC Filter and a Finite DC Inductor

AC Filter

The effect of the input filter on the overall input current is important as the filter draws reactive power from the supply. At 50Hz the input inductors' impedances are vanishingly small. Thus of crucial importance are the sizes of the ac input capacitors. The current in the n^{th} phase due to these capacitors can be shown to be

$$I_{Cac} = 3VC_{ac}\omega_m \cos(\omega_m t + \frac{n\pi}{3}) \qquad \text{n=0,1,2} \qquad (3.51)$$

If the phase input current due to the converter is given by $I_a = I_{dc}M\sin(\omega_m t + n\pi/3)$, then the resultant input current is given by the vector sum $\overrightarrow{I_{ac}} = \overrightarrow{I_a} + \overrightarrow{I_{Cac}}$

$$I_{ac} = I_p \cos(\omega_m t - \alpha + \frac{n\pi}{3}) \qquad \text{n=0,1,2} \qquad (3.52)$$

where $I_p = \sqrt{(3VC_{ac}\omega_m)^2 + (I_{dc}M)^2}$

and $\alpha = \tan^{-1}\left(\frac{I_{dc}M}{3VC_{ac}\omega_m}\right)$

The combination of these two effects results in the ac input current exhibiting a slight phase lead of $\pi/2-\alpha$ radians (if the input capacitors are chosen so that the reactive current is much smaller than the active current drawn by the converter). Because the switching frequency of the converter is high, the input capacitors and hence reactive power is small. For example, if the dc current I_{dc}=30A @ M=1 where V=240V and C_{ac}=3μF then the phase lead of the input current is approximately 1.3° and the peak value of the reactive current is approximately 0.68A compared to a peak active current of 30A. If a larger value of C_{ac} is to be used so giving significant phase shift, then it

would be possible to implement a more sophisticated control scheme that made use of the ability of the converter to draw leading or lagging current that cancelled the effect of the filter [3.11].

Finite DC Inductor

One of the basic assumptions made for the operation of the converter is that the dc inductor is of infinite size. In practice this is not true and it is desirable to make the inductor as small as possible to reduce cost and volume. The input current waveforms (Figure 2.9) show a characteristic phase shifted flat-top appearance even when the input voltages and PWM signals are pure sinusoids. The phase shift is due to the input filter. The flat-top appearance is due to the error caused by the imperfect current averaging effect of the finite dc inductor on the applied voltage. This was investigated in more detail using the MATLAB™ simulation package by writing two M-files (Appendix A8) that compute from first principles the dc and ac side current waveforms. The dc-side capacitor is considered to be infinite and can therefore be represented by a voltage source. The charging of the dc inductor is given by a linear approximation (valid for $\Delta t_{on} \leq T_s$), as the time constants of the passive components are much greater than the switching period

$$\Delta I_{dc(charge)} = \frac{1}{L_{dc}}(V_l - V_{out})\Delta t_{on} \tag{3.53}$$

where V_l is the line voltage, V_{out} the output voltage and Δt_{on} the on-time of the switch at any instant. Likewise, the discharge of the inductor current (freewheeling state) is linearly approximated by

$$\Delta I_{dc(discharge)} = \frac{-V_{out}}{L_{dc}}\Delta t_{off} \tag{3.54}$$

where Δt_{off} is the off-time of the switch. If the modulating frequency is scaled down to 1Hz from 50Hz, then the switching frequency is scaled from 76.8kHz to 1536Hz, the dc

inductor scaled from 160μH to 8mH and input ac capacitors scaled from 3μF to 150μF. The dc inductor current is plotted in Figure 3.30. The second of the two M-files is used to take the average of the current over each switching cycle and assign it to phase 'a' of the phase voltages giving Figure 3.31, where C_{ac}=3μF. Also plotted is the input current, assuming a 10mH (i.e. large) dc inductance. It is seen that there is an error due to the finite dc inductor, especially around the 60° and 120° points, that increases as the dc inductor size decreases. This error contributes 5th and 7th harmonics to the ac side. The PSpice™ simulation includes series resistance with each diode to aid convergence and this too contributes to the flat top appearance of the supply currents.

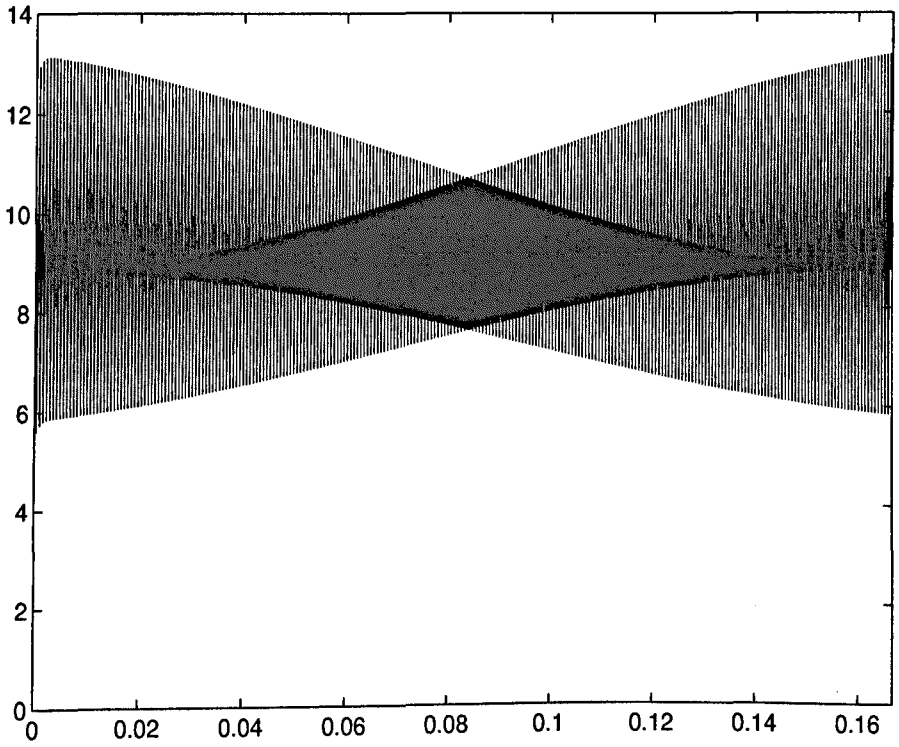

Figure 3.30 - DC Inductor Current

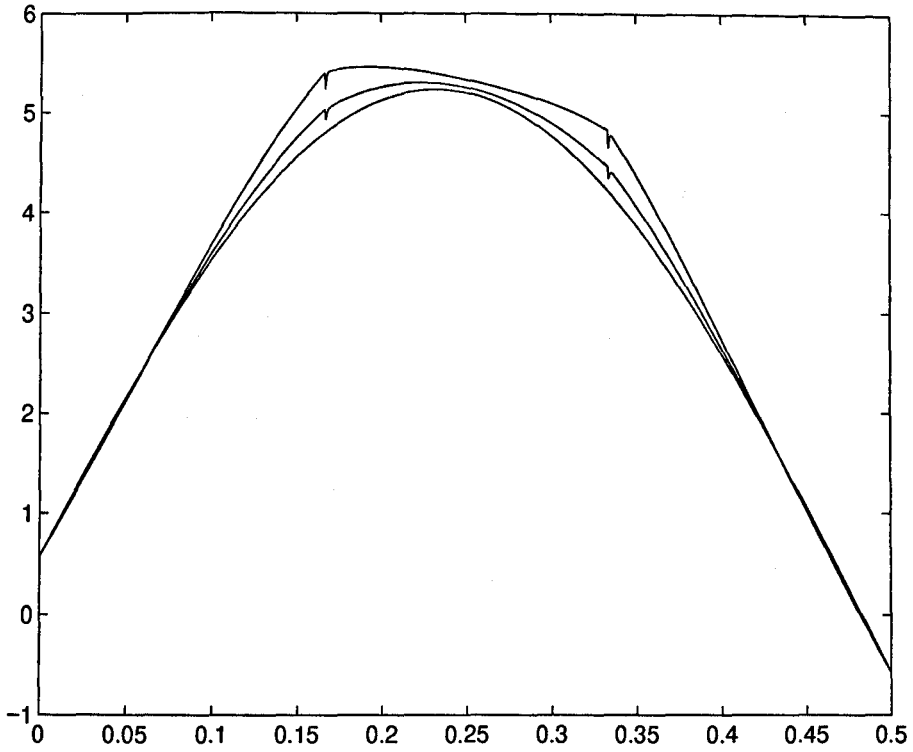

Figure 3.31 – Input Current Half-Cycle

Upper Trace : L_{dc}=100μH, Middle Trace : L_{dc}=160μH,

Lower Trace : L_{dc}=10mH

Further DC Inductor Considerations

The presence of low frequency harmonics due to supply voltage flat-topping creates currents that flow through the system. The corner frequency of the dc output filter should be chosen so that it is not close to the 6^{th} harmonic (300Hz) otherwise resonant amplification will occur.

3.8 Conclusions

This chapter has examined the low and switching frequency harmonic production of the converter. Closed-form expressions for the input current, output voltage and output current have been developed for the dead-band PWM scheme for one converter using the FTJ theory (which is of help when trying to analyse PWM systems). A closed-form expression for the input current of dual, interleaved converters

was found. A MathCAD™ derived analysis of the soft-switching PWM scheme's input current was made. All results were compared to PSpice™ simulations and found to be in agreement. Given the assumptions of sinewave voltage phases, synchronous PWM and infinite dc inductor size, then the dead-band scheme for one converter and the dead-band dual interleaved converter scheme produce no low frequency harmonics. The soft-switching scheme does, under the same assumptions. Under the same operating conditions as the single converter, the dual interleaved scheme will eliminate the harmonics around ω_s. The input ac current switching harmonics exhibit an FM process, the dc-side harmonics exhibit both FM and DSBM and the low frequency harmonic dc/ac transfer process exhibits AM.

The effect of supply voltage flat top was examined and found to greatly influence the low frequency harmonic production of the converter. The finite size of the dc inductor also, but to a lesser degree, generates low frequency harmonics. The dominant low frequency harmonics being the 5^{th} and 7^{th} on the ac side and corresponding 6^{th} harmonic on the dc side. Harmonic transfer in the converter was examined and it was confirmed that both switching and low frequency harmonics can be predicted on the ac/dc side if the harmonic and sequence of the dc/ac side harmonics are known.

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CHAPTER 4 – Converter Modelling and Control

4.1 Introduction

DC-DC Converter Average Behaviour

The control of dc-dc switched-mode power supplies (SMPS) has long been a subject for research. In order to understand converter behaviour, models have been developed. Modelling is complicated by the fact that SMPS exhibit non-linear, discontinuous and time varying properties, which makes them difficult to analyse. Three-phase ac-dc SMPS converters have the additional complication of having three time varying inputs, unlike dc-dc converters which only have one time-invariant input. DC-DC SMPS are a close relative of three-phase ac-dc SMPS and many of the techniques and methods used to analyse the former are transferable to the latter. One of the original, classic papers on dc-dc SMPS modelling introduced the method of state-space averaging as applied to continuous current conduction [4.1]. This method works by developing the state-space equations for the converter when the switch is on and when it is off (freewheeling state) and then taking the average of these two states so that the result describes the average behaviour during both states. Subsequently there have been many refinements to this theory and additional techniques such as; discontinuous current mode converters [4.2], closed loop peak [4.3] or average current control [4.4] and behaviour with an input filter [4.5]. An important improvement on the state-space averaging method [4.6] concentrated on replacing only the freewheel diode and switch of a converter with an equivalent circuit theory model rather than averaging the whole converter. This means that once the switch and diode circuit-theory model is obtained, it is readily transferable to any converter topology.

Three-Phase AC-DC Converter Modelling

Three-phase ac-dc converters can be modelled by using a dq transformation where the rotating co-ordinate frame is synchronised to the input phase-voltage frequency, so rendering all state variables constant under steady-state operating conditions [4.7]. Another method in use is to again use dq modelling but to represent the switches as equivalent transformers and gyrators [4.8]. A key paper [4.9] looked at unifying the analysis of three-phase ac-dc and dc-dc converters by using the PWM switch model [4.6] and reducing the average behaviour of the three-phase boost converter to a dc-dc boost converter. The main assumptions of this paper are that the d-channel alone determines system stability (the q channel has better stability than the d-channel) and that the cross coupling between the channels is negligible. The three-phase converter is approximated by a dc-dc converter whose input voltage is the rms value of the time-varying line voltage. This method was tested against the previously mentioned dq method and found to be a good approximation. This approximation is important as it means that the well developed dc-dc converter modelling techniques can applied to their three-phase cousins. This method was applied to the three-phase buck converter in Section 4.4.

Switched Models

Little work has been done on developing switched models of SMPS. One paper [4.10] generated a SIMULINK™ switched model of a dc-dc resonant mode converter. The general idea is to achieve a PSpice™ type model only by using SIMULINK™, which has the advantages of access to powerful control algorithms and produces faster simulation run-times. A SIMULINK™ switching model for the three-phase buck converter is produced in Section 4.2

Input Filter and Control

The addition of an input filter to a dc-dc SMPS is recognised as considerably increasing the complexity of the analysis of the SMPS and also produces some significant and undesirable instability effects when closed loop current-mode control is used [4.11]. The input filter raises the input impedance of the supply and can result in interaction between converter and filter if the input impedance of the converter approaches the output impedance of the filter at any frequency. Step changes in demand or load can excite the filter and cause ringing. This problem also exists for ac-dc three-phase converters. For three-phase ac-dc converters, ways of damping the input filter include active schemes where the oscillations are sensed and damped using a controller [4.12] and active and passive damping on a multi-stage input filter [4.13]. This active damping method uses a separate high-power op-amp to sense the oscillations across one input filter inductor and applies a damping current to the second. None of these papers tackles the fact that the supply itself has inductance associated with the long wiring cables and utility step-down transformer leakage, although this problem is mentioned in another paper [4.9] as being a particular problem. If the input filter inductances of the converter are small, then the dominant inductance can be that of the utility supply itself. This variable and unknown inductance will then have a significant influence on the input filter resonant circuit and is discussed in Section 4.8.

Three-Phase AC-DC Control Methodologies

Many different techniques have been employed to control the three-phase ac-dc converter. These range from; analogue or digital proportional plus integral (PI) current and voltage controllers, state variable controllers, neural networks, one-cycle control and sliding-mode control. All try to achieve the same thing i.e. unity power factor, constant and yet adjustable dc output voltage, rejection of step changes in line and load

and a fast and well-damped response to changes in demand. The controller used in this thesis' converter is a simple analogue PI controller that senses the average dc output current combined with a digital look-up table to generate the sinusoidal current templates and is examined in Section 4.4.

4.2 A Switching Model of the Three-Phase Step-Down Converter

Introduction

The idea behind developing this model is so that the behaviour of the converter can be accurately reproduced using the computer. This means that different control strategies and operating conditions can be quickly examined. The model will then be a reference by which other, simpler models can be compared.

Converter Model

The model can be split up into seven distinct stages; output filter and load, input filters, triangle generator, PWM generator, controlled bridge, input current assignation and average current-mode controller. These stages, for the case of this converter, can be conveniently decoupled from each other as illustrated in Figure 4.1. The actual currents and voltages across the bridge's diodes and switches are not needed from a system point of view and so the bridge is viewed as a "black-box" that takes three ac input voltages and converts them to a dc output via a controlled PWM process. (In fact, it is possible to extract the voltage and currents across and through the bridge devices using this model, see Section 4.2.9).

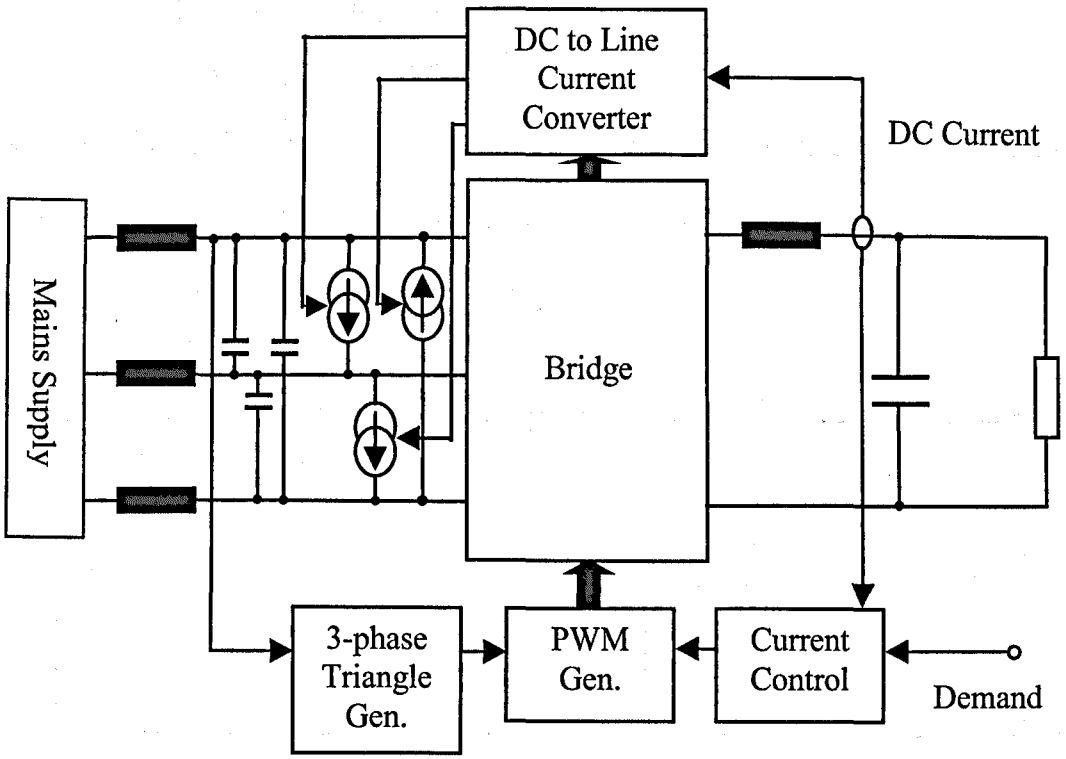

Figure 4.1 – Three Phase ac-dc Step Down Converter Model

It is necessary to couple the output dc current to the input filters so that the input filters "see" the current flowing in them due to the converter, because from a SIMULINK™ point of view, the bridge only transmits voltages. This is accomplished by assigning the switched dc current to each phase at the correct instances. The input filters are therefore modelled as three LC filters with phase-to-phase connected controlled current sources/sinks from which the converter currents are extracted from/fed back into.

4.2.1 Output Filter and Load

This is modelled using the state-space representation according to Equations (4.1a) and (4.1b). Series resistances are included with the inductor, r_{ldc}, and capacitor, r_{cdc}. The load can be resistive or constant current.

$$\begin{bmatrix} \dot{u}_l \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-(r_{ldc}+r_{cdc})}{L_{dc}} & \frac{-1}{L_{dc}} \\ \frac{1}{C_{dc}} & 0 \end{bmatrix} \begin{bmatrix} u_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{dc}} & \frac{r_{cdc}}{L_{dc}} \\ 0 & \frac{-1}{C_{dc}} \end{bmatrix} \begin{bmatrix} V_{in} \\ u_o \end{bmatrix} \tag{4.1a}$$

and

$$\begin{bmatrix} v_{out} \\ u_l \end{bmatrix} = \begin{bmatrix} r_{cdc} & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} u_l \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & -r_{cdc} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ u_o \end{bmatrix} \quad (4.1b)$$

where v_c is the dc capacitor voltage, u_l the inductor current, L_{dc} the dc inductance, C_{dc} the dc capacitance, V_{in} the voltage input to the filter, V_{out} the output voltage and u_o the current drawn by the load. Figure 4.2 illustrates the filter model.

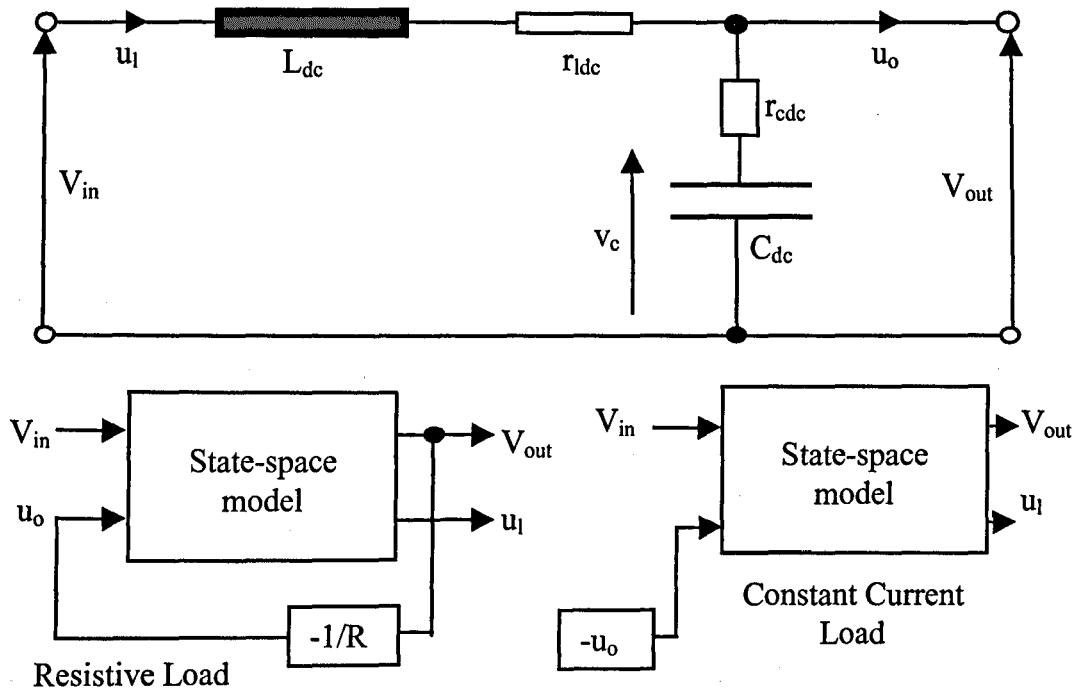

Figure 4.2 – Output Filter and State Space Model

The SIMULINK™ block is shown in Figure 4.3, where each element is modelled separately to allow for the inclusion of a saturation element that prevents negative current from flowing during transient oscillations.

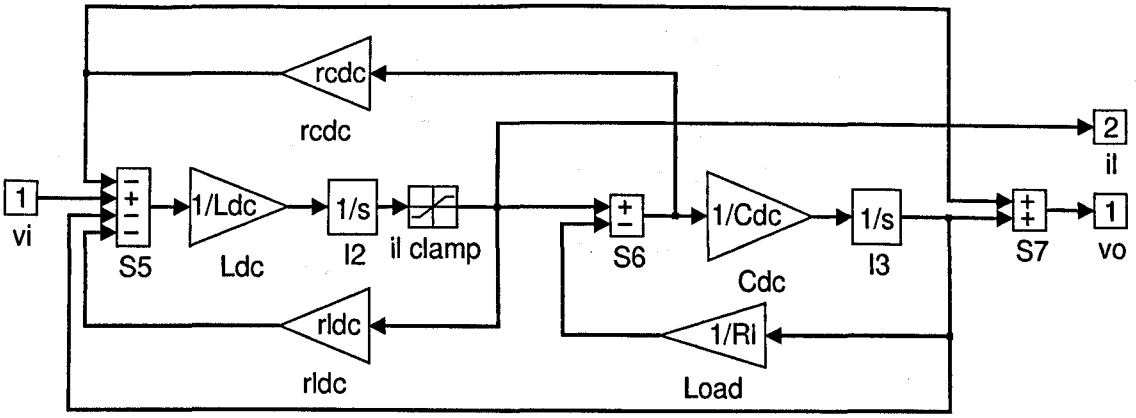

Figure 4.3 – SIMULINK™ Output Filter and Load

4.2.2 Input Filters

The three-phase input filter is modelled using the state-space representation. For a three-phase, three-wire system, the input currents sum to zero so reducing the number of state variables by one to five. The state variables are two input currents, u_1 and u_2 and the three capacitor voltages, v_4, v_5 and v_6. The input voltages sum to zero, which reduces the number of inputs to the system by one to five. The inputs to the system are two line input voltages, v_{12} and v_{23} and the three controlled current sources/sinks, u_{o4}, u_{o5} and u_{o6}. The output voltages are v_7, v_8 and v_9. The state-space equations are given by Equations (4.2a) and (4.2b) and the input filter model is shown in Figure 4.4.

$$\begin{bmatrix} \dot{u}_1 \\ \dot{u}_2 \\ \dot{v}_4 \\ \dot{v}_5 \\ \dot{v}_6 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} \frac{-(3r_l+r_c)}{L_{ac}} & 0 & \frac{-1}{L_{ac}} & 0 & \frac{1}{L_{ac}} \\ 0 & \frac{-(3r_l+r_c)}{L_{ac}} & \frac{1}{L_{ac}} & \frac{-1}{L_{ac}} & 0 \\ \frac{1}{C_{ac}} & \frac{-1}{C_{ac}} & \frac{-1}{r_cC_{ac}} & \frac{-1}{r_cC_{ac}} & \frac{-1}{r_cC_{ac}} \\ \frac{1}{C_{ac}} & \frac{2}{C_{ac}} & \frac{-1}{r_cC_{ac}} & \frac{-1}{r_cC_{ac}} & \frac{-1}{r_cC_{ac}} \\ \frac{-2}{C_{ac}} & \frac{-1}{C_{ac}} & \frac{-1}{r_cC_{ac}} & \frac{-1}{r_cC_{ac}} & \frac{-1}{r_cC_{ac}} \end{bmatrix}\begin{bmatrix} u_1 \\ u_2 \\ v_4 \\ v_5 \\ v_6 \end{bmatrix} +$$

$$\frac{1}{3}\begin{bmatrix} \frac{r_c}{L_{ac}} & 0 & \frac{-r_c}{L_{ac}} & \frac{2}{L_{ac}} & \frac{1}{L_{ac}} \\ \frac{-r_c}{L_{ac}} & \frac{r_c}{L_{ac}} & 0 & \frac{-1}{L_{ac}} & \frac{1}{L_{ac}} \\ \frac{-2}{C_{ac}} & \frac{1}{C_{ac}} & \frac{1}{C_{ac}} & 0 & 0 \\ \frac{1}{C_{ac}} & \frac{-2}{C_{ac}} & \frac{1}{C_{ac}} & 0 & 0 \\ \frac{1}{C_{ac}} & \frac{1}{C_{ac}} & \frac{-2}{C_{ac}} & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{o4} \\ u_{o5} \\ u_{o6} \\ v_{12} \\ v_{23} \end{bmatrix} \tag{4.2a}$$

and

$$\begin{bmatrix} v_7 \\ v_8 \\ v_9 \\ u_1 \\ u_2 \\ u_3 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} r_c & -r_c & 2 & -1 & -1 \\ r_c & 2r_c & -1 & 2 & -1 \\ -2r_c & -r_c & -1 & -1 & 2 \\ 3 & 0 & 0 & 0 & 0 \\ 0 & 3 & 0 & 0 & 0 \\ -3 & -3 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ v_4 \\ v_5 \\ v_6 \end{bmatrix} + \frac{1}{3}\begin{bmatrix} -2r_c & r_c & r_c & 0 & 0 \\ r_c & -2r_c & r_c & 0 & 0 \\ r_c & r_c & -2r_c & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{o4} \\ u_{o5} \\ u_{o6} \\ v_{12} \\ v_{23} \end{bmatrix} \tag{4.2b}$$

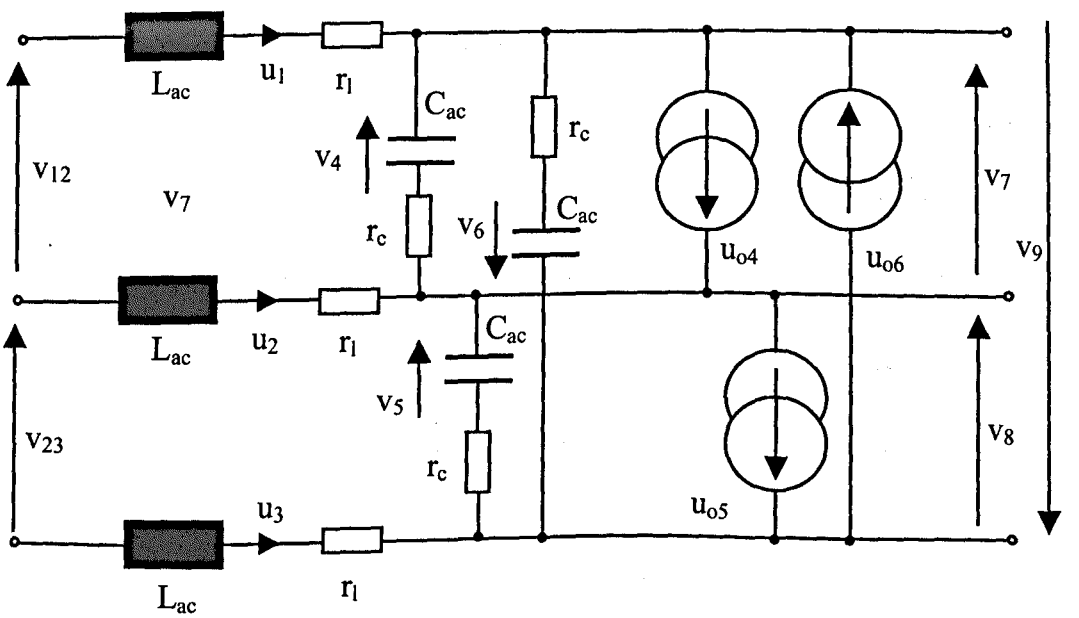

Figure 4.4 – Three-Phase Input Filter

The SIMULINK™ input filter is shown in Figure 4.5. The line voltages are derived from the 50Hz phase input via the "PNV to LV2" block that converts phase voltages to line voltages and is shown in Figure 4.6.

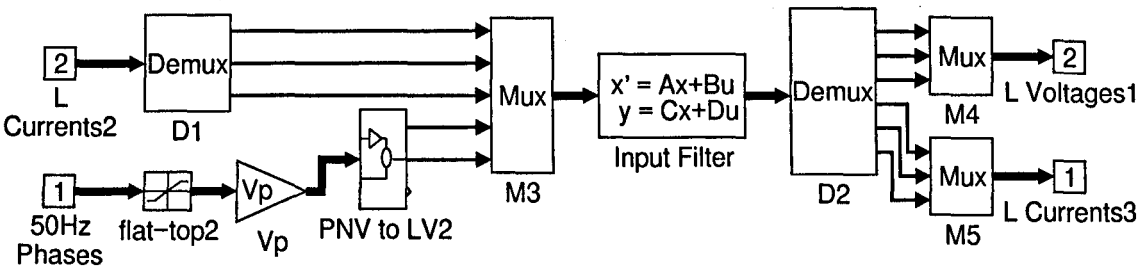

Figure 4.5 – Input Filter

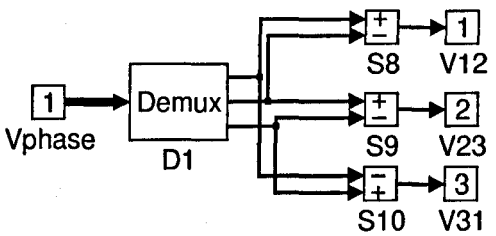

Figure 4.6 – SIMULINK™ Phase to Line Voltage Converter

4.2.3 Three-Phase Triangle Generator

Two, co-phasal triangle waveforms are compared with a demand signal to produce the PWM signal. Which phase is using which triangle (or no triangle if the phase is held on) is determined by this SIMULINK™ block seen in Figure 4.7 with a 50kHz (T_s=20μs) triangle carrier frequency. The 'delay' block delays the carrier by $T_s/2$ so as to generate the second carrier. The carriers are synchronised to the 50Hz mains.

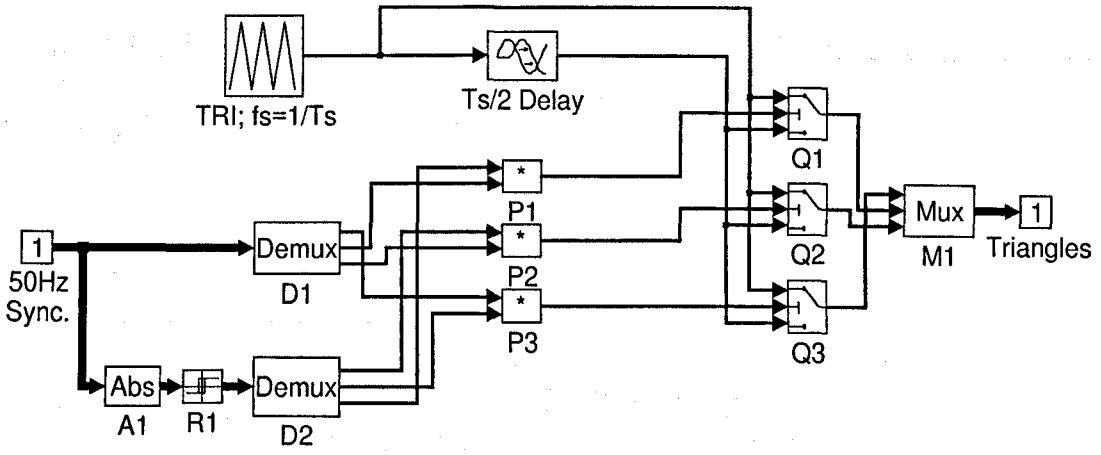

Figure 4.7 – SIMULINK™ Three-Phase Triangle Generator

Figure 4.8 shows the output from the generator block at a point when the triangle's phase for signal 'c' is reversed.

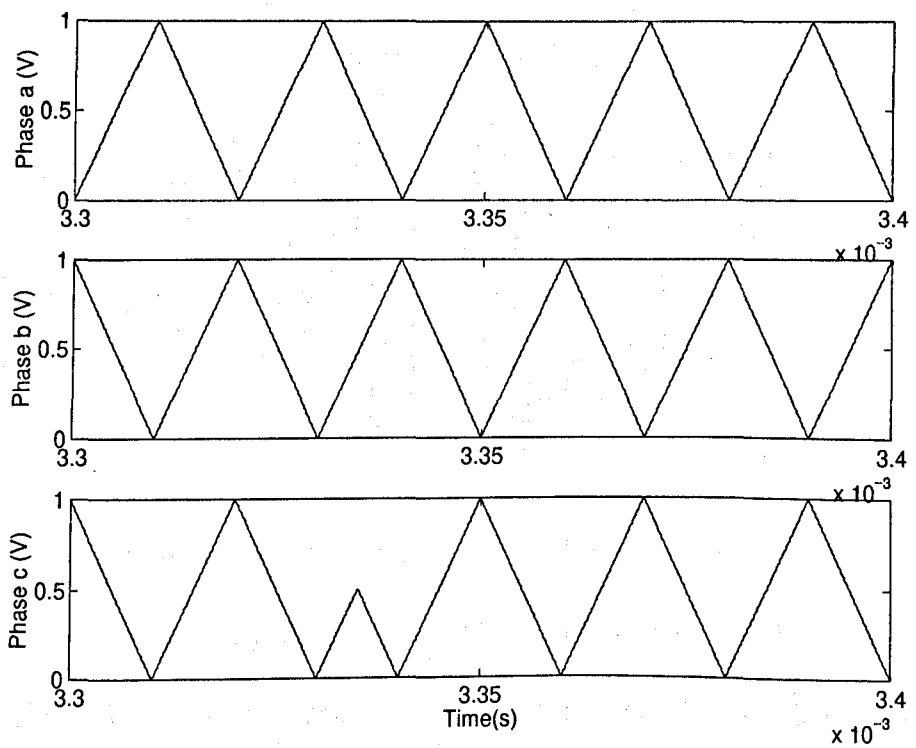

Figure 4.8 – Three-Phase Triangle Waveforms at a Change-Over Point

4.2.4 Three-Phase PWM Generator

The function of this block is to take the three-phase triangle carriers, compare them with a reference value, $0 \leq M \leq 1$, and produce the on/off PWM pattern for the three

switches of the converter. The block is seen in Figure 4.9. The function of the "LLPWM" block (Figure 4.10) is to convert the PWM signals into a form that can be accepted by the SIMULINK™ "switch" block.

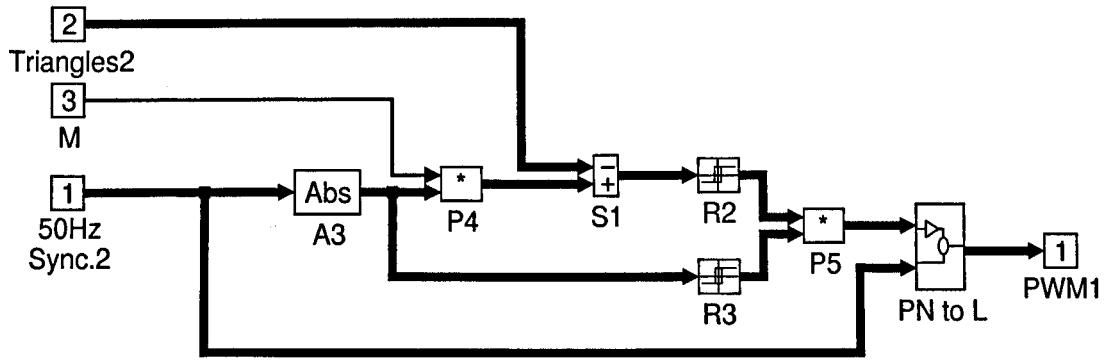

Figure 4.9 - SIMULINK™ Three-Phase PWM Generator Block

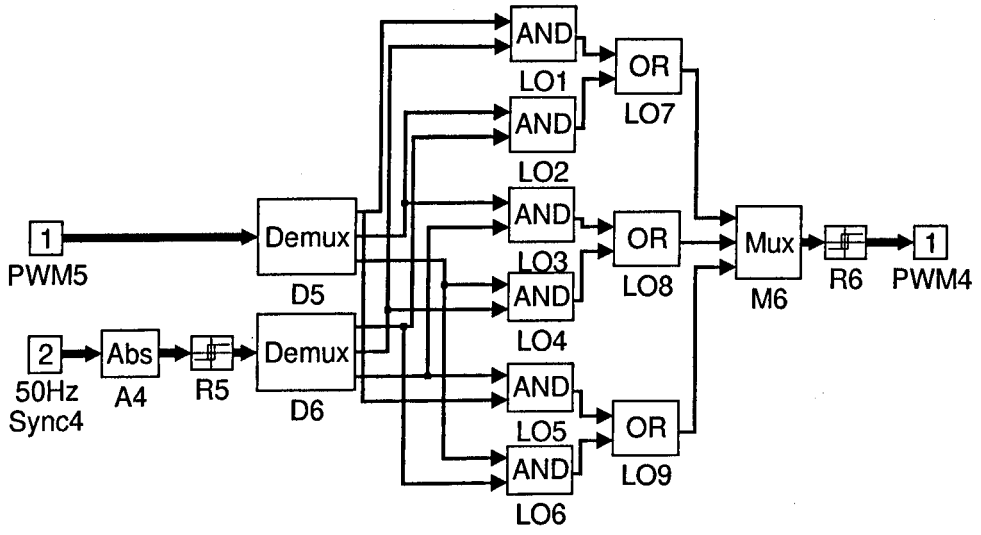

Figure 4.10 – SIMULINK™ Phase to Line PWM Converter

Figure 4.11 shows the PWM pulses at the 60° change-over point where phase 'c' goes from being held on to switching and phase 'a' goes from switching to being held on.

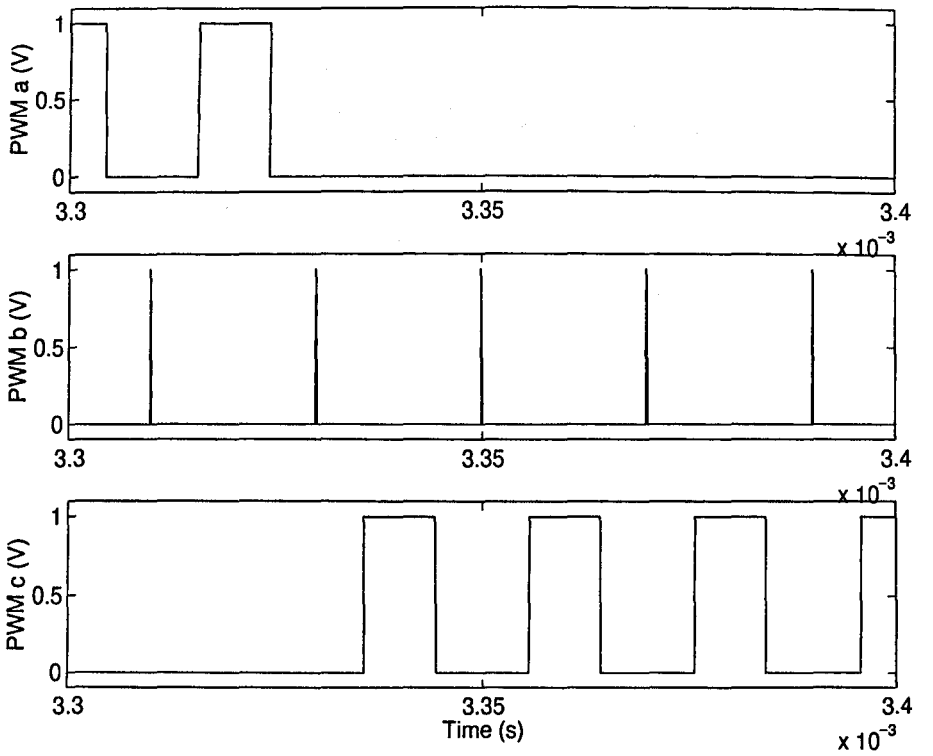

Figure 4.11 – Three-Phase PWM Pulses at a Change-Over Point; M=0.5

4.2.5 Controlled Bridge

The bridge takes the three-phase voltages fed to it from the input filter (Vin) and switches them according to the output of the PWM generator (PWM3) to produce a dc output. Figure 4.12 shows the SIMULINK™ file and Figure 4.13 gives typical bridge output voltage and dc filter current. Note that the bridge itself is represented by only three blocks; Q5, A2 and S2.

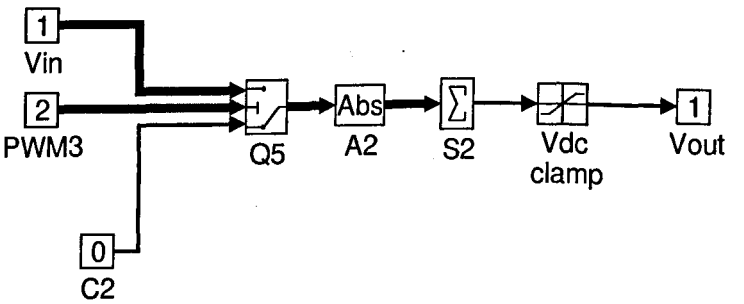

Figure 4.12 – SIMULINK™ Converter Bridge

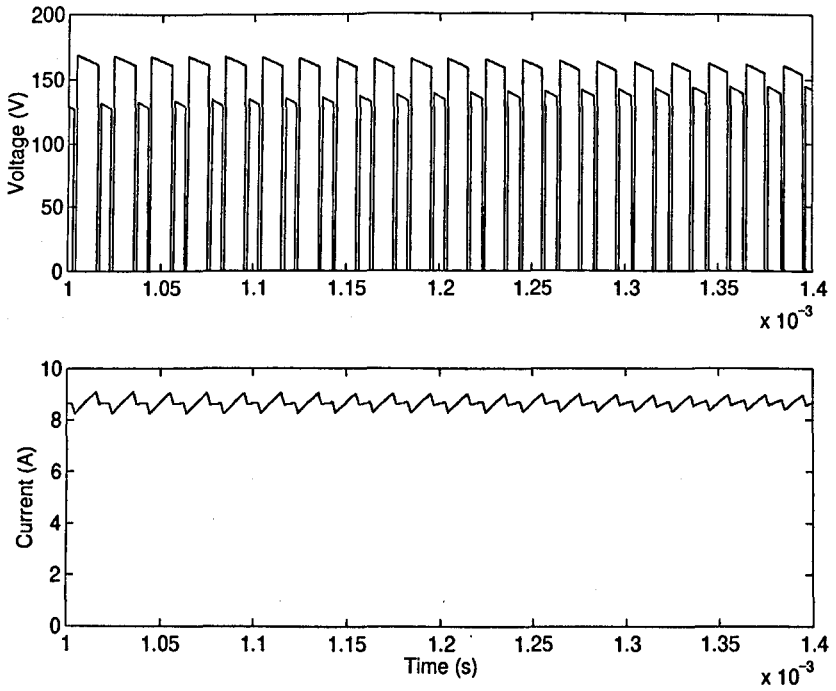

Figure 4.13 – Upper Trace : DC Bridge Voltage Output, Vout

Lower Trace : DC Inductor Current, u_l

4.2.6 Input Current Assignation

The job of this block is to chop the dc inductor current (Idc1) and assign it to the correct phases. This is the pulsed current that is actually drawn from the input filter by the converter. The SIMULINK™ file is shown in Figure 4.14 and typical currents in Figure 4.15.

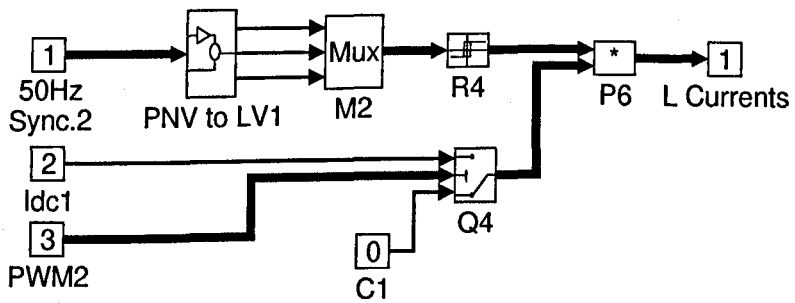

Figure 4.14 – SIMULINK™ Input Current Assignor

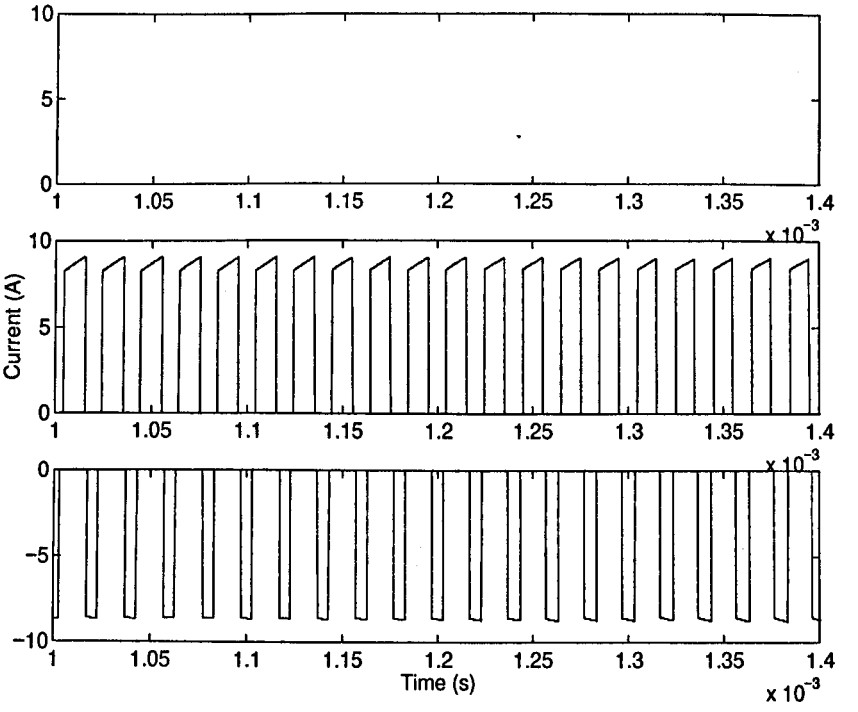

Figure 4.15 – Typical Pulsed Currents Drawn From the Input Filter

Upper Trace : u_{o4}, Middle Trace : u_{o5} and Lower Trace : u_{o6}

4.2.7 Current Controller

The current controller compares the demand with the actual dc inductor current and generates an error signal accordingly so as to achieve constant inductor current. The controller is shown in Figure 4.16 and is of the proportional plus integral (PI) type.

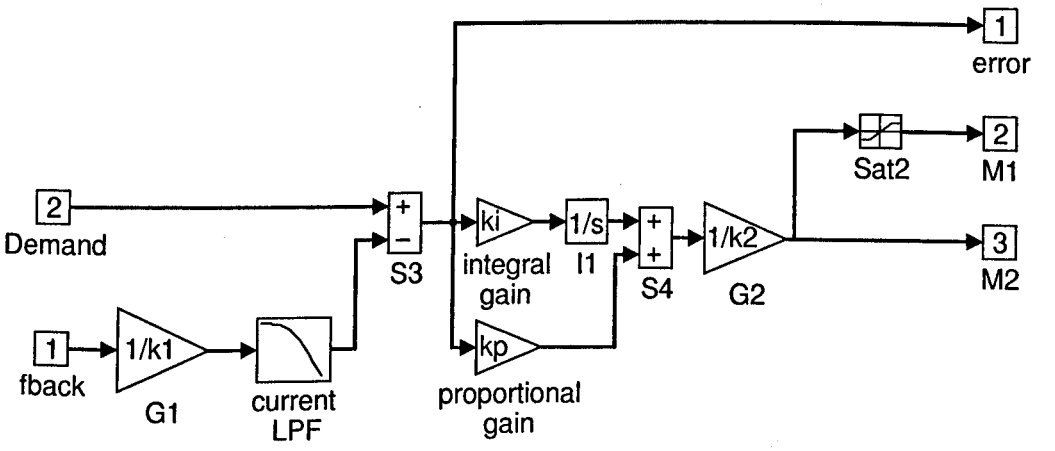

Figure 4.16 – DC-Side Current Controller

4.2.8 System Connectivity

An overall system view as to how the various blocks are assembled together is shown in Figure 4.17 and the input currents for the system shown in Figure 4.18. Appendix A9 lists the text m-file that sets all the parameters for the system SIMULINK™ m-file.

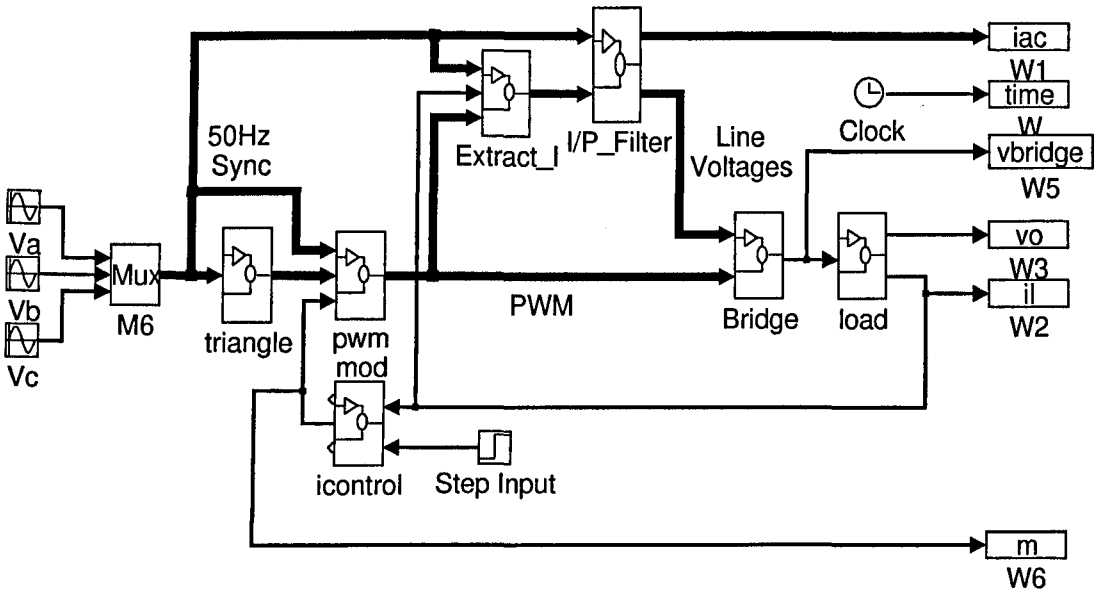

Figure 4.17 – SIMULINK™ Three-Phase AC-DC Current Controlled Converter

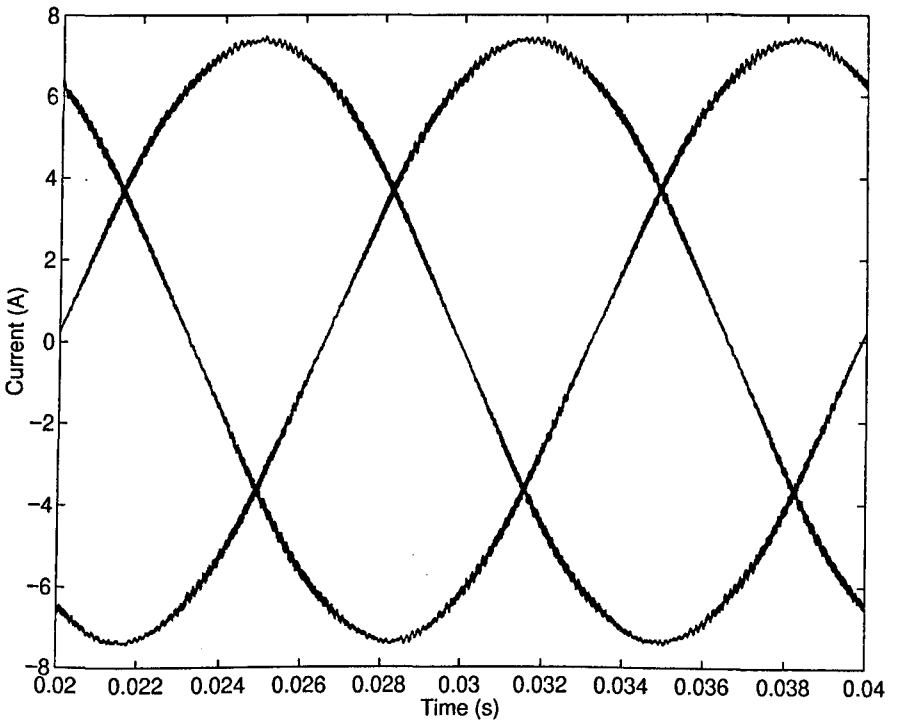

Figure 4.18 – Three-Phase Input AC Currents; u_1, u_2 and u_3

4.2.9 Deriving the Bridge Currents From the Model

Although the bridge is not directly modelled in the same way as PSpice™, it is still possible to reconstitute the switching device currents (or voltages) from the dc inductor current and PWM scheme. The SIMULINK™ block that does this is shown in Figure 4.19 and average current waveforms in Figure 4.20. The average waveforms were derived from the switching waveforms by applying second-order Butterworth low-pass filters with cut-off frequencies of 3kHz.

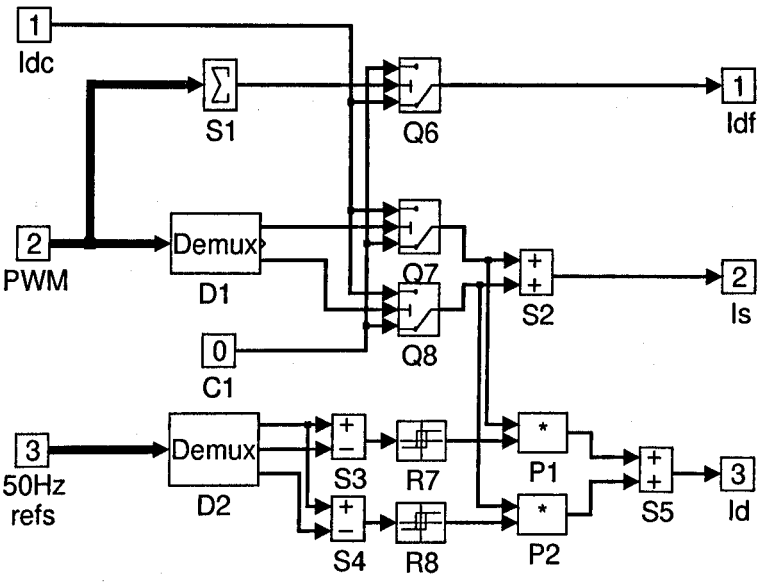

Figure 4.19 – SIMULINK™ Average Current Calculator Block

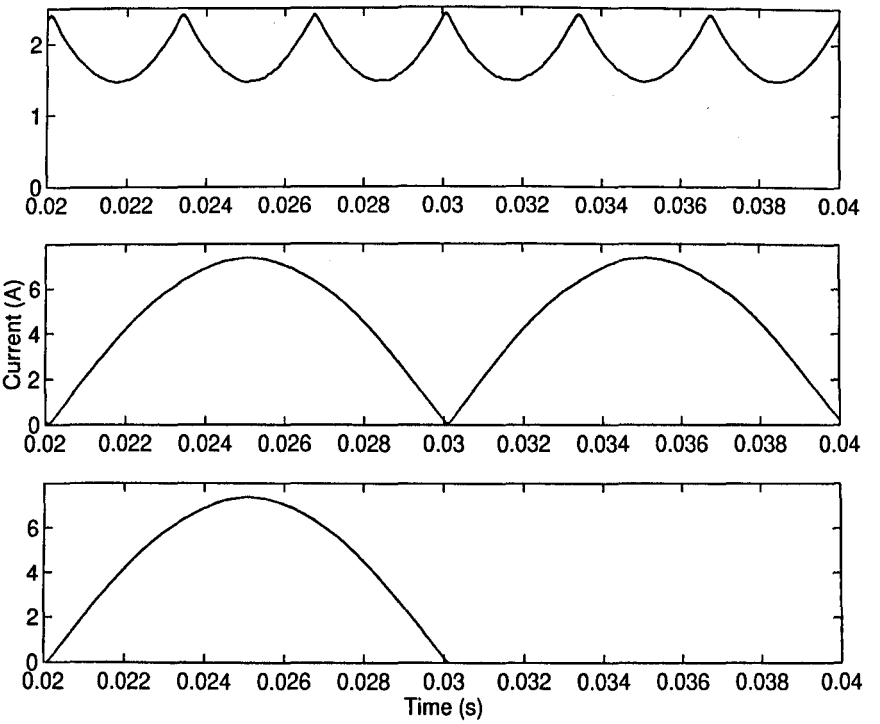

Figure 4.20 – Average Current Waveforms of Devices

Upper Trace : Average Free-Wheel Diode Current, I_{df}

Middle Trace : Average Switch Current, I_s

Lower Trace : Average Diode Current, I_d

4.2.10 Modulator Phase-Lag

The action of regular-sampled PWM is to sample the modulating input at certain fixed points and produce a PWM output. The fact that the input signal (of frequency f_{mod}) is sampled at fixed points and not at the natural intersections introduces a phase delay between the input and PWM output. For this converter, the input is sampled once every two switching cycles, as illustrated in Figure 4.21. The first PWM pulse is delayed by ϕ_{lag1} radians and the second PWM pulse is delayed by ϕ_{lag2} radians.

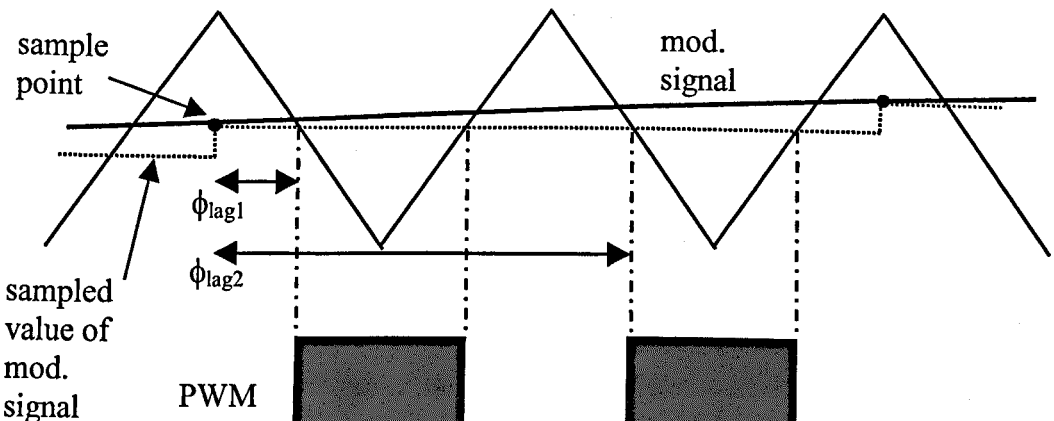

Figure 4.21 – Phase Lag Due to Regular-Sampled PWM

To achieve less phase delay and hence a higher current-loop bandwidth, the ADC sample rate could be increased to f_s or $2f_s$ [4.12]. The effect of the phase delay in the controller will have the effect of decreasing the phase margin of the overall system. The phase delay effect is not considered further, as the dominant effect as regards stability of the system is the input filter resonance frequency, which occurs at a much lower frequency (1kHz) than the sampling frequency of the ADC (38.4kHz). Filtering of the feedback signal and aliasing are considered in Section 4.7.

4.3 Use of the Switching Model

The switching model has a number of uses and these are now examined.

4.3.1 Obtaining Bode Plots from the Switching Model

Method

The frequency response of the converter is of interest to the designer in order to understand its operation and to see whether or not the control system employed promotes stability. It is difficult to obtain frequency response data from practical systems because of the large amount of switching noise swamping the signal of interest. In the case of the ac-dc converter, the extra difficulty of harmonics already existing in

the ac supply is encountered and can give false readings. This is not so much of a problem when using dc-dc or dc-ac converters, as the starting point is a dc source and this can readily be obtained with a negligible amount of harmonic distortion. If an accurate switching model is obtained then the measurements can be carried out on it, as the ideal condition of pure sinusoidal supplies is easily created. Moreover, it is possible to null the switching ripple by using the following method; **(i)** Run the simulation under the dc conditions required (modulation depth=M) to obtain the steady-state output of the variable of interest (e.g. the dc inductor current, I_{dc}). **(ii)** Sinusoidally perturb the input variable of interest (e.g. the depth of modulation, $M+\hat{m}$) at some frequency and re-run the simulation to obtain $I_{dc}+\hat{i}_{dc}$. **(iii)** Plot the difference between the two inductor current waveforms to be left with just $\hat{i}_{dc}$, which is the small-signal inductor current with no switching ripple contamination. **(iv)** The two small-signal waveforms, $\hat{i}_{dc}, \hat{m}$, can be plotted and the gain and phase read off. **(v)** Repeat steps (ii) to (iv) for different perturbation frequencies.

Results

Using the above method, Bode plots of both open and closed loop responses were obtained for the output impedance of the converter and the dc-current-to-demand response shown in Figures 4.22 to 4.29. All plots were taken with no input filter.

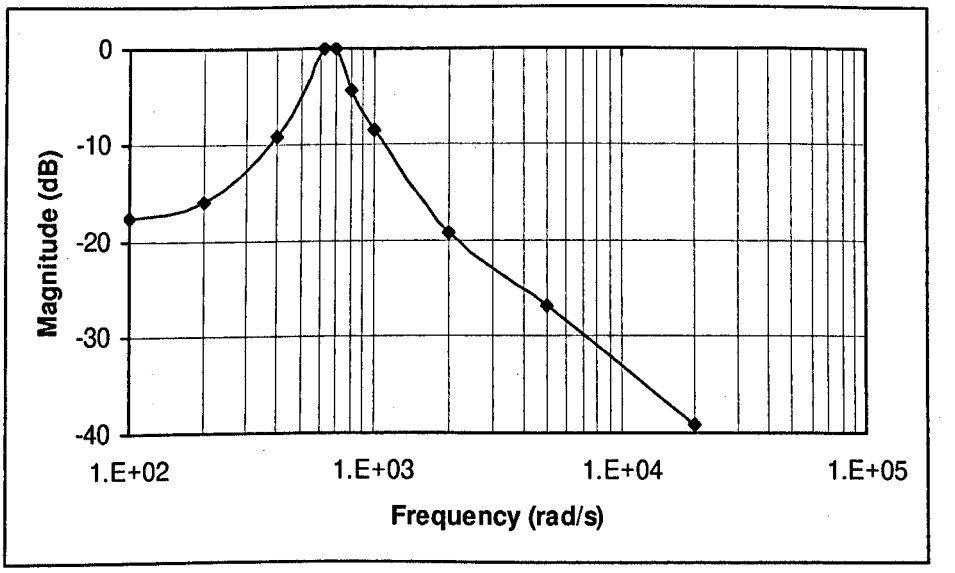

Figure 4.22 – Open-Loop Output Impedance Gain Response, $1\Omega \equiv 0dB$

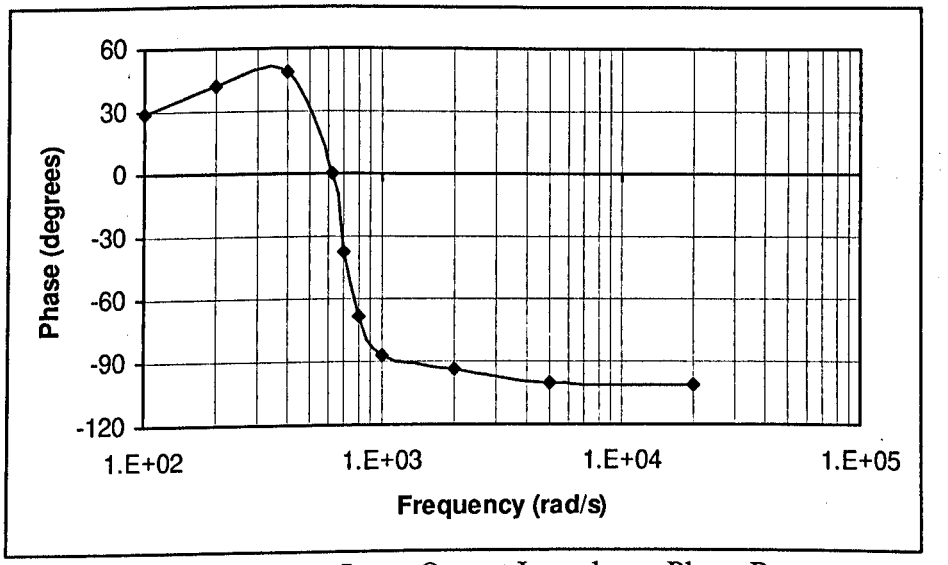

Figure 4.23 – Open-Loop Output Impedance Phase Response

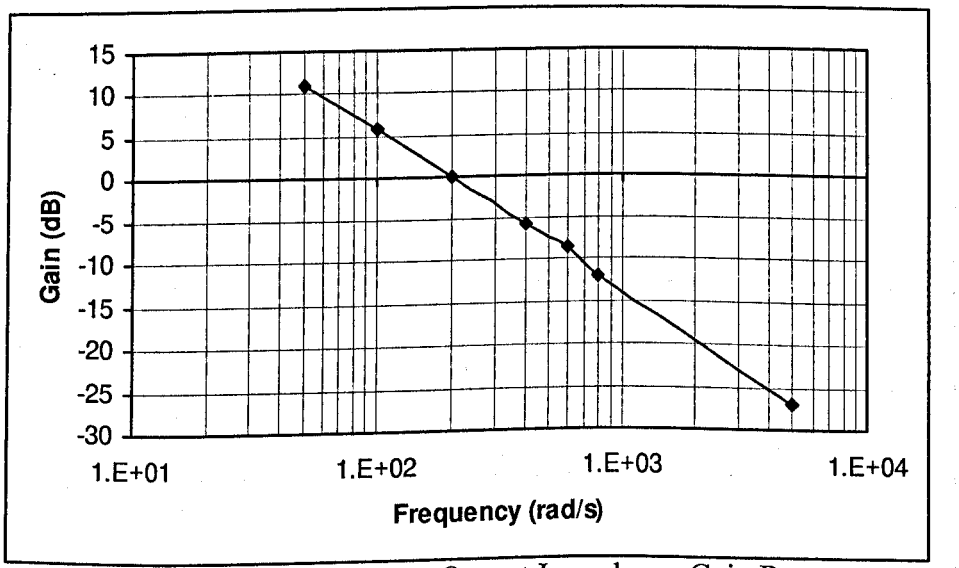

Figure 4.24 – Closed-Loop Output Impedance Gain Response

$1\Omega \equiv 0dB$

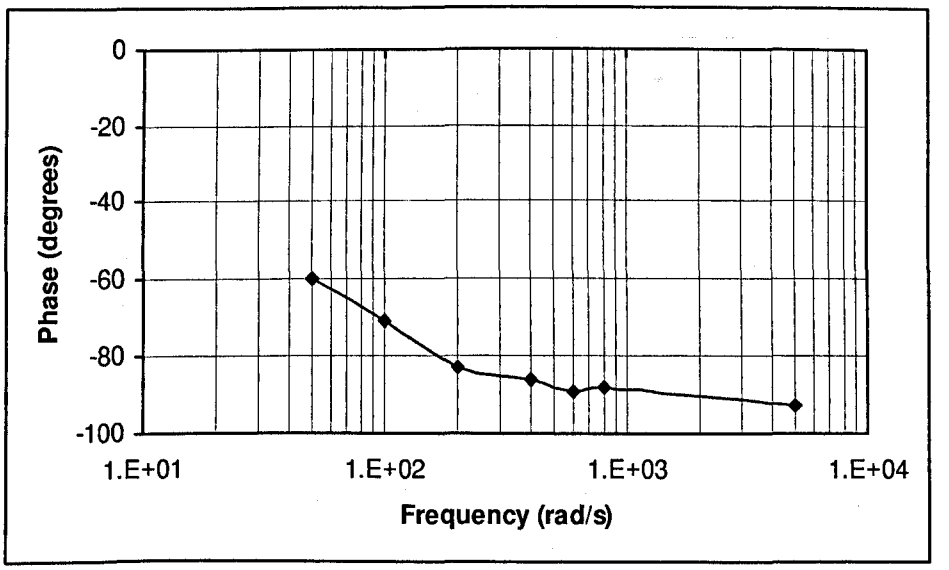

Figure 4.25 – Closed-Loop Output Impedance Phase Response

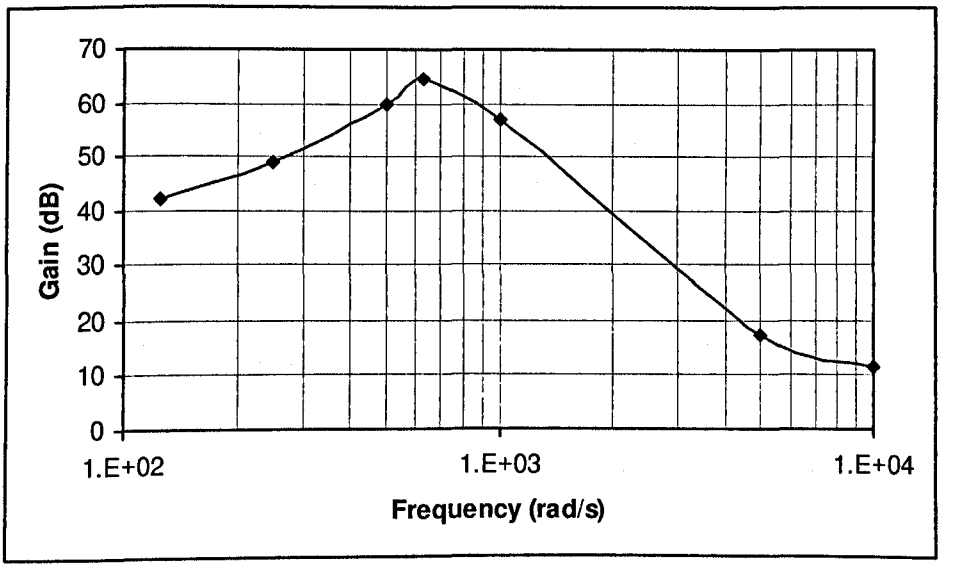

Figure 4.26 – Open-Loop Output-Current-to-Demand Gain Response

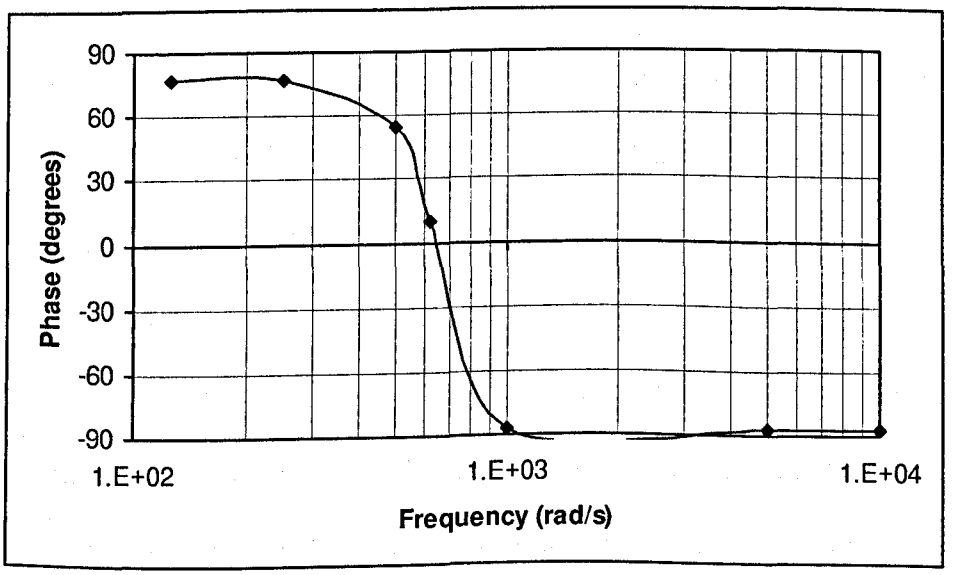

Figure 4.27 – Open-Loop Output-Current-to-Demand Phase Response

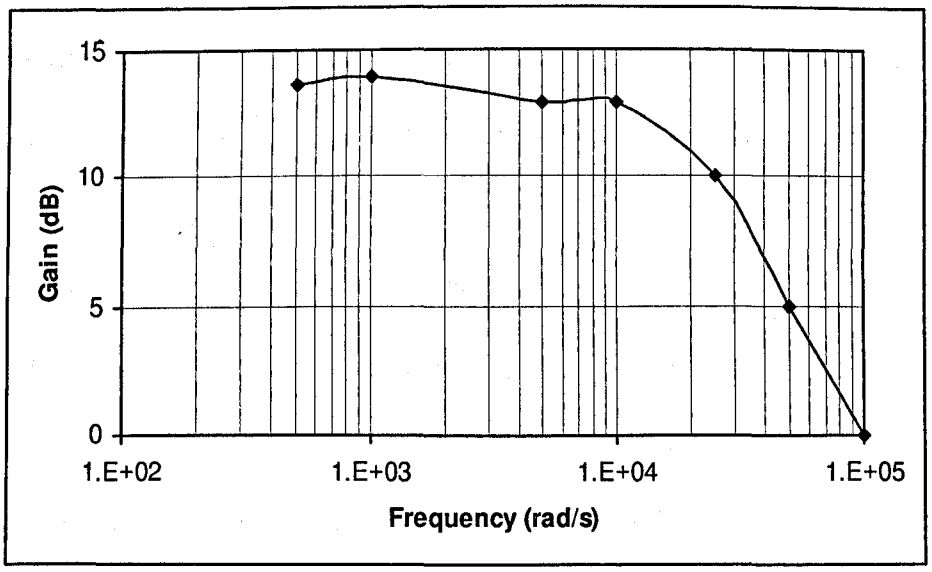

Figure 4.28 – Closed-Loop Output-Current-to-Demand Gain Response

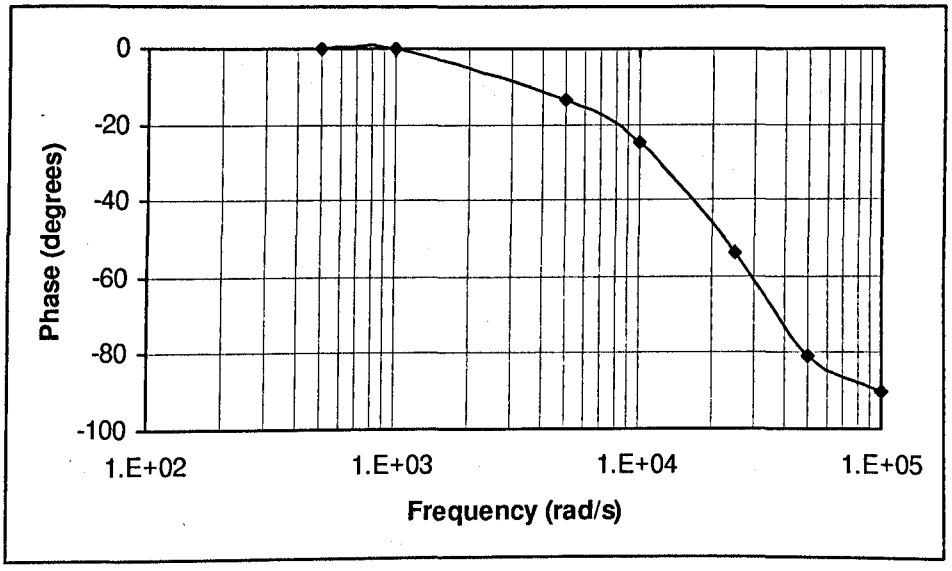

Figure 4.29 – Closed-Loop Output-Current-to-Demand Phase Response

The open loop plots show a resonant point at approximately 100Hz, which is the corner frequency of the dc filter (L_{dc}=500μH, C_{dc}=4700μF). Closing the current feedback loop has the effect of damping the resonant dc output filter, so that both the output impedance and output-current-to-demand plots exhibit single pole roll-off responses. This is desirable as it means that a stable system will exhibit a non-oscillatory response to changes in load and/or demand. The magnitude of the low frequency closed loop output impedance has increased compared with the open loop case and this, on the one hand, is undesirable as ideally it should be as low as possible to improve the rejection of

sudden changes in load. On the other hand, current feedback increases the input impedance of the dc filter, so reducing the magnitude of any 6^{th} harmonic currents due to flat-top mains distortion and this enables the use of a smaller dc-side inductance.

Limitations of Bode Plot Method for Switching Model

A limitation of the method described to obtain Bode plots from the switching model is that it becomes impractical for high or low perturbation frequencies. At low frequencies, the simulation will have a long run-time in order to simulate enough cycles. At high frequencies, aliasing becomes a problem and the perturbation signal becomes corrupted. Results are readily obtained for frequencies in the approximate range of 0.1 to 100 krad/s. For results over a wider range of frequencies, the dc-dc converter model can be used. One of the reasons behind taking point-by-point results from the switching model is to enable comparison with, and validation of, the dc-dc converter model. The point-by-point method can be used to obtain the frequency response of the system around several areas of interest; the cross-over point, the dc filter resonance point and the ac filter resonance point. However, it does not allow examination of the low frequencies down to dc, nor the high frequency response.

4.3.2 The Effects on the Frequency Responses of Adding an Input Filter

Demand-to-DC Current Transfer Function

Figures 4.30 and 4.31 show the effect of adding an input filter plus supply inductance of L_{ac}=1.4mH (corresponding to a variac setting of 40%, Section 4.8) and C_{ac}=6μF, with the current loop controller gain, k_p=6. The results are taken from the switching model.

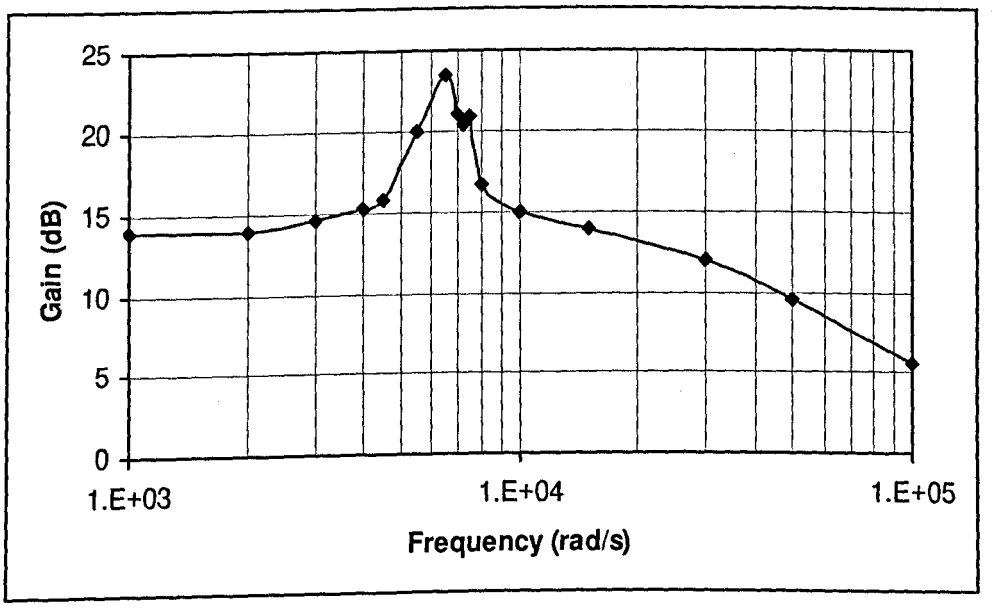

Figure 4.30 – Closed-Loop Current-to-Demand Gain Response

With an AC Input Filter

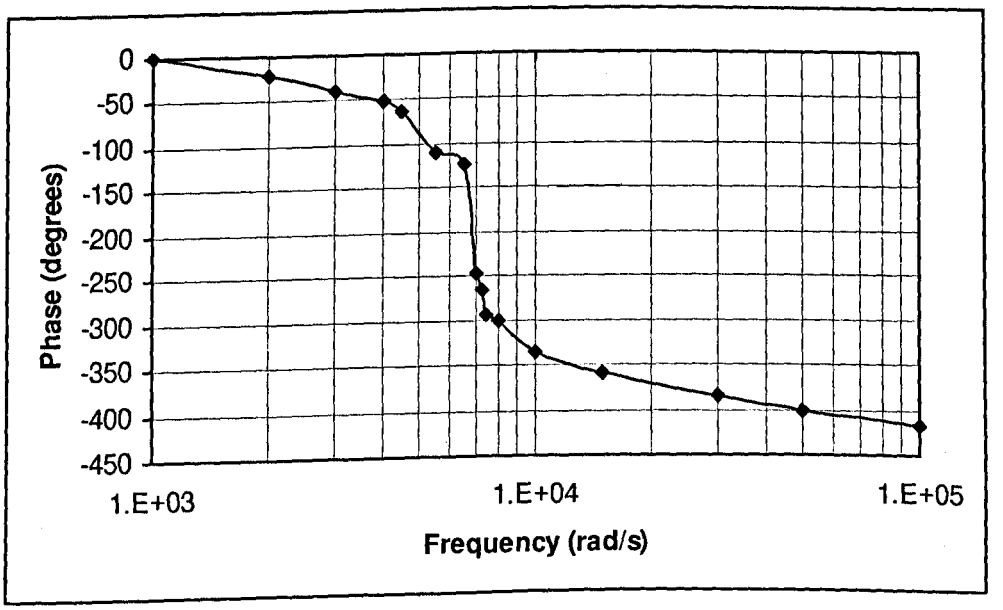

Figure 4.31 – Closed-Loop Current-to-Demand Phase Response

With an AC Input Filter

An unstable system results, with a resonant point of approximately f_{ac}=1kHz, which coincides with the resonant point of the input filter given by

$$f_{ac} = \frac{1}{2\pi}\sqrt{\frac{1}{3L_{ac}C_{ac}}} \tag{4.3}$$

(A factor of three appears in this equation due to the fact that the line-to-line inductance and capacitance are $1.5L_{ac}$ and $2C_{ac}$). The inductance seen at the input of the converter is dominated by the supply inductance, which can be an order of magnitude greater than

the inductance of the converter's input filter, Section 4.8. The input filter can turn a well-damped current-controlled system into an unstable, oscillatory one. The input filter needs to be damped and this is considered in Section 4.9. N.B. The converter itself provides no damping for the input ac filter because it is current controlled. Any increase in input voltage is countered by the current-loop maintaining constant dc-side current. Thus the converter is said to be a negative resistance load and can form a negative resistance oscillator.

DC-Side Output Impedance Transfer Function

The dc-side output impedance when using an input filter is shown in Figures 4.32 and 4.33.

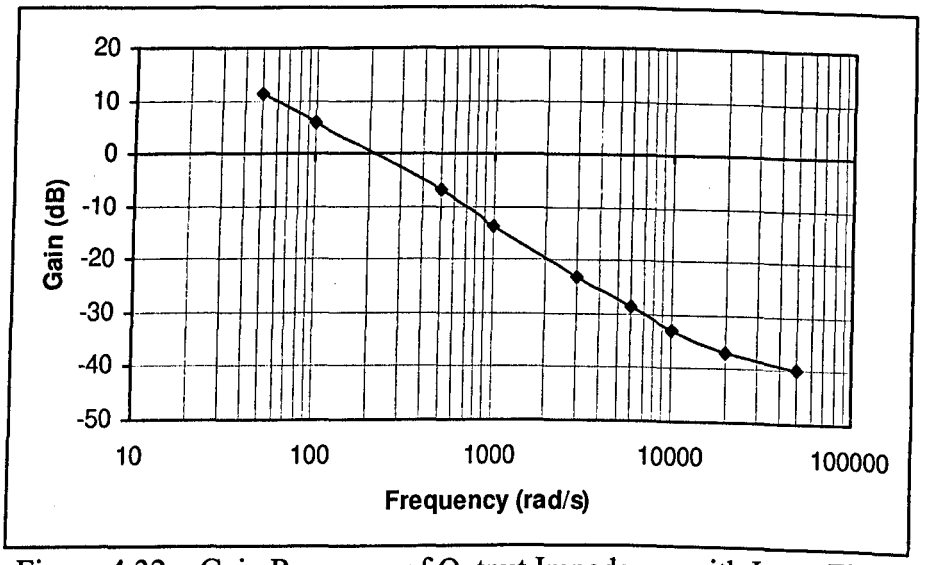

Figure 4.32 – Gain Response of Output Impedance with Input Filter

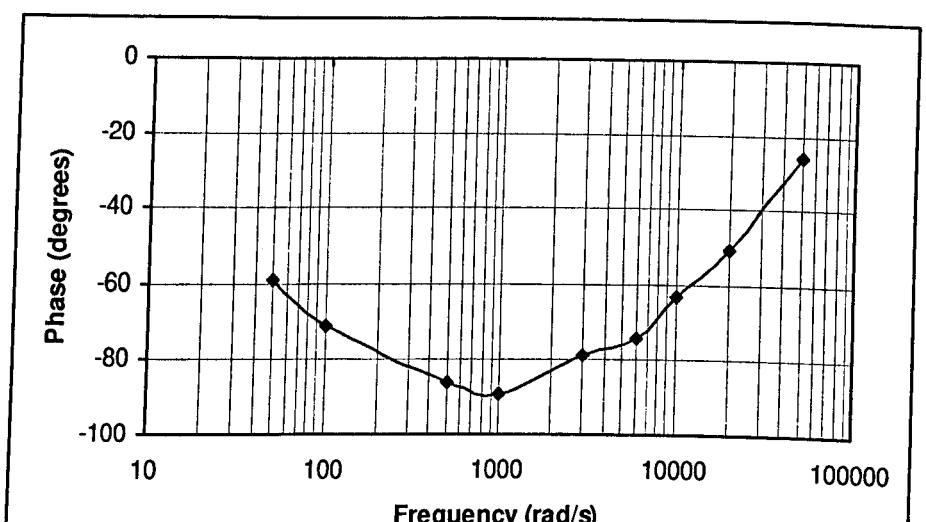

Figure 4.33 – Phase Response of Output Impedance with Input Filter

Note the lack of a high Q point due to the input filter. The response is essentially a single pole with a zero at high frequency (25 krad/s) caused by the dc capacitance's esr.

4.4 DC-DC Converter with Input Filter Equivalent Circuit Model

Development of the Model

The rationale behind reducing an ac-dc three-phase converter to a dc-dc converter [4.9] is that the analysis of the latter is simpler and well developed in the literature. The three-phase ac-dc converter can be represented as a dc-dc converter by realising that the formers operation is identical over each sextant, i.e. one phase is held on and the other two are switched. As regards to the control operation of the converter, it is unimportant as to which phases are switching and which phase is held on. Considering the ac-dc converter over any one sextant, the slowly-varying line-to-line voltages are averaged to a dc voltage and a conventional dc-dc converter PWM scheme substituted for the sinusoidal PWM scheme. The input and output of the converter can be separated; to the ac-side, the dc side looks like a current sink and to the dc side, the ac-side looks like a voltage source [4.14], Figure 4.34. The value of the dc voltage to replace the three-phase supplies is found by working backwards from the dc output

filter side as follows; the voltage applied to the output filter from the bridge is a pure dc one and equal to 1.5MV. The converter is a step-down one therefore when M=1 then, assuming a lossless system, the average dc input voltage is 1.5V. The value of the current drawn from the dc side and reflected into the "ac" side is MI_l. Input-to-output steady-state active power balance is achieved using these values; In the steady-state, V_{ac}=1.5V, and so active input power equals active output power which equals $1.5MVI_l$. The phase-to-phase inductance and capacitance on the "ac" side are $1.5L_{ac}$ and $2C_{ac}$.

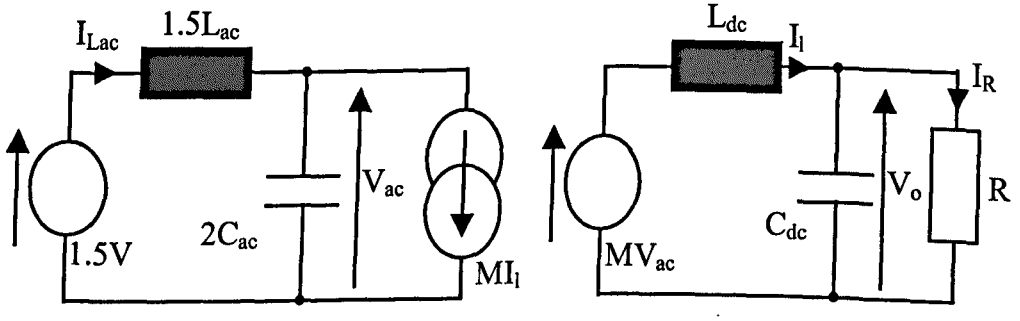

Figure 4.34 – DC-DC Converter Equivalent Model

Figure 4.34 can be represented by Equations (4.4a) and (4.4b) for the "ac" side and Equations (4.4c) and (4.4d) for the dc side. N.B. A high-value damping resistor, R_d=10kΩ, is placed in parallel with C_{ac} to aid simulation convergence by preventing the Q from being infinite.

$$I_{Lac} = \frac{1}{L_{ac}} \int (1.5V - V_{ac}) dt \tag{4.4a}$$

$$V_{ac} = \frac{1}{C_{ac}} \int (I_{Lac} - I_{Rd} - MI_l) dt \tag{4.4b}$$

$$I_l = \frac{1}{L_{dc}} \int (MV_{ac} - V_o) dt \tag{4.4c}$$

$$V_o = \frac{1}{C_{dc}} \int (I_l - I_R) dt \tag{4.4d}$$

The above equations are represented using SIMULINK™ in Figure 4.35, which also uses the same current controller (Figure 4.16) as for the switching model.

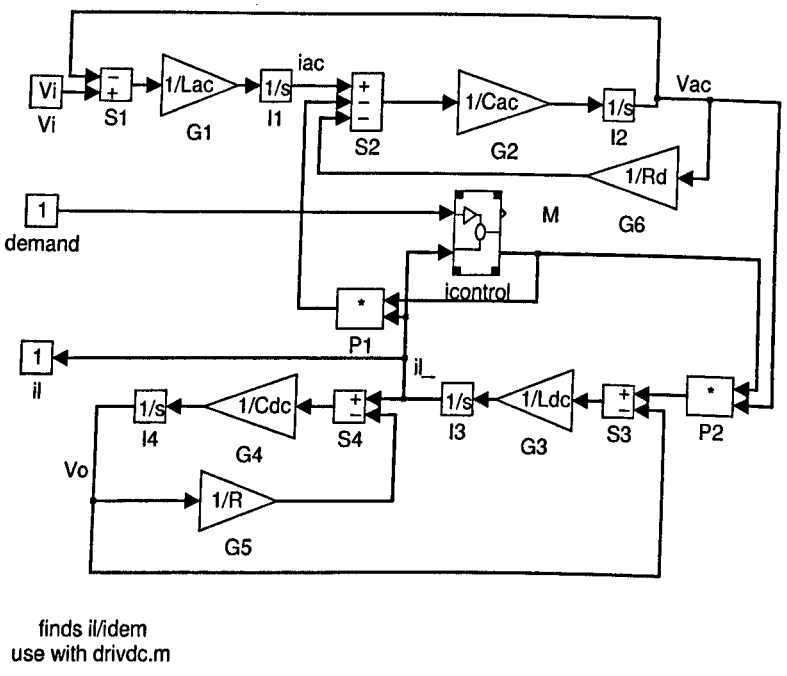

Figure 4.35 – DC-DC Converter Equivalent Model with Input Filter

This non-linear model can be linearised around a dc operating point (using the MATLAB™ commands 'trim' and 'linmod') and a number of different frequency responses examined to check for agreement between this model and the switching model.

Frequency Responses Using the DC-DC Model

Figure 4.36 gives the closed-loop current-to-demand response, taken under identical conditions to those used for the switching model responses shown in Figures 4.30 and 4.31. There is good agreement between the two models. The M-file used to produce Figures 4.36 and 4.38 is given in Appendix A10.

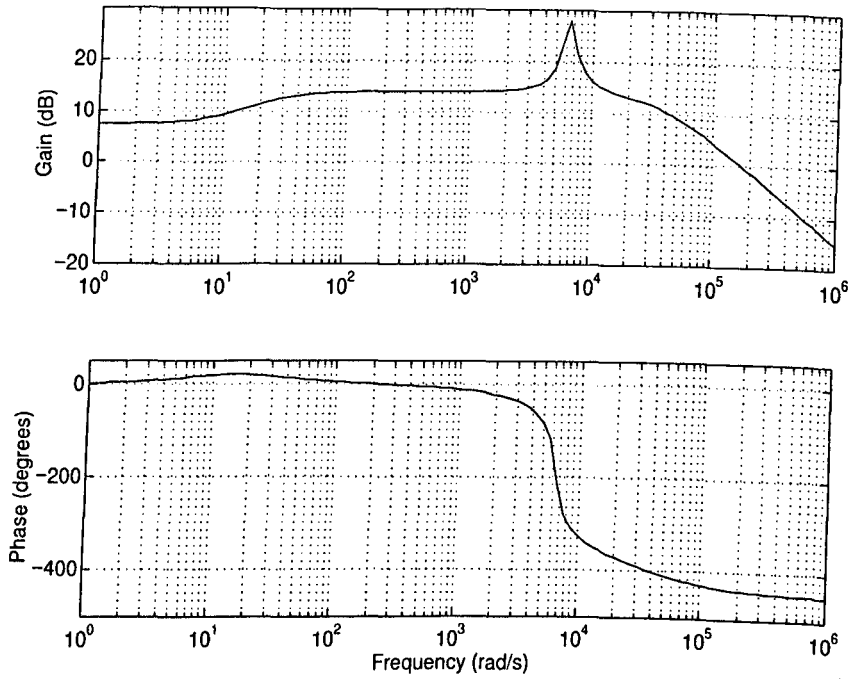

Figure 4.36 – Current-to-Demand Frequency Response Using the DC-DC Model with an Input Filter

The output impedance is shown in Figure 4.37 and should be compared with Figures 3.33 and 3.34.

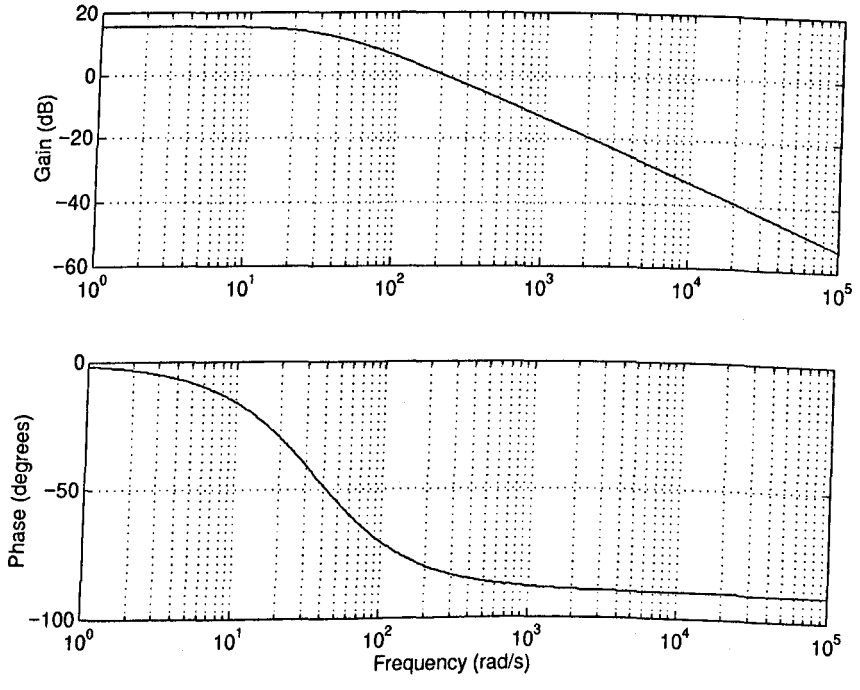

Figure 4.37 – Output Impedance Using DC-DC Converter Model with an Input Filter

The root-locus of the system is shown in Figure 4.38. This shows that the input filter generates a complex conjugate pair of left-half-plane (LHP) poles and a complex

conjugate pair of right-half-plane (RHP) zeros in the closed loop frequency response. The RHP zeros will cause the system to oscillate in an unstable manner.

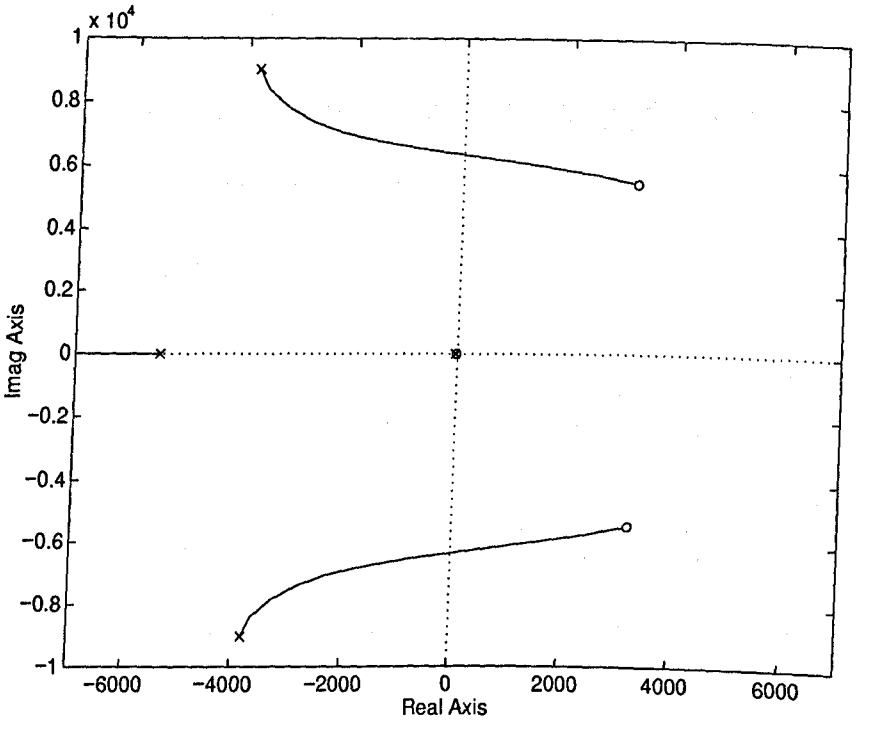

Figure 4.38 – Root-Locus of the DC-DC Converter Model with an Undamped Input Filter

Impedance Criterion

The impedance criterion states that the impedance looking back into the input filter from the ac input filter capacitor should be much less than the impedance of the converter looking forward from the ac input filter capacitor [4.18]. These two impedances can be found from the SIMULINK™ dc-dc converter model, Figure 4.35. The first impedance is found by adding a perturbation current via the summation block "S2" and looking at the ac voltage "Vac". The second impedance is found by taking the reciprocal of the admittance, which is found by adding a perturbation voltage to "Vac" and looking at the output current from block "P1". For a high value of damping resistor, R_d=3kΩ, the two impedance plots are shown in Figure 4.39. The impedance stability criterion is broken and the converter will oscillate in an uncontrolled fashion.

For a low damping resistance, R_d=30Ω, the impedance plots are shown in Figure 4.40 and the system will be stable. R_d=50Ω is the approximate boundary condition which corresponds to the complex conjugate zeros being positioned on the Imaginary axis. Increasing the controller gain also promotes the breaking of the impedance criterion as expected. See Appendix A11 for the M-files.

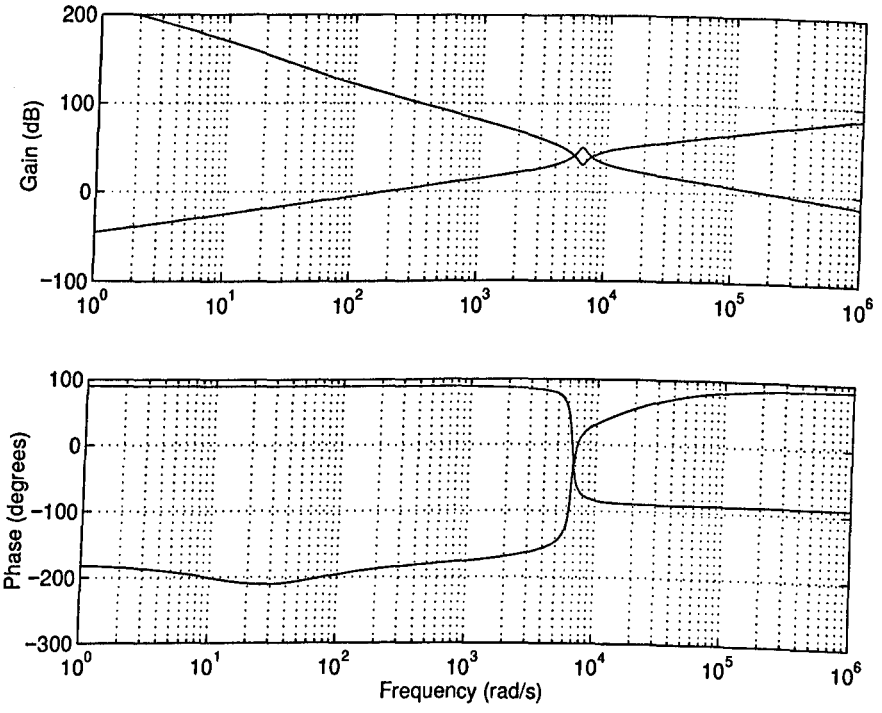

Figure 4.39 – Closed-Loop Impedance Plots for R_d=3kΩ

Upper Trace : Input Impedance of Converter

Lower Trace : Output Impedance of Input Filter

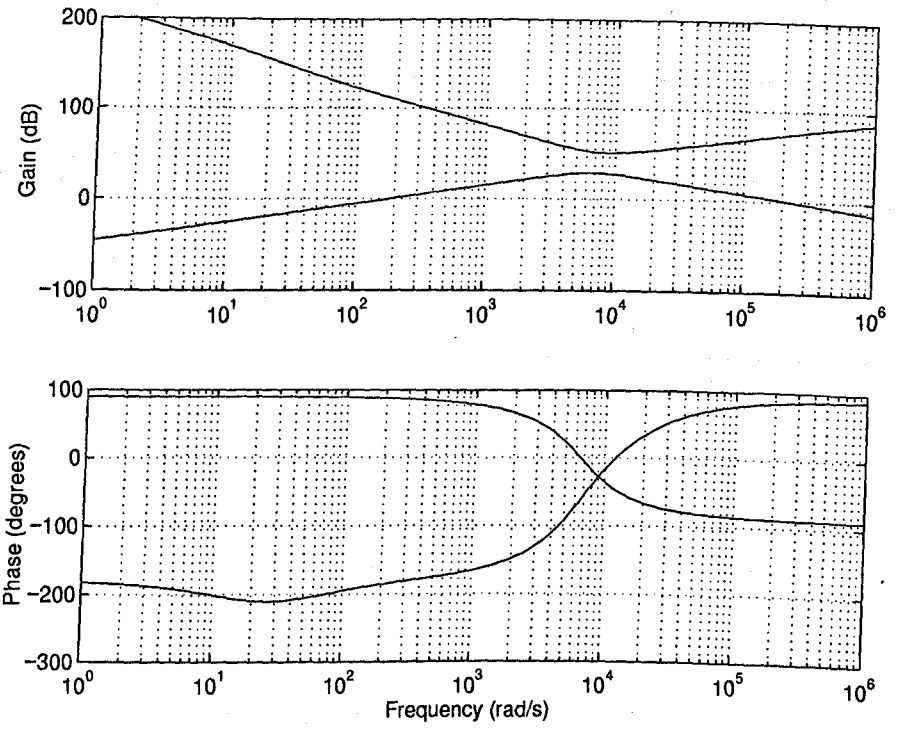

Figure 4.40 – Closed-Loop Impedance Plots for R_d=30Ω

Upper Trace : Input Impedance of Converter

Lower Trace : Output Impedance of Input Filter

4.5 Four Benefits of Average Current-Mode Control When Applied to the Converter

Four different benefits are derived from using a single dc-side current sensor and incorporating this into an average current-mode control scheme.

4.5.1 Damping of the Resonant DC Filter

Mathematical Analysis

The converter can be represented in the dc-dc converter format, only this time without the input filter, in order to isolate the effects of average current-mode control, Figure 4.41.

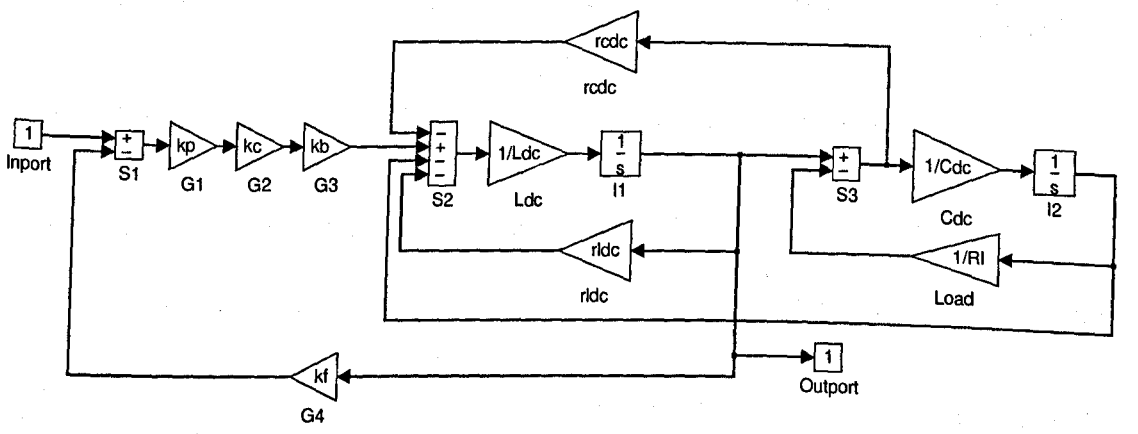

Figure 4.41 – DC-DC Converter Equivalent Model Without Input Filter

Note that this system is inherently linear compared with the case when there is an input filter. The transfer function, P(s), of the output filter and resistive load only is given by Equation (4.5), written in a form that normalises all frequencies to the centre frequency, ω_0, and expressing all other terms with respect to the Q-factors and the characteristic impedance, z_0 [4.18].

$$\frac{I_l}{V_{in}}(s) = P(s) = D\frac{\left[1+Q_L\left(s/\omega_0\right)\right]}{\frac{1}{F}\left(s/\omega_0\right)^2 + \left(\frac{1/Q_e + 1/Q_L}{F}\right)\left(s/\omega_0\right)+1} \tag{4.5}$$

where $\omega_0 = \sqrt{\frac{1}{L_{dc}C_{dc}}}$, $F = 1 + 1/Q_L Q_e$ and the dc gain, $D = 1/Q_L z_0 F$. (N.B. $D \approx 1/R$ and $F \approx 1$ if $\frac{1}{Q_e Q_L} << 1$). Also, the characteristic impedance, $z_0 = \sqrt{\frac{L_{dc}}{C_{dc}}}$, the series Q-factor, $Q_e = z_0/R_e$ and the parallel load Q-factor, $Q_L = R/z_0$. When the feedback loop is closed, the demand-to-current transfer function becomes

$$G(s) = \frac{kD}{1+kk_fD}\frac{\left[1+Q_L\left(s/\omega_0\right)\right]}{\left[\frac{1}{F'}\left(s/\omega_0\right)^2 + \left(\frac{1/Q_e + 1/Q_L + 1/Q_d}{F'}\right)\left(s/\omega_0\right)+1\right]} \tag{4.6}$$

where the forward gain, $k=k_pk_ck_b$, the feedback path gain, $k_f=1/5$, $F'=F+\frac{1}{Q_LQ_d}$ and the damping due to the feedback, $Q_d=\frac{z_0}{kk_f}$. This equation shows that the location of the zero is unchanged, whilst the location of the poles and dc gain vary with k and k_f. The denominator of Equation (4.6) can be arranged in the form $\left(\frac{s}{\omega_0'}\right)^2+\frac{1}{Q'}\left(\frac{s}{\omega_0'}\right)+1$, where the centre frequency and damping have changed to $\omega_0'=\omega_0\sqrt{F'}$ and $\frac{1}{Q'}=\frac{\frac{1}{Q_e}+\frac{1}{Q_L}+\frac{1}{Q_d}}{\sqrt{F'}}$. If $\frac{1}{Q_d}>>\frac{1}{Q_e},\frac{1}{Q_L}$ (as is the case for the component values used in this converter) then Q' can be approximated by $Q'\approx\frac{\omega_0'}{\omega_0}Q_d$, i.e. the damping of the system is dominated by the feedback damping effect. When Q_d is compared with $Q_e=z_0/R_e$, it is seen that with current feedback, the overall damping of the filter can be approximated by a loss-less resistor of size $kk_f\,\Omega$ in series with the inductor. This resistor has a large damping effect on the underdamped output filter and causes the resonant double poles to become two widely-separated poles. Examining the root-locus of the system, it is seen that as k increases, one of these poles moves towards the low frequency zero of Equation (4.6), which reduces or even cancels the effect of the pole, whilst the other pole moves towards infinity. If k is large enough, then the resulting system can be well-approximated by two widely separated real poles and a zero according to

$$G(s)\approx\frac{kD}{1+kk_fD}\frac{(s+\omega_z)}{(s+\omega_{hp})(s+\omega_{lp})} \tag{4.7}$$

where the high frequency pole, $\omega_{hp} = \frac{\omega_0'}{Q'}$, the low frequency pole, $\omega_{lp} = Q'\omega_0'$ and the zero, $\omega_z = \frac{\omega_0}{Q_L}$. (N.B. The capacitor esr will produce a zero that may need to be compensated for, but this is not considered here).

Frequency Domain Response

The Bode plot for Figure 4.41 for a proportional controller where k_p is varied is shown in Figure 4.42.

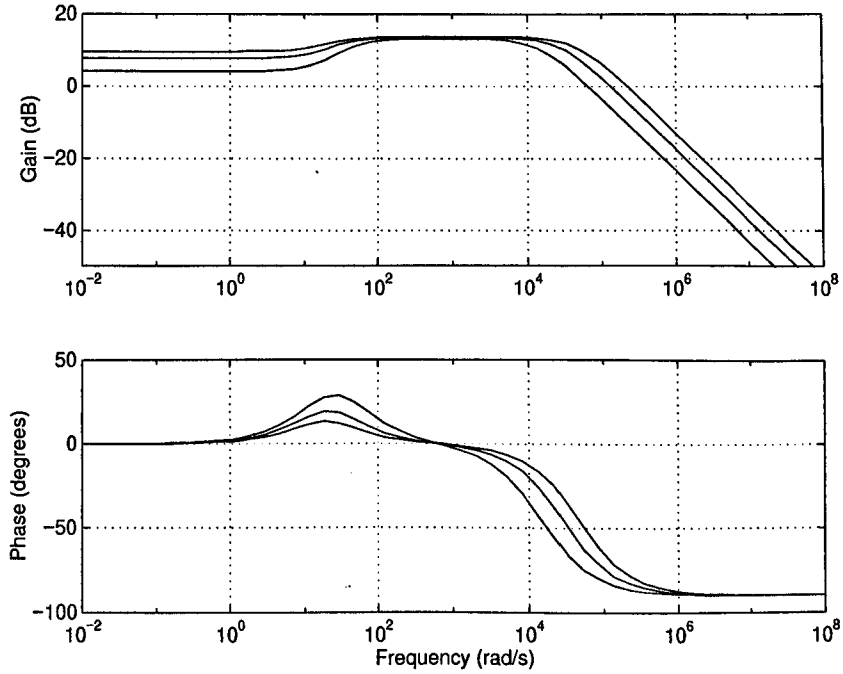

Figure 4.42 – Closed-Loop Bode Plot of Current-to-Demand as k_p is Varied

Gain Plot Upper Trace : k_p=10, Gain Plot Middle Trace : k_p=6

Gain Plot Lower Trace : k_p=3

The locations of the poles from Figure 4.42 for k_p=3 are –14650 and –44 rad/s and the zero is at –15 rad/s. These agree with the approximated theoretical values of -13200, -47 and –16 rad/s. Incomplete cancellation leads to the slow response and dc error shown in e.g. Figure 4.52. For the pole and zero to completely cancel, the gain k_p has to be large. This can lead to problems when the input filter is added, as if the gain around the resonant frequency of the filter is large the system can become unstable. A better

method is to use a PI controller where the zero is placed to cancel the low-frequency pole and k_p can be reduced. This is shown in Figure 4.43, where k_p=3 and k_i=300k_p rad/s. The poles are at -14370, -312 and -14 rad/s and the zeros are at -300 and -15.2 rad/s. The two lower-frequency poles and zeros cancel, to be left with only the high frequency pole according to

$$G(s) \approx \frac{kD}{1+kk_fD} \frac{1}{(s+\omega_{hp})} \tag{4.8}$$

Appendix A12 gives the text M-file details for the P and PI controller cases.

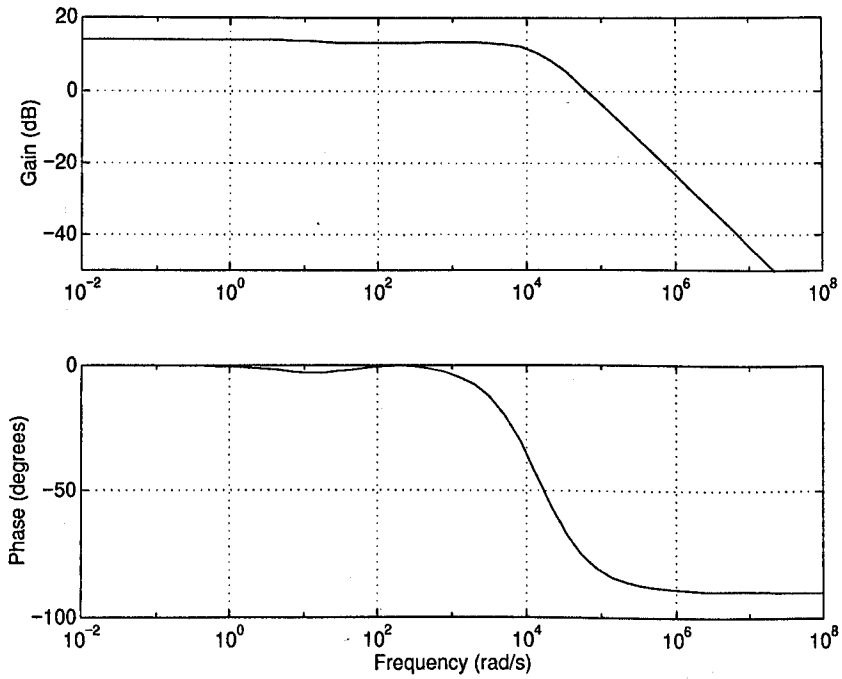

Figure 4.43 – Closed-Loop Bode Plot of Current-to-Demand for System with PI Controller

PI Gain Setting

Several different methods exist for tuning the gains of a PI controller. The most well known is the Zeigler-Nichols tuning method [4.21]. In practice, the switching noise of the converter, digital sampling effects and the input filter all reduce the controller gain that can be used to achieve a stable system. The Bode plots and root loci developed could be utilised to position the closed loop poles of the system.

Time Domain Response

Time-domain responses are shown in Figure 4.44 for a current demand of 7.5A. These show the dc error and slow settling time for the P controller and the improved response from the PI controller. In practice, the current loop will not respond as quickly as this approximation suggests, due to; the impedance of the input filters, the time delay due to the PWM and ADC and the delay due to the low-pass filter on the current-loop feedback signal.

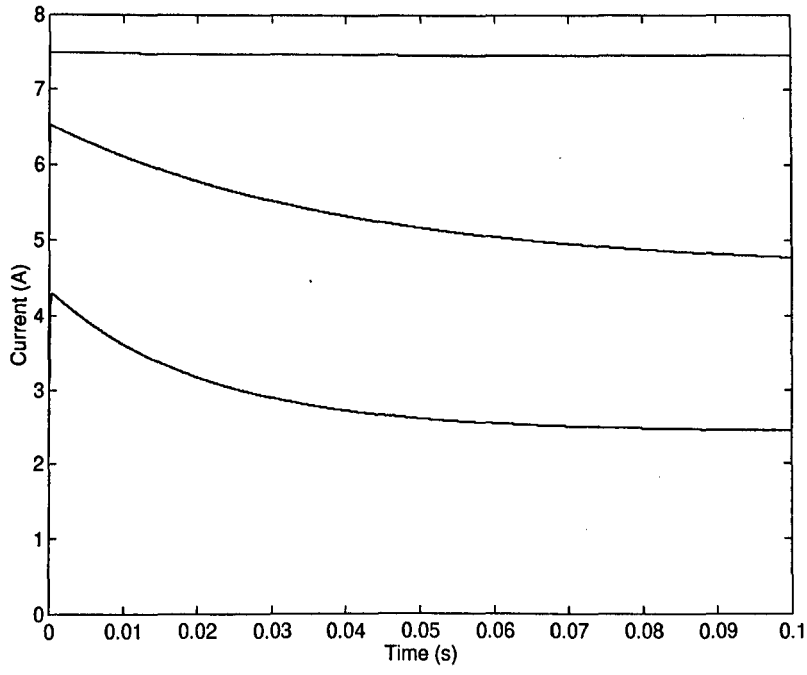

Figure 4.44 – Closed-Loop Step-Change Time-Domain Responses of DC Inductor Current

Upper Trace : $k_p=3$, $k_i=300k_p$

Middle Trace : $k_p=10$, Lower Trace : $k_p=3$

Approximating the current-control loop to a single pole system is useful when the outer voltage feedback loop is added. The resulting simplified system has slow and fast poles that can be considered to be decoupled from each other and is straightforward to analyse.

Analysis of the System with an Input Filter

In theory, the case of a converter with an input filter could be analysed using the circuit-theory equivalent linear model of the switch and diode [4.6]. In practice, this leads to a transfer function with a third-order numerator and fourth-order denominator. The extra-element theorem (EET) [4.16, 4.17], which allows the converter to be analysed without the filter (as has already been done) and the filter added later as the extra element, does not simplify the analysis. The EET, it was discovered, only reduces the amount of circuit theory analysis when the original circuit contains only resistive elements and the extra element is reactive. Examples of the original circuit where the EET reduces the amount of work needed are resistive bridges and resistively biased transistors. The method outlined in Section 4.4 makes the simulation package perform the linearisation around a dc operating point. The simulation's linear systems analysis functions can then be used.

Non-Linear Loads

Consideration of the converter supplying non-linear or constant-current loads has not been considered, although this could be a topic for further work. Previous work has indicated that the size of the dc-side capacitor compared to the capacitor located in the load itself is important [4.18].

4.5.2 Reduction of Harmonic Currents

The effect of the average current-control loop is to increase the impedance of the dc output filter as seen by the bridge. Any voltage harmonics output from the bridge will produce lower magnitude harmonic currents, which means lower ac-side harmonics. The controller tries to force the dc-side current to be a pure dc term. If 6^{th} harmonic exists on the dc side, the current controller will feed 6^{th} harmonic of the

opposite sign back, which on the ac-side translates into 5th and 7th of the opposite sign to the 5th and 7th produced by flat-topping In the limit, the control loop with infinite gain and bandwidth will achieve this (the dc-side becomes a pure dc controlled current-source). MathCAD™ was used to examine the limiting case to see the effect on ac harmonic production. Figure 4.45 shows a typical example of the ac-side current when the dc-side current has been corrected to a pure dc term. The mains is flat-topped by 15% (and will therefore generate harmonics) and M=0.8. See Appendix A13 for the MathCAD™ listing.

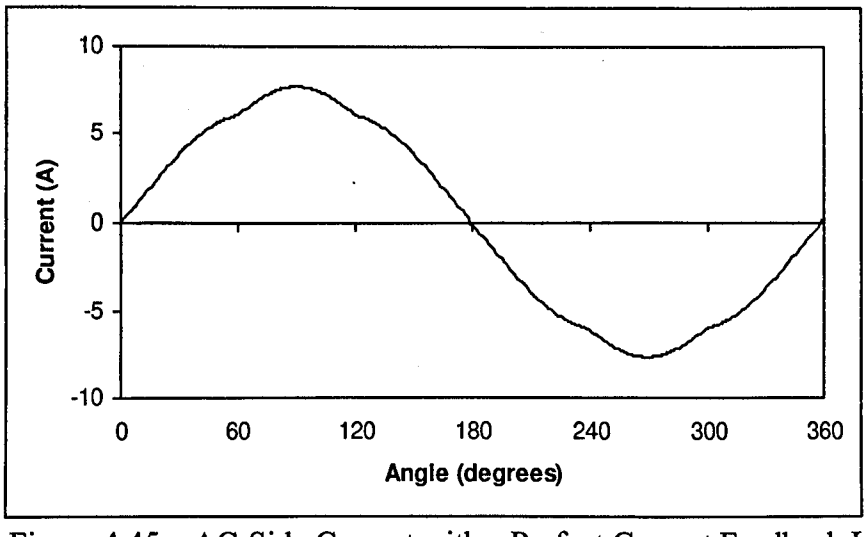

Figure 4.45 – AC-Side Current with a Perfect Current Feedback Loop

The variation in M over a 60° interval to achieve this current is shown in Figure 4.46.

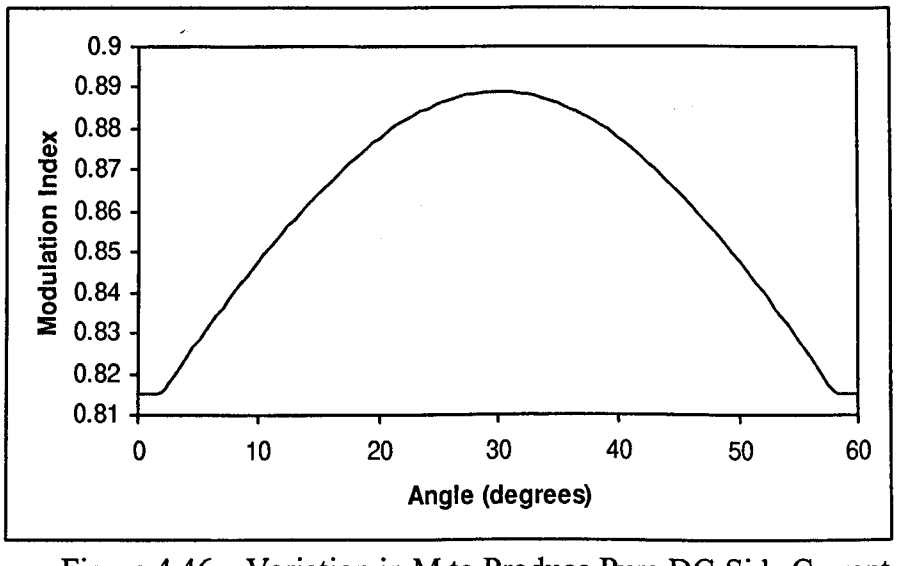

Figure 4.46 – Variation in M to Produce Pure DC-Side Current

The ac-side current harmonics are shown in Figure 4.47, these harmonics being mostly 5^{th} and 7^{th}. Controlling the dc-side current does not force the harmonic currents to zero, but it does reduce them. The same simulation as used for the closed loop case was modified to run open-loop. In the open-loop case, for varying M, the input current total harmonic distortion (THD) was found to be constant at 8.7%. For the closed loop case and varying M, the THD was constant at 3%. At high modulation indices (M>0.95), the controller starts to saturate, resulting in the closed-loop THD approaching the open-loop value.

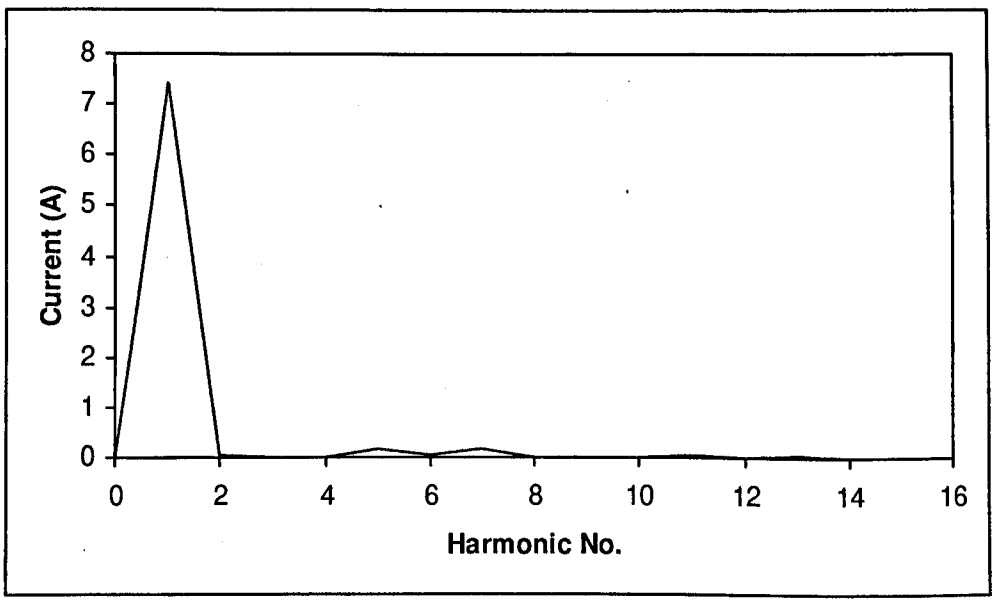

Figure 4.47 – AC-Side Current Harmonics with Perfect Current Feedback Loop

The switching simulation, when run under the same conditions, gives the ac-side current as being Figure 4.48 (which should be compared with Figure 4.45). The same waveshape is also seen on the practical result in Figure 4.49.

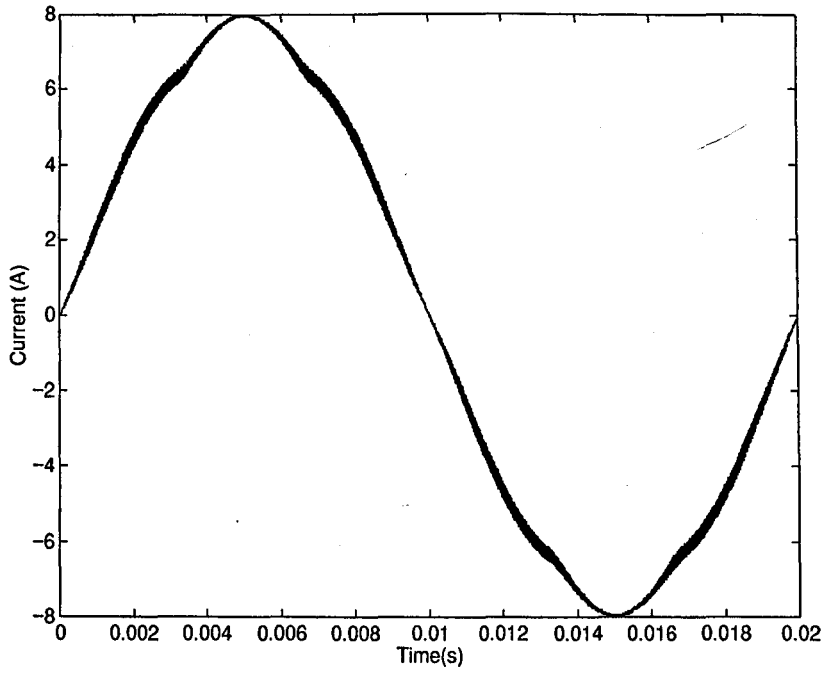

Figure 4.48 – Closed-Loop Switching Simulation

Input AC Current for k=0.85

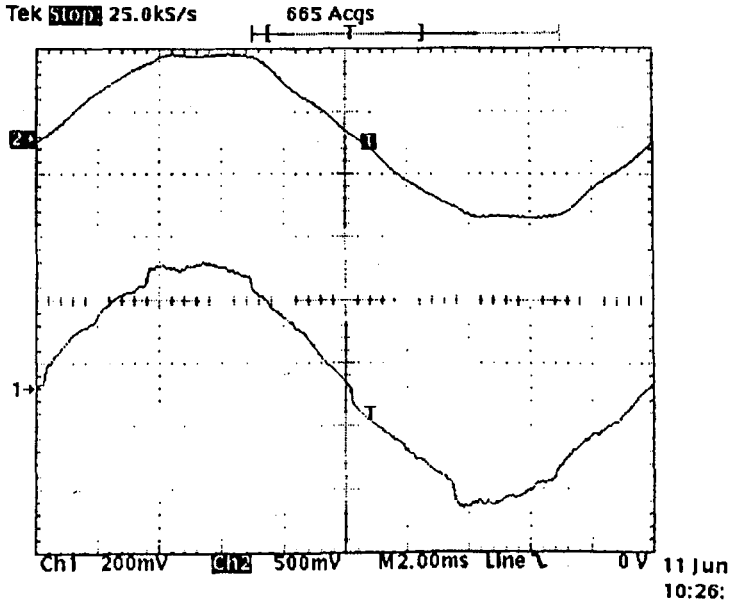

Figure 4.49 – Practical Waveforms for Closed Current Loop Control

Upper Trace : Line-Neutral Voltage 200V/div

Lower Trace : Input Current 2A/div

The reduction in both the ac and dc-side current harmonics due to the closed current loop is shown in Figures 4.51 and 4.52 when compared with the open-loop case, Figures 3.30 and 3.31.

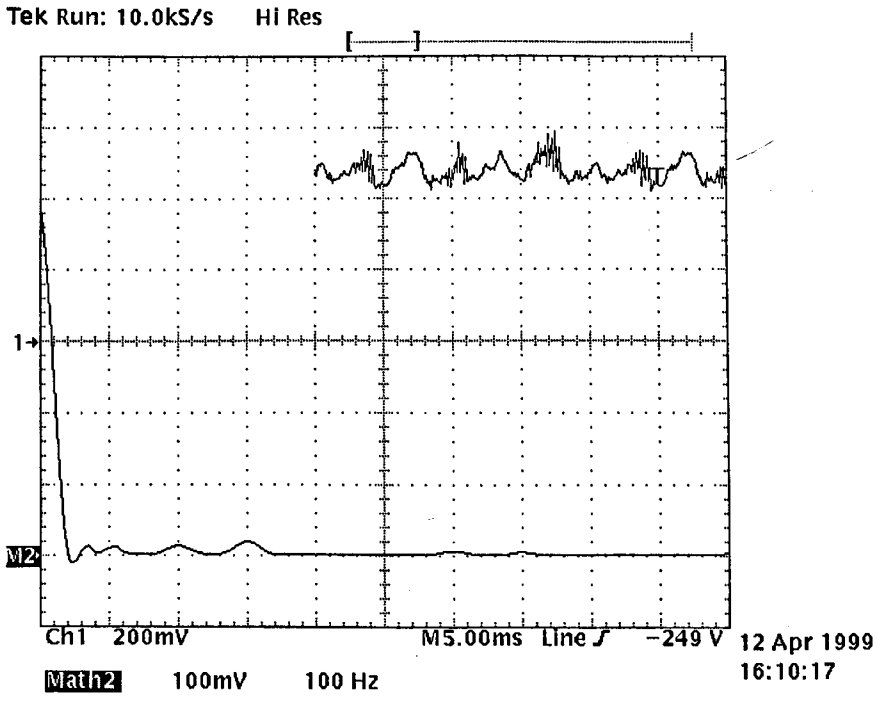

Figure 4.50 – Practical Closed-Loop Steady-State Performance

Upper Trace : DC Inductor Current 2A/div

Lower Trace : FFT of DC Inductor Current 100Hz/div, 1A/div

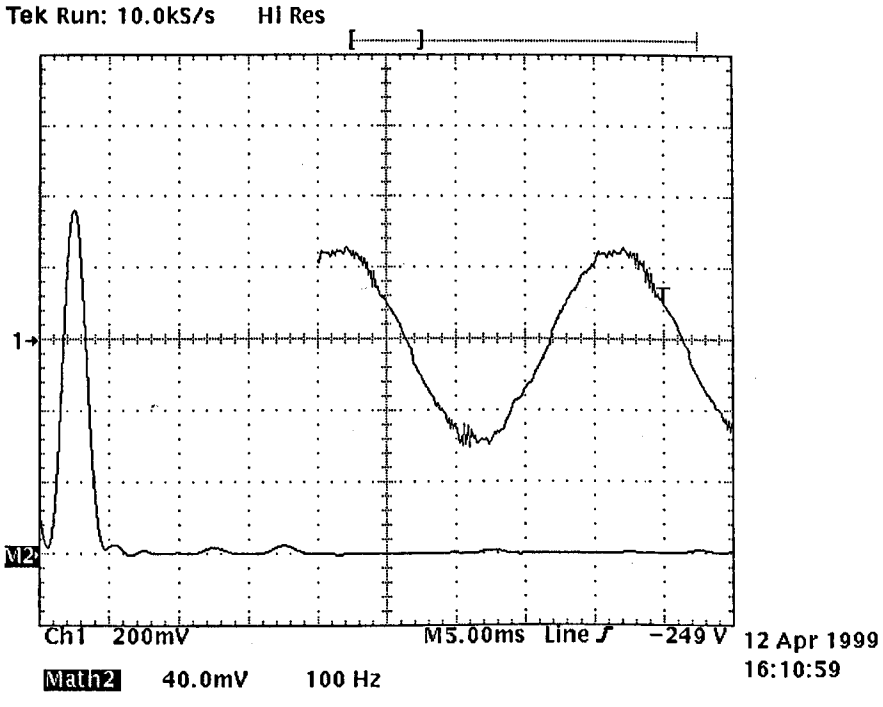

Figure 4.51 –Practical Closed-Loop Steady-State Waveforms

Upper Trace : AC Input Current 2A/div

Lower Trace : FFT of AC Input Current 100Hz/div, 0.4A/div

4.5.3 Parallel Operation of Converters Driving a Common Load

For parallel operation of converters driving a common load and sharing the same dc output capacitor (see Chapter 5), the dc currents produced by each converter (when run under open-loop conditions and for the same value of M) will be different. This is due to the two converters not having the same impedance or voltage drops across semiconductor devices in their "go" and "return" current-paths. PI current controllers placed in each converter's dc-side current path can reduce the current-sharing error.

4.5.4 Average DC-Side Current Limit

Hardware or software current limits can be set to take action if the dc inductor current exceeds certain values. The action taken could vary from; doing nothing (to allow a specified over-current condition to exist for a certain time), reducing the value of M, and finally shutting down the converter if the over-current condition persists.

4.6 Step-Change Responses

The step responses of the switching converter to a step-change in current demand were taken under conditions of closed-loop average current control and **(i)** no input filter, **(ii)** an undamped input filter and **(iii)** a damped input filter. The controller used for these tests is just a P rather than PI in order to keep things as simple as possible and to exclude the possibilty of the integral term of the PI controller causing instability. The inductance of the supply, L_s, is included in the input filter model.

The simulation response of the system without an input filter to a change in demand is shown in Figure 4.52.

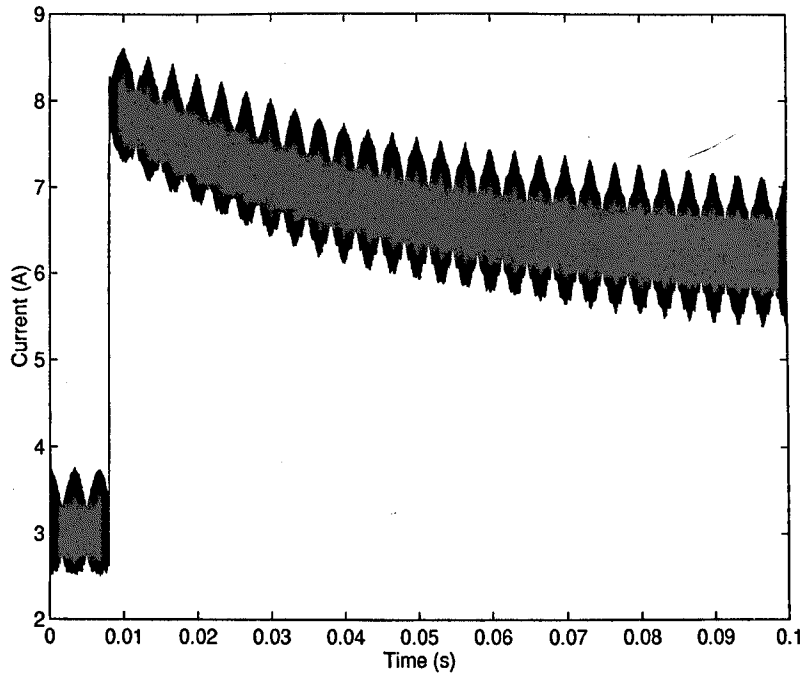

Figure 4.52 – DC Inductor Current Response to Step Demand, No Input Filter

The response is well damped. When an input filter is added, the simulated response changes to that of Figures 4.53 and 4.54 which show underdamped behaviour.

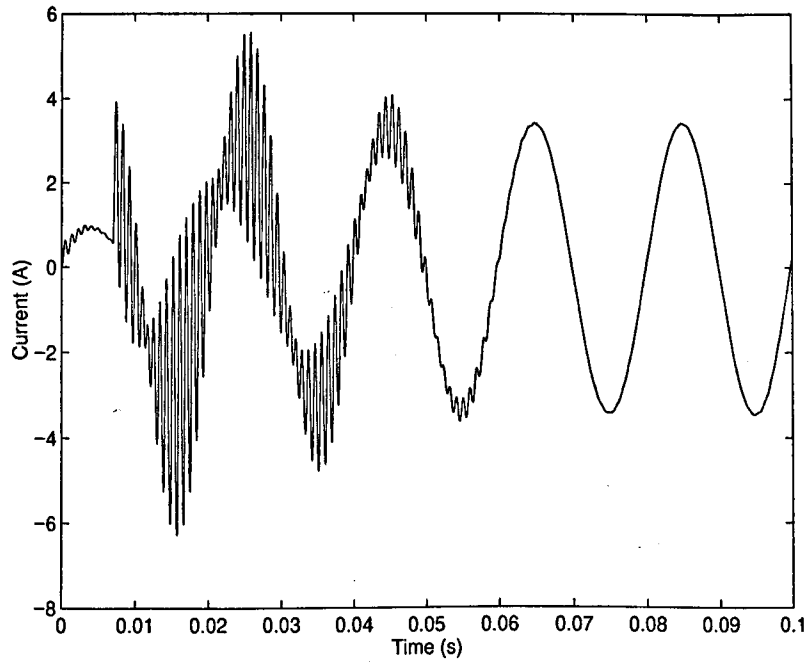

Figure 4.53– Step-Response AC Input Current with Undamped Input Filter

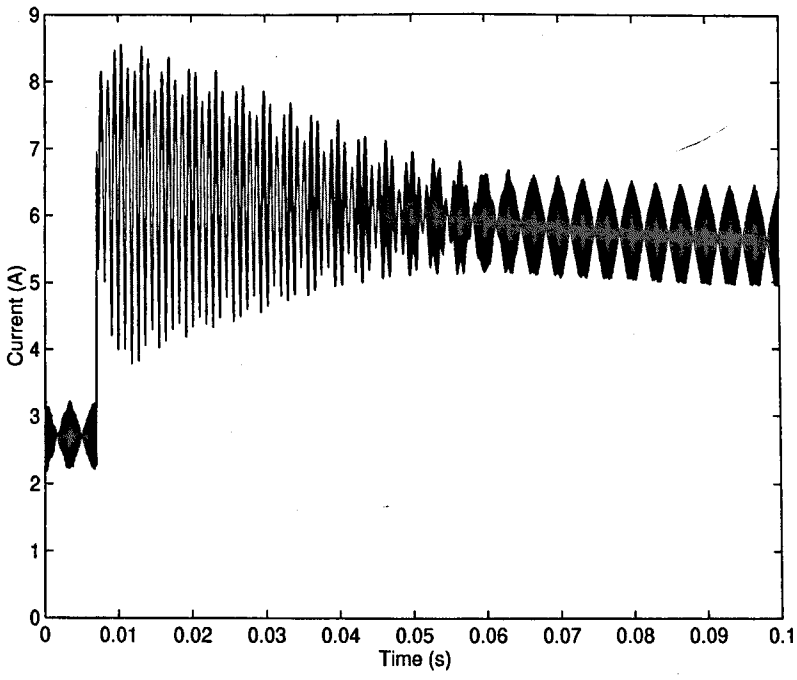

Figure 4.54– Step-Response DC Output Current with Undamped Input Filter

The practical test-rig response is shown in Figure 4.55 The oscillation frequency coincides with that of the simulation at approximately 1kHz. The practical result shows better damping compared with the simulation possibly due to frequency dependant damping in the power supply and variac.

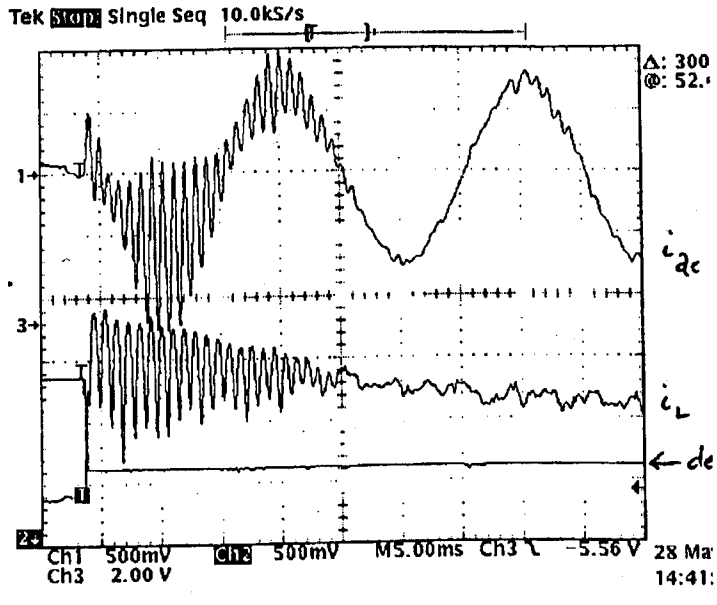

Figure 4.55– Step Change Response On Practical Rig

Upper Trace : Input Current 5A/div

Middle Trace : DC Inductor Current 5A/div

Lower Trace : Demand 2V/div

4.7 Low-Pass Filter on Current Feedback Signal and Gain/Stability Trade-Off

Choice of Low-Pass Filter Corner Frequency

The single pole low-pass noise filter placed in the current control loop is shown in Figure 4.16. The choice of its corner frequency is important, as an incorrect choice will reduce the phase margin of the system. If the filter corner frequency is too low, then a significant additional phase lag will be introduced at around the cross-over frequency of the system, degrading the phase margin. This problem only becomes apparent when an input filter is used and the phase shift associated with it exists. The purpose of the control loop filter is to reduce the high frequency noise on the current feedback signal and provide some anti-aliasing properties and so it should be placed at such a point so as not to degrade the phase margin e.g. a factor of ten away from the crossover frequency.

Slope Condition and ADC Aliasing

The slope condition for average-mode current-controllers states that for stability, the slope of the measured, amplified current should be less than the slope of the triangular carrier at the comparator's inputs [4.20]. In the case of this converter which utilises an ADC, this condition does not apply as each sampled value is held for two switching cycles and there is no possibility of subharmonic oscillations or multiple switching transitions due to this effect. Instead, there exists the problem of high frequency signals being aliased to become low frequency signals, so adding a distortion component into the feedback signal. The dc-side filter is part of the low-pass anti-aliasing filter, as is the low-pass filter in the current control loop. The system might benefit from the ADC sampling rate being increased from $f_s/2$ to f_s or $2f_s$ and a high-

order, low-pass or notch filter added to the control loop at a frequency that will not introduce significant additional phase lag around the cross-over frequency.

Correction of Harmonic Distortion and Stability Trade-Off

The gain of the current control loop needs to be as high as possible around the 6th harmonic frequency (300Hz) in order to reduce the input current distortion when the supply voltages are flat-topped. Even when using a PI controller, where the proportional gain can be set to be low and the location of the zero placed in-between 300Hz and the input ac filter resonance point, it is difficult to achieve a stable system. A stable system can be achieved if the low-pass filter on the current control loop is set to a low frequency, but at the expense of correcting for the distortion. A better solution is to introduce some damping of the input filter to reduce its Q-factor, Section 4.9, which has the effect of making the system easier to stabilise.

4.8 Mains Supply and Variac Inductance

Note that the frequency of oscillation is 1kHz in the case of an undamped input filter. The natural, line-to-line frequency of the input filter (L_{ac}=50μH, C_{ac}=6μF) is 5.3kHz. The difference between the two frequencies is due to the inductance of the supply decreasing the resonant frequency of the input filter. Adjusting the variac to a number of different positions and connecting a C_T=18μF capacitor across the variac line-to-line output gives a transient oscillation which can be captured on a digital oscilloscope. If the capacitance is known (C_T is assumed to dominate the supply capcitance) and the frequency of oscillation measured, then the inductance per phase, L_s, can be found using Equation (4.9). The results are tabulated in Table 4.1.

$$L_s = \frac{1}{8C_T\pi^2 f_{osc}^2} \tag{4.9}$$

Variac Setting (%)	Oscillation Freq. f_{osc} (kHz)	Inductance L_s (mH)
20	1.1	0.6
30	0.83	1.0
40	0.71	1.4
50	0.68	1.5

Table 4.1 – Per-Phase Inductance of the Variac Plus Supply

The supply short circuit per-phase current was measured to be 1.6kA for a 240V supply. The full power inductance was therefore calculated to be approximately 0.5mH. Even if the variac was not in the circuit, the supply inductance is much larger than the input filter inductance. The corner frequency of the input filter is therefore strongly dependant on the power system it is connected to and creates a degree of uncertainty as to whether or not the system will be stable.

4.9 Passive Damping of the Input Filter

The undamped system is characterised by being difficult to stabilise whilst on the other hand, the damped system is easily stabilised and is relatively insensitive to the PI controller and low-pass filter pole and zero placement. The simplest method of damping is to place resistors in parallel with the filter capacitors. On the practical rig this gives rise to Figure 4.56 and shows an increase in damping as expected compared with Figure 4.55.

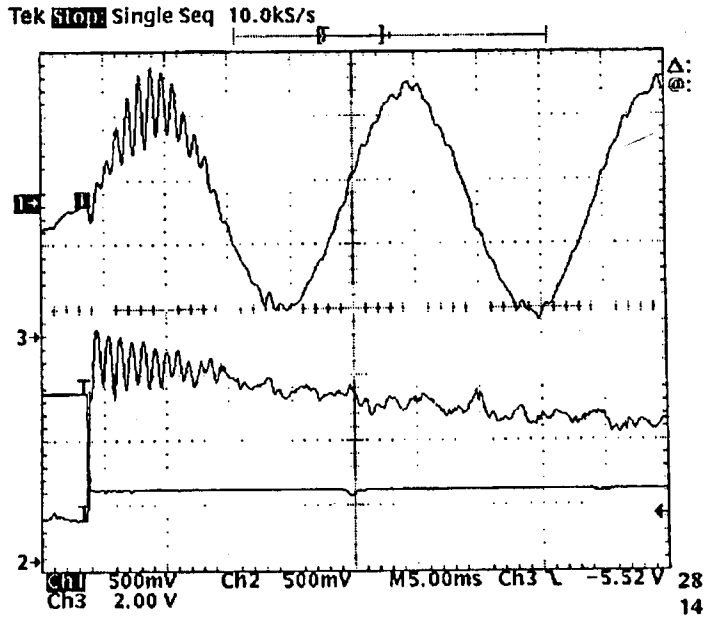

Figure 4.56– Step Change Response on Practical Rig with Damping Resistor

Upper Trace : Input Current 5A/div, Middle Trace : DC Inductor Current 5A/div,

Lower Trace : Demand 2V/div

If the dc-dc converter model is used with a heavily resistively damped input filter (R_d=30Ω) then the RHP zeros move into the LHP and the system is stable, Figure 4.57 This figure should be compared with the undamped case, Figure 4.40

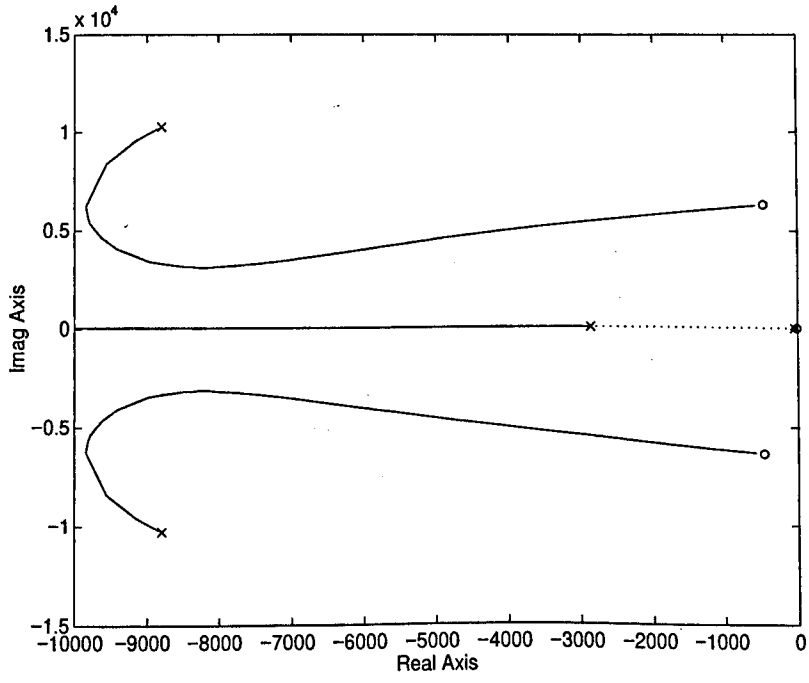

Figure 4.57– DC-DC Converter Model Root-Locus Plot for Damped Input Filter

This method of damping is energy inefficient and so an alternative method is to use the ac-line-blocked capacitor and resistor method illustrated in Figure 4.58 for a three-phase

system. The principle of operation of this method is that at resonance, the resistive path (C_d, R_d) is preferred over the non-resistive path (L_{ac}, C_{ac}). Thus C_d should be much larger than C_{ac} [4.19].

$$C_d \geq 3C_{ac} \tag{4.9}$$

For the three-phase filter, the damping resistor, R_d, is typically made equal to the line-to-line filter characteristic impedance.

$$R_d = \sqrt{\frac{3L_{ac}}{4C_{ac}}} \tag{4.10}$$

If C_{ac}=6μF and L_{ac}=1.4H then $C_d \geq 18\,\mu F$ and R_d=13Ω. The actual values used in practice are C_d=18μF and R_d=15Ω. These values were used as the components were readily to-hand. Section 4.10 shows that the system is tolerant to changes in the input filter inductance; the choices of R_d and C_d are not critical. Mains frequency power is still dissipated in each damping resistor. The power dissipated in each resistor is given by

$$P_d = \left(\frac{V_L}{1/\omega_m C_d + R_d} \right)^2 R_d \tag{4.11}$$

Where V_L is the rms line voltage and ω_m the line frequency. A line voltage of 190Vrms gives P_d=15W.

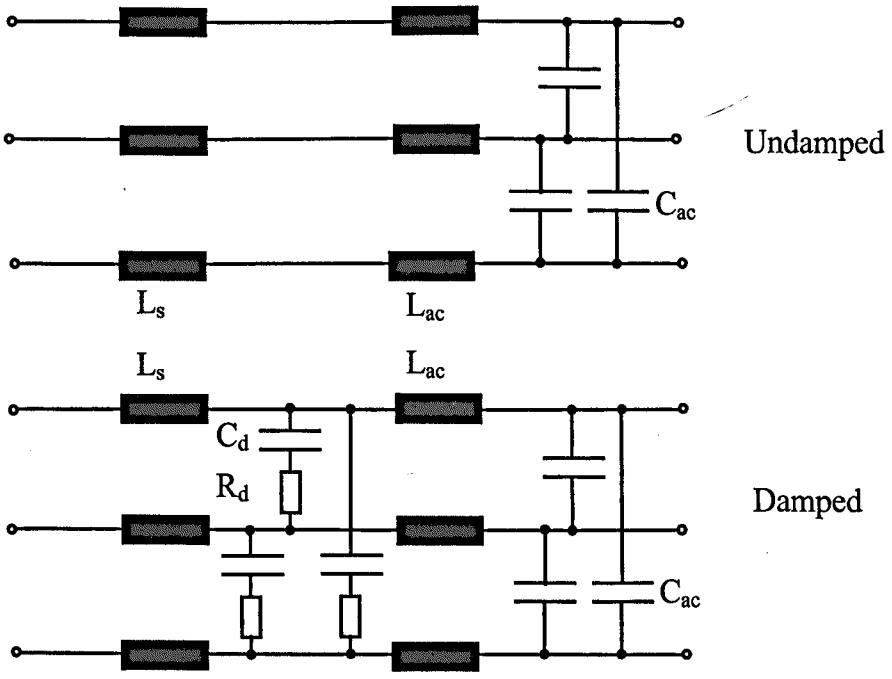

Figure 4.58 – Undamped and Damped Input Filters

It was found to be beneficial stability-wise to place the damping components before rather than after the ac filter inductors. This is possibly because any input filter oscillations are steered down R_d and C_d and the input filter inductors, L_{ac}, provide some isolation between this and the voltages at the input filters' outputs. The effect of the damping is shown in Figures 4.59 and 4.60 where the increase in current demand signal is shown as a negative voltage step due to operational amplifier inversion in the practical test rig. The system, under a step-change in demand, behaves as it did before the input filter was added, i.e. a well damped response.

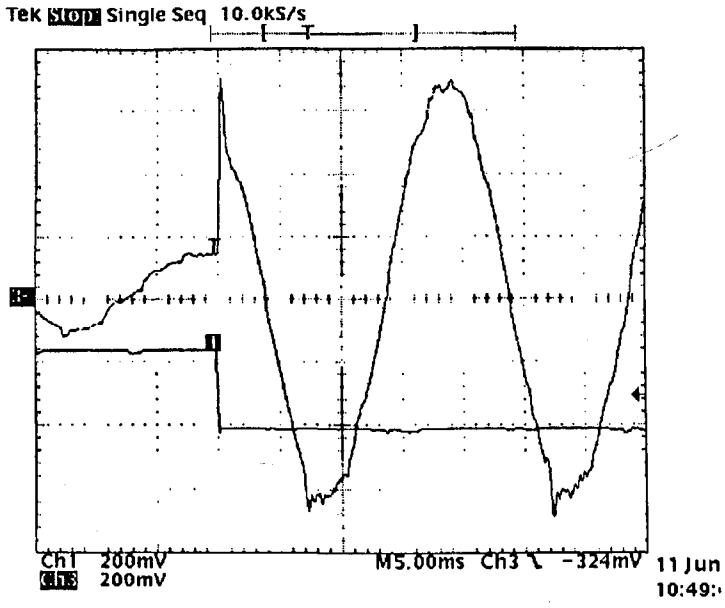

Figure 4.59 – Step Change in Demand for Damped Input Filter

Upper Trace : AC Input Current 2A/div

Lower Trace : Demand Signal 2V/div

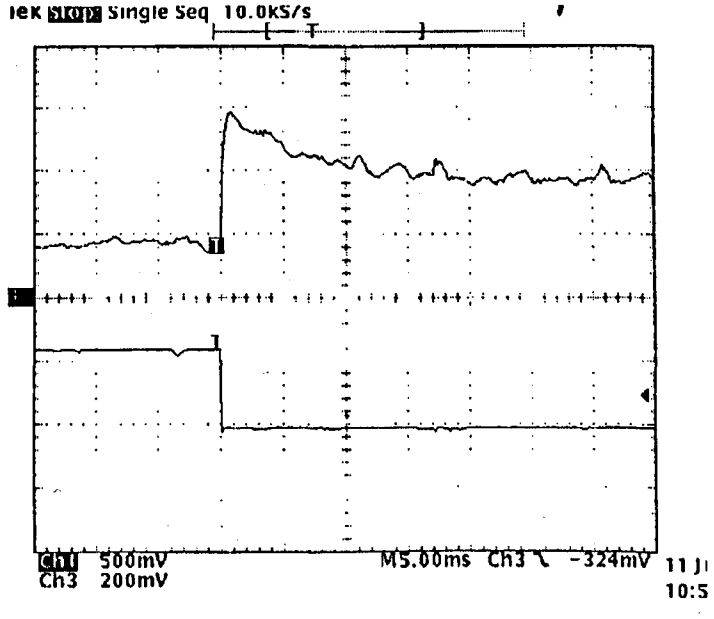

Figure 4.60 – Step Change in Demand for Damped Input Filter

Upper Trace : DC Inductor Current 5A/div

Lower Trace : Demand Signal 2V/div

The switching simulation was modified to run with the damping components. The three-phase supply inductance and damping components have the same state-space representation as the input filter in Figure 4.4. The overall system in Figure 4.61 has two cascaded input filters to represent the supply inductance and damping components

and the input filter. Note the use of the memory block to break the algebraic loop. (N.B. Algebraic loops increase the simulation run-time). The supply and damping components block is shown in Figure 4.62. The text M-file is given in Appendix A14.

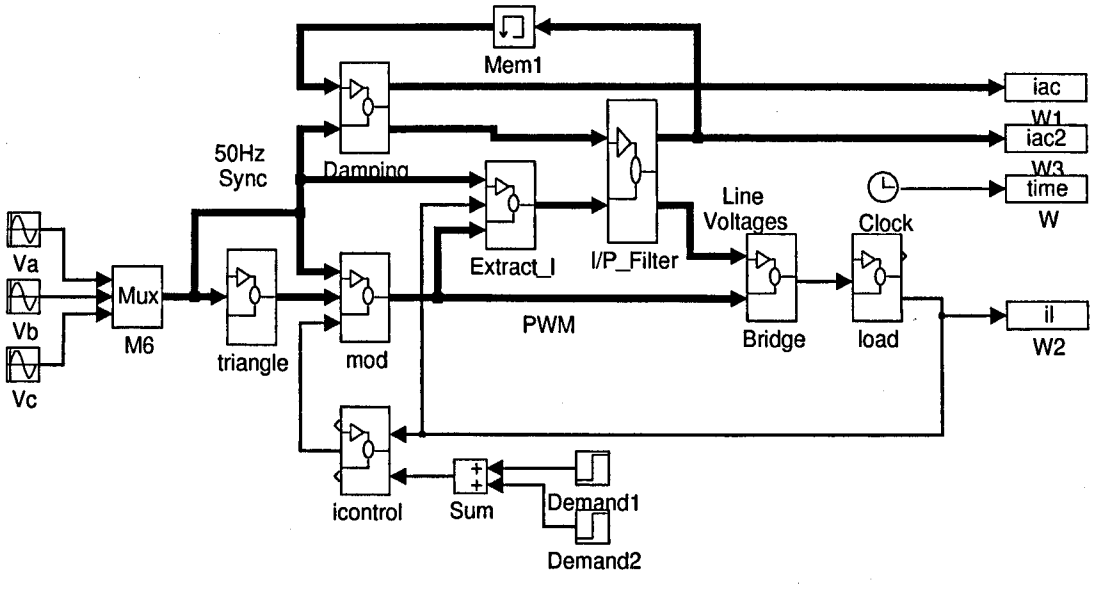

Figure 4.61 – Switching Simulation with Input Inductance and Damping Components

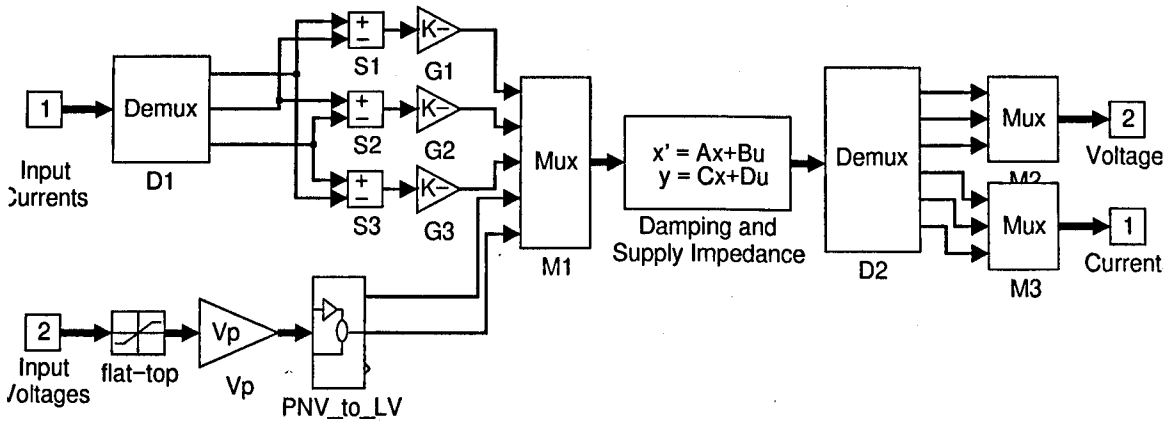

Figure 4.62 – Supply Inductance and Damping Components Building Block

The simulation results are shown in Figures 4.63, 4.64 and 4.65.

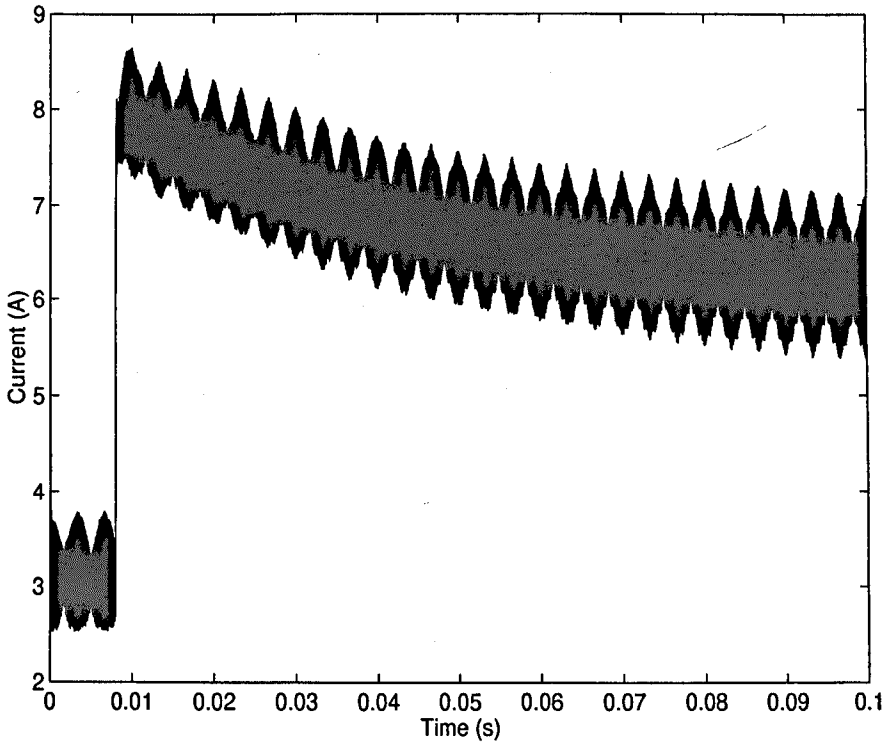

Figure 4.63 – DC Current Step Response with Damped Input Filter

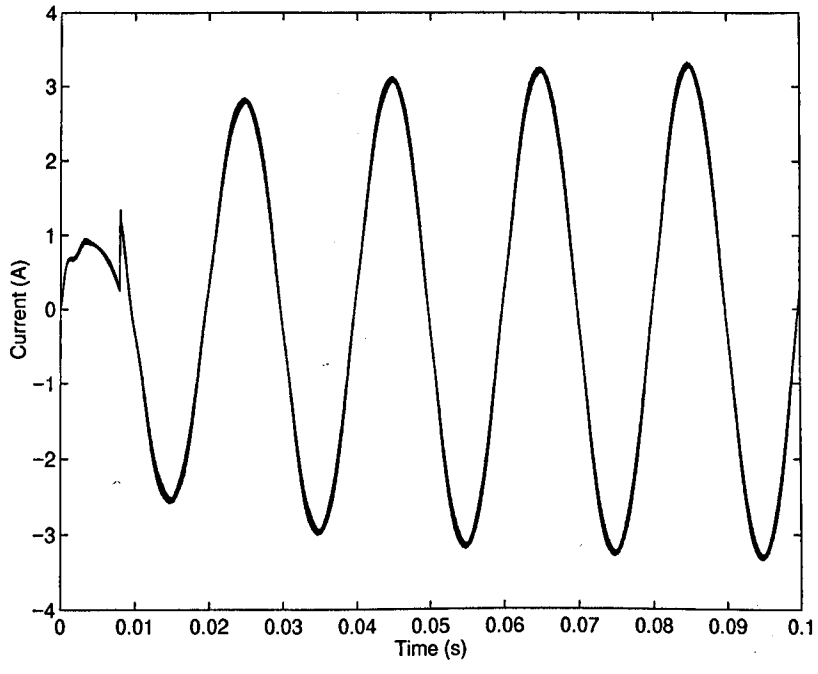

Figure 4.64 – Input AC Current Upstream of Damping Components

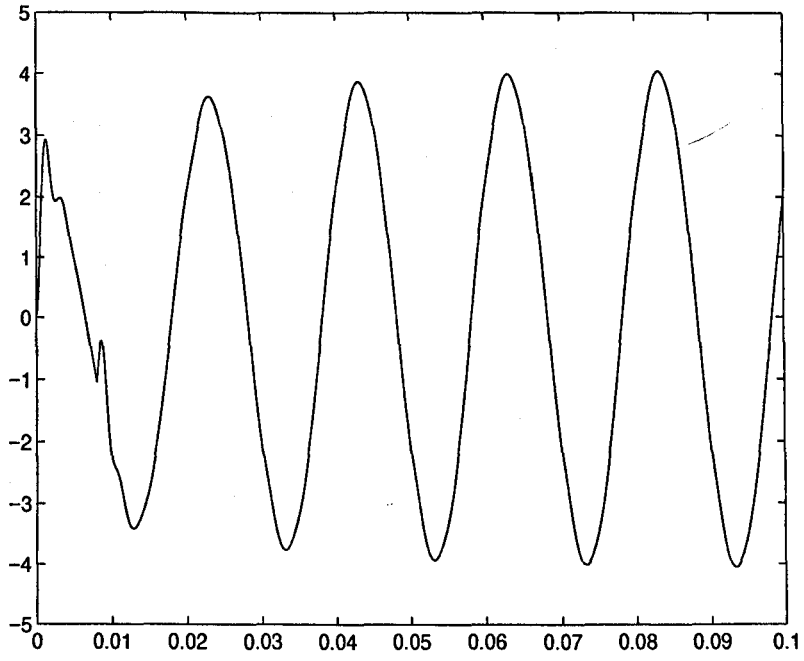

Figure 4.65 – Input AC Current Downstream of Damping Components

4.10 Robustness of Damping to Changes in Supply Inductance

The input supply inductance will change from supply system to supply system. The capacitor-plus-resistor method of damping was investigated using the switching model to see if it still adequately damps the system when the input inductance varies. The system is more sensitive to increases in L_s than to decreases. L_s can be decreased by better than a factor of twenty before the system oscillates during step changes, whereas increasing L_s by more than a factor of two results in oscillations during step changes in demand. There is scope for more work to be done on this subject, in particular to look at more advanced control schemes, (e.g. sliding-mode control) that exhibit greater robustness to changes in L_s.

4.11 Conclusions

A switching model has been developed that shows good agreement with the practical test rig. This model can be used to obtain small-signal frequency responses which predict the converter's behaviour with or without an input filter. The input filter and supply inductances were found to be of critical importance when the feedback loops are being designed. A dc-dc converter equivalent model of the three-phase ac-dc converter was developed. This model has the advantages of fast simulation time and ease of finding the frequency responses using the software's built-in linearisation functions. The frequency responses were found to be in agreement with those of the switching simulation. Four benefits are derived from using an average current-mode controller for the converter. These are; **(i)** damping of the dc output filter, **(ii)** reduction of the ac and dc-side converter current harmonics caused by supply voltage distortion, **(iii)** ability to reduce steady-state current sharing error for paralleled converters driving the same load and **(iv)** ease of implementation of an output over-current limit. The main disadvantage of this controller is that it can result in unstable input filter oscillations if the impedance criterion is broken. The input filter should be damped and if the impedance criterion is met the converter becomes straightforward to stabilise.

4.12 References

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CHAPTER 5 – Parallel Converter Operation

5.1 Introduction

The parallel connection of current-fed converters to drive a common load has already been applied in a number of different situations. Paralleling of converters to drive a load offers various advantages, such as being able to adopt a modular approach whereby extra converters are added into the system to boost the power output if the load increases, without the need to purchase a completely new power supply system. An increase in reliability of the overall power supply can be expected, because if one module fails, the others can still deliver power to the load. Another advantage of parallel operation is ripple current reduction on both the dc and ac sides of the converter, leading to lower filtering requirements and lower ripple current losses. The ripple current reduction is achieved by interleaving the PWM schemes of the converters so that they operate $2\pi/n_c$ radians out of phase with each other, where n_c is the number of converters paralleled. Thus, the effective switching frequency seen by the reactive components is raised to $n_c f_s$ kHz, where each converter is still switching at f_s kHz. A disadvantage of parallel converter operation is increased cost; $n_c=1$ converters would be cheaper to use to power a load, rather than $n_c>1$ converters.

Parallel operation of ac-dc single-phase boost converters using a hysteresis control method has been applied [5.1]. It had the advantage of simple control and a spread of switching frequencies, each of lower magnitude compared to fixed switching frequency schemes. Three-phase, single switch, ac-dc unity power factor boost converters were paralleled [5.2] with similar advantages. These converters operated in discontinuous current conduction mode, where interleaving also reduced the peak current stress seen by the IGBT switches.

5.2 Parallel Operation of the Three-Switch Converters

Converters' Connectivity

Figure 5.1 shows the parallel connection of two, three-switch converter stages, sharing the same input filter and dc output capacitor [5.3].

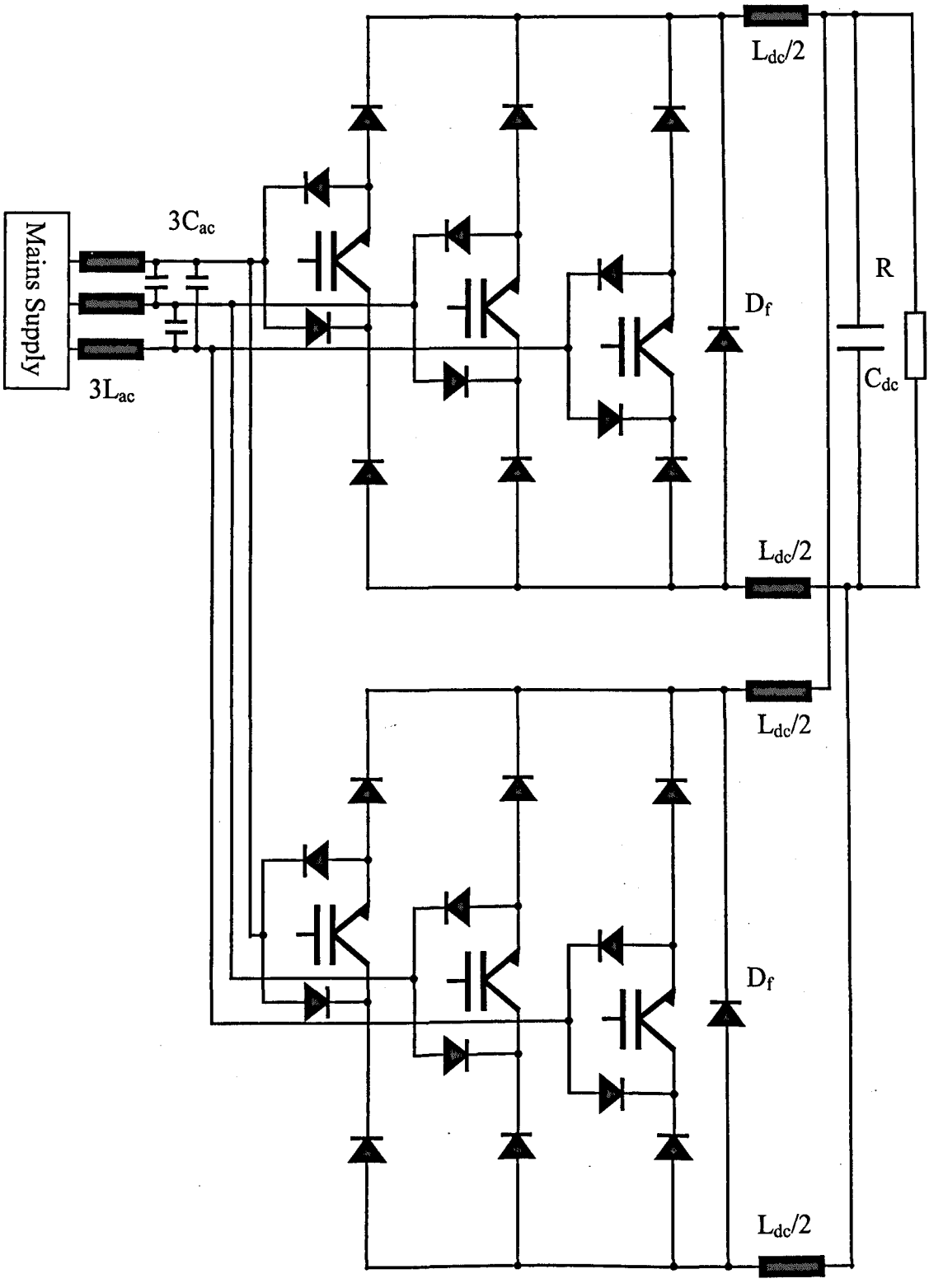

Figure 5.1 – Paralleled Three Phase AC-DC Step Down Converters

Four dc-side inductors are necessary for correct operation, so as to isolate each bridge's output voltage from the other. Compared to six-switch paralleled boost converters [5.4] the three-switch paralleled step-down converters have the advantage of no inter-bridge currents. This is because the three-switch step-down converters supply the load through blocking diodes which prevent the inter-bridge currents from flowing. (Interbridge currents are those currents that flow from one input phase voltage via both converters to another input phase voltage without passing through the load).

Current Control

Two average-mode current control loops are needed, one for each converter, located in the high-side dc inductor current paths. Two analogue PI current controllers and two ADCs are used and the resulting values of modulation depths for each converter are fed to the Xilinx™ FPGA. The FPGA generates two sets of three CAPWM signals to drive the converters' IGBT gates. The CAPWM signals for each converter are interleaved so as to be 180° out of phase with each other. No additional look-up tables are stored, as the second converter accesses the same pulse durations as the first, only at different times. Figure 5.2 gives the overall paralleled converters scheme.

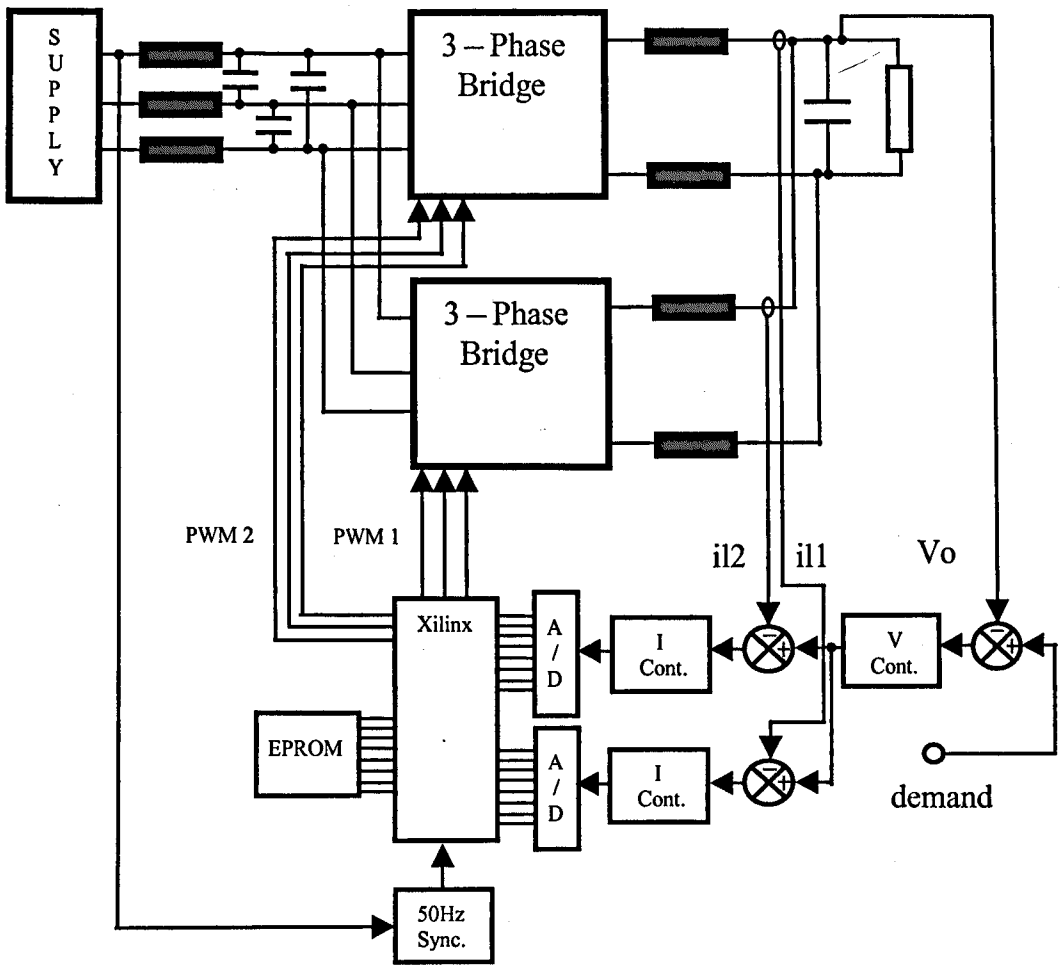

Figure 5.2 – Paralleled Converters System Block Diagram

Figure 5.3 shows the production of the PWM pulses over the 0-60° period for the two paralleled and interleaved converters. The total current drawn from Phase A will be the sum of the currents represented by PWM A1+PWM A2. Likewise, the sum of PWM B1+PWM B2 gives the total Phase B current. The total current flowing into Phase C is given by PWM A1+PWM A2+PWM B1+PWM B2. The minimum ripple current frequency is now $2f_s$ instead of f_s, as in the case when one converter is used. The effect on the input current harmonics of interleaving is discussed in Section 3.3.3.

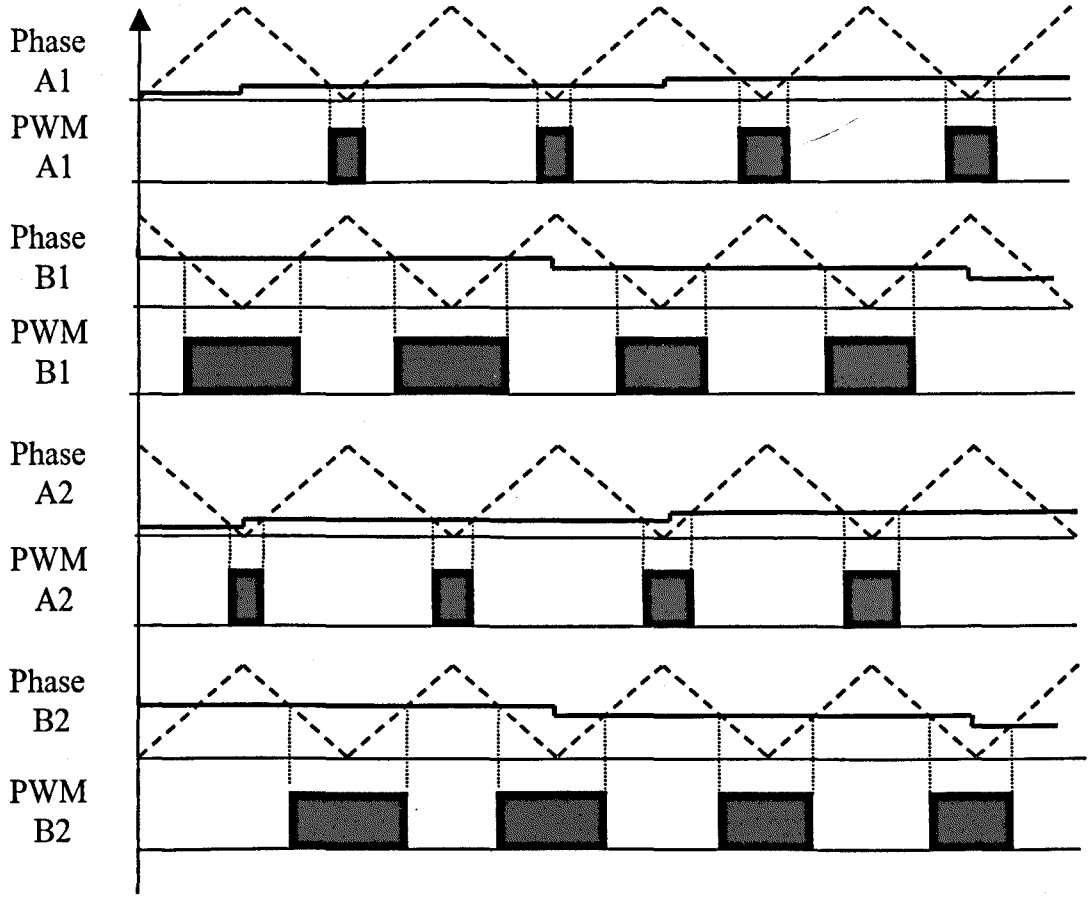

Figure 5.3 – Production of PWM for Dual Converters

5.3 PSpice™ Simulation

PSpice™ is used to simulate the dual converter scheme, Figures 5.4 to 5.10. The PSpice™ PWM signal files are produced by using Appendix A2 and following the instructions to generate the six PWM files needed. The PSpice™ circuit file is given in Appendix A15. Note the reduction in ripple current in the inductors connected to a phase being held on for 60°. This is due to the current from the two switching phases of both converters dividing itself between the two converters' return paths. This will have the beneficial effect of reducing the overall dc inductor core and winding losses.

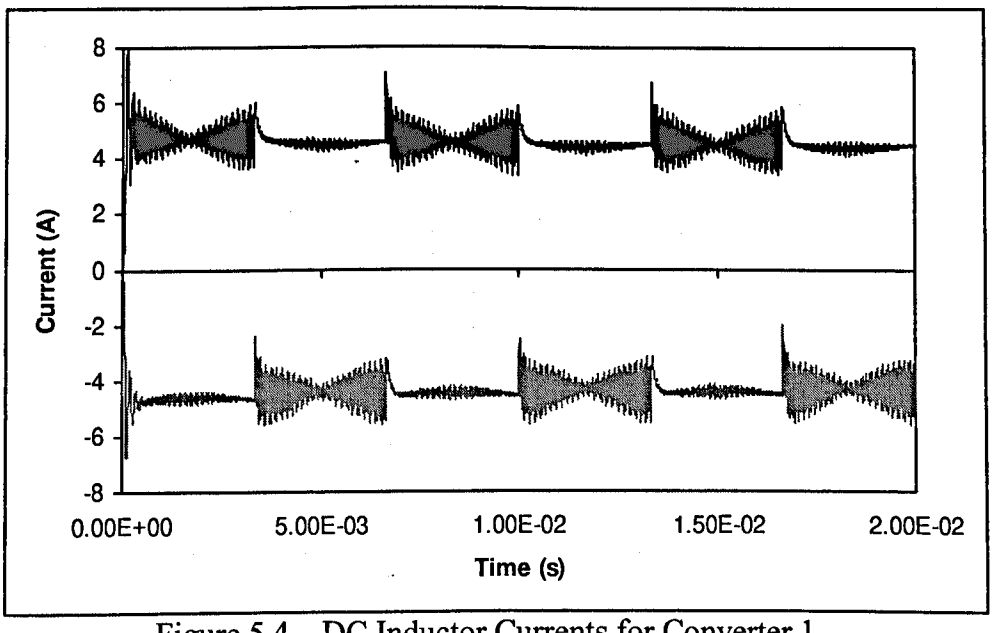

Figure 5.4 – DC Inductor Currents for Converter 1

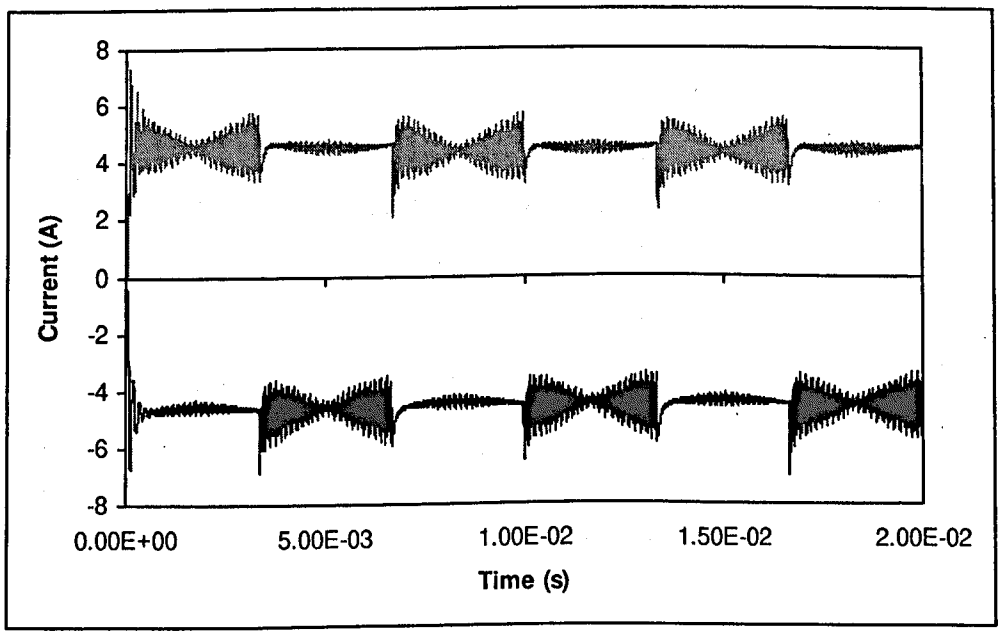

Figure 5.5 – DC Inductor Currents for Converter 2

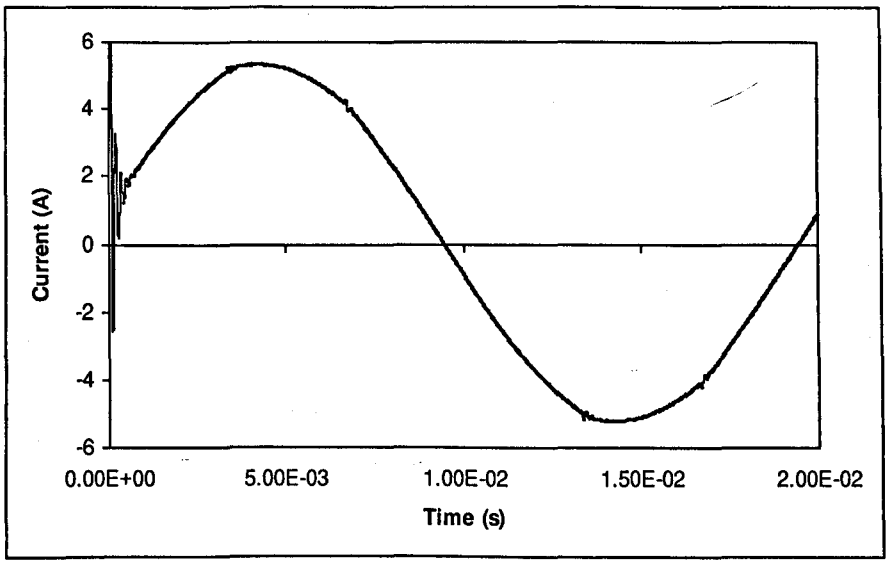

Figure 5.6 – AC Input Current

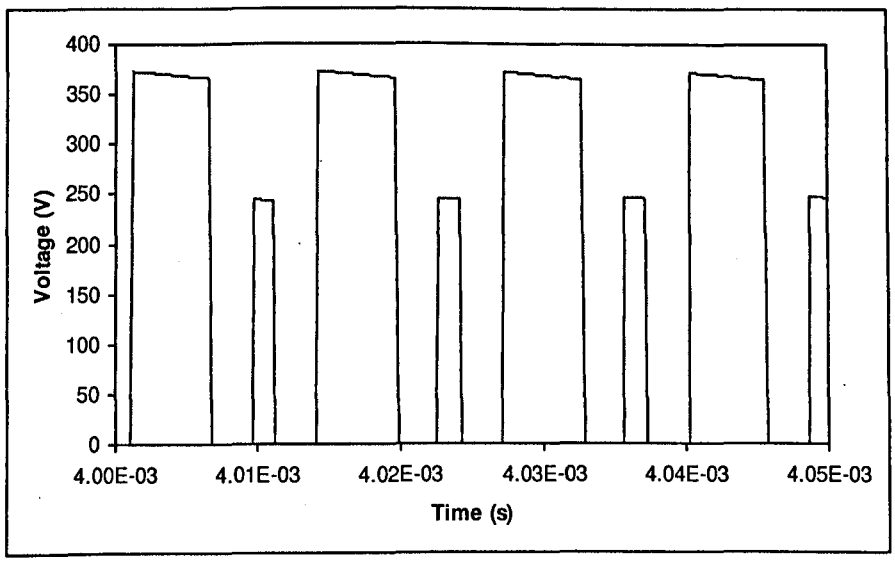

Figure 5.7 – Converter 1 Bridge Output Voltage

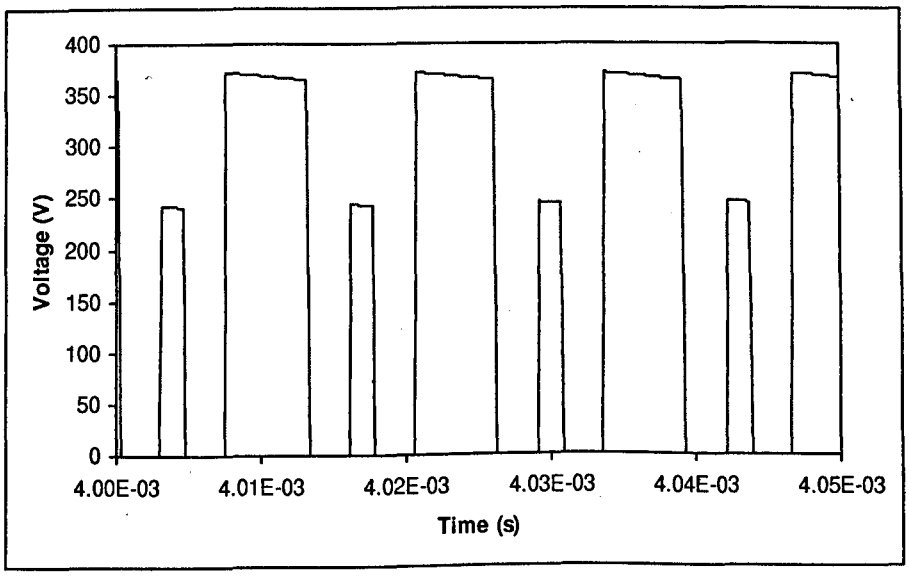

Figure 5.8 – Converter 2 Bridge Output Voltage

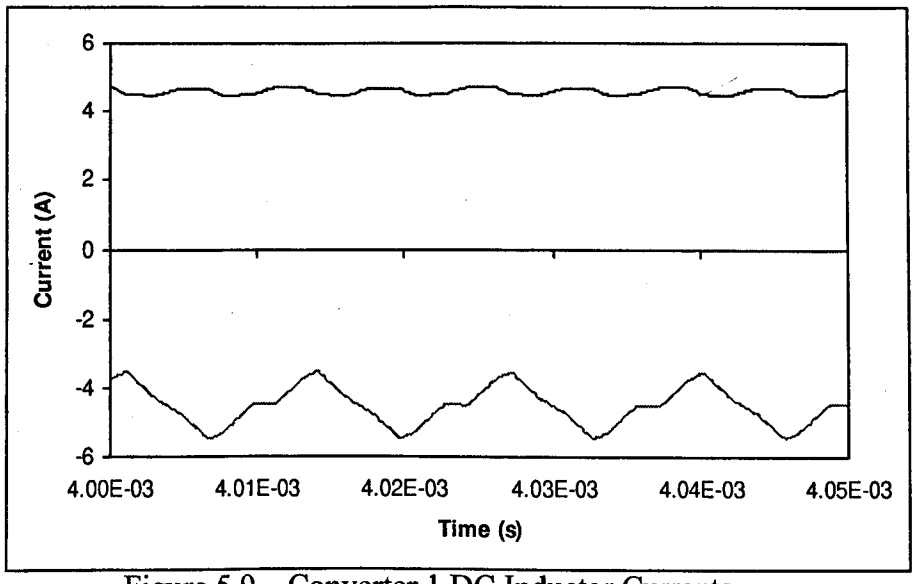

Figure 5.9 – Converter 1 DC Inductor Currents

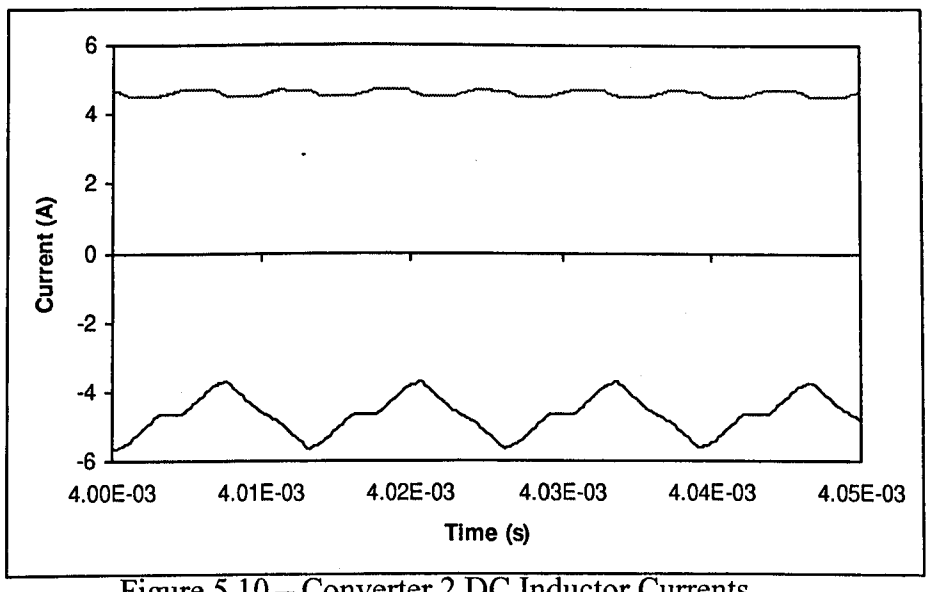

Figure 5.10 – Converter 2 DC Inductor Currents

5.4 Practical Results

DC inductor and ac input current waveforms are shown in Figures 5.11 and 5.12 to prove the operation.

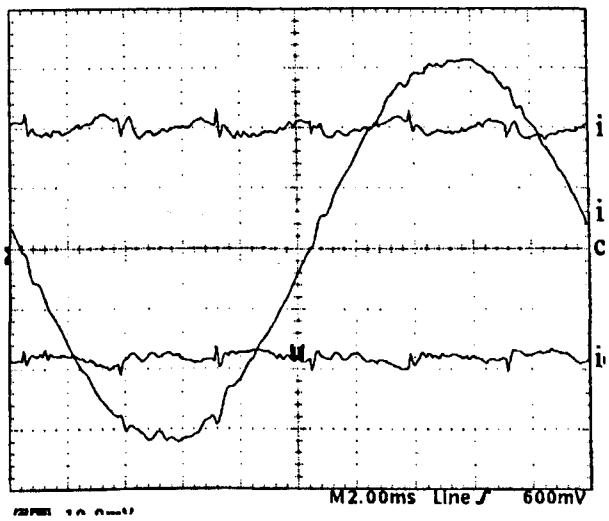

Figure 5.11 – Dual Converter Currents

Upper Trace : Average DC Inductor Current for Converter 1, 2A/div

Middle Trace : Average Input AC Current, 2A/div

Lower Trace : Average DC Inductor Current for Converter 2, 2A/div

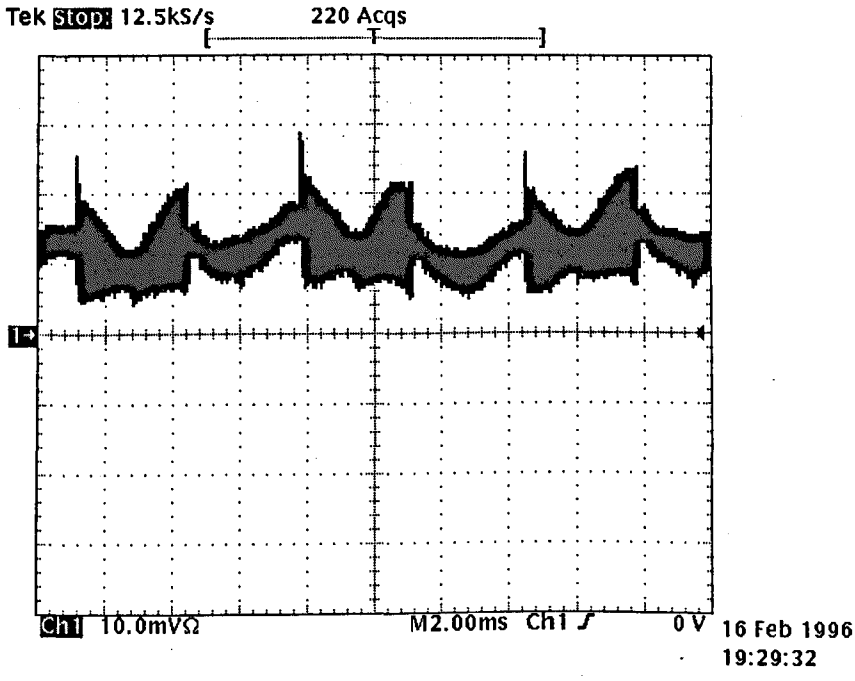

Figure 5.12 – DC Inductor Current, 5A/div

5.5 Conclusions

Parallel operation of two current-controlled converters using an interleaved PWM scheme has been proved. Interleaving eliminates the switching harmonics around the switching frequency, f_s, and will reduce the losses in the dc inductors. Paralleling of the three-switch converters does not suffer from interbridge currents as does the six-switch paralleled boost converters scheme.

5.6 References

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CHAPTER 6 – A Soft-Switching PWM Scheme (SSPWM)

6.1 Introduction

The main reasons for using soft-switching are;

(i) A reduction in switching loss and hence an increase in switching frequency is possible or, if the switching frequency is unchanged, then a cooler-running power supply can be achieved.

(ii) A reduction in electromagnetic interferance (EMI) due to the elimination of fast voltage and/or fast current edges by using sinusoidal or part-sinusoidal voltage or current pulses.

There are disadvantages associated with soft-switching and these are contained in the implementation, which requires additional components such as inductors and capacitors to be added in order to achieve resonance. Because sinusoidally shaped voltages and/or currents are used, the peak voltage and/or current stress experienced by the semiconductor devices (in the on-state) is higher compared to hard-switched converters and so they need to be accordingly uprated. Higher peak currents and/or voltages will increase the losses in the semiconductor devices and also the loss due to the winding resistance of the resonant inductor. Soft-switching decreases the overall losses, but not by as much as might be first thought. Resonant type converters are used mainly in military or telecommunications applications, where a tighter EMI specification is demanded, or where higher power density is required.

Another type of soft-switching circuit is non-resonant and uses a MOSFET in parallel with the main IGBT power device [6.1]. Turn-off of the IGBT occurs just before turn-on of the MOSFET, so that current is transferred from the former to the latter. The IGBT turns off under zero-current conditions and the MOSFET turns off a short time later. Above 600V, IGBTs switch just as fast as MOSFETs and so the method only applies to devices rated below 600V. The soft-switching PWM scheme (SSPWM) is

related to this type of soft-switching topology in that one device is used to assist the other at the switching instants, but it does not require the additional components as it uses the existing power devices of the converter.

6.2 Theory of Operation

Introduction

Compared to the centre-aligned PWM scheme (CAPWM) SSPWM [6.2] exhibits both zero current, zero voltage and reduced voltage stress switching behaviour. Unlike other soft-switching converter schemes, this converter performs soft-switching without any additional hardware components, but rather only through a change to the PWM scheme.

Comparison between CAPWM and SSPWM

CAPWM

The converter has 60° symmetry, so considering just one sextant is sufficient to prove the operation. The 0-60° sextant and a single switching cycle of CAPWM are shown in Figure 6.1, where phases V_a and V_b are switching and phase V_c remains held on.

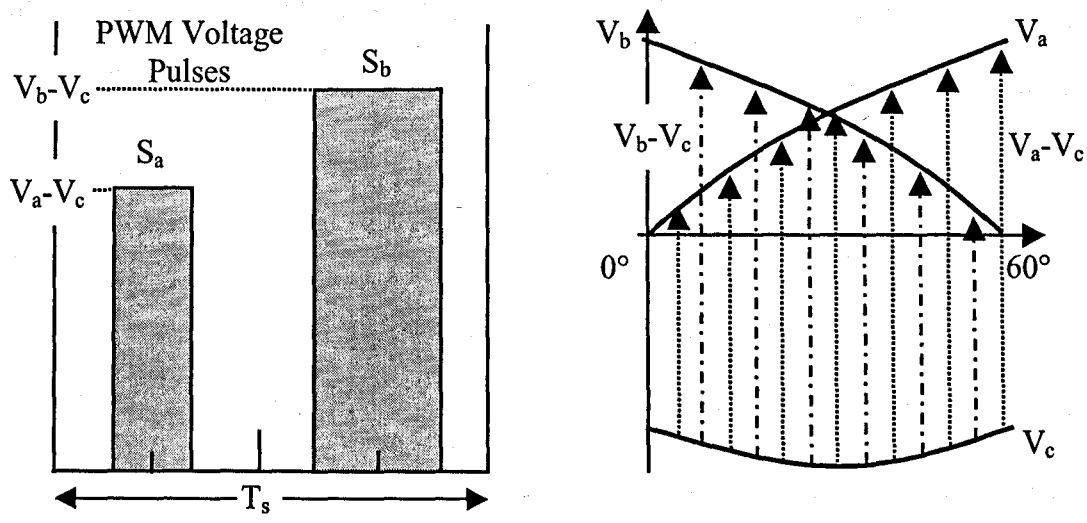


Figure 6.1 – Switches S_a and S_b Voltage Stresses During Turn-On and Turn-Off for CAPWM

The variable voltage stress applied to switch S_a during the sextant is V_a-V_c. For an infinite dc inductor, the current through each switch over the 0-60° cycle is constant, Figure 6.2.

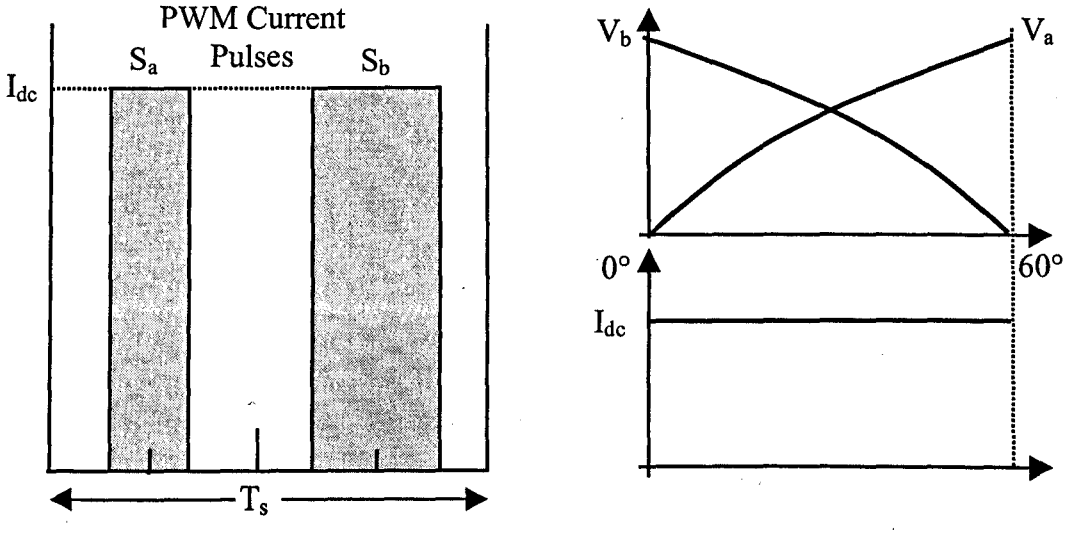


Figure 6.2 – Switches S_a and S_b Current Stresses During Turn-On and Turn-Off for CAPWM

SSPWM

Figure 6.3 shows that SSPWM shifts the PWM pulses together so that the falling edge of the first pulse touches the rising edge of the second. The first pulse is then extended in time by an over-lap, T_o, so that the on-time of the first switch overlaps with that of the second. Furthermore, the lowest potential voltage phase forms the first PWM

pulse and the higher potential phase the second. There is therefore a change-over point every 30°, when the phase with the previously higher potential becomes the lower potential and the phase with the lower potential becomes the phase with the higher potential. For the 0-30° period, S_a remains on for T_o seconds while S_b turns on. S_b therefore sees a reduced voltage across it, i.e. V_b-V_a (instead of V_b-V_c as in the CAPWM case). For the 30-60° period, S_b remains on while S_a turns on and S_a has V_a-V_b across it (instead of V_a-V_c as in the CAPWM case). The voltages across S_a for the 0-30° period and across S_b for the 30-60° period are zero in the case of SSPWM.

N.B. The same volt-seconds are applied to the load per switching cycle by using SSPWM compared with CAPWM. Therefore, the linear input to output voltage relationship and sinusoidal input current features are retained.

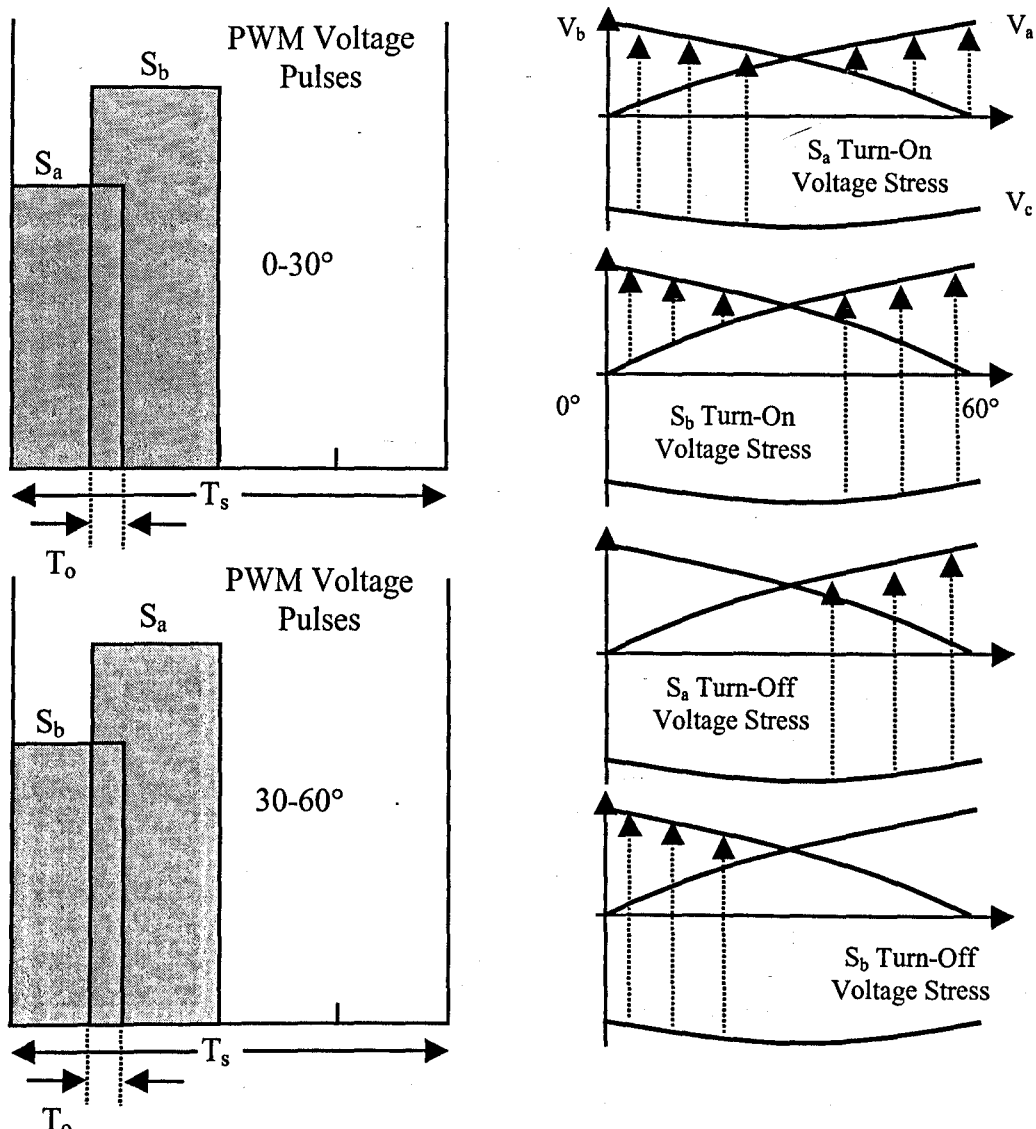


Figure 6.3 – Switches S_a and S_b Voltage Stresses for SSPWM

Similarly, Figure 6.4 shows the effect soft-switching has on the current through the devices. For the period 0-30°, S_a experiences zero current turn-off. This is because S_b turned on T_o seconds before S_a turned off and so the current naturally commutates from S_a (the phase with lower potential) into S_b (the phase with higher potential). For the 30-60° period, S_a has the higher potential and so current commutates from S_b into S_a before S_b turns off, so giving zero current switching for S_b.

An additional advantage of SSPWM is that the number of freewheel periods is reduced from two to one, in comparing CAPWM with SSPWM. The SSPWM freewheel diode therefore has one half the switching losses of the CAPWM freewheel diode.

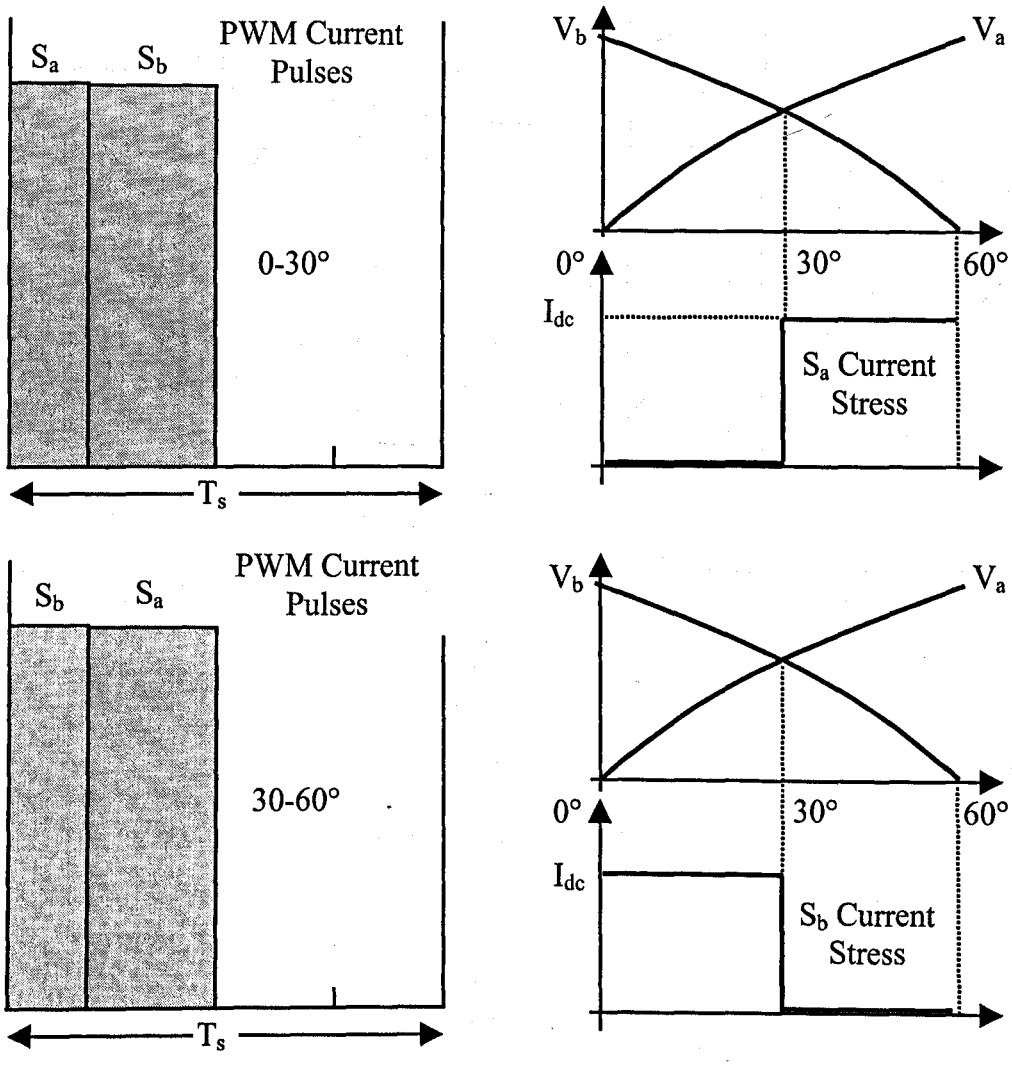


Figure 6.4 – Switches S_a and S_b Current Stresses for SSPWM

Implementation of SSPWM Scheme

The simplest way to implement SSPWM is to use count-up and count-down saw-tooth carriers and compare them with two sinusoidal modulating functions, Figure 6.5. Additional hardware and software is used to extend the leading pulse by T_o seconds to create the overlap. Note the presence of a glitch at the 30° point where the change-over in carriers is made. This glitch will give rise to some distortion in the input current waveform.

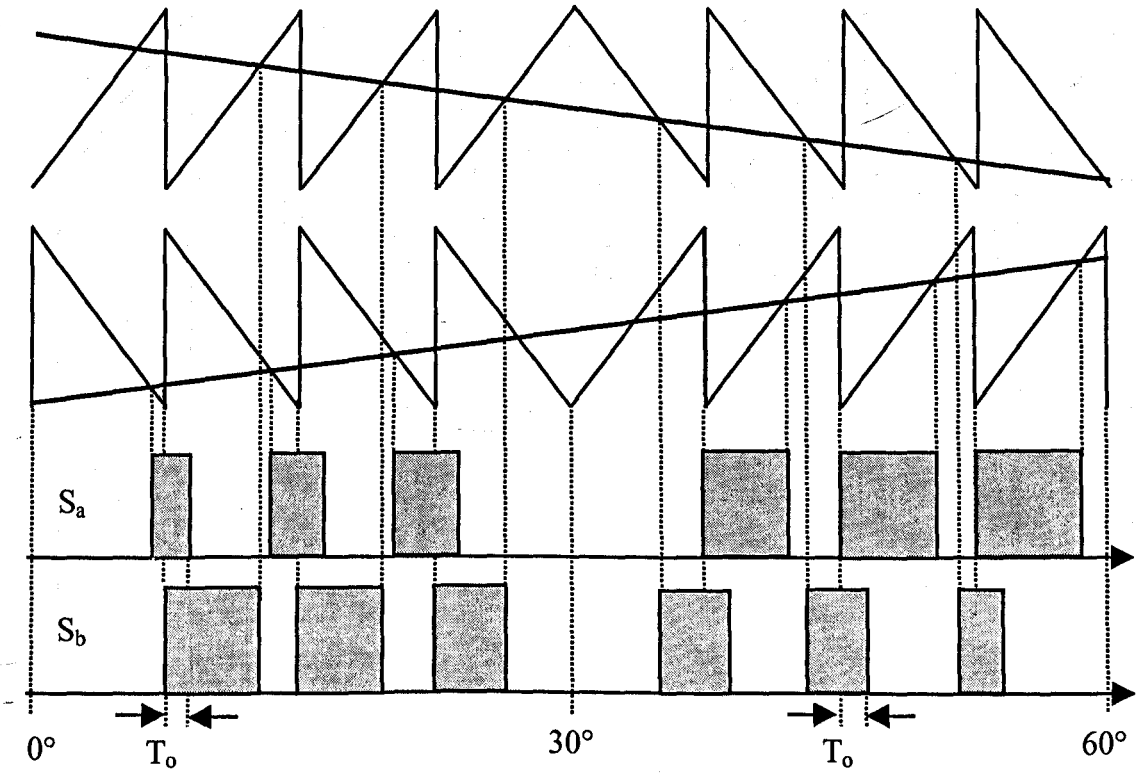


Figure 6.5 – SSPWM Sawtooth Modulation Scheme

Modified SSPWM (MSSPWM) Scheme

A way to overcome the distortion around the 30° point is to not change-over carriers, Figure 6.6. After the 30° point, the highest voltage phase is switching first and remains on for T_o seconds after the lower voltage phase has turned on. Thus the lower voltage phase's switch will turn on with no current in it. Current will only flow in this switch when the higher potential phase's switch turns off. The higher potential phase's switch will turn off with a reduced voltage across it. One possible disadvantage with this method is that when current suddenly starts to flow in the lower potential switch due to the higher potential switch being turned off, it may result in the lower potential switch coming out of its zero-voltage on-state and so give a delayed turn-on switching loss.

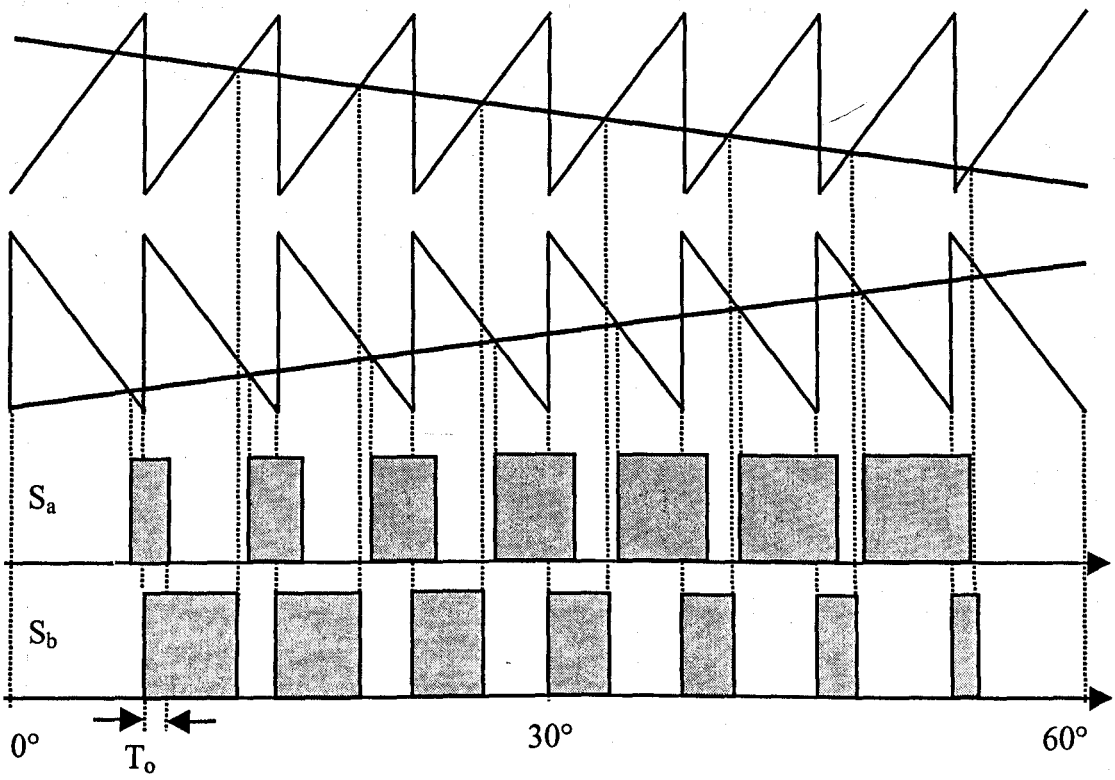


Figure 6.6 – MSSPWM Sawtooth Modulation Scheme

The scheme used for practical purposes is SSPWM. In practice, because of the inability of the μC to generate a count-down type sawtooth carrier, two count-up sawtooth carriers are used and some manipulation carried out to get the correct pulse shapes and positions, Figure 6.15.

Table 6.1 summarises the different switching losses for CAPWM, whilst Table 6.2 shows the changes relative to Table 6.1 that SSPWM makes on the switching losses.

Switch	0-30°				30-60°			
	Voltage		Current		Voltage		Current	
	Turn On	Turn Off	Turn On	Turn Off	Turn On	Turn Off	Turn On	Turn Off
S_a	V_a-V_c	V_a-V_c	I_{dc}	I_{dc}	V_a-V_c	V_a-V_c	I_{dc}	I_{dc}
S_b	V_b-V_c	V_b-V_c	I_{dc}	I_{dc}	V_b-V_c	V_b-V_c	I_{dc}	I_{dc}

Table 6.1 – Switching Voltages and Currents for CAPWM

Switch	0-30°				30-60°			
	Voltage		Current		Voltage		Current	
	Turn On	Turn Off	Turn On	Turn Off	Turn On	Turn Off	Turn On	Turn Off
S_a	-	0	-	0	$\downarrow V_a$-V_b	-	-	-
S_b	$\downarrow V_b$-V_a	-	-	-	-	0	-	0

Table 6.2 – Changes in Switching Losses for SSPWM Relative to CAPWM

- = no change, $\downarrow$ = decrease and 0 = zero

6.3 SSPWM PSpice™ Simulation

A PSpice™ simulation was used to assess the viability of SSPWM. The C-programme used was a modified version of the programme used to generate the PWM pulses for CAPWM and is given in Appendix A16. The results, Figures 6.7 to 6.14, show that SSPWM works for the converter. The dc-side ripple inductor current, Figure 6.8, is constant and at the maximum value of the CAPWM scheme. The dc inductor used for CAPWM can also be used be used for SSPWM and the maximum ripple

current will be the same. Comparing Figures 6.9 and 6.10 shows the small amount of overlap (0.4μs) present on the gate-drive pulse of S_b, which for the 30-60° interval, is the leading, narrow-width pulse. Figures 6.12 and 6.13 show that S_a turns on when the voltage across it has dropped to V_a-V_b, i.e. reduced voltage turn-on. Figures 6.11 and 6.14 show that S_b turns off with zero voltage across it. Figures 6.9 and 6.11 show that S_b turns off with zero current flowing through it.

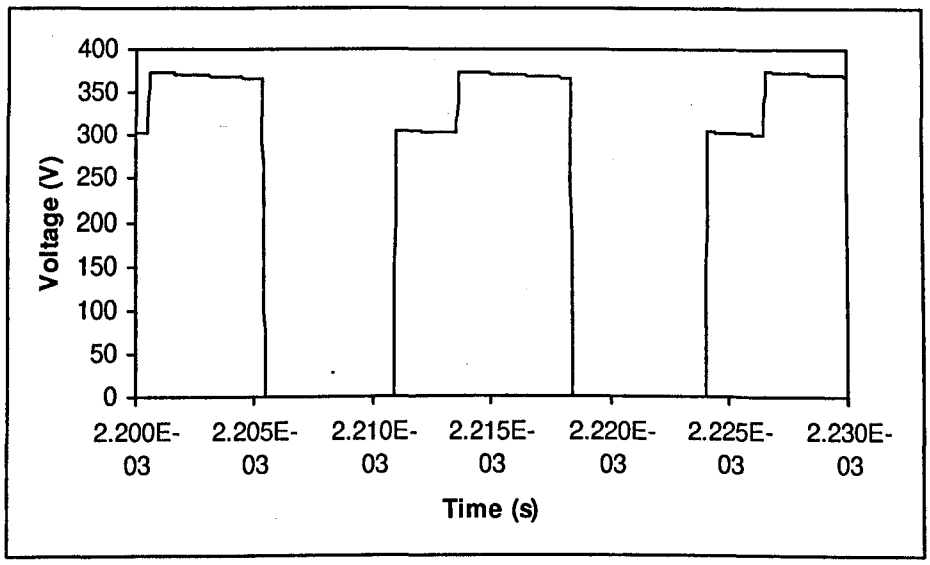


Figure 6.7 – Bridge Output Voltage

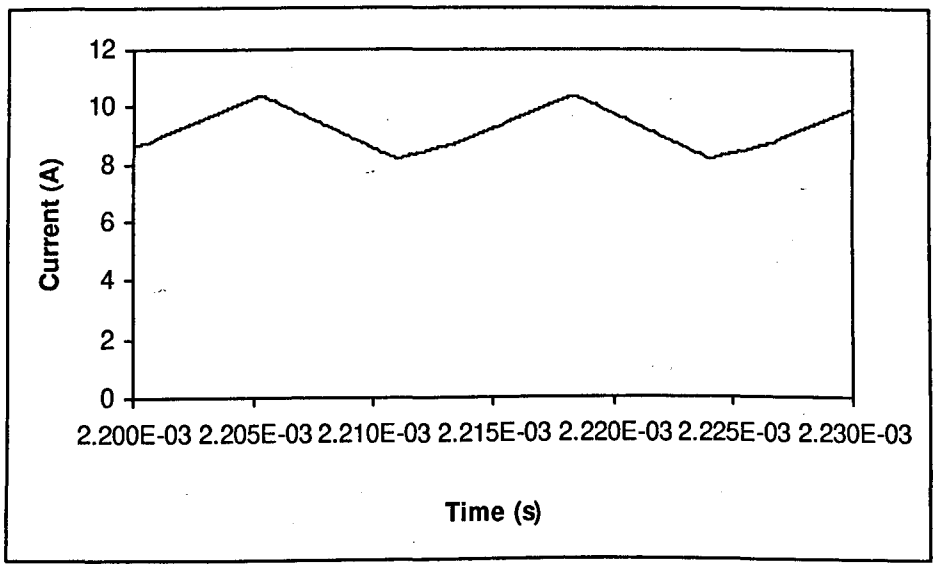


Figure 6.8 - DC Inductor Current

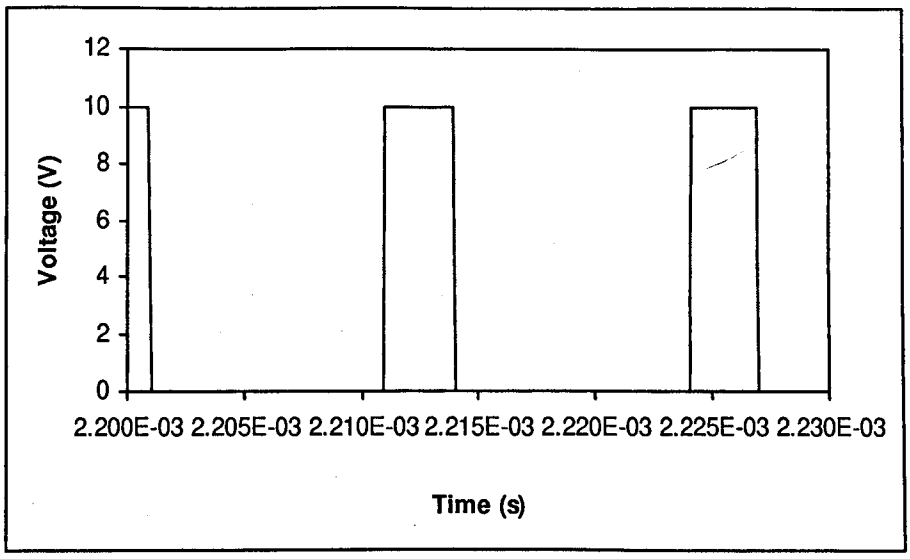


Figure 6.9 – Switch S_b Gate Drive Pulses

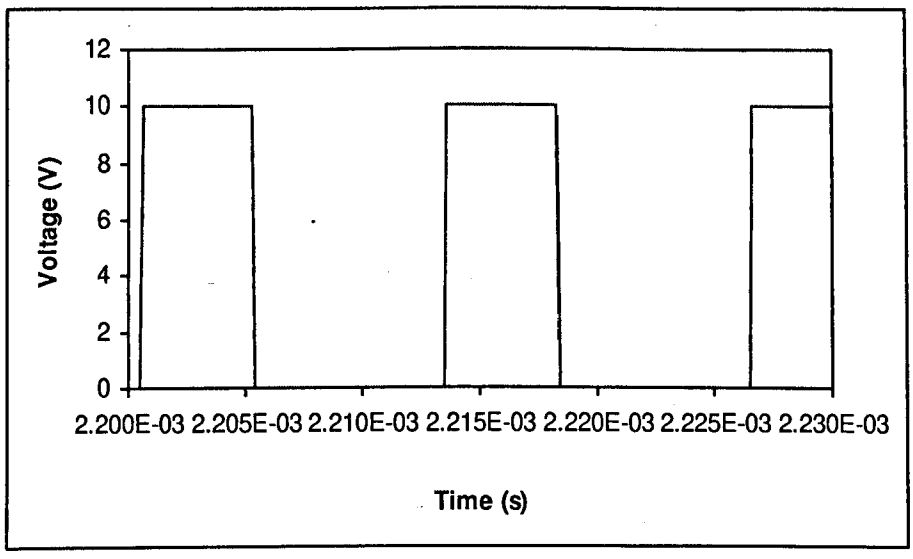


Figure 6.10 – Switch S_a Gate Drive Pulses

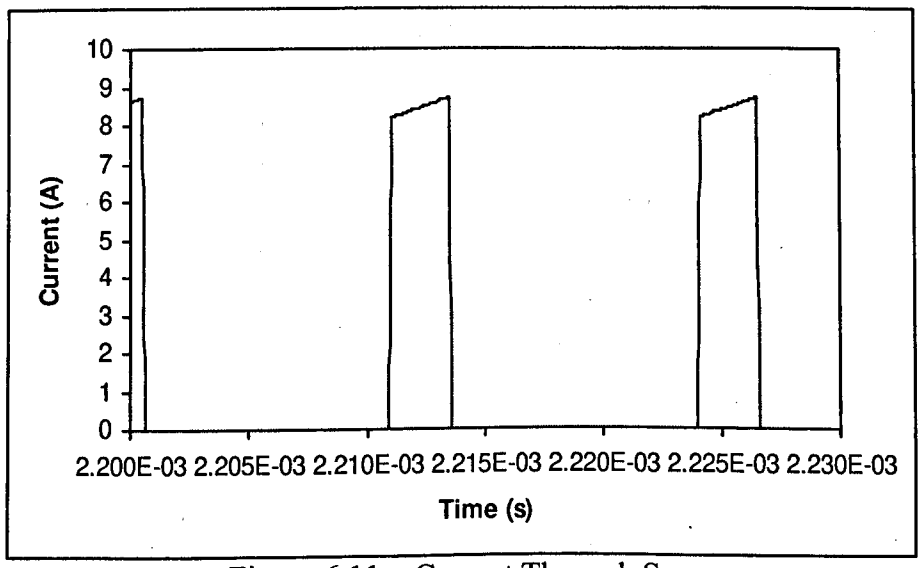


Figure 6.11 – Current Through S_b

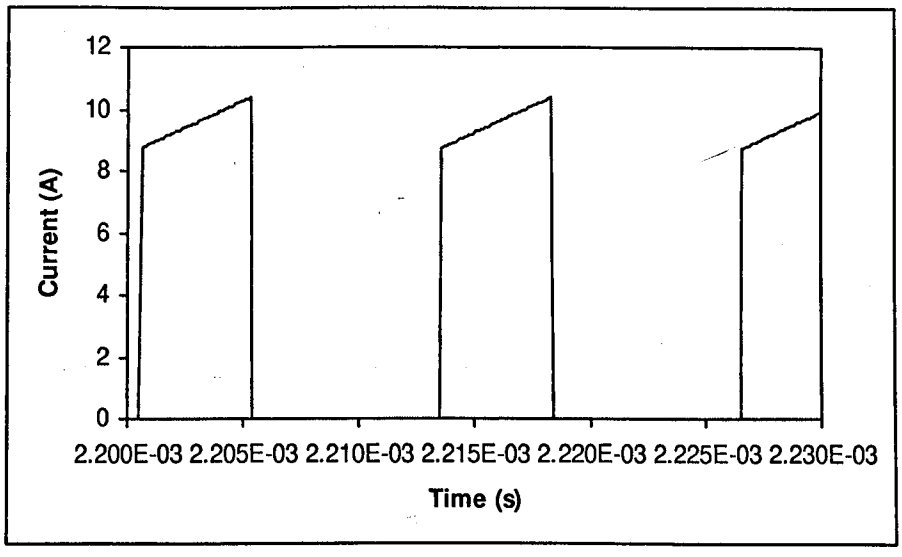


Figure 6.12 – Current Through S_a

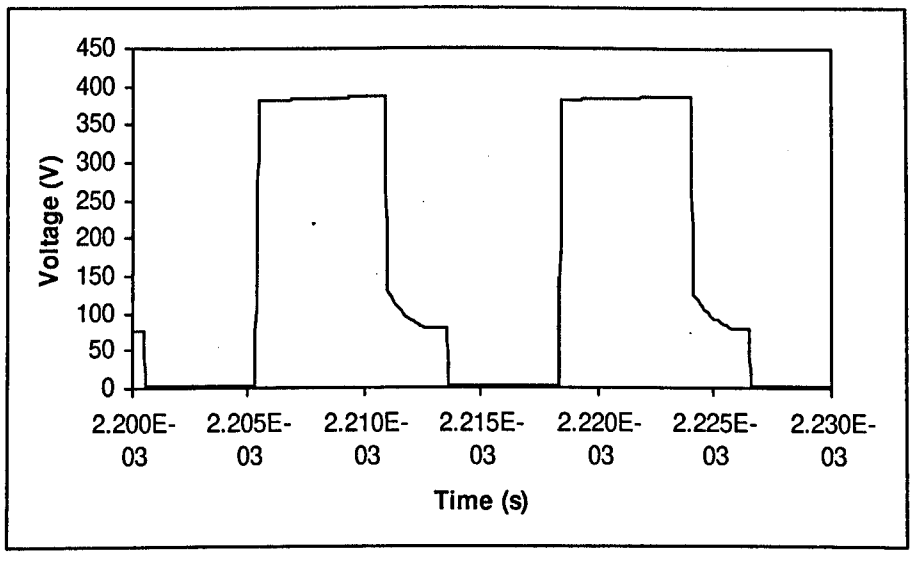


Figure 6.13 – Voltage Across S_a

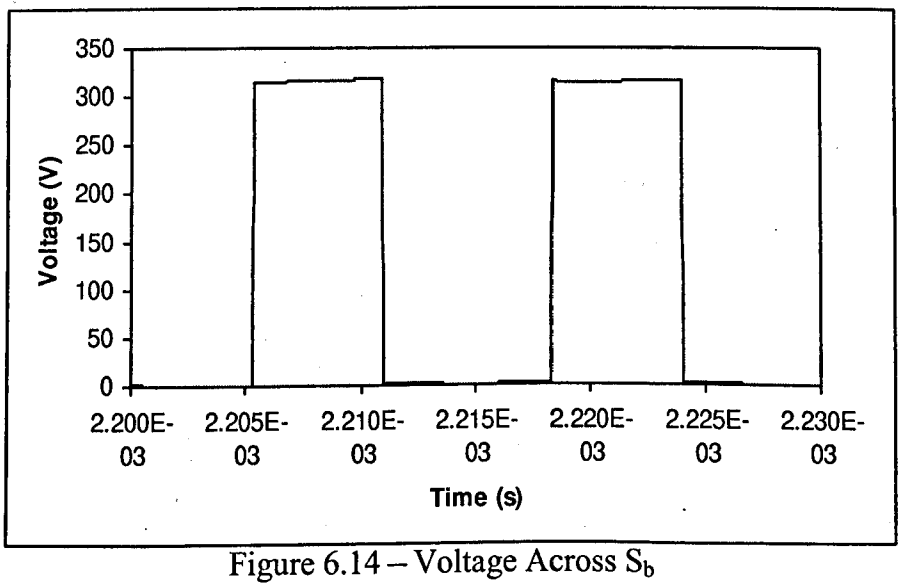


Figure 6.14 – Voltage Across S_b

6.4 Hardware and Software Implementation of SSPWM

Microcontroller Based Implementation

Recently, the distinction between digital signal processors (DSPs) and microcontrollers (μCs) has become blurred due to DSPs acquiring the sort of peripherals seen on μCs and μCs becoming faster. Implementation of SSPWM is carried out using a Siemens SABC167 μC evaluation board [6.3]. The μC has a number of features that make it suitable for use in power electronics circuits. These include; 16-channel 10-bit ADC, 4-channel dedicated PWM generation unit, 7 general purpose 16-bit timers/counters, 2*16 channel capture/compare (CAPCOM) unit and 2kB of on-board RAM. The μC is a 16-bit one, operating at a clock speed of 20MHz and can execute a 16-bit*16-bit multiplication in 0.5μs and a 32-bit/16-bit division in 1μs

The μC has to perform a number of functions in this application; generate the three-phase SSPWM signals, read-in the modulation depth and use this to select the correct look-up table values and synchronise to the nominal 50Hz mains supply.

The C167 evaluation kit contains the following; on-board 64kB RAM, serial communications port for communication with a personal computer and μC. Software includes; C-programme editor, compiler and linker, in-circuit emulator and debugger.

Programme Operation

The C-programme is listed in Appendix A17. The programme's basic operation is as follows;

(1) The variables are declared. N.B. M0 is a pointer that points to the start of the 32kB look-up data table located between 0x4000 and 0xC000 in the evaluation board's RAM memory.

(2) The input of CAPCOM 0 is fed with the externally derived mains synchronisation signal and is configured to set a flag for polling purposes

on both the falling and rising edges. This flag is used to synchronise the SSPWM to the mains.

(3) CAPCOM 23 and Timer 7 are set to generate a nominal 50Hz output from a 19.6608MHz μC clock input for use with the external phase-locked-loop (PLL). The PLL generates the μC clock signal locked to the mains supply in the same way as for the original Xilinx™ implemented CAPWM scheme. The division ratio is 19.6608MHz/50Hz=384*1024. The CAPCOM unit is clocked using the timer, which is set to produce a clock signal of 19.6608MHz/1024=19.2kHz. The CAPCOM unit is loaded with a value equivalent to 384/2 and every time that it counts up to this value, its output is toggled. Thus its output toggles at a 100Hz rate i.e. a 50Hz signal is produced.

(4) The PWM generation unit is set to produce three sawtooth carrier based PWM outputs at a nominal 78.25kHz frequency. A fourth PWM signal is generated of constant width and this output is summed with the leading SSPWM pulse to generate the overlap.

(5) The ADC is configured to read the analogue modulation depth and convert it to a binary number. The clock time of the μC is t_{cl} where $2t_{cl}$=1/20MHz. The ADC's conversion clock is set to $t_{cc}=48t_{cl}$ and the sample clock to $2t_{cc}$. A complete conversion will take $14t_{cc}+2t_{sc}+4t_{cl}=21.7\mu s$ [6.3]. This meets the requirement of the ADC to produce one reading within every two switching cycles i.e. 25.6μs.

(6) The programme waits for the first mains synchronisation pulse to arrive. The programme enters an endless loop that waits for a PWM interrupt and proceeds to execute the interrupt routine every other interrupt. Every

other interrupt is serviced as each table value is held for two switching cycles.

(7) If the interrupt routine is entered, then two variable assignments are made. These are called the "trailing" and "leading" values and contain the current look-up table values to be loaded into the PWM registers for the first and second SSPWM pulses respectively. The variable "trailing" starts at the end of the table and counts backwards, whilst "leading" starts at the beginning of the table and counts forwards. The variable "new_address" is the address of the correct table from which to extract the values and so this variable changes in steps of 128 as there are 128 values per table. The variable "i" counts through the individual table values.

(8) The interrupt routine is divided into three main "if-then" sections. These sections correspond to the periods 0-60°, 60-120° and 120-180° in the mains cycle. In turn, each of the three sections are broken down into two further "if-then" sections representing the 0-30° and 30-60°, 60-90° and 90-120° etc. periods. The 60°-wide sections change which phases are switching and which phase is held on. The 30°-wide sections decide which pulse should be leading/trailing the other according to which phase voltage is the lowest/highest.

(9) At the end of the interrupt routine, "i" is updated every second time so that the table's next values are pointed to. If the 180° point has been reached in the mains cycle ("cycle_pos=3") before the 50Hz synchronisation signal has been received, then all SSPWM signals are turned off.

(10) Monitoring of the mains synchronisation signal is done via polling rather than an interrupt as it does not matter if the synchronisation signal is late by two switching cycles. When the synchronisation signal is received, the variables are reset to point to the start of the look-up table again.

(11) If the ADC has finished a conversion, then the value produced is converted into a 7-bit number and stored in "new_address" and the conversion process started again. The 10-bit value read is stored in a 16-bit variable and converted to a 8-bit number by removing the two least-significant bits and shifting the result five places to the left.

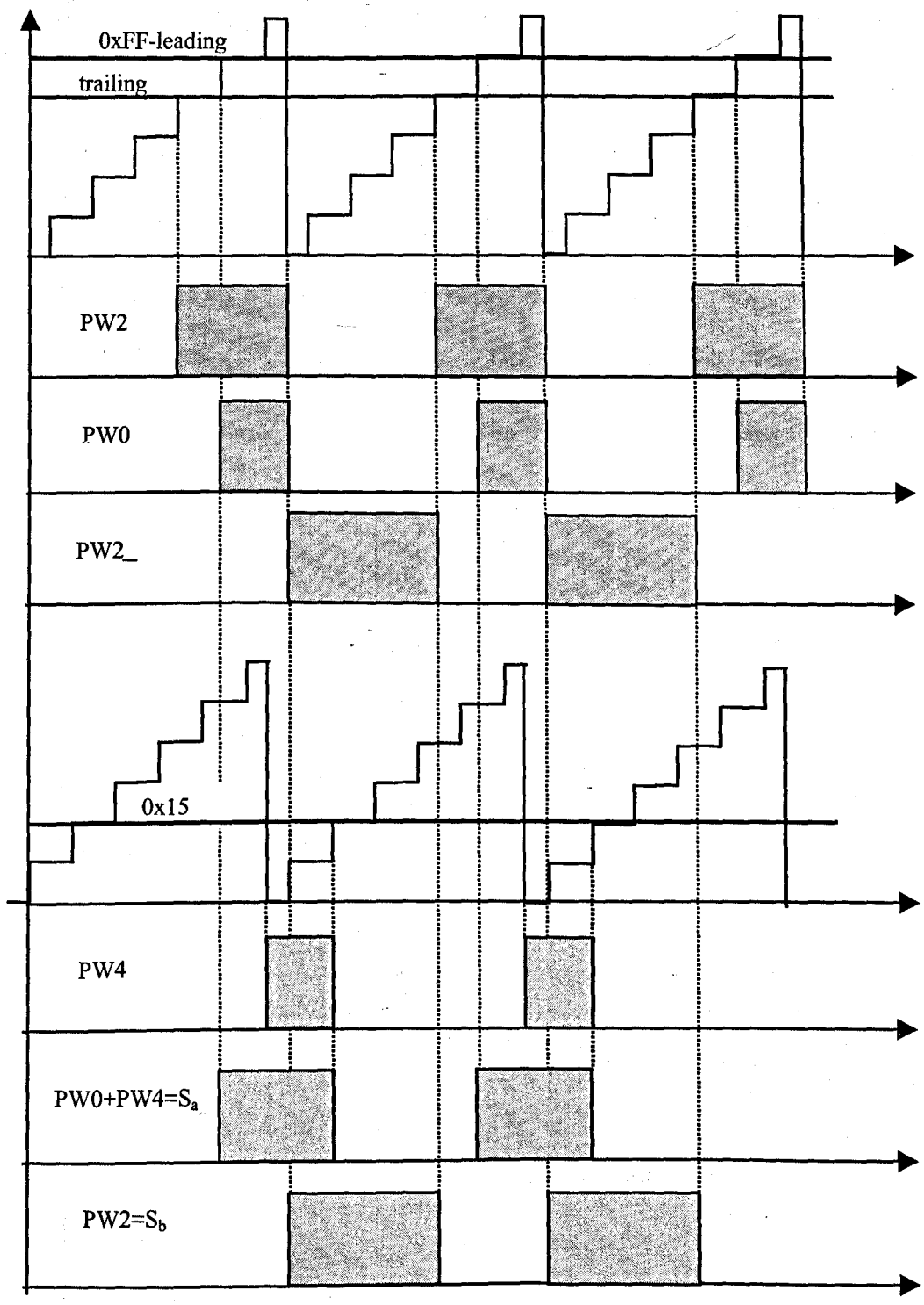


Figure 6.15 – SSPWM μC Implementation

Figure 6.15 shows the approximate timing diagram for SSPWM implementation for pulses in the 0-30° period of the mains cycle. Three of the PWM generators of the μC are used for the SSPWM itself and the fourth generates the overlap pulses. The three SSPWM carriers all start running at the same time. The overlap carrier is started one

instruction cycle before the SSPWM carriers. The carriers all count up to 0xFF and are then reset to zero. The values read from the table are the "trailing" and "leading" variables. The short duration pulse is generated by comparing the carrier with 0xFF-leading to produce the output PW0. The table value "trailing" produces PW2 and is inverted to give the long duration pulse, PW2_. PW0 and PW2_ are the short and long SSPWM pulses output by the μC, only without the overlap on the short pulse. The overlap is generated by comparing the overlap carrier with a constant, 0x15 (which gives approximately 750ns overlap time), to give PW4. PW4 is added to PW0 using external logic to give the short pulse plus overlap. The external logic is controlled by three μC outputs, so that the correct phase has the overlap pulse added onto it. PW3 (not shown) is set high, as this is the phase that is held on for this period.

Figure 6.16 shows the overall system block diagram. The clock of the μC is modulated by the mains frequency. Thus all timing, including the switching frequency, is modulated by and locked to the mains frequency.

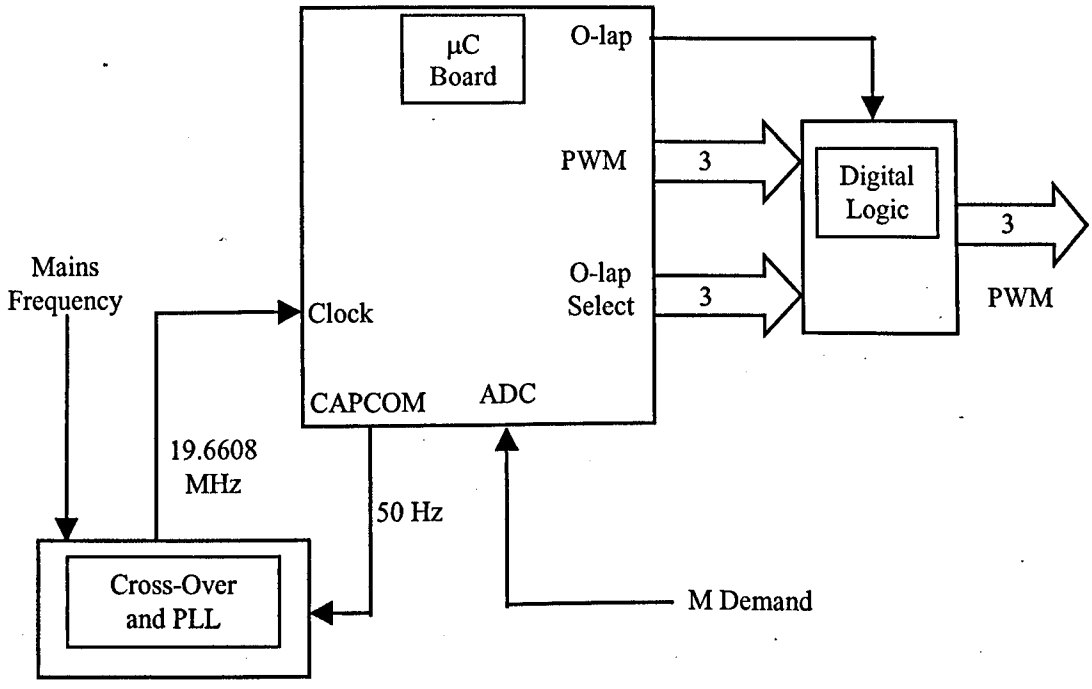


Figure 6.16 – Overall SSPWM System Layout

6.5 Theoretical Switching Loss Reduction of SSPWM Over CAPWM

General Switching Loss Analysis

The idealised (voltage over-shoot at turn-off and diode reverse-recovery at turn-on are ignored) turn-on and turn-off voltage and current waveforms for a constant current load (such as is the three-phase converter) are shown in Figure 6.17 [6.4].

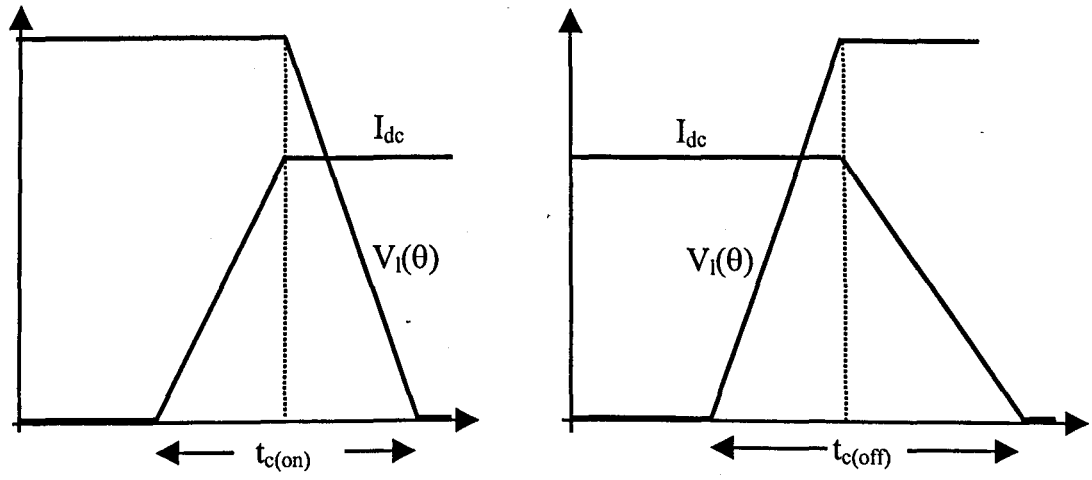


Figure 6.17 – Turn-On and Turn-Off Switching Waveforms

The instantaneous turn-on energy loss, $W_{c(on)}(\theta)$, at a position θ in the mains cycle is given by Equation (6.1a) and the instantaneous turn-off energy loss, $W_{c(off)}(\theta)$, at a position θ in the mains cycle by Equation (6.1b).

$$W_{c(on)}(\theta) = \frac{1}{2} V_l(\theta) I_{dc} t_{c(on)} \tag{6.1a}$$

and

$$W_{c(off)}(\theta) = \frac{1}{2} V_l(\theta) I_{dc} t_{c(off)} \tag{6.1b}$$

Where $V_l(\theta)$ is the line-to-line voltage across the switch and varies throughout the mains cycle as a function of the angular position within the cycle, θ, $t_{c(on)}$ is the turn-on cross-over interval, $t_{c(off)}$ is the turn-off cross-over interval and I_{dc} is the dc current and is assumed to be constant throughout a mains cycle.

CAPWM Theoretical Switching Losses

The turn-on power loss, P_{s1}, and the turn-off power loss, P_{s2}, converted into an average power over one mains cycle by using the approximation that $T_s \to 0$, are given by the integral

$$P_{sx} = \frac{f_s}{2\pi} k_{sx} \int_0^{2\pi} V_l(\theta) d\theta \qquad \text{x=1, 2} \qquad (6.2)$$

where the constant $k_{s1}=0.5t_{c(on)}I_{dc}$ and x=1 for the turn-on switching losses and the constant $k_{s2}=0.5t_{c(off)}I_{dc}$ and x=2 for the turn-off switching losses. Each switch is only switching for four out of every six sextants in one mains cycle, where the switching loss for one sextant is the same as for any other. Equation (6.2) is rewritten as

$$P_{sx} = \frac{f_s}{3\pi} k_{sx} \int_0^{\frac{\pi}{3}} V_l(\theta) d\theta \qquad \text{x=1, 2} \qquad (6.3)$$

For the 0-60° sextant, $V_l(\theta) = V\left[\sin\theta - \sin\left(\theta + \frac{4\pi}{3}\right)\right]$ for both turn-on and turn-off, where V is the peak phase voltage. The total switching power loss is given by

$$P_{s(total)} = P_{s1} + P_{s2} = \frac{f_s}{2\pi} V(k_{s1} + k_{s2}) \qquad (6.4)$$

SSPWM Theoretical Switching Losses

SSPWM still uses the same 60° dead-band scheme as CAPWM, where each switch only switches for four out of every six sextants in a mains cycle. The turn-on switching loss for switch S_a is composed of CAPWM type losses from between 0-30° and reduced-voltage-stress type loss from 30-60° according to

$$P_{s1(sspwm)} = \frac{f_s}{3\pi} k_{s1} V \left\{ \int_0^{\frac{\pi}{6}} \left[\sin\theta - \sin\left(\theta + \frac{4\pi}{3}\right)\right] + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} \left[\sin\theta - \sin\left(\theta + \frac{2\pi}{3}\right)\right] \right\} \qquad (6.5)$$

The turn-off switching loss for S_a between 0-30° is zero and between 30-60° the loss is as in the case for CAPWM and is given by

$$P_{s2(sspwm)} = \frac{f_s}{3\pi} k_{s2} V \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} \left[\sin\theta - \sin\left(\theta + \frac{4\pi}{3}\right) \right] \tag{6.6}$$

The total switching power loss for SSPWM is given by

$$P_{st(sspwm)} = P_{s1(sspwm)} + P_{s2(sspwm)} = \frac{\sqrt{3} f_s}{6\pi} V\left(k_{s1} + k_{s2}\right) \tag{6.7}$$

Comparing this equation with Equation (6.4), SSPWM shows an approximate 42% reduction over CAPWM for both turn-on and turn-off losses.

6.6 Practical Results

Heat-runs for both CAPWM and SSPWM using a small modulation index, M, so as to reduce the effect of conduction losses, are shown in Figure 6.18. SSPWM gives a lower heatsink temperature rise compared with CAPWM.

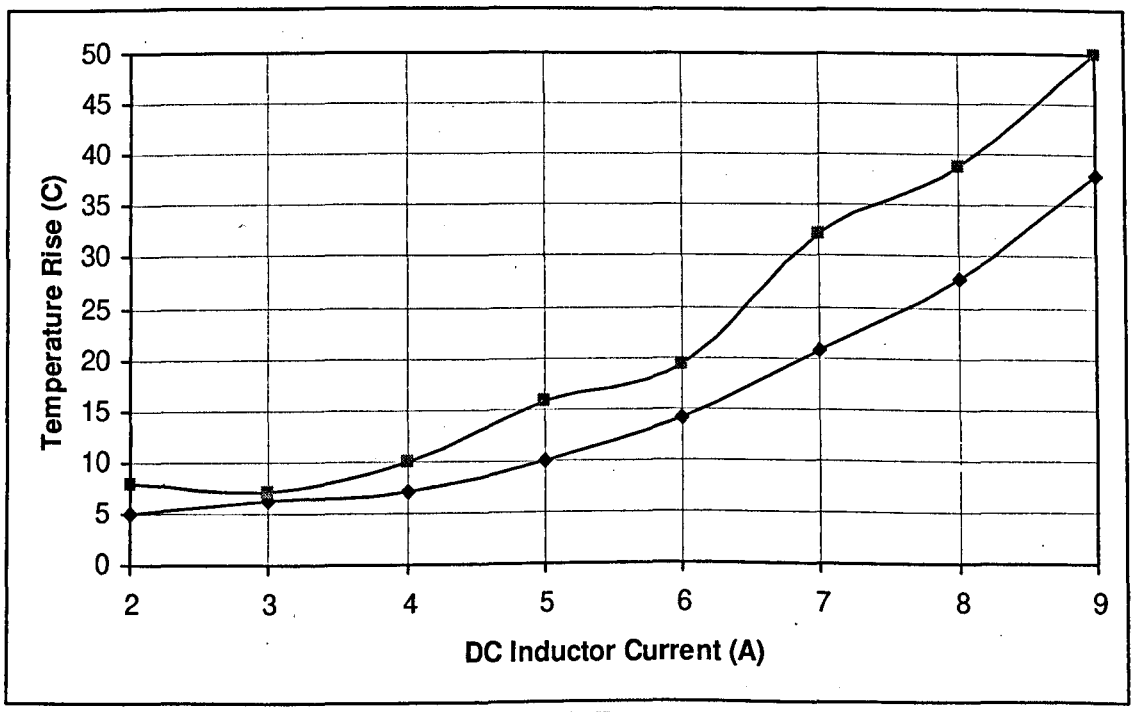


Figure 6.18 – Heatsink Temperature Rise

Upper Plot : CAPWM and Lower Plot : SSPWM

Figure 6.19 shows the practical converter waveforms for SSPWM. Current commutation from S_a into S_b is shown.

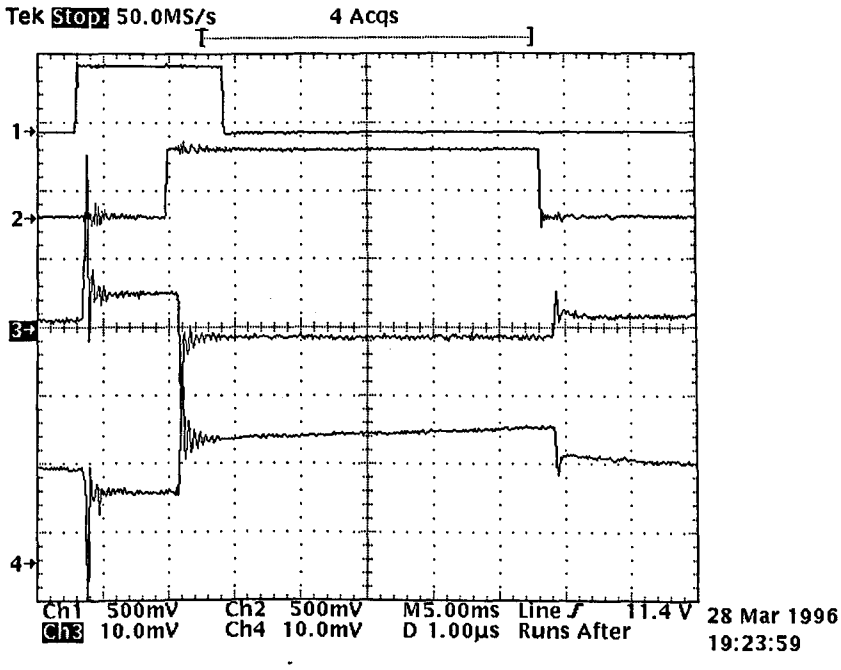


Figure 6.19 – Gate Drive and Diode Current SSPWM Pulses

Upper Trace : S_a Gate Pulse 5V/div, Second Trace : S_b Gate Pulse 5V/div

Third Trace : S_a Current 5A/div and Lower Trace : S_b Current 5A/div

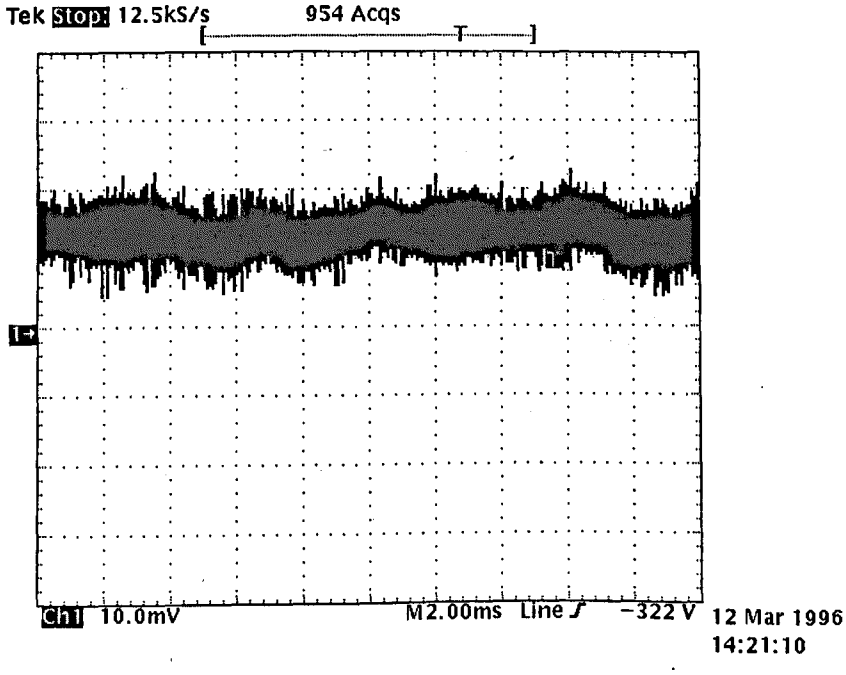


Figure 6.20 - DC-Side Inductor Current 5A/div

The dc-side inductor current is similar to the PSpice™ waveform, Figure 6.20, only with some 300Hz ripple due to the flat-topped mains

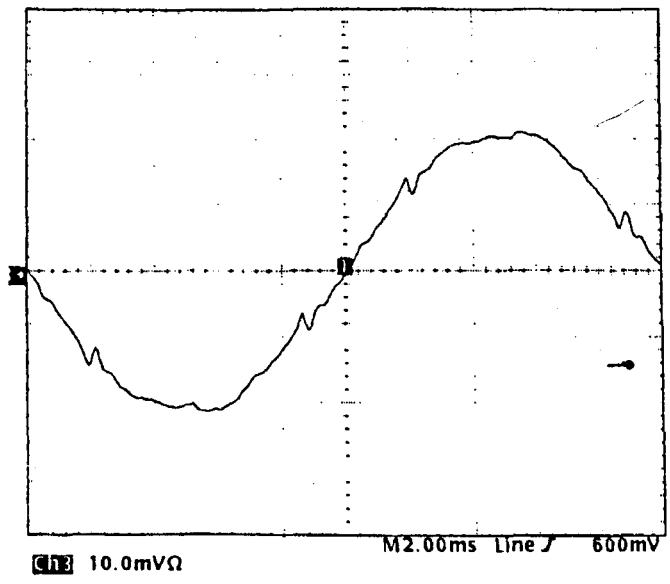


Figure 6.21 – Input AC Current 5A/div

Figure 6.21 shows the sinusoidal ac input current. Distortion around the 30, 120, 150 and 270° points is due to; **(i)** incomplete commutation of current from the lower potential phase into the higher potential one as the two voltages are nearly equal in magnitude and **(ii)** the 30° glitch in SSPWM, Figure 6.5, as the carriers change over.

6.7 Conclusions

A new PWM scheme has been proved to reduce the switching losses in the three-phase converter. The scheme requires no additional power-associated components, rather, a simple change in the PWM pulses' positions and the introduction of some overlap time. A disadvantage of the scheme is that distortion is introduced around the 30° points of the ac input current waveform, but it is possible that this can be reduced by using MSSPWM. SSPWM is more complicated to implement than CAPWM.

6.8 References

6.1 S. J. Finney, B. W. Williams and T. C. Green, "IGBT Turn-Off Characteristics and High Frequency Applications", IEE Colloquim, No. 1994/104, April 1994

6.2 D. J. Tooth, S. J. Finney, J. N. McNeill and B. W. Williams, "Soft Switching and Interleaving for Sinusoidal Input Current AC to DC Step Down Converters", IEEE PESC Conf., Vol. I, pp. 183-187, 1996

6.3 _____, "SABC167 16-Bit Microcontroller User Manual 03.96 Version 2.0", Siemens, 1996

6.4 B. W. Williams, "Power Electronics", Second Edition, MacMillan Press, p. 134, 1992

CHAPTER 7 - Conclusion

Conclusions

The three-switch, three-phase step-down ac-dc converter has been analysed in a number of different ways. A CAPWM scheme using an EPROM look-up table was implemented that, under the ideal conditions of sinusoidal input voltages and infinite dc inductor, gives a pure dc output voltage term and sinusoidal input currents. In practice, neither of these two conditions are met and this gives rise to ac and dc-side harmonic distortion. Steady state design equations describing the average currents in the diodes, free-wheeling diode and switches were developed. An equation describing the maximum and minimum ripple current for the dc-side inductor was found, as was an equation that describes the maximum voltage ripple on the ac-side capacitors. Average power loss equations for the converter were developed and used to estimate the losses in the 3kW design example. It is noted that the six-switch converter would be less than 1% more efficient than the three-switch converter due to the large conduction power loss in high frequency optimised IGBTs.

The FTJ was found to be useful when developing closed-form expressions for the input current and output voltage/current harmonics of converters with complex PWM schemes. The harmonics are found to vary in magnitude according to the Bessel functions and occur in sideband pairs around integer multiples of the switching frequency. The input current harmonic equation is similar to the harmonic equation for FM and the output voltage harmonic equation is similar to FM and DSBM. The input current harmonics are all odd and do not contain triplen harmonics. The output voltage harmonics are all multiples of six, due to the underlying rectification process and are all even. Interleaving the PWM schemes for two converters eliminates the harmonics centred around f_s. The PSpice™ simulations for the harmonics yield results that all agree with the mathematical analysis.

The effects of the supplies being flat-topped due to non-linear loading was found to generate a strong 6^{th} harmonic component on the dc-side and 5^{th} and 7^{th} on the ac-side. A similar, but weaker, effect was noted as regards using a finite dc inductor. The rules regarding predicting the transfer of harmonics from the ac/dc and dc/ac sides were confirmed to hold for this converter.

A switching, three-phase SIMULINK™ model was developed for the converter. This model enables the converter to be studied under easily-set conditions, such as pure sinusoidal supplies or supplies with a constant distortion component. By perturbing the model, Bode plot transfer functions can be plotted to gain understanding. In particular, the effects of the input filter and closing the current feedback loop were studied. The input filter and closed current-loop can easily form an unstable system due to the impedance criterion being broken, i.e. for a stable system, the output impedance of the input filter should be much less than the input impedance of the bridge. The inductance of the mains supply itself is problematical, as its inductance is much greater than the inductance of the converter's input filter. This means that the resonant frequency of the input filter is dominated by the supply inductance and therefore varies from mains distribution system to system. Therefore, although the input filter can be successfully damped using resistors and capacitors, it does not mean that the converter is guaranteed to be stable when supplied by another mains network. Closing the current loop has several advantages. The two major advantages being damping of the dc filter resonance and reducing the current harmonics due to flat-topped mains supplies.

A dc-dc average converter model was developed and found to be in agreement with the three-phase switching model as regards to its time and frequency domain responses.

Parallel connection of two converters to drive the same dc-side load and work from a common input filter was successfully implemented. Interleaving the PWM

schemes was found to greatly reduce the harmonics around f_s in practice and eliminate them under ideal, simulated conditions. Unlike the six-switch boost converter, the three-switch converter does not suffer from inter-bridge currents when two converters are paralleled.

SSPWM was implemented and found to reduce the measured heatsink temperature rise in a converter. SSPWM does not rely on the addition of any hardware components, instead, changes in the positions of the PWM pulses are made so that they overlap, so creating reduced voltage, zero voltage and zero current switching transitions at different points in a mains cycle. Approximate equations were developed that show a theoretical 42% reduction in switching losses.

Suggestions for Further Work

More work could be carried out on the issue of input filter damping, especially as regards robustness of the damping with respect to input inductance variations. More sophisticated control schemes (sliding mode control) could be implemented that give greater robustness to known changes in the input inductance could be considered. Also, active damping of the input filter should be considered in order to decouple the damping of the input filter from the main control function.

To meet the impedance criterion more easily, the input filter capacitors could be increased in size. This would give rise to an increase in lagging power factor reactive power flow, but this could be compensated for by making the converter draw leading power factor current.

Whilst techniques exist for measuring the frequency responses for dc-dc or dc-ac converters, the measuring of transfer functions on three-phase ac-dc practical converter rigs remains a problem due to the significant and variable harmonics injected from the

three-phase supply. Work could be carried out to concentrate on finding good methods to do this.

More experimental work could be done as regards measuring of input harmonics to the converter to check for compliance with the relevant harmonic standards and the selection of a minimum-size input filter.

Author's Contribution

Steady-state equations for the converter currents, dc filter inductor ripple and power losses were developed. Use of the FTJ to develop closed-form expressions for the harmonics of the converter was demonstrated. PSpice™ simulations of the converter, dual interleaved converters and soft-switching converter were implemented and the waveforms and harmonics compared with the practical and mathematical equations' results. A thorough investigation into the effects of closed-loop average current mode control was made, including the stability problem when an input filter is added and a clear explanation was given using simulation results and mathematics of the damping of the dc filter due to current-mode control. The effects of the mains voltage flat-topping were studied in relation to closed-loop current control. Two SIMULINK™ models were derived and tested with respect to frequency responses with and without an input filter and under open and closed current loop control. A soft-switching PWM scheme was implemented and investigated (the original idea for the scheme was proposed by Mr. N. M^{c}Neill) as regards its switching loss reduction and found to be effective. The effectiveness of using dual interleaved converters was found, via simulation and practical work, to be feasible and to reduce the input current switching harmonics.

Appendix A1 – PSpice™ Listing for a Single Converter

```
*unity power factor circuit for three-phase ac-dc converter
.TRAN 20u 40m 0m 5U UIC
.OPTIONS ABSTOL 10UA VNTOL 100mV RELTOL=0.01 NUMDGT=8

V1 1 0 SIN(0 240 50 0 0 0.0)
L1 1 9 50u IC=0
R1 9 10 0.2
C1 10 20 3u IC=-208
D11 11 10 DIODE
D12 10 12 DIODE
S1 11 12 17 0 SSWITCH
D13 11 13 DIODE
D14 14 12 DIODE

V2 2 0 SIN(0 240 50 0 0 120.0)
L2 2 19 50u IC=5
R2 19 20 0.2
C2 20 30 3u IC=208
D21 21 20 DIODE
D22 20 22 DIODE
S2 21 22 27 0 SSWITCH
D23 21 13 DIODE
D24 14 22 DIODE

V3 3 0 SIN(0 240 50 0 0 240.0)
L3 3 29 50u IC=-5
R3 29 30 0.2
C3 30 10 3u IC=-416
D31 31 30 DIODE
D32 30 32 DIODE
S3 31 32 37 0 SSWITCH
D33 31 13 DIODE
D34 14 32 DIODE

LR 13 18 160u IC=9
R4 18 15 0.2
CR 15 14 4700u IC=180
RLOAD 15 14 20
Df 14 13 DIODE

RDUMMY1 16 0 .5
.INC "c:\mseval61\PWLFILE0.OUT"
RC1 17 0 1K

RDUMMY2 26 0 .5
.INC "c:\mseval61\PWLFILE1.OUT"
RC2 27 0 1K

RDUMMY 36 0 .5
.INC "c:\mseval61\PWLFILE2.OUT"
RC3 37 0 1K

.MODEL SSWITCH VSWITCH(VON=5, VOFF=2, RON=0.2)
.MODEL DIODE D(RS=0.2 CJO=0.01N)
.PRINT TRAN i(r1) i(r2) i(r3) i(lr)
.PROBE i(lr) i(r1) v(10,30) v(15,14)
.END
```

Appendix A2 – "C" Programs for Generating PWM

```
/*********************************************************************/
/* THIS ROUTINE PROVIDES A MAIN LINKING ROUTINE FOR THE PWM
MODULATION SIMULATION.
The program generates three PWL files corresponding to the sinusoidal
PWM switching pattern.*/
/*********************************************************************/

#define MODULATION  (double)1/50 /*The modulation period*/
#define SAMPLE (float)1.0/76800.0 /*The switching period*/
#define NUM_CYCLES (int)2/*Number of modulation cycles*/
#define MOD_INDEX  (double)0.577

float t[10000];
void main()
{
double get_dec();
void wrt_pwl();
int pwm_mod();

int carrier;
int cycles=NUM_CYCLES;
double Tmod=MODULATION;
float Ts=SAMPLE;
double mod_index=MOD_INDEX;
double phase=0;
char name[]={'p','w','l','f','i','l','e','.','o','u','t'};
/*This subroutine generates the PWM times*/
carrier=pwm_mod(cycles,Tmod,Ts,mod_index, phase);

/*PWL file for phase 1 (+0)*/
wrt_pwl("PWLFILE0.OUT", carrier,t,Tmod,phase);
phase++;

/*PWL file phase 2 (+120)*/
carrier=pwm_mod(cycles,Tmod,Ts,mod_index, phase);
wrt_pwl("PWLFILE1.OUT", carrier,t,Tmod, phase);
phase++;

/*PWL file phase 3 (+240)*/
carrier=pwm_mod(cycles,Tmod,Ts,mod_index, phase);
wrt_pwl("PWLFILE2.OUT", carrier,t,Tmod,phase);
}
```

```
/*
AUTHOR :S.J.FINNEY modified D.J. TOOTH

FUNCTION    : This creates a time array of On and Off times simulating
              a PWM signal.

PSEUDO CODE : n.b. this is the bog-standard version. The only thing
              added is the code to generate an extra fall & rise time
              for glitch free operation at crossover.

              Line changed to '<' to create interleaving effect. This
              program should be run in conjunction with orig.prj. The
              two together produce six pwl files for use with two,
              phase-overlapping converters.

*/
```

```
#include<stdio.h>
#include<math.h>

extern float t[6000];

char pwm_mod(cycles,Tmod,Ts,mod_index,phase)
int cycles;
double Tmod;
float Ts;
double mod_index;
float phase;
{
FILE *fopen();
int fclose();

double cos(),sin();

double ang_freq,pi=(double)4*atan(1.0);
double Vc=(double)1,Vs;
int N=1,M=1, SN=1;
float P,rise,fall,Tcyc;

/* the voltages are normalised to Vc=1 */

Vs=mod_index*Vc;
/* normalise the time period to 1 Hz */
Ts=Ts/Tmod;
Tmod=1;

ang_freq=(double)2*pi/Tmod;

M=cycles;
P=0.0;
phase=phase*2*pi/3;
/*this selects the approriate phase*/


/*correct for the negative values*/
for(N=0;(N/2*Ts)<(M*Tmod);N=N+2)
        {
        if( sin(P*ang_freq*Ts+phase)<0)
        {
        SN=-1;
        }
        else
        {
        SN=1;
        }

P=(float)(N)/2.0;
fall=(float)Ts/2.0*(1.0 - Vs*SN*sin(P*ang_freq*Ts+phase));
rise=(float)Ts/2.0*(Vs*SN*sin((P+0.50)*ang_freq*Ts+phase));


      if  ( cos( P*ang_freq*Ts+phase)>0)  /*use '<' to interleave 2nd
      data set*/
            {
            t[N+1]=(float)P*Ts+fall;
            /*ON time */
            t[N+2]=(float)(P+0.50)*Ts+rise;

            /*OFF time */
            }
```

```
            else
            {
            /*This ensures that the two pulses occupy different time
              slots*/
            t[N+1]=(float)P*Ts+fall+Ts/2;
            /*ON time */
            t[N+2]=(float)(P+0.50)*Ts+rise+Ts/2;
            /*OFF time */
            }

      }
return(N/2);
}
```

```
/*
AUTHOR :S.J.FINNEY

MODULE NAME : wrt_pwl

FILE NAME   : wrt_pwl.c

FUNCTION    : This file reads in the PWM switching times and writes
              them to a PWL file format.
*/

#include<stdio.h>
#include<math.h>

void wrt_pwl( f_name,length,c,Tmod, phase)

char f_name[];
int length;
float c[], Tmod ;
double phase;

{
FILE *fopen();
int fclose();
double pi=(double)4*atan(1.0);
FILE *stream, *stream2;
float T1,T2;
float Tr, Tmin , Tcyc;
int n, P1, P2;
int flag1=1;
int flag2=1;
int zero=0;
Tr=  0.000001;     /* the rise time*/
Tmin=0.000002;     /* the MINIMUM on time */

stream=fopen(f_name,"w");

/*Piece wise linear file headers*/
if (phase==0) fprintf (stream,"V12 17 16 PWL(");
if (phase==1) fprintf (stream,"V22 27 26 PWL(");
if (phase==2) fprintf (stream,"V32 37 36 PWL(");
c[0]=5*Tr;

for(n=1;n<2*length;n=n+1)
 {
/*This tests for the part of the cycle where the switch is always ON*/
       if( (sin(c[n]*2*pi+(phase*2*pi/3))>sin(pi/3))
       ||(sin(c[n]*2*pi+(phase*2*pi/3))<-sin(pi/3)) )
```

```
            {     /* ON all the time*/
            P1=10;
            P2=10;

      if (flag1==1)    /*check for a phase changing from
                              switching to on*/
                  {
                  T1=(c[n-1]+2*Tr)*Tmod;
                  fprintf(stream," +%1.8f  %d \n ",T1,P1);  /*add a
                                                      rise time in*/
                  flag1=0;
                  flag2=1;
                  }
            }
      else
            {     /*switching*/
            P1=0;
            P2=10;
      if (flag2==1)    /*check for change from on to switching*/
                  {
                  T1=(c[n-1]+2*Tr)*Tmod;
                  fprintf(stream," +%1.8f  %d \n ",T1, zero);
                                          /*add a fall time in*/
                  flag2=0;
                  flag1=1;
                  }
            }

      /* minimum pulse width test*/

      if(((c[n+1]-c[n])>Tmin)&&((c[n]-c[n-1])>Tmin))
            {
            /*This writes the P1-P2 tranition to file*/
            T1=c[n]*Tmod;
            T2=(c[n]+Tr)*Tmod;
            fprintf(stream," +%1.8f  %d \n ",T1, P1);
            fprintf(stream," +%1.8f  %d  \n",T2, P2);
            }
      n++;

      /*minimum pulse width test*/
      if(((c[n+1]-c[n])>Tmin)&&((c[n]-c[n-1])>Tmin))
            {
            /*write P2-P1 transition to file*/
            T1=c[n]*Tmod;
            T2=(c[n]+Tr)*Tmod;
            fprintf(stream," +%1.8f  %d \n ",T1, P2);
            fprintf(stream," +%1.8f  %d \n ",T2, P1);
            }
 } /*FOR*/
fprintf(stream, ")");
fclose(stream);
return;
}
```

Appendix A3 - Input Current Harmonics

test4.mcd calculates fourier bn coeff's using jumps method for entirety of the normal centre-aligned, interleaved pwm switching waveform.Uses Bessel functions.
7/4/98

$Idc := 10 \qquad fm := 1 \qquad fs := 69 \qquad M := 0.3$

$I := Idc \qquad n := 1,3..fs\cdot 10.5 \qquad Ts := \frac{1}{fs} \qquad p := 1,2..\frac{fs-3}{6} \qquad q := 1,3..11 \qquad wm := 2\cdot\pi\cdot fm$

$x_n := \frac{n\cdot M\cdot wm\cdot Ts}{2} \qquad wt_p := wm\cdot Ts\cdot p \qquad wt2_p := wm\cdot\frac{Ts}{2}\cdot(2\cdot p-1)$

$$b1_n := \frac{2\cdot I}{n\cdot\pi}\cdot\left[\sum_p\sum_q\left(4\cdot Jn\left(q,x_n\right)\cdot\sin\left(n\cdot wt_p\right)\cdot\sin\left(q\cdot wt_p\right)\right)\right]$$

0 to 60 degrees

$$b2_n := \frac{2\cdot I}{n\cdot\pi}\cdot\left[\sum_p\sum_q\left(4\cdot Jn\left(q,x_n\right)\cdot\sin\left(n\cdot wt2_p+n\cdot\frac{\pi}{3}\right)\cdot\sin\left(q\cdot wt2_p+2\cdot\frac{\pi}{3}\cdot q\right)\right)\right]$$

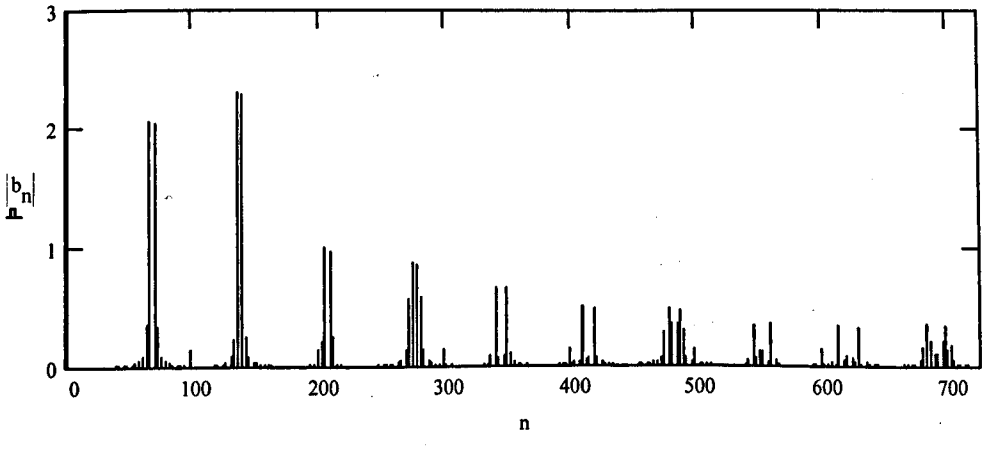
60 to 120 degrees

$$b3_n := \frac{2\cdot I}{n\cdot\pi}\cdot\left[\sum_p\sum_q\left(4\cdot Jn\left(q,x_n\right)\cdot\sin\left(n\cdot wt_p+n\cdot\frac{\pi}{3}\right)\cdot\sin\left(q\cdot wt_p\right)\right)\right]$$

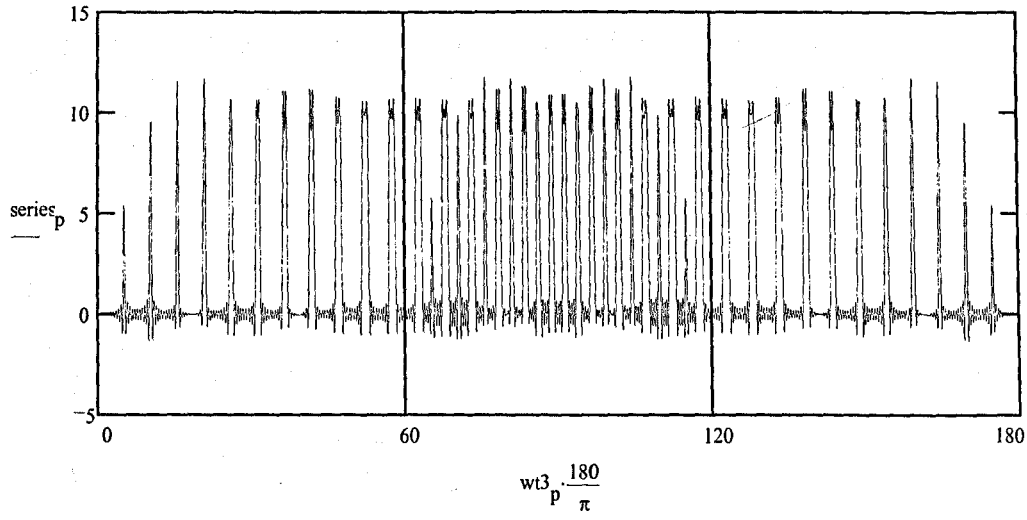
$$b4_n := \frac{2\cdot I}{n\cdot\pi}\cdot\left[\sum_p\sum_q\left(4\cdot Jn\left(q,x_n\right)\cdot\sin\left(n\cdot wt2_p+n\cdot\frac{2\cdot\pi}{3}\right)\cdot\sin\left(q\cdot wt2_p+2\cdot\frac{\pi}{3}\cdot q\right)\right)\right]$$

120 to 180 degrees

$b_n := b1_n + b2_n + b3_n + b4_n$

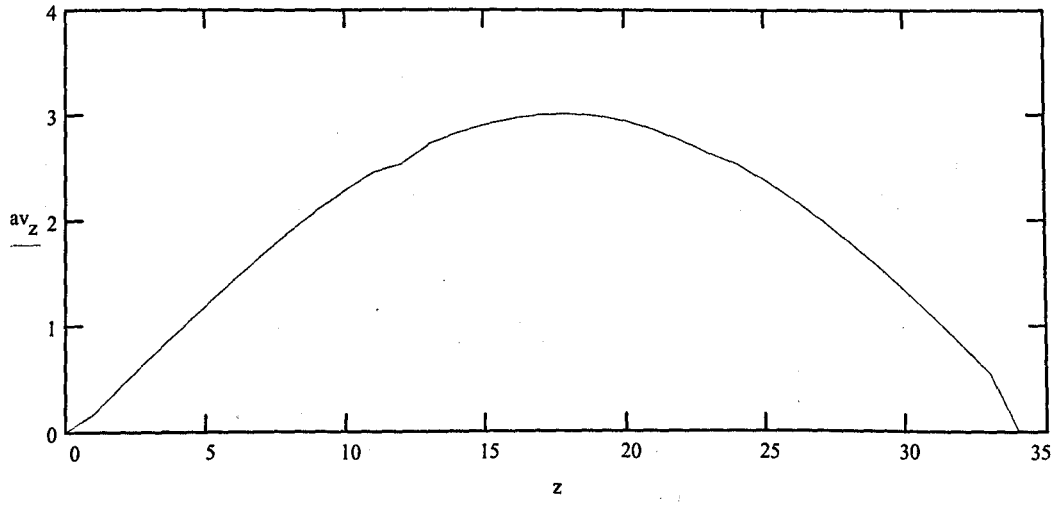


$p := 1,2..\frac{80\cdot fs-3}{2} \qquad wt3_p := wm\cdot\frac{p}{80}\cdot Ts \qquad series_p := \sum_n\left(b_n\cdot\sin\left(n\cdot wt3_p\right)\right)$



$q := 0,1..\frac{fs}{2} - \frac{3}{2\cdot 80} - 1$ $p := 1,2..80$ $z := 0,1..34$ $av_{q+1} := \frac{1}{80}\cdot\sum_{p} series_{p+80\cdot q}$

$av_0 := 0$ $av_{34} := 0$



Appendix A4 - Output Voltage Harmonics

test10.mcd calculates fourier bn coeff's using jumps method for entirety of the normal centre-aligned, interleaved pwm switching waveform.Uses Bessel functions. This one for output voltage harmonics. this version is much simplified. assumes all harmonics will be multiples of six. 16/4/98

$fm := 1 \qquad fs := 87 \qquad M := 0.3 \qquad V := 150$

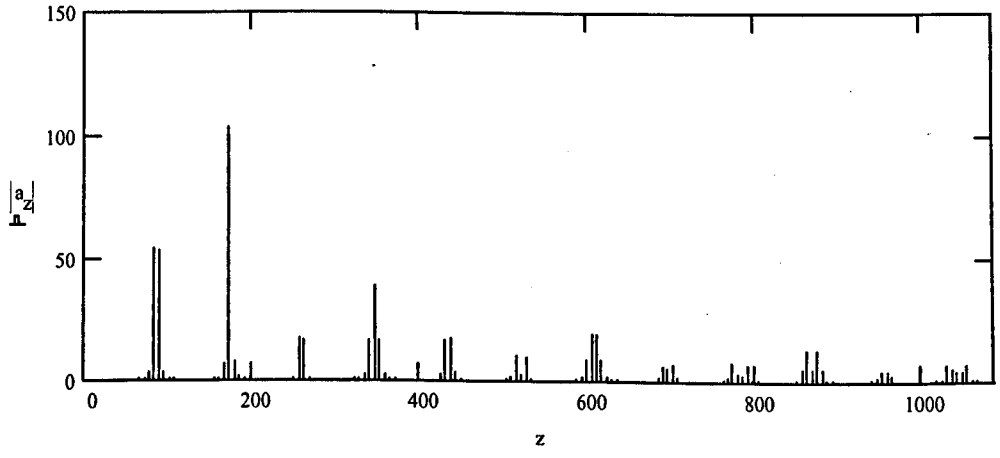
$n := 6, 12 .. 20.5 \cdot fs \quad z := 0, 2 .. 20.5 \cdot fs \quad Ts := \frac{1}{fs} \qquad p := 1, 2 .. \frac{fs - 3}{6} \qquad q := 1, 3 .. 11 \qquad wm := 2 \cdot \pi \cdot fm$

$x_n := \frac{n \cdot M \cdot wm \cdot Ts}{2} \qquad wt_p := wm \cdot Ts \cdot p \qquad wt2_p := wm \cdot \frac{Ts}{2} \cdot (2 \cdot p - 1)$

$V1_p := \sqrt{3} \cdot V \cdot \sin\left(wt_p + \frac{\pi}{6}\right) \qquad V2_p := \sqrt{3} \cdot V \cdot \cos\left(wt2_p\right)$

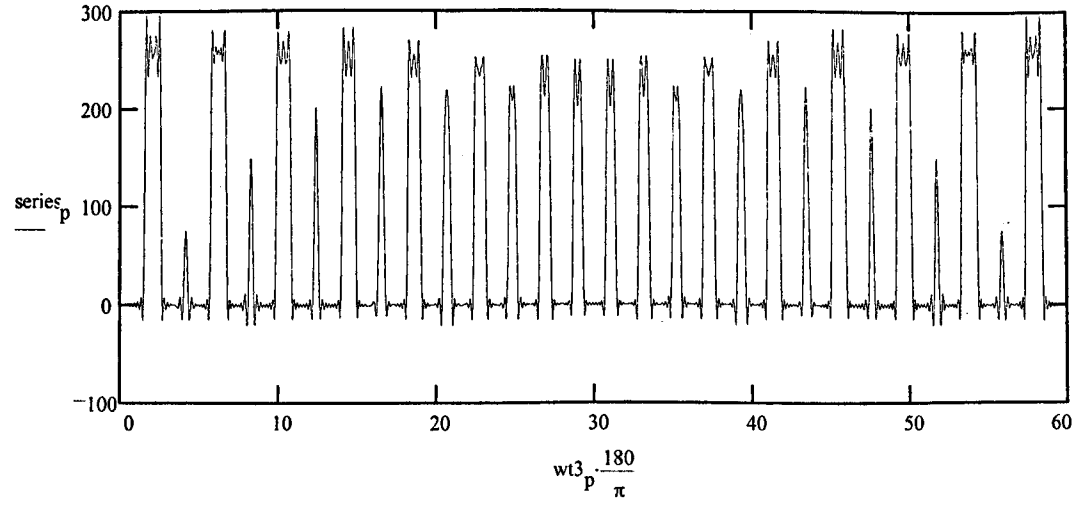
$$a_n := \frac{24}{n \cdot \pi} \cdot \left[\sum_p \sum_q Jn\left(q, x_n\right) \cdot \left(V1_p \cdot \cos\left(n \cdot wt_p\right) \cdot \sin\left(q \cdot wt_p\right) + V2_p \cdot \cos\left(n \cdot wt2_p\right) \cdot \sin\left(q \cdot wt2_p + 2 \cdot \frac{\pi}{3} \cdot q\right) \right) \right]$$

$a_0 := \frac{3}{2} \cdot M \cdot V \qquad a_0 = 67.5$



$a_{84} = -54.008 \quad a_{174} = 102.98 \quad a_{168} = -6.941 \quad a_{252} = -0.778 \quad a_{258} = -17.346$

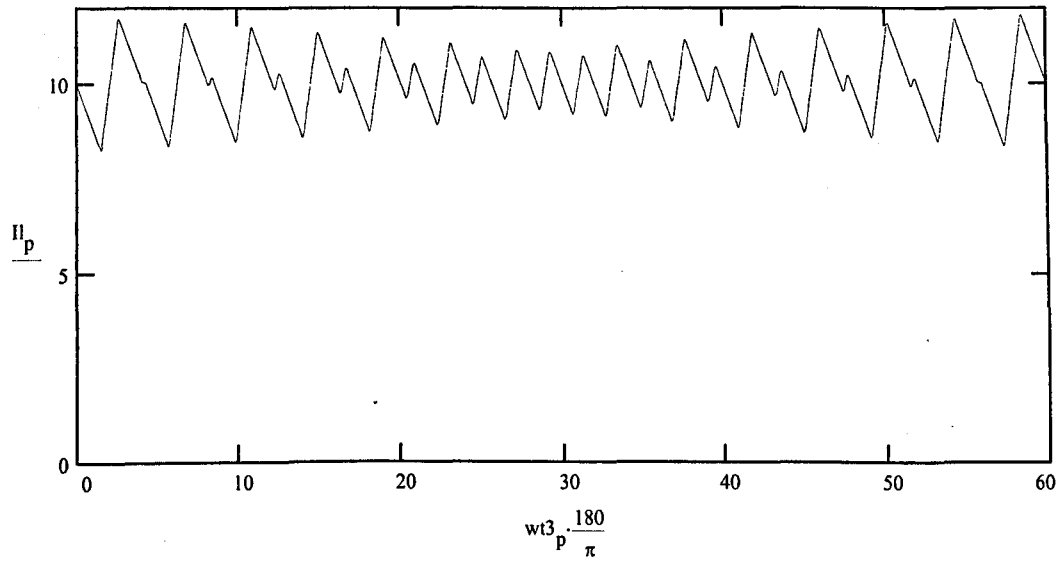
$n := 6, 12 .. 20.5 \cdot fs \qquad p := 1, 2 .. \frac{fs \cdot 80 - 3}{6} \qquad wt3_p := wm \cdot \frac{Ts}{80} \cdot p \qquad series_p := \sum_n \left(a_n \cdot \cos\left(n \cdot wt3_p\right)\right) + a_0$



$L := 1 \cdot 10^{0}$ $R := 6.75$ $p := 1, 2 .. \frac{fs \cdot 80 - 3}{6}$ $wt3_p := wm \cdot \frac{Ts}{80} \cdot p$ $Il_0 := \frac{a_0}{R}$

$Il_p := \frac{1}{L} \cdot \left(series_p - a_0\right) \cdot wm \cdot \frac{Ts}{80} + Il_{p-1}$ length of each p in time is wm*Ts/80

$ripplei := \max(Il) - \min(Il)$ $ripplei = 3.569$



Appendix A5 - Dual Interleaved Converters Input Current Harmonics

test5.mcd calculates fourier bn coeff's using jumps method for entirety of the normal centre-aligned, interleaved pwm switching waveform.Uses Bessel functions. This one for dual interleaved converters
14/4/98

$Idc := 10 \quad fm := 1 \quad fs := 87 \quad M := 0.5$

$I := Idc \quad n := 1,3..4.5 \cdot fs \quad Ts := \frac{1}{fs} \quad p := 1,2..\frac{fs-3}{6} \quad q := 1,3..33 \quad wm := 2 \cdot \pi \cdot fm$

$x_n := \frac{n \cdot M \cdot wm \cdot Ts}{2} \quad wt_p := wm \cdot Ts \cdot p \quad wt2_p := wm \cdot \frac{Ts}{2} \cdot (2 \cdot p - 1) \quad wt3_p := wm \cdot \frac{Ts}{2} \cdot (2 \cdot p - 1) + wm \cdot Ts$

Converter 1

$$b1_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin(n \cdot wt_p) \cdot \sin(q \cdot wt_p) \right) \right]$$

0 to 60 degrees

$$b2_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin\left(n \cdot wt2_p + n \cdot \frac{\pi}{3}\right) \cdot \sin\left(q \cdot wt2_p + 2 \cdot \frac{\pi}{3} \cdot q\right) \right) \right]$$

60 to 120 degrees

$$b3_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin\left(n \cdot wt_p + n \cdot \frac{\pi}{3}\right) \cdot \sin(q \cdot wt_p) \right) \right]$$

$$b4_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin\left(n \cdot wt2_p + n \cdot \frac{2 \cdot \pi}{3}\right) \cdot \sin\left(q \cdot wt2_p + 2 \cdot \frac{\pi}{3} \cdot q\right) \right) \right]$$

120 to 180 degrees

Converter 2

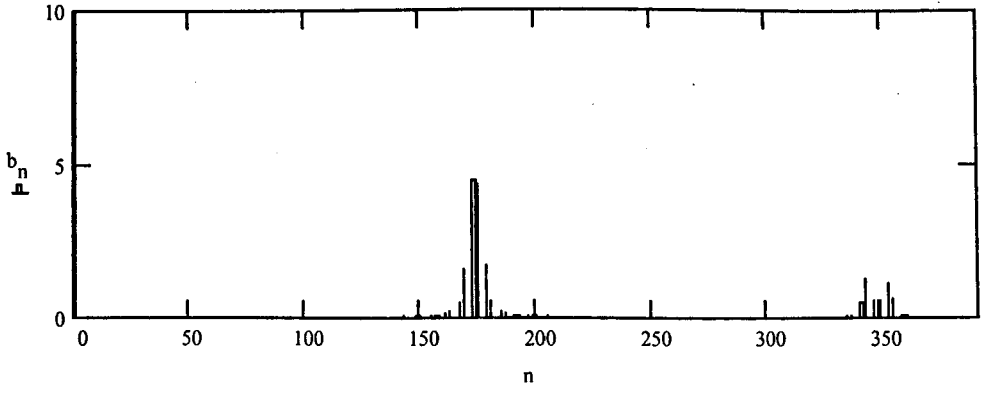
$$b21_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin(n \cdot wt3_p) \cdot \sin(q \cdot wt3_p) \right) \right]$$

$$b22_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin\left(n \cdot wt_p + n \cdot \frac{\pi}{3}\right) \cdot \sin\left(q \cdot wt_p + 2 \cdot \frac{\pi}{3} \cdot q\right) \right) \right]$$

$$b23_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin\left(n \cdot wt3_p + n \cdot \frac{\pi}{3}\right) \cdot \sin(q \cdot wt3_p) \right) \right]$$

$$b24_n := \frac{2 \cdot I}{n \cdot \pi} \cdot \left[\sum_p \sum_q \left(4 \cdot Jn(q, x_n) \cdot \sin\left(n \cdot wt_p + n \cdot \frac{2 \cdot \pi}{3}\right) \cdot \sin\left(q \cdot wt_p + 2 \cdot \frac{\pi}{3} \cdot q\right) \right) \right]$$

$$b_n := \left| b1_n + b2_n + b3_n + b4_n + b21_n + b22_n + b23_n + b24_n \right|$$



Appendix A6 - SSPWM Input Current Harmonics

This file,soft2.mcd, computes soft-switching harmonics and input current ac waveshape 24/3/99

$fs := 42 \quad Ts := \frac{1}{fs} \quad n := 1,2..400 \quad w := 2\cdot\pi \quad M := 0.577 \quad I := 9.75$

0-30 and 180-210 degrees

$p := 1..\frac{fs}{12} - \frac{1}{2} \qquad x_p := p\cdot Ts - |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)| \quad j_p := I \quad y_p := p\cdot Ts \quad k_p := -I$

$p := \frac{fs}{2} + 1..\frac{fs}{2} + \frac{fs}{12} - \frac{1}{2} \qquad x_p := p\cdot Ts - |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)| \quad j_p := -I \quad y_p := p\cdot Ts \quad k_p := I$

30-60 and 210 to 240 degrees

$p := \frac{fs}{12} + \frac{1}{2}..\frac{fs}{6} \qquad x_p := p\cdot Ts \quad j_p := I \quad y_p := p\cdot Ts + |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)| \quad k_p := -I$

$p := \frac{fs}{2} + \frac{fs}{12} + \frac{1}{2}..\frac{fs}{2} + \frac{fs}{6} \qquad x_p := p\cdot Ts \quad j_p := -I \quad y_p := p\cdot Ts + |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)| \quad k_p := I$

60-90 and 240-270 degrees

$p := \frac{fs}{6} + 1..\frac{fs}{6} + \frac{fs}{12} - \frac{1}{2} \qquad x_p := p\cdot Ts - \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + 2\cdot\frac{\pi}{3}\right)\right| \quad j_p := I$

$y_p := p\cdot Ts + \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + \frac{4\cdot\pi}{3}\right)\right| \quad k_p := -I$

$p := \frac{fs}{2} + \frac{fs}{6} + 1..\frac{fs}{2} + \frac{fs}{6} + \frac{fs}{12} - \frac{1}{2} \qquad x_p := p\cdot Ts - \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + 2\cdot\frac{\pi}{3}\right)\right| \quad j_p := -I$

$y_p := p\cdot Ts + \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + \frac{4\cdot\pi}{3}\right)\right| \quad k_p := I$

90-120 and 270-300 degrees

$p := \frac{fs}{6} + \frac{fs}{12} + \frac{1}{2}..2\cdot\frac{fs}{6} \qquad x_p := p\cdot Ts - \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + 4\cdot\frac{\pi}{3}\right)\right| \quad j_p := I$

$y_p := p\cdot Ts + \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + 2\cdot\frac{\pi}{3}\right)\right| \quad k_p := -I$

$p := \frac{fs}{2} + \frac{fs}{6} + \frac{fs}{12} + \frac{1}{2}..\frac{fs}{2} + 2\cdot\frac{fs}{6} \qquad x_p := p\cdot Ts - \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + 4\cdot\frac{\pi}{3}\right)\right| \quad j_p := -I$

$y_p := p\cdot Ts + \left|Ts\cdot M\cdot\sin\left(p\cdot Ts\cdot w + 2\cdot\frac{\pi}{3}\right)\right| \quad k_p := I$

120-150 and 300-330 degrees

$p := 2\cdot\frac{fs}{6} + 1..2\cdot\frac{fs}{6} + \frac{fs}{12} - \frac{1}{2} \qquad x_p := p\cdot Ts \quad j_p := I \quad y_p := p\cdot Ts + |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)| \quad k_p := -I$

$p := \frac{fs}{2} + 2\cdot\frac{fs}{6} + 1..\frac{fs}{2} + 2\cdot\frac{fs}{6} + \frac{fs}{12} - \frac{1}{2} \qquad x_p := p\cdot Ts \quad j_p := -I \quad y_p := p\cdot Ts + |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)| \quad k_p := I$

150-180 and 330-360 degrees

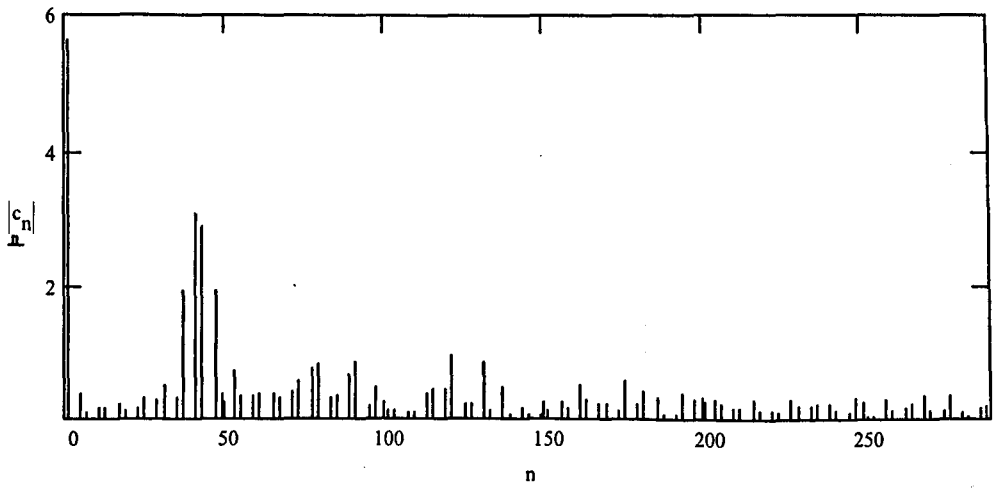
$p := 2\cdot\frac{fs}{6} + \frac{fs}{12} + \frac{1}{2} .. 3\cdot\frac{fs}{6}$ $\quad x_p := p\cdot Ts - |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)|$ $\quad j_p := I$ $\quad y_p := p\cdot Ts$ $\quad k_p := -I$

$p := \frac{fs}{2} + 2\cdot\frac{fs}{6} + \frac{fs}{12} + \frac{1}{2} .. \frac{fs}{2} + 3\cdot\frac{fs}{6}$ $\quad x_p := p\cdot Ts - |Ts\cdot M\cdot\sin(p\cdot Ts\cdot w)|$ $\quad j_p := -I$ $\quad y_p := p\cdot Ts$ $\quad k_p := I$

$p := 1, 2 .. fs$

$$a_n := -\frac{1}{n\cdot\pi}\cdot\sum_p\left(j_p\cdot\sin\left(n\cdot x_p\cdot w\right) + k_p\cdot\sin\left(n\cdot y_p\cdot w\right)\right) \qquad b_n := \frac{1}{n\cdot\pi}\cdot\sum_p\left(j_p\cdot\cos\left(n\cdot x_p\cdot w\right) + k_p\cdot\cos\left(n\cdot y_p\cdot w\right)\right)$$

$$c_n := \sqrt{\left(a_n\right)^2 + \left(b_n\right)^2}$$

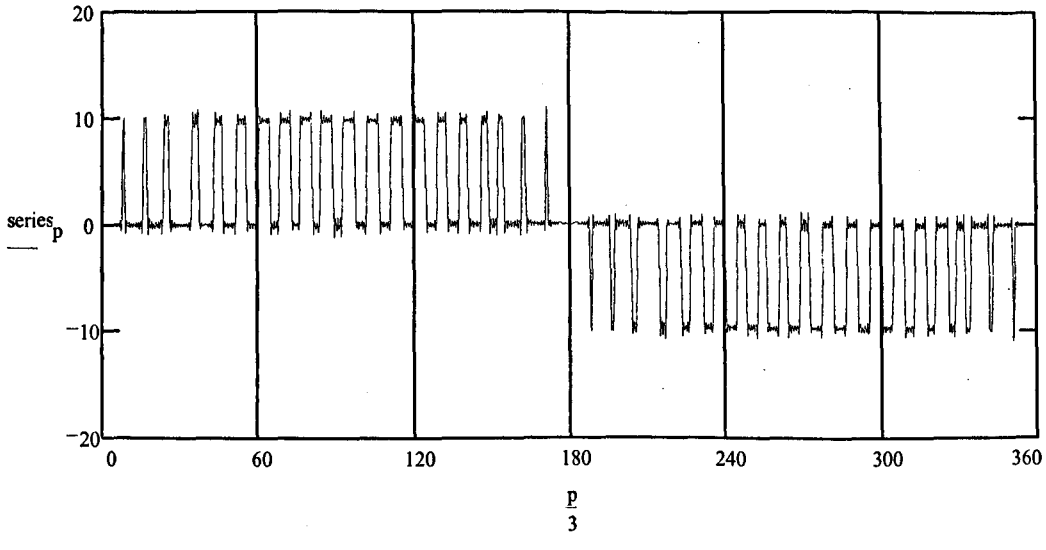


$c_{83} = 0.325$ $\quad c_{85} = 0.345$ $\quad c_{89} = 0.65$ $\quad c_{173} = 0.135$ $\quad c_{175} = 0.552$ $\quad c_{179} = 0.212$

$c_1 = 5.624$ $\quad c_5 = 0.367$ $\quad c_7 = 0.088$

$p := 0, 1 .. 1080$

$$series_p := \sum_n\left(a_n\cdot\cos\left(n\cdot\frac{p}{1080}\cdot w\right) + b_n\cdot\sin\left(n\cdot\frac{p}{1080}\cdot w\right)\right)$$



Appendix A7 - Effects of Flat-Top Phase Voltages on Currents

fharm4.mcd looks at what happens when a distorted mains voltage produces current harmonics from a fixed mod index and with a dc inductor
29/4/98

$b := 2\cdot\frac{\pi}{3}$ $c := 4\cdot\frac{\pi}{3}$ $M := 0.876$ $Vp := 150$ $R := 11.25$ $n := 0,1..60$ $Vout := \frac{3}{2}\cdot M\cdot Vp$

$wt := \frac{\pi}{3}\cdot\frac{1}{60}$ $q := 0,1..359$ $k := 0.85$ $h3 := 0$ $fs := 360$ $L := 100\cdot 10^{-3}$

$x := 1,2..60$

$Va_q := Vp\cdot\sin(q\cdot wt) + h3\cdot\sin(3\cdot q\cdot wt)$ $Vb_q := Vp\cdot\sin(q\cdot wt + b)$ $Vc_q := Vp\cdot\sin(q\cdot wt + c)$

$Va_q := if(Va_q > k\cdot Vp, k\cdot Vp, Va_q)$ $Va_q := if(Va_q < -k\cdot Vp, -k\cdot Vp, Va_q)$

$Vb_q := if(Vb_q > k\cdot Vp, k\cdot Vp, Vb_q)$ $Vb_q := if(Vb_q < -k\cdot Vp, -k\cdot Vp, Vb_q)$

$Vc_q := if(Vc_q > k\cdot Vp, k\cdot Vp, Vc_q)$ $Vc_q := if(Vc_q < -k\cdot Vp, -k\cdot Vp, Vc_q)$

$Vac_n := Va_n - Vc_n$

$Vbc_n := Vb_n - Vc_n$

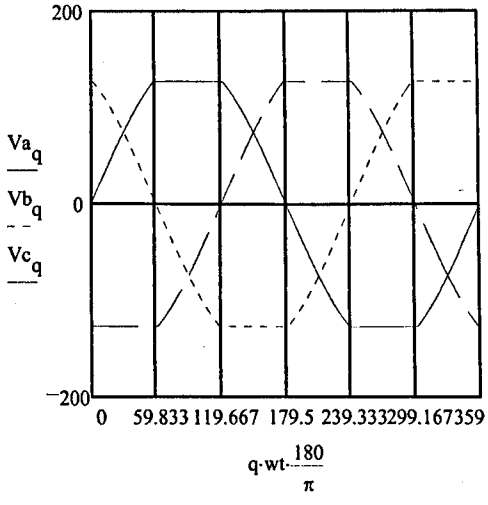
$m1_n := M\cdot\sin(n\cdot wt)$ $m2_n := M\cdot\sin(n\cdot wt + b)$

$Vout2_n := m1_n\cdot Vac_n + m2_n\cdot Vbc_n$

$Vav := \frac{1}{61}\cdot\sum_n Vout2_n$ $Idc_0 := \frac{Vav}{R}$

$Idc_x := \frac{1}{L}\cdot(Vout2_x - Vav)\cdot\frac{1}{fs} + Idc_{x-1}$

$Ia_n := Idc_n\cdot m1_n$



$n := 61,62..120$

$Vba_n := Va_n - Vb_n$

$Vca_n := Va_n - Vc_n$

$m1_n := |M\cdot\sin(n\cdot wt + b)|$ $m2_n := |M\cdot\sin(n\cdot wt + c)|$

$Vout2_n := m1_n\cdot Vba_n + m2_n\cdot Vca_n$

$Vav := \frac{1}{60}\cdot\sum_n Vout2_n$ $Idc_n := \frac{1}{L}\cdot(Vout2_n - Vav)\cdot\frac{1}{fs} + Idc_{n-1}$ $Ia_n := Idc_n\cdot(m1_n + m2_n)$

$n := 121,122..180$ $Vab_n := Va_n - Vb_n$ $Vcb_n := Vc_n - Vb_n$

$m1_n := |M\cdot\sin(n\cdot wt + c)|$ $m2_n := |M\cdot\sin(n\cdot wt)|$

$Vout2_n := m1_n\cdot Vcb_n + m2_n\cdot Vab_n$

$$Vav := \frac{1}{60}\cdot\sum_{n} Vout2_n$$

$$Idc_n := \frac{1}{L}\cdot\left(Vout2_n - Vav\right)\cdot\frac{1}{fs} + Idc_{n-1} \qquad Ia_n := Idc_n\cdot m2_n$$

$p := 0,1..180$ $\quad Vout = 197.1$ $\quad Idc_{p+179} := Idc_p$ $\quad ripplev := \max(Vout2) - \min(Vout2)$

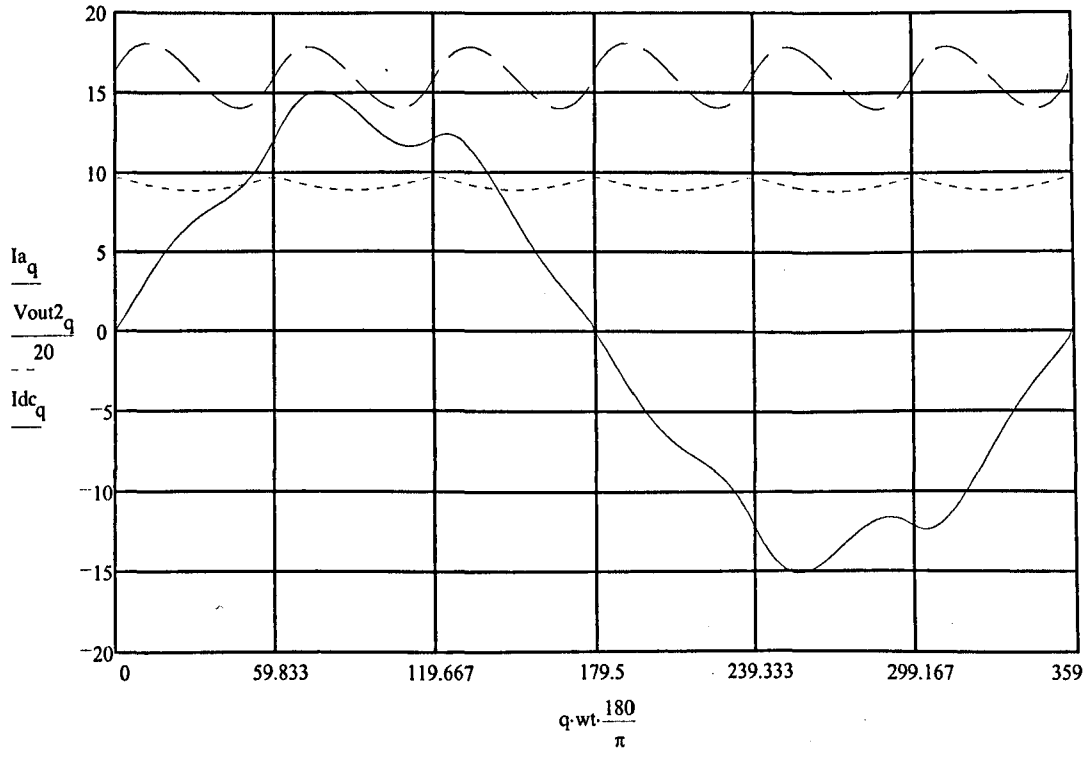
$$Ia_{p+179} := -Ia_p \qquad Vout2_{p+179} := Vout2_p \qquad Vout2av := \frac{1}{360}\cdot\sum_{q} Vout2_q \qquad Idcav := \frac{1}{360}\cdot\sum_{q} Idc_q$$

$length(Ia) = 360$ $\quad ripplei := \max(Idc) - \min(Idc)$

$ripplev = 16.073$ $\quad ripplei = 4.103$ $\quad Vout2av = 183.668$ $\quad Idcav = 15.986$

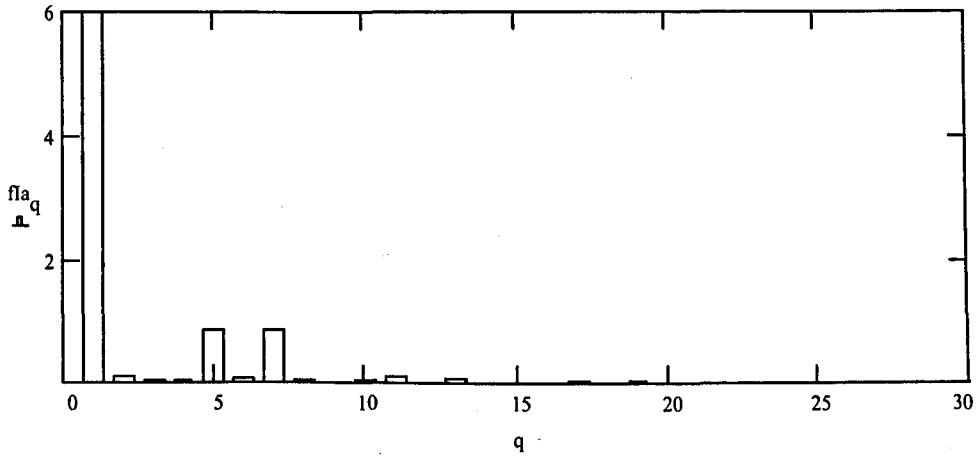
$length(Idc) = 360$ $\quad length(Vout2) = 360$

nb for cfft to work properly, total number of points should not be a prime number. This is why the data set is restricted to 360 points (0 to 359) instead of 361 (0 to 360). This avoids generating the spurious 20th harmonic seen when we have 361 points.



$fIa := 2 \cdot \overrightarrow{|(CFFT(Ia))|}$ Note use of CFFT rather than cfft. Difference is is scaling of amplitudes of frequencies.

$fIa_1 = 13.973$ $fIa_3 = 0.02$ $fIa_5 = 0.851$ $fIa_7 = 0.856$ $fIa_{11} = 0.089$ $fIa_{13} = 0.084$

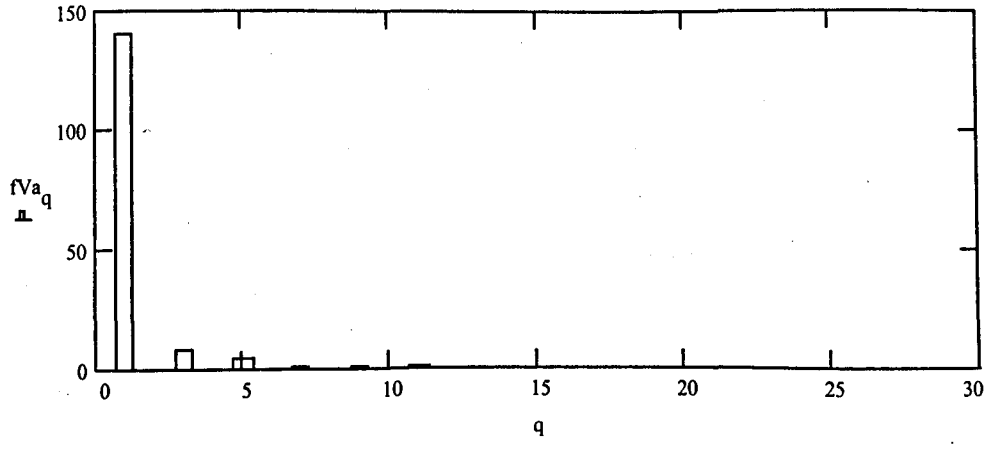


$n := 2,3..15$ $p := 1,2..15$

$$DF := \frac{100}{fIa_1} \cdot \left[\sum_p \left(\frac{fIa_p}{p^2} \right)^2 \right]^{\frac{1}{2}}$$ $DF = 100.001$ $$THD := \frac{100}{fIa_1} \cdot \left[\sum_n \left(fIa_n \right)^2 \right]^{\frac{1}{2}}$$ $THD = 8.738$

$fVa := 2 \cdot \overrightarrow{|(CFFT(Va))|}$ $length(Va) = 360$ $Va_{100} = 127.5$

$fVa_1 = 139.778$ $fVa_3 = 7.91$ $fVa_5 = 4.398$ $fVa_7 = 1.218$



$$DF := \frac{100}{fVa_1} \cdot \left[\sum_p \left(\frac{fVa_p}{p^2} \right)^2 \right]^{\frac{1}{2}}$$ $DF = 100.002$ $$THD := \frac{100}{fVa_1} \cdot \left[\sum_n \left(fVa_n \right)^2 \right]^{\frac{1}{2}}$$ $THD = 6.58$

Appendix A8 – MATLAB™ Finite DC Inductor Ripple Current

```
% \dan\cafi5.m
% M-file to create arrays of times and currents from 0-60 deg. for
% [c]entre [a]ligned pwm with [f]inite dc [i]nductor.
% Use with av5.m which takes cycle-by-cycle average over 180 deg. Use
% plot(t,u) to view switching current in dc link.
% 29/3/99

Vo=181;
R=20;
fs=1536;
T=1/fs;
% Switching period = 0.651ms (1536Hz). Therefore we have 1536/6=256 of
these periods in 60 deg.

w=2*pi;
% Mod. freqency = 1Hz

L=8e-3;
% scale dc inductor in real life (160uH) by 76.8kHz/fs Hz=50

M=0.577;
Vp=Vo/1.5/M;
k=0;
step=4;
kmax=fs/6*step;
% Each switching period is composed of six current up and down swings.
The times and currents are stored in fs*1 arrays

tb=M*T*sin(2*pi/3);
t(step-1)=0;
u(step-1)=Vo/R+0.5/L*Vo*(T/2+T/4-tb/2);
% Because matrix indicies of zero are not allowed, store the initial
time,current at this point in the matrix and step through in inc's of
six

for k=step:step:kmax

ta=M*T*sin(w*(k/step-1)*T);
tb=M*T*sin(w*T*(k/step-1)+2*pi/3);
% Compute switching times for two phases. (k/step-1) factor allows for
fact that we step through in 6 steps and thus as k goes 6,12,18.., the
k/step-1 value goes 1,2,3...

Va=Vp*sin(w*T*(k/step-1));
Vb=Vp*sin(w*T*(k/step-1)+2*pi/3);
Vc=Vp*sin(w*T*(k/step-1)+4*pi/3);

t(k)=(k/step-1)*T+T/4-ta/2;
t(k+1)=t(k)+ta;
t(k+2)=(k/step-1)*T+3*T/4-tb/2;
t(k+3)=t(k+2)+tb;

u(k)=u(k-1)*exp(-R/L*(t(k)-t(k-1)));
u(k+1)=ta/L*(Va-Vc-Vo)+u(k);
u(k+2)=u(k+1)*exp(-R/L*(t(k+2)-t(k+1)));
u(k+3)=tb/L*(Vb-Vc-Vo)+u(k+2);

end
end
```

```
% \dan\av5.m
% M-file to take results from cafi5.m m-file and average the inductor
% current over one switching cycle for entire 180 deg.
% Constants used; T, kmax, step are defined in cafi4.m. Use plot(tt,A)
% to observe averaged output.
% This version adds in ac filter phase shift caused by reactive
% current flow.
% 29/3/99

C=150e-6;
% scale 3uF input capacitor by 76.8kHz/fs=50

for k=step:step:kmax
% sum 0-60 average current
A(k/step)=0;
% otherwise A=A+e line doesn,t work
e(k/step)=0.5*(t(k+1)-t(k))*(u(k+1)+u(k));
% area=0.5*(sum of parallel sides)*distance between them
% Computes the area under one up/down swing of dc inductor current -
it's a trapezium
A(k/step)=e(k/step)/T+3*C*Vp*w*cos(w*T*k/(step));
% averages the area over each switching cycle
tt(k/step)=k/step*T;
end

for k=step:step:kmax
% 60-120 average current can be found using 0-60 dc link current
e(kmax/step+k/step)=e(k/step)+0.5*(t(k+3)-t(k+2))*(u(k+3)+u(k+2));
% adds phase 'a' current to phase 'b' current to get 60-120 current.
Result is stored in array starting from kmax
A(kmax/step+k/step)=e(kmax/step+k/step)/T+3*C*Vp*w*cos(w*T*(kmax/step+
k/(step)));
tt(kmax/step+k/step)=kmax/step*T+k/step*T;
% store the average and time values starting from kmax/step position
end

for k=step:step:kmax
% 120-180 average current
e(2*kmax/step+k/step)=0.5*(t(k+3)-t(k+2))*(u(k+3)+u(k+2));
% computes 120-180 phase current. Result is stored in array starting
from 2*kmax
A(2*kmax/step+k/step)=e(2*kmax/step+k/step)/T+3*C*Vp*w*cos(w*T*(2*kmax
/step+k/(step)));
tt(2*kmax/step+k/step)=2*kmax/step*T+k/step*T;
% store the average and time values starting from 2*kmax/step position
end

for k=1:1:kmax/4*3
% plot the current if dc inductor is infinite
B(k)=Vo*M/R*sin(w*T*k)+3*C*Vp*w*cos(w*T*k);
end
end
```

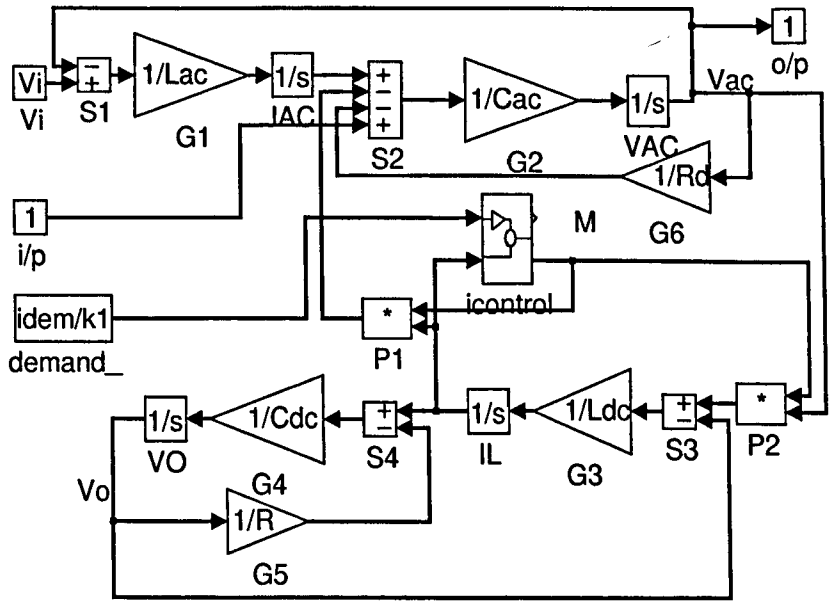
Appendix A9 – Switching Simulation M-File Parameters

```
% set-up variables for pwm.m
% pwm.m models standard converter with combined ac input filter
% and line-line pwm patterns
% 16/4/99

clear

res=50;                          %resolution of stored var's
variac=30;                       %reading from variac dial
Vp=variac/100*240*sqrt(2);       %peak supply-neutral volts
fltop=1;                         %set amount of flat-top. 1=none

k1=5;
k2=14;

demand1=9/k1;

%dc filter
Ldc=500e-6;
Cdc=4700e-6;
r1dc=0.2;
rcdc=0.1;
R1=14;
I1dcinit=demand1*k1;             %dc initial conditions
Vodcinit=I1dcinit*R1;
M=Vodcinit/(1.5*Vp);             %compute M from idemand & R1

%controller:- actual current demanded=demand*k1
kp=6;
fz=0;
wz=2*pi*fz;
ki=kp*wz;
kiinit=M*k2;
G1=1/3;

%ac filters
Lac=50e-6;
Cac=3e-6;
rc=0.1;                          %don't set too small else converge. prob
r1=0.2;

Ilacinit1=0;                     %ac initial conditions for L-L
Voacinit1=-sqrt(3)/2*Vp;         %voltages and phase currents
Ilacinit2=sqrt(3)/2*Ildcinit*M;
Voacinit2=sqrt(3)*Vp;
Ilacinit3=-Ilacinit2;
Voacinit3=Voacinit1;

%low-pass filter
Rf=10e3;
Cf=333e-12;
flpf=1/(2*pi*Rf*Cf);
wlpf=2*pi*flpf;
```

Appendix A10 – M-File to Plot il/demand Response with Input Filter

```
% m-file takes dc converter model, finds
% the dc operating point,
% linearises about this point and plots
% the il/demand.

variac=30;                              %reading from variac dial
Vp=variac/100*240*sqrt(2);              %peak supply-neutral volts
Vi=3/2*Vp;
Lac=2.75e-3*2;
Cac=3e-6*3/2;
Ldc=500e-6;
Cdc=4700e-6;
R=14;
Rd=10000;                               %small amount of damping
                                        %essential for good convergence
kp=3;
ki=0;
wlpf=1/(10e3*333e-12);
k1=5;
k2=14;
idem=7;
kiinit=idem*R/Vi*k2;

vac=Vi;
vo=idem*R;
m=vo/Vi;
iac=idem*m;

x0=[idem;vac;iac;vo];
u0=idem/k1;
y0=idem;
ix=[];
iu=[1];
iy=[];

[s,z0,xst]=dc;
opts=foptions;
opts(14)=500;
[x,u,y,dx]=trim('dc',x0,u0,y0,ix,iu,iy);
[a,b,c,d]=linmod('dc',x,u);
w=logspace(-2,6,500);
[mag,phase,w]=bode(a,b,c,d,1,w);

figure(1);
subplot(211);
semilogx(w,20*log10(mag));
grid
subplot(212);
semilogx(w,phase);
grid

figure(2);
%pzmap(a,b,c,d);
rlocus(a,b,c,d);
[w,e]=damp(a);
```

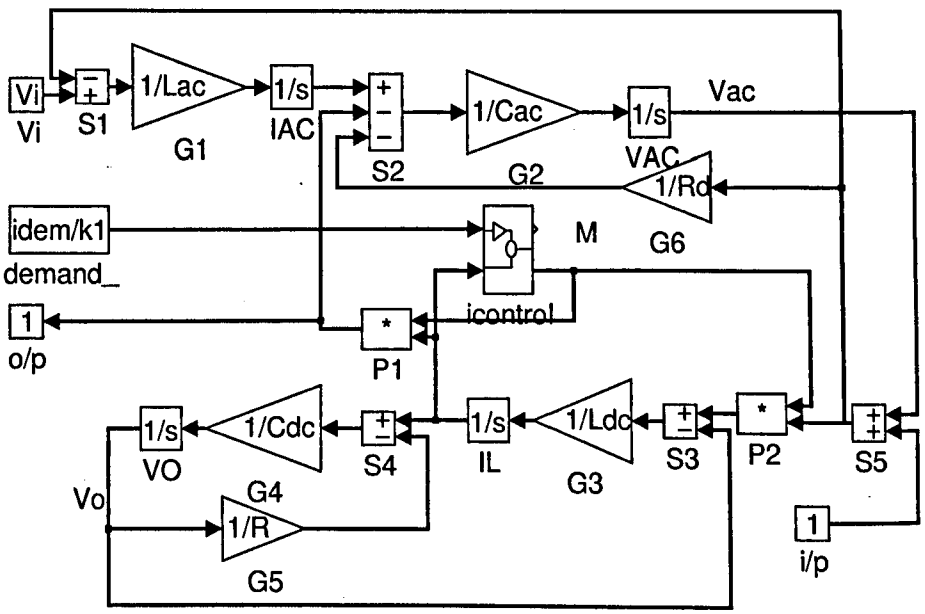
Appendix A11 – M-Files to Plot Impedance Criterion Responses



finds vac/io
use with drivdc6.m

```
% dc6.m m-file takes dc converter model, finds
% the dc operating point,
% linearises about this point and plots
% the il/demand.

variac=30;                          %reading from variac dial
Vp=variac/100*240*sqrt(2);          %peak supply-neutral volts
Vi=3/2*Vp;
Lac=2.75e-3*2;
Cac=3e-6*3/2;
Ldc=500e-6;
Cdc=4700e-6;
R=14;
Rd=50;                              %small amount of damping
                                    %essential for good convergence
kp=30;
ki=0;
wlpf=1/(10e3*333e-12);
k1=5;
k2=14;
idem=7;
kiinit=idem*R/Vi*k2;

vac=Vi;
vo=idem*R;
m=vo/Vi;
iac=idem*m;

x0=[vac;idem;iac;vo];
u0=0;
y0=vac;
ix=[];
iu=[];
iy=[];

[s,z0,xst]=dc6;
```

```
opts=foptions;
opts(14)=500;
[x,u,y,dx]=trim('dc6',x0,u0,y0,ix,iu,iy);
[a,b,c,d]=linmod('dc6',x,u);
w=logspace(-2,6,1000);
[mag,phase,w]=bode(a,b,c,d,1,w);

figure(1);
subplot(211);
semilogx(w,20*log10(mag));
grid
subplot(212);
semilogx(w,phase);
grid

%figure(2);
%pzmap(a,b,c,d);
%rlocus(a,b,c,d);
%[w,e]=damp(a);
```

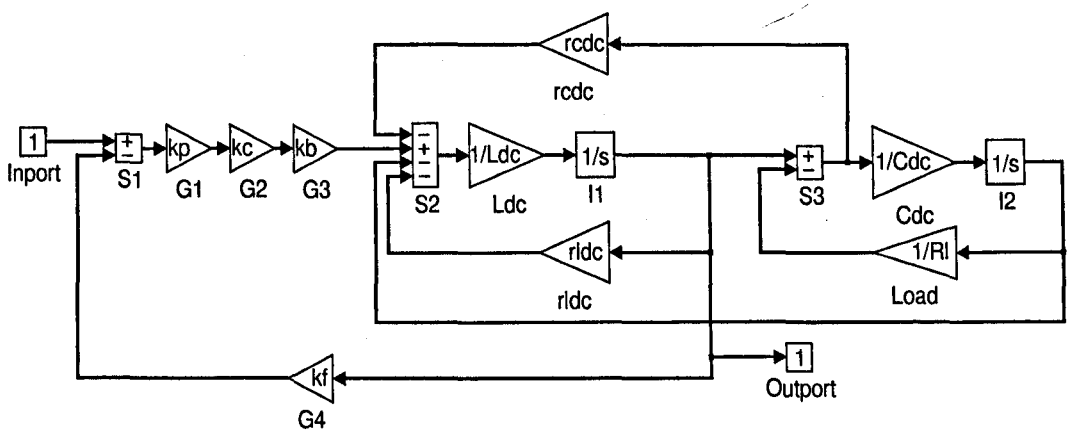


finds vac/io
use with drivdc7.m

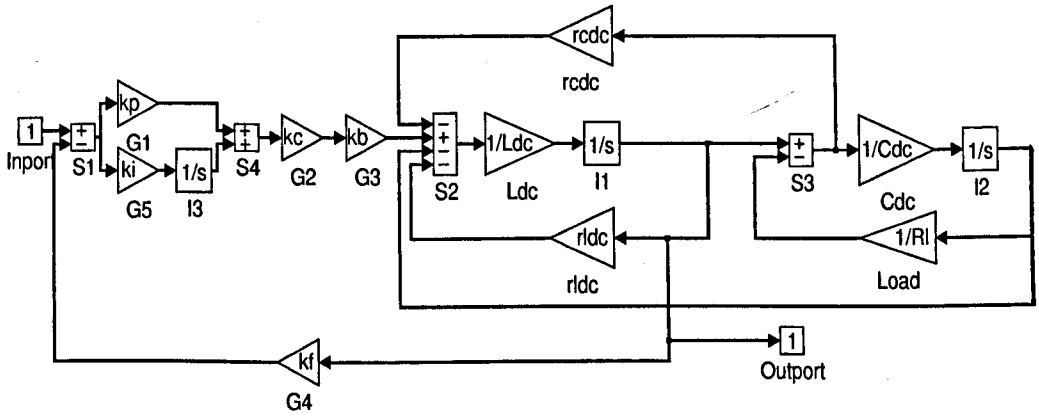
```
% dc7.m m-file takes dc converter model, finds
% the dc operating point,
% linearises about this point and plots
% the il/demand.

variac=30;                          %reading from variac dial
Vp=variac/100*240*sqrt(2);          %peak supply-neutral volts
Vi=3/2*Vp;
Lac=2.75e-3*2;
Cac=3e-6*3/2;
Ldc=500e-6;
Cdc=4700e-6;
R=14;
Rd=50;                              %small amount of damping
                                    %essential for good convergence
kp=30;
ki=0;
wlpf=1/(10e3*333e-12);
k1=5;
```

```
k2=14;
idem=7;
kiinit=idem*R/Vi*k2;

vac=Vi;
vo=idem*R;
m=vo/Vi;
iac=idem*m;

x0=[idem;vac;iac;vo];
u0=0;
y0=0;
ix=[];
iu=[];
iy=[];

[s,z0,xst]=dc7;
opts=foptions;
opts(14)=500;
[x,u,y,dx]=trim('dc7',x0,u0,y0,ix,iu,iy);
[a,b,c,d]=linmod('dc7',x,u,1);
w=logspace(-2,6,1000);
[num,den]=ss2tf(a,b,c,d,1);
%[mag,phase,w]=bode(a,b,c,d,1,w);
[mag,phase,w]=bode(den,num,w);          % Z=1/Y

figure(1);
subplot(211);
semilogx(w,20*log10(mag));
grid
subplot(212);
semilogx(w,phase);
grid

%figure(2);
%pzmap(a,b,c,d);
%rlocus(a,b,c,d);
%[w,e]=damp(a);
```

Appendix A12 – M-Files to Plot P and PI Controller Responses




```
%for use with linloo.m. Plots P Controller Bode of Linear Model

variac=30;
kp=3;
kc=1/(5.44*2.5);
kb=variac/100*240*sqrt(2)*1.5;
kf=1/5;

Ldc=500e-6;
Cdc=4700e-6;
rcdc=0.01;
rldc=0.1;
Rl=14;

demand=7;
x0=[demand;demand*Rl];
u0=[demand*kf];
y0=[demand];
ix=[];
iu=[1];
iy=[];
[x,u,y,dx]=trim('linloo',x0,u0,y0,ix,iu,iy)
[a,b,c,d]=linmod('linloo',x,u,0.1);

w=logspace(-2,8);
[mag,phase]=bode(a,b,c,d,1,w);
subplot(211);
semilogx(w,20*log10(mag));
subplot(212);
semilogx(w,phase);
```




```
%for use with linloo2.m. Plots Bode of PI controlled linear model

variac=30;
kp=3;
kc=1/(5.44*2.5);
kb=variac/100*240*sqrt(2)*1.5;
kf=1/5;
wz=300;
ki=kp*wz;

Ldc=500e-6;
Cdc=4700e-6;
rcdc=0.1;
rldc=0.5;
Rl=14;

demand=7;
x0=[demand;demand;demand*Rl];
u0=[demand*kf];
y0=[demand];
ix=[];
iu=[1];
iy=[];
[x,u,y,dx]=trim('linloo2',x0,u0,y0,ix,iu,iy)
[a,b,c,d]=linmod('linloo2',x,u);

w=logspace(-2,8);
[mag,phase]=bode(a,b,c,d,1,w);
subplot(211);
semilogx(w,20*log10(mag));
subplot(212);
semilogx(w,phase);
```

Appendix A13 - Perfect Correction of DC Inductor Current

fharm.mcd looks at what happens when a distorted mains voltage is corrected for by modulating the mod index,m, of m.sin(wt) in such a way as to create pure dc voltage. The mod index produced is m[n]. Includes a mod index clamp, maxm=1.0.
28/4/98

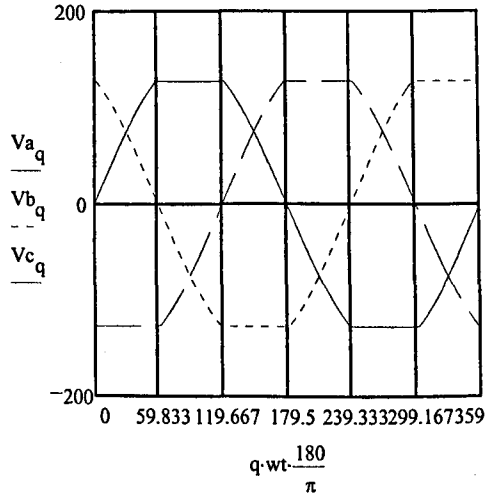
$b := 2\cdot\frac{\pi}{3}$ $c := 4\cdot\frac{\pi}{3}$ $M := 0.8$ $Vp := 150$ $R := 20.8$ $n := 0,1..60$ $Vout := \frac{3}{2}\cdot M\cdot Vp$

$wt := \frac{\pi}{3}\cdot\frac{1}{60}$ $Idc := \frac{Vout}{R}$ $q := 0,1..359$ $k := 0.85$ $h3 := 0$ $maxm := 1.0$

$Va_q := Vp\cdot\sin(q\cdot wt) + h3\cdot\sin(3\cdot q\cdot wt)$ $Vb_q := Vp\cdot\sin(q\cdot wt + b)$ $Vc_q := Vp\cdot\sin(q\cdot wt + c)$

$Va_q := \text{if}(Va_q > k\cdot Vp, k\cdot Vp, Va_q)$
$Vb_q := \text{if}(Vb_q > k\cdot Vp, k\cdot Vp, Vb_q)$
$Vc_q := \text{if}(Vc_q > k\cdot Vp, k\cdot Vp, Vc_q)$

$Va_q := \text{if}(Va_q < -k\cdot Vp, -k\cdot Vp, Va_q)$
$Vb_q := \text{if}(Vb_q < -k\cdot Vp, -k\cdot Vp, Vb_q)$
$Vc_q := \text{if}(Vc_q < -k\cdot Vp, -k\cdot Vp, Vc_q)$



$Vac_n := Va_n - Vc_n$ $Vbc_n := Vb_n - Vc_n$

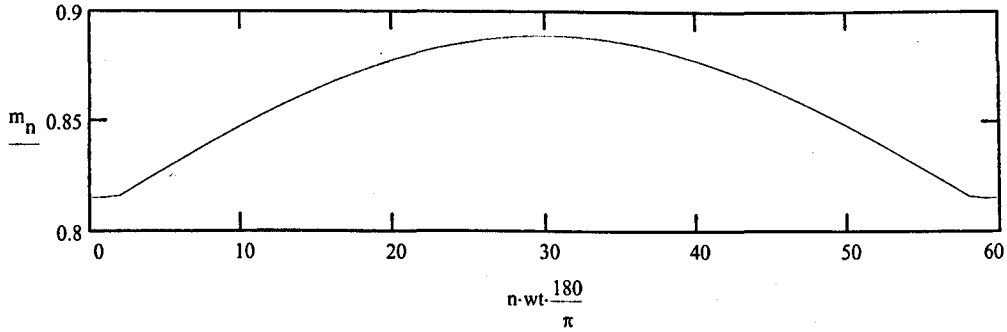
$m_n := \frac{Vout}{Vac_n\cdot\sin(n\cdot wt) + Vbc_n\cdot\sin(n\cdot wt + b)}$

$m_n := \text{if}(m_n > maxm, maxm, m_n)$

$m1_n := m_n\cdot\sin(n\cdot wt)$ $m2_n := m_n\cdot\sin(n\cdot wt + b)$

$Vout2_n := m1_n\cdot Vac_n + m2_n\cdot Vbc_n$

$Ia_n := \frac{Vout2_n}{R}\cdot m1_n$



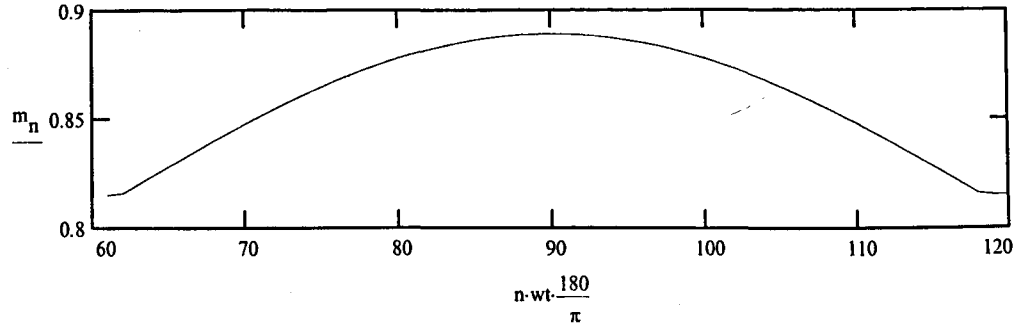
$n := 61,62..120$ WRITEPRN(m) := m_n

$Vba_n := Va_n - Vb_n$ $Vca_n := Va_n - Vc_n$

$m_n := \frac{Vout}{\left|Vba_n\cdot\sin(n\cdot wt + b) + Vca_n\cdot\sin(n\cdot wt + c)\right|}$

$m_n := \text{if}(m_n > maxm, maxm, m_n)$ $m1_n := \left|m_n\cdot\sin(n\cdot wt + b)\right|$ $m2_n := \left|m_n\cdot\sin(n\cdot wt + c)\right|$

$Vout2_n := m1_n\cdot Vba_n + m2_n\cdot Vca_n$ $Ia_n := \frac{Vout2_n}{R}\cdot(m1_n + m2_n)$



$n := 121, 122 .. 180$

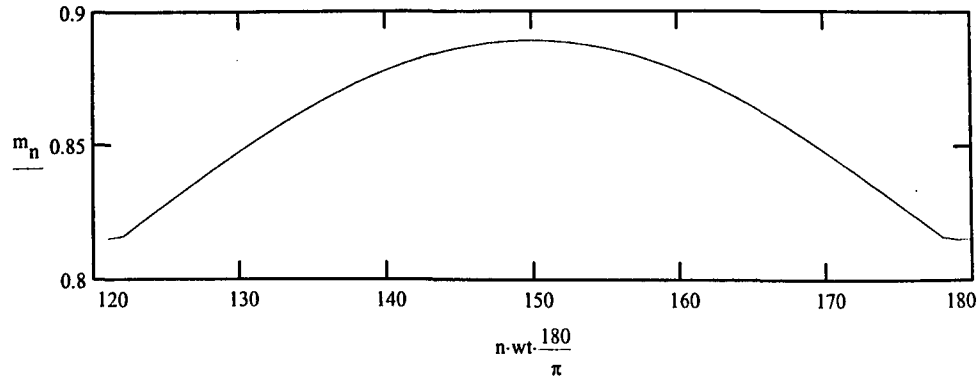
$Vab_n := Va_n - Vb_n \qquad Vcb_n := Vc_n - Vb_n$

$$m_n := \frac{Vout}{\left| Vcb_n \cdot \sin(n \cdot wt + c) + Vab_n \cdot \sin(n \cdot wt) \right|}$$

$m_n := if(m_n > maxm, maxm, m_n) \quad m1_n := \left| m_n \cdot \sin(n \cdot wt + c) \right| \quad m2_n := \left| m_n \cdot \sin(n \cdot wt) \right|$

$Vout2_n := m1_n \cdot Vcb_n + m2_n \cdot Vab_n$

$$Ia_n := \frac{Vout2_n}{R} \cdot m2_n$$

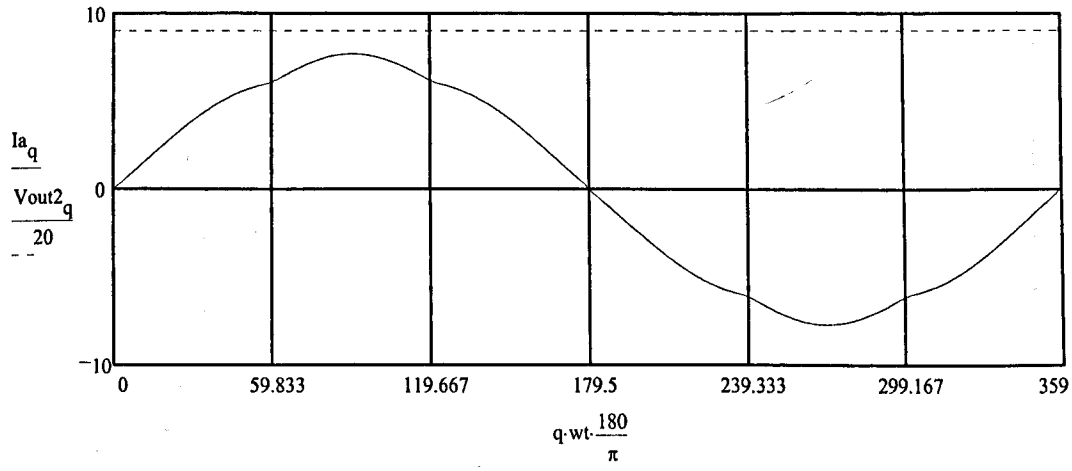


$p := 0, 1 .. 180 \quad length(Ia) = 181 \qquad Idc = 8.654$

$Ia_{p+179} := -Ia_p \quad Vout2_{p+180} := Vout2_p \quad Vout3 := \frac{1}{360} \cdot \sum_q Vout2_q \quad Vout = 180 \quad Vout3 = 180$

$ripplev := max(Vout2) - min(Vout2) \quad ripplev = 8.527 \cdot 10^{-14} \quad \frac{ripplev}{R} = 4.099 \cdot 10^{-15} \quad \frac{Vout3}{R} = 8.654$

nb for cfft to work properly, total number of points should not be a prime number. This is why the data set is restricted to 360 points (0 to 359) instead of 361 (0 to 360). This avoids generating the spurious 20th harmonic seen when we have 361 points.

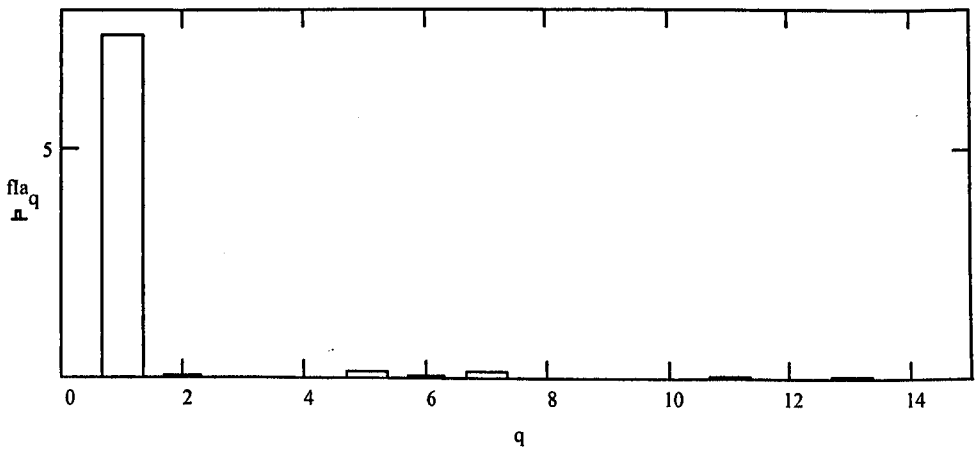


WRITEPRN(Ia) := Ia_q WRITEPRN(deg) := $q \cdot wt \cdot \frac{180}{\pi}$

Note use of CFFT rather than cfft. Difference is is scaling of amplitudes of frequencies. Still a factor of 2 is required to get answer that is sensible. Check:- when k=1, fIa(1)=5 Amps.

$fIa := 2 \cdot \overrightarrow{|(CFFT(Ia))|}$

$fIa_1 = 7.435$ $fIa_5 = 0.148$ $fIa_7 = 0.148$ $fIa_{11} = 0.027$ $fIa_{13} = 0.027$

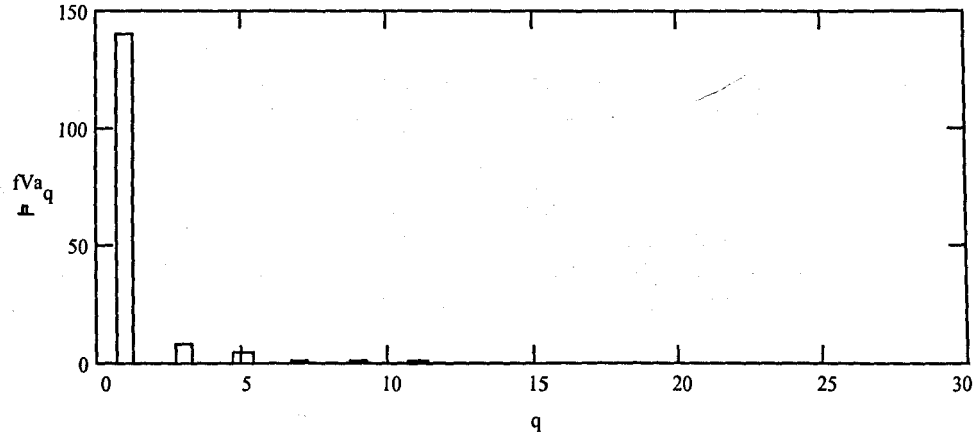


$n := 2,3..15$ $p := 1,2..15$ WRITEPRN(fIa) := fIa_q

$$DF := \frac{100}{fIa_1} \cdot \left[\sum_p \left(\frac{fIa_p}{p^2} \right)^2 \right]^{\frac{1}{2}} \qquad DF = 100 \qquad THD := \frac{100}{fIa_1} \cdot \left[\sum_n \left(fIa_n \right)^2 \right]^{\frac{1}{2}} \qquad THD = 2.99$$

$fVa := 2 \cdot \overrightarrow{|(CFFT(Va))|}$ length(Va) = 360 $Va_{100} = 127.5$

$fVa_1 = 139.778$ $fVa_3 = 7.91$ $fVa_5 = 4.398$ $fVa_7 = 1.218$



$$\text{WRITEPRN}(fVa) := fVa_{\blacksquare}$$

$$DF := \frac{100}{fVa_1}\cdot\left[\sum_p\left(\frac{fVa_p}{p^2}\right)^2\right]^{\frac{1}{2}} \qquad DF = 100.002 \qquad THD := \frac{100}{fVa_1}\cdot\left[\sum_n\left(fVa_n\right)^2\right]^{\frac{1}{2}} \qquad THD = 6.58$$

Appendix A14 – M-File for Damped Switching Simulation

```
% set-up variables for pwm.m
% pwm.m models standard converter with combined ac input filter
% this version caters for supply impedance and damping
% 16/4/99

res=10;                          %resolution of stored var's
variac=30;                       %reading from variac dial
Vp=variac/100*240*sqrt(2);       %peak supply-neutral volts
fltop=1;                         %set amount of flat-top. 1=none

k1=5;
k2=14;
k3=1/3;

demand1=4/k1;
demand2=8/k1-demand1;
tchange=8e-3;

%dc filter
Ldc=500e-6;
Cdc=4700e-6;
rldc=0.2;
rcdc=0.1;
Rl=14;
Ildcinit=demand1*k1;             %dc initial conditions
Vodcinit=Ildcinit*Rl;
M=Vodcinit/(1.5*Vp);             %compute M from idemand & Rl

%controller:- actual current demanded=demand*k1
kp=3;
fz=0;
wz=2*pi*fz;
wz=300;
ki=kp*wz;
kiinit=M*k2;
G1=1/3;

%ac filters
Lac=50e-6;
Cac=3e-6;
rc=0.1;                          %do not set too small
rl=0.2;

%supply impedance and damping
Lacd=2.25e-3/20;
rcd=15;                          %set high (1e6) to eliminate
rld=0.1;
Cacd=18e-6;                      %set low (1e-12) to eliminate

Ilacinit1=0;                     %ac initial conditions for L-L
Voacinit1=-sqrt(3)/2*Vp;         %voltages and phase currents
Ilacinit2=sqrt(3)/2*Ildcinit*M;
Voacinit2=sqrt(3)*Vp;
Ilacinit3=-Ilacinit2;
Voacinit3=Voacinit1;

%low-pass filter
Rf=10e3;
Cf=333e-12;
flpf=1/(2*pi*Rf*Cf);
wlpf=2*pi*flpf;
```

Appendix A15 – PSpice™ Dual Interleaved Converters

```
*unity power factor circuit, dual converters
.TRAN .15u 4.05m 4m 5U UIC
.OPTIONS ABSTOL 10UA VNTOL 100mV RELTOL=0.1 NUMDGT=8

*Converter #1
V1 1 0 SIN(0 240 50 0 0 0.0)
L1 1 9 50u
R1 9 10 0.75
C1 10 20 4u
D11 11 10 DIODE
D12 10 12 DIODE
S1 11 12 17 0 SSWITCH
D13 11 13 DIODE
D14 8 12 DIODE

V2 2 0 SIN(0 240 50 0 0 120.0)
L2 2 19 50u IC=1.4
R2 19 20 0.75
C2 20 30 4u IC=55
D21 21 20 DIODE
D22 20 22 DIODE
S2 21 22 27 0 SSWITCH
D23 21 13 DIODE
D24 8 22 DIODE

V3 3 0 SIN(0 240 50 0 0 240.0)
L3 3 29 50u IC=-1.4
R3 29 30 0.75
C3 30 10 4u IC=55
D31 31 30 DIODE
D32 30 32 DIODE
S3 31 32 37 0 SSWITCH
D33 31 13 DIODE
D34 8 32 DIODE

LR 13 18 500u IC=4.5
R4 18 15 0.5
LRR 14 25 500u IC=4.5
R44 25 8 0.5

RDUMMY1 16 0 .5
.INC "c:\mseval61\PWLFILE0.out"
RC1 17 0 1K

RDUMMY2 26 0 .5
.INC "c:\mseval61\PWLFILE1.out"
RC2 27 0 1K

RDUMMY 36 0 .5
.INC "c:\mseval61\PWLFILE2.out"
RC3 37 0 1K


*Converter #2
D111 111 10 DIODE
D121 10 121 DIODE
S11 111 121 171 0 SSWITCH
D131 111 131 DIODE
D141 81 121 DIODE

D211 211 20 DIODE
```

```
D221 20 221 DIODE
S21 211 221 271 0 SSWITCH
D231 211 131 DIODE
D241 81 221 DIODE

D311 311 30 DIODE
D321 30 321 DIODE
S31 311 321 371 0 SSWITCH
D331 311 131 DIODE
D341 81 321 DIODE

LR1 131 181 500u IC=4.5
R41 181 15 0.5
LRR1 14 251 500u IC=4.5
R441 251 81 0.5

RDUM3 161 0 0.5
.INC "c:\mseval61\PWLFILE3.out"
RC4 171 0 1k

RDUM4 261 0 0.5
.INC "c:\mseval61\PWLFILE4.out"
RC5 271 0 1k

RDUM5 361 0 0.5
.INC "c:\mseval61\PWLFILE5.out"
RC6 371 0 1k

*Common load
CR 15 14 2000u IC=175
RLOAD 15 14 20

.MODEL SSWITCH VSWITCH(VON=5, VOFF=2 RON=1)
.MODEL DIODE D(RS=1 CJO=0.1N)
*.PROBE i(lr) V(15,14) V(13,14) i(v1) i(v2)
.PROBE i(L1) i(LR) i(lrr) i(lr1) i(lrr1) v(13,8) v(131,81)
*.PROBE v(17,0) v(27,0) v(37,0) v(13,8) i(lr) i(11)
*.PRINT TRAN i(lr) i(lr1) i(lrr) i(lrr1) i(r1) v(13,8) v(131,81)
*.PROBE i(lr) i(lr1) i(lrr) i(lrr1) i(r1) v(15,14)
*.PROBE v(17,0) v(27,0) v(37,0) v(171,0) v(271,0) v(371,0)
.END
```

Appendix A16 – "C" Programmes for SSPWM

```
/*********************************************************************/
/* THIS ROUTINE PROVIDES A MAIN LINKING ROUTINE FOR THE PWM
MODULATION SIMULATION
The program generates three PWL files corresponding to the sinusoidal
SSPWM switching pattern.*/
/*********************************************************************/

#define MODULATION  (double)1/50 /*The modulation period*/
#define SAMPLE (float)1.0/76800.0 /*The switching period*/
#define NUM_CYCLES (int)2/*Number of modulation cycles*/
#define MOD_INDEX  (double)0.577

float t[10000];
void main()
{
double get_dec();
void wrt_pwl();
int pwm_mod();

int carrier;
int cycles=NUM_CYCLES;
double Tmod=MODULATION;
float Ts=SAMPLE;
double mod_index=MOD_INDEX;
double phase=0;
char name[]={'p','w','l','f','i','l','e','.','o','u','t'};
/*This subroutine generates the PWM times*/
carrier=pwm_mod(cycles,Tmod,Ts,mod_index, phase);

/*PWL file for phase 1 (+0)*/
wrt_pwl("PWLFILE6.OUT", carrier,t,Tmod,phase);
phase++;

/*PWL file phase 2 (+120)*/
carrier=pwm_mod(cycles,Tmod,Ts,mod_index, phase);
wrt_pwl("PWLFILE7.OUT", carrier,t,Tmod, phase);
phase++;

/*PWL file phase 3 (+240)*/
carrier=pwm_mod(cycles,Tmod,Ts,mod_index, phase);
wrt_pwl("PWLFILE8.OUT", carrier,t,Tmod,phase);
}
```

```
/*AUTHOR     :S.J.FINNEY modified D. J. TOOTH

FUNCTION     : This creates a time array of On anf Off times simulating
               a PWM signal.*/

#include<stdio.h>
#include<math.h>

extern float t[6000];

char pwm_mod(cycles,Tmod,Ts,mod_index,phase)
int cycles;
double Tmod;
float Ts;
double mod_index;
float phase;
```

```
{
FILE *fopen();
int fclose();

double cos(),sin();
double ang_freq,pi=(double)4*atan(1.0);
double Vc=(double)1,Vs;
int N=1,M=1, SN=1, i=0;
float P,rise,fall,Tcyc,Ton,Tovl;

/* the voltages are normalised to Vc=1 */
Vs=mod_index*Vc;
/* normalise the time period to 1 Hz */
Ts=Ts/Tmod;
Tmod=1;
ang_freq=(double)2*pi/Tmod;

M=cycles;
P=0.0;
Tovl=0.00002;
phase=phase*2*pi/3;  /*this selects the approriate phase*/

/*correct for the negative values*/
for(N=0;(N/2*Ts) < (M*Tmod);N=N+2)
{
P=(float)(N)/2.0;
      if( sin((P+4)*ang_freq*Ts+phase) < 0)
      {
       SN=-1;
      }
      else
      {
       SN=1;
      }

      if (SN*sin(ang_freq*(P+4)*Ts+phase) <= 0.5) /*short duration
                                                    pulse*/
      {
            for (i=1;i < 129;i++,N=N+2)      /*i.e. do i=1 to 128*/
            {
             P=(float)(N)/2.0;

            Ton=(float)(Ts*(Vs*SN*sin(P*ang_freq*Ts+phase)));
                  if ((N==0) && phase==0.0){
                   t[N+1]=-1*Ton; /*correct for starting condition on
                                    phase=0*/
                   t[N+1]=P*Ts-Ton;  /*ON time*/
                   t[N+2]=P*Ts+Tovl; /*OFF time with overlap*/
                   }
                  N=N-2; /*need to correct N at the end of each pi/6*/
            }
      else    /*long duration pulse*/
      {
            for (i=1;i < 129;i++,N=N+2)
            {
             P=(float)(N)/2.0;

             Ton=(float)(Ts*(Vs*SN*sin(P*ang_freq*Ts+phase)));
             t[N+1]=P*Ts;          /*ON time*/
             t[N+2]=P*Ts+Ton;      /*OFF time*/
            } /*for*/
       N=N-2;    /*correct N otherwise net effect is N=N+4*/
      }  /*if*/
```

```
}    /*Main FOR*/

return(N/2);
}
```

```
/*
AUTHOR :S.J.FINNEY

FUNCTION  : This file reads in the PWM switching times and writes then
            to a PWL file format.
*/

#include<stdio.h>
#include<math.h>

void wrt_pwl( f_name,length,c,Tmod, phase)

char f_name[];
int length;
float c[], Tmod ;
double phase;

{
FILE *fopen();
int fclose();
double pi=(double)4*atan(1.0);
FILE *stream, *stream2;
float T1,T2;
float Tr, Tmin , Tcyc;
int n, P1, P2;
int flag1=1;
int flag2=1;
int zero=0, dzero=1, P3=12;
Tr=  0.000001;
/* the rise time*/
Tmin=0.000002;
/* the MINIMUM on time */

stream=fopen(f_name,"w");
/*Piece wise linear file headers*/

if (phase==0) fprintf (stream,"V12 17 16 PWL(");
if (phase==1) fprintf (stream,"V22 27 26 PWL(");
if (phase==2) fprintf (stream,"V32 37 36 PWL(");
c[0]=0;
for(n=1;n<2*length;n=n+1)
{
/*This tests for the part of the cycle where the switch is always ON*/

      if( (sin(c[n]*2*pi+(phase*2*pi/3))>sin(pi/3))
        ||(sin(c[n]*2*pi+(phase*2*pi/3))<-sin(pi/3)) )
      {
       /* ON all the time*/
       P1=10;
       P2=10;

            if (flag1==1 && (n>1))    /*check for a phase changing from
                                        switching to on*/
            {
             T1=(c[n-1]+2*Tr)*Tmod;
             fprintf(stream," +%1.8f  %d \n ",T1,P3);  /*add a rise
                                                         time in*/
             flag1=0;
```

```
            flag2=1;
           }
      }
      else
      {
       /*switching*/
       P1=0;
       P2=10;
            if (flag2==1 && (n>1))     /*check for change from on to
                                         switching*/
            {
             T1=(c[n-1]+2*Tr)*Tmod;
             fprintf(stream," +%1.8f  %d \n ",T1, dzero);   /*add a
                                                    fall time in*/
             flag2=0;
             flag1=1;
            }
      }

 /*This writes the P1-P2 tranition to file*/
 T1=c[n]*Tmod;
 T2=(c[n]+Tr)*Tmod;
 fprintf(stream," +%1.8f  %d \n ",T1, P1);
 fprintf(stream," +%1.8f  %d  \n",T2, P2);
 n++;

 /*write P2-P1 transition to file*/
 T1=c[n]*Tmod;
 T2=(c[n]+Tr)*Tmod;
 fprintf(stream," +%1.8f  %d \n ",T1, P2);
 fprintf(stream," +%1.8f  %d \n ",T2, P1);
}
fprintf(stream, ")");
fclose(stream);
return;
}
```

Appendix A17 – "C" Programme for C167 μC SSPWM

```
/*
This program o/p's three phase pwm from three pwm counters P7.0=red,
P7.1=yellow, P7.2=blue. The pwm scheme used is overlapping pulses dead
banding type. P2.4 provides an o/p which is high if the 50Hz sync is
present. P7.3, the fourth pwm counter, provides the overlap pulses
which are OR'd with the normal pwm pulses. P2.1=red, P2.2=yellow, P2.3
=blue provide the phase select control to determine which phase has
the overlap pulses added to it.
*/

/*By D. J. Tooth Sept. 1995*/

#pragma SMALL   /*choose default memory model to be small*/
#pragma MOD167  /*use the extended c167 instruction set*/
#pragma CODE    /*add assembly code onto C program in the .lst file*/
#pragma DEBUG   /*include debug info. in .obj file*/
#include "c:\c166v2\inc\stdio.h"  /*general stuff*/
#include "c:\c166v2\inc\reg167.h"  /*c167 reg's and bit definitions*/

unsigned char huge *idata M0 = 0x4000;  /*huge as table > 16kB*/
unsigned int idata new_address=0;
unsigned int idata test=0;
unsigned char idata cycle_pos=0;    /*idata = store in uC's RAM*/
unsigned char idata inc_flag=0;
unsigned char idata leading=0;
unsigned char idata trailing=0;
unsigned int idata i=0;         /*char is 1 byte, int is 2 bytes*/
char bdata flag=1;


void main (void)
{

 IEN=0;    /*disable all interupts until set-up is complete*/

 BUSCON0 |= 0x2F; /*set number of wait states to zero i.e. 1X1111*/

 /*CAPCOM input/output 0 is set up to capture the 50Hz edges*/
 DP2_0=0;  /*set direction control to input*/
 T01CON=0x0B;  /*set counter mode and trigger on both edges*/
 CCM0=0x03;  /*select capture mode*/
 CC0IC=0x1C; /*re-set interrupt enable and set priority to 0111 00*/

 /*CAPCOM timer 7, pin7_7 set to produce 50Hz from 19.6608MHz clock*/
 DP8_7=1; /*pin 8_7 is CAPCOM register 23's o/p or i/p pin*/
 CC23=0xFFFF; /*ff40 set count value*/
 T7REL=0xFF42; /*set reload value to get 10ms before o/p is switched*/
 T7IC=0x0; /*disable timer 7 interrupt*/
 CC23IC=0x0; /*disable CAPCOM register 23 interrupt*/
 CCM5=0x5000; /*set to 0101&000000000000 = compare mode 1, Timer 7*/
 T78CON=0x47; /*T71=111 (/1024), T7M=0 (timer mode), T7R=1 (run)*/

 /*parllel ports set-up*/
 /*pins 2.1=r, 2.2=y, 2.3=b are enable pins for add-on o-lap pulses*/
 DP2_1=DP2_2=DP2_3=1;  /*set add-on pulse ports to output mode*/

 P2_4=0; /*set up LED o/p to show 50Hz sync*/
 DP2_4=1;
 P2_1=1;     /*set up sync o/ps*/
 P2_2=P2_3=0;
 DP2_6=DP2_7=1;
```

```
DP2_5=1;

/*set general pwm reg's, but don't start clks yet*/
PP0=PP1=PP2=PP3=0xFF;  /*period of carrier is (255+1)*50ns=78.25kHz*/
PW3=0x15;  /*set mod. level of ch.3*/
PWMCON1=0xF; /*i.e.PEN0=PEN1=PEN2=PEN3=1=enable all pwm o/p's*/
PW0=PW1=PW2=0x0; /*initial dummy values - keeps all o/p's=1*/
PWMIC=0x50;  /*enable overall interrupt amd set priority to 0100 00*/
DP7=0xF;  /*set direction of PWM port pins 0,1,2,3 to o/p mode*/
P7_3=1; /*set up ch.3 to be in inverted mode*/

/*set general ADC registers to read ch.0 once*/
ADCON=0xD000;  /*set conversion time to 11$01B, don't start convert*/
ADCIC=0x0;  /*disable conversion complete interrupt*/
ADEIC=0x0;  /*disable error interrupt*/
ADST=1;  /*start conversion*/

PTR3=1;  /*set pwm 3 carrier going*/
PWMCON0 |=0x7;  /*set pwm 0,1,2 carriers going clk=Tcpu*/

IEN=1;

CC0IR=0;
while (CC0IR == 0);  /*wait till 50Hz sync. arrives (start-up only)*/
CC0IR=0;
PIE0=1;   /*enable pwm 0 interrupt only*/

 while (1) /*loop forever*/
  {
    if ((flag==0) && (PIR0==1))
     {   /*only go to interrupt routine every 2nd interrupt request*/
      P2_6=flag=PIE0=1; /*saves time. The interrupt gen'd that does*/
      PIR0=P2_6=0; /*not result in the IR being jmp'd to is catered*/
      i++;  /* for by these instructions*/
     }
  } /*while*/
}  /*main*/


void pwm (void) interrupt 0x3F using PWM_BANK
{      /*'trailing' = this ch. is o/p' g small width pulses*/

 P2_6=1; /*sync pulse for logic*/

 trailing=M0[new_address+127-i]; /*start at end of table*/
 leading=M0[new_address+i]; /*start at beginning of table*/

  if (cycle_pos==0)   /*0 to 60 degrees*/
   {
    if (i < 64)
     {        /*red=leading, blue=trailing*/
      P2_2=0; /*need these next two lines as 50Hz sync may have*/
      P2_1=1; /*missed them out of 120 to 180 degrees routine*/
      PW1=0x100;  /*normally set by 120 to 180o routine*/
      PW2=trailing;
      PW0=0xFF-leading;
      PIR0=0;       /*'red phase, add-on o-lap pulses, enable pin=set*/
     }              /*we - 'leading' from PP0=255=0xFF*/
    else            /*n.b. should by 0x100 but to save time use 0xFF*/
     {  /*P2_1, P2_3 are reset/set now, doesn't take effect until*/
      P2_1=0; /*the next P2_6 +'ve edge reads values into latches.*/
      P2_3=1; /*enable PW2's add on pulses*/
      PW2=0xFF-trailing; /*M0 has base address = 0x4000 Accessing M0*/
      PW0=leading;       /*as array looks at the next address along*/
```

```
      PIR0=0;              /*and takes the value held at that location*/
     }
    }

  if (cycle_pos==1)    /*60 to 120 degrees*/
   {
    if (i < 64)
     {         /*yellow=trailing, blue=leading*/
      PW0=0x100; /*loading with zero forces next o/p to be high,*/
      PW1=trailing;  /*thus no need for PENx to be reset*/
      PW2=0xFF-leading;
      PIR0=0;
     }
    else
     {         /*yellow=leading, blue=trailing*/
      P2_3=0;
      P2_2=1; /*enable PW1's add on pulses*/
      PW2=leading;
      PW1=0xFF-trailing;
      PIR0=0;
      /*CC0IR=0;*/
      /*CC0IE=1;*/
     }
    }

  if (cycle_pos==2)    /*120 to 180 degrees*/
   {
    if (i < 64)
     {       /*red=trailing, yellow=leading*/
      PW2=0x100;  /*PW2 is 60o on, so load with 0 to force to on*/
      PW0=trailing;
      PW1=0xFF-leading;  /*yellow is leading hence shift by 255*/
      PIR0=0;
     }
    else
     {       /*yellow=leading, red=trailing*/
      P2_2=0;
      P2_1=1;
      PW1=leading;
      PW0=0xFF-trailing;
      PIR0=0;
     }
    }

 if (i==127)  /*reset to start of the table*/
  {
   i=0;        /*inc_flag will already be = 0 from previous statement*/
   cycle_pos++;
  }

 if (cycle_pos==3)
  {
   /*cycle_pos=0; reset to start; i and inc_flag are already =0*/
   cycle_pos=3;  /*make sure that if no 50Hz sync then we stick here*/
   PW0=PW1=PW2=0; /*set all final pwm o/p's low effectively*/
   P2_4=0;  /*reset 50Hz LED until sync arrives*/
   P2_1=0; /*reset this in case not done by previous statements*/
  }

  if (CC0IR==1) /*50 Hz sync. is done via polling*/
   {              /*doesn't matter if routine is 1 carrier period out*/
    cycle_pos=i=inc_flag=0;
    CC0IR=0;  /*reset interrupt flag and ignore further noise edges*/
    P2_4=1; /*set 50Hz sync present LED on*/
```

```
  }

 if (ADBSY==0)  /*i.e. ADC has finished conversion*/
  {            /*only read ADC when can be sure of no interruptions*/
   new_address=ADDAT & 0x3FC;/*and when ADC has finished converting*/
   new_address=new_address << 5; /*chop last two bits, shift 5 left*/
   ADST=1; /*begin a new conversion. As 0000000100 00000=128 bytes*/
  } /*only shift 5 places as lopping off 2 bits is a 2 bit shift*/

P2_6=PIE0=flag=0; /*reset o-lap enable / end of interrupt pin*/
/*disable interrupt so that IR will not be used next time PIR0=1*/

}  /*end of pwm interrupt*/
```

Appendix A18 – Explanation of the FTJ

The "jump", j, of a function g(x) at a point x_0 is defined as the difference between the right hand and left hand limits of g(x) at x_0, i.e.

$$j = g(x_0 + 0) - g(x_0 - 0) \tag{1}$$

An upward jump is positive and a downward jump is negative, Figure 1.

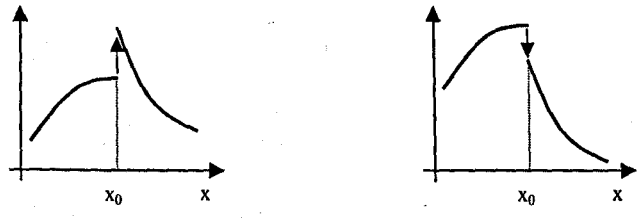


Figure 1 – Positive and Negative Jumps

For a derivation of the a_n and b_n coefficients jumps formulae, Equations (3.5) and (3.6) see Reference 3.5.

Example

The Fourier coefficients of the function shown in Figure 2 are to be found.

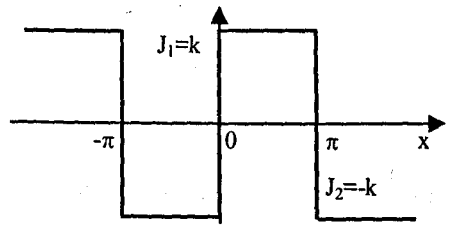


Figure 2 – Periodic Squarewave

The function is odd and has no dc component therefore $a_0=a_n=0$. In each period of the function there are two jumps of magnitude 2k and –2k. The derivatives of these two jumps are zero as they are constant and independent of x. From Equation (3.6) we get

$$b_n = \frac{1}{n\pi}[j_1\cos(nx_1) + j_2\cos(nx_2)] = \frac{1}{n\pi}[2k\cos(0) - 2k\cos(n\pi)] \tag{2}$$

Therefore $b_n\big|_{n=odd} = \frac{4k}{n\pi}$ and $b_n\big|_{n=even} = 0$ completely describe the b_n coefficients.

Appendix A19 - List of Figures

Chapter 1

Chapter 2

Chapter 4

Chapter 5

Chapter 6