Silicon Carbide Power Devices

Jue Wang

B.Sc.

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Heriot-Watt University

Department of Computing & Electrical Engineering

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ABSTRACT

Recently, Silicon Carbide has been widely recognised as a strong candidate for high temperature, high power and high frequency semiconductor devices as Si technology for power devices is approaching the limit determined by material properties. In this thesis, after establishing the physical models and material parameters for 6H-SiC and 4H-SiC, a systematic evaluation of SiC power devices from 1 kV to 10 kV is carried out by employing a two dimensional finite element semiconductor simulation package. Below 4 kV, 4H-SiC MOSFETs and BJTs show better current handling ability than IGBTs, GTOs and SIThs. Above 4 kV, SiC IGBTs are the best choice because they are easy to use and reliable, although their current handling ability is not as attractive as with SIThs and GTOs. The latter two have unfavourable application properties due to the relatively large SiC dopants' ionization energies.

Detailed investigation of the performance of SiC diodes (Schottky, PiN), MOSFETs, IGBTs and BJTs is undertaken. It is found that SiC devices with P^+ substrates are not favoured and complementary structures should be employed. Improvement in gate oxide technologies is necessary to realise the advantages of SiC UMOSFETs. The NPN BJT is shown to be a promising SiC device for evolution in the near future. Various structures for IGBTs (N-channel, P-Channel, Trench, Multiple Implantation, NPT, PT) are simulated, compared and analysed. An analytical closed-form solution is presented for 6H-SiC punch-through junction limited breakdown voltage.

Two analytical power PiN diode circuit simulation models are modified, validated and compared in PSpice. An analytical 6H-SiC PiN diode model is also developed in PSpice and challenges facing SiC device analytical modelling are discussed. A novel analytical Static Induction Thyristor (SITh) model based on device internal physics

operating mechanisms is proposed. The model exhibits accurate results, good convergence and fast simulation speed. A simple, unified voltage-controlled switch for PSpice to improve simulation speed and convergence is also proposed.

NOMENCLATURE

Symbol	Description
k	Boltzman constant
T	temperature
E_g	bandgap
$E_g(T)$	bandgap at temperature T
$E_g(300)$	bandgap at 300 K
N_c	effective density of states in the conduction band
N_v	effective density of states in the valence band
n_i	intrinsic carrier concentration
μ_n	low field electron mobility
μ_p	low field hole mobility
$\mu_{n,p}^{min}$, $\mu_{n,p}^{\delta}$, $N_{n,p}^{\mu}$, $\alpha_{n,p}$, $\gamma_{n,p}$	parameters in Eqn. (2.3)
μ_n^E	high field electron mobility
μ_p^E	high field hole mobility
E	electric field
v_s	saturation velocity
μ_{inv}	inversion layer mobility
$E_\perp$	electric field perpendicular to the current flow direction
R_{SRH}	Shockley-Read-Hall recombination-generation rate
τ_n	electron lifetime
τ_p	hole lifetime
n_{ie}	intrinsic carrier density taking into account the bandgap narrowing effect
N_D	donor density

N_A	acceptor density
n	electron concentration
p	hole concentration
R_{Au}	Auger recombination rate
G	generation rate of electron-hole pair
α_n	electron impact ionization rate
α_p	hole impact ionization rate
J_n	electron current density
J_p	hole current density
I_D	degree of ionization
$N_{D,A}^{+}$	ionizaed donor or acceptor density
E_{fn}	quasi fermi level for electron
E_{fp}	quasi fermi level for hole
E_D	donor energy level
E_A	acceptor energy level
χ	electron affinity
g_D, g_A	degeneracy factor
$R_{drift,sp}$	drift region specific on-state resistance
q	electric charge
V_{RT}	reach-through voltage
V_{PT}	punch-through junction breakdown voltage
β	$=V_{RT}/V_{PT}$
w	the drift region width
N	the drift region doping
ϵ_s	the dielectric constant

E_{crit}	the critical electric field
α_{eff}	effective impact ionization rate
V_f	forward voltage
J_f	forward current density
η	ideality factor
A^*	effective Richardson constant
Φ_{Bn}	barrier height
$R_{N-,mod}$	the modulated specific PiN diode drift region resistance
$R_{N+,sp}$	substrate specific resistance
V_{j1}	PiN diode P^+/N^- junction voltage
V_{j2}	PiN diode N^-/N^+ junction voltage
V_{bi}	built-in voltage
L_{ch}	MOS channel length
S	cell pitch
C_{ox}	MOS system gate oxide capacitance
V_{gs}	gate bias voltage
V_{th}	threshold voltage
V_b	breakdown voltage
V_{ds}	drain bias voltage
V_{ce}	collector bias voltage
BV_{ceo}	open-base blocking voltage
BV_{cbo}	open-emitter blocking voltage
t_{don}	turn-on delay time
t_{doff}	turn-off delay time
t_r	current rise time during turn-on

t_f	current fall time during turn-off
V_{on}	on-state voltage
E_{on}	turn-on loss
E_{off}	turn-off loss
N_a	doping level of P base in IGBTs
ε_{ox}	permittivity of silicon dioxide
V_{fp}	difference between Fermi level and intrinsic Fermi level
t_{ox}	thickness of silicon dioxide
V_{ms}	metal-semiconductor function difference
α_T	base transport factor
W_L	undepleted drift region width
L_e	the electron diffusion length in the drift region
D_e	electron diffusion coefficient
τ_0	carrier lifetime in lightly doped region
V_{on}, V_{off}, R_{on}, R_{off}	parameters in Eqn (8.1)
V_c	control variable in Eqn. (8.1)
R_s	switch resistance
T_j, T_c, T_a	junction, case and ambient temperature, Equation (7.1)
$R_{th,jc}$, $R_{th,ca}$	junction to case and case to ambient thermal resistance, Equation (7.1)
P_D	power loss of the device, Equation (7.1)
J_{fcm}	maximum continuous forward current density
E_{sw}	switching loss
t_{on} t_{off}	turn-on time, turn-off time
V_T	thermal voltage

ε_{si}	dielectric constant for Si
p_0	hole concentration at the emitter end of the base
p_w	hole concentration at the collector end of the base
p_{B0}	the equilibrium hole concentration in the base
N_B	base doping level
N_{epx}	the doping level of the base region between the gate and the cathode
Q_0	$qAp_0w/2\tau_a$
Q	base excess carrier charge
μ_n	electron mobility in the base
μ_p	hole mobility in the base
D_a	ambipolar diffusion coefficient, $2V_T\mu_n\mu_p/(\mu_n+\mu_p)$
τ_a	ambipolar lifetime
L_a	ambipolar diffusion length, $\sqrt{D_a\tau_a}$
b	μ_n/μ_p
w_B	base width
w	quasi-neutral base width
I_n	electron current
I_p	hole current
I_{n0}	electron current at the emitter end of the base
I_{nw}	electron current at the collector end of the base
I_{pw}	hole current at the collector end of the base
V_b	base ohmic voltage drop
V_{j1}	p^+ anode/N^- base junction voltage
V_{j2}	collector-base junction voltage
V_{j3}	p^+ gate/N base junction voltage

V_{j4}	N base/N^+ cathode junction voltage
V_{bi}	the built-in voltage of the collector-base junction
I_a	anode current
I_g	gate current
V_{ak}	anode-cathode voltage
V_{gk}	gate-cathode voltage
A	area

PREFACE

1. Scope of the work

Silicon Carbide is a wide bandgap semiconductor material having desirable properties ascribed to high thermochemical stability, high thermal conductivity, high saturation velocity of electrons and high breakdown electric field. Recently, significant improvements in SiC material growth and extremely attractive projections, stimulated renewed interest in SiC devices. Various small area Silicon Carbide devices have been demonstrated. It is generally expected that SiC devices will experience a rapid development in the next few years.

In this relatively new research area, many important questions remain unanswered. How do SiC devices compare quantitatively with established Si devices? What are the application ranges for different devices (diodes, BJTs, MOSFETs, IGBTs, GTOs, etc.)? What device type will evolve first according to the maturity of technology? What is the best structure for a specific device type? What unusual features will SiC devices exhibit due to their unique material properties? What device types will not be viable for SiC technology? What difficulties will there be in the modelling of SiC devices? Since the development of SiC technology is in its infancy, research work addressing these questions will provide invaluable information for SiC device development and its roadmap. This thesis aims at quantifying possible improvements to be made by this new material, as well as determining limitations, by carrying out a systematic investigation of SiC power devices. Device simulation is a powerful tool for obtaining reliable and quantitative semiconductor device information of semiconductor devices. After choosing appropriate physical models and material parameters to reflect SiC device properties, a numerical simulator is employed to achieve accurate results. The device structures are defined according to fabrication

technology and material limitations. Device performance is analysed and compared.

High-quality semiconductor device models for circuit simulation are required for prediction of circuit behaviour and computer-aided design (CAD) of power electronics systems. It is important to derive SiC device models for circuit simulations as the development of SiC device technology continues. A 6H-SiC analytical PiN diode model is developed in PSpice and problems facing SiC device modelling work are assessed. An analytical, non quasi-static Silicon Static Induction Thyristor (SITh) model is proposed and validated by comparison with experimental and numerical simulation results. This model can be extended to SiC. A new voltage-controlled switch model with improved convergence for PSpice is also presented. Two analytical power PiN diode models are implemented in PSpice, verified and compared.

2. Arrangement of the thesis

The thesis is divided into two parts: SiC power devices (Chapters one to seven) and analytical modelling of power devices (Chapters eight and nine). Chapter 10 forms the conclusion.

Chapter one provides a brief introduction to SiC technology. It summarises the history of SiC development, crystal structures and material properties, the current situation of material growth and device technologies.

Among three SiC polytypes of practical importance: 3C-SiC, 6H-SiC and 4H-SiC, the latter two have received the most attention for power devices. Hence, Chapter two describes physical models and material parameters for 4H-SiC and 6H-SiC used in numerical modelling of SiC devices in later chapters.

In Chapter 3, the 6H-SiC punch-through limited junction breakdown voltage is derived and is used to design soft recovery PiN diodes. The static and dynamic

performance of SiC Schottky diodes and PiN diodes is investigated. The electrical rating border between the unipolar diode and the PiN diode is derived.

Significant research effort has been devoted to the development of SiC MOSFETs. In Chapter 4, the maximum blocking voltage of 4H-SiC UMOSFETs versus the N^- drift region doping level, when accounting for insulator reliability, is obtained by numerical simulations. The performance of UMOSFETs, when accounting for the oxide reliability, are analyzed and compared with theoretical cases.

Chapter 5 and 6 consider 4H-SiC for BJTs and IGBTs, respectively. Various aspects of device performance are investigated and different structures are compared.

Chapter 7 is a comprehensive comparison and evaluation of SiC switching devices (MOSFETs, BJTs, IGBTs, SIThs and GTOs) with regard to thermal limitations. The performance of SiC devices from 1 kV to 10 kV is simulated for high power, high temperature and high frequency applications.

Chapter 8 begins with a brief introduction to the analytical modelling of semiconductor devices. Then two analytical PiN diode models are implemented in PSpice. Device modelling requirements for circuit simulations are highlighted by comparison of the two models. A PiN diode model for 6H-SiC is also developed and verified. Finally, a voltage-controlled switch model for PSpice is proposed.

In Chapter 9, a physically based Static Induction Thyristor (SITh) model is presented. It is accurate, computationally fast and exhibits good convergence.

Chapter 10 concludes the work presented in this thesis. The contributions made by the author are highlighted and future research work is suggested.

CHAPTER 1

INTRODUCTION

1.1 History of SiC development

As power electronics systems move to higher operating frequencies, higher temperature and higher voltages, demands for semiconductor devices with "ideal" characteristics have motivated continuous efforts in developing material technologies and novel device structures. Although the power semiconductor market is dominated by Si currently, Si technology is approaching the limit set by the physics laws. It is necessary to consider other materials if further improvements in device performance are to be realised. Recently, Silicon Carbide has been widely recognised as a strong candidate for high temperature, high power and high frequency semiconductor devices. In fact, it is not a new material. Acheson developed the electric smelting furnace to grow crystals around 1885 and gave this material the chemical formula SiC. Initially, Silicon Carbide was used as an abrasive and cutting material due to its excellent mechanical properties. It is not a natural mineral, hence techniques for growing high quality SiC crystals are required. As Schokley stated at the 1959 Silicon Carbide conference: "The SiC situation suffers from the very same thing that makes it so good. The bond is very strong so all the processes go on at high temperature..." [1.1]. Thus difficulties in fabricating SiC materials were met. SiC does not melt at atmospheric pressure, but it sublimes at a temperature above 1800°C. Based on this property, Lely proposed a sublimation process to provide large bulk SiC crystals in 1955, which aroused interest in using SiC as an electronic device material [1.2]. However, the most serious drawback of the Lely method is uncontrollable nucleation, which causes simultaneous growth of several SiC polytypes and only a small size crystal is obtained

(averagely 5×7 mm^2) [1.3]. In the 1960's and 70's, research activities in SiC were carried out mainly in the former Soviet Union. From 1978, a modified Lely method, also called the seeded sublimaition process, was developed by Tairov, Tsvetkov, Ziegler, et al. [1.4-1.6], which can also be applied to grow thin epitaxial films. Thus preparation of high quality SiC bulk crystal was possible. The availability of large area SiC wafers in conjunction with papers about the potential of wide bandgap semiconductors [1.7-1.9], renewed interests in SiC. Systematic studies in the field of SiC electronics have been undertaken from the late 1980's.

1.2 Silicon Carbide Crystal Structure and Properties

An unusual aspect of SiC is that it exhibits a form of one-dimensional polymorphism [1.10]. In SiC, a plane of close-packed Si atoms lies over a plane of close-packed C atoms, constituting a double layer of Si and C atoms. In each double layer, one Si atom lies directly over a C atom. The SiC polytypes differ from each other in the stacking sequence of the double layers. Only three possible relative positions, labelled A, B, and C, are allowed because double layers stack in a close-packed manner. Hence various cubic, hexagonal, or rhombohedral structures, are produced. The stacking direction is the c-axis in the hexagonal frame of reference.

Table 1.1 Examples of SiC Polytypes

	Ramsdell Notation	Stacking Sequence
Cubic or Beta	3C	ABCABC...
Alpha	6H	ABCACBABCACB...
	15R	ABCBACABACBCACB...
	4H	ABACABAC...
	2H	ABAB...

Examples of SiC polytypes are listed in Table 1.1. The most common way of designating the various structures is with the Ramsdell notation which is a number followed by a letter. The number is the number of double layers in the stacking repeat sequence and the letter designates the structure. 3C-SiC is the only cubic SiC, which is also called β-SiC. All of the other polytypes are know as α-SiC.

In Table 1.2 [1.10], properties of SiC are compared with diamond, GaP (two other contenders for high temperature semiconductor applications) and the two most commercially available semiconductors, Si and GaAs.

Table 1.2 Comparison of Semiconductor Properties

Properties	Si	GaAs	β-SiC	6H-SiC	4H-SiC	GaP	GaN	Diamond
Bandgap (eV) RT	1.1	1.4	2.2	2.9	3.3	2.3	3.5	5.5
Maximum operating temperature (°C)	300	460	873	1240	>1240	925	—	1100
Melting Point (°C)	1420	1238	sublimate > 1800			1470	—	phase change
Physical Stability	Good	Fair	Excellent			Fair	Very Good	Very Good
Breakdown Field E_b (10^6 V/cm)	0.3	0.4	2	3	3	—	3	10
Thermal Conductivity, σ_T, W/cm°C	1.5	0.5	3.3			0.8	0.6	20
Sat. Elec. Vel., 10^7cm/s	1	2	2	2	2	—	—	2.7
Dielectric Const.	11.8	12.8	9.7			5.5	9.5	11.1
Electron Mobility RT, cm^2/Vs	1400	8500	1000	370	720	350	900	2200
Relative JFOM	1	7	1100	1100	1100	—	—	8100
Relative KFOM	1	0.5	6	6	6	—	—	32
Relative BFOM	1	13.3	97.8	106.3	282.9	—	—	8574

In many applications, operating temperature (and sometimes radiation) approaches or exceeds limits of commercially available semiconductors. Long-term stability at high temperature will be a problem with common III-V compounds, such as GaAs and GaP [1.10]. Silicon Carbide has a significant advantage where long-term operating reliability at high temperature is a requirement. Silicon Carbide does not melt at any reasonable pressure, but it sublimates at temperatures greater than 1800°C. Below 1500°C, its physical stability is excellent and its stability in an oxidizing atmosphere gives it an edge over diamond.

SiC has extremely high thermal conductivity, can withstand high electric field before breakdown and can conduct high current densities. The wide bandgap results in a low leakage current, even at high temperature. Compared to Si, the high breakdown electric field strength permits one order of magnitude smaller drift region width and more than two orders of magnitude higher doping level of the drift region for a given blocking voltage. This results in a much lower specific on-state resistance for unipolar devices, and potentially lower resistances for high voltage bipolar devices.

The expected excellent performance of SiC devices is often expressed by figures of merit. Keyes' figure of merit (KFOM) [1.11] takes into account the switching speed of transistors and their thermal limitation due to generated heat that must be removed. Johnson's figure of merit (JFOM) [1.12] considers the high frequency and high power capability of transistors. Both indicate that SiC is an excellent material for high frequency devices. Baliga's figure of merit (BFOM) [1.7] considers the on-state resistance of power MOSFETs. From this figure of merit the excellent performance of high voltage unipolar devices in SiC can be deduced.

In addition, despite the differences with Si, their chemistry is similar, hence the exisiting processes for Si can be applied to SiC, with refinement. SiO_2 is the best insulator

so far. In SiC, SiO_2 can be grown on the Si layer by oxidation.

Other potentially important applications for SiC are light-emitting diodes (LEDs) and high frequency components. In the field of integrated circuits, NMOS circuits displaced TTL circuits, then CMOS circuits displaced NMOS circuits; both replacements occured because of decreased power consumption [1.13]. With SiC, its negligible reverse leakage currents and excellent thermal conductivity (three times that of Si) are invaluable for integrated circuit technologies.

1.3 SiC Material Growth Technologies

1.3.1 Crystal Growth

Physical vapour deposition via seeded sublimation has been the most investigated and successful technique for growth of SiC boules. Westinghouse (1995) has produced high resistivity <0001>-oriented 6H-SiC single crystals with diameters up to 75mm. 50 mm diameter 4H boules have been grown by Cree (1995). However, the micropipe defects (a small diameter hole in the material which may extend through the entire length of a boule) limit the active area size of devices, especially high current power devices. Recent results at Cree Research, including wafers with micropipe densities as low as 0.8 cm^{-2} on a 35 mm^2 wafer [1.14], indicate that micropipes will be reduced to a level that makes high current devices viable.

1.3.2 Epitaxy Growth

Chemical vapour deposition (CVD) remains the principle process route by which SiC films are deposited. The main mechanism of this method is step controlled CVD. This is based on using a SiC substrate misoriented by 3-4° off the <0001> basal plane toward the <1120> direction [1.15], [1.16]. 4H-SiC layers as thick as $100\mu m$ have been grown in

a hot-wall CVD reactor [1.17] at a growth rate of 3.5 μm/h.

1.4 SiC Device Technologies

1.4.1 Doping

Doping of SiC is accomplished in situ during epitaxy or ion implantation followed by high temperature annealing. Because of the very low diffusion coefficients of the impurities at temperatures when good surface morphology of SiC can be maintained, thermal diffusion doping of SiC is not possible. The lowest doping level of unintentionally doped epitaxial layers is $0.5\sim1\times10^{14}$ cm^{-3}. Vanadium ion implantation can successfully be applied to obtain semi-insulating properties [1.18]. C plus Al co-implantation for p-type doping reduces the specific contact resistance of Al ohmic contacts and enhances acceptor activation efficiency.

1.4.2 Ohmic Contacts

A low ohmic contact resistivity of 3.8×10^{-5} Ωcm^2 on p-type SiC has been obtained [1.19]. Nickel contacts reaching a low specific contact resistivity of 10^{-6} Ωcm^2 have been realised to highly n-doped 6H-SiC and 4H-SiC [1.20].

1.5 Conclusion

In this chapter, the history of SiC material development and structures of SiC polytypes were reviewed briefly. By comparing SiC properties with other semiconductors, its advantages for electronic devices can be appreciated. Aspects of the present situation in SiC material growth and device technologies have been summarised. With improvements in both wafer size and quality, fulfulling SiC's full potential for power conditioning and control can be expected in the near future.

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CHAPTER 2

PHYSICAL MODELS AND MATERIAL PARAMETERS FOR SIC DEVICE NUMERICAL MODELLING

The importance of simulations to the semiconductor industry has been recognised throughout the world [2.1]. By providing a description of the device and its operating conditions, a simulation can predict how the actual device would behave. Simulation results can often provide results with superior accuracy to 'closed-form' analysis for many semiconductor devices. Physically based numerical simulators are powerful tools to predict and investigate the performance of semiconductor devices. The Silvaco device simulation software package is employed [2.2] to investigate the performance of SiC devices. It calculates the electrical characteristics that are associated with specified physical structures and bias conditions, provides information that is difficult or impossible to measure and insight into the internal mechanisms related to device operation. This is achieved by defining a two or three dimensional device structure and approximating it onto a 2-D or 3-D grid, which consists of a number of nodes. By specifying material parameters, physical models and electrical bias conditions, the simulator applies a set of coupled, non-linear partial differential semiconductor physics equations (Poisson's equation, carrier continuity equations and drift-diffusion transport equations, etc.) to this grid. Therefore the transport of carriers through the structure is simulated. The simulator can model the electrical performance of a device in DC, AC or transient modes of operation. The simulation and experimental results in Figure 2.1 illustrate the simulator's accuracy [2.3].

BLAZE is a general purpose framework for compound semiconductors and devices with a position dependent band structure [2.2]. It employs models that stem from Si with

user-defined material parameters to simulate SiC devices. Anisotropies are not considered in this program. In order to achieve realistic results, it is imperative to choose proper models and material parameters. The completeness and accuracy of the models are by necessity tied to the maturity of material and device technologies and can only be improved with time. For the scope of the thesis, the current models are assumed to be adequate. In this chapter, the physical models and material parameters used for 6H-SiC and 4H-SiC are described.

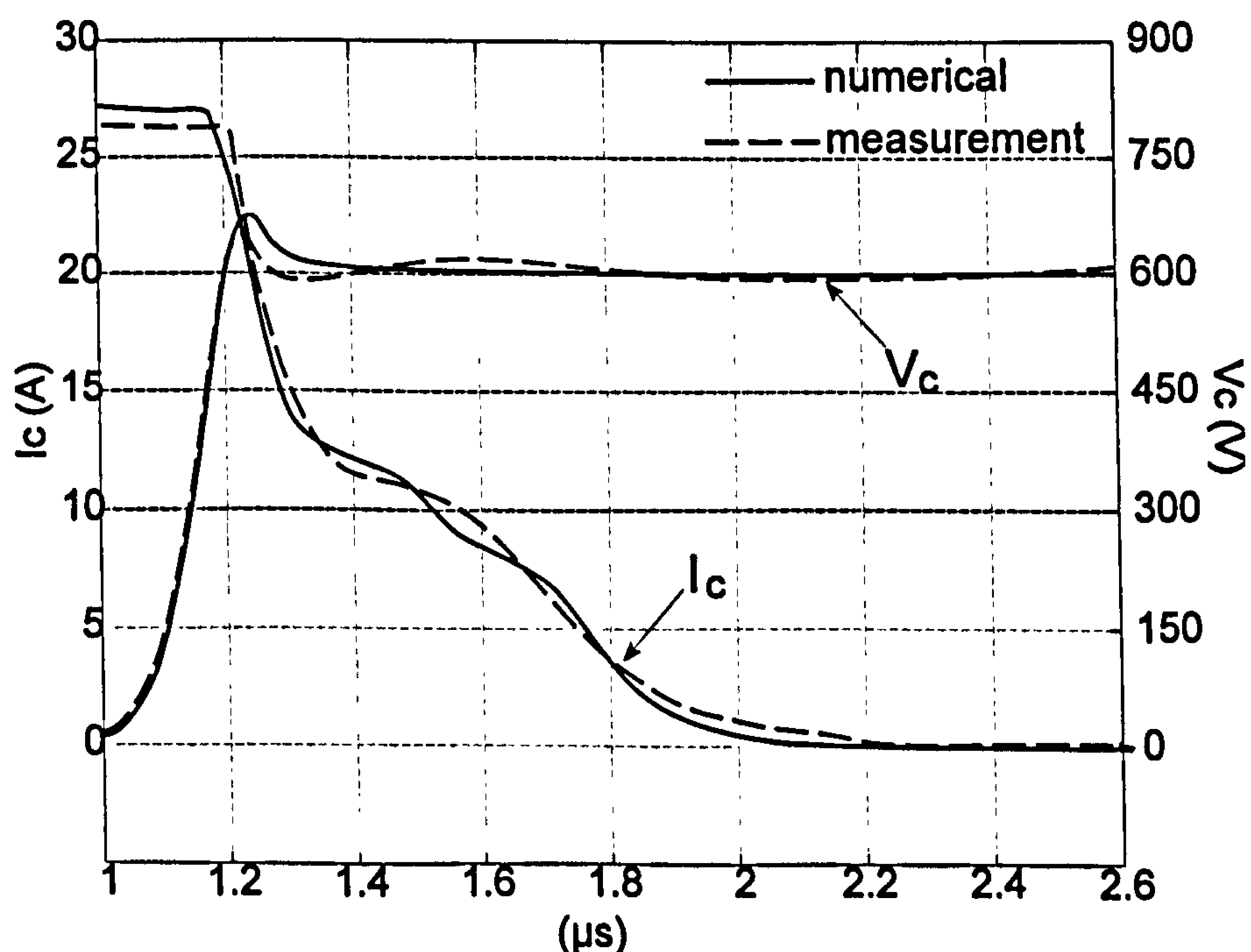

Figure 2.1 Comparison of numerical simulation result and experimental result of a Silicon IGBT turn-off characteristic

2.1 Bandgap E_g, Effective Densities of States in the Conduction Band (N_c) and Valence Band (N_v)

The 6H-SiC and 4H-SiC bandgaps E_g are measured as 2.9 eV [2.2] and 3.26 eV [2.4] respectively, at 300K. The 6H-SiC bandgap temperature dependence is taken from [2.5].

$$E_g(T)=E_g(300)-3.3\times10^{-4}(T-300) \quad \text{(eV)} \quad (2.1)$$

Since no reports exist for 4H-SiC bandgap temperature dependence, Equation (2.1) is also

applied to 4H-SiC.

The effective densities of states in the conduction band N_c and in the valence band N_v are set as 7.68×10^{18}cm^{-3} and 4.76×10^{18}cm^{-3} [2.2] for 6H-SiC and 4H-SiC. From Equation (2.2), the intrinsic carrier concentration n_i is 2.63×10^{-6}cm^{-3} and 2.49×10^{-9} cm^{-3} for 6H-SiC and 4H-SiC at 300 K respectively. These extremely low values of n_i cause convergence problems when simulating SiC devices.

$$n_i=\sqrt{N_c N_v}\exp(\frac{-E_g}{2kT}) \qquad (\mathrm{cm}^{-3}) \quad (2.2)$$

The bandgap narrowing (BGN) effect is important in highly doped regions. Due to the lack of a physical model for SiC, the BGN model and parameters for Si [2.2] are utilized when accounting for the BGN effect.

2.2 Mobility Modelling

2.2.1 Low-Field Mobility ($\mu_{n,p}$)

The low electric field mobility is modelled by the Caughey-Thomas equation [2.6]:

$$\mu_{n,p}=\mu_{n,p}^{min}+\frac{\mu_{n,p}^{\delta}*(\frac{T}{300})^{\alpha_{n,p}}}{1+(\frac{N_D+N_A}{N_{n,p}^{\mu}})^{\gamma_{n,p}}} \qquad (\mathrm{cm}^2/\mathrm{Vs}) \quad (2.3)$$

where N_D and N_A are local impurity concentrations. For 4H-SiC and 6H-SiC, the electron and hole mobilities in terms of doping and temperature have been measured [2.7]. By fitting with Equation (2.3), parameters $\mu_{n,p}^{min}$, $\mu_{n,p}^{\delta}$, $N_{n,p}^{\mu}$, $\alpha_{n,p}$, $\gamma_{n,p}$ are determined [2.7] and listed in Table 2.1.

2.2.2 High-Field Mobility ($\mu_{n,p}^{E}$)

At high electric field levels, the implemented model of the field dependent mobility

μ_E is given by [2.2]:

$$\mu_{n,p}^{E}=\mu_{n,p}\left(\frac{1}{1+\left(\frac{E*\mu_{n,p}}{v_s}\right)^{\beta}}\right)^{1/\beta} \qquad (cm^2/Vs) \quad (2.4)$$

with the low field mobility $\mu_{n,p}$ taken from Equation (2.3).

2.2.3 Saturation Velocity (v_s)

The 6H-SiC and 4H-SiC electron saturation velocities at 300 K are 2×10^7 cm/s [2.2] and 2.7×10^7 cm/s [2.8] respectively. The hole saturation velocity is assumed the same as the electron saturation velocity. The temperature dependence of the saturation velocity is accounted for as with Si [2.2]:

$$v_s(T)=\frac{v_s(0)}{1+0.8\exp(\frac{T}{600})} \qquad (cm/s) \quad (2.5)$$

The carrier-carrier scattering effect on moblity is not considered due to the lack of such data.

2.2.4 Inversion Layer Mobility (μ_{inv})

The physics of the SiC MOS surface still requires extensive investigation. Even in the field of Si MOS surface physics, there are some questions unresolved. Due to the lack of an inversion layer mobility model for SiC, the Shirahata inversion layer mobility model is used [2.2]. It takes into account screening effects in the inversion layer. In the simulations for the P base region of MOSFETs and IGBTs, it has an improved perpendicular field dependence for thin gate oxides.

$$\mu_{n,p,shi}=\frac{\mu_{n0,p0}}{(1+\frac{|E_\perp|}{E_1})^{P_1}+(1+\frac{|E_\perp|}{E_2})^{P_2}} \qquad (2.6)$$

The parameters μ_{n0} and μ_{p0} in Equation (2.6) are tuned to obtain a required average inversion layer carrier mobility, such as 100 cm^2/Vs at room temperature, which is measured with V_{gs}=15 V and V_{ds}=0.1 V for the N-channel MOSFET and IGBT.

2.3 Generation and Recombination

2.3.1 Shockley-Read-Hall Statistics and Low-Level Lifetime (R_{SRH}, τ):

The Shockley-Read-Hall (SRH) recombination-generation rate R_{SRH} is given by [2.2]:

$$R_{SRH}=\frac{np-n_{ie}^2}{\tau_p(n+n_{ie})+\tau_n(p+n_{ie})} \tag{2.7}$$

where n_{ie} is the intrinsic carrier concentration taking into account the bandgap narrowing effect, and n and p are local electron and hole concentrations respectively. The lifetime of electrons and holes, τ_n and τ_p, depend on doping level, as described by the Scharfetter relationship [2.2].

$$\tau_{n,p}(T)=\frac{\tau_{n0,p0}}{1+\left(\frac{N_D+N_A}{N_{n,p}^{SRH}}\right)^{\gamma_{n,p}}}\left(\frac{T}{300}\right)^{2.3} \quad \text{(s)} \tag{2.8}$$

Additionally, in the simulations the relation $\tau_{n0}=\tau_{p0}$ is used.

2.3.2 Auger Recombination (R_{Au})

Measurement data for Auger recombination rate R_{Au} [2.2] which is given by:

$$R_{Au}=(C_p p+C_n n)(np-n_{ie}^2) \tag{2.9}$$

can be found in [2.9] and [2.10]. However, these results differ from each other significantly ($2.5\sim3.5\times10^{-29}$ cm^6/s in [2.9] and $(7\pm1)\times10^{-31}$ cm^6/s in [2.10]). Hence, the parameters for Si are used to model the Auger Recombination process in SiC.

2.3.3 Impact Ionization (G)

The generation rate of electron-hole pairs due to impact ionization is modelled according to Selberherr [2.6]:

$$G=\alpha_n\frac{|J_n|}{q}+\alpha_p\frac{|J_p|}{q} \tag{2.10}$$

where J_n and J_p are electron and hole current densities respectively and α_n and α_p are the electron and hole ionization rates.

The Selbeherr model uses the following expression to describe the field dependence of the ionization rates[2.6]:

$$\alpha_{n,p}=a_{n,p}\exp(-\frac{E_{n,p}^{crit}}{|E|}) \tag{2.11}$$

Impact ionization in both SiC polytypes is dominated by holes, which attribute to the discontinuity of the conduction band for the electron momentum along the c-axis [2.11]. From avalanche ionization rate measurements, an average measured value for the 6H-SiC ionization rate is achieved [2.12]. The temperature dependence of $a_{n,p}$ and $E_{n,p}^{crit}$ are as for Si [2.2]:

$$\begin{aligned} a_{n,p}(T)&=a_{n,p}(0.412+0.588\frac{T}{300}) \\ E_{n,p}^{crit}(T)&=E_{n,p}^{crit}(0.752+0.248\frac{T}{300}) \end{aligned} \tag{2.12}$$

Up to date, only two sets of 4H-SiC avalanche ionization rate measurement values have been reported. Using the Van Overstraeten Equation: $\alpha=ae^{-b/E}$ (α is the effective impact ionization rate), a_p and E_p^{crit} are measured as $(3.5\pm0.5)\times10^6\,cm^{-1}$ and $(1.7\pm0.4)\times10^7$ V/cm respectively, for 4H-SiC at 300K [2.13]. However, no data for a_n and E_n^{crit} exists in the same publication [2.12]. In [2.11], the hole ionization rate along the c-axis in 4H-SiC is approximated by a theoretical relationship in the form suggested by Thornber [2.14], after fitting with measured data:

$$\alpha_p = c_1 E \exp(\frac{-c_2}{c_3 E^2 + c_4 E}) \qquad (2.13)$$

The electron ionization rates are given in the form of Equation (2.11). The results from [2.13] fall somewhere between α_n and α_p obtained from [2.11]. Since these two results do not correspond, the relationship given by Equation (2.12) is utilized to simulate 4H-SiC devices.

2.4 Incomplete Ionization

Unlike Si, the deep donor (E_D) and acceptor (E_A) levels in SiC lead to incomplete ionization of the impurities, even at higher temperatures.

The degree of ionization for electrons is described by [2.2]:

$$I_D = \frac{N_D^+}{N_D} = \frac{1}{1 + g_D \exp(\frac{E_{Fn} - E_D}{kT})} \qquad (2.14)$$

The corresponding equation is used for holes. In equation (2.14), E_{Fn} is the quasi-Fermi level and g_D is the degeneracy factor. For 6H-SiC and 4H-SiC, doping with N leads to a donor (substituting on a C-site) which has two different energy levels below the conduction band, because there are two C or (Si) sites, one with a cubic (k) surrounding and the other with a hexagonal (h) surrounding. Nitrogen atoms substituting on these sites therefore experience somewhat different surroundings, giving rise to different ionisation energies. The two donor levels (82 meV and 137 meV for 6H-SiC [2.15] and 52.1 meV and 91.8 meV for 4H-SiC [2.16]) can be lumped together and replaced by a single effective level E_D, using the following equation [2.17]:

$$\frac{0.5N_D}{1 + g_D \frac{n}{N_c} \exp(\frac{E_c - E_h}{kT})} + \frac{0.5N_D}{1 + g_D \frac{n}{N_c} \exp(\frac{E_c - E_k}{kT})} = \frac{N_D}{1 + g_D \frac{n}{N_c} \exp(\frac{E_c - E_D}{kT})} \qquad (2.15)$$

Single energy levels of 120 meV and 65 meV result for 6H-SiC and 4H-SiC respectively.

For Al acceptors in 6H-SiC, two ionisation energies of 0.22 eV and 0.25 eV are measured [2.18] because of the same structure reason. A single energy level of 0.23 eV is calculated using an equation similar to (2.15). Al acceptors in 4H-SiC should also in principle generate two different energy levels, however the difference seems to be too small to be readily detectable. According to [2.16], the ionisation energy is 0.191 eV.

2.5 Electron Affinity (χ)

The electron affinity, χ, the difference between the vacuum energy band and the conduction band, is 3.55 eV for 4H-SiC [2.19] and 3.7 to 3.8 eV for 6H-SiC at the Si-face [2.20]. This parameter is critical to the performance of Schottky diodes.

The surface potential-energy barrier height Φ_B is given by Φ_M-χ (Φ_M is the metal work-function). Using a different metal to form the Schottky contact results in different Φ_B, therefore, different device characteristics. In practice, there is an oxide layer with a thickness of 5-25 Å between the semiconductor and the metal. Due to the existence of the surface charge, the surface potential-energy barrier height is not a strict function of metal workfunction.

2.6 Conclusion

In this chapter, the physical models and parameters for the characterization of 6H-SiC and 4H-SiC devices have been described. The parameters are listed in Table 2.1. The most important models employed are for bandgap, mobility, generation and recombination, incomplete ionization and Schottky contact. With the continuing development of SiC technology, more accurate and complete physical SiC models will become available.

Table 2.1 6H-SiC, 4H-SiC and Si parameters used in device simulations

	6H-SiC	4H-SiC	Si
Dielectric Constant (ε)	9.66	9.66	11.8
Intrinsic Concentration			
n_i:			
E_g (T) (eV)	$2.9-3.3\times10^{-4}(T-300)$	$3.26-3.3\times10^{-4}(T-300)$	$1.17-7.02\times10^{-4}T^2/(T+108)$
N_C (300K) (cm^{-3})	7.68×10^{18}	7.68×10^{18}	2.8×10^{19}
N_V (300K) (cm^{-3})	4.76×10^{18}	4.76×10^{18}	1.04×10^{19}
n_i (300K) (cm^{-3})	2.63×10^{-6}	2.49×10^{-9}	1.5×10^{10}
Bandgap Narrowing:			
C_g (eV)	9×10^{-3}	9×10^{-3}	9×10^{-3}
N_{BGN} (cm^{-3})	1×10^{17}	1×10^{17}	1×10^{17}
Mobility μ^1:			
μ_n^{min} (cm^2/Vs)	0	0	92
μ_n^{δ} (cm^2/Vs)	415	947	1268
N_n^{μ} (cm^{-3})	1.11×10^{18}	1.94×10^{17}	1.3×10^{17}
γ_n	0.59	0.61	0.91
α_n	-2.07	-2	-2.42
μ_p^{min} (cm^2/Vs)	6.8	15.9	52
μ_p^{δ} (cm^2/Vs)	99	124	453
N_p^{μ} (cm^{-3})	2.1×10^{19}	1.76×10^{19}	1.9×10^{17}
γ_p	0.31	0.34	0.63
α_p	-2.5	-2.5	-2.2
V_{sn} (300K) (cm/s)	2×10^7	2.7×10^7	1×10^7
β_n	2	2	2
V_{sp} (300K) (cm/s)	2×10^7	2.7×10^7	1×10^7
β_p	1	1	1
p_{1n}	0.28	0.28	0.28
p_{2n}	2.9	2.9	2.9
p_{1p}	0.3	0.3	0.3
p_{2p}	1.0	1.0	1.0
E_{1n} (V/cm)	8.9×10^3	8.9×10^3	8.9×10^3
E_{2n} (V/cm)	1.22×10^6	1.22×10^6	1.22×10^6

Table 2.1 (Cont.)

		6H-SiC	4H-SiC	Si
E_{1p}	(V/cm)	8.0×10^3	8.0×10^3	8.0×10^3
E_{2p}	(V/cm)	3.9×10^5	3.9×10^5	3.9×10^5
Shockley-Read-Hall lifetime:				
N_n^{SRH}	(cm^{-3})	5×10^{16}	5×10^{16}	5×10^{16}
γ_{ns}		1	1	1
N_p^{SRH}	(cm^{-3})	5×10^{16}	5×10^{16}	5×10^{16}
γ_{ps}		1	1	1
Auger Recombination:				
C_n	(cm^6/s)	8.3×10^{-32}	8.3×10^{-32}	8.3×10^{-32}
C_p	(cm^6/s)	1.8×10^{-31}	1.8×10^{-31}	1.8×10^{-31}
Impact Ionization:				
a_n	(cm^{-1})	1.66×10^6	1.66×10^6	7.03×10^5
E_n^{crit}	(V/cm)	1.273×10^7	1.273×10^7	1.231×10^6
a_p	(cm^{-1})	5.18×10^6	5.18×10^6	1.582×10^6
E_p^{crit}	(V/cm)	1.4×10^7	1.4×10^7	2.036×10^6
Incomplete Ionization				
E_D	(meV)	120	65	44
g_D		2	2	2
E_A	(meV)	230	191	45
g_A		4	4	4

[1]Perpendicular to C-axis

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CHAPTER 3

SIC SCHOTTKY AND PIN DIODES

High voltage diodes are needed for many power electronic applications, such as motor control. There is a general trend towards higher operating frequencies in power systems due to a resultant reduction in the size of passive components and an increase in system efficiency. These circuits require diodes with fast switching speeds and low switching and on-state losses.

The use of the Schottky Barrier Diode (SBD) is attractive in order to improve switching performance and reduce power consumption. However, the series resistance of the N^- drift region increases with breakdown voltage and temperature, which in turn increases the on-state voltage. The performance of Si SBDs with blocking voltages of over 100 V is intolerable. Most high voltage systems utilize the P-i-N rectifier structure. These devices are available with blocking voltages in excess of 5 kV. The primary drawback is the large reverse recovery current during switching from the on-state to the reverse blocking state, due to the large stored charge in the drift region. The reverse recovery phenomena of power diodes contributes a large part to the switching losses, therefore diode trade-offs are of great interest. Many methods and structures have been proposed in order to improve diode properties:

a) merged PiN/Schottky structure (MPS)

b) uniform lifetime control and profiled lifetime control using electron or proton irradiation

c) hybrid diodes-combining two diodes with different recovery behaviours

d) a diode with a third terminal to control the injection of stored charge.

However, these devices can not be considered as ideal for power switching because they still exhibit a substantial reverse recovery transient. Today's best diodes are not far short of theoretical performance limits determined by modern simulation tools. The diode is a performance limiting element in many high voltage circuits. It often sets the limits on how fast the switching devices can be operated, since the switching deficiencies of the diode are generally transferred to the main switching device as losses.

For the same blocking voltage, SiC devices have a 10 times thinner drift region and 100 times higher drift doping level than corresponding Si devices. For Schottky diodes, this means a much lower N^- region series resistance, therefore the voltage and temperature application ranges of SiC Schottky diodes are projected to be greatly expanded compared to their Si counterparts. For PiN diodes, this results in significantly reduced stored charge, hence the reverse recovery current is expected to be much smaller.

6H-SiC has received considerable attention for SiC high power device application since it has the best crystal quality. On the other hand, 4H-SiC has been regarded as the most promising SiC polytype for power devices because its electron mobility perpendicular to the c-axis is about ten times that of 6H-SiC with low doping and its bandgap (3.26 eV) is wider than that of 6H-SiC (2.9 eV) [3.1]. 4H-SiC is an apparently better choice for unipolar devices because their on-state voltages mainly depend on the drift region specific resistance, which is given by $R_{drift,sp}=w/q\mu N_{drift}$. The higher 4H-SiC electron mobility generates a lower drift region resistance. However for bipolar devices, the wider bandgap of 4H-SiC results in a larger P^+/N^- junction voltage, which contributes to the on-state voltage. Consequently, whether 6H-SiC or 4H-SiC is more suitable for bipolar devices needs further investigation.

Several SiC Schottky Barrier and PiN diodes have been demonstrated [3.2] - [3.11]. Diode failure mechanisms and diode characteristics have also been investigated [3.12] -

[3.17].

A punch-through structure is often utilised to reduce the drift region specific on-resistance when designing a bipolar device. In this chapter, a closed-form analytical solution for SiC punch-through limited junction breakdown voltage, is presented. The solution can be used to readily calculate 6H-SiC punch-through diode breakdown voltages, with the accuracy of numerical simulation. Then 6H-SiC and 4H-SiC diode performance are evaluated and compared with numerical simulation. The application range of SiC SB and PiN diodes are subsequently determined.

3.1 An Analytical Solution for SiC Junction Punch Through Limited Breakdown Voltage

3.1.1 The Solution

An analytical expression for the Si based critical electric field parallel-plane junction punch-through limited breakdown voltage has been derived [3.18], which introduces significant error, especially when the epitaxial-layer thickness is thin. Numerical calculations of the punch-through parallel-plane junction breakdown voltage based on ionization rates is time-consuming. Recently, a closed-form analytical expression for the silicon PT limited breakdown voltage based on ionization rate integration was reported [3.19]. In this section, an analytical solution for 6H-SiC junction punch-through breakdown voltage is derived.

By defining a parameter $\beta = V_{RT}/V_{PT}$ (V_{RT} is the reach-through voltage, the voltage when the depletion layer just extends to the i/N+ junction and V_{PT} is the junction PT limited breakdown voltage), the following equations apply when diode reach-through and avalanche breakdown occur respectively, provided the P^+/N^- junction is an abrupt junction:

$$\frac{1}{2}\frac{qNw^2}{\epsilon_s}=\beta V_{PT} \tag{3.1}$$

$$E_{crit}w-\frac{1}{2}\frac{qNw^2}{\epsilon_s}=V_{PT} \tag{3.2}$$

where: E_{crit} the critical electric field

w the drift region width

N the drift region doping

ϵ_s the dielectric constant.

Combining Eqns. (3.1) and (3.2) generates a critical electric field expression:

$$E_{crit}=\frac{1+\beta}{\sqrt{\frac{2\beta\epsilon_s}{qN}}}V_{PT}^{0.5} \tag{3.3}$$

While breakdown occurs, assuming the axis origin is at the P^+/N^- junction, the electric field in the drift region is described by:

$$E(x)=E_{crit}-\frac{qN}{\epsilon_s}x \tag{3.4}$$

An approximate form of ionization rates α_n and α_p is $\alpha_{eff}=\alpha_n=\alpha_p=aE^b$, where a and b are parameters reflecting the properties of semiconductor materials. Using this expression and solving the breakdown condition $\int_0^w \alpha_{eff}dx=1$, a general expression of the base width w in terms of base doping N is derived:

$$w=\frac{2\beta}{[(1+\beta)^{b+1}-(1-\beta)^{b+1}]^{\frac{1}{b+1}}}(\frac{b+1}{a})^{\frac{1}{b+1}}(\frac{\epsilon_s}{q})^{\frac{b}{b+1}}N^{-\frac{b}{b+1}} \tag{3.5}$$

For 6H-SiC, the ionization rate expressions are shown in Equation (2.11) and Table 2.1. By fitting to numerical simulation results, a and b are 1.256×10^{-41} and 7 for $\alpha_{eff}=aE^b$ respectively. From Equation (3.5), an approximation solution of β $(0<\beta\leq1)$ is obtained:

$$\beta=1.221-\sqrt{1.525-1.502c} \tag{3.6}$$

with $c=7.72\times10^{-12}wN^{\frac{7}{8}}$.

Hence, given a base width w and doping N, the punch-through limited breakdown voltage V_{PT} is computed from Equation (3.6) and $V_{PT}=V_{RT}/\beta$ (for $V_{RT}=\frac{1}{2}\frac{qN}{\epsilon_s}W^2$).

To verify the accuracy of Equation (3.6), numerical simulation results are compared with analytical results in Figure 3.1. The analytical results correspond well with the numerical simulation results. The same procedure can also be applied for deriving PT diode breakdown voltages for devices fabricated with other semiconductors.

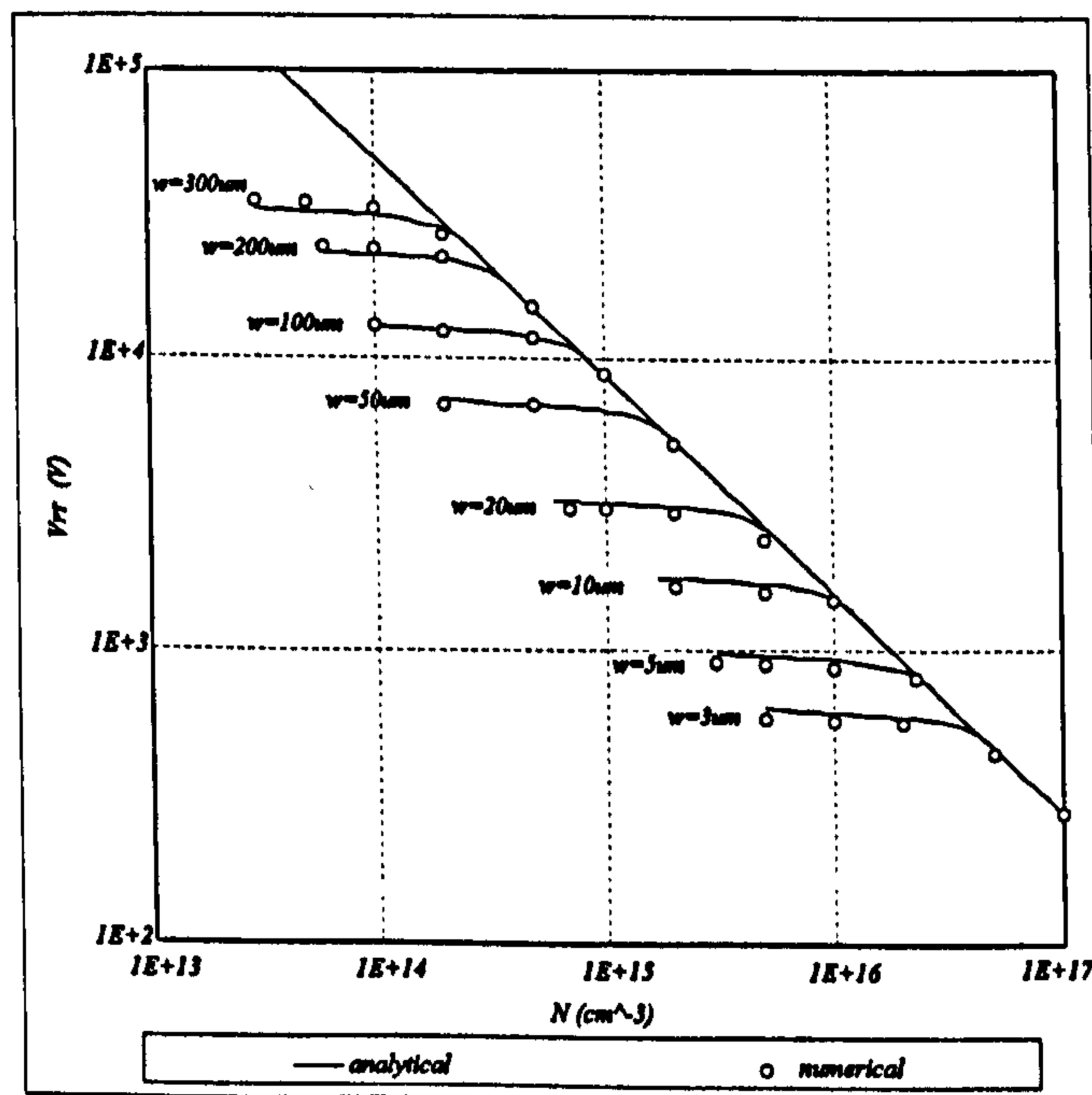
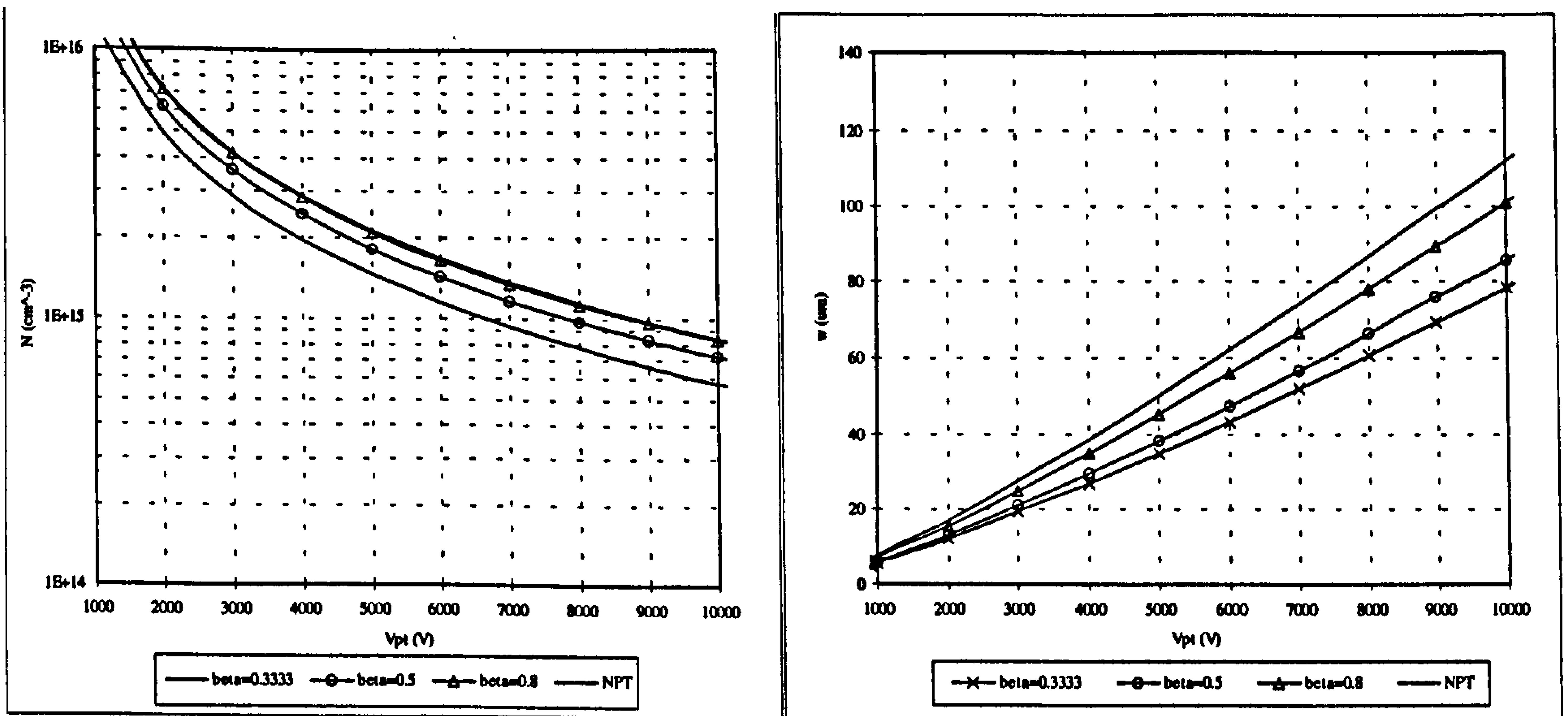


Figure 3.1 6H-SiC junction PT limited breakdown voltages

To design a 6H-SiC punch-through diode with a specific V_{PT} and β, the following expressions for N and w apply:

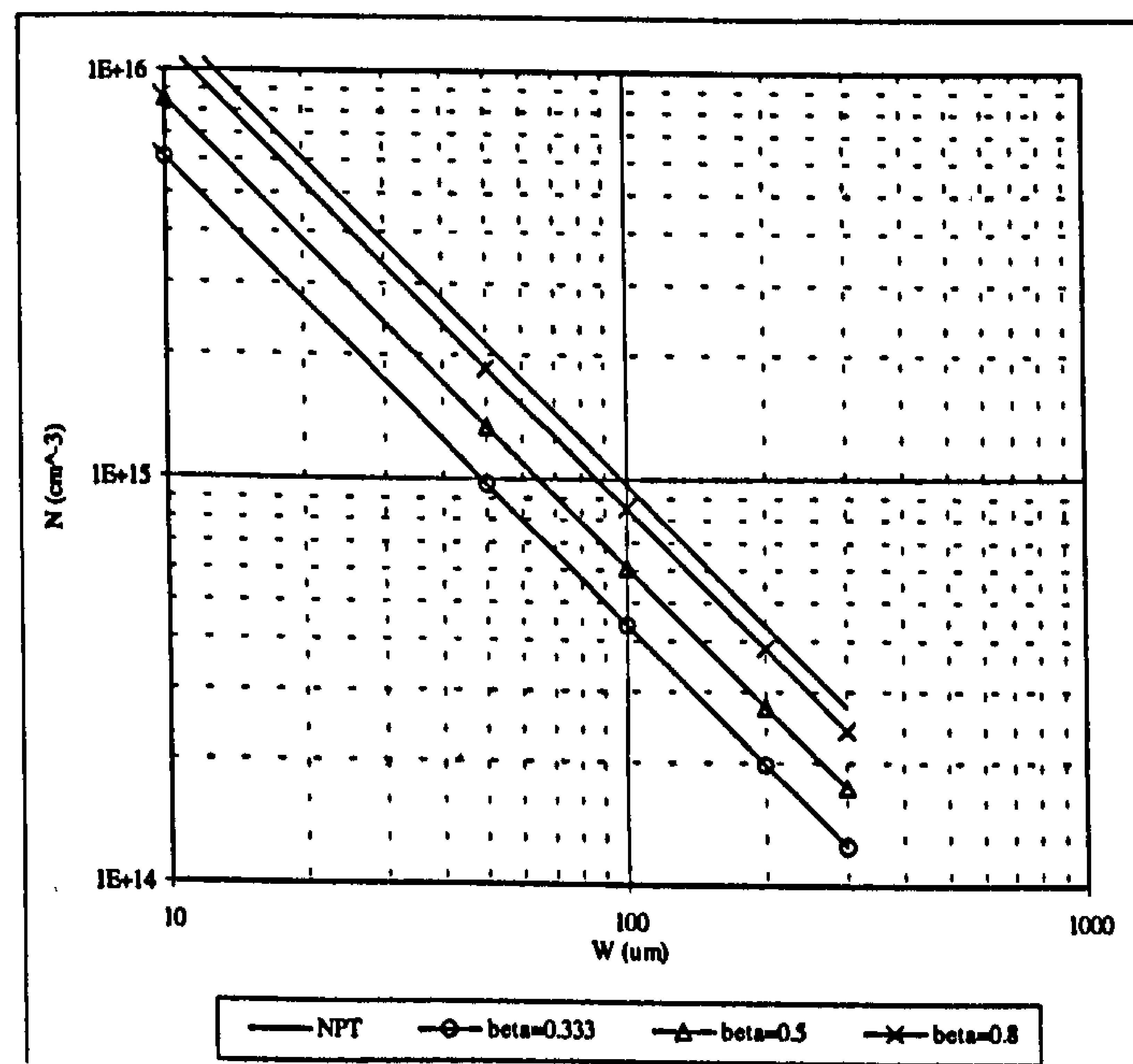
$$N=4.6\times10^{20}\frac{\beta}{(1+7\beta^2+7\beta^4+\beta^6)^{\frac{1}{3}}}V_{PT}^{-\frac{4}{3}} \tag{3.7}$$

$$w=1.524\times10^{-7}(1+7\beta^2+7\beta^4+\beta^6)^{\frac{1}{6}}V_{PT}^{\frac{7}{6}} \tag{3.8}$$



(a)

(b)



(c)

Figure 3.2 6H-SiC junction base region (a) doping (b) width, versus voltage rating and (c) doping versus width

For a NPT junction, Equations (3.7) and (3.8) are simplified by setting β to 1 (also plotted in Figure 3.2):

$$N_{NPT}=1.826\times10^{20}V_{NPT}^{-\frac{4}{3}} \qquad w_{NPT}=2.42\times10^{-7}V_{NPT}^{\frac{7}{6}} \tag{3.9}$$

In Figure 3.2, the base region doping level and width with β=0.33, 0.5 and 0.8 for a 6H-SiC punch-through limited junction are compared with those for 6H-SiC NPT structures (β=1).

3.1.2 Minimum Base Region Specific On-State Resistance

When designing punch-through devices, it is customary to minimize the base region specific on-state resistance. For a fixed breakdown voltage, the ratio of punch-through junction base region specific on-state resistance to NPT junction $R_{on,sp}$ is described by:

$$f(\beta)=\frac{0.25\sqrt{1+7\beta^2+7\beta^4+\beta^6}}{\beta} \tag{3.10}$$

The definition of β is as above ($\beta=V_{RT}/V_{PT}$). In the range $0<\beta\leq1$, a minimum value of $f(\beta)$ occurs at β=0.60. Therefore, to design a device with a minimum base region specific on-state resistance, a value of $\beta\cong0.6$ would be used.

3.2 Numerical Characterization of SiC Diodes

The diodes simulated in this work have a punch-through structure. All the devices have a 300 μm substrate with a doping level of 1×10^{19} cm^{-3}. The P^+ region thickness and doping for PiN diodes are 1.5 μm and 5×10^{17} cm^{-3} respectively. τ_0 is 1 μs for PiN diodes. The barrier height is 1.1 eV for Schottky diodes.

3.2.1 4H-SiC Schottky Diodes versus PiN Diodes

The current handling ability of 4H-SiC Schottky and PiN diodes is analysed in this section. The forward voltage across a Schottky diode is given by:

$$V_f=\eta\frac{kT}{q}\ln\left(\frac{J_f}{A^*T^2}\right)+\eta\Phi_{Bn}+R_{on,sp}J_f \tag{3.11}$$

where: η ideality factor

A^* effective Richardson constant

T temperature

Φ_{Bn} barrier height

$R_{on,sp}$ specific on-state resistance of the drift region and the substrate

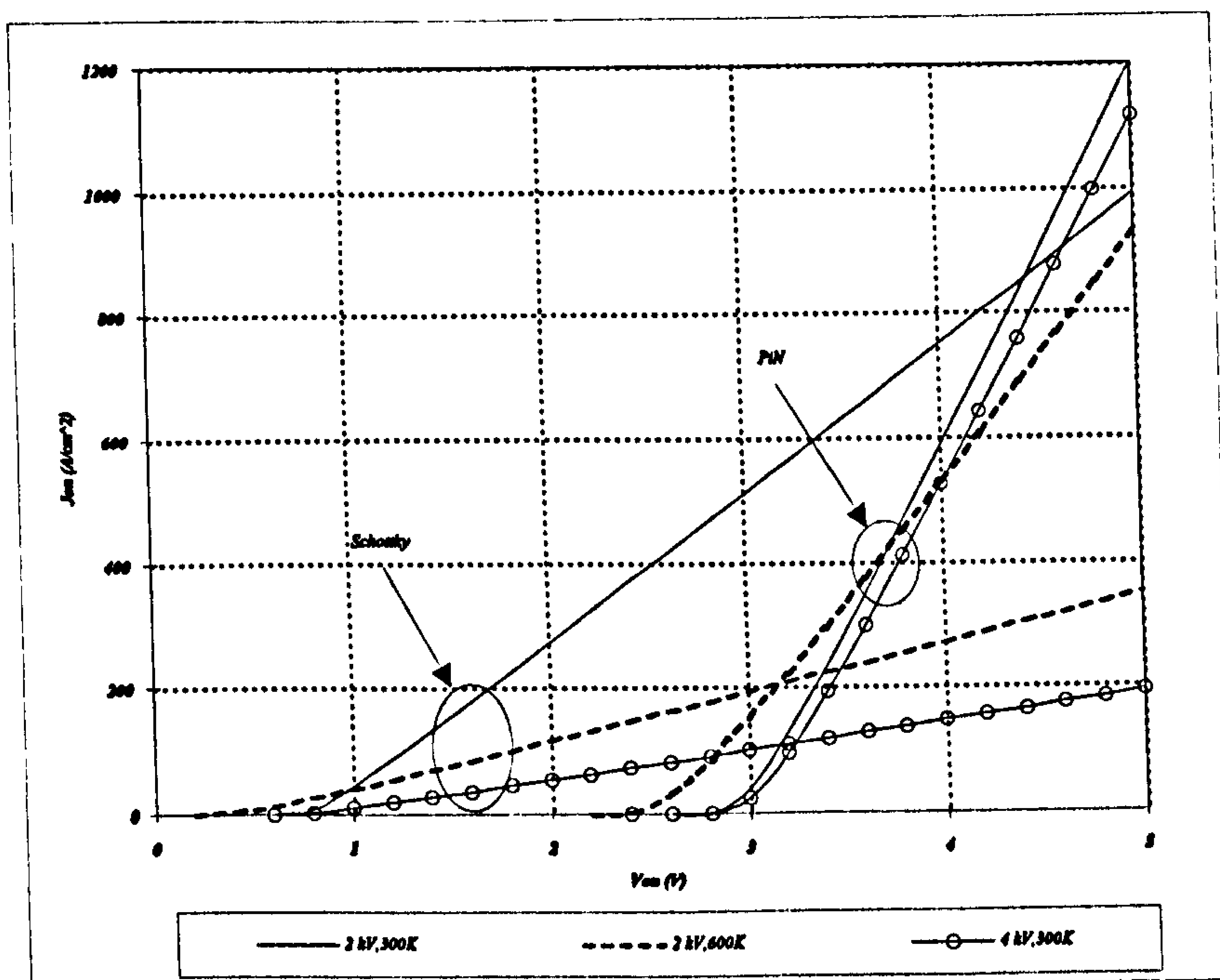


Figure 3.3 4H-SiC Schottky diodes and PiN diodes on-state characteristics

For a high voltage Schottky diode, the main component of the forward voltage is the ohmic voltage drop across the drift region and the substrate. In Figure 3.3, the on-state characteristics of 4H-SiC Schottky diodes and PiN diodes are plotted. Compared to Si Schottky diodes, the application voltage range of 4H-SiC Schottky diodes has been significantly extended. SiC produces not only a much smaller drift region specific on-resistance, but also a higher 4H-SiC P/N junction voltage than Si, which must be exceeded before significant forward current can flow. However, current handling ability mainly depends on the drift region and substrate series resistances, which increase rapidly with temperature or voltage rating. Biased at 4 V, the 2 kV 4H-SiC Schottky diode on-state

current densities are 280 A/cm^2 at 300K and 120 A/cm^2 at 600K respectively, whereas the 4 kV 4H-SiC Schottky diode has a current density of 145 A/cm^2 at room temperature. In comparison, the current handling ability of 4H-SiC PiN diodes is not influenced greatly by temperature or voltage rating. At an on-state current density of 300 A/cm^2, the forward voltages of a 2 kV 4H-SiC PiN diode are 3.52 V at 300 K and 3.41 V at 600 K, while a 4 kV device has forward voltages of 3.6 V at 300 K and 3.5 V at 600 K. Generally, the 4H-SiC Schottky diode is better than the PiN diode below 3 kV and 400K.

3.2.2 4H-SiC PiN Diodes versus 6H-SiC PiN Diodes

Equation (3.12) gives the expression of the forward voltage for the PiN diode:

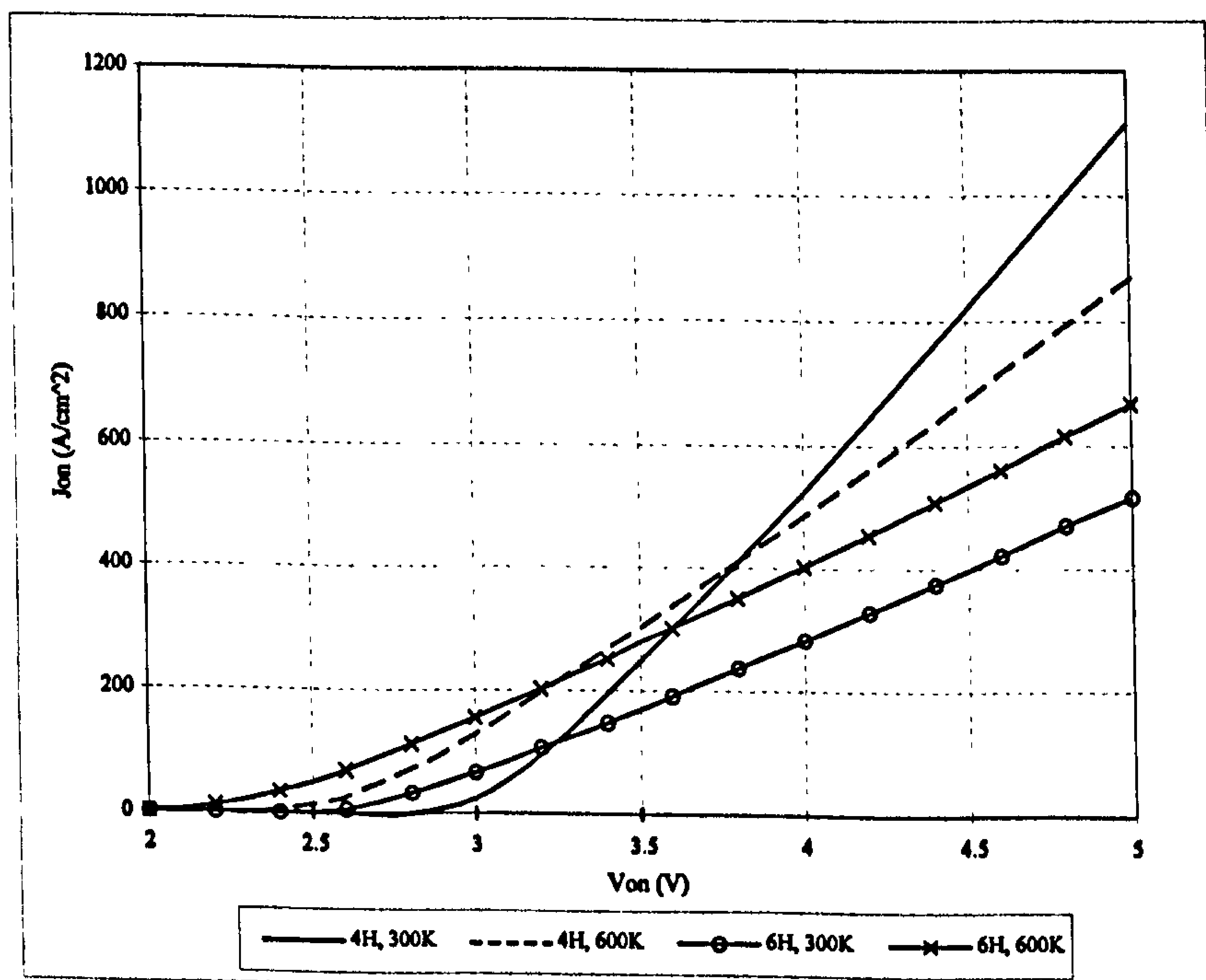
$$V_f = V_{j1} + V_{j2} + J_f(R_{N^-,mod} + R_{N^+,sp}) \qquad (3.12)$$

where $R_{N-,mod}$ the modulated specific drift region resistance

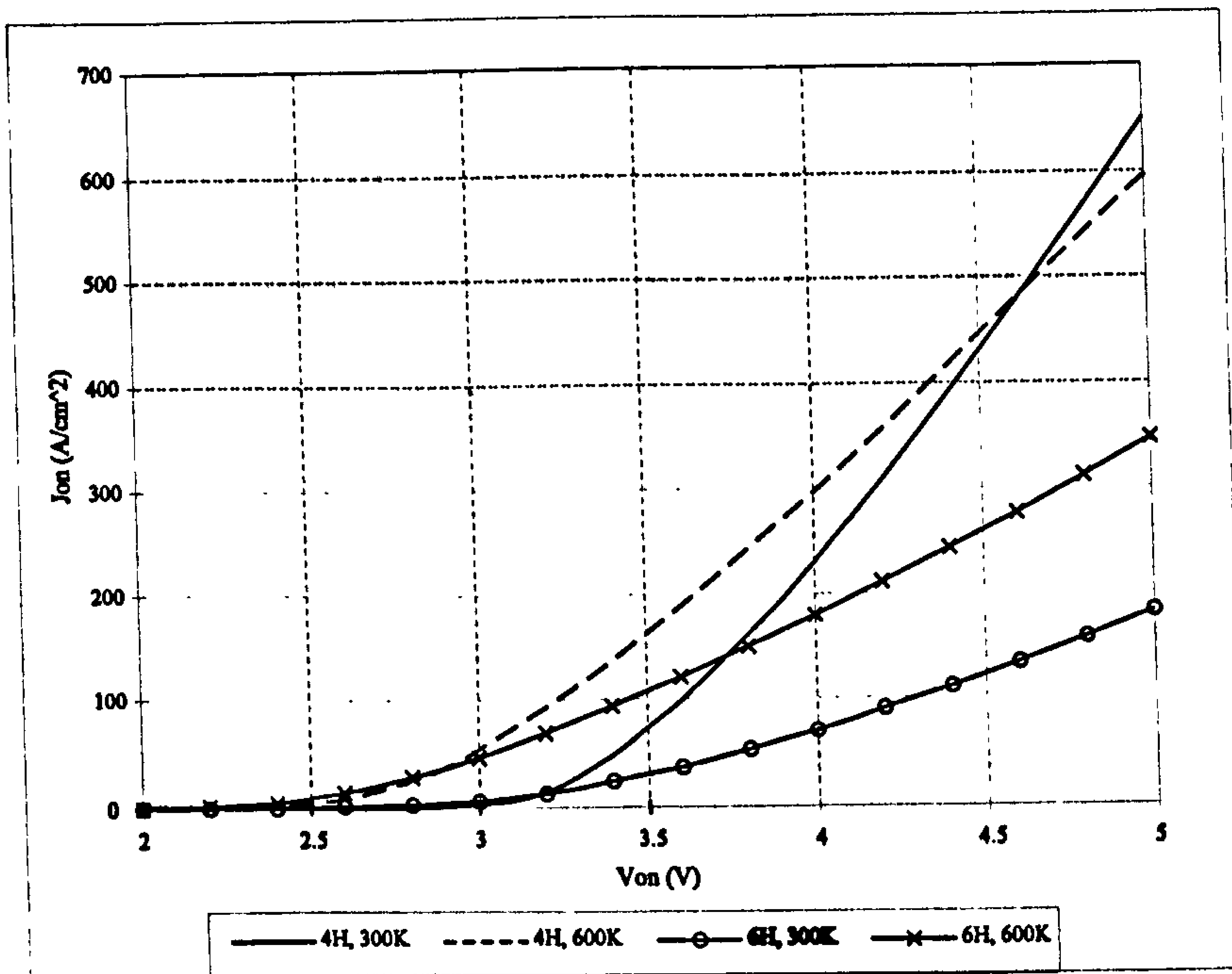
$R_{N+,sp}$ substrate specific resistance

V_{j1} P^+/N^- junction voltage

V_{j2} N^-/N^+ junction voltage



(a)



(b)

Figure 3.4. (a) 4 kV (b) 10 kV 4H-SiC and 6H-SiC PiN diodes on-state characteristics

The contribution of V_{j2} to the forward voltage is negligible, while V_{j1} is the main component of the SiC on-state voltage, which can be estimated in the normal operating range by the built-in voltage V_{bi}:

$$V_{bi}=\frac{kT}{q}\ln\left(\frac{N_D^+N_A^-}{n_i^2}\right) \tag{3.13}$$

with N_D^+ and N_A^- the P^+ and N^- region ionized dopants density respectively and n_i the intrinsic carrier concentration.

An extremely low intrinsic carrier concentration n_i due to the SiC wide bandgap introduces a high built-in voltage, which has a negative temperature coefficient. In Figure 3.4, the forward characteristics of 4 kV and 10 kV PiN diodes are shown. At higher temperature, the diode begins to conduct current at a lower voltage due to the smaller built-in voltage. The drift region and substrate resistances are affected by the drift region carrier lifetime, carrier mobility and impurity ionisation. Longer carrier lifetime and mobility introduce a larger carrier diffusion length, hence a smaller drift region resistance.

Increasing the degree of ionisation leads to a reduced substrate resistance, and more importantly, an enhanced emitter injection efficiency. Carrier lifetime and degree of ionisation increase with elevated temperature, but mobility is reduced due to the enhanced lattice scattering effect. For 4H-SiC diodes, the net effect is a lower modulated drift region resistance and a larger substrate resistance. As shown, the current rise in 4H-SiC PiN diodes is slower at elevated temperature. It is the opposite for 6H-SiC PiN diodes: elevating the temperature improves the diode current handling ablity, which is not favoured when paralleling devices.

Comparing the forward characteristics of 4H-SiC and 6H-SiC PiN diodes, it is apparent that the 4H-SiC PiN diode is a better choice, especially at high current densities and voltage ratings. As expected, the larger 4H-SiC bandgap introduces a larger junction voltage than with 6H-SiC. However, the 4H-SiC electron mobility in a lightly doped region is higher than in 6H-SiC, resulting in a lower drift region resistance. In addition, its ionisation gradient is larger, specifically, for the same doping level, the free electron concentration in a 4H-SiC substrate is higher than in a 6H-SiC substrate. Consequently, 4H-SiC diodes exhibit a lower substrate resistance than 6H-SiC PiN diodes despite the slightly lower electron mobility in a highly doped 4H-SiC region. A higher degree of ionisation also favours a high emitter injection efficiency.

In a PiN diode, both the P^+ and N^+ emitters inject excess carriers into the drift region, making the ohmic voltage drop in the drift region negligible in the typical operation range. For devices in which only one end injects minority carriers into the drift region, such as the IGBT, the higher 4H-SiC electron mobility is more attractive. In Figure 3.5, the forward conduction characteristic of a 5 kV 4H-SiC IGBT is compared to a corresponding 6H-SiC device at 300K. The voltage drop in the drift region can be no longer neglected. Hence the better conductivity modulation ability of the 4H-SiC IGBT overrides. For such

devices, 4H-SiC is more suitable.

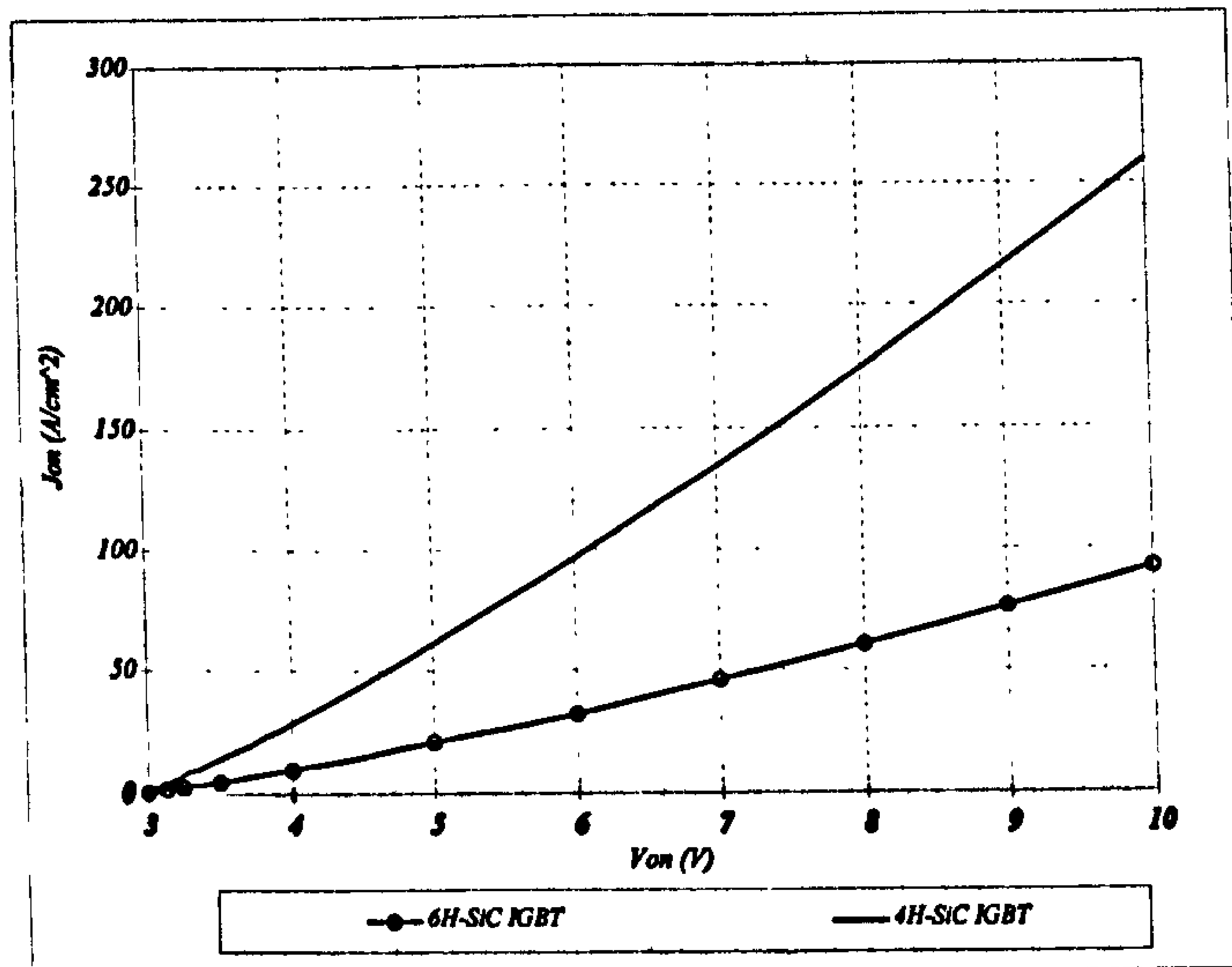


Figure 3.5 Comparison of 5 kV 4H and 6H-SiC IGBT on-state characteristics at 300K

3.2.3 Effect of Substrate Resistance

Because of the existence of deep levels, the incomplete ionisation phenomenon is pronounced in SiC devices, even at the room temperature. One of the most important consequences is the increased substrate resistance. Carriers 'freeze out', hence the substrate resistance, $R_{subs}=w/q\mu nA$, is relatively high. As shown in Figure 3.4, the current in SiC PiN diodes rises linearly with voltage after the built-in voltage is exceeded, indicating the substrate resistance is a dominant current limiting factor. Table 3.1 shows calculated substrate resistance per cm^2 for a substrate doping level and thickness of 1×10^{19} cm^{-3} and 300 μm respectively. The 4H-SiC diode substrate resistance at 600K is larger than that at 300 K. By contrast, 6H-SiC diodes show a lower substrate resistance at elevated temperature. This is confirmed by the characteristics presented in Figure 3.4.

Table 3.1 SiC Diode Substrate Resistances

	4H-SiC(300K)	4H-SiC(600K)	6H-SiC(300K)	6H-SiC(600K)
n (cm^{-3})	1.56×10^{18}	4.12×10^{18}	5.82×10^{17}	2.72×10^{18}
R (mΩ/cm^2)	1.53	2.32	3.62	3.25

The 4 kV PiN diodes on-state resistance (sum of substrate and drift region on-state resistances) values fit well with the calculated values in Table 3.1, indicating a negligible drift region ohmic voltage. However, the drift region specific on-state resistance increases with voltage rating because the drift region is widened and the doping reduced to block higher voltage. Consequently, the ohmic voltage drop across the drift region is higher for devices with a higher voltage rating. It is of interest to investigate at what voltage rating the drift region ohmic voltage would become higher than the substrate ohmic voltage. For 4H-SiC and 6H-SiC PiN diodes, the bounds are 12 kV and 10 kV respectively.

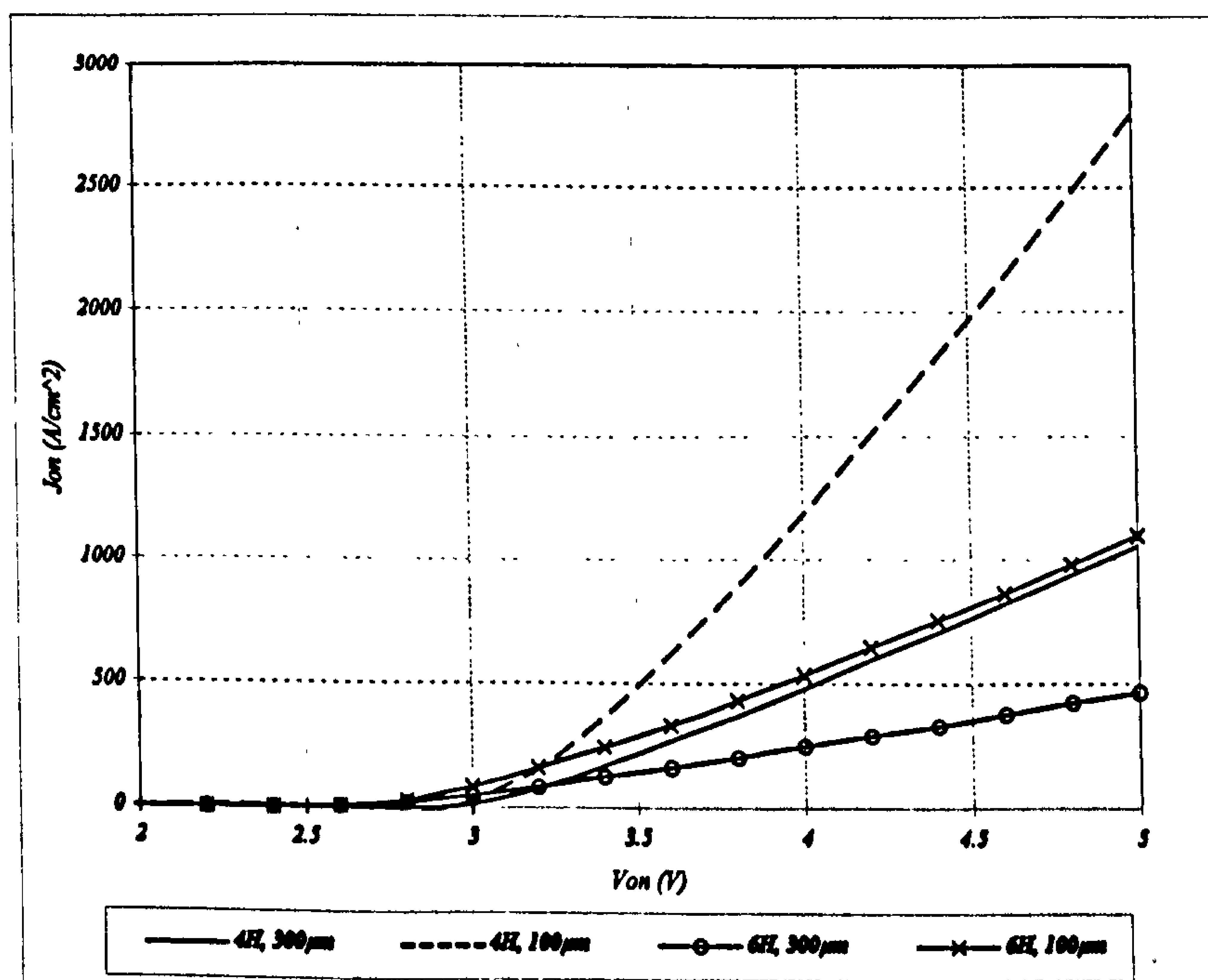


Figure 3.6 Comparison of 5 kV 4H-SiC and 6H-SiC PiN diodes with different substrate thickness at 300 K

One way to reduce substrate resistances is with a thinner substrate. It is necessary to keep a thick substrate in order to withstand mechanical stresses during device processing. Consequently, 300 μm is a typical substrate thickness. The lowest device thickness available is about 100 μm. In Figure 3.6, the on-state characteristics of 5 kV PiN diodes at room temperature with substrates of 100 μm and 300 μm are shown. The current handling ability of both diodes is improved greatly by reducing the substrate resistance.

However, for a typical operating current density, such as 300 A/cm^2, the on-state voltages do not change significantly, especially for 4H-SiC PiN diodes. The 4H-SiC PiN diode on-state voltage decreases by 0.3 V, while the 6H-SiC PiN diode on-state voltage decreases by 0.73 V.

3.2.4 Diode Reverse Recovery

Diode reverse recovery behaviour is investigated using a Mixed-Mode Simulation Package [3.20]. The diodes are switched from an on-state current of 1.5 kA to block an anode voltage half of the device voltage rating, with a di/dt of 500 A/μs. In Figure 3.7, the test circuit is shown. The device area is 10 cm^2, hence the on-state current density is 150 A/cm^2. The snubber capacitance and resistance are chosen carefully to ensure device soft recovery. The typical values of L_l, C and R_c are 2μH, 0.5μF and 5 Ω respectively.

When switching the Schottky diode, only majority carriers must be removed to form the depletion layer which supports the blocking voltage. As shown in Figure 3.8, the reverse recovery peak current of a 2 kV 4H-SiC Schottky diode is only 36 A and the reverse recovery time is about 300 ns. Furthermore, Schottky diode reverse recovery characteristics are not affected by temperature, indicating that the displacement current is the dominant component of the reverse recovery current, giving excellent device switching stability.

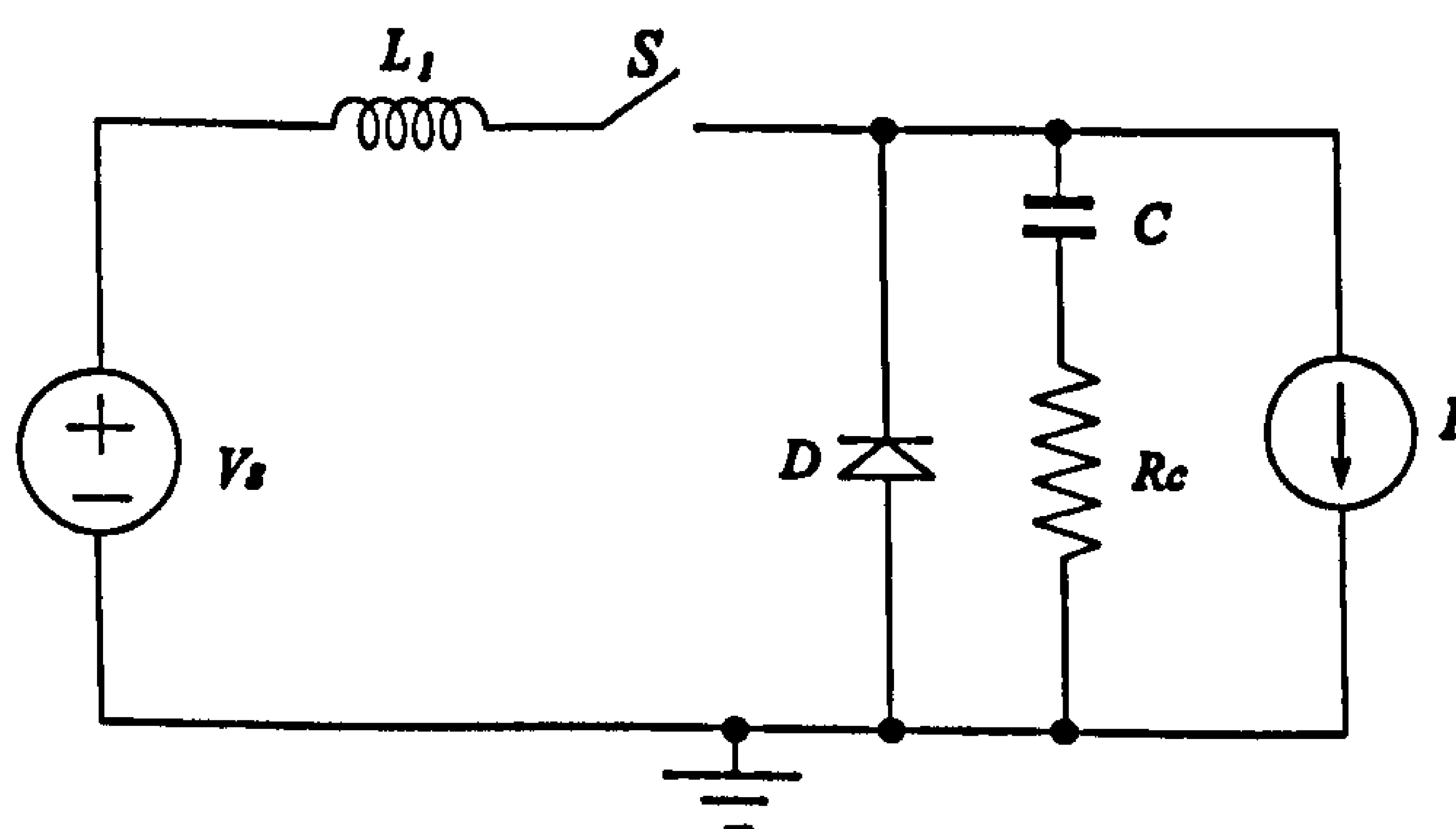


Figure 3.7 Diode reverse recovery test circuit

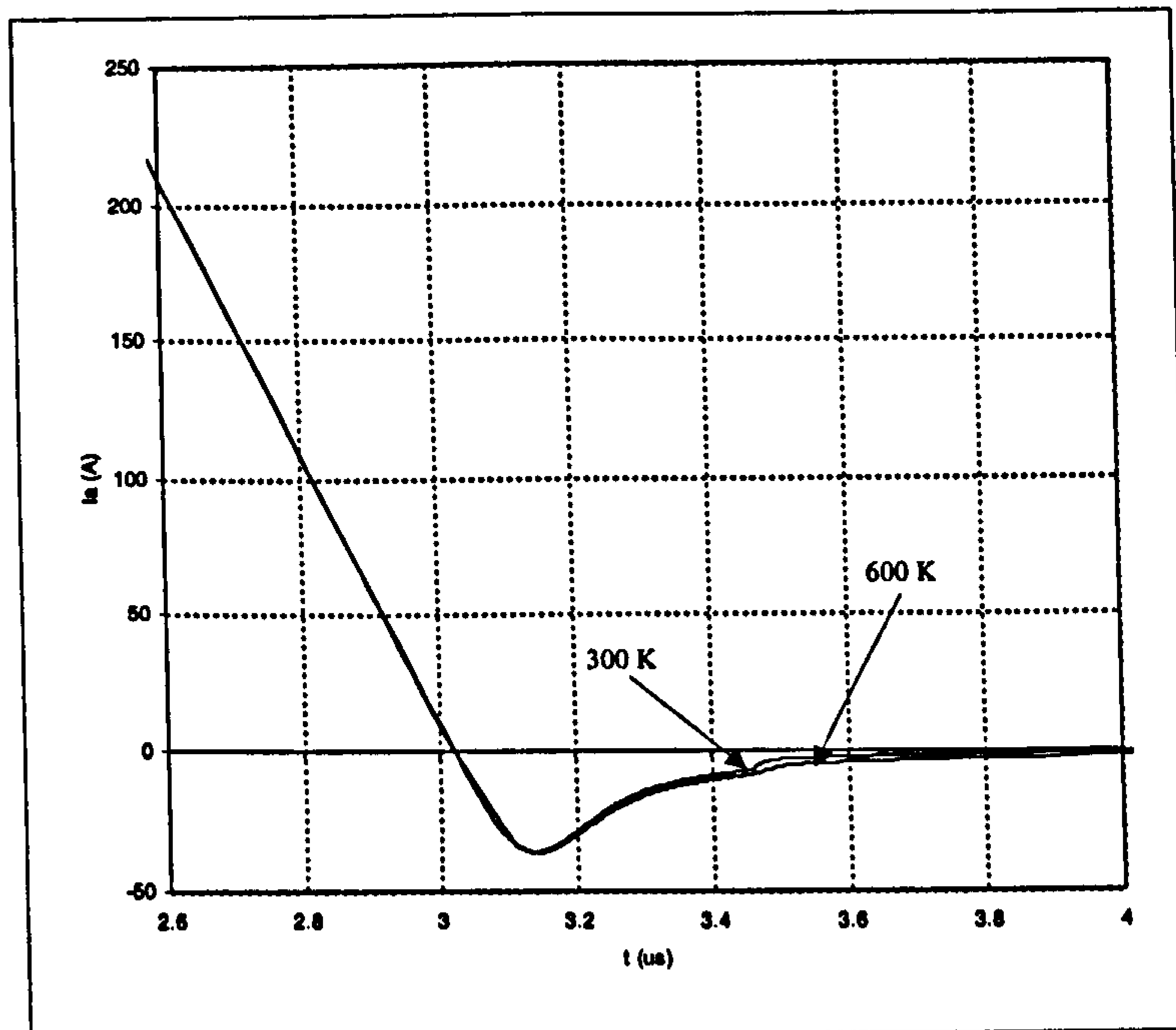
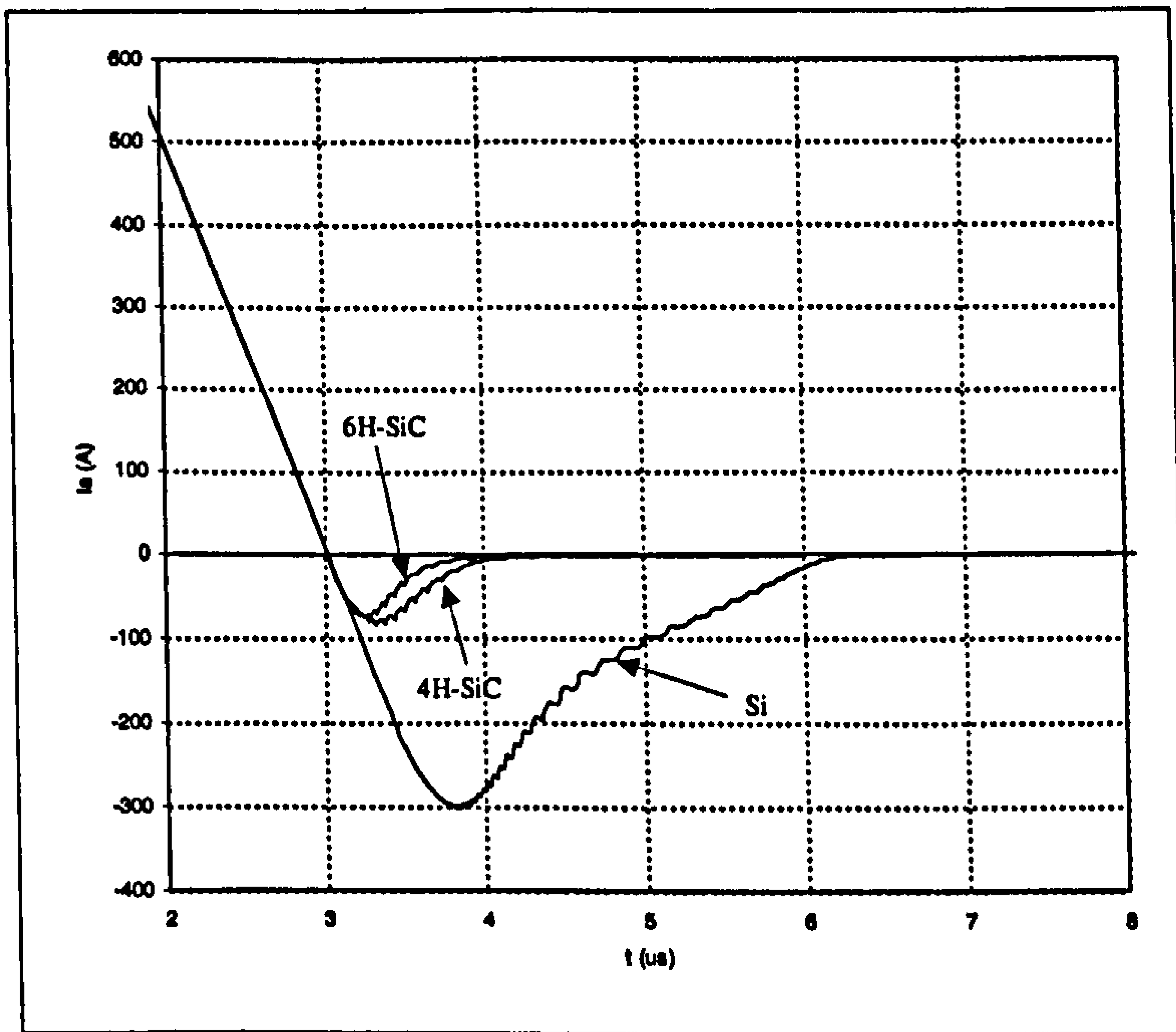


Figure 3.8 2 kV Schottky diode reverse recovery characteristics

In the case of PiN diodes, there is stored charge in the drift region, which leads to reverse recovery charge. In Figure 3.9, the reverse recovery characteristics of 5 kV 4H-SiC, 6H-SiC and Si PiN diodes at 300 K, 400 K and 600 K are compared. The switching waveform of the 5 kV Si PiN diode at 600 K is not included for such a high junction temperature is impractical for Si devices. The SiC PiN diode and the Si PiN diode carrier lifetimes are set to 1 μs and 2 μs at 300 K respectively, to obtain diode on-state voltages of less than 4 V. The SiC PiN diodes exhibit better switching characteristics than their Si counterparts. The Si PiN diode reverse recovery time is 2 to 4 times longer than for the SiC PiN diode and its reverse recovery charge is 10 times larger. The carrier mobility and degree of ionisation in 4H-SiC are larger than in 6H-SiC, resulting in a longer carrier diffusion length and a higher emitter injection efficiency. Consequently, more excess carriers are stored in the 4H-SiC PiN diode drift region than in the 6H-SiC diode, hence, larger reverse recovery time and charge are observed. However the switching performance of both diodes are similar.



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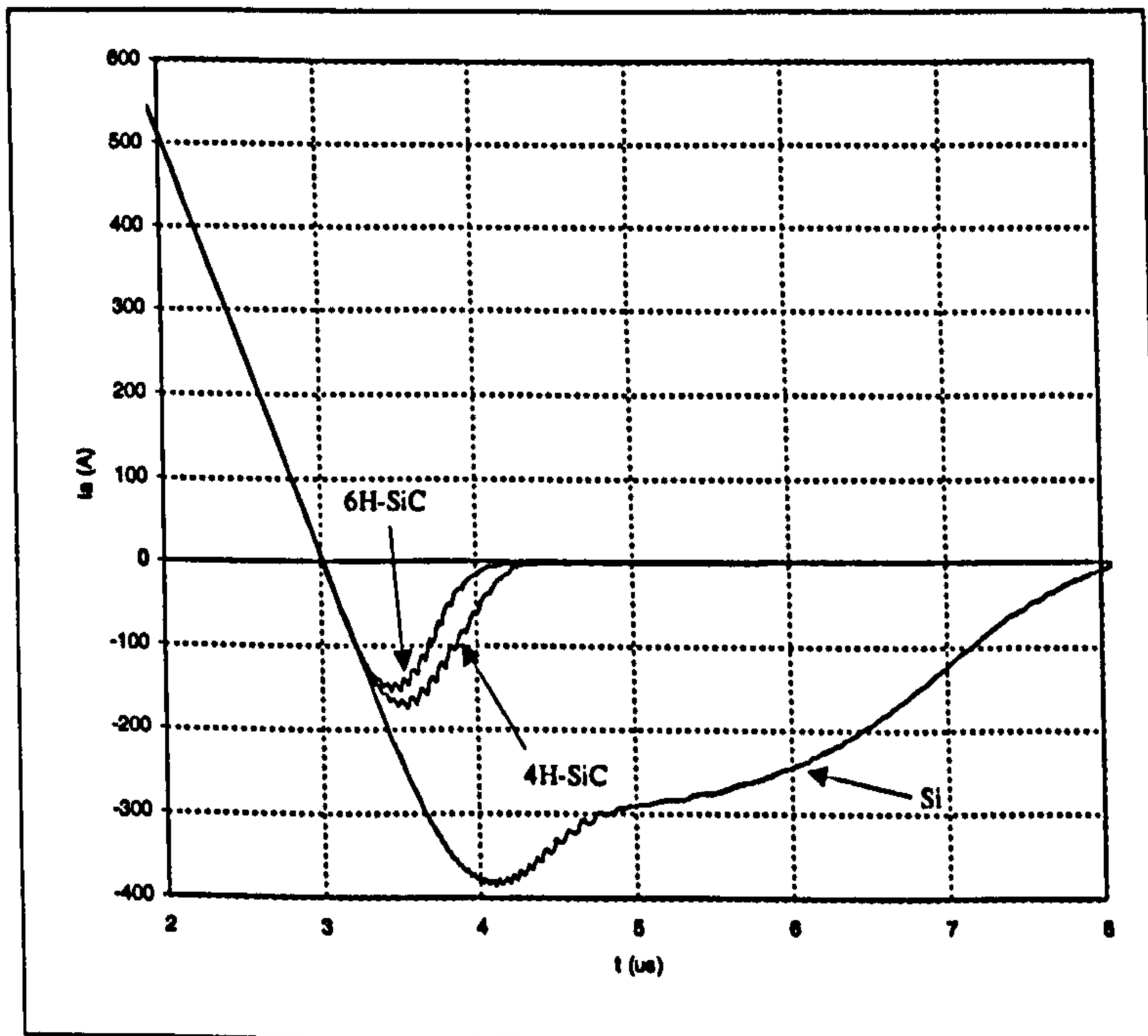

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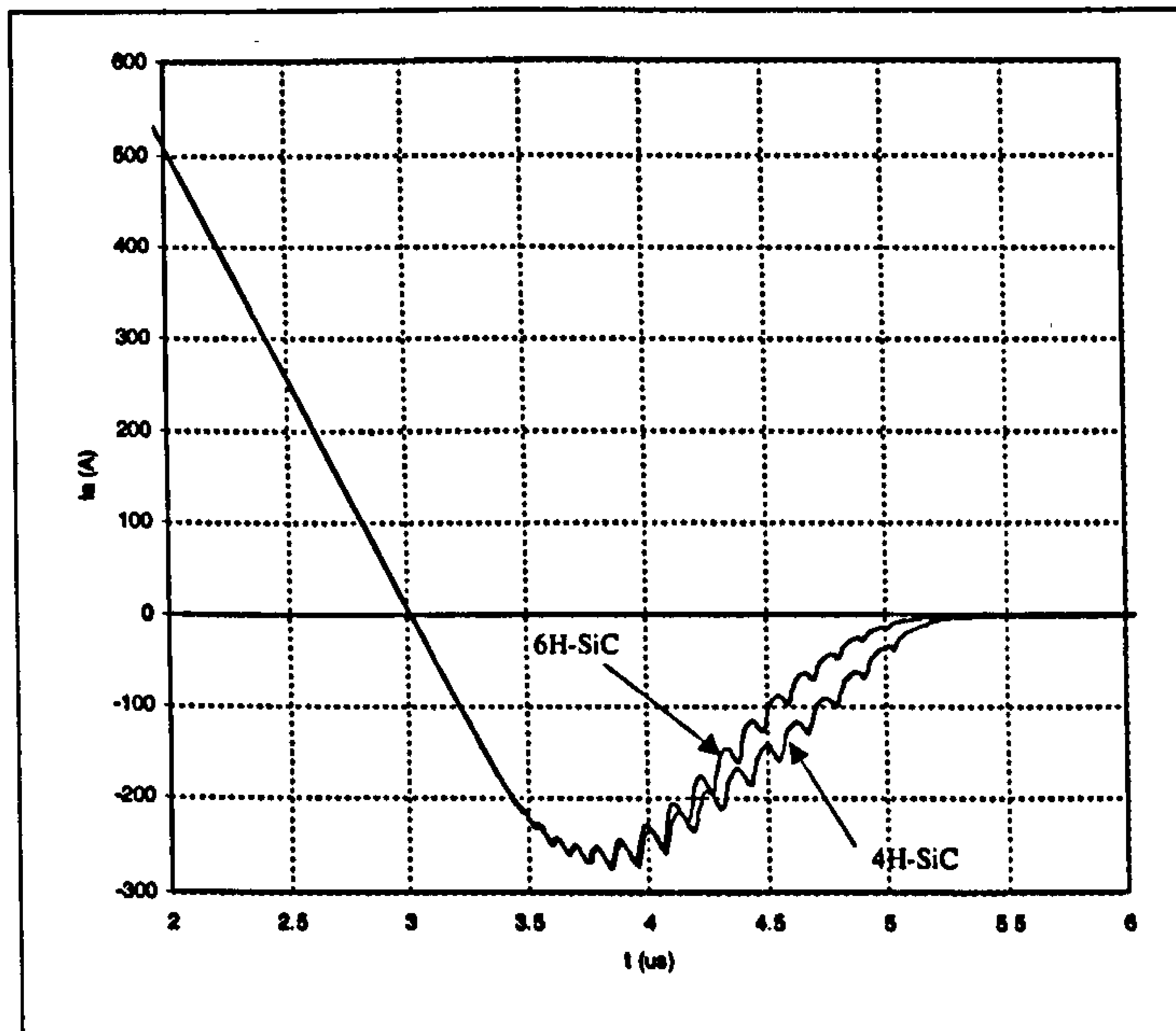


(c)

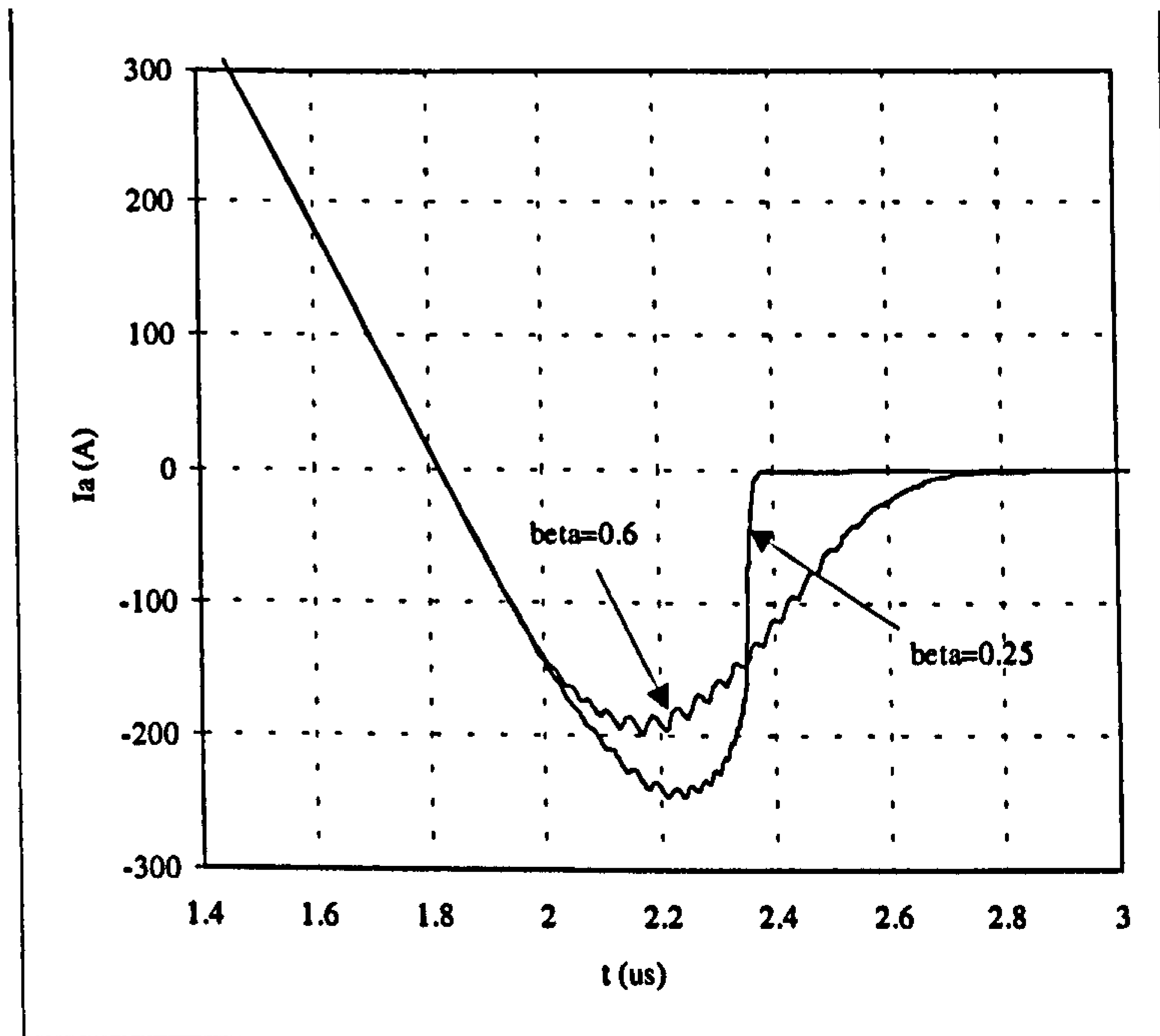
Figure 3.9 Comparison of 5 kV PiN diodes reverse recovery characteristics at (a) 300 K (b) 400 K and (c) 600 K

3.3 Soft Recovery Design of 6H-SiC PiN Diodes

It is customary to minimise the drift region width so that the injected charge during the on-state can be reduced greatly compared to non punch-through devices. However, this does not apply to PiN diodes. The most important issue when designing a PiN diode is to avoid snap recovery. Snap recovery is when the magnitude of diode reverse current decreases abruptly during the reverse recovery. When the depletion layer reaches the i/N+ junction, most stored charge has been swept out of the drift region or diminished via recombination. A rapid change of the diode current occurs at that moment. Generally, V_{RT} is designed to be equal to the likely DC link voltage, which is half to 80% of the diode breakdown voltage V_{PT}.

Numerical simulations are performed to compare the reverse recovery behaviours of two 5 kV 6H-SiC PiN diodes, which are designed with β of 0.25 and 0.6 respectively. The devices are switched from an on-state current of 1.5 kA to blocking a cathode voltage of 2.5 kV. An RC snubber circuit is parallel connected to the diode. The junction

temperature is 500 K. The diode with β of 0.6 shows a favoured soft recovery characteristics. In comparison, the diode with β of 0.25 exhibits a snap recovery behaviour. The snap can cause a large voltage spike due to the existence of parasistic inductances and even catastrophic destruction of other circuit components.



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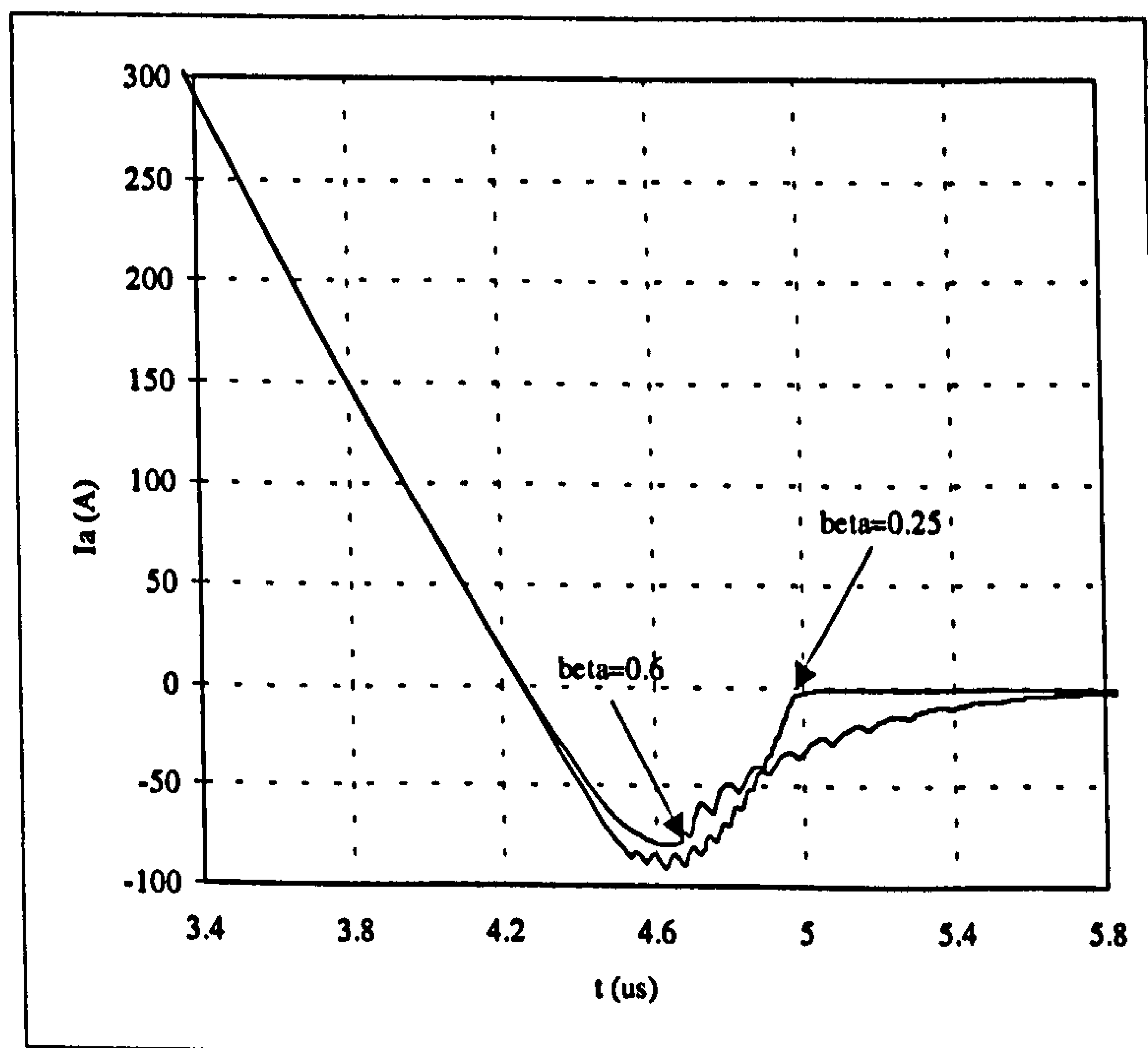

(b)

Figure 3.10 Comparison of diode reverse recovery characteristics (a) L=3μH and (b) L=7μH, 500 K

3.4 Conclusion

In this chapter, an analytical closed-form solution of 6H-SiC punch-through limited junction breakdown voltage was presented. The solution corresponds well with numerical simulation results. Based on this solution, the value of β (0.6) for the minimum value of base region specific on-state resistance, was derived. SiC diode on-state and switching characteristics were simulated and compared with the Si diode. As expected, SiC diodes exhibit significantly superior characteristics than their Si counterparts. The boundary between the PiN diode being better than the Schottky diode is above 3 kV and 400 K. The current handling ability of 4H-SiC PiN diodes is better than 6H-SiC PiN diodes while the switching loss is slightly larger. The effect of substrate resistance was also analysed in detail. Finally, the reverse recovery characteristics of two diodes designed with different β values were compared. Snap recovery is more probable in a diode with a small β.

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CHAPTER 4

EVALUATION OF 4H-SIC UMOSFET PERFORMANCE IN RELATION TO INSULATOR RELIABILITY

Extensive effort to develop the SiC MOSFET is being carried out. Several high voltage MOSFETs have been fabricated [4.1] - [4.5]. Extremely attractive performance projections have been made for the 4H-SiC UMOSFET structure, claiming 100 times better performance than silicon devices for power electronics applications [4.6]. These projections are made on the basis of the 10 times higher breakdown field in SiC compared to silicon. However, closer examination reveals that the limitations of the gate insulator such as SiO_2, will prevent the full potential of these devices from being exploited [4.7].

In the forward blocking state, the gate electrode of the MOSFET is connected to the source. The applied drain-source voltage is supported by the reverse biased P base/N drift junction and a depletion layer extends into both sides. The potentials in silicon carbide at the sidewall and bottom of the trench are raised to positive values. Due to the extremely thin oxide width, the electric field in the gate oxide is very high, especially near the trench corners. Since the critical electric field for avalanche breakdown in SiC is about 2×10^6 V/cm and the dielectric constants ratio of SiO_2/SiC is 3.9/10, the electric field in the oxide can approach 1×10^7 V/cm at the trench corners. This leads to the rupture of the oxide well before the avalanche breakdown voltage is reached. Furthermore, considering the long-term reliability of the insulator, the maximum electric field in the oxide should not exceed 2×10^6 V/cm to avoid Fowler-Nordheim injection of electrons from the conduction band of the N^+ polysilicon gate into the insulator at room temperature. This limit can be raised to 3×10^6 V/cm if a P^+ polysilicon gate is employed, due to about a 1V increase in the barrier

height [4.8].

In this chapter, the impact of oxide reliability on the performance of the 4H-SiC UMOSFET is investigated.

4.1 Simulation Results and Discussion

To analyze insulator reliability in the SiC UMOSFET, the two dimensional Poisson equation in the N^- drift region and the oxide must be solved. Due to the difficulty in obtaining an analytical solution, a numerical simulation program is used. The 4H-SiC UMOSFET structure simulated is shown in Figure 4.1. The oxide sidewall width is maintained at 500 Å in order to minimize the threshold voltage. The P base doping is 1×10^{17} cm^{-3} and a P^+ polysilicon gate is employed. The cell pitch, the trench bottom width and the channel length are 30 μm, 8 μm and 2 μm, respectively. The fixed oxide charge density is 1×10^{11} cm^{-2} in all the simulations. The physical models and material parameters described in Chapter 2 are employed.

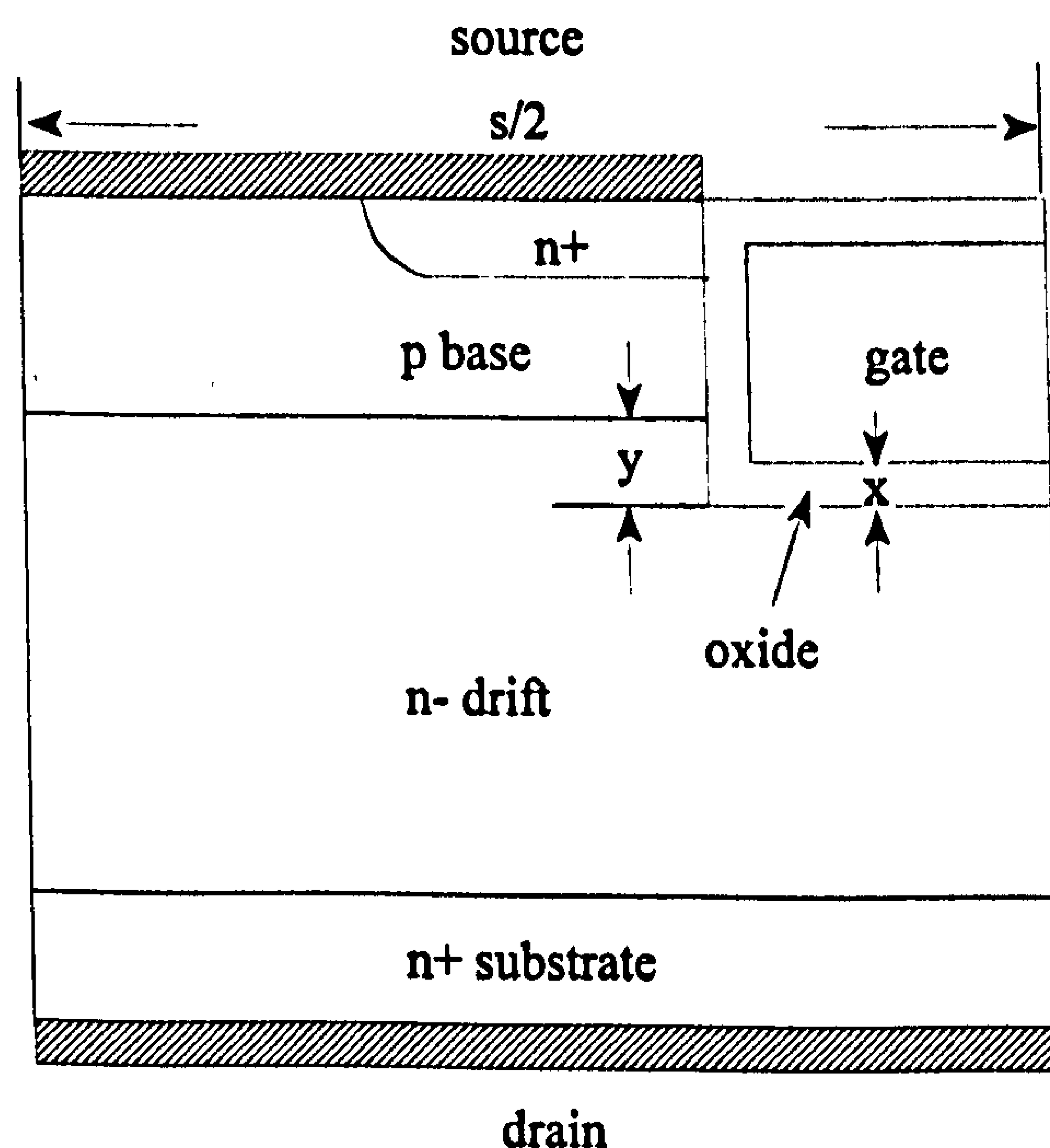

Figure 4.1 Half of a UMOSFET cell structure

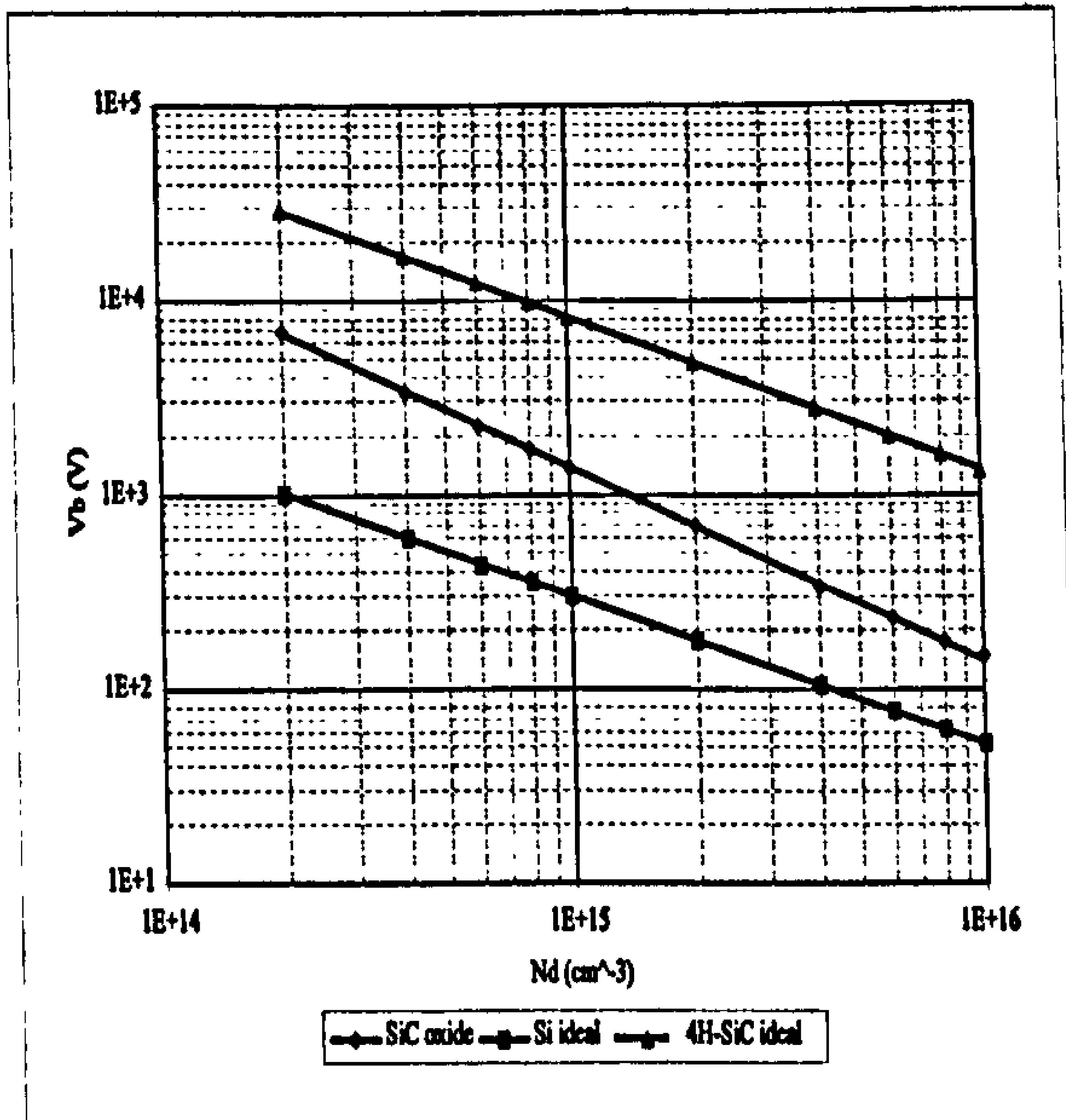

Figure 4.2 Breakdown voltage versus drift region doping for UMOSFETs

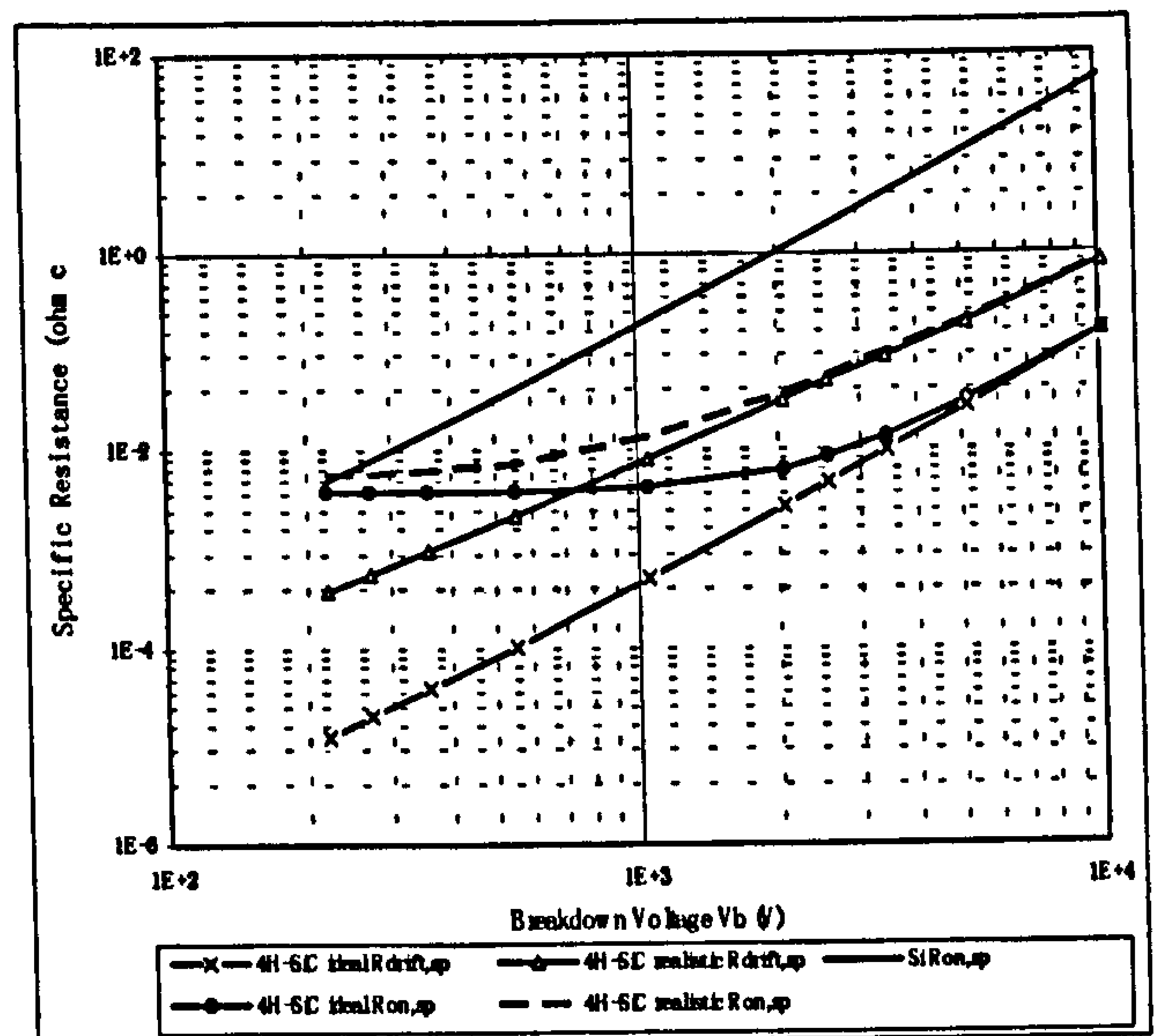

Figure 4.3 Specific on state resistances of UMOSFETs versus breakdown voltage

The maximum blocking voltage of 4H-SiC UMOSFETs versus the N^- drift region doping level with the limit that the maximum electric field in the oxide is 3×10^6 V/cm are compared with the ideal cases for Si and SiC in Figure 4.2. The analytical expression for the breakdown voltage of the 6H-SiC PN abrupt junction (Equation (3.9)) is used to calculate the ideal 4H-SiC UMOSFET breakdown voltage. The breakdown voltage of the Si UMOSFET is assumed to be equal to that of an ideal Si abrupt junction. The oxide overlap over the drift region y and the trench bottom thickness x are 0.1 μm and 0.05 μm, respectively. It is apparent that the voltage blocking capability of 4H-SiC UMOSFETs are severely hampered by oxide reliability, especially with high doping. By decreasing the doping level, these devices gradually approach their ideal values, due to the corresponding reduction of the critical electric field in SiC. A 4H-SiC UMOSFET, taking into account insulator reliability with drift region doping $N_d=1\times10^{16}cm^{-3}$, can only support 220V, whilst an ideal 4H-SiC UMOSFET's breakdown voltage is 1570V. However, the 4H-SiC UMOSFET still exhibits far better forward voltage blocking capability than the Si UMOSFET.

Figure 4.3 shows the UMOSFETs' specific resistance dependence on breakdown voltage. In this study, the total on-state resistance $R_{on,sp}$ comprises the specific channel resistance $R_{ch,sp}$, the specific drift region resistance $R_{d,sp}$ and the specific substrate resistance $R_{sub,sp}$. The contact resistances and the N^+ source resistance are neglected for simplicity. Simulation results suggest that the current spreads throughout the drift region in the on-state because of the accumulation layer formed under the bottom of the trench. Therefore the conduction area of the drift region is taken as the area of the device when calculating the drift region resistance. The MOS channel resistance is calculated using the gradual-channel approximation [4.9]:

$$R_{ch,sp} = \frac{L_{ch} S}{2\mu_{inv} C_{ox} (V_{gs} - V_{th})} \tag{4.1}$$

where

L_{ch}	channel length	S	cell pitch
μ_{inv}	electron mobility in the inversion layer	C_{ox}	gate oxide capacitance
V_{gs}	gate bias voltage	V_{th}	threshold voltage

In Equation (4.1), V_{gs} is set to 15V, which is a typical value in power electronic circuits. The channel electron mobility is assumed to be 500 cm²/Vs for Si, 300 cm²/Vs for SiC in the ideal case and 100 cm²/Vs for SiC in the realistic case [4.10]. To calculate $R_{sub,sp}$, a substrate thickness of 300 μm is used. The substrate resistivity is 0.01 Ωcm for Si, which is commercially available. Considering the impact of incomplete ionization, the substrate resistivity is set as 0.1 Ωcm for 4H-SiC. In Si UMOSFETs with blocking voltages greater than 100V, the dominant contributor to the on-state resistance is the drift region resistance, which rapidly increases with increased breakdown voltage due to the lack of conductivity modulation. This is the primary disadvantage of the Si UMOSFET. In comparison with Si UMOSFETs, the current handling capability of SiC UMOSFETs is mainly limited by

the substrate series resistance and the channel resistance in the blocking voltage range less than 1000V. Beyond this voltage, the drift region resistance starts to dominate. 4H-SiC UMOSFETs, when taking into account the insulator reliability and low channel electron mobility with a blocking voltage less than 250V, exhibit higher on-state resistance than Si UMOSFETs. Their drift region resistance is 5 to 30 times higher than the ideal SiC UMOSFET and their channel resistance is 3 times higher. It is necessary to point out that the drift region doping of an ideal SiC UMOSFET with a breakdown voltage of less than 500V is higher or comparable to its P base region doping. Under this condition, the calculation of the drift region resistance, assuming a one-sided abrupt junction, is inaccurate.

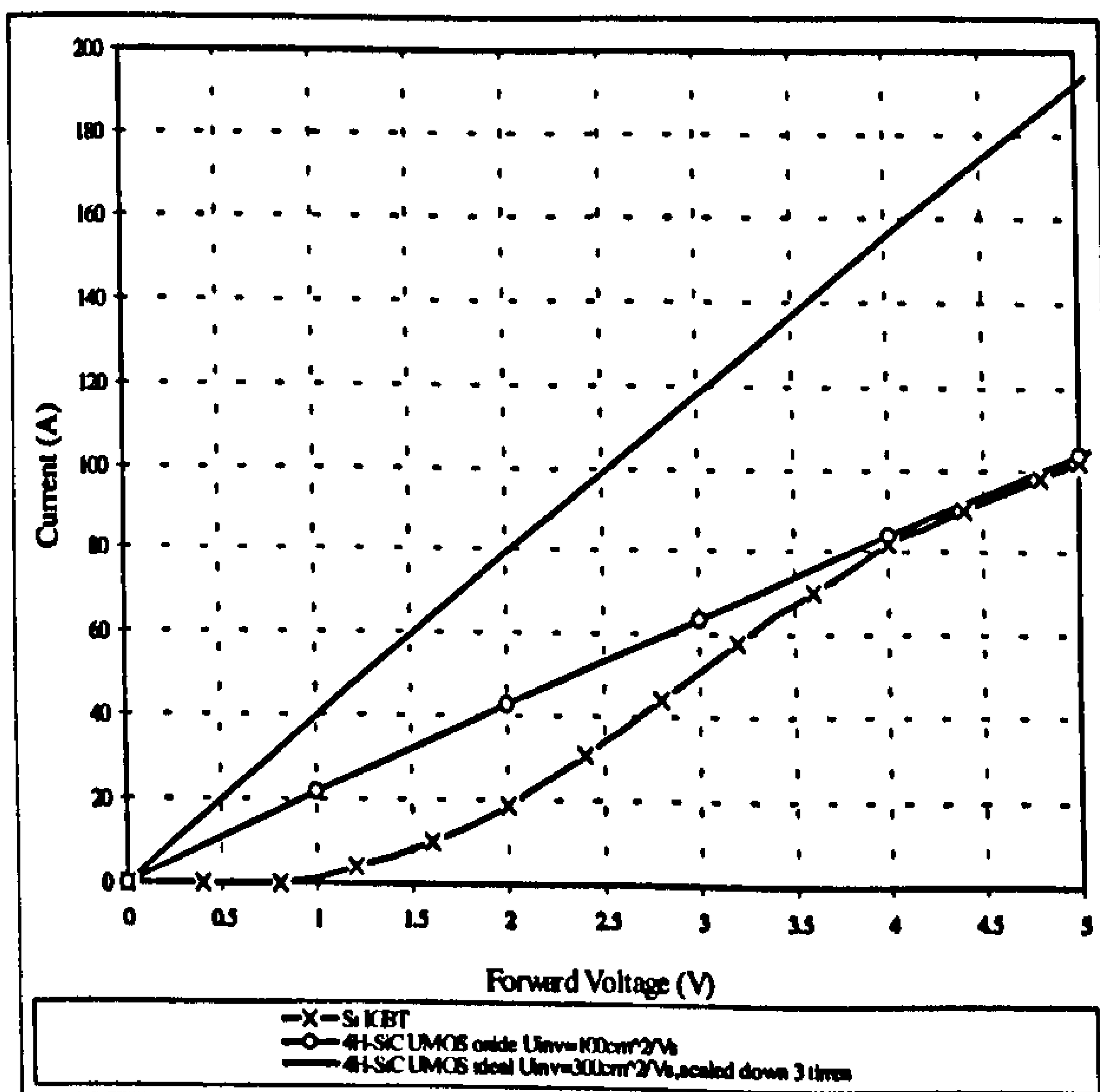

Figure 4.4 Comparison of 1200V Si IGBT and 4H-SiC UMOSFETs' forward characteristics at 300K

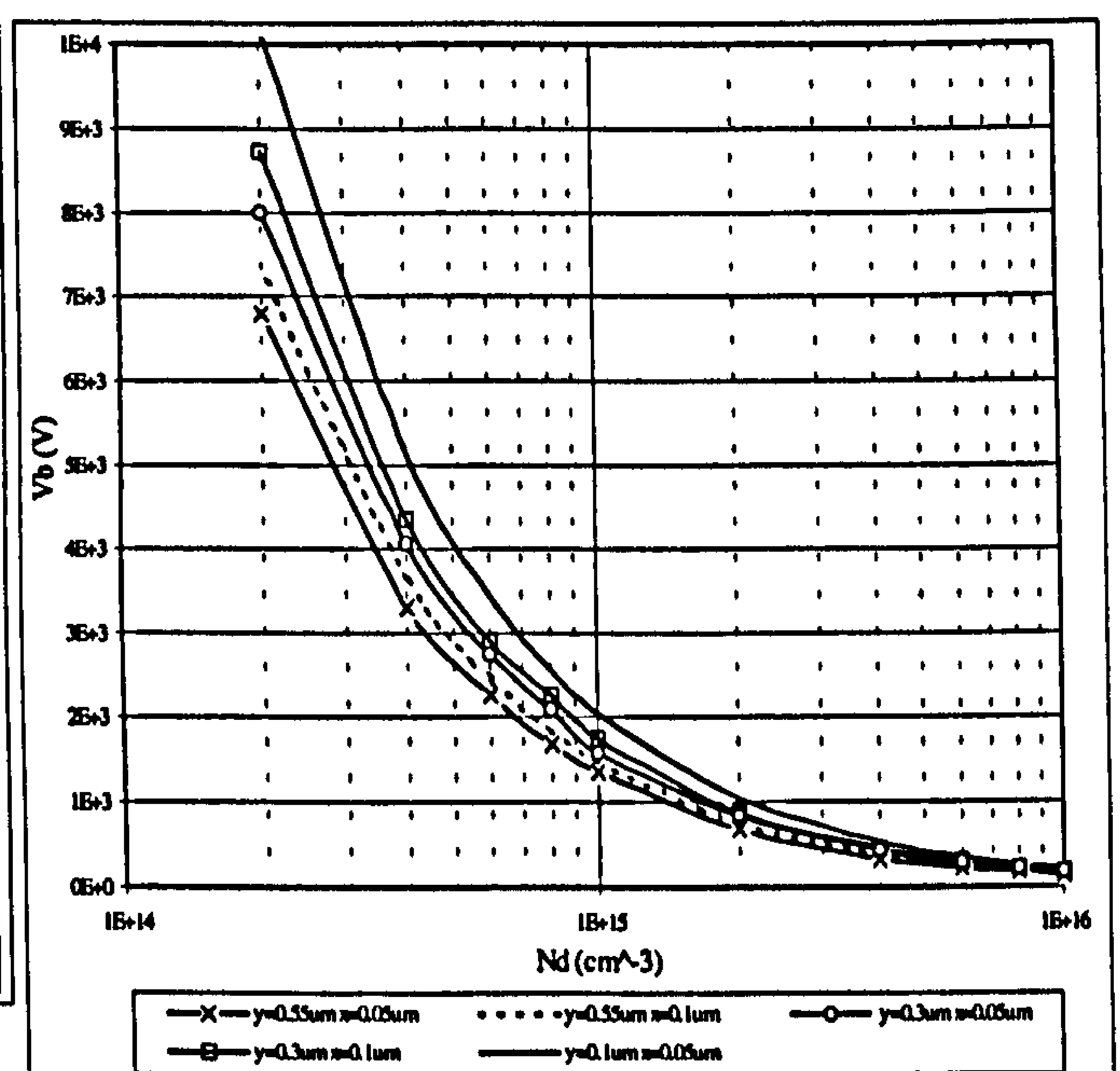

Figure 4.5 Structure parameters' impact on the breakdown voltage of 4H-SiC UMOSFETs at 300K

Although the 4H-SiC UMOSFETs' performance is severely hampered by insulator breakdown and low channel mobility, these devices still have far lower on resistances than Si UMOSFETs in the high breakdown voltage range. In Figure 4.4, the characteristics of 1.2 kV SiC UMOSFETs are compared with the Si IGBT. All the devices modelled have an area of 0.405 cm^2 and the gate voltage is 15V. The Si IGBT's current increases rapidly

after the P-N junction built-in voltage V_{bi} is exceeded. It conducts a current of 100A at the voltage bias of 5V, which is nearly the same as that of a 4H-SiC UMOSFET structure, taking into account the oxide limitation and the low inversion layer electron mobility. When the voltage is raised to 5V, the Si IGBT enters the saturation range. Meanwhile, the 4H-SiC UMOSFET exhibits a quasisaturation characteristic due to the large on-resistance. The current handling capability of an ideal 4H-SiC UMOSFET with an inversion layer electron mobility of 300 cm^2/Vs is far better than that of the Si IGBT. Note that its characteristic, where approriate, is scaled down 3 times. Considering its high switching speed, the 4H-SiC UMOSFET is an attractive replacement for the Si IGBT. Practically, the channel resistance can be reduced by increasing the cell density. Decreasing the cell pitch to 6 μm, which is commercially possible, the channel resistance is 1/6th that of the structure simulated. This has a similar effect to increasing the channel electron mobility.

The overlap of oxide over the N^- drift region y and the oxide bottom thickness x are varied to investigate their effects on the devices' voltage blocking capability. It can be seen from Fig. 4.5 that decreasing y and increasing x improves the devices' voltage blocking capability. At $N_d=2\times10^{14}$ cm^{-3}, a 4H-SiC UMOSFET with y=0.1 μm, x=0.05 μm can block a maximum voltage of 10200V whilst a device with y=0.55 μm, x=0.05 μm breaks down at 6800V, and a device with y=0.55 μm, x=0.1 μm blocks a maximum voltage of 7300V. This phenomenon can be explained by the potential distribution in the drift region. Assuming the potential distribution in the N^- drift region is the same as that in a P^+-N^- junction's N^- region, the potential at the P base/N^- drift junction is 0V and approaches the applied voltage as the distance from the junction increases. So the potential at y=0.55 μm is higher than that at y=0.1 μm. The gate is grounded in the blocking state. This means, the higher the potential at the trench corners, the higher the electric field in the oxide. Hence, a device with a large value of y tends to breakdown at a lower blocking voltage than

one with a small y. On the other hand, for devices with equal values of y, the potentials under the trench bottom are nearly same. A thicker oxide on the trench bottom will relieve field-crowding in the oxide at the trench corners and also increases the breakdown voltage. Interestingly, in Fig. 4.5 all the curves are parallel. Hence the relationship between breakdown voltage and doping can be described by $V_b = aN_d^b$. The exponent is found to be -0.97 by curve fitting.

4.2 Conclusion

The performance of 4H-SiC UMOSFETs taking into account oxide reliability are simulated and analyzed. It is found that the current handling ability of 4H-SiC UMOSFETs is severely hampered by oxide breakdown, but is still superior to those of Si UMOSFETs. Improvement in gate oxide technologies is necessary to realise the advantages of SiC UMOSFETs. It has also been shown that decreasing the gate oxide overlap over the N^- drift region and increasing the trench bottom thickness can improve UMOSFET voltage blocking capability.

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CHAPTER 5

THE 4H-SIC NPN POWER BIPOLAR JUNCTION TRANSISTOR

Progress has been made in SiC material growth and device processing. A 0.8 cm^{-2} micropipe defect density has been demonstrated on a 35 mm wafer [5.1]. A lifetime of 2.1 μs at 300 K and 4.5 μs at 600 K have been reported [5.2]. SiC power devices such as diodes, Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), Junction Field Effect Transistors (JFETs), Static Induction Thyristors (SIThs), Insulated Gate Bipolar Transistors (IGBTs), Gate Turn-Off Thyristors (GTOs), Thyristors and MOS Controlled Thyristors (MCTs) with small areas have been demonstrated [5.3] - [5.10]. However, no reports on the fabrication of power SiC BJTs exist.

The appealing advantages of power MOSFETs, such as switching speed, wide safe operating area (SOA) and ease of drive, have provided the motivation to develop the Silicon Carbide MOSFET. However, suffering from pre-mature insulator breakdown and poor oxide quality, these devices exhibit current handling ability far from theoretical expectations [5.11]. Specifically, taking into account oxide breakdown and assuming the maximum field magnitude in the oxide is 6×10^6 V/cm, the drift region specific on-state resistance is 9 times greater than the theoretical value [5.12]. To address this insulator reliability problem, a few new structures have been proposed or fabricated [5.12]-[5.15]. Up to date, the most significant progress made in SiC MOSFET technology is a 1.8 kV 6H-SiC triple implanted vertical MOSFET with a lateral channel [5.12]. 6H-SiC is used to avoid the much lower lateral channel mobility in 4H-SiC MOSFETs in spite of its relatively higher base specific on-state resistance. The device delivers a drain current of 0.3 A at V_{gs}=10V and V_{ds}=8 V with an area of 1mm^2. Considering the long-term device reliability,

V_{gs} is limited to 10 V so as not to exceed the maximum oxide electric field of 2.5-3 MV/cm. The results represent one eighth the 6H-SiC limit. It is also suggested that in order to achieve the theoretical limit of 4H-SiC MOSFETs, a 25 times enhancement in the inversion layer electron mobility is necessary.

Bipolar Junction Transistors (BJTs) have been commercially available for more than 40 years [5.16]. This device offers a good trade-off between on-state voltage and switching speed. Desirable features include direct control of minority carrier injection, ability to accelerate turn-off with negative base current and normally off behaviour [5.17]. The lack of interest in SiC BJTs originates from the gradual displacement of power Si BJTs by power Si MOSFETs and IGBTs. The incorporation of a high resistivity, thick drift region into the power BJT collector and high level injection occurring at typical operation current densities induce a low current gain for silicon power bipolar transistors. This necessitates use of bulky and expensive base drive circuits. As a result, with the advent of the power MOSFET in the 1970's and the Insulated Gate Bipolar Transistors in the 1980's, application of the Silicon power BJT is diminishing. However, which device type will evolve first depends on both material properties and technology. With the superior properties of SiC, the current gain problem associated with power BJTs will be greatly alleviated. Additionally, the 2.7 V (300K) built-in voltage of the 4H-SiC p-n junction has severely hampered the current handling ability of some SiC bipolar devices such as IGBTs and thyristors, which have an odd number of structure junctions. In bipolar junction transistors, the voltages across the two series p-n junctions offset each other, resulting in a low on-state voltage when the device is operated in the saturation region. Finally, compared to MOSFETs and IGBTs, the SiC BJT is easier to fabricate since oxide quality and manufacturing tolerances are no longer important issues.

In this chapter, the performance of 4H-SiC BJTs is investigated by employing 2-D

numerical simulations [5.18].

5.1 Device Structure

Since the bulk electron mobility in 4H-SiC is twice that of 6H-SiC perpendicular to the c-axis and almost 10 times that of 6H-SiC parallel to the c-axis and it is shown in Chapter 3 that 4H-SiC PiN diodes are better than 6H-SiC PiN diodes, the power switching devices investigated are 4H-SiC based.

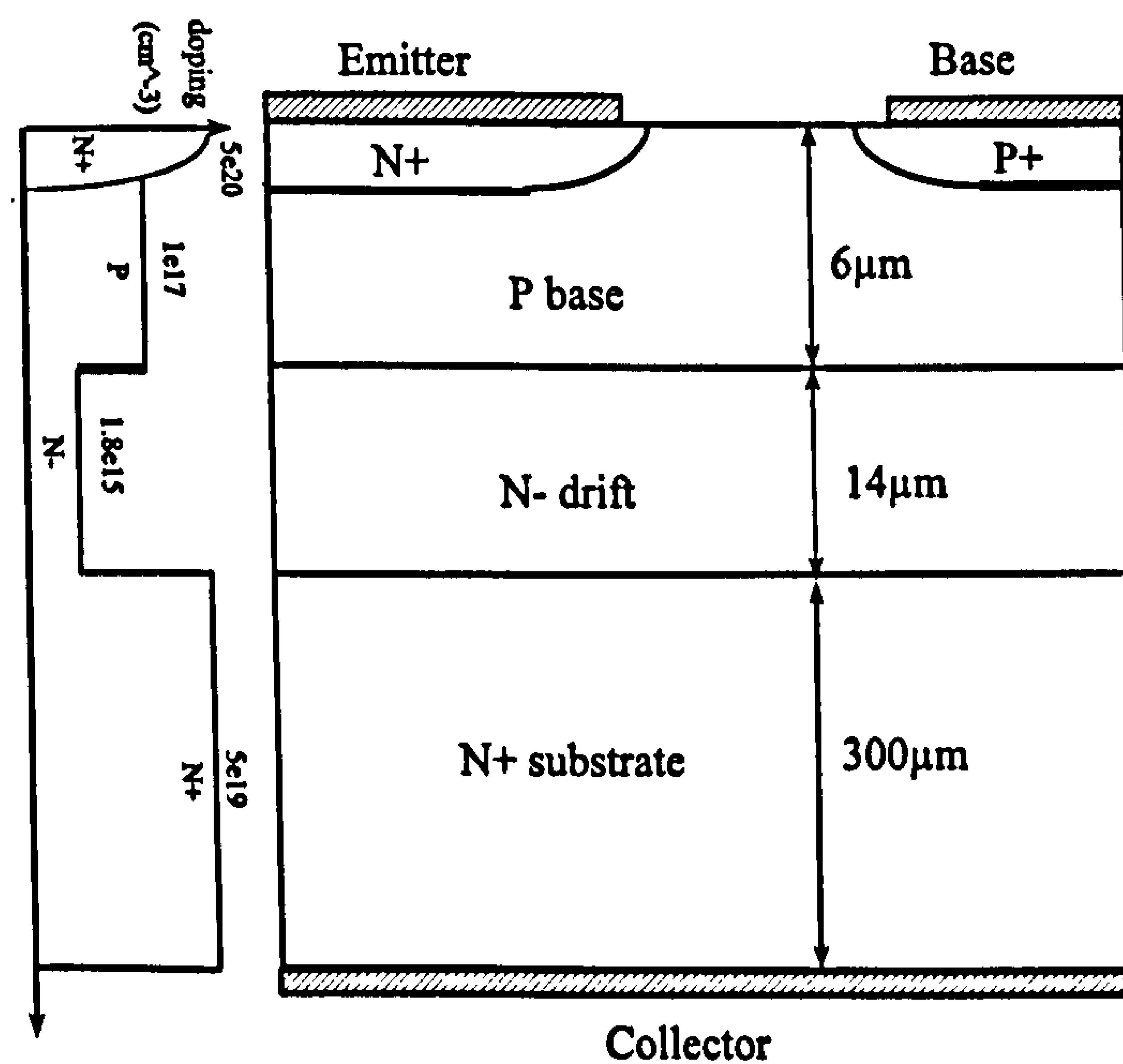


Figure 5.1 The power BJT cell structure

The 4H-SiC NPN BJT structure is defined and plotted in Figure 5.1. A thin, highly doped P^+ region is formed by implantation under the base to reduce contact resistance. The N^+ emitter is realised by shallow ion implantation. An N^- buffer is incorporated between the N^+ collector and the P base to support the high blocking voltage. The devices are designed with a punch-through structure so as to promote high current gain.

5.2 Static Characteristics

5.2.1 Open-Base Blocking Voltage (BV_{ceo})

The open-base blocking voltage BV_{ceo} of the BJT is not only determined by the blocking capability of the reverse biased P base/N collector junction, BV_{cbo}, but also the common-base current gain. The leakage current is amplified by the transistor current gain, hence device avalanche breakdown occurs below BV_{cbo}, when the product of the multiplication factor M and the current gain α reaches unity [5.16]. The expression $BV_{ceo}=BV_{cbo}(1-\alpha_0)^{1/n}$ applies (Figure 5.2), where α_0 is the common-base current gain when open-base breakdown occurs and n is a constant accounting for the material properties and device structure. It is obvious that a high current gain induces a low blocking voltage as illustrated in Figure 5.2. When the temperature increases, the multiplication factor M decrease, because the impact ionization coefficients decrease due to enhanced scattering of free carriers at elevated temperature. In contrast, the carrier lifetime has a positive temperature dependence, which tends to increase the current gain with temperature. On the other hand, the carrier mobilities fall with temperature, mitigating the impact of lifetime on

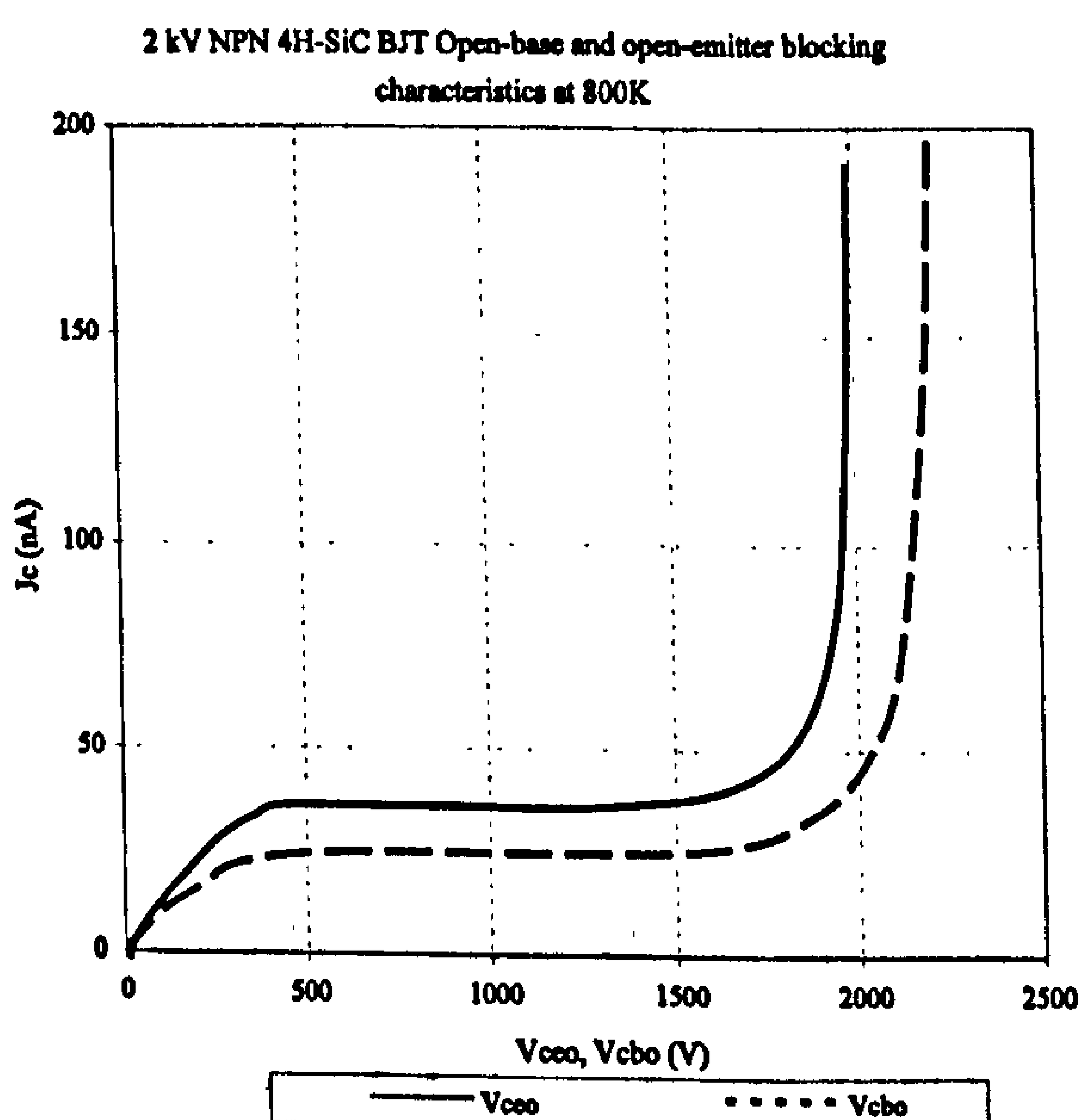


Figure 5.2 2 kV NPN 4H-SiC BJT open-base and open-emitter blocking characteristics at 800K

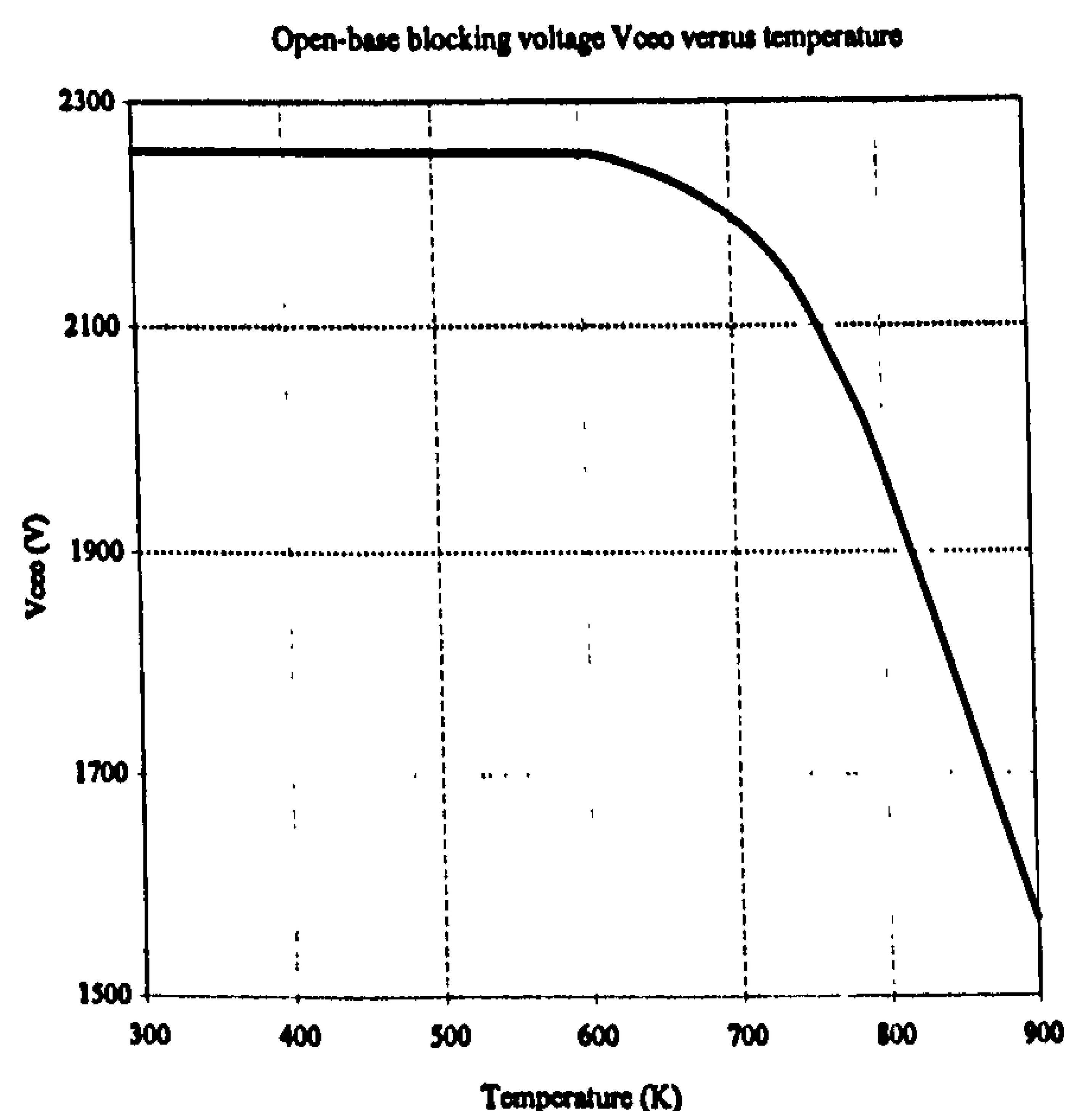


Figure 5.3 BJT open-base blocking voltage V_{ceo} against temperature

current gain.

An unusual feature of SiC devices is their relatively large donor and acceptor ionization energies. The degree of ionization for carriers at room temperature is low, especially for holes. Increasing the temperature promotes the degree of ionization, in turn, this results in a higher emitter injection efficiency. To design a BJT which can block a high collector-emitter voltage reliably, the breakdown voltage must be measured at the maximum operating temperature.

In Figure 5.3, the BJT open-base blocking voltage BV_{ceo} versus temperature is shown. To operate a power device reliably, a positive breakdown voltage temperature dependence is crucial. From 300K to 600K, BV_{ceo} remains nearly constant, which is favoured. However, BV_{ceo} drops, squarely, from 600 K to 900 K. BV_{ceo} at 600K is 480 V higher than that at 900K.

5.2.2 On-State Voltage:- Incomplete Ionization

The incomplete ionization of dopants in SiC devices introduces a relatively high substrate resistivity at room temperature. From Equation (2.14), it is obvious that the higher the doping level the lower the degree of ionization. For the SiC BJT, incomplete ionization causes a relatively low free electron concentration in the emitter, therefore, the emitter injection efficiency is degraded. However, due to the existance of the N^- buffer, the activated electron concentration in the N^+ collector does not have a significant impact on the collector efficiency. In order to achieve a high current gain, the emitter surface doping level is chosen as $5\times10^{20}cm^{-3}$ with a Gaussian doping profile and a junction depth of $1\mu m$.

Figure 5.4 shows the on-state V-I characteristics of a 2 kV NPN BJT with a base current density of 20 A/cm^2. The figure shows how the effect of incomplete ionization hampers the current handling ability of the transistor. At the operating current density, if

the device on-state voltage exhibits a negative temperature coefficient, thermal run-away is likely to occur for large area devices or when paralleling devices. By assuming complete ionization, higher voltages occur at 600K than at 300K, for all collector current densities. As shown in Figure 5.4, from 362 A/cm^2 to 626 A/cm^2, the collector voltage is higher at room temperature than at 600K when considering the incomplete ionization effect. Hence, the device would need to be able to operate at current densities of greater than 626 A/cm^2 if inherent current sharing was to be accomplished.

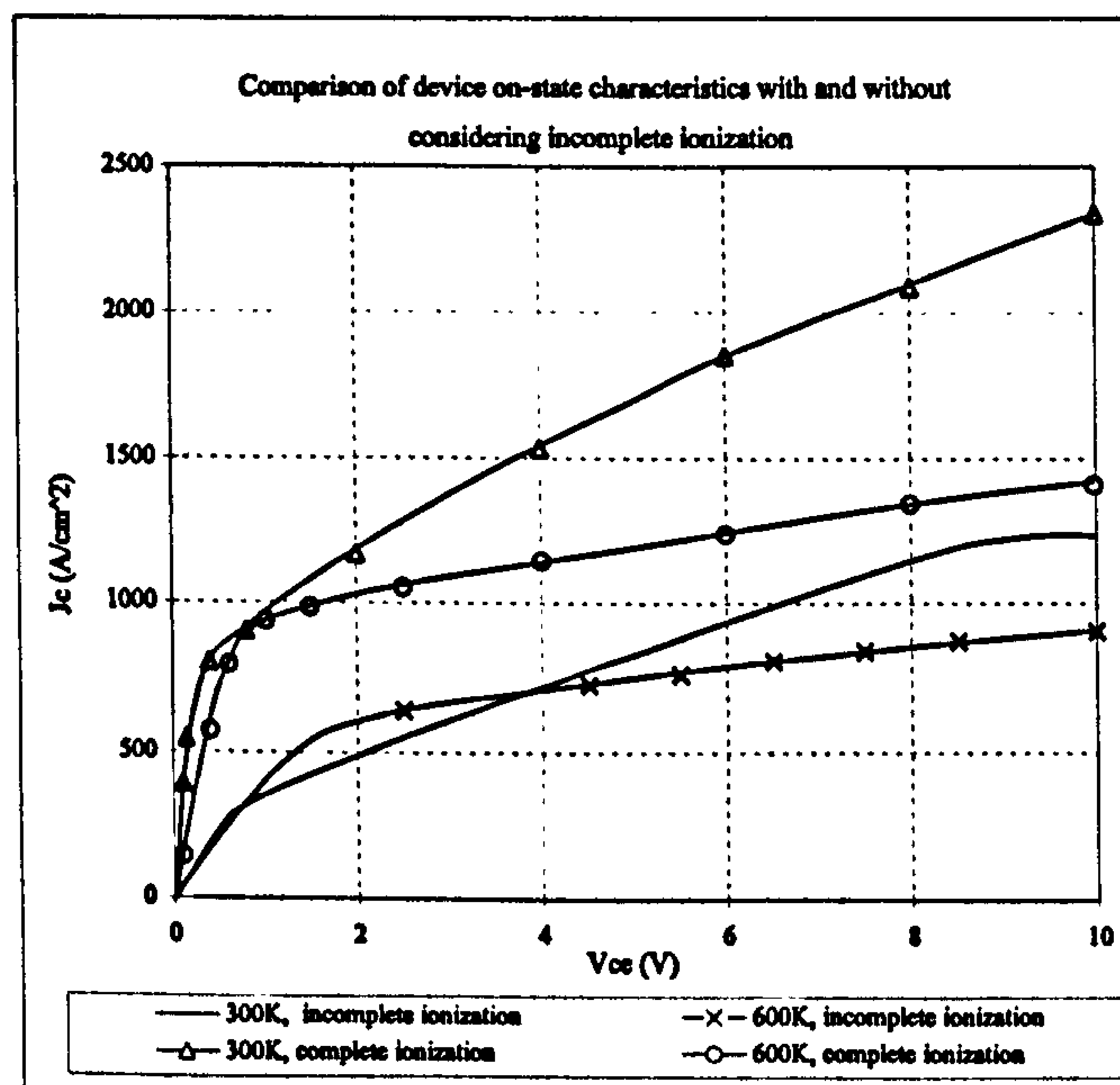


Figure 5.4 Comparison of device on-state characteristics with and without considering incomplete ionization

5.2.3 Current Gain Versus Breakdown Voltage:- Device Structure Parameters

As shown in Section 5.2.1, a high current gain conflicts with a high blocking voltage, therefore, a trade-off between these two device characteristics is necessary. By plotting common-emitter gain β against open-base blocking voltage BV_{ceo}, device characteristics and the corresponding device structure parameters can be seen. Figure 5.5 presents the trade-off curves by changing the device structure parameters: lifetime, P base doping and N$^+$ emitter peak doping. Decreasing the lifetime from 5μs to 2μs, BV_{ceo}

increases 120V while β reduces from 33.5 to 31.3. From 1 μs to 0.2 μs, the rate of BV_{ceo} increase slows down, but β is severely reduced especially for a 0.2 μs lifetime. According to the trade-off curve, a lifetime of 2 μs is suitable and realistic, since a 2.1 μs lifetime for 4H-SiC at room temperature has been reported [5.2]. The current gain β appears to saturate when the P base doping is reduced below $1\times10^{17}cm^{-3}$. Elevating the P base doping above $5\times10^{17}cm^{-3}$ severely degrades the current gain, with only a moderate improvement in the device voltage blocking capability. From the trade-off curve, an N^+ emitter peak doping of $5\times10^{20}cm^{-3}$ is suitable.

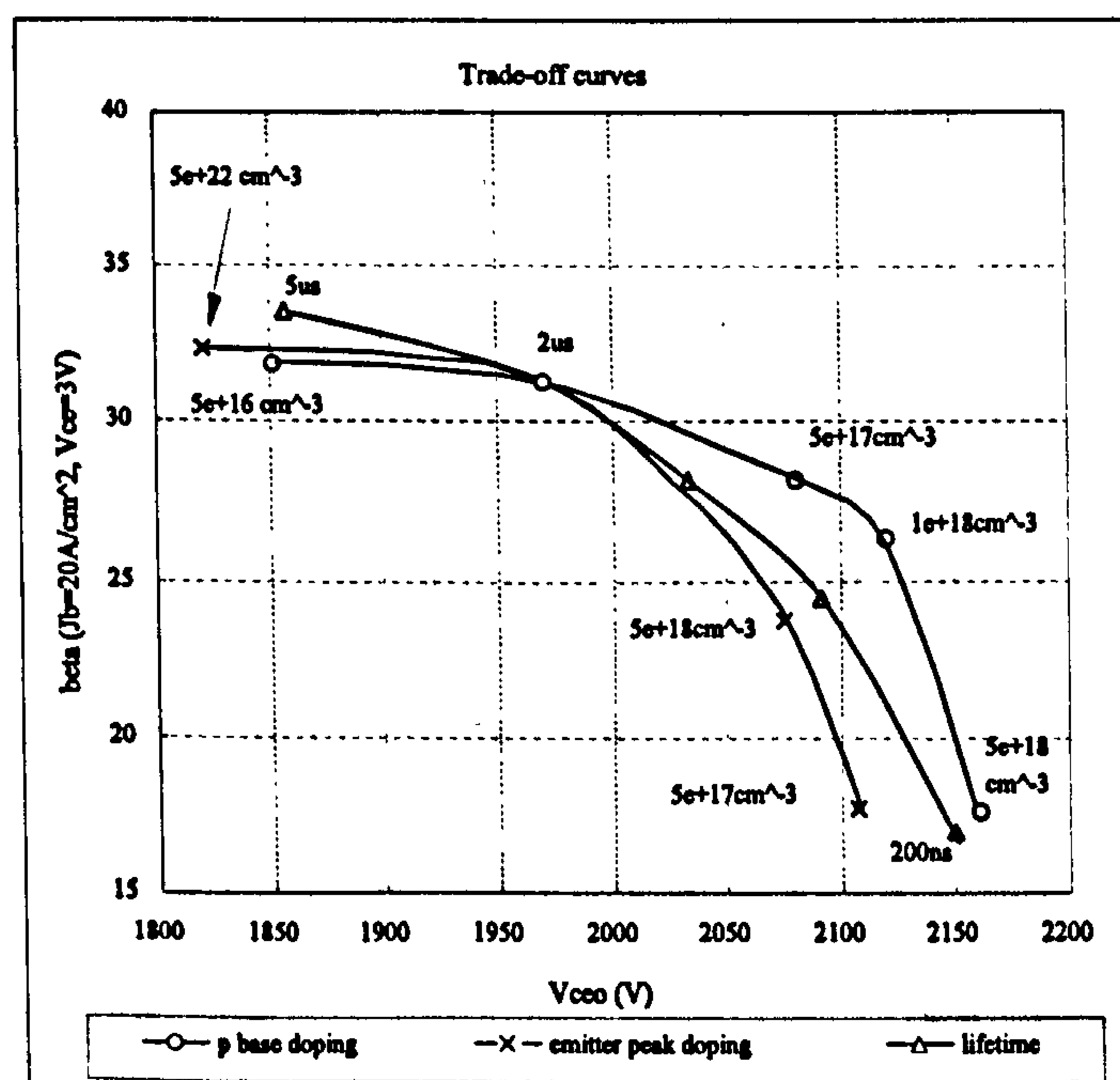
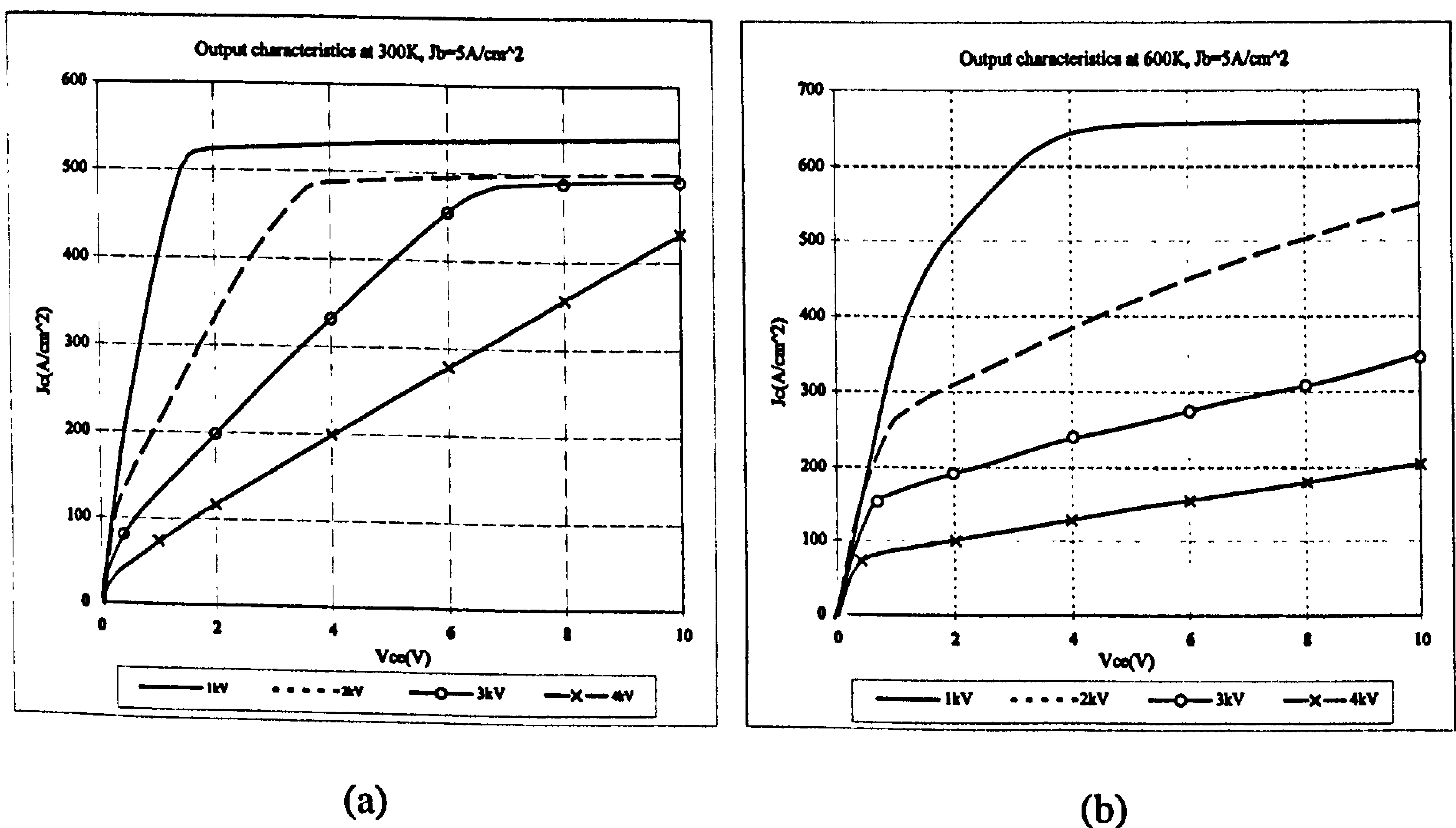


Figure 5.5 BJT trade-off curves

5.2.4 Current Handling Ability versus Voltage Rating

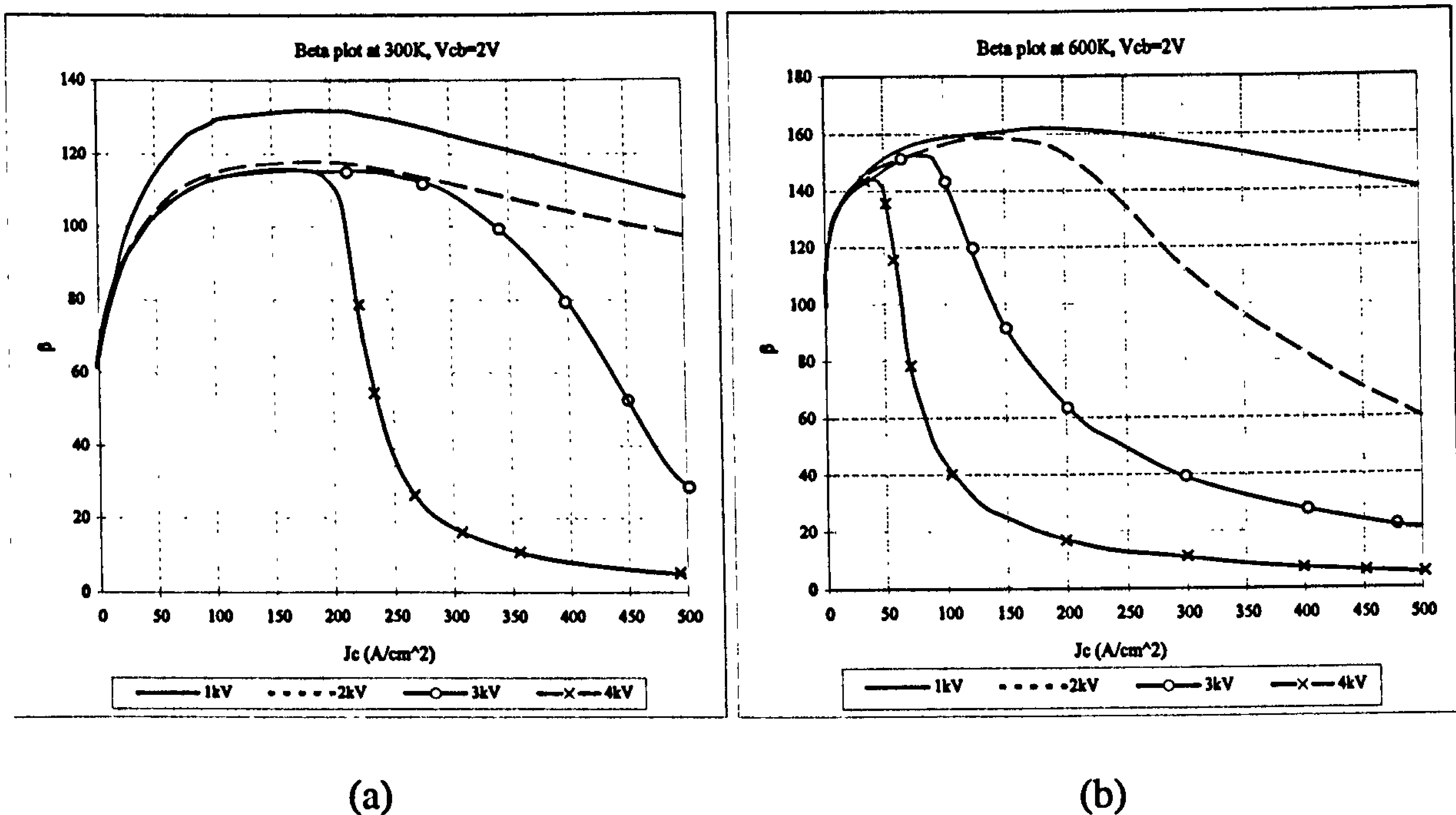
The output characteristics of NPN BJTs with voltage ratings from 1kV to 4kV and a base current density of $5A/cm^2$ are plotted in Figure 5.6. To support a higher blocking voltage, the N^- collector region is widened and the doping level is decreased. This leads to degradation of device current handling ability. As shown, at 300K, the current gain degrades from 103 for the 1kV device to 24 for the 4kV device, when biased at 2 V (v_{cb}). At 600K, these values are 100 and 21 respectively. In the beta plot (Figure 5.7), the

maximum gain and corresponding collector current density decrease with voltage rating. At 300K, the maximum current gain is reduced from 132 for the 1 kV device to 112 for the 4 kV device. The 2, 3 and 4 kV devices all have a similar maximum current gain. By contrast, the maximum gain decreases gradually with voltage rating, from 159 to 144 at 600K. A common feature, independent of temperature, is that the gain fall-off rate after the maximum, increases with voltage rating. This indicates that the current gain becomes more sensitive to the change of collector current density with increased voltage rating. Another critical characteristic is the collector current density at which the maximum current gain occurs. At room temperature, this value is around 200 A/cm^2. This means that to operate the device at 200 A/cm^2 with v_{cb} of 2V at room temperature, a base drive current density of 1.6 to 1.8 A/cm^2 is required ($\beta \approx 120$). However, elevating the temperature to 600K, the collector current density at the maximum current gain is 200, 150, 85 and 45 A/cm^2 for the 1, 2, 3 and 4 kV devices respectively. To drive a 4kV BJT at 200 A/cm^2, v_{cb}=2V and 600K, a 10.5 A/cm^2 base current density must be provided (β=19). The current handling ability of the transistor is affected by both voltage rating and temperature.



(a) (b)

Figure 5.6 4H-SiC NPN BJT output characteristics with Jb=5A/cm^2 at (a) 300K and (b) 600K



(a) (b)

Figure 5.7 4H-SiC BJT Beta plot at V_{cb}=2V, T= (a) 300K and (b) 600K

5.2.5 NPN BJT versus PNP BJT

Due to electron mobility being higher than hole mobility, the NPN BJT N^- collector resistance is smaller than the PNP P^- collector resistance, hence the silicon power NPN BJT is more widely used than the silicon power PNP BJT. To validate the better choice with SiC technology, simulations are performed for 2kV NPN and PNP BJTs. The on-state characteristics of the devices with a 20A/cm^2 base current density are shown in Figure 5.8. It is obvious that the 4H-SiC NPN BJT has superior current handling ability than the 4H-SiC PNP BJT. Another disadvantage of the PNP BJT is that the forward voltage at high temperature is lower than at room temperature. This adversely effects current sharing properties. In Figure 5.9, the carrier and potential distribution for both devices are plotted with J_b=20A/cm^2 and V_{ce}=10V. Obviously, the lower degree of ionization of acceptors induces fewer free carriers in the PNP emitter and substrate than in an NPN device. The base/collector junction in both devices is reversed biased. However, the main voltage drop in the PNP BJT is across the base/collector junction. By contrast, in an NPN BJT the main voltage drop is the ohmic voltage across the N^- drift region.

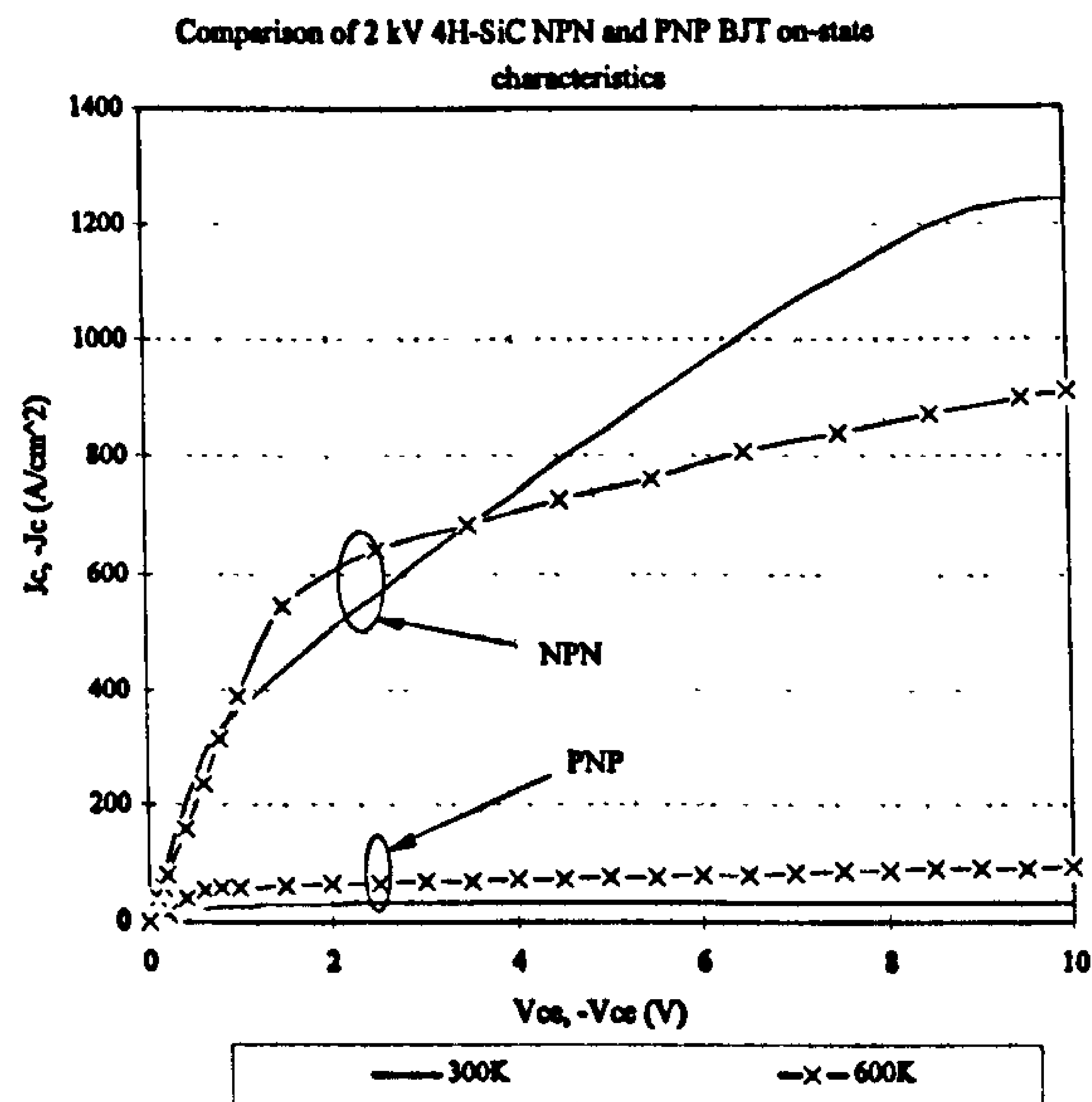


Figure 5.8 Comparison of 2 kV 4H-SiC NPN and PNP BJT on-state characteristics with J_b=20A/cm^2

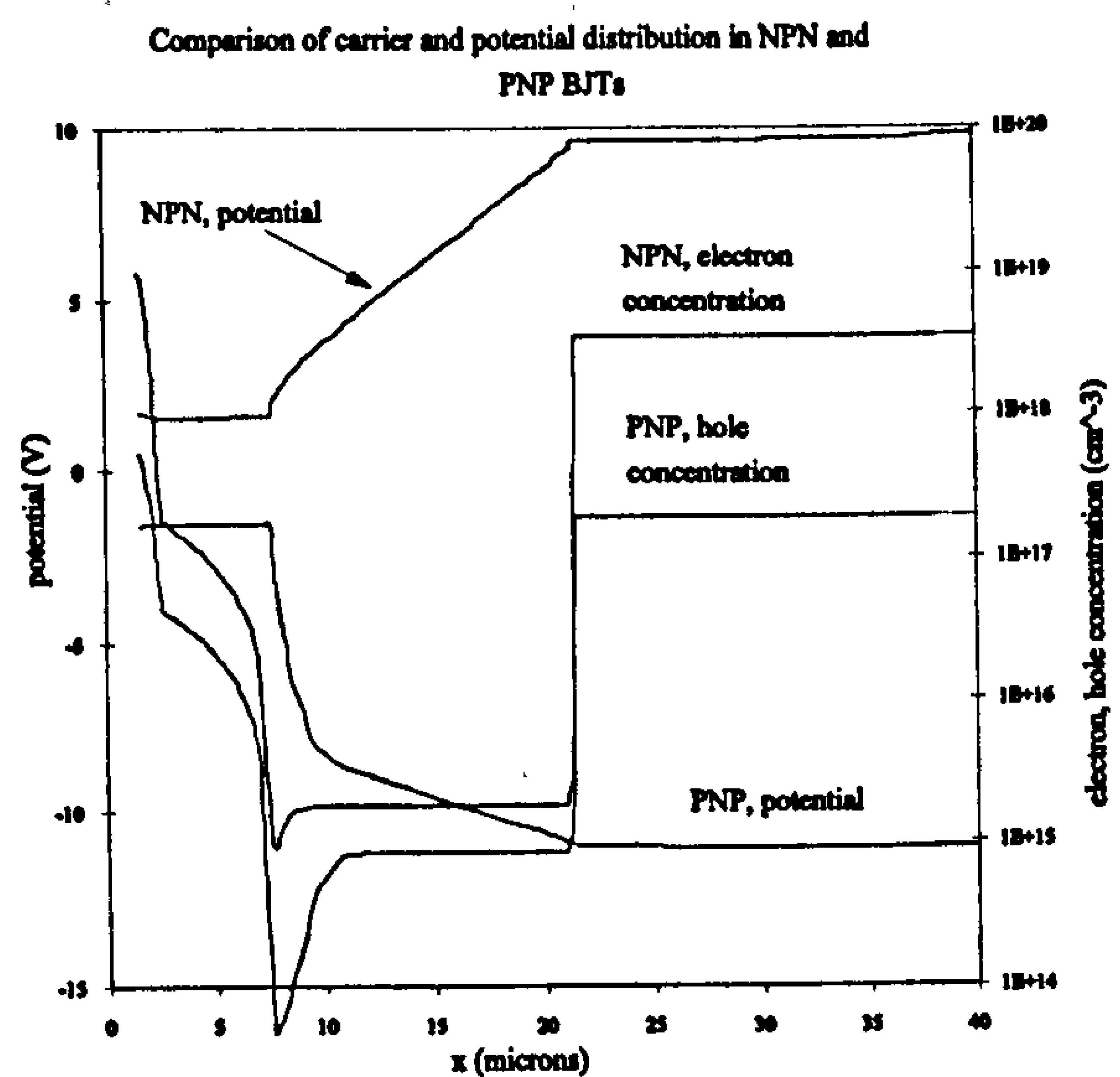


Figure 5.9 Comparison of carrier and potential distribution in NPN and PNP BJTs

5.2.6 BJT versus MOSFET

As a unipolar device, the current handling ability of a high voltage MOSFET is primarily affected by the resistance of the N^- drift region and its lack of conductivity modulation. It is projected that the SiC MOSFET voltage application range can extend to 4.5 kV [5.14]. However, the current development of the SiC MOSFET suffers from two major problems: low inversion layer mobility and insulator reliability. The highest inversion layer mobility for a vertical SiC MOSFET was reported as 26 V·cm^2/s [5.19]. Because of the absence of the JFET region in the silicon Trenched Gate MOSFET (UMOSFET), this structure is demonstrated to have a much lower specific on-state resistance than a silicon Double Diffused MOSFET (DMOSFET). Unfortunately, with SiC, the UMOSFET suffers from a more severe oxide reliability problem than the DMOSFET. The electric field in the oxide can approach 1×10^7 V/cm at the trench corners. This leads to oxide rupture well before the avalanche breakdown voltage is reached. To obtain a specific voltage blocking capability, the drift region doping has to be decreased to lower the maximum electric field. Adversely, as shown in Chapter 4, the on-state specific

resistance is raised. With the DMOSFET structure, this problem is alleviated to some extent, but it inherently exhibits a higher on-state resistance because of the JFET region resistance and the accumulation layer resistance.

The simulated on-state characteristics of the SiC UMOSFET, accounting for low inversion layer mobility, are presented in Figure 5.10. The oxide breakdown limitation is not considered. The effective inversion layer mobility is measured at V_{gs}=15 V and V_{ds}=0.1 V and 300 K. In the typical operating region, BJT forward voltages are lower, even with an effective inversion layer mobility of 150 Vcm^2/s for the UMOSFET. At 200 A/cm^2, with a base current of 20 A/cm^2, the BJT has a 0.4 V on-state voltage, while the UMOSFET with an effective inversion layer mobility, as high as 50 Vcm^2/s, supports 4 V. In Figure 5.11, the on-state voltages of UMOSFETs and BJTs in the voltage range of 1 to 4 kV at 200A/cm^2 are compared. The SiC UMOSFET shows a strong temperature and voltage rating dependence. The 1 kV UMOSFET with effective inversion layer mobilities of 50, 100, 150 Vcm^2/s exhibits a v_{ds} of 3.5, 1.5, 1 V at 300K and 4.4, 2.5, 2 V at 600K. The 4 kV UMOSFET exhibits a v_{ds} of 7.2, 5.2, 4.6 V at 300K and 18, 16.4, 16 V at 600K, which

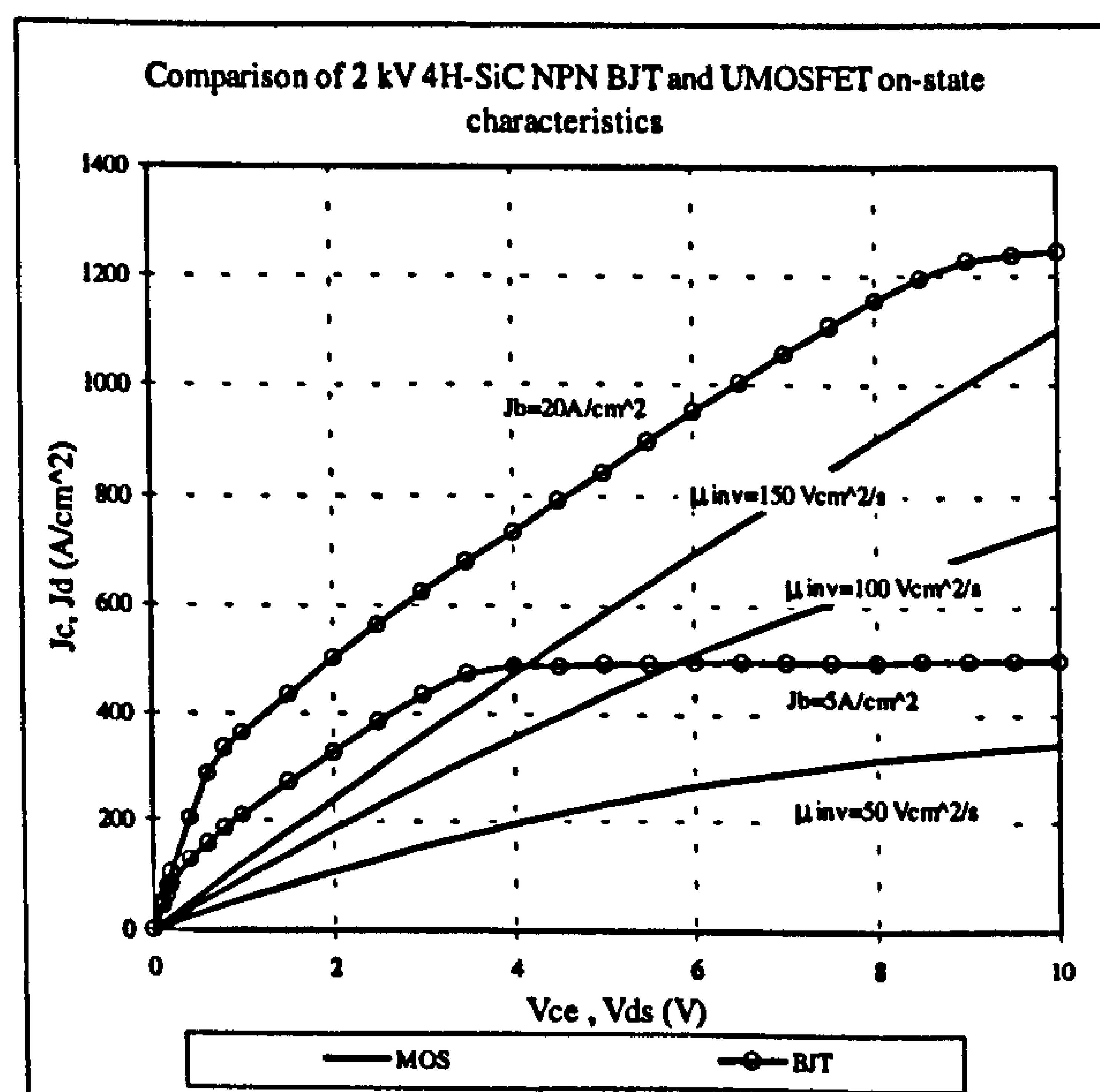


Figure 5.10 Comparison of 2kV 4H-SiC NPN BJT and UMOSFET on-state characteristics at 300K

are unacceptably high for practical use. Elevating v_{gs} to 20V improves the MOSFET current handling ability at room temperature slightly, but has minimal impact at 600K. The current handling ability of SiC BJTs is also affected by voltage rating and temperature. However, with conductivity modulation, the dependence is less. With J_b=20A/cm^2, the on-state voltage is less than 1V at room temperature and less than 2.5V at 600K. Decreasing J_b to 10A/cm^2, the on-state voltage is still less than 3.5 V except for the 4kV device at 600K, where V_{ce} is about 5.7 V. From 3 kV, the 4H-SiC UMOSFET behaves like a resistor, indicating that the drift region resistance is a major current limiting factor. If, not withstanding the practical MOSFET insulator reliability problem, the drift region doping is decreased and the width increased, then the on-state characteristics of the SiC UMOSFET deteriorate further. This makes the current handling ability of SiC BJTs more attractive.

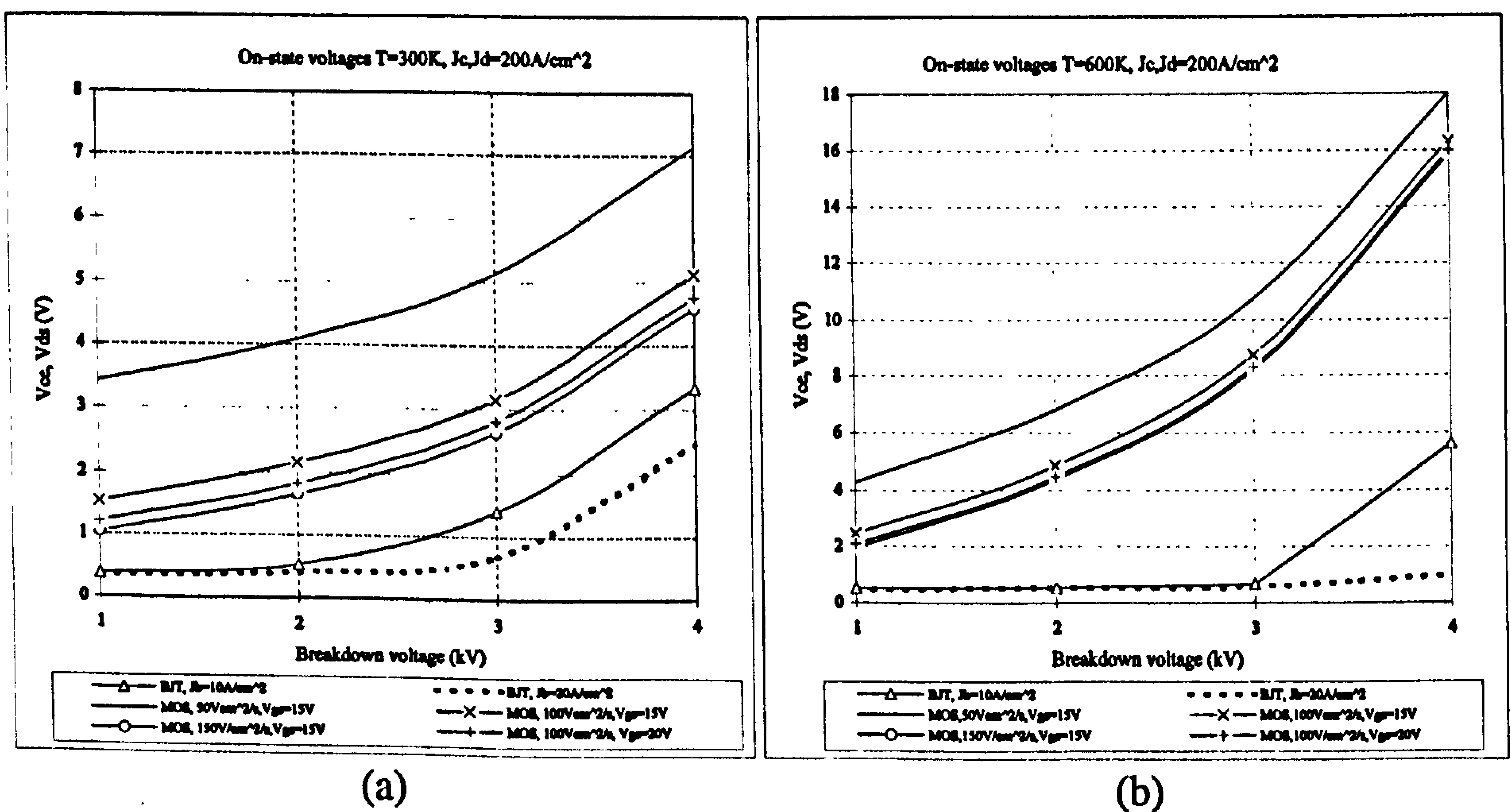
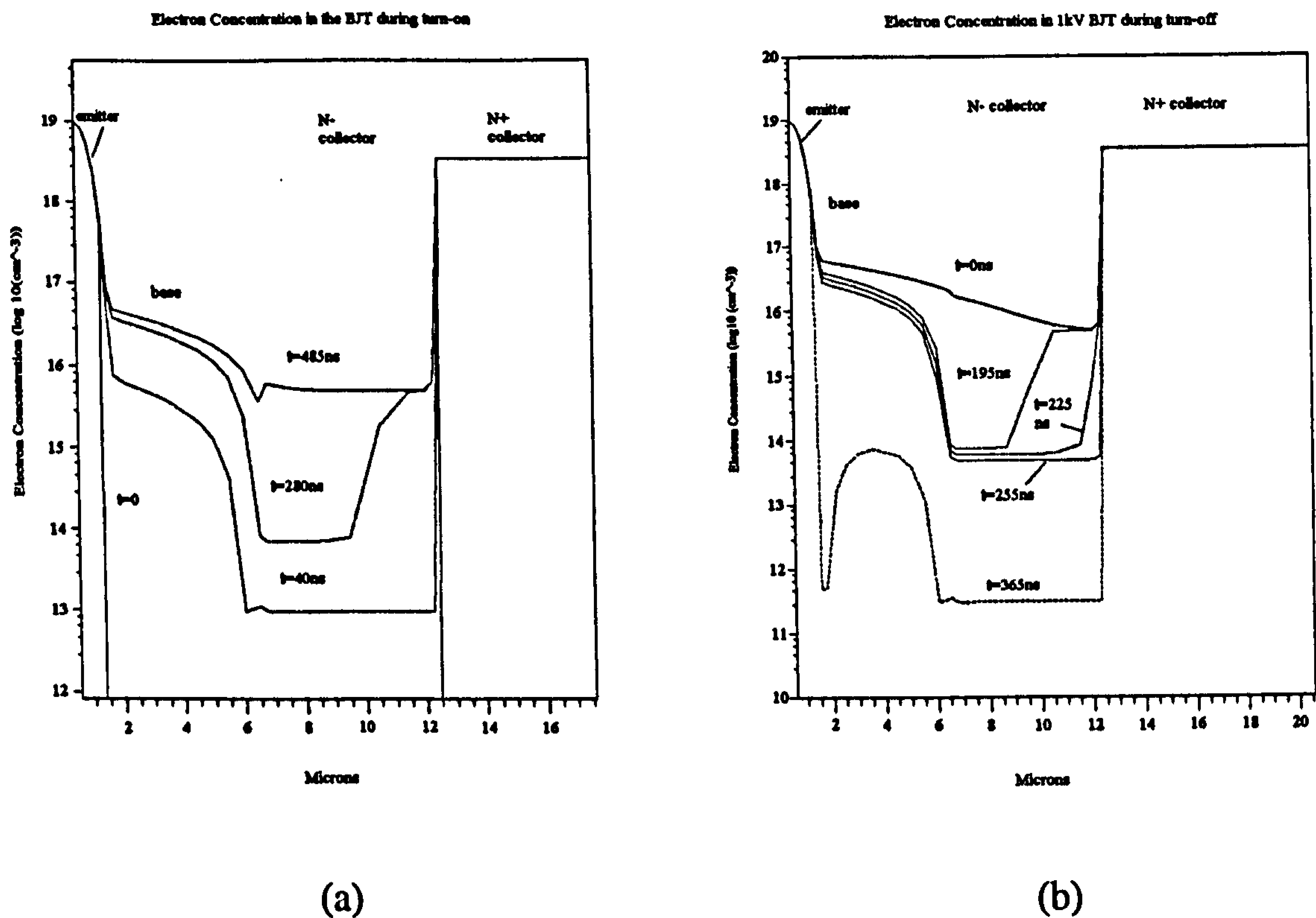


Figure 5.11 4H-SiC device on-state voltages against voltage rating with 200A/cm^2 on-state current density at (a) 300K and (b) 600K

5.3 Switching Characteristics

In Section 5.2, it was shown that the current gain of the 4H-SiC BJT is high, thereby

avoiding the need of a bulky and expensive base drive circuit. It has a better current handling ability than the UMOSFET, which results in a much lower on-state power loss.



(a) (b)

Figure 5.12 Electron distribution in 1kV 4H-SiC NPN BJT at 300K during (a) turn-on and (b) turn-off

In Figure 5.12, the electron concentration in a 1 kV BJT during turn-on and turn-off is shown. In the off-state, the electron concentration in the base is extremely low because of the wide bandgap of 4H-SiC. In the N^- collector, electrons are swept out because of the high electric field caused by the high blocking voltage. During turn-on, after a 34ns delay, the collector-emitter voltage decreases by 84% in 246ns. At 485ns, the base and N^- collector are flooded with excess carriers. Electrons are injected into the base faster than into the N^- collector and the electron concentration in the base in the on-state is larger than in the N^- region. During turn-off, the base excess carriers are extracted by the base current and gradually decay via recombination, while the depletion layer in the N^- region is formed

immediately after the storage phase.

5.3.1 BJT versus MOSFET

For high frequency applications, switching speed and switching loss are critical characteristics in measuring device performance. As a unipolar device, the switching speed of the UMOSFET is dominated by the charging and discharging times of the parasitic capacitances. The BJT, on the other hand, has stored minority carriers to reduce resistivity, which must be removed or injected during switching. Fortunately, before the switching transients occur, the base current injects or extracts a large amount of excess carriers. As a result, the collector voltage and current can be switched rapidly, leading to a low switching power loss compared to other kinds of bipolar devices.

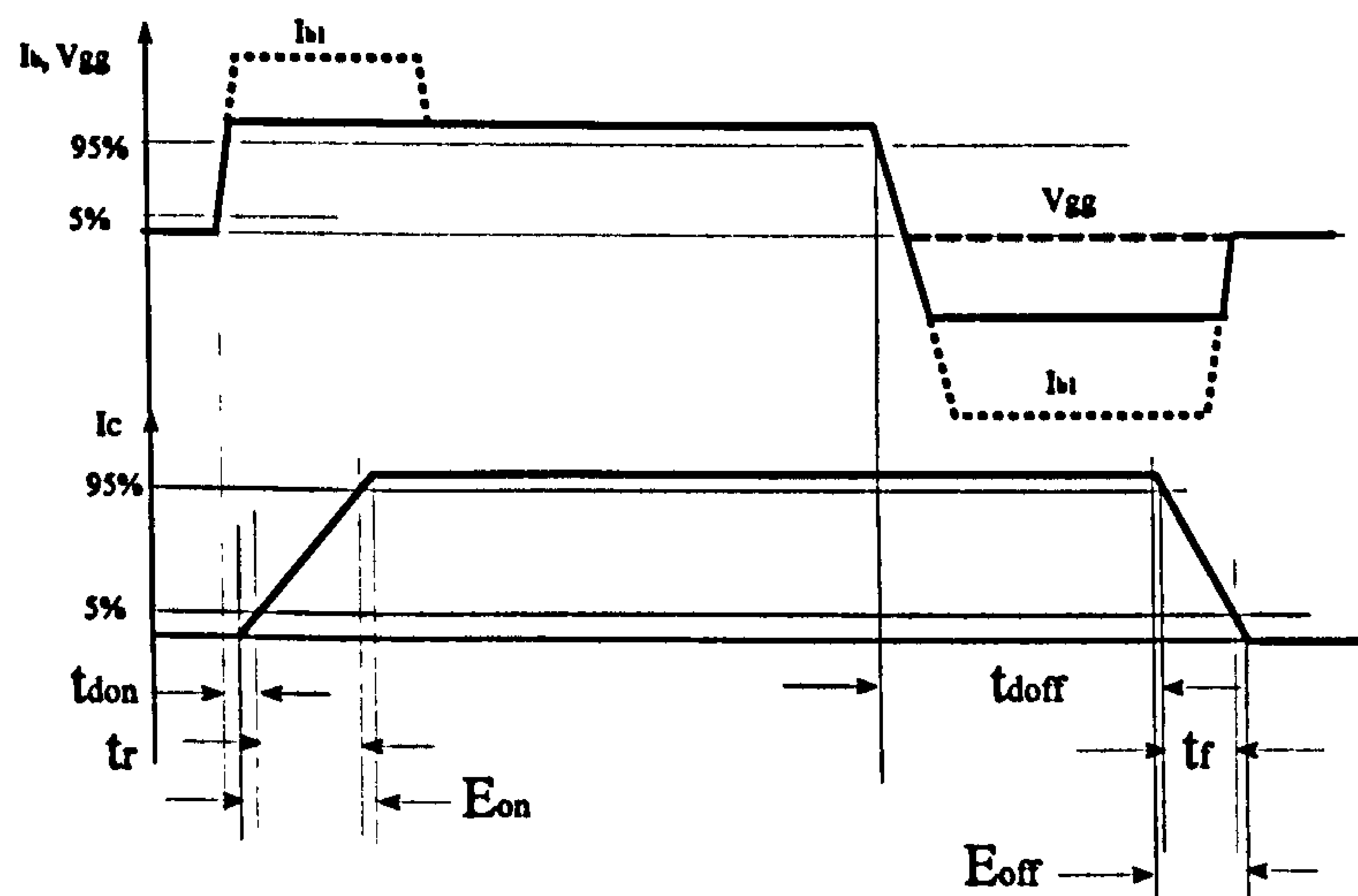
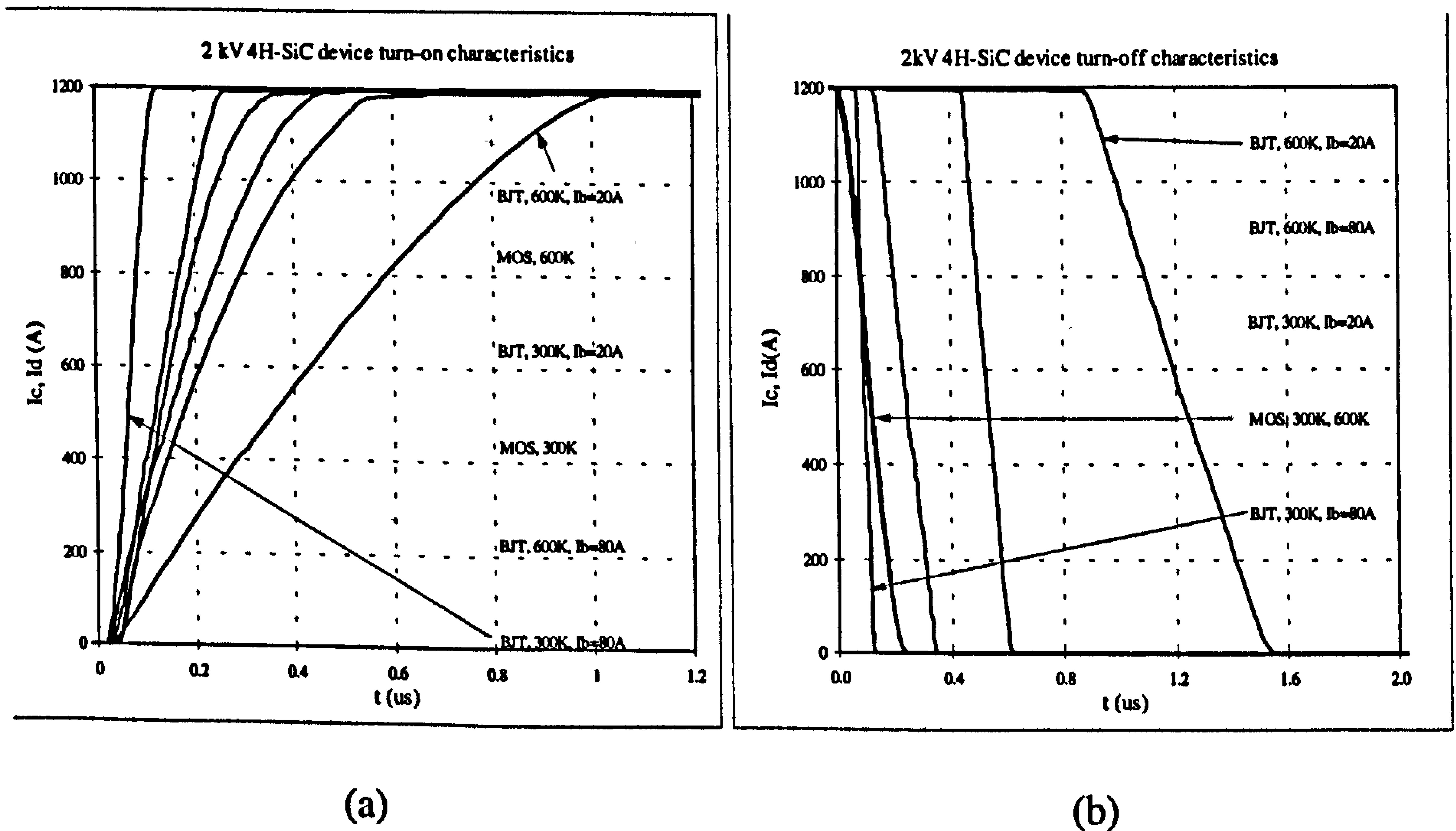


Figure 5.13 Definition of the switching time

To compare the switching performance of the 4H-SiC UMOSFET and BJT, mixed-mode numerical simulations are conducted. The numerical physically-based device simulation in conjunction with a conventional circuit simulation for the rest of the circuit, accurately predicts circuit behaviour. The typical application circuit for power switches involves a hard switched circuit with a clamped inductive load. However, due to the

instability introduced by the compact diode model in the simulator, the simulated switching characteristics of the diode do not reflect the real situation. Also diode characteristics dominate hard switching inductive turn-on. In addition, this work is of a comparative nature. Hence, the switching performance of the devices are simulated for a resistive load circuit.

The DC link voltage is half the device voltage rating and the load current is 1.2 kA. The UMOSFET gate circuit resistance is 1 Ω and the gate drive voltage is changed between 0 and 15 V to switch. The effective inversion layer mobility is 100 Vcm²/s for the MOSFET. The base drive current is changed between I_{bf} and $I_{br}=-I_{bf}$ to switch the BJT. The BJT negative base current is only a transient requirement during turn-off. All device areas are 4 cm². The various switching times and power losses are defined in Figure 5.13.



(a) (b)

Figure 5.14 2 kV 4H-SiC device switching characteristics (a) turn-on and (b) turn-off

The switching characteristics of the 4H-SiC devices are shown in Figure 5.14. BJT turn-off power loss is smaller than its turn-on power loss, although the turn-off processes have a longer time duration if the storage phase is included. In the storage phase, the

negative base current extracts a large number of excess carriers from the drift region until the minority carrier concentration in the N^- drift/P base junction drops nearly to zero. Then the collector voltage supported by the device begins to increase to the supply voltage. Because the remaining minority carriers in the drift region are relatively few compared to the on-state, this phase completes quickly, resulting in lower turn-off power loss than at turn-on. With the MOSFET, no storage time at turn-off is observed with $R_g=1\Omega$. In contrast to its current handling ability, BJT switching speed has a strong temperature dependence. The turn-on speed and power loss of the MOSFET increase with temperature, while turn-off speed and loss change slightly.

As shown in Figure 5.14, when a 20 A base current is used to switch the BJT, its switching speed is slower than the MOSFET, with larger switching power losses, especially at elevated temperatures. At 600K, a 1 μs storage time and a 500 ns current falling time are obtained. If an 80 A, 1μs initial base current I_{b1} is used to switch the BJT and the base drive current during the steady state, I_{b2}, falls back to 20 A, then BJT switching improves. In this case, the BJT turn-on speed at both temperatures is faster than the MOSFET turn-on speed at 300K. Although the BJT turn-off speed at 600K is still slower than the MOSFET due to the storage phase, the power loss is smaller (Table 5.1). Besides, the BJT on-state voltage is 1.8 V and 1.9 V at 300 K and 600 K respectively, while for the UMOSFET the corresponding voltages are 3.3 V and 7.4 V respectively.

5.3.2 Switching Speed and Power Loss versus Voltage Rating

In Table 5.2, the dependence of switching time and power loss on voltage rating is presented. The areas for the 1 to 4 kV devices are 3, 4, 4.8 and 6 cm^2 respectively thereby maintaining the 1.2 kA rating. The base drive currents for the BJT are chosen as 12, 20, 36, 90A to obtain on-state voltages of less than 4V. The gate drive voltage for the

MOSFET is changed between 0V and 15V. While the voltage rating increases, the BJT current handling ability degrades hence the current density is reduced and a larger base current is required to maintain an on-state voltage of less than 4V. This leads to a shorter turn-on time. Since no storage time is observed at turn-on, this faster turn-on results in a lower power loss. In comparison, MOSFET switching speed depends strongly on device area: larger device area, longer charging and discharging times, hence higher power losses.

Table 5.1 Main Result of 2 kV 4H-SiC Device Performance at 1.2 kA

T(K)		V_{on}(V)	t_{don}(ns)	t_r(ns)	t_{doff}(ns)	t_f(ns)	E_{on}(mJ)	E_{off}(mJ)
300	BJT, I_{b1}=20 A	1.75	31	312	153	166	80	42
	BJT, I_{b1}=80 A	1.75	22	69	72	42	20	11
	MOS	3.3	59	213	46	145	56	37
600	BJT, I_{b1}=20 A	1.9	99	748	976	506	190	130
	BJT, I_{b1}=80 A	1.9	50	167	460	120	44	33
	MOS	7.4	57	388	35	152	100	44

The 1 and 2 kV BJTs have longer turn-on times and higher turn-on power loss than the corresponding MOSFET, but 3 and 4 kV BJTs have smaller turn-on times and lower turn-on power losses. BJT turn-off times are longer than for the MOSFET because of the storage phase. However, the turn-off power losses are not always larger than the MOSFET. The 4kV BJT exhibits a turn-off power loss of 19 mJ at 300K, which is much smaller than the 110mJ of the MOSFET. The 4kV MOSFET has a voltage drop of 5.2 and 16.3 V at 300K and 600K respectively, indicating that a 200A/cm^2 current density is too high for a 4kV MOSFET. To obtain a reasonable on-state voltage, the device area must be enlarged.

Unfortunately this slows down switching. The switching speed of the BJT can be enhanced by using a larger base current during switching, then reduced base current during steady state. The BJT switching performance is improved significantly as demonstrated in Figure 5.14 and Table 5.1, although this base current specification complicates the base drive circuit. The short term switching current pulse, I_{b1}, is also benefical in reducing desaturation during diode reverse recovery when hard switching inductive loads.

Table 5.2 4H-SiC Device Switching Results versus Voltage Rating at 1.2 kA

	Voltage rating (kV)	BJT 300K	BJT 600K	MOS 300K	MOS 600K
t_{on} (μs)	1	0.65	1.56	0.24	0.4
	2	0.34	0.85	0.27	0.44
	3	0.18	0.48	0.3	0.5
	4	0.08	0.22	0.34	0.58
t_{off} (μs)	1	0.26	1	0.14	0.18
	2	0.32	1.48	0.2	0.19
	3	0.36	2.05	0.27	0.3
	4	0.43	3.02	0.29	0.33
E_{on} (mJ)	1	78	180	28	49
	2	80	190	56	106
	3	58	148	91	164
	4	31	105	136	250
E_{off} (mJ)	1	33	94	14	17
	2	42	130	40	40
	3	37	114	67	74
	4	19	65	110	116

5.4 Conclusion

The static and dynamic performance of 1 to 4 kV 4H-SiC NPN BJTs has been investigated by 2-D numerical simulations. The Si BJT current gain degradation problem is greatly alleviated because of the much thinner drift region width and much higher drift region doping in SiC BJTs. Device characteristics: open-base voltage blocking capability, current handling ability, switching speed and effects of incomplete ionization, device structure parameters and voltage rating on the device performance were studied. It was found that the NPN BJT is a better choice than the PNP BJT with SiC technology. The BJT exhibits much better current handling ability than, and comparable switching speed to, the corresponding 4H-SiC UMOSFET. Considering the relative ease of fabricating a SiC BJT, it is a more suitable candidate than the SiC MOSFET for high voltage (1 kV to 4 kV), high current and high frequency applications in the near future.

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CHAPTER 6

HIGH-VOLTAGE 4H-SIC IGBTS

The advent of the Insulated-Gate Bipolar Transistor (IGBT) solved the main problem of the silicon Metal Oxide-Semiconductor Field-Effect Transistor (MOSFET): that of rapid degradation of the current handling ability with increased voltage rating. Being a minority carrier device, the current handling ability of the IGBT is not affected by the resistivity of the drift region as severely as with the MOSFET. Sharing many of the appealing features of power MOSFETs, such as ease of drive, wide Safe Operation Area (SOA), peak current capability and ruggedness, silicon IGBTs have displaced silicon Bipolar Junction Transistors (BJTs) in medium and high voltage applications.

However, their current handling ability can not compete with silicon thyristors and Gate Turn-off (GTO) Thyristors. Currently, the silicon thyristor is the only device available meeting the power rating requirement of modern High Voltage Direct Current (HVDC) transmission systems. The phase-controlled three-phase full-bridge converter used in HVDC has many disadvantages such as low power factor under deep control and high harmonic components. Nevertheless, to turn off the thyristor, the voltage across the device must reverse, thereby limiting the kinds of converter configurations that can be used. If high voltage SiC IGBTs are commercially available in the future, the conventional phase-controlled three-phase full-bridge converters used in HVDC systems can be replaced by other kinds of converters with better performance, in which Punch-through (PT) IGBTs can be employed to minimize device power losses.

SiC bipolar devices exhibit a relative high built-in voltage (2.7V) compared to their silicon counterparts (0.7V), hence, the on-state voltage drop is at least 2.7V, mitigating the

conductivity modulation property of bipolar devices. In addition SiC unipolar devices show much lower specific on resistances than their silicon counterparts. As a consequence SiC IGBTs with low and medium voltage rating are not projected to compete with SiC MOSFETs and BJTs. The same applies to the corresponding silicon devices.

For the reasons stated above, this chapter aims at investigating the performance of high voltage (especially above 5 kV) 4H-SiC IGBTs by employing a 2-D physically-based numerical simulation package [6.1] and a 2-D on-state analytical IGBT model [6.2] respectively. Different IGBT structures are studied.

6.1 Results and Discussion

6.1.1 Threshold Voltage

Figure 6.1 shows the typical structure of an IGBT. In IGBTs, an inversion layer will form in the P/N base region under the gate oxide after the gate-emitter voltage V_{ge} exceeds the threshold voltage V_{th}. In an N-channel IGBT, electrons flow from the N^+ emitter region to the N base region through this channel, providing the base current for the integral $P\text{-}N\text{-}P^+$ transistor. The threshold voltage V_{th} for an N-channel MOS structure without considering the effects of fixed surface charge, mobile ions in the oxide and charged surface states at the oxide-silicon interface, is given by [6.3]:

$$V_{th}=\frac{t_{ox}}{\varepsilon_{ox}}(4qN_a\varepsilon_s V_{fp})^{1/2}+V_{ms}+2V_{fp} \tag{6.1}$$

where

N_a: doping level of P base

ε_s, ε_{ox}: permittivity of semiconductor and silicon dioxide, respectively

V_{fp}: difference between Fermi level and intrinsic Fermi level

t_{ox}: thickness of silicon dioxide

V_{ms}: metal-semiconductor function difference.

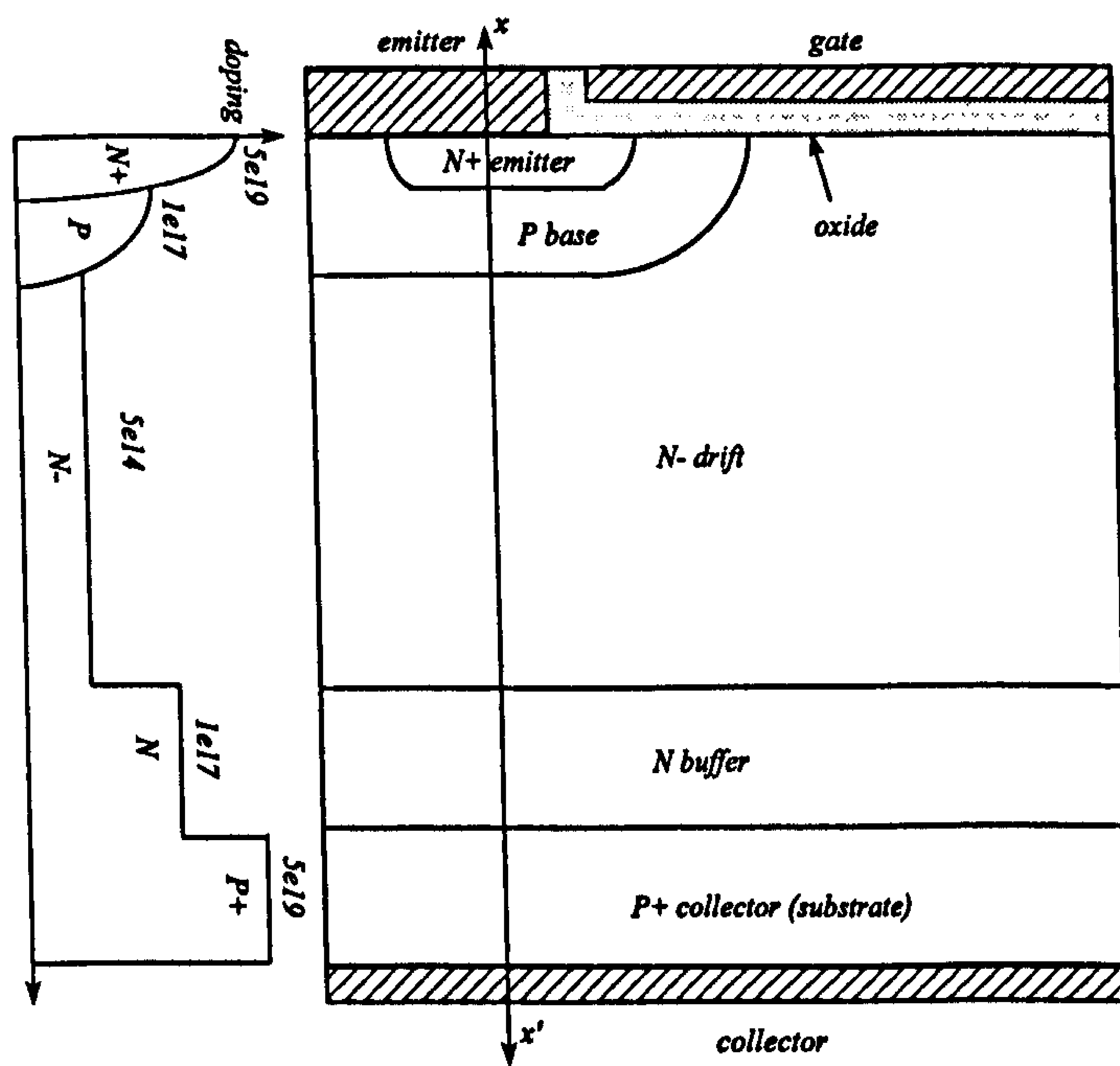


Figure 6.1 (a) A typical N-channel Punch-Through DMOS IGBT cell structure and typical doping profile

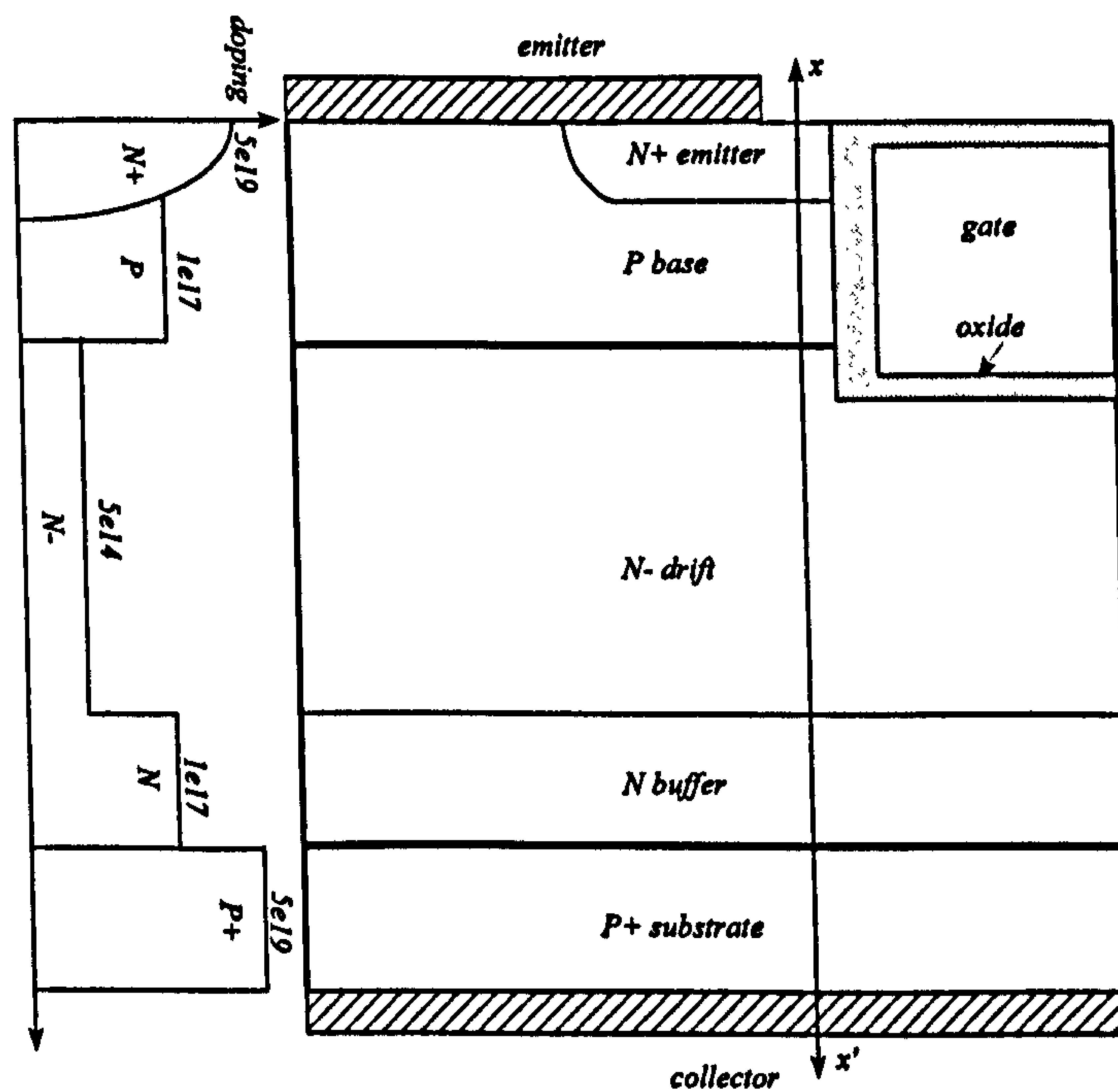


Figure 6.1 (b) A typical N-channel Punch-Through TIGBT cell structure and typical doping profile

Figure 6.2 shows N channel SiC IGBT threshold voltage plotted against P base doping level at 300 K with N^+ polysilicon as the insulator and an oxide thickness of 500 Å. Silicon IGBT threshold voltages are also shown for comparison. It can be seen that the

threshold voltages of SiC IGBTs are higher than the corresponding silicon devices. This is mainly caused by the higher V_{fp} for SiC, which is given by:

$$V_{fp} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{6.2}$$

where N_a is the doping level and n_i is the intrinsic carrier concentration. Due to the wide bandgap of SiC, its intrinsic carrier concentration is extremely low, only 2.2×10^{-9} cm^{-3} at 300K. In contrast, the intrinsic carrier concentration for silicon is 1.5×10^{10} cm^{-3} at 300K.

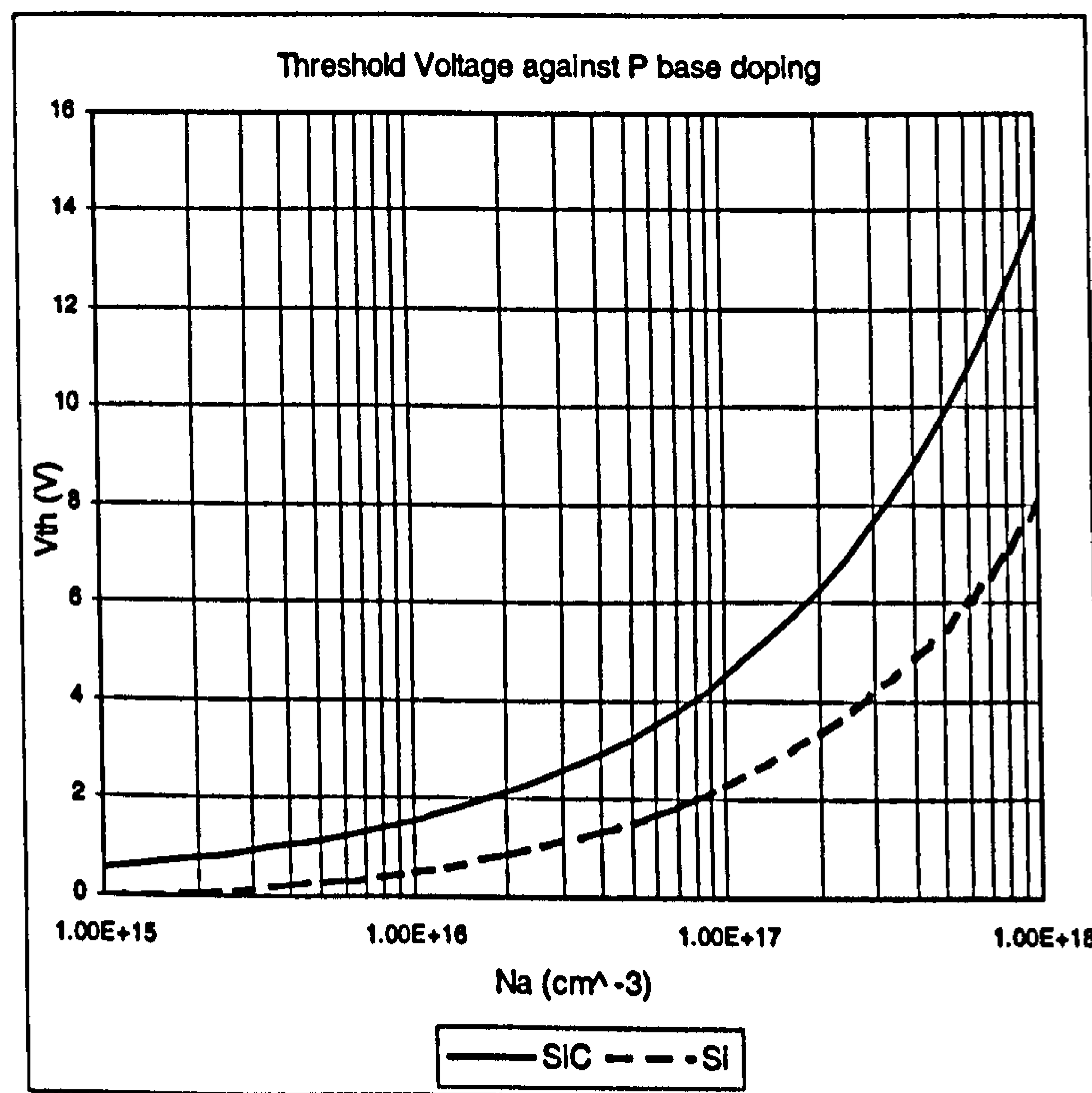


Figure 6.2 SiC IGBTs threshold voltage versus P base doping at 300K

The P base doping level is a critical design parameter affecting V_{th}. For SiC devices, the N drift region doping level chosen to support the desired blocking voltage is about 100 times higher than that for the corresponding silicon devices, in the order of 1×10^{14} cm^{-3} for 10 kV SiC devices. Hence to avoid punchthrough of the N^+ emitter, the P base doping should be at least 1×10^{16} cm^{-3} for 10 kV SiC devices. Furthermore, the hole current flow must traverse a path beneath the N^+ emitter region to reach the emitter

electrode. The lateral hole current flow produces a forward bias across the N^+-P junction close to the channel [6.3]. If this voltage bias exceeds the built-in voltage, the parasitic thyristor structure in the IGBT will be activated, thereby losing gate voltage control of the collector current. To prevent this latchup, the P base resistance under the N^+ emitter must be low, therefore, low P base doping is not suitable. However, high P base doping will result in a high threshold voltage, inducing a high gate drive voltage requirement to maintain the device in the on-state. To account for the gate-emitter voltage rise due to parasitic capacitance coupling and to provide enough immunity to external disturbance, a threshold voltage of between 4 and 6 V is suitable. This corresponds to a base doping level of 1 to 3×10^{17} cm^{-3}.

Typically, doping of SiC is mostly accomplished in situ during epitaxial growth due to the extremely low diffusion coefficients of dopants in SiC. The lateral inversion layer in SiC is realized using multiple implantation [6.4], [6.5]. Triple implantation provides a doping profile increasing from a low surface concentration in the order of 1×10^{16} cm^{-3} to a concentration in the order of 1×10^{18} cm^{-3} near the P base/N drift junction [6.5]. This solves the contradiction between a low P base doping for achieving a low threshold voltage and a high inversion layer carrier mobility and sufficiently high P base doping for the blocking capability and contact formation. The implantation depth is practically less than 1 μm, therefore this is not suitable for Trench Gate IGBTs and only a uniform P base doping is realizable in SiC TIGBTs.

The transfer characteristics of a 10 kV P-channel Punch-Through Trench Gate IGBT obtained via numerical simulation are plotted in Fig. 6.3. The oxide thickness, the P base doping level and the device area are 500Å, 1×10^{17} cm^{-3} and 1 cm^2, respectively. The collector-emitter voltage bias is 10 V and the temperature is 300K. The transfer characteristic for τ_0=240 ns shows a small transconductance g_m while the applied gate

voltage magnitude is greater than 10 V. This indicates that the channel resistance is negligible compared with the drift region resistance in the high gate voltage range. Increasing the carrier lifetime to 1 μs, the collector current rises rapidly with increased gate bias even after entering the high gate voltage bias region. Elevating carrier lifetime reduces the N base series resistance to a value comparable to the channel resistance.

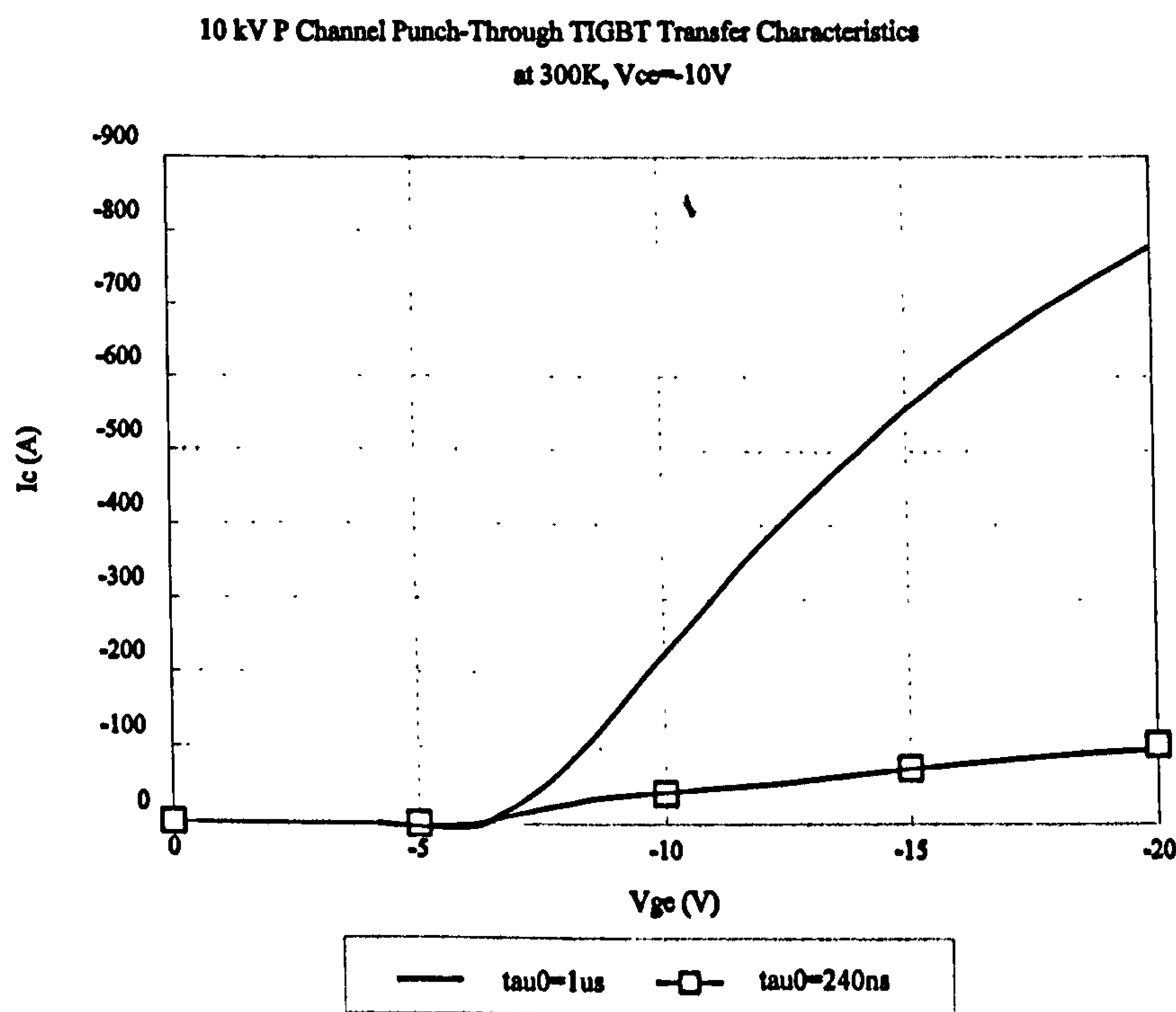


Figure 6.3 10 kV P-channel Punch-Through Trench Gate IGBT Transfer Characteristics at 300K, V_{ce}=-10V

6.1.2 Voltage Blocking Capability

Non Punch-Through (NPT) IGBTs (no N buffer) have both forward and reverse blocking ability and can be used in AC circuits. In DC circuit applications, only forward blocking is usually required. This affords the use of the Punch-Through structure to optimize the forward conduction characteristics for a given forward blocking capability, without considering the reverse blocking capability. The forward blocking capability of IGBTs is determined by the open-base breakdown voltage of the integral P base/N drift/P^+

collector BJT transistor, which is strongly influenced by minority carrier lifetime in the N base. Open-base PNP transistor breakdown occurs when the product of the multiplication factor M and the current gain α equals unity.

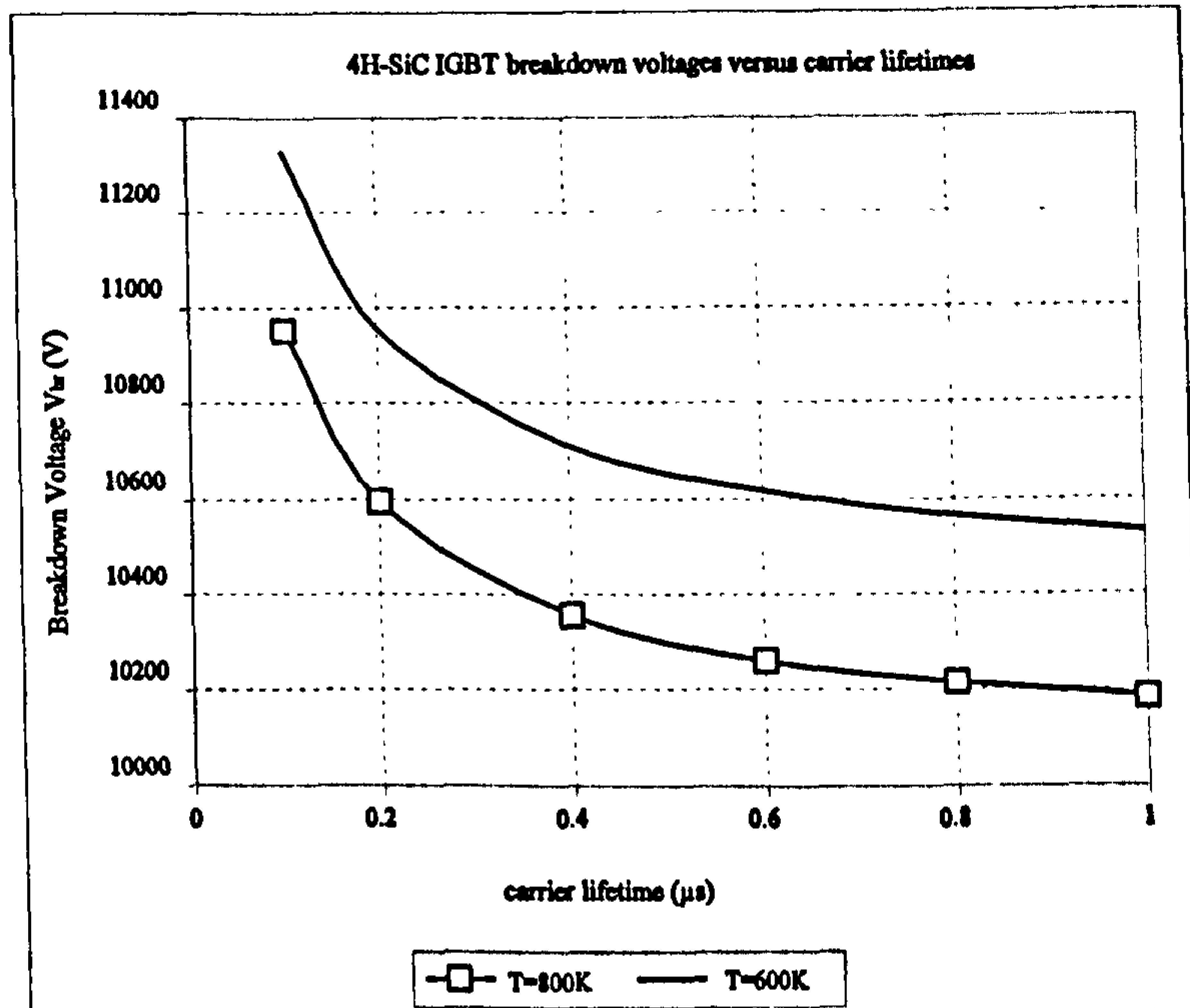


Figure 6.4 4H-SiC IGBT breakdown voltages versus carrier lifetime

Due to its large drift region width which is required for a high blocking voltage, the current gain of the NPN transistor can be approximated by the base transport factor:

$$\alpha_T = \frac{1}{\cosh(W_L/L_e)} \tag{6.3}$$

where W_L is the undepleted drift region width and L_e is the electron diffusion length in the drift region determined by the drift region carrier lifetime τ_0 and electron diffusion coefficient D_e: $L_e=(D_e\tau_0)^{1/2}$.

A device with a longer N base carrier lifetime has a larger L_e, hence a higher current gain. Therefore the forward blocking voltages of IGBTs degrade with increased carrier lifetime. Figure 6.4 shows the reduction of forward blocking capability of SiC IGBTs with increased lifetime. A device with a carrier lifetime of 1 μs has a forward breakdown

voltage 800 V less than a device with a 100 ns carrier lifetime.

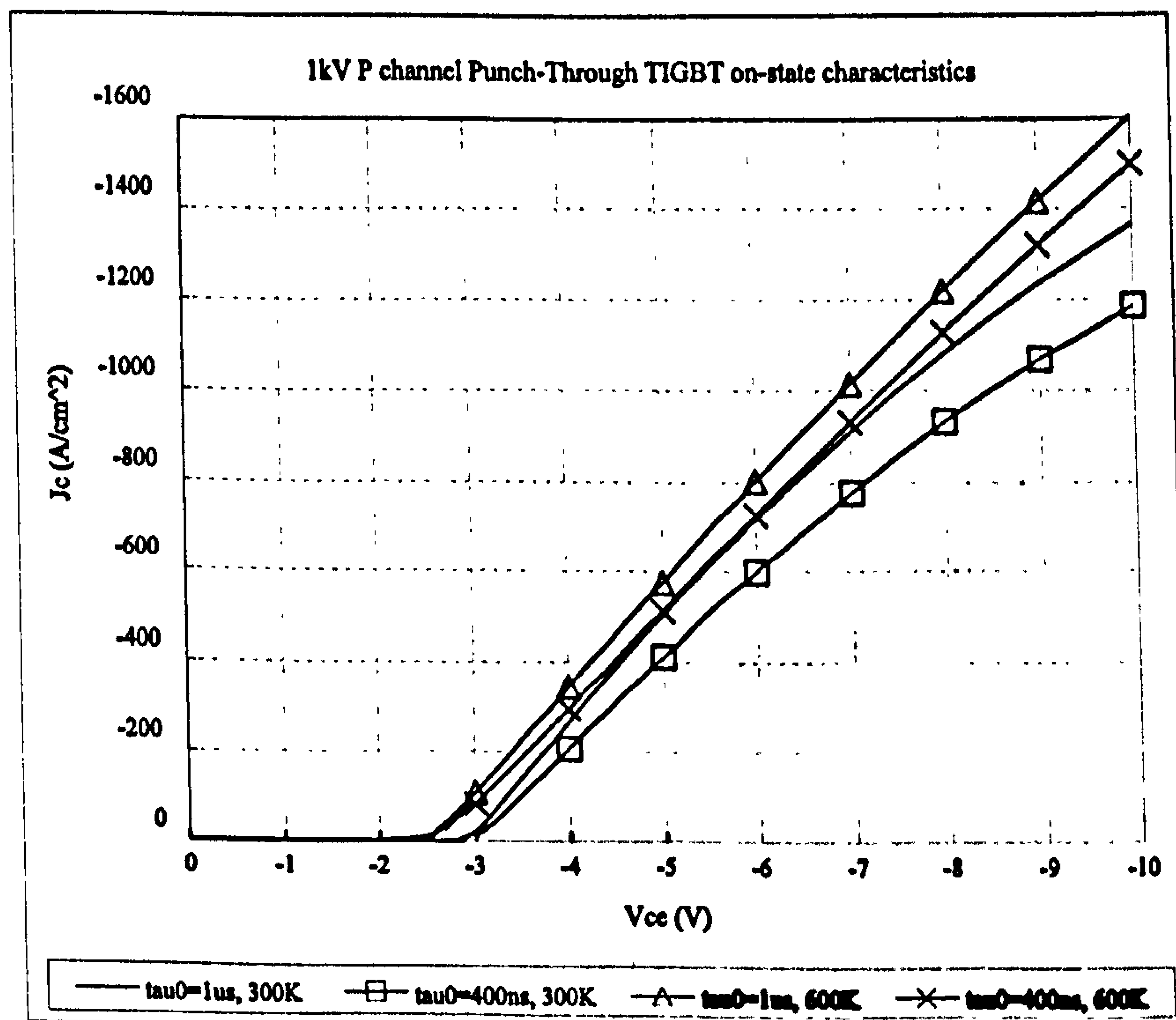
For SiC IGBTs designed for high temperature operation, the impact of temperature on the breakdown voltage must be taken into account for similar reasons as those stated in Chapter 5, Section 5.2.1. Figure 6.4 shows the forward blocking voltages both at 600 K and 800 K. The breakdown voltages at 600 K are about 350 V higher than those at 800 K. When designing the device, the breakdown voltage must be measured at the maximum operating temperature. In this work, SiC lifetime varies with temperature according to $T^{2.3}$ [6.1].

6.1.3 On-State Characteristics

The on-state characteristics of 1 kV, 5 kV and 10 kV P-channel Punch-Through TIGBTs with V_{ge}=-15 V are simulated and shown in Figure 6.5. The cell pitch and channel length are 16 μm and 2 μm respectively. The gate/emitter area ratio is 1:1. At high current densities, the devices show a current saturation trend, which is favourable for practical use. The sensitivity of device current handling ability to carrier lifetime increases with voltage rating. For the 10 kV IGBT, a 400 ns carrier lifetime is not long enough to achieve good device performance. To ensure steady-state current sharing of parallel connected devices at high current levels, it is preferred that the device exhibits a higher on-state voltage at higher temperature. However, as shown in Figure 6.5, in most cases, the on-state voltages are slightly lower at elevated temperature. This is mainly caused by the increased dopant degree of ionization at high temperature, hence, improved injection efficiency.

The on-state characteristics of a 3.3 kV Si IGBT, 6.5 kV GTO and thyristor are compared with 4H-SiC IGBTs in Figure 6.6. The 4 kV 4H-SiC IGBT with a lifetime of 400 ns exhibits much better current handling ability than a 3.3 kV Si IGBT in spite of the fact that the built-in voltage $V_{bi,SiC}$ (2.7 V) for SiC is about 2 V higher than $V_{bi,Si}$ (0.7 V).

The current handling ability of the 6.5 kV Si GTO can not compete with that of SiC IGBTs. Biased at 5 V, the SiC IGBT with gate/emitter area ratio of 1:1 and a lifetime of 5 μs can conduct a current density of 200 and 280 A/cm^2 at 300 K and 600 K respectively whilst the GTO can only conduct 50 A/cm^2 at 390 K. Compared with the Si thyristor, the SiC IGBT on-state characteristics are not comparable at room temperature. However, the Si thyristor on-state characteristics degrade with temperature rapidly whilst the SiC IGBT current handling ability temperature dependence is small. The Si thyristor and 4H-SiC IGBT have on-state voltages of 5.1 V and 4.8 V respectively at 400 K. The typical operating junction temperature is more than 400 K. Because of the thermal limitation and the limit of intrinsic carrier concentration, 600 K is impractical for Si devices. Together with the ease of using the IGBT, fast switching speed and high reliability, the 4H-SiC IGBT is a promising replacement for the Si thyristor.



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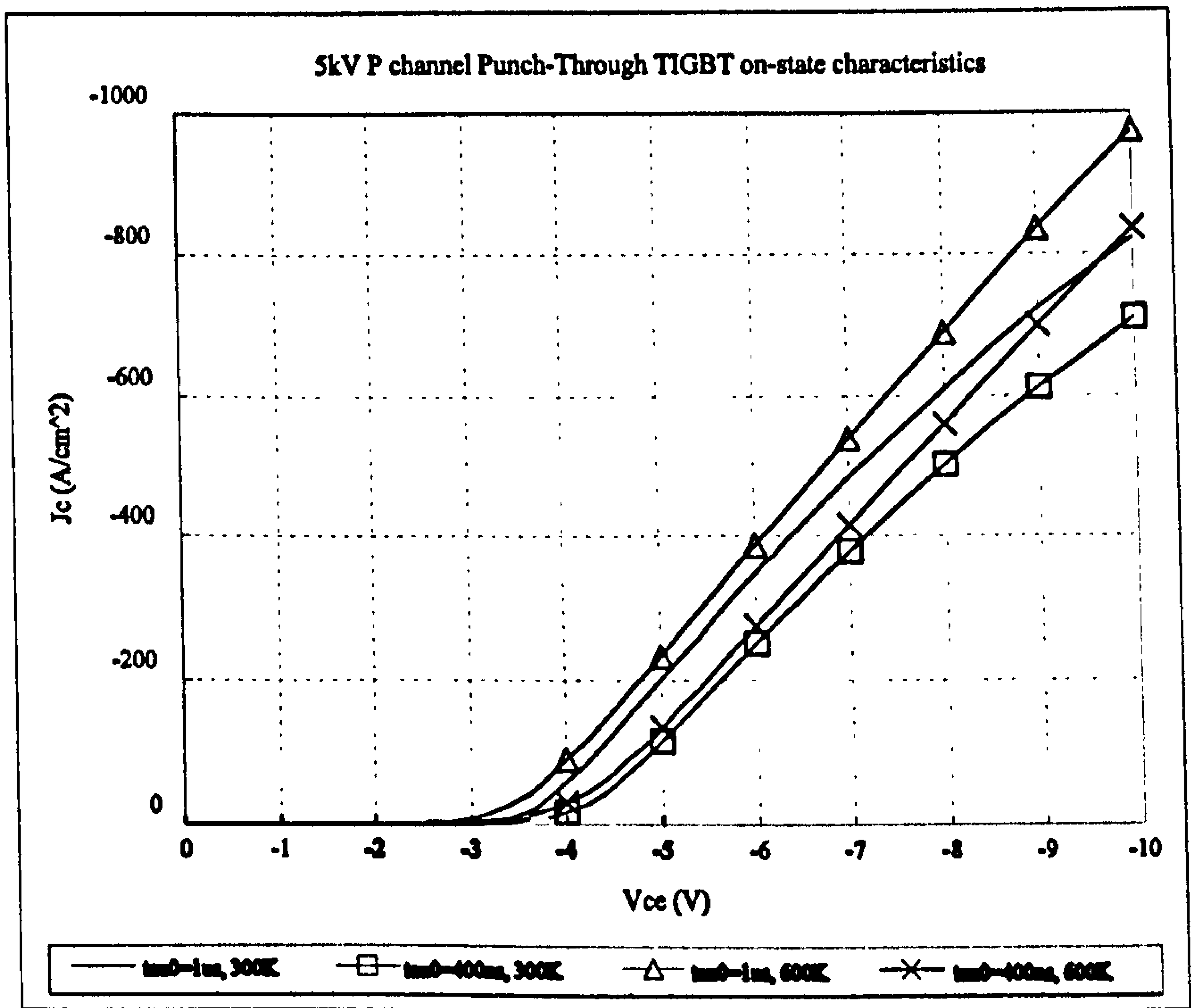

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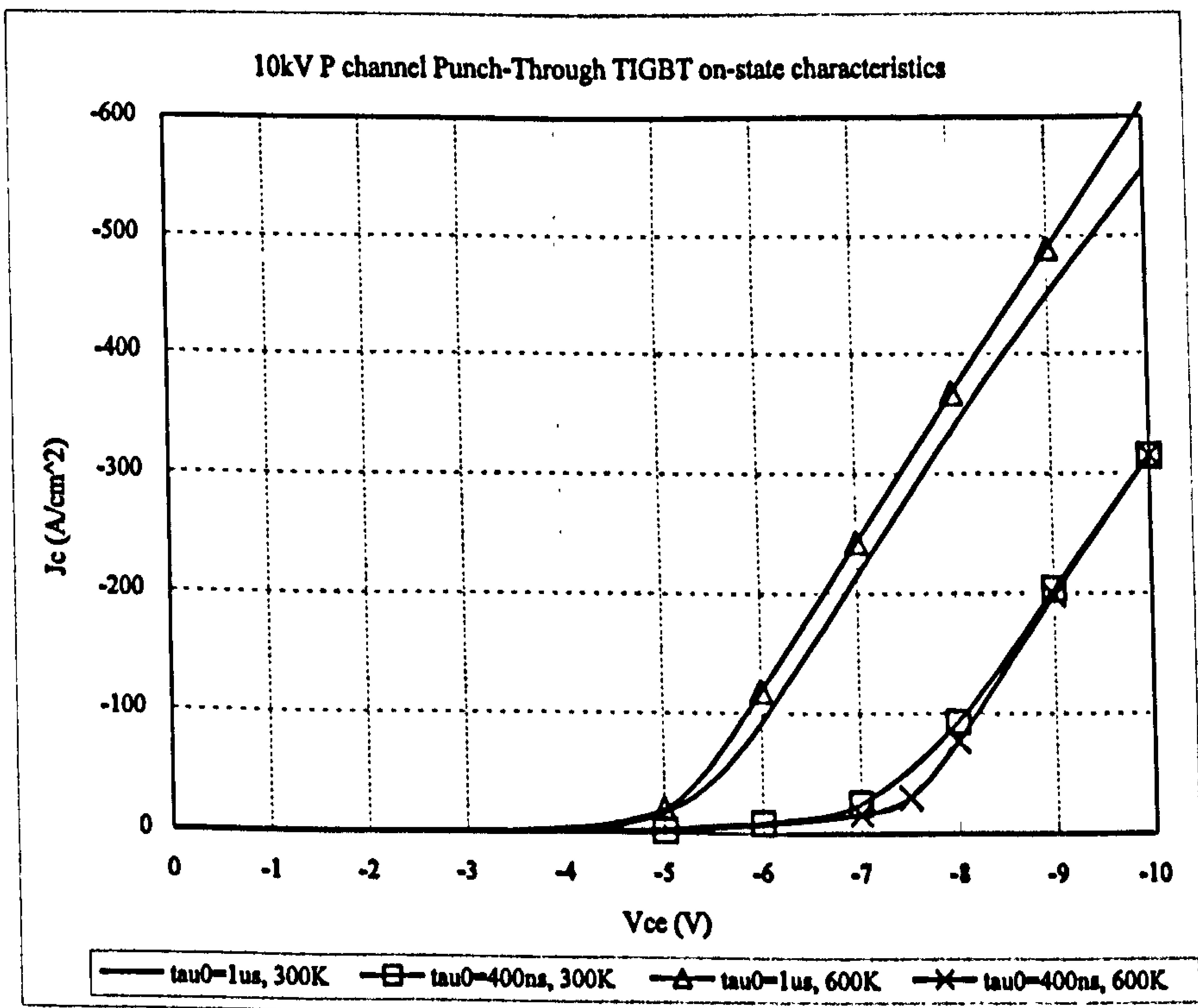
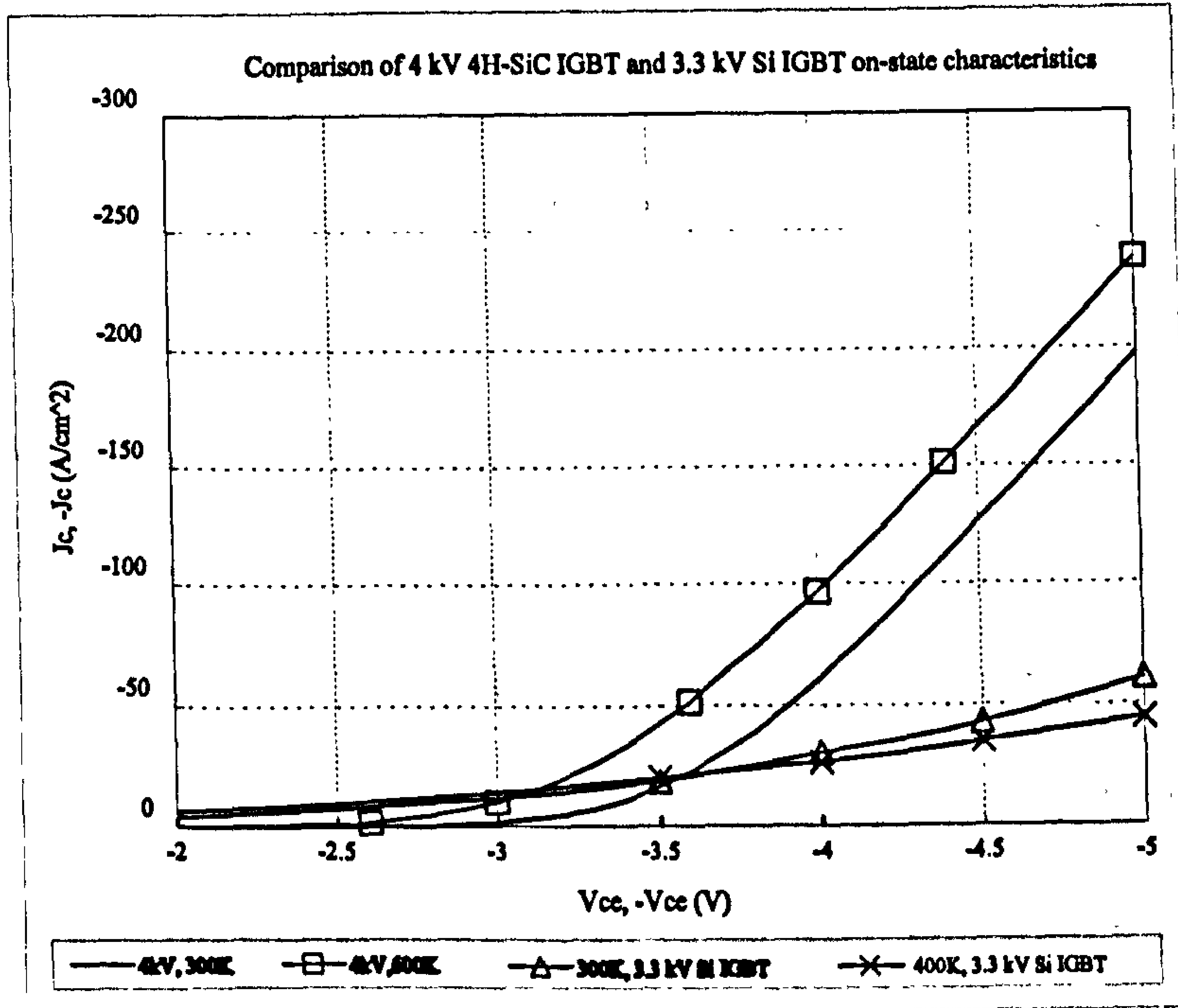


(c)

Figure 6.5 (a) 1 kV, (b) 5 kV and (c) 10 kV P-channel PT TIGBT on-state characteristics



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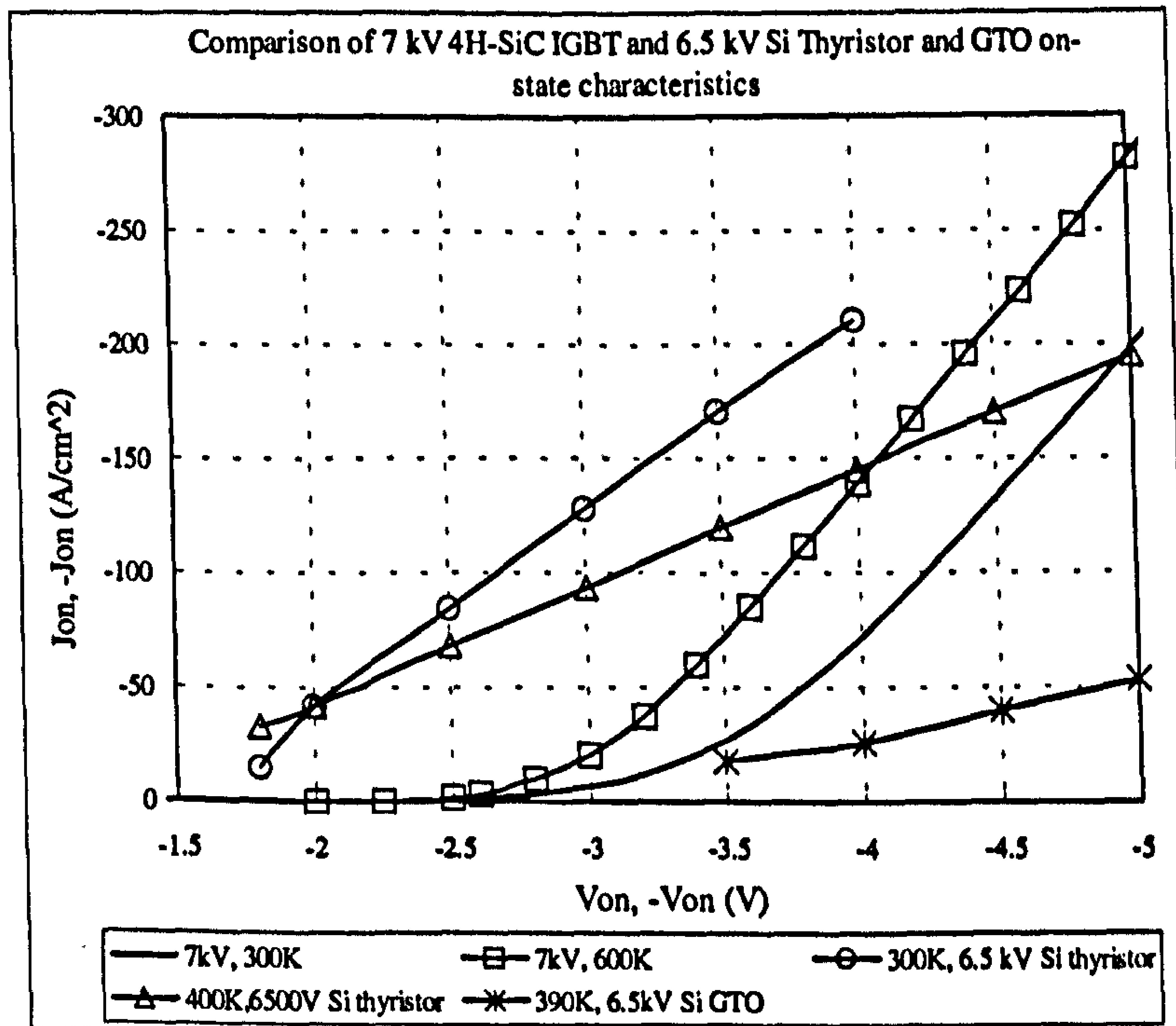


(b)

Figure 6.6 Comparison of 4H-SiC IGBT and Si device on-state characteristics

6.1.4 Switching Characteristics

Table 6.1 shows the simulated switching characteristics for 1 kV, 5 kV and 10 kV P-channel Punch-Through TIGBTs with a resistive load. The on-state current is 1.2 kA and the DC rail voltage is half of the device voltage rating. The devices are turned on and off by increasing the gate drive circuit supply from 0 V to -15 V and vice versa. The device lifetimes and operating current densities are varied to obtain an on-state voltage less than 4 to 6 V. The definition of switching times $t_{d(on)}$, $t_{d(off)}$, t_r and t_f can be extracted from Fig. 6.7. The devices switch on slightly faster, but switch off significantly slower, at 600 K than at 300 K. No substantial change in the delay times with temperature is observed. The device switching losses increase rapidly with voltage rating, from 75.6 mJ for the 1 kV IGBT to 1.86 J for the 10 kV IGBT. However, 1.2 kA on-state current can still be turned off in 6 μs for the 10 kV IGBT at 600 K, indicating high voltage, high current, high temperature and high frequency snubberless operation is realizable using SiC technologies.

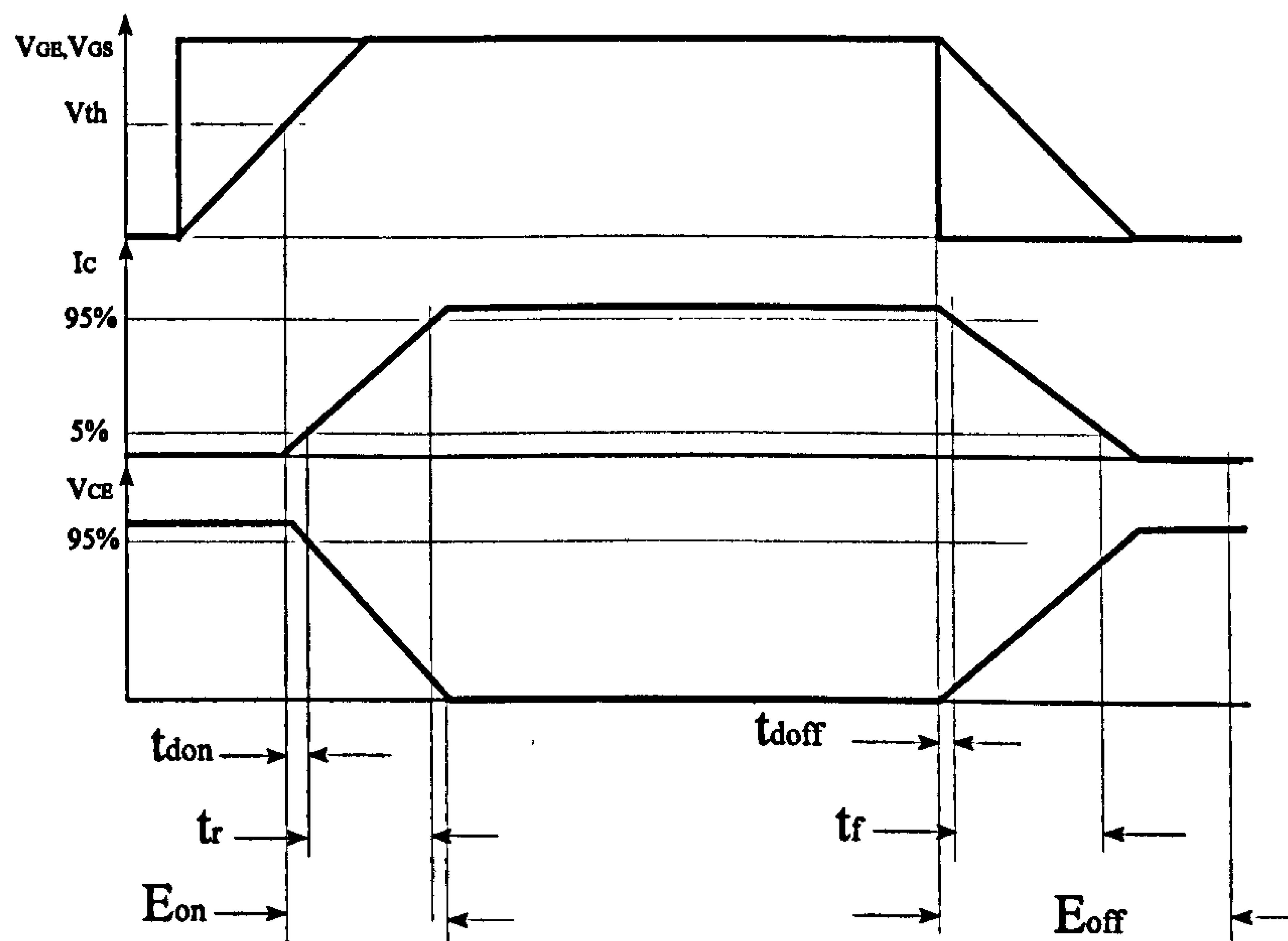


Figure 6.7 Definition of the switching time

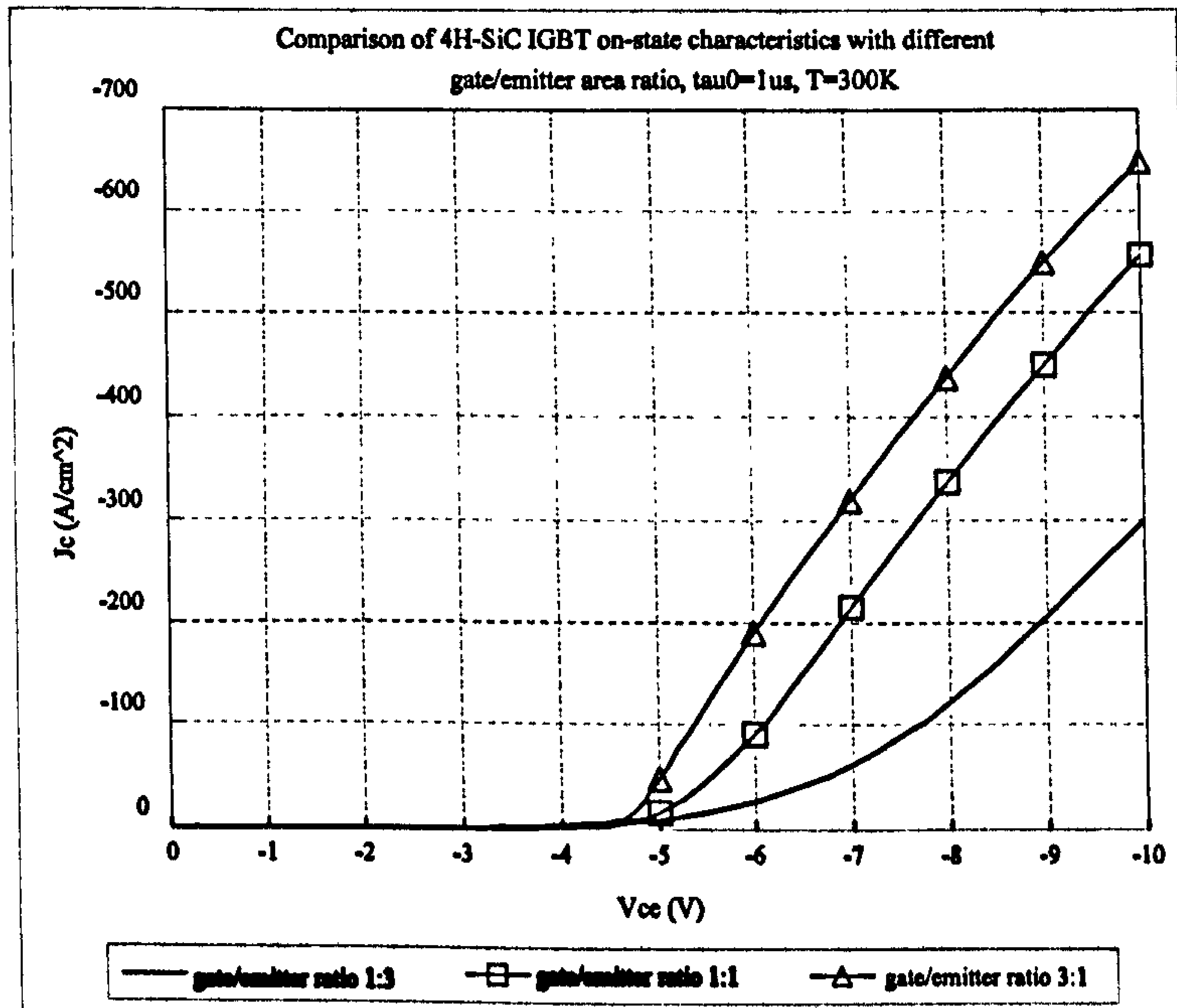
Table 6.1 High Voltage 4H-SiC P-channel PT TIGBT Switching characteristics

Voltage Rating	Conditions	τ_0 (ns)	T (K)	$t_{d(on)}$ (ns)	t_r (μs)	$t_{d(off)}$ (μs)	t_f (μs)	E_{on} (mJ)	E_{off} (mJ)
1 kV	J_{on}=300 A/cm^2, V_s=500 V	400	300	47	0.46	0.28	0.7	52.3	75.6
			600	37	0.45	0.44	2.57	50.8	272
5 kV	J_{on}=180 A/cm^2, V_s=2.5 kV	600	300	100	0.64	0.47	0.86	346	500
			600	95	0.6	0.68	3.58	322	2173
10 kV	J_{on}=50 A/cm^2, V_s=5kV	1000	300	170	1.37	1.1	1.77	1501	1864
			600	200	1.26	1.4	4.58	1410	4640

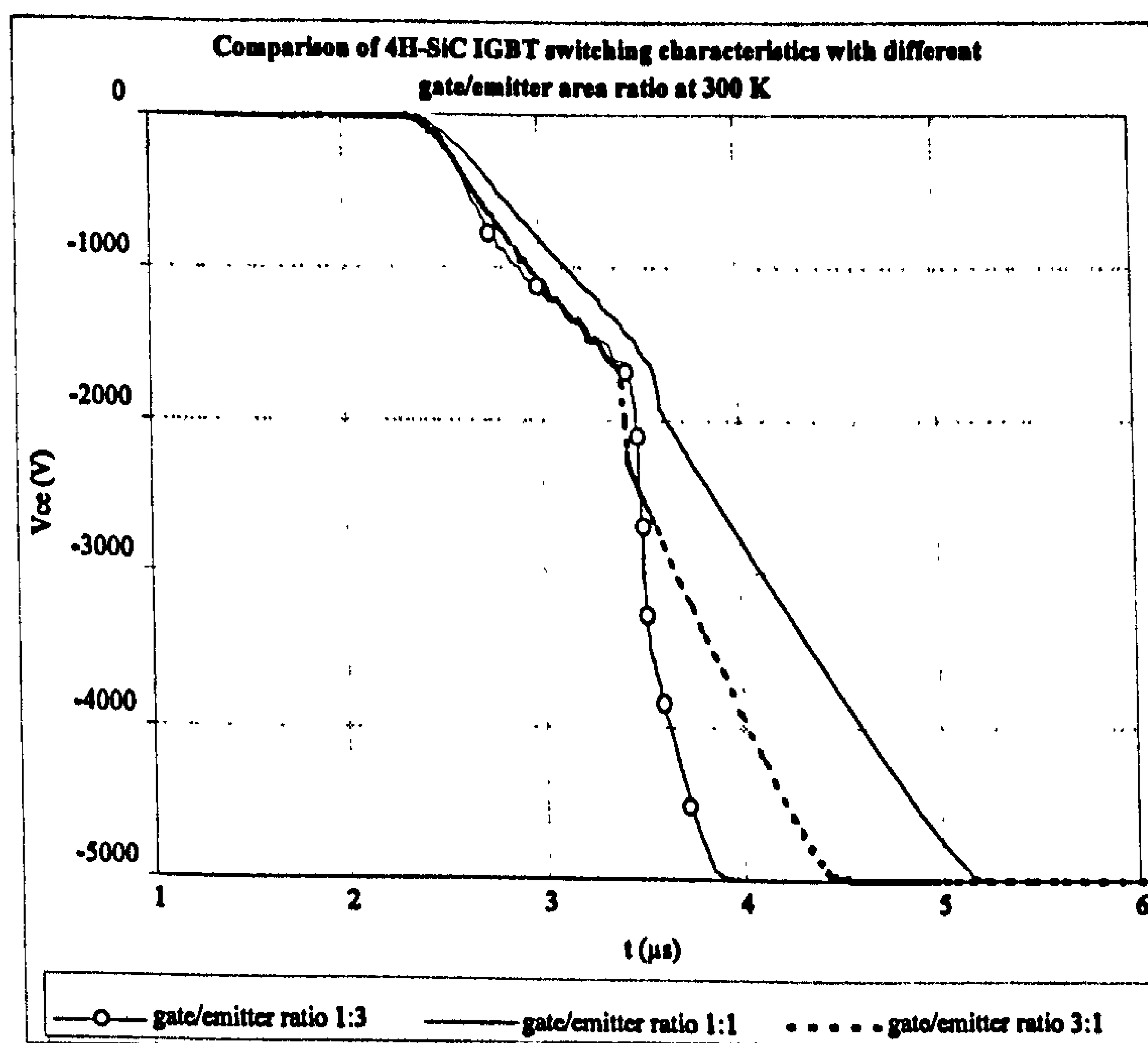
6.1.5 Effect of Gate/Emitter Area Ratio

Because of the voltage drop in the channel, the base/drift junction in IGBTs is reverse biased and the excess carrier concentration in the drift region at the base/drift junction is near zero in the on-state. Hence, the main voltage drop in the drift region is near the base/drift junction. This applies to both the Trench Gate and DMOS gate structures. An increase in the carrier concentration near the base/drift junction will improve the device on-state characteristics greatly without necessarily any substantial increase in the amount of stored excess carriers, that is, no degradation of switching performance. The gate/emitter area ratio has a significant impact on the carrier distribution near the gate area. In Figure 6.8, the on-state and switching characteristics of SiC TIGBTs with different gate/emitter area ratios at 300 K are shown. The cell pitch is 16 μm and the device area is 24 cm^2 while simulating the switching characteristics. Increasing the gate/emitter area ratios from 1:3

to 3:1 reduces the on-state voltage by 2.5 V at 100 A/cm². But the enhanced excess carriers in the drift region slows down the switching speed. The IGBT with a gate/emitter area ratio of 1:3 turns off 1.5 μs faster than the one with a gate/emitter area ratio of 3:1. Hence a trade-off between current handling ability and switching speed is needed.



(a)



(b)

Figure 6.8 Comparison of 10 kV 4H-SiC IGBT (a) on-state and (b) switching characteristics with different gate/emitter area ratios at 300K, τ_0=1 μs

6.2 P-Channel 4H-SiC IGBTs versus N-Channel 4H-SiC IGBTs

The vast majority of Si IGBTs have an N-channel because electron mobility is higher than that of holes for silicon. However, it will be shown that some unique characteristics of SiC will make P-channel IGBTs comparable to their N-channel counterparts.

Performance investigation of SiC IGBTs has been carried out by numerical simulations [6.6-6.8]. A 200V fully planar, 6H-SiC TIGBT has also been demonstrated [6.9]. All the devices have an N-channel structure. Because of the relatively high ionization energy of dopants required in SiC and degree of ionization decreases with doping level, most impurity atoms are not ionized in highly doped regions. The degree of ionization of dopants in a P type SiC region is much lower than that in an N type SiC region since the ionization energy of acceptors is larger than donors. Hence, devices with a P^+ substrate exhibit larger specific on-state resistance than those with an N^+ substrate. For bipolar devices, incomplete ionization also induces lower injection efficiency, hence poorer on-state characteristics. As shown in Figure 2 of [6.9], the current handling ability of the TIGBT at 250°C is 10 times better than at 25°C because the degree of ionization of dopants increases with temperature. Therefore, the incomplete ionization effect has a more severe impact on the performance of N-channel IGBTs than P-channel IGBTs. Meanwhile, the channel carrier mobility and the drift region carrier mobility in N-channel IGBTs are higher than in P-channel IGBTs, indicating smaller channel and drift region specific on-state resistances. Therefore, it is worthwhile investigating the feasibility of a P-channel IGBT in SiC.

For the same carrier lifetime and forward blocking voltage, the P-channel IGBT drift region width is larger and doping is lower than in N-channel IGBTs. The IGBT

forward blocking voltage is determined by the open-base breakdown voltage of the integrated transistor, which is pertinent to the gain of the parasitic base/drift/substrate transistor. The current gain of the P-channel IGBT parasitic transistor is intrinsically higher than the N-channel IGBT parasitic transistor because the former is an NPN transistor whilst the latter is a PNP transistor. So the P-channel IGBT is prone to breakdown at a lower forward voltage than the N-channel IGBT for the same structure. To achieve the same blocking voltage capability, a longer drift region and a lower doping level is required for the P-channel IGBT. Along with the lower mobility of majority carriers (holes) in the P-channel IGBT, the performance of the P-channel IGBT is projected to be poorer than N-channel counterparts. However, as will now be shown, when considering incomplete ionization of dopants in SiC, P-channel IGBTs offer better current handling ability at room temperature.

Figure 6.9 shows the temperature dependence of on-state voltage $|V_{on}|$ at 100 A/cm^2 of 5 kV SiC P-channel IGBTs and N-channel IGBTs with different lifetimes. The gate/emitter area ratio is 1:1 and the gate voltage amplitude is 15 V. The on-state voltages of the SiC N-channel IGBTs at 300K are more than 9 V, even with a 1 μs lifetime. By investigating the carrier distribution inside the device, it is found that at room temperature only a small quantity of minority carriers are injected into the drift region. Elevating the lifetime to 10 μs, the on-state voltage is decreased to 5.8 V. The on-state voltages are in the range of 4 to 5 V at 600 K because of the increased degree of ionization, hence improved injection efficiency at high temperature. Generally, the current handling ability of a SiC N-channel IGBT is improved with increased temperature and carrier lifetime. Its drift region modulated resistance depends largely on the injection efficiency, i.e., N^+ substrate doping and P buffer doping. Its sensitivity to the carrier lifetime is less. However, this sensitivity will increase with voltage rating.

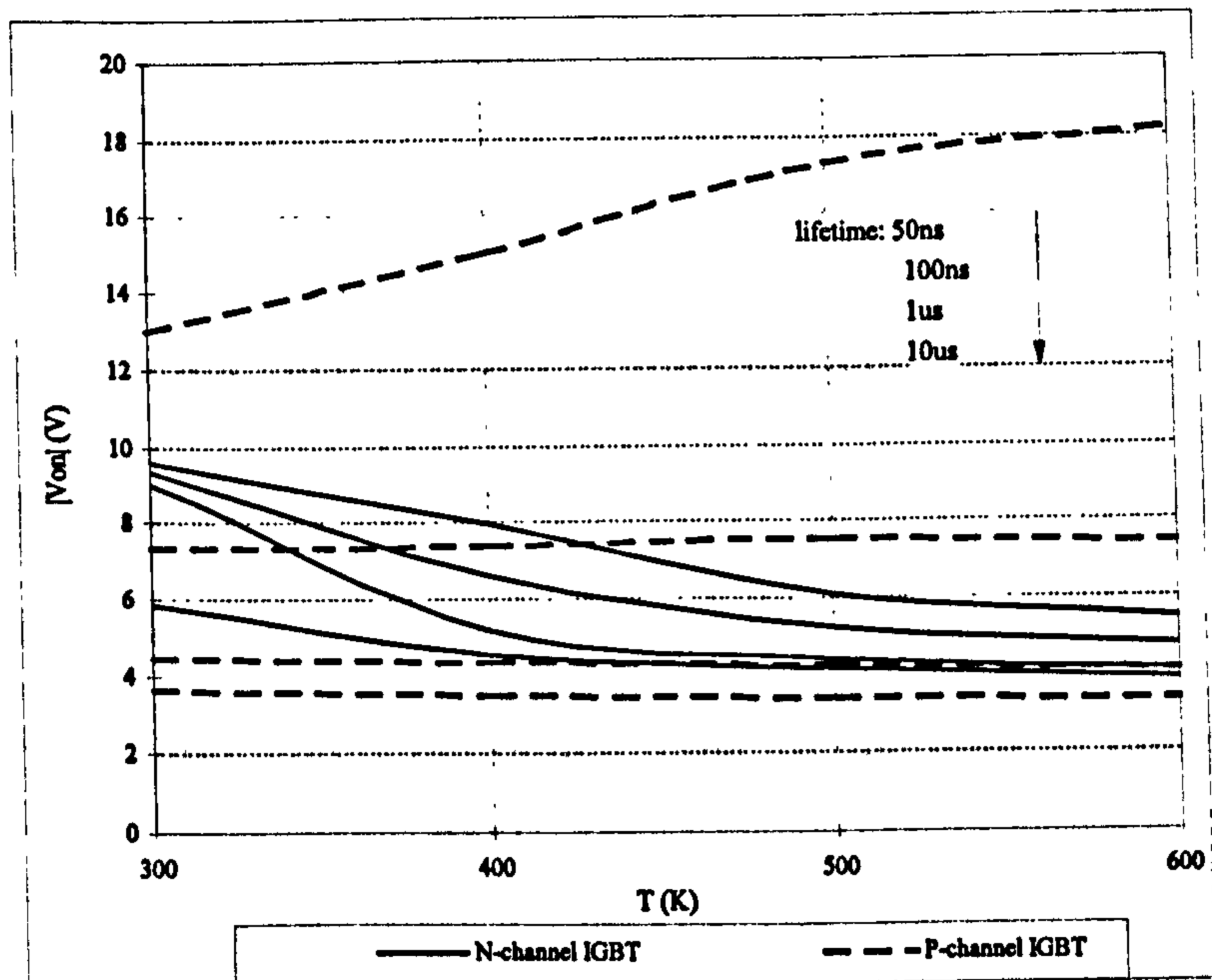


Figure 6.9 On-state voltages at 100A/cm² versus temperature

In contrast, it is more complicated for the P-channel IGBT. The degree of ionization of dopants in the P-channel IGBT substrate is larger than that in the N-channel IGBT substrate, thus, even at room temperature, a reasonable on-state voltage is observed. Increasing the lifetime to 10 μs does not substantially improve the device on-state performance. The on-state voltage of the P-channel IGBT changes rapidly with carrier lifetime, but only slightly with temperature, except with a 50 ns lifetime. The majority carriers of the P-channel IGBT drift region are holes, which exhibit lower mobility than electrons, resulting in larger intrinsic drift region resistance than for the N-channel IGBT. Thus, the carrier lifetime has a more significant impact on the performance of the P-channel IGBT than on the N-channel IGBT for the same voltage rating. With a lifetime of 50ns, few minority carriers are injected into the drift region at all temperatures, resulting in a relatively high on-state voltage. Several factors influencing device performance change with temperature:

(1) The degree of ionization of dopants in the substrate - the higher the ratio of the activated dopants, the higher the injection efficiency;

(2) The degree of ionization of dopants in the buffer - the higher the ratio of the activated dopants, the lower the injection efficiency;

(3) The mobilities of carriers - which degrade with temperature and

(4) The carrier lifetime - which increases with temperature.

With lifetimes from 10 μs to 100 ns, these effects counteract each other, hence the on-state voltages are steady. With a lifetime of 50 ns, the effects of the buffer and drift region mobilities are more significant than others, thus an increase in on-state voltage with temperature is observed.

The IGBT collector temperature dependence of collector current fall time at switch-off with a resistivity load is plotted in Figure 6.10. The on-state current is 1.2 kA and the DC link voltage is 2.5 kV. The switching speed of N-channel IGBTs only changes slightly with temperature and carrier lifetime. The switching speed of the P-channel IGBT with a lifetime of 1 μs or 500 ns decreases quickly with temperature. With a lifetime of 50 ns, there are few excess carriers stored in the drift region at all temperatures, hence device switch-off speed is constant.

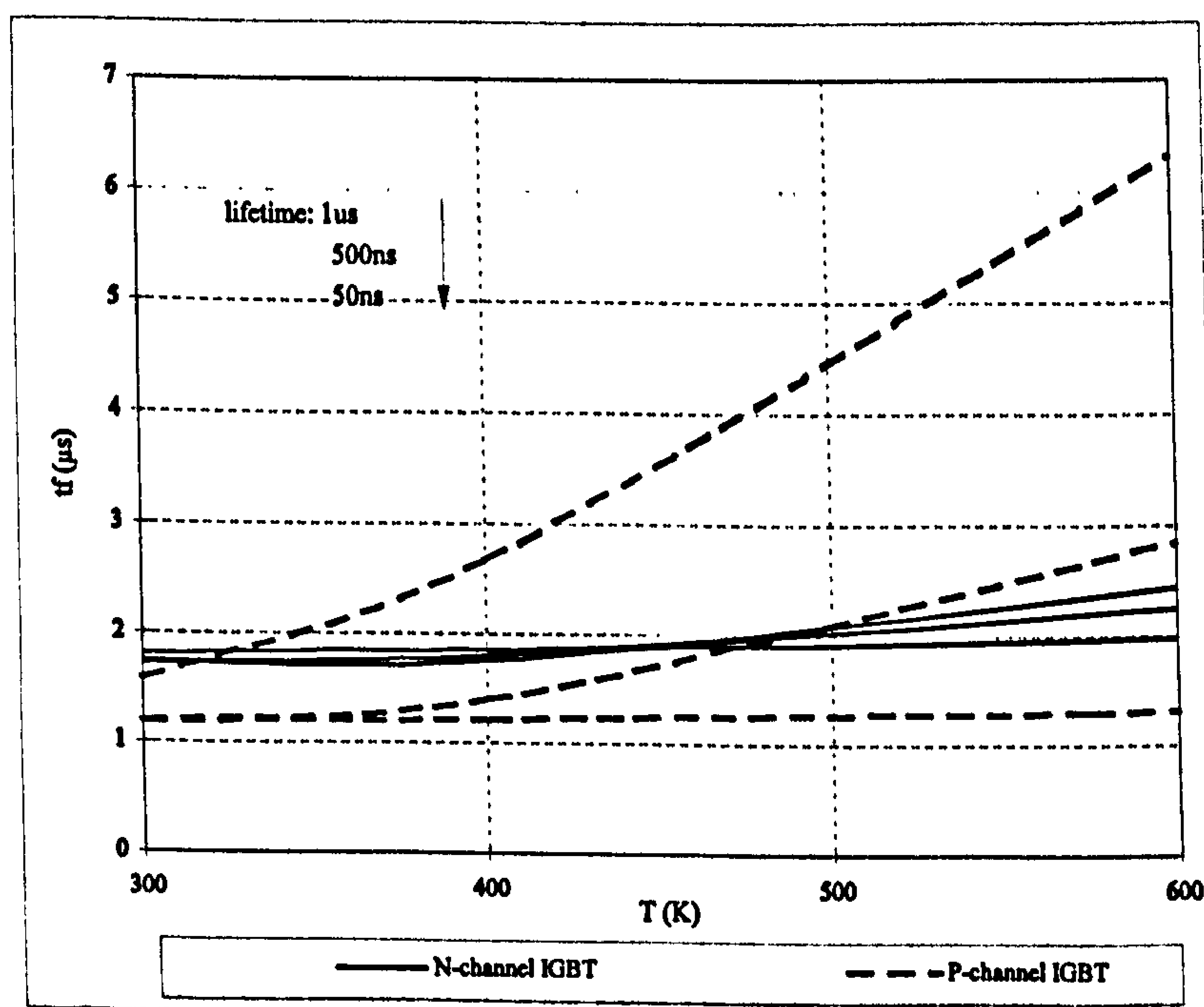


Figure 6.10 1.2 kA 4H-SiC IGBT collector current fall time at switch-off versus temperature

When switching off the devices, after the gate voltage drops below the threshold voltage, the channel current is cut off. The channel current is a significant part of the on-state current in the N-channel IGBT. In contrast, the channel current, comprising holes in P-channel IGBTs, is much less than the electron current at the N base/P^- drift region junction. In addition, for the same breakdown capability, the P-channel IGBT drift region width is larger than in the N-channel IGBT. Thus, generally N-channel IGBTs are faster than P-channel IGBTs.

A device with a higher carrier lifetime has better current handling ability, but slower switching speed. It is useful to plot trade-off curves between on-state voltage and switching speed in order to observe device structure requirements. The device trade-off curves between t_f and $|V_{on}|$ are shown in Figure 6.11.

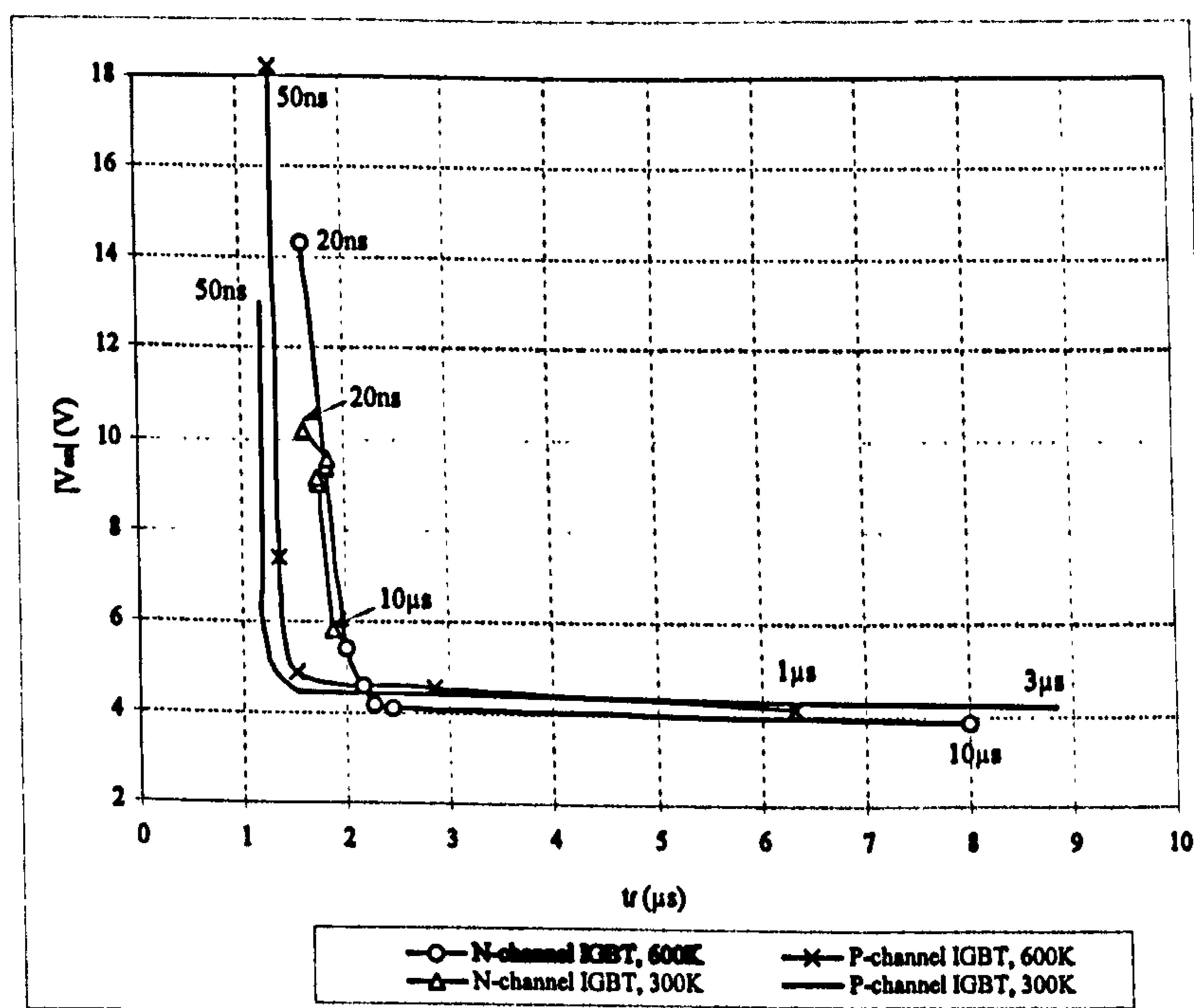


Figure 6.11 4H-SiC IGBT trade-off curves

The trade-off curve for N-channel IGBTs at 300 K is not smooth because a higher lifetime produces a lower blocking voltage and thicker drift region width, together with a lower injection efficiency. Therefore, an N-channel IGBT with a higher lifetime does not

necessarily exhibit a lower on-state voltage. Even increasing the lifetime to 10 μs, N-channel IGBTs still have a steady switching speed. Obviously, P-channel IGBTs are a better choice at room temperature because they exhibit lower on-state voltages and a faster switching speed. At 600K, at the best trade-off point, P-channel IGBTs have a faster switching speed while N-channel IGBTs have a lower on-state voltage. Hence, generally, the P-channel IGBT is suitable for fast-switching devices and the N-channel IGBT is suitable for devices with low on-state voltages at elevated temperature. The specific application will determine the device type preference.

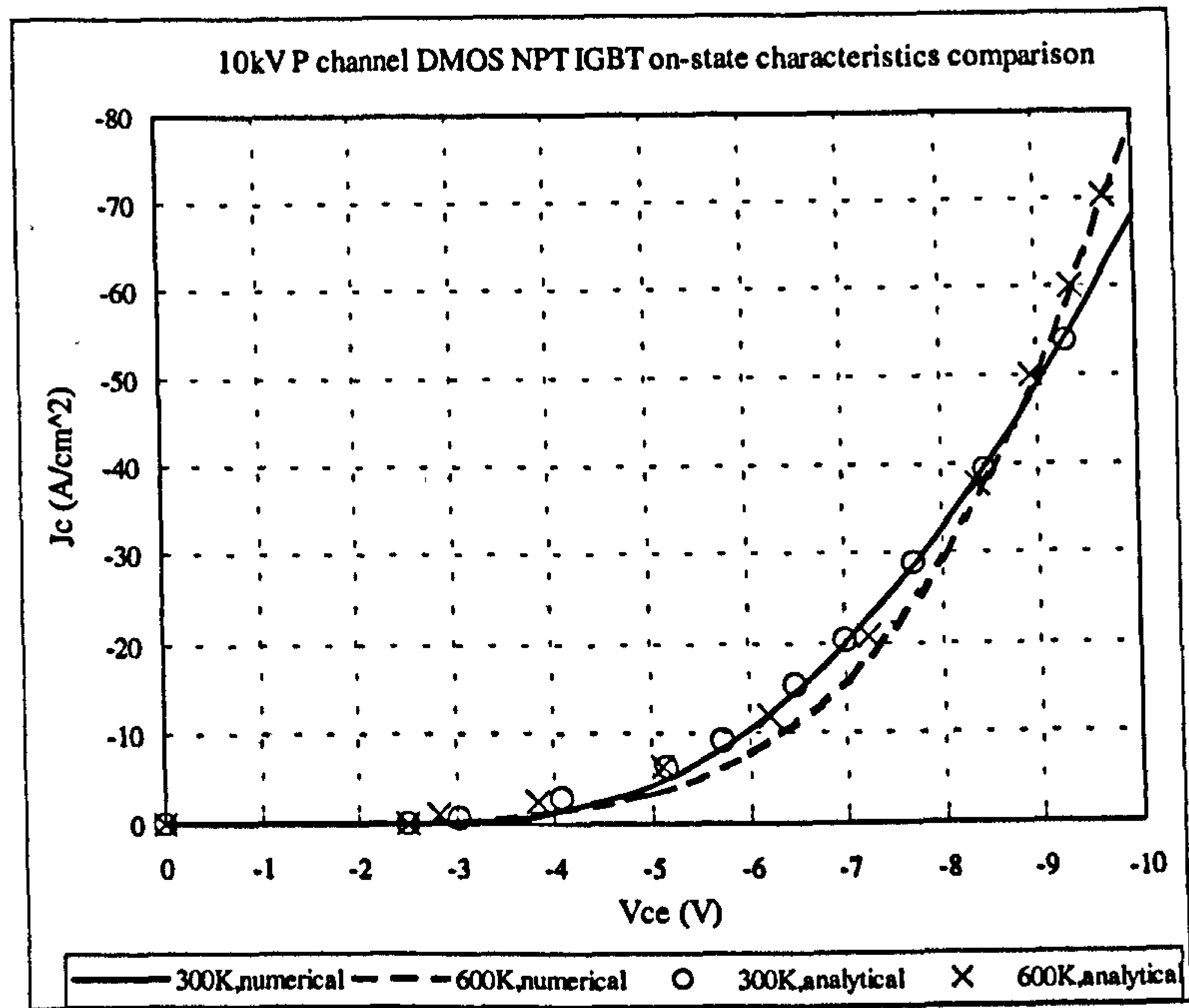
6.3 Various Structures

Vertical SiC IGBTs are classified as multiple implanted, lateral inversion layer IGBTs (MI IGBTs) and vertical inversion layer Trench Gate IGBTs (TIGBTs), according to their gate structures. They can also be classified as Punch-Through IGBTs and Non Punch-Through IGBTs depending on the existence of an N type buffer layer. Hence there are four different IGBT structures: NPT MI, PT MI, NPT and PT TIGBTs.

Currently all commercially available high voltage silicon IGBTs are double-diffused DMOS IGBTs. TIGBTs are available at 1200 V and under development for several thousands of voltages. Plotted in the parts of Fig. 6.12 are the forward conduction characteristics of 10 kV SiC MI IGBTs obtained using a two-dimensional on-state IGBT model [6.2] and the 2-D numerical simulator. The results fit well with each other.

To compare the current handling capability of different IGBT structures, the on-state characteristics of 10 kV P-channel IGBTs are simulated employing the numerical simulator and results are shown in Fig. 6.14. The cell pitch is 30 μm for MI IGBTs and 16 μm for TIGBTs. Two values of carrier lifetime: 500 ns and 1 μs are chosen to study lifetime impact on device performance. The drift region width and doping for the different devices

are adjusted to block 10 kV at 800 K.



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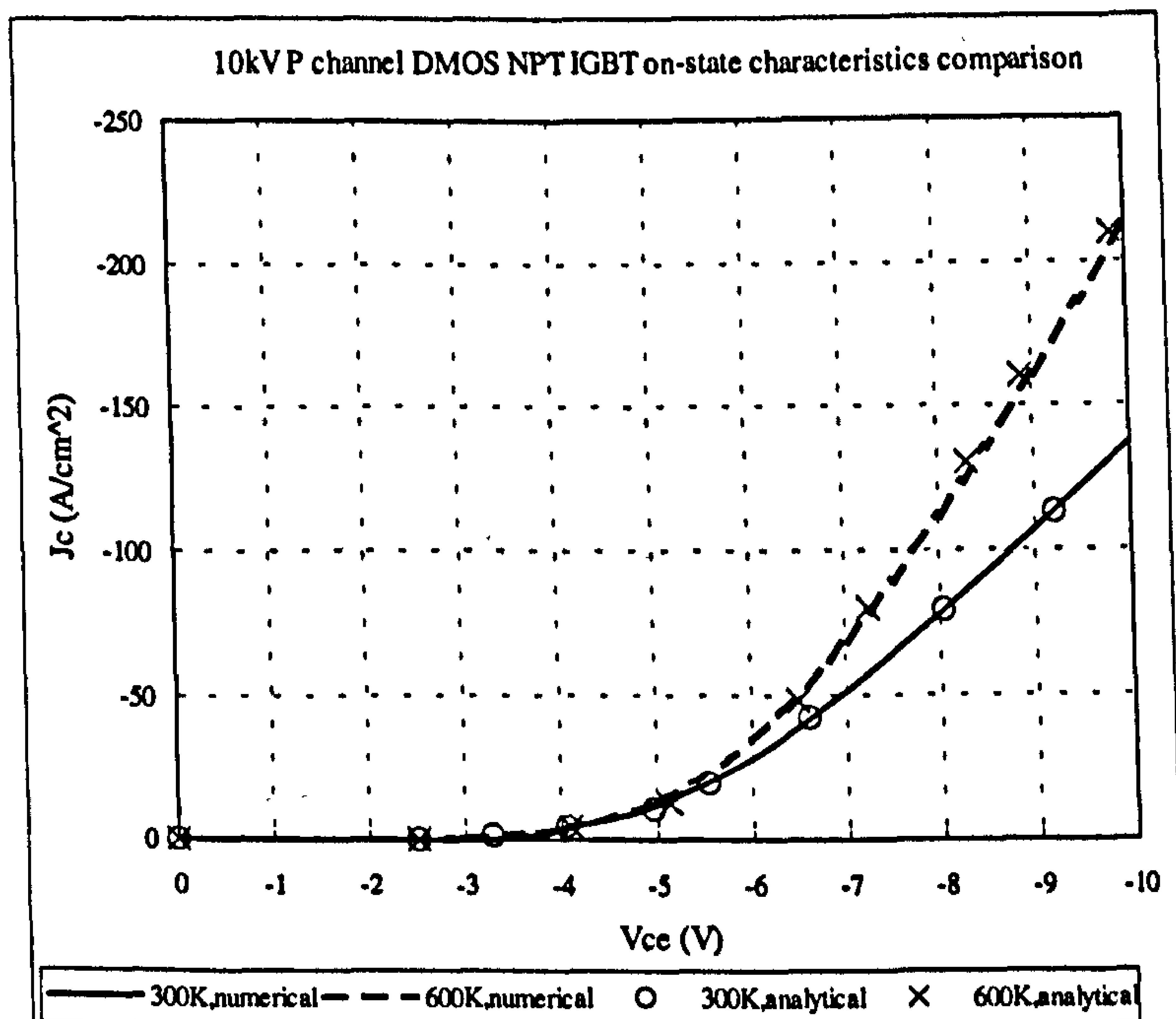


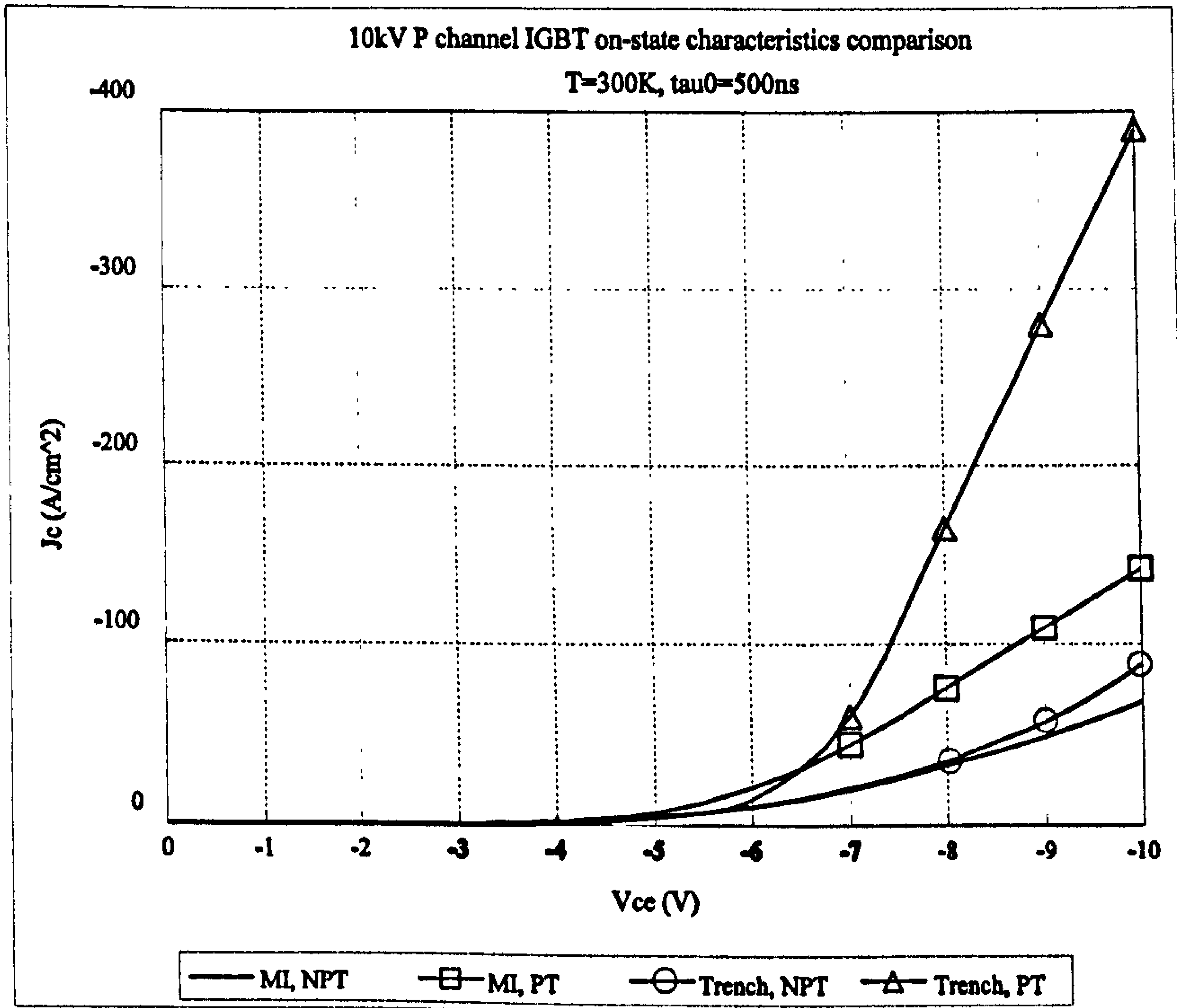
(b)

Figure 6.12 10 kV P-Channel DMOS NPT IGBT on-state characteristics obtained using a 2-D analytical model (a) τ_0=500 ns and (b)τ_0=1 μs

Si TIGBTs exhibit much better current handling ability than Si DMOS IGBTs. The main factor responsible for this is the JFET component between the base diffusions in DMOS IGBTs and the higher cell density. In addition, the accumulation layer formed

under the trench bottom in Trench Gate IGBTs also improves their on-state characteristics. In SiC technology, multiple implatation is employed to fabricate lateral inversion layer MOSFETs (Section 6.1.1), providing a higher inversion layer mobility, lower threshold voltage and preventing the space charge layer from reaching the emitter/base junction. As shown in Figure 6.13, generally 4H-SiC MI IGBTs exhibit higher on-state voltages than the corresponding Trench IGBTs. However, at 600 K, with a lifetime of 500 ns, the Non Punch-Through MI IGBT has better current handling ability than the TIGBT. In the case of devices with a Punch-Through structure, the Trench Gate IGBT has higher on-state voltages than the corresponding MI IGBT at low on-state current densities. Although biased at 10 V, it can conduct 0.4 to 2.5 times higher on-state currents. Another reason accounting for this is that in TIGBTs, the gate length is 8 μm, corresponding to a gate/emitter area ratio of 1:1, whilst in MI IGBTs, the gate length is 20 μm, hence the gate/emitter area ratio is 3:1. As discussed in Section 6.1.5, the on-state characteristics can be improved by changing the gate/emitter area ratio. For 10 kV 4H-SiC TIGBTs, increasing the gate/emitter area ratio enhances device on-state performance. For MI IGBTs, the lateral channel occupies a part of the surface area, hence spacing between two base regions is limited.

Compared with the NPT IGBT, the PT IGBT has an additional buffer layer to reduce the drift region width. In order to support the same breakdown voltages, 50%-75% lower drift region doping is required for the PT IGBT than for the NPT IGBT. This difference in drift region doping results in only a slight difference in carrier mobilities. The carrier diffusion lengths are nearly the same if the carrier lifetimes are the same in both structures. Therefore, the modulated drift region resistivity of the PT IGBT is smaller than that of the NPT IGBT for the former has a thinner drift region width. In Figure 6.13, the performance of PT IGBTs is better than that of the corresponding NPT IGBTs for all cases.



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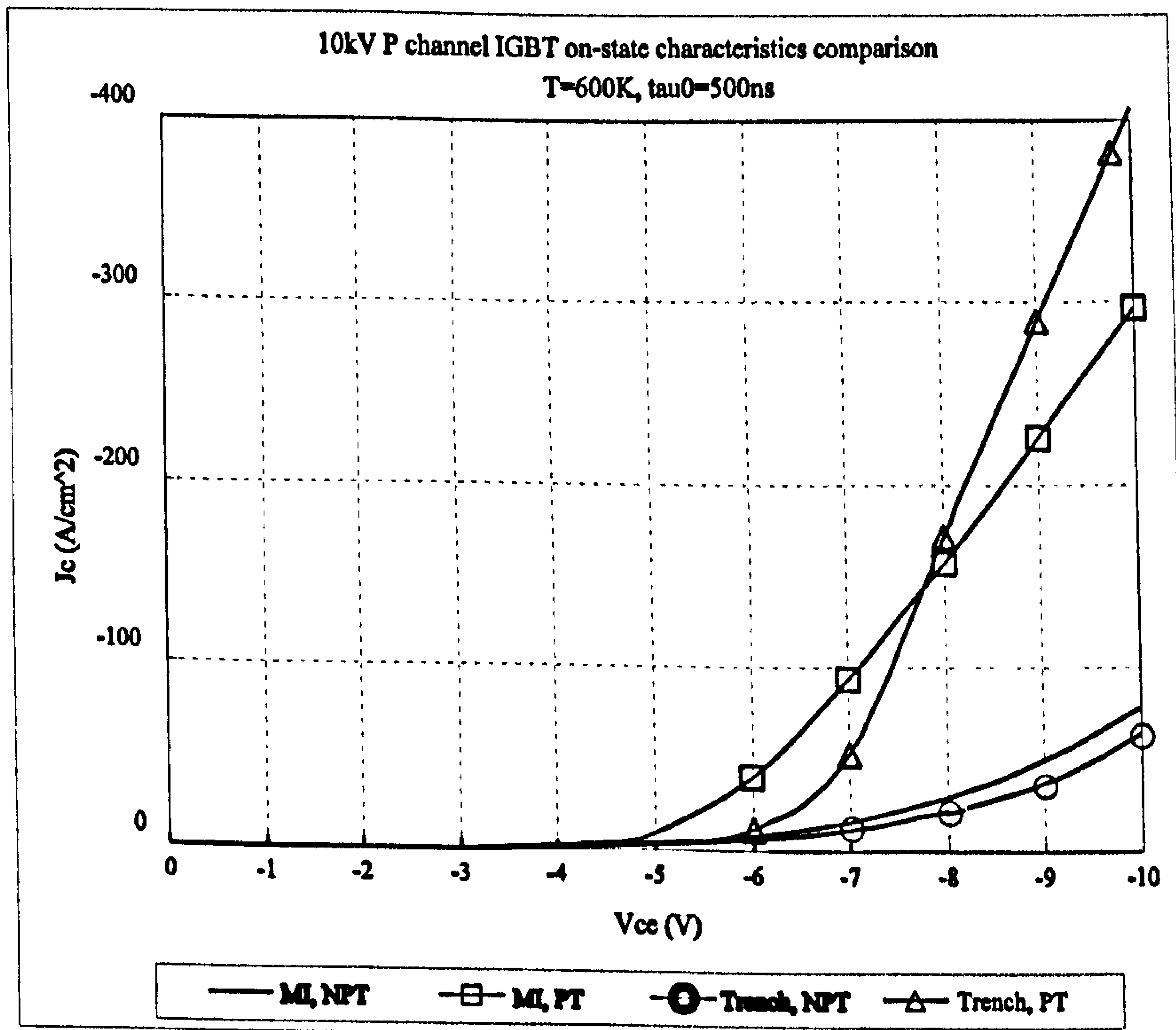

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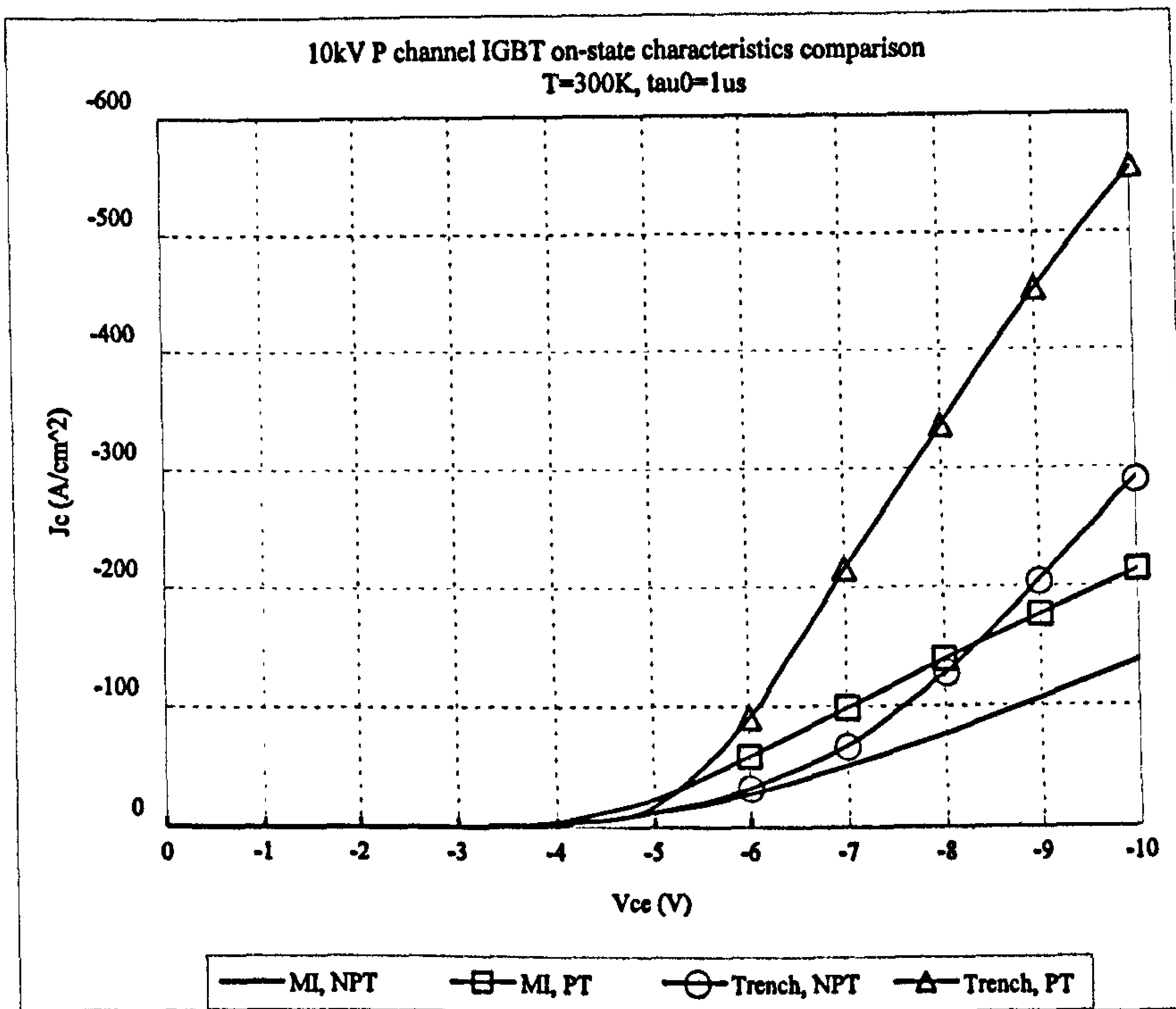

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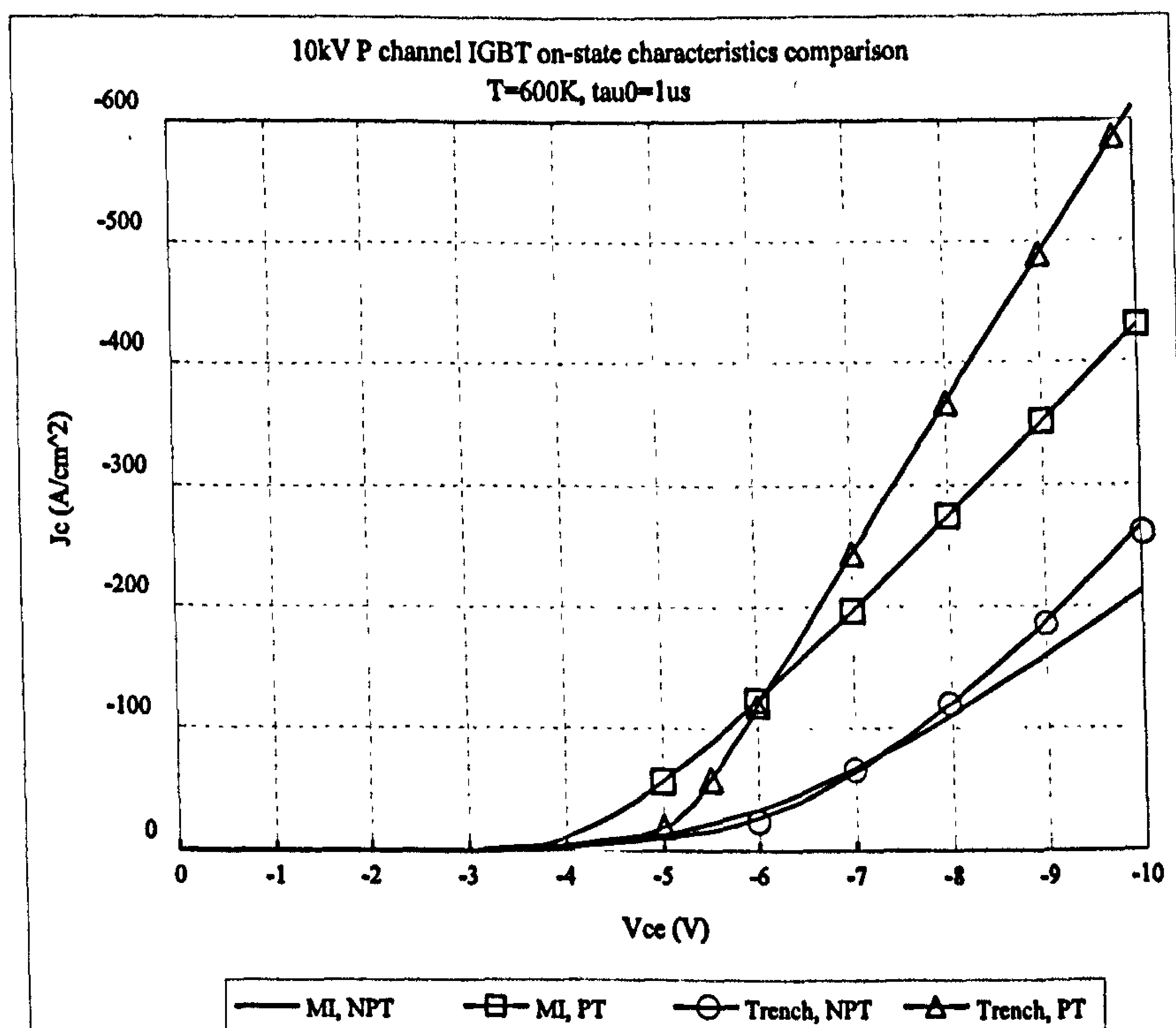

(d)

Figure 6.13 Comparison of 10 kV P-channel IGBT on-state characteristics with various structures (a)300K, τ_0=400ns, (b)600K, τ_0=400ns, (c)300K, τ_0=1μs and (d) 600K, τ_0=1μs

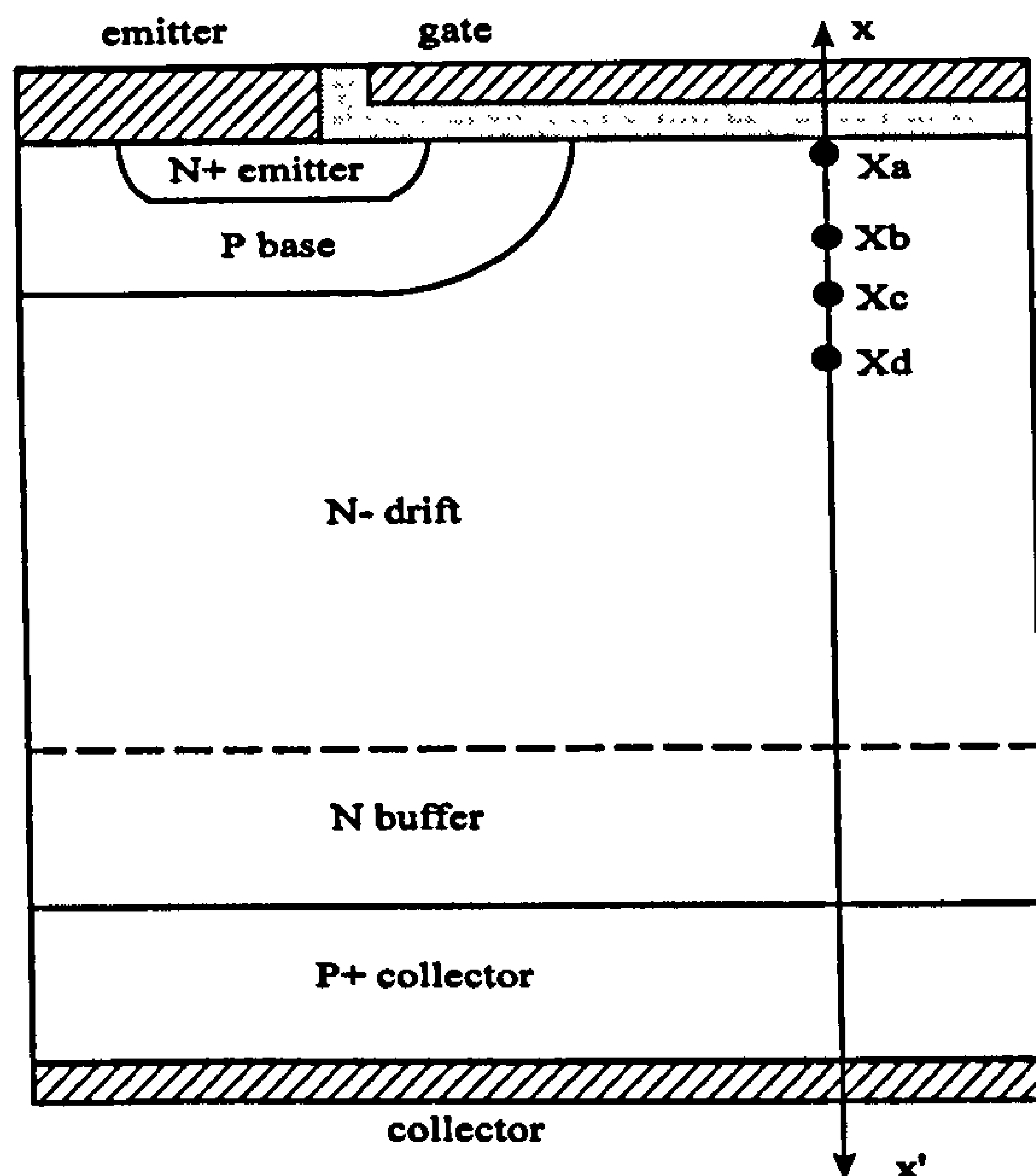

Figure 6.14 (a) SiC N-channel MI IGBT cell structure

However, if the drift region doping and width are not carefully designed, the PT IGBT may exhibit a worse performance than its NPT couterpart. Master files which contain potential and carrier distribution information for devices can be generated in the numerical simulators. The two structures have a forward current density of 100 A/cm^2. Figure 6.14 (b) shows hole concentration and potential distribution along the cutline X-X' (Figure 6.14.(a)) in N-channel IGBTs. In both structures, the accumulation layer formed under the gate between the P base diffusions and holes injected from the P base into the N drift region reduce the N drift region resistivity from point x_a to point x_b, resulting in a negligible voltage drop. However, between x_b and x_c, the depletion layer which extends into the N drift region reduces both the carrier concentrations and the current path width, leading to a rapid potential increase in this JFET region. The resistivity in this region is mainly determined by the N drift region doping level. Compared to the NPT IGBT, the JFET effect hampers the performance of the PT IGBT more severely because the PT IGBT has a 50%-75% lower doping level than the NPT IGBT. It can be seen in Fig. 6.14. (b) that the potential in the PT IGBT increases by 1.5 V more from x_b to x_c than in the NPT IGBT.

From point x_d, carriers injected from the P^+ collector modulate the resistivity of the N drift region, hence the potential increases slowly. Because of the smaller drift region thickness of the PT IGBT, the hole concentration in this device is higher than that in the NPT IGBT.

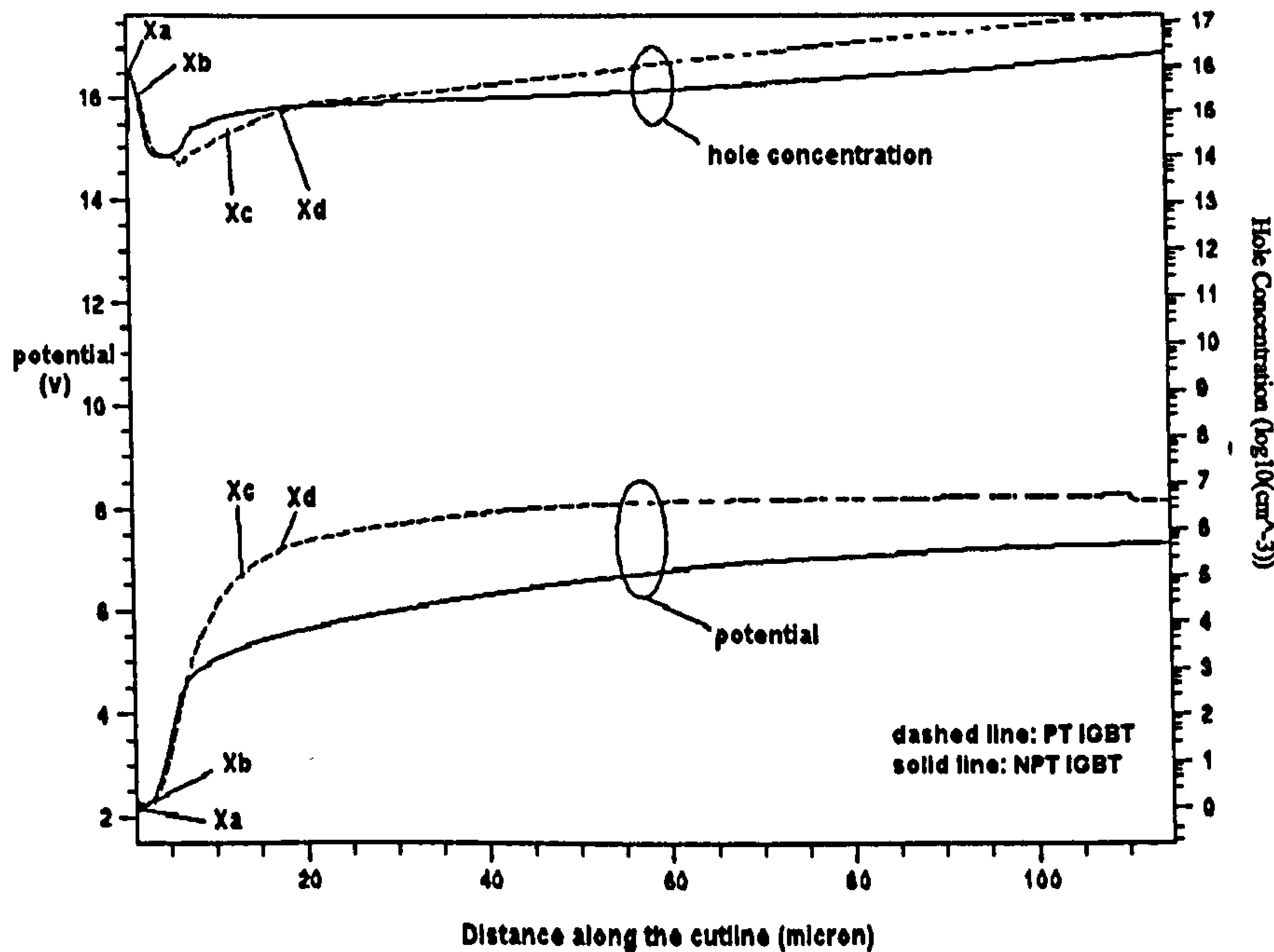

Figure 6.14 (b) On-state electric field and hole concentration distribution in SiC IGBTs

The hard switching characteristics of the devices with a clamped resistive load have been simulated at temperatures of 300 K and 600 K. The supply voltage is 5 kV and the on-state current is 1.2 kA. The device area is 24 cm^2. Table 6.2 lists the main results.

As expected, the devices show increased turn-off losses when increasing lifetime and temperature because more excess carriers must be removed. The turn-on times and losses remain relatively steady with change of lifetime. Elevating the temperature, the devices turn on slightly faster, leading to a slightly smaller turn-on loss.

The NPT IGBTs switch slower than their PT couterparts in most cases. With a lifetime of 1 μs, it takes 22.5 μs for the collector current to fall from 95% to 5% of the steady-state value in an NPT TIGBT and the turn-off loss is 21 J, whilst for the PT case the current fall time and turn-off loss are 4.6 μs and 4.6 J respectively.

Comparing the switching performance of TIGBTs and MI IGBTs, the MI IGBT turn-on losses are smaller. MI NPT IGBTs have smaller turn-off losses than their Trench Gate counterparts, whilst MI PT IGBTs have larger turn-off losses than their Trench Gate counterparts except when τ_0=500 ns and T=300 K.

Table 6.2 The Switching characteristics of 10 kV IGBTs

	T (K)	τ_0 (μs)	$t_{d(on)}$ (μs)	t_r (μs)	$t_{d(off)}$ (μs)	t_f (μs)	E_{on} (J)	E_{off} (J)
Trench PT	300	0.5	0.24	1.39	1.9	1.67	1.5	1.8
		1	0.16	1.37	1.1	1.77	1.51	1.87
	600	0.5	0.3	1.27	2.06	2.97	1.39	3.11
		1	0.2	1.25	1.42	4.62	1.38	4.64
Trench NPT	300	0.5	0.32	2.12	1.83	2.53	2.28	2.88
		1	0.33	2.1	1.87	4.48	2.26	4.17
	600	0.5	0.29	1.95	2.08	9.48	2.1	8.3
		1	0.2	1.96	2.17	22.5	2.1	21
MI PT	300	0.5	0.04	0.42	1.88	1.28	0.45	1.24
		1	0.06	0.41	1.93	2.86	0.45	2.6
	600	0.5	0.04	0.45	2.19	6.87	0.56	6.51
		1	0.05	0.47	2.75	14.1	0.54	12.6
MI NPT	300	0.5	0.14	0.66	1.94	1.6	0.69	1.59
		1	0.14	0.65	1.98	3.8	0.71	3.22
	600	0.5	0.15	0.71	1.99	9.11	0.82	7.72
		1	0.14	0.7	2.07	21.5	0.76	20.37

A noticeable point of PT IGBT turn-off is a voltage flattening out during the voltage rising phase (Fig. 6.15 (a)). In Fig. 6.15 (b)-(c) the hole concentration and the electric field distribution in the drift region of the device during turn-off are shown. At room

temperature, initially the depletion layer quickly extends into the N^- drift region towards the N buffer. At t_b, the voltage waveform flattens out until t_c. It only takes 110 ns (t_b-t_a) for the voltage to increase 1200V. In comparison, it takes 800ns (t_c-t_b) for the voltage to increase another 1200V. With the aid of Fig. 6.15 (c), this phenomenon can be explained by considering the hole concentration distribution in the N^- drift region. In the forward conduction state, holes are injected from the P^+ collector into the N buffer and N^- drift region. The hole concentration in the N^- drift region has a peak value at the N^- drift/N buffer junction, which decays exponentially toward the P base/N^- drift junction. Therefore, a large portion of excess carriers exists in the region near the N^- drift/N buffer junction. As indicated in Fig. 6.15 (c), between t_b and t_c, the stored charges removed from the N^- drift region as a result of the extending depletion layer, are about 10 times higher than those between t_a and t_b. At the time t_c, the depletion layer edge reaches the N buffer. Then it extends slightly into the N buffer and the magnitude of the electric field, hence the collector voltage increases quickly. In NPT IGBT structures, most of the excess carriers in the N drift region also exist near the P^+ collector. However, to support the supplied voltage, the depletion layer edge does not approach the P^+ collector due to the NPT structure. Therefore, the voltage across the NPT IGBTs rises rapidly and does not slow down as with PT IGBTs, although a long current tail is observed. If the blocking voltage is less than the reach-through voltage (the voltage when the depletion layer just extends to the drift region/buffer layer junction) of the PT IGBT, voltage flattening-out will not occur during turn-off. The flattening-out of the voltage in PT IGBTs can be minimised by designing the structure carefully so that the drift region minority carrier distribution under conduction is more uniform.

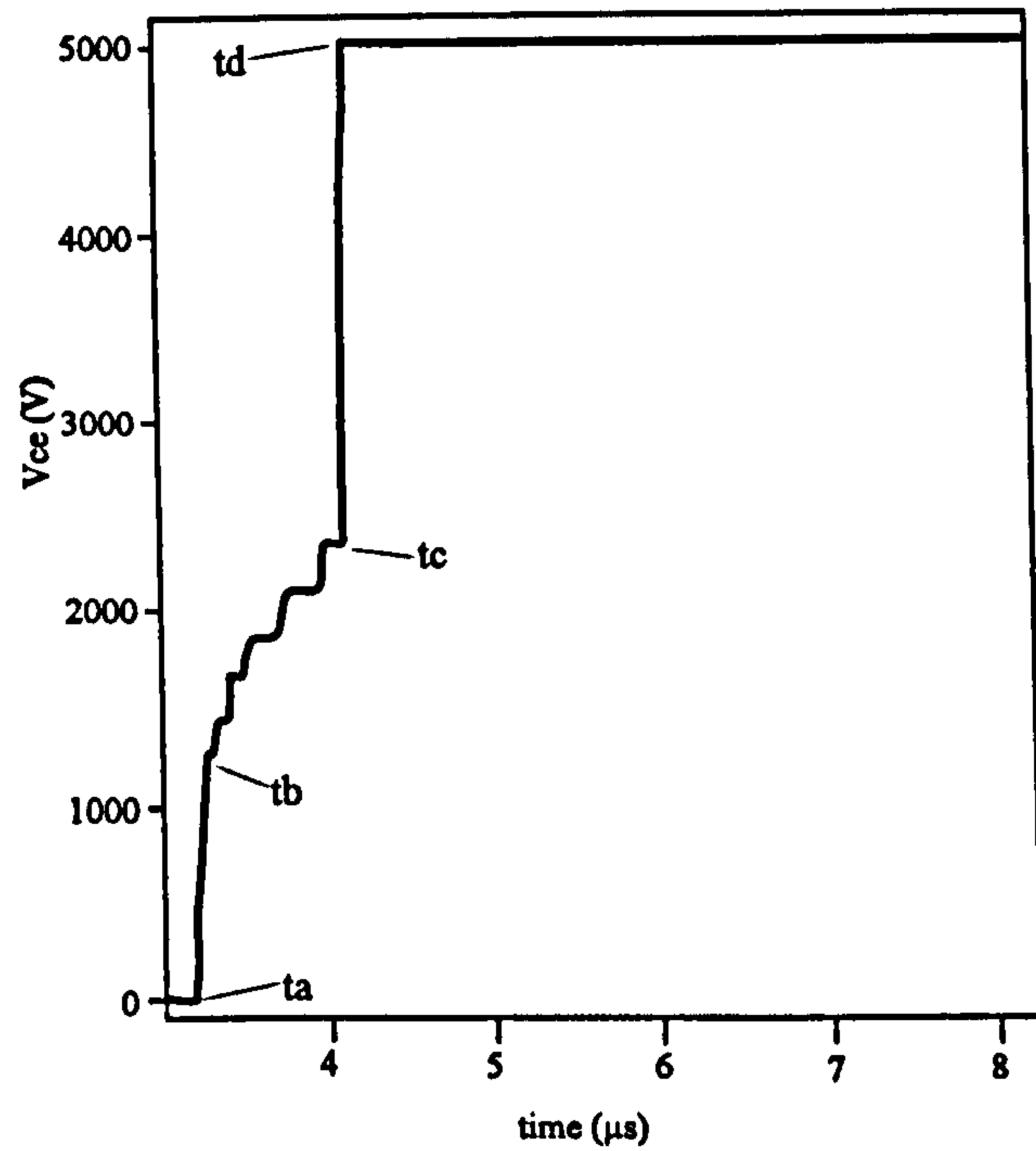

Figure 6.15 (a) A 4H-SiC N-channel TIGBT switch-off characteristic

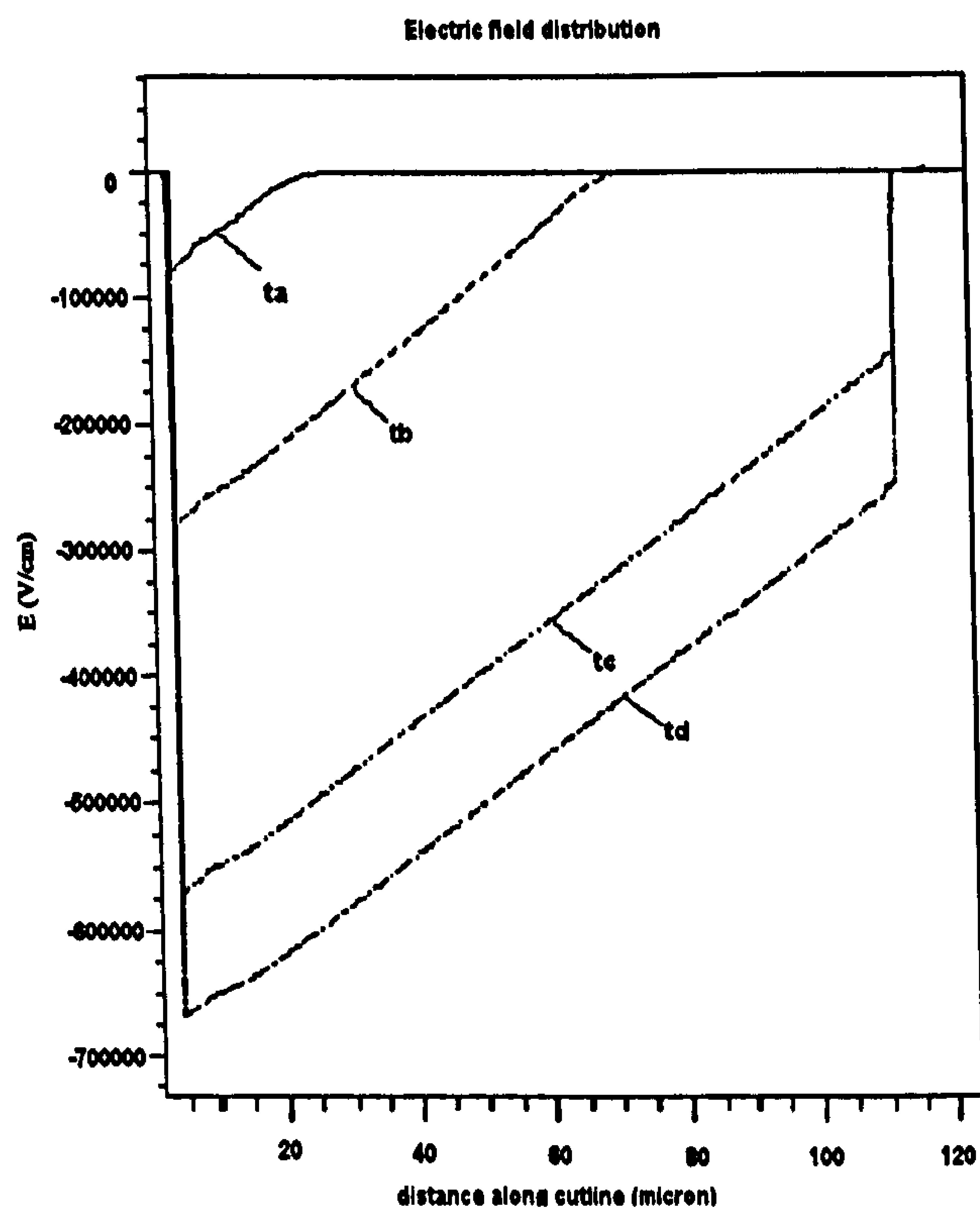

Figure 6.15 (b) Electric field distribution during 4H-SiC IGBT turn-off at T=300K

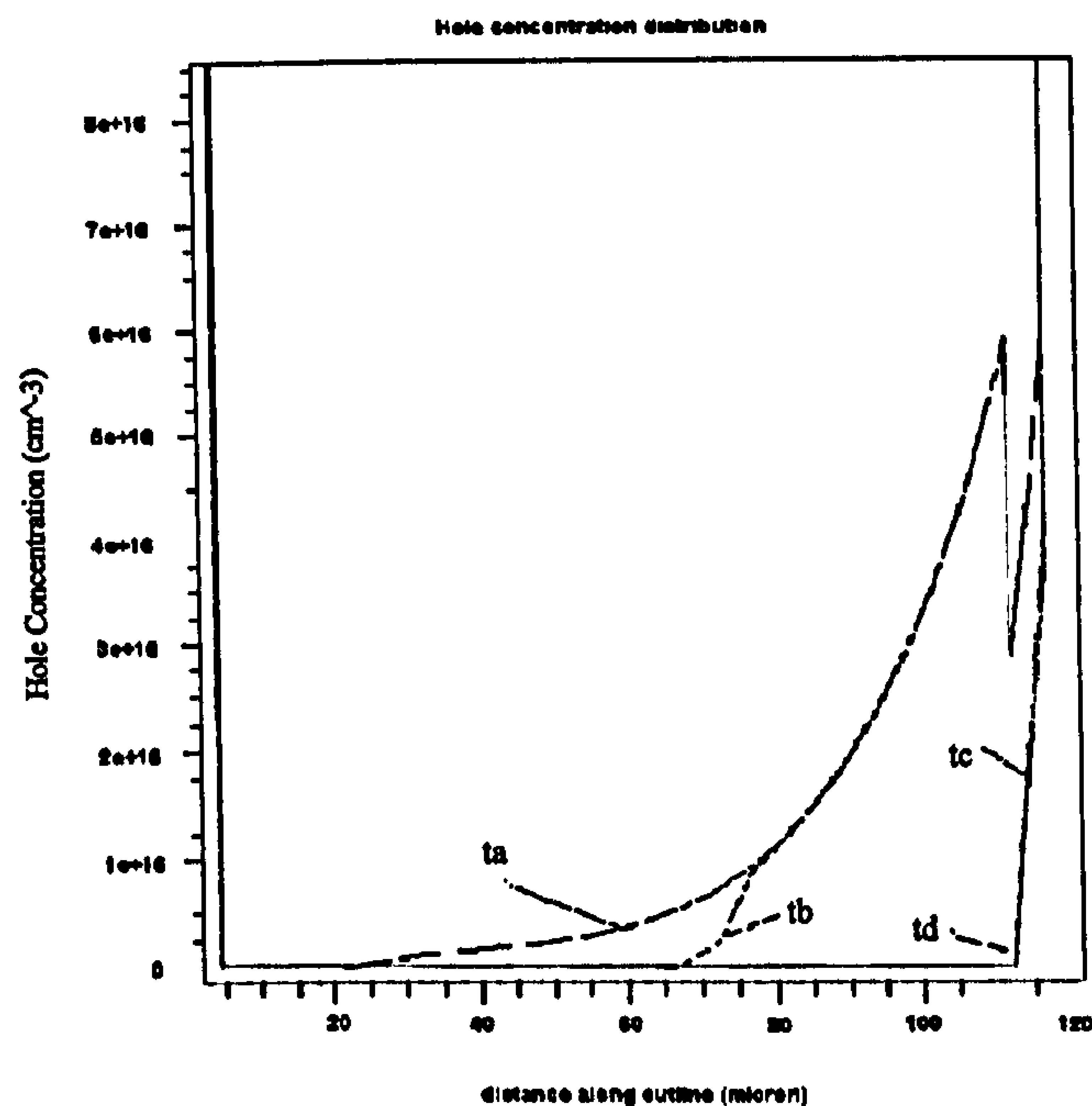

Figure 6.15 (c) Hole concentration distribution during SiC 4H-SiC IGBT turn-off at T=300 K

6.4 Conclusion

In this chapter, the performance of SiC IGBTs with various voltage ratings, lifetime and structure have been simulated using a 2-D finite element simulator and a 2-D analytical IGBT model. Some characteristics such as threshold voltage versus base doping level, breakdown voltage versus lifetime, gate/collector area ratio impact on device performance and P-channel IGBTs versus N-channel IGBTs have been studied and presented.

To ensure current sharing between parallel connected IGBTs and on large area devices, a negative on-state characteristic temperature dependence is desirable. However, due to significantly improved degree of ionization at elevated temperature, the IGBTs simulated show lower on-state voltage at 600 K than 300 K in the typical operating current range. The 4 kV and 7 kV 4H-SiC P-channel IGBTs show much better on-state characteristics than a 3.3 kV Si IGBT and 6.5 kV Si GTO respectively. At 400 K, the 7 kV SiC IGBT has comparable current handling ability to the 6.5 kV Si thyristor. Considering

the long turn-off time of Si thyristors (typically in the order of 100 μs), SiC IGBTs are promising future replacement for the Si thyristor.

By choosing suitable device areas to obtain a reasonable on-state voltage at a 1.2 kA on-state current, the turn-off times of 1 kV and 10 kV IGBTs are 0.7 and 1.7 μs at 300 K respectively. The turn-off times at 600 K are 2 to 3 times longer than those at room temperature.

Due to the relatively higher degree of ionization of acceptors than donors in SiC, the 4H-SiC N-channel TIGBT is not suitable for applications at 300 K-400 K and the P-channel IGBT is a better choice. Increasing the temperature, the 4H-SiC N-channel IGBT performance is greatly improved. At high temperature, from the trade-off curves between switching speed and current handling ability, it is clear that P-channel IGBTs have a faster switching speed whilst N-channel IGBTs exhibt a lower on-state voltage at the respective best trade-off points.

The multiple implantation technology used in fabricating the base region in DMOS lateral channel IGBTs results in a lower threshold voltage, higher channel carrier mobility and prevents the depletion layer from reaching the emitter/base junction. Consequently, the performance of SiC MI IGBTs is improved significantly. At low operating current density, MI IGBTs have lower on-state voltages than TIGBTs. However, the current handling ability of MI IGBTs can not compete with that of TIGBTs in the high operating current density range. The current handling ability of TIGBTs can be improved by changing the gate/emitter area ratio.

The performance of SiC PT IGBTs is superior to that of SiC NPT IGBTs. The reason for voltage flattening-out during PT IGBT turn-off has been explained by investigating the carrier and electric field distribution inside the device.

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CHAPTER 7

EVALUATION OF HIGH-VOLTAGE 4H-SIC SWITCHING DEVICES

Properties such as high breakdown electric field strength, reasonable electron mobility, wide bandgap, high thermal conductivity and high electron saturation velocity make SiC an attractive candidate for fabricating power devices with reduced power losses and die size [7.1].

The SiC MOSFET is a promising solution to the problem of Si MOSFET's strong conduction characteristic dependence on voltage rating and temperature. Extremely attractive projections for SiC MOSFETs have been made based on analysis of the specific on-resistance associated with the drift layer, $R_{D,sp}=W/q\mu n$ [7.2], [7.3]. The near ideal on-resistance projection of SiC devices and the appealing advantages of MOSFETs, such as switching speed, peak current capability, ease of drive, wide safe operating area (SOA), avalanche and dv/dt ability [7.4], meant that the SiC MOSFET was the first type of SiC power switch to be developed. Several high voltage SiC MOSFETs have been demonstrated [7.5-7.9].

Having traded off between different characteristics, minority carrier devices such as the IGBT, BJT, GTO, thyristor and SITh [7.10-7.14] are important for various applications. A 200 V fully planarized, 6H-SiC TIGBT and a 300 V 4H-SiC SITh have been reported [7.15], [7.16]. In spite of their high switching losses and gate drive circuit complexity, silicon thyristors and GTOs continue to dominate very high voltage and current applications. For applications such as the electric gun [7.17] where high power pulses are needed, the exceptional current handling ability of thyristors and GTOs is of particular

importance. A 700 V SiC thyristor and GTO have been fabricated [7.18], [7.19].

This chapter investigates the performance of SiC MOSFETs, IGBTs, BJTs, SIThs and GTOs for high voltage, high temperature, high frequency applications. SiC thyristors are not included for they are only semi-controllable devices and their general characteristics are indicated by GTOs. Based on the simulation results, a comprehensive comparison and evaluation of SiC devices is carried out with regard to thermal limitations. Comparison with silicon devices is included.

The SiC devices investigated are 4H-SiC based for the reasons stated in Chapter 3 and Chapter 5.

7.1 Simulation Parameters and Structures

The simulated structures and parameters are shown in Figure 7.1. The only parameters adjusted when varying the design voltage are the drift region doping level and thickness. In Figure 7.1, the drift region doping level and thickness are for 10 kV devices. To reflect technology and material limitations, all the devices are fabricated using chemical

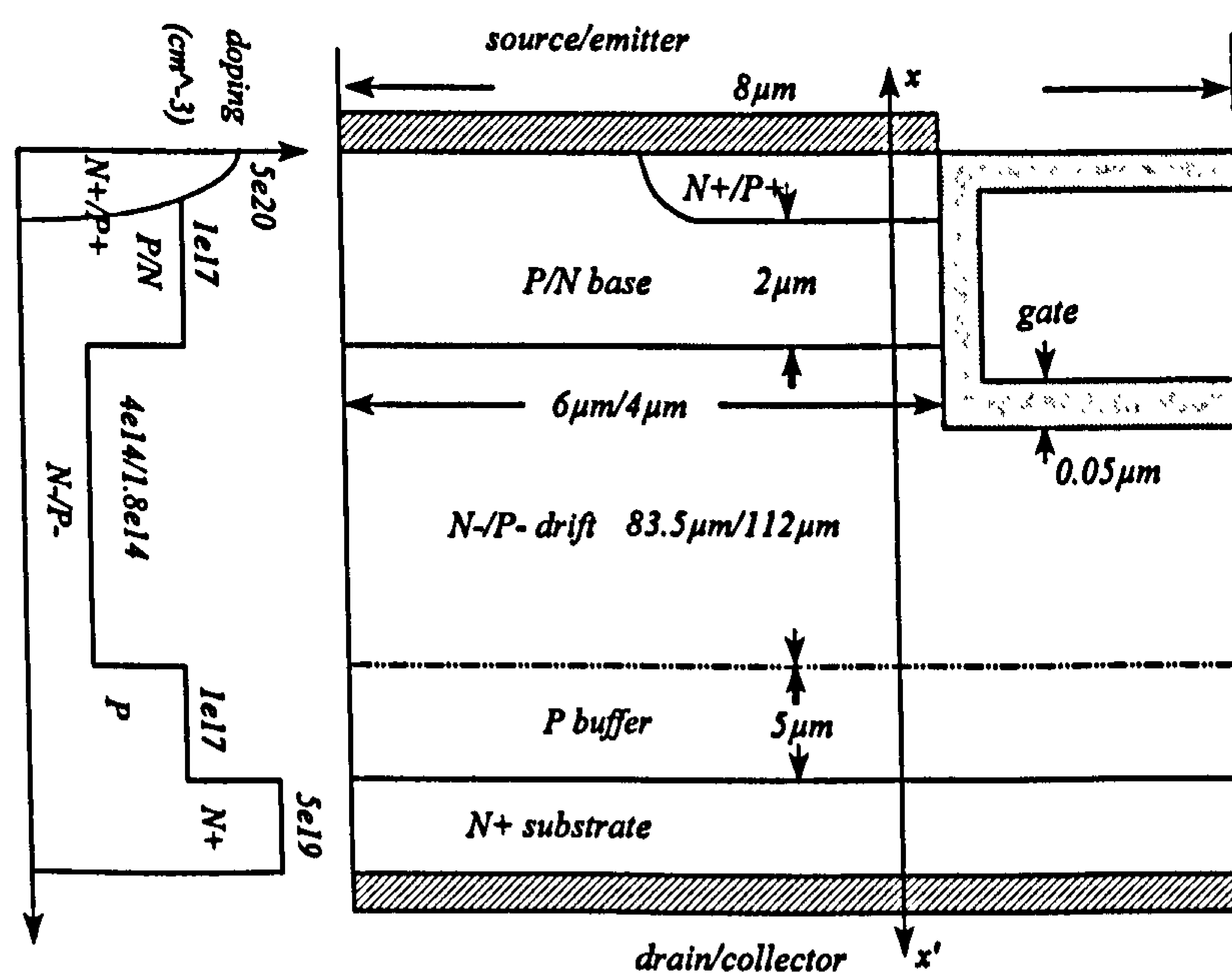


Figure 7.1 (a)

vapour deposition (CVD) epitaxy, reactive ion etching (RIE) and relatively shallow ion implantations.

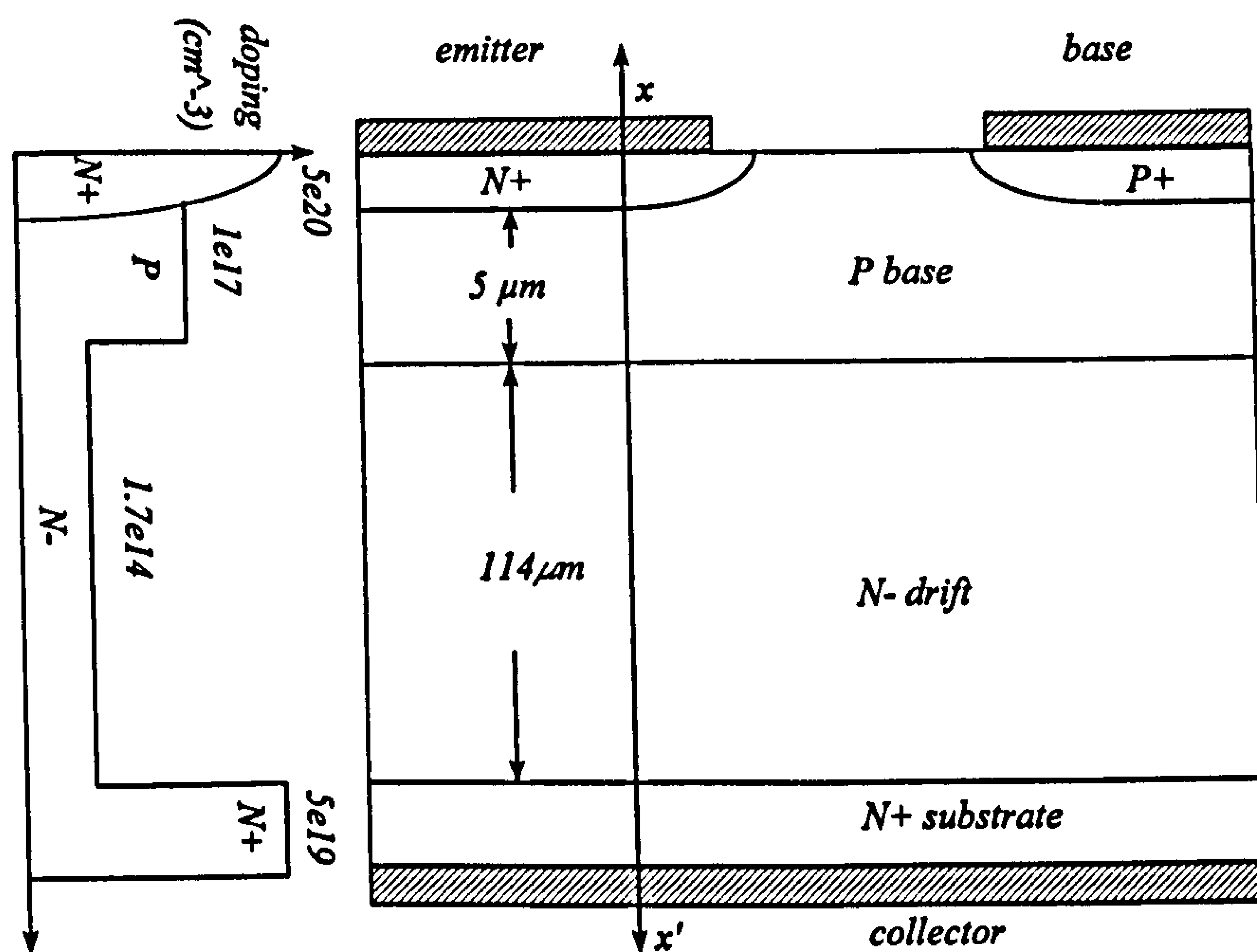


Figure 7.1 (b)

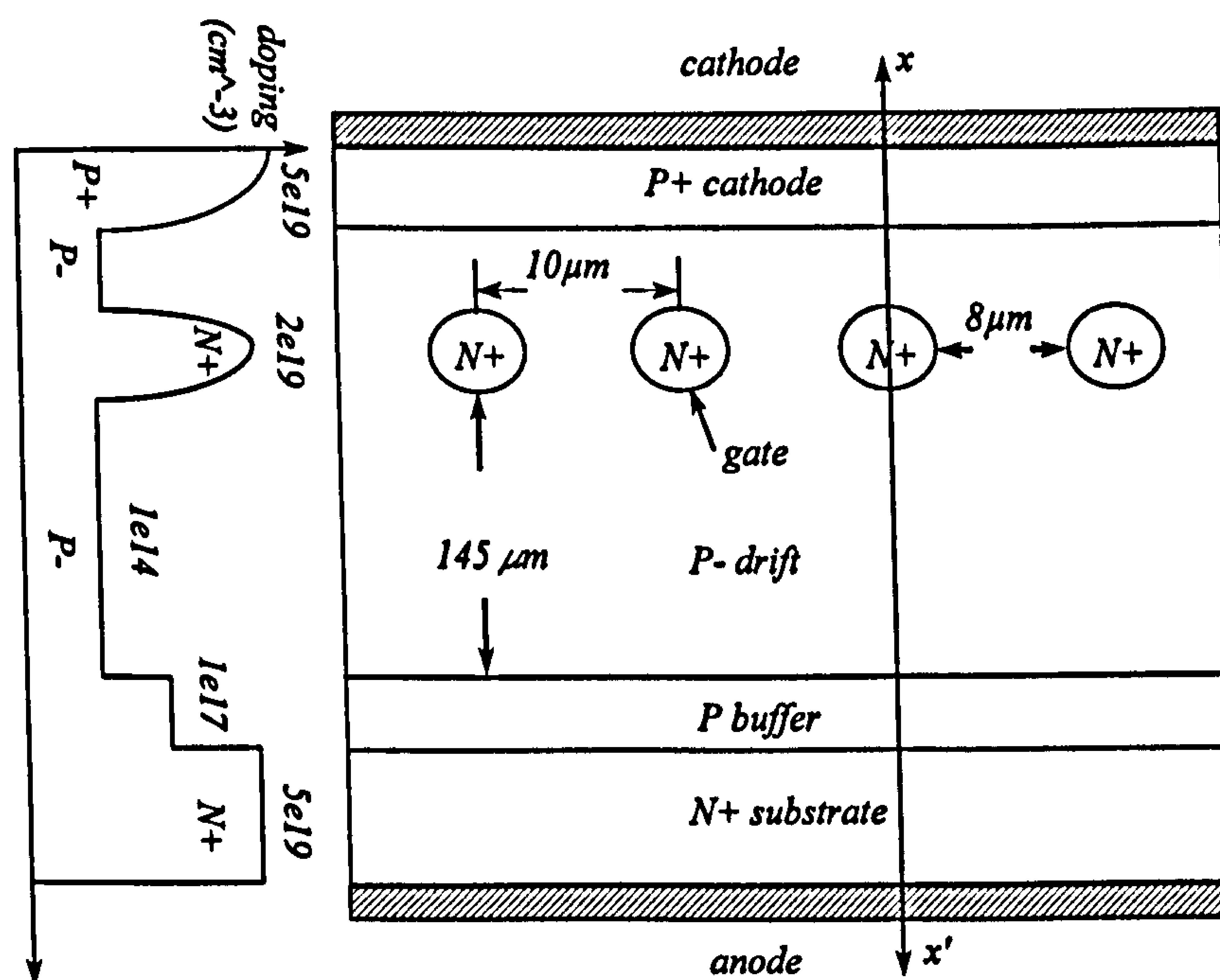


Figure 7.1 (c)

The simulations are performed for SiC devices with voltage ratings from 1 kV to 10 kV. To obtain better on-state characteristics, it is customary to utilize a punch-through (PT) or PiN structure. For IGBTs, MOSFETs, BJTs and SIThs, the punch-through structure

is utilized. However, for GTOs where latch-up is necessary to hold-on the device, the PT structure elevates the latching and holding current levels, hence a high gate drive current is required. For this reason the simulated GTOs utilize a NPT structure.

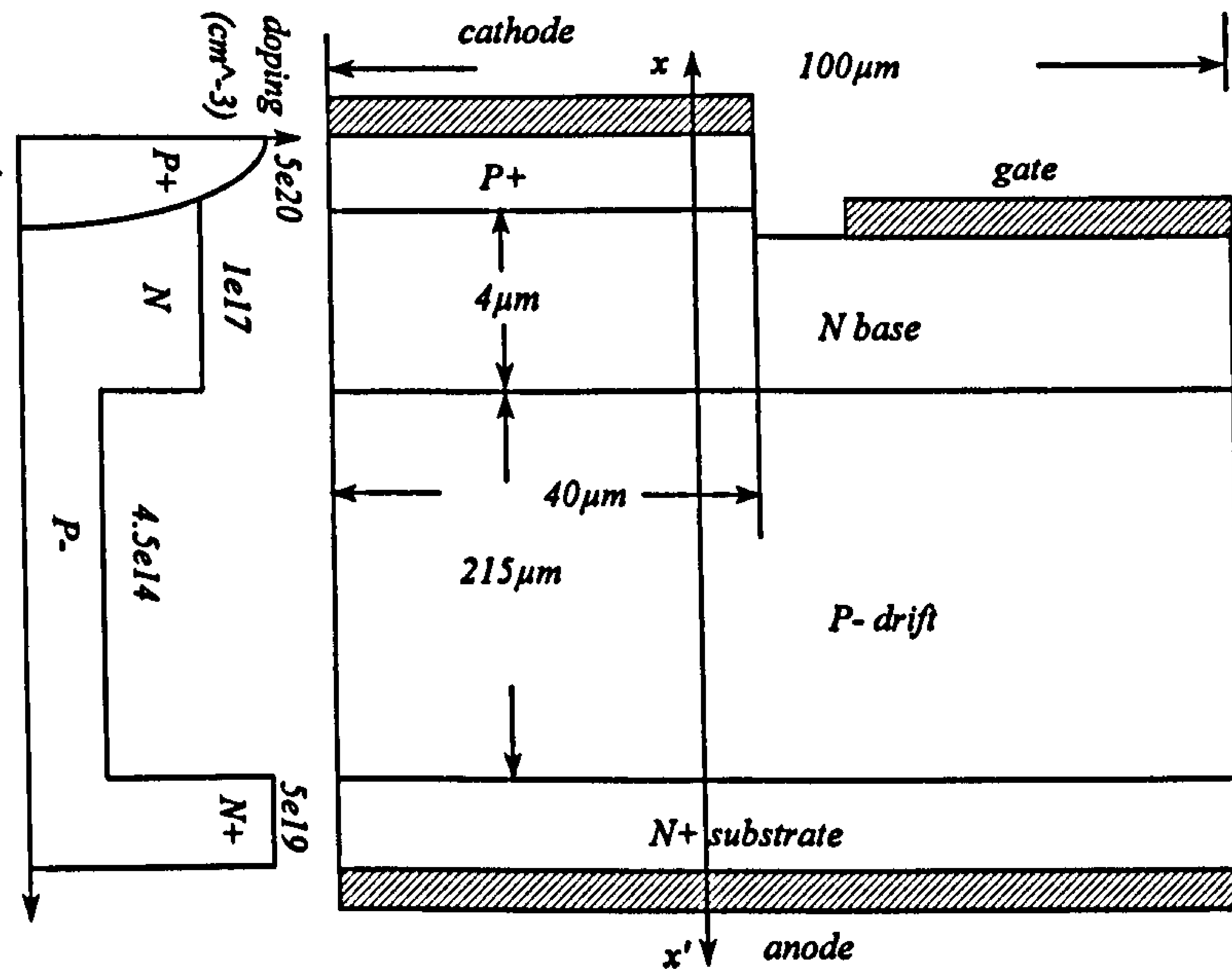


Figure 7.1 (d)

Figure 7.1 Simulated device cell structures (a) IGBT/MOSFET, (b) BJT, (c) SITh and (d) GTO

The breakdown voltage of a MOSFET depends on its internal P base/N^- drift diode whilst the breakdown voltage of an IGBT depends on its integral P^+ substrate/N^- drift/P base transistor. Breakdown in a BJT structure occurs when the product of the multiplication factor M and the current gain α reaches unity, resulting in a lower voltage rating than the corresponding P-N junction diode. Therefore IGBTs and BJTs have a lower drift region doping level and a thicker drift region than corresponding MOSFETs. The doping level of the SITh drift region is kept at 1×10^{14} cm^{-3} for all the voltage ratings to improve gate turn-off capability.

As shown in Chapter 6, the current handling ability of SiC N channel IGBTs (which have a P^+ substrate) is severely impaired by the relatively larger ionization energy of acceptors, especially at room temperature. Since in SiC the degree of ionization of donors

is larger than that of acceptors, the IGBTs, SIThs and GTOs investigated have a complementary structure to the typical Si devices in order to incorporate an N^+ substrate. The 300 μm substrate is doped at 5×10^{19} cm^{-3}.

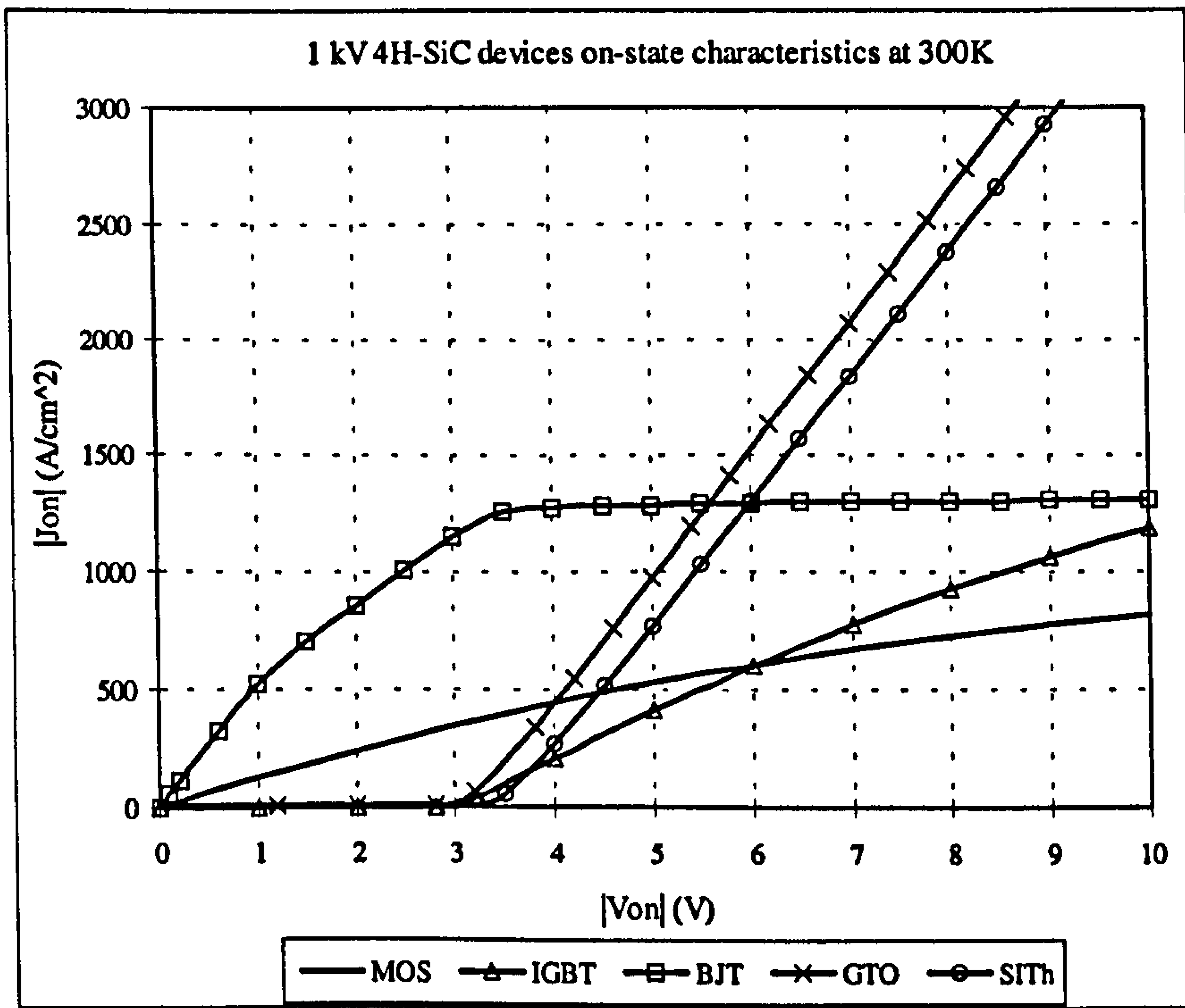
The simulated MOSFETs and IGBTs have a trench gate (UMOS) structure. SIThs have a buried-gate structure.

7.2 On-State Characteristics

The on-state characteristics of the SiC devices are simulated at temperatures of 300 K and 600 K. Figure 7.2 shows the forward conduction characteristics of SiC devices with voltage ratings of 1 kV, 5 kV and 10 kV. The gate-source voltage magnitude for the SiC IGBTs and MOSFETs is 15 V. BJT base current and GTO gate current are maintained at 20 A and 5 A respectively. The SITh is operated with an open-circuit gate.

For SiC BJTs and MOSFETs, τ_0 is 2 μs and 20 ns respectively. For IGBTs and SIThs the lifetime is adjusted with voltage rating to achieve a reasonable trade-off between on-state characteristics and switching characteristics. The GTO lifetime τ_0 is chosen as 3 μs and 1 μs at 300 K and 600 K respectively. The reasons for these values will be explained in subsequent sections.

The forward voltages with an on-state current density of 100, 200 and 300 A/cm^2 are plotted in Figure 7.3.



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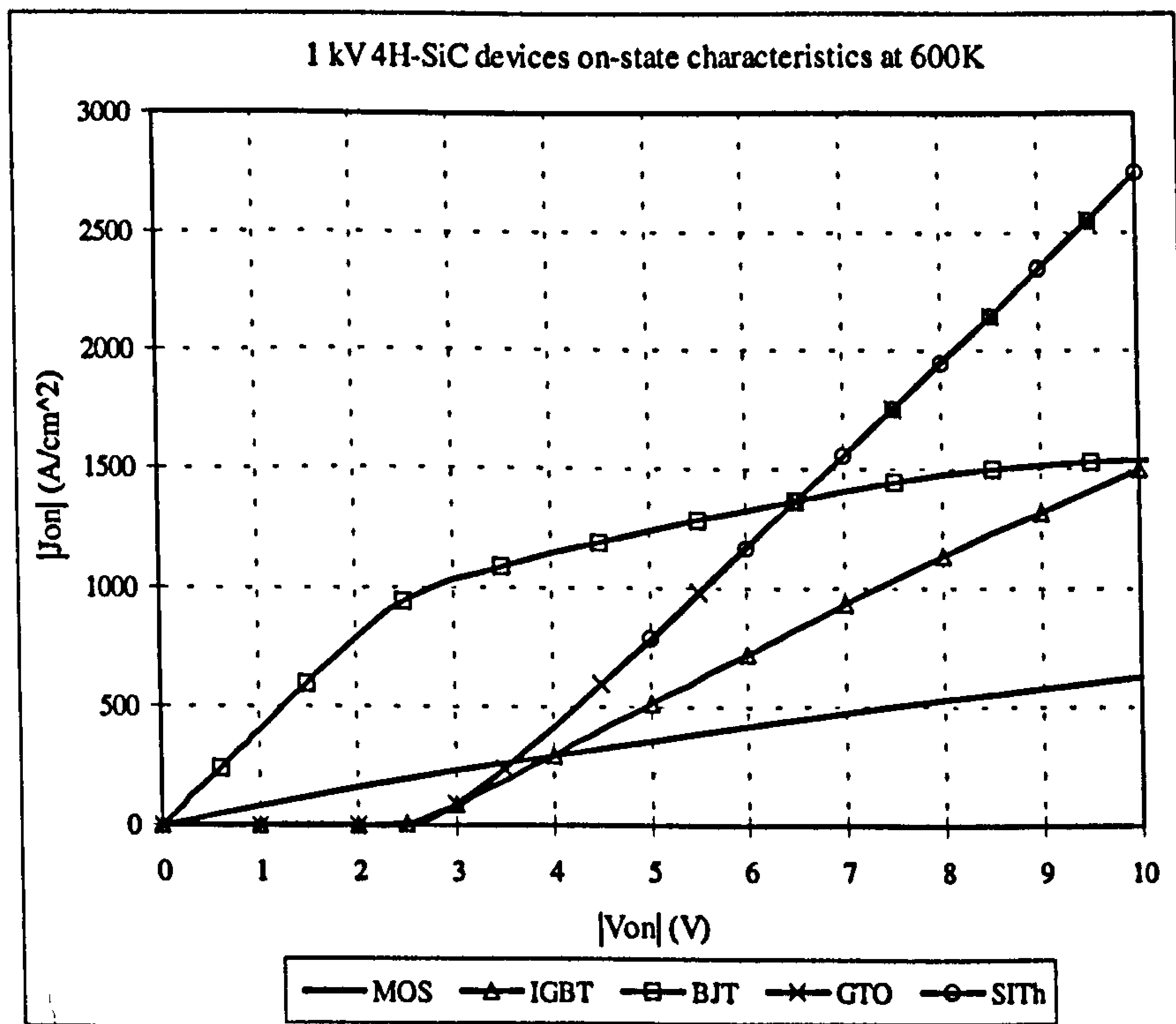

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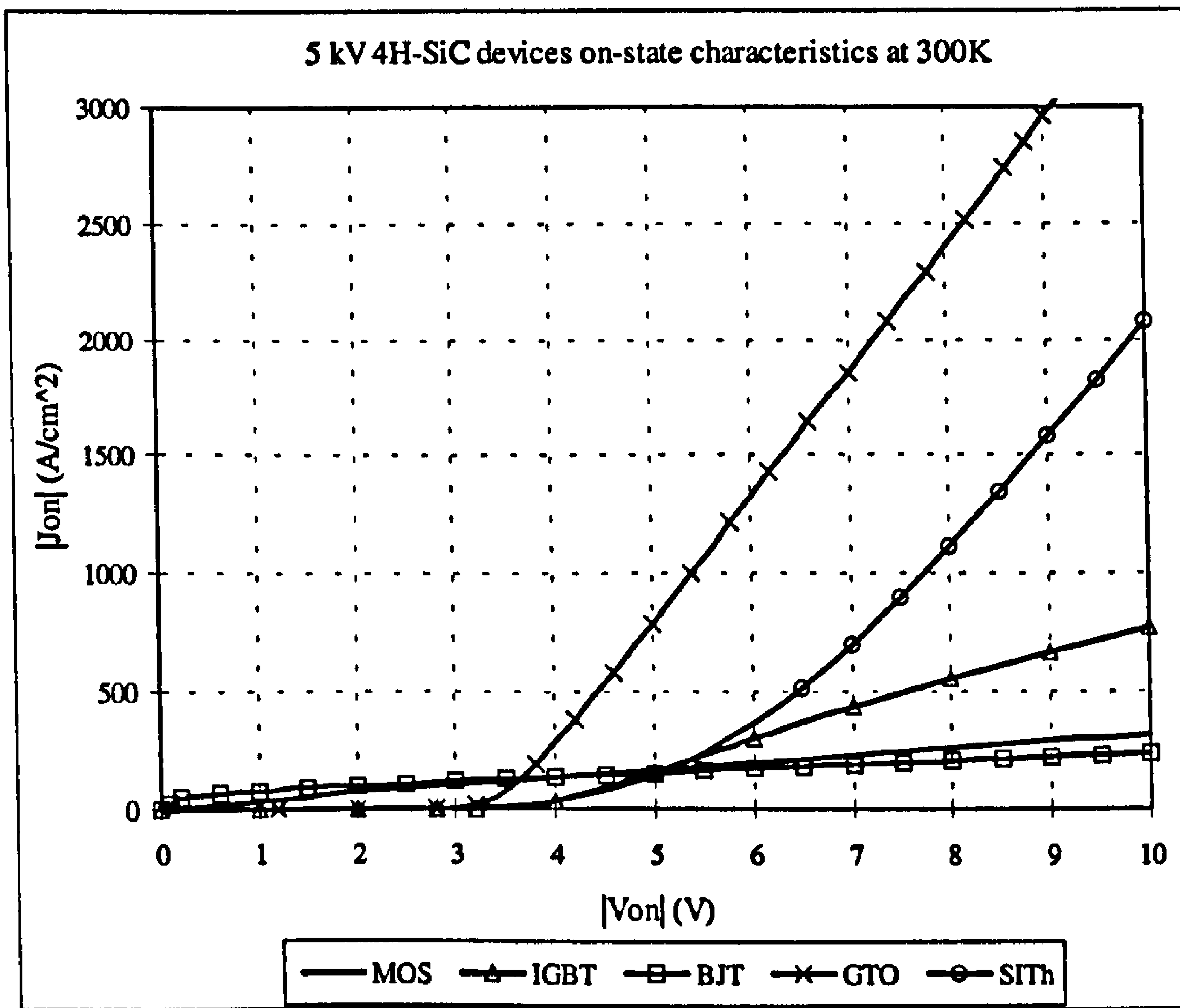

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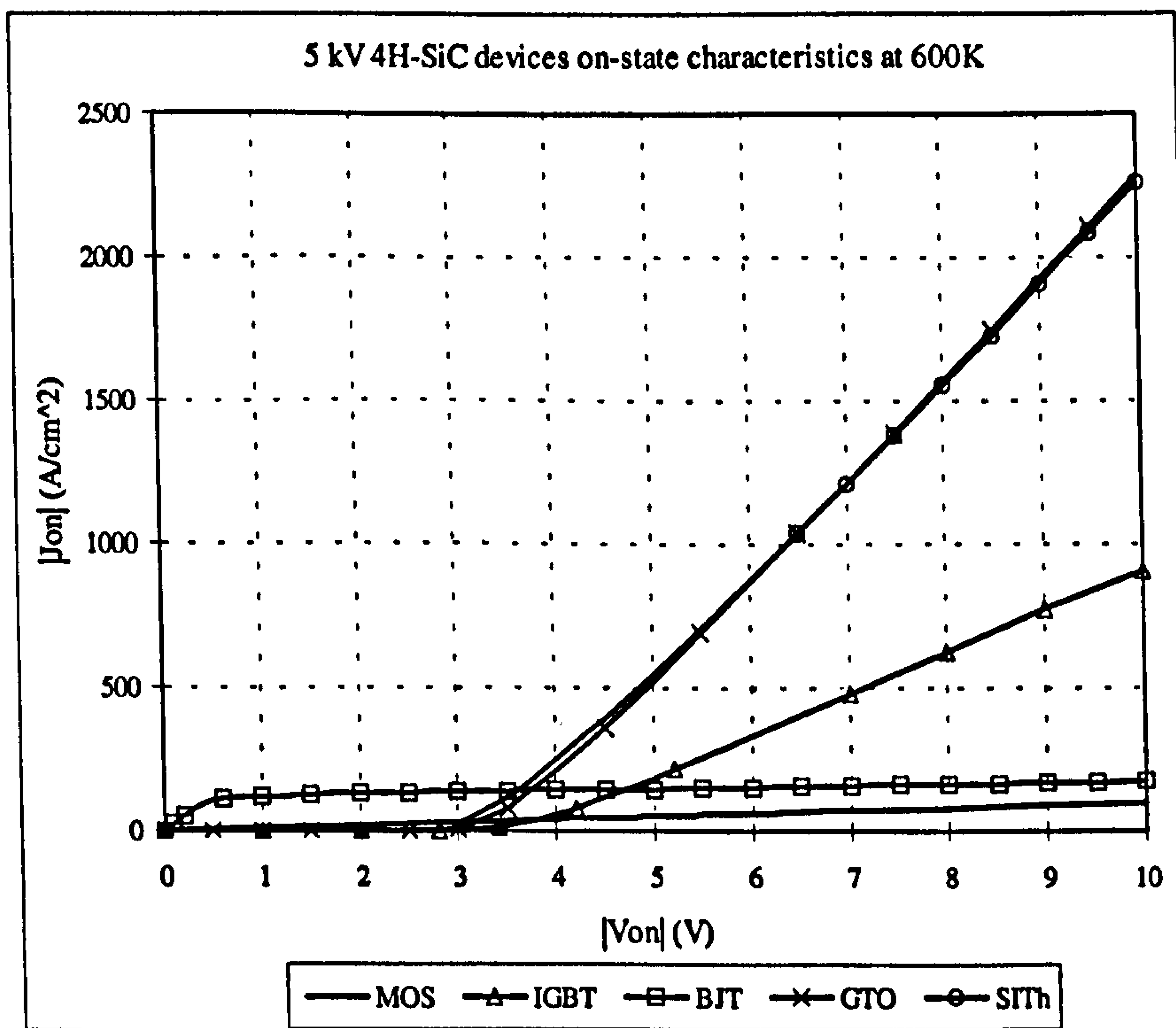

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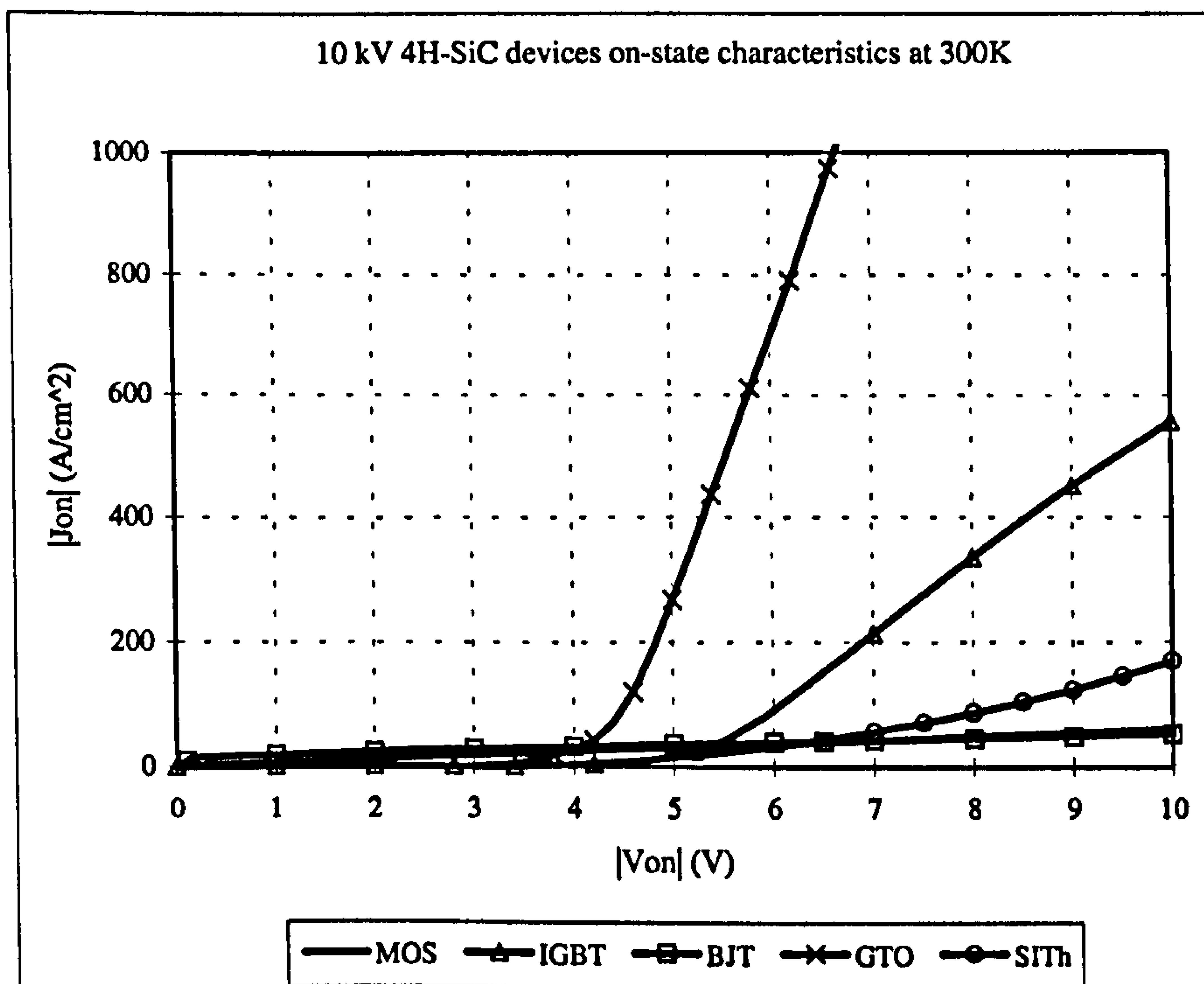

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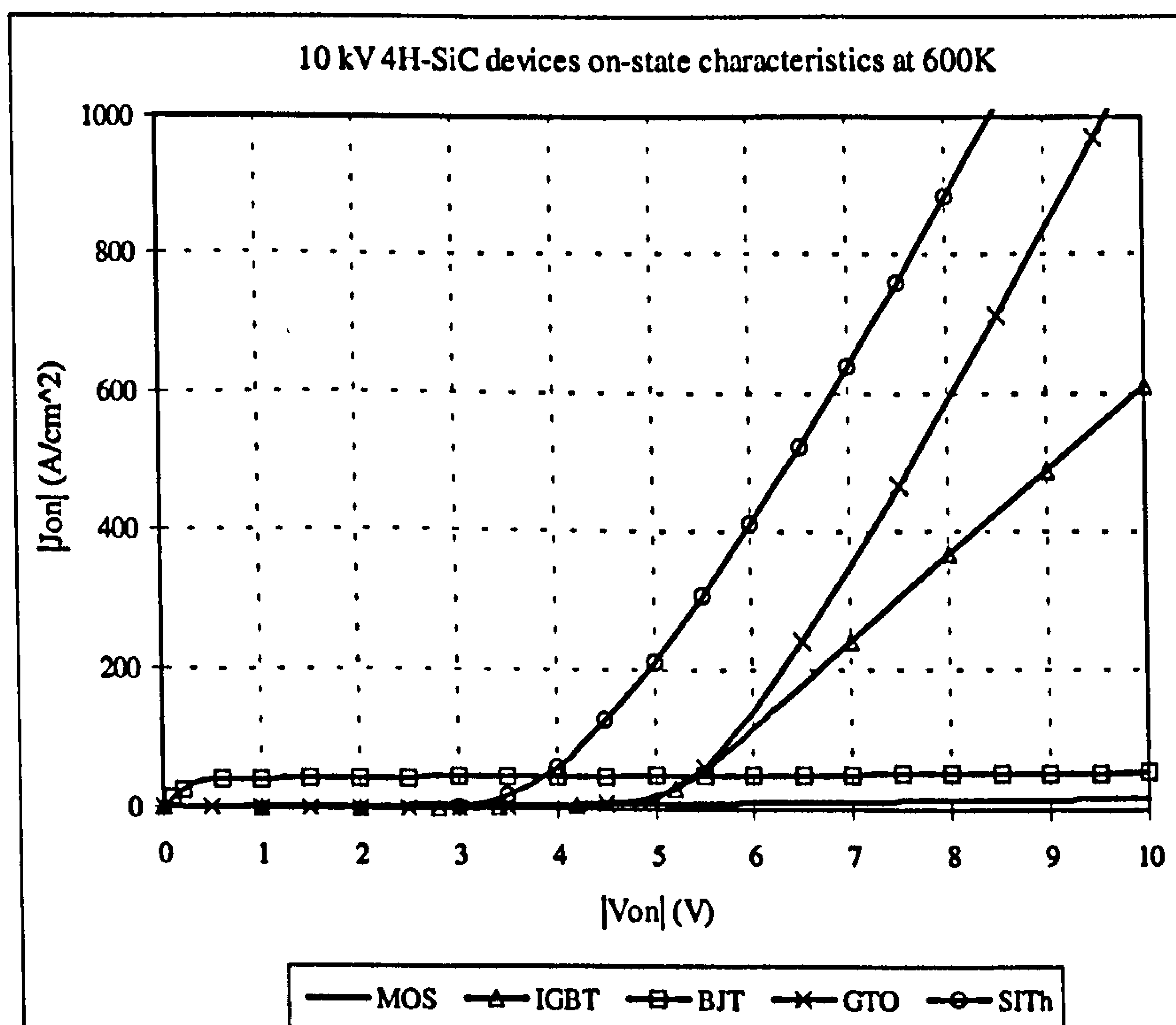
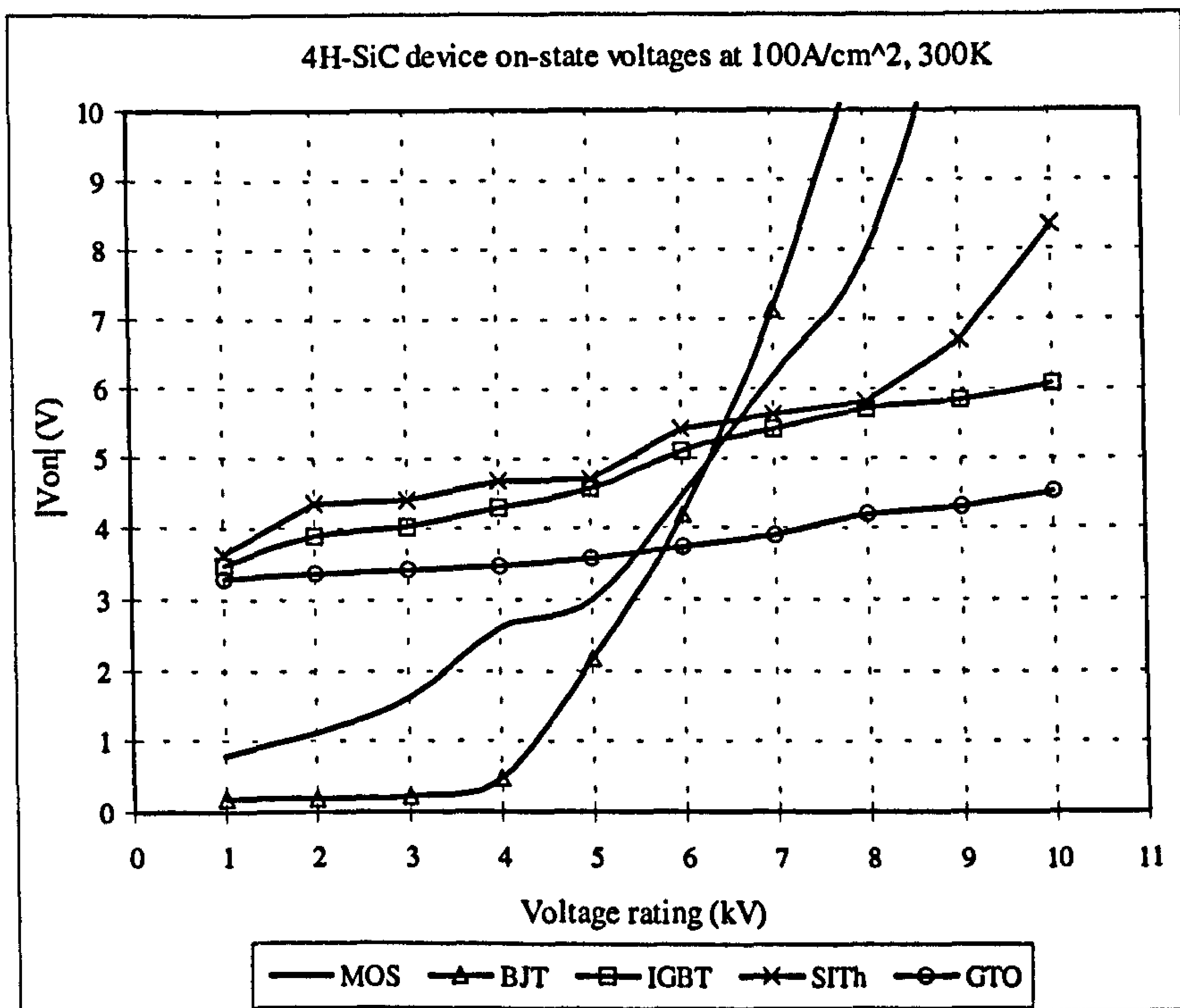


(f)

Figure 7.2 4H-SiC devices on-state characteristics (a) 1kV, 300K; (b) 1kV, 600K; (c) 5kV, 300K; (d) 5kV, 600K; (e) 10 kV, 300K and (f) 10 kV, 600K



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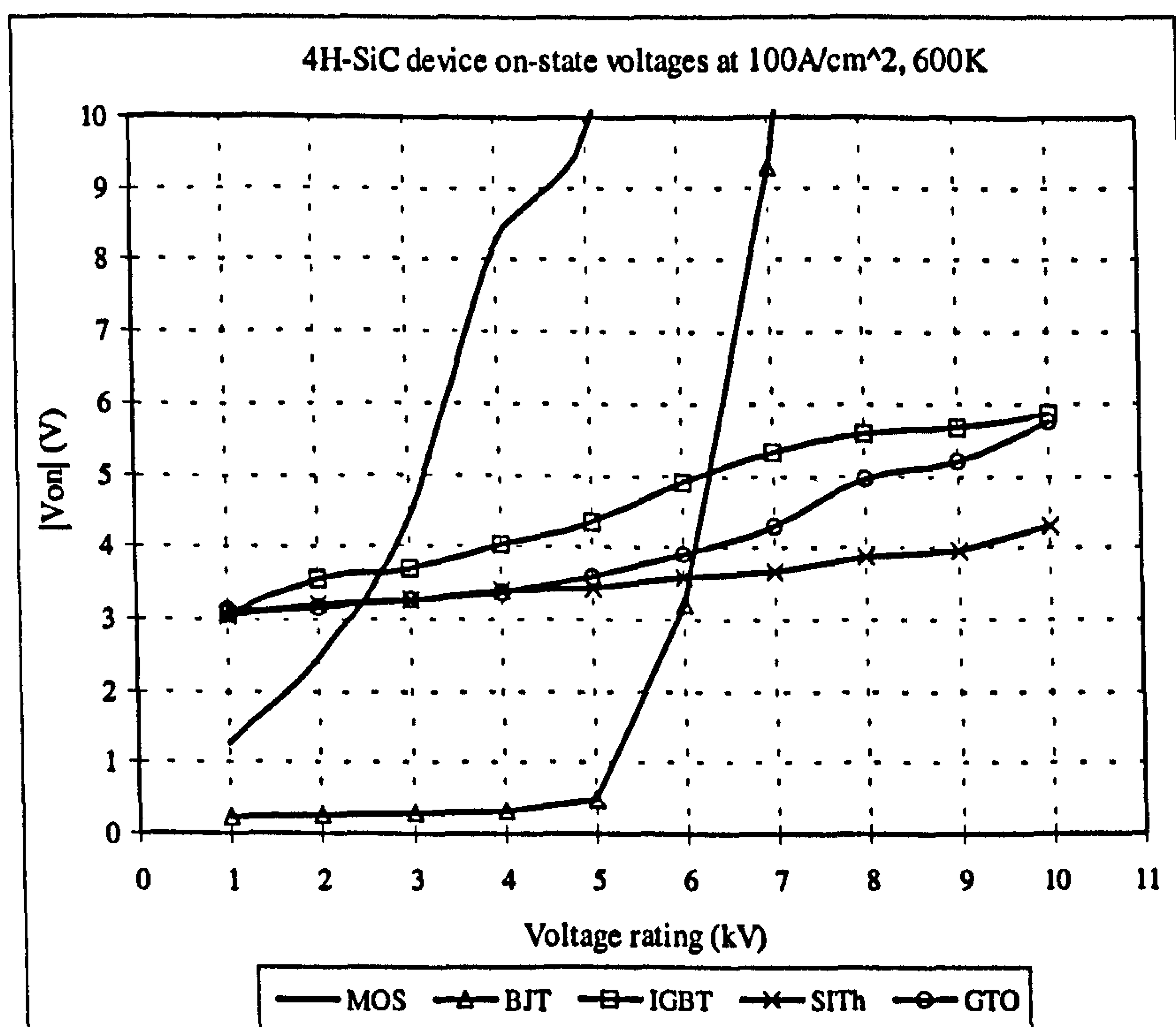

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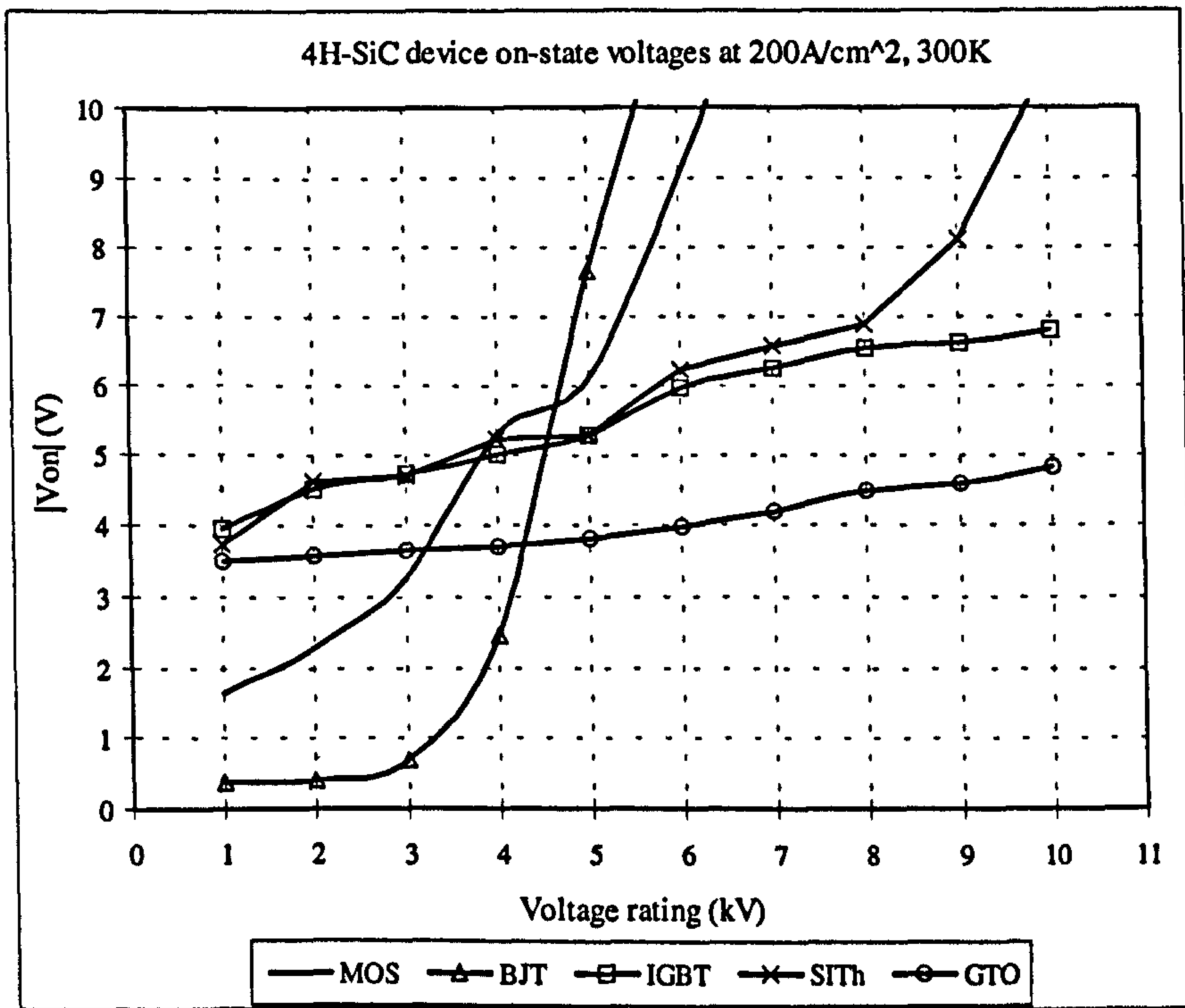

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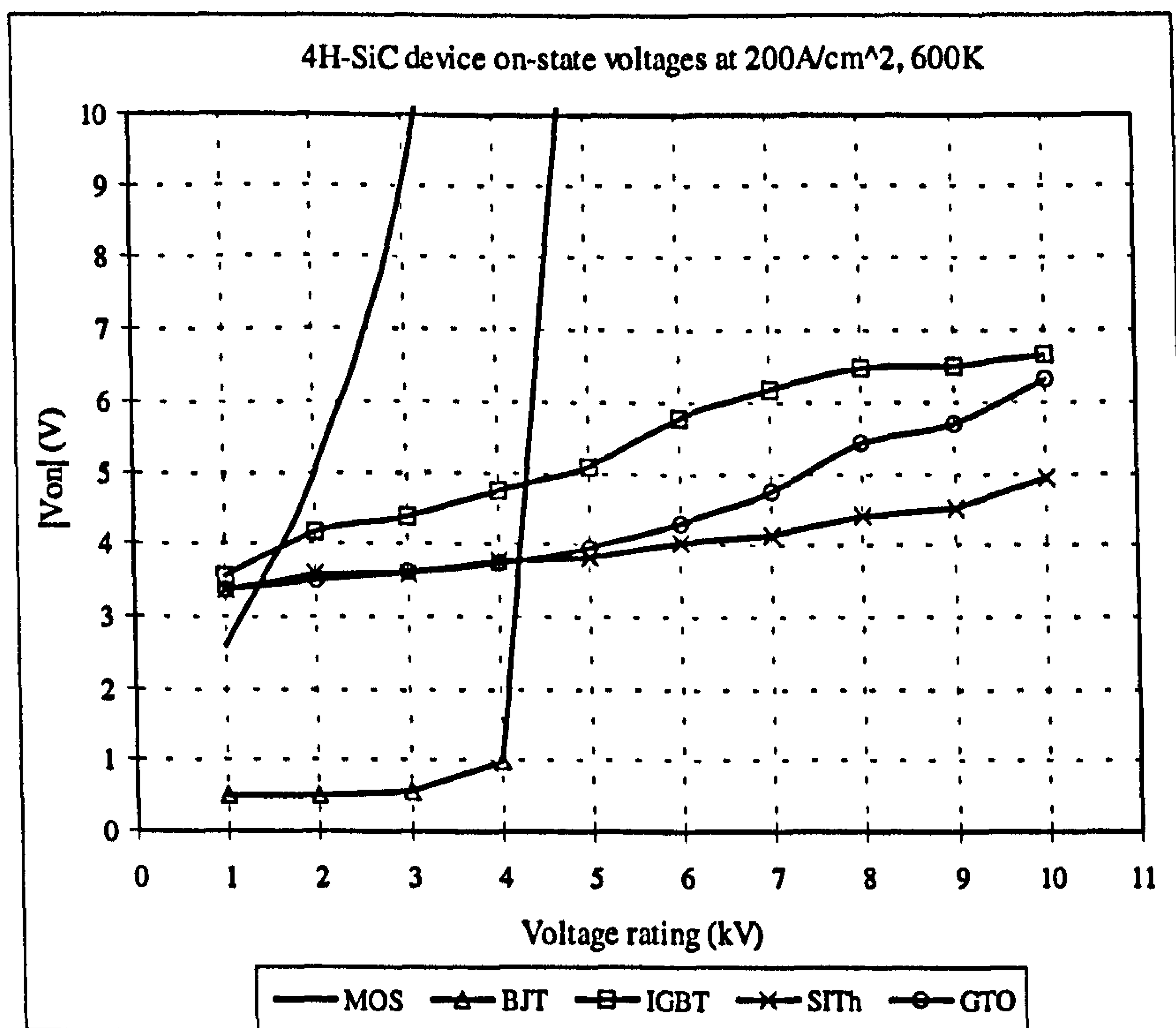

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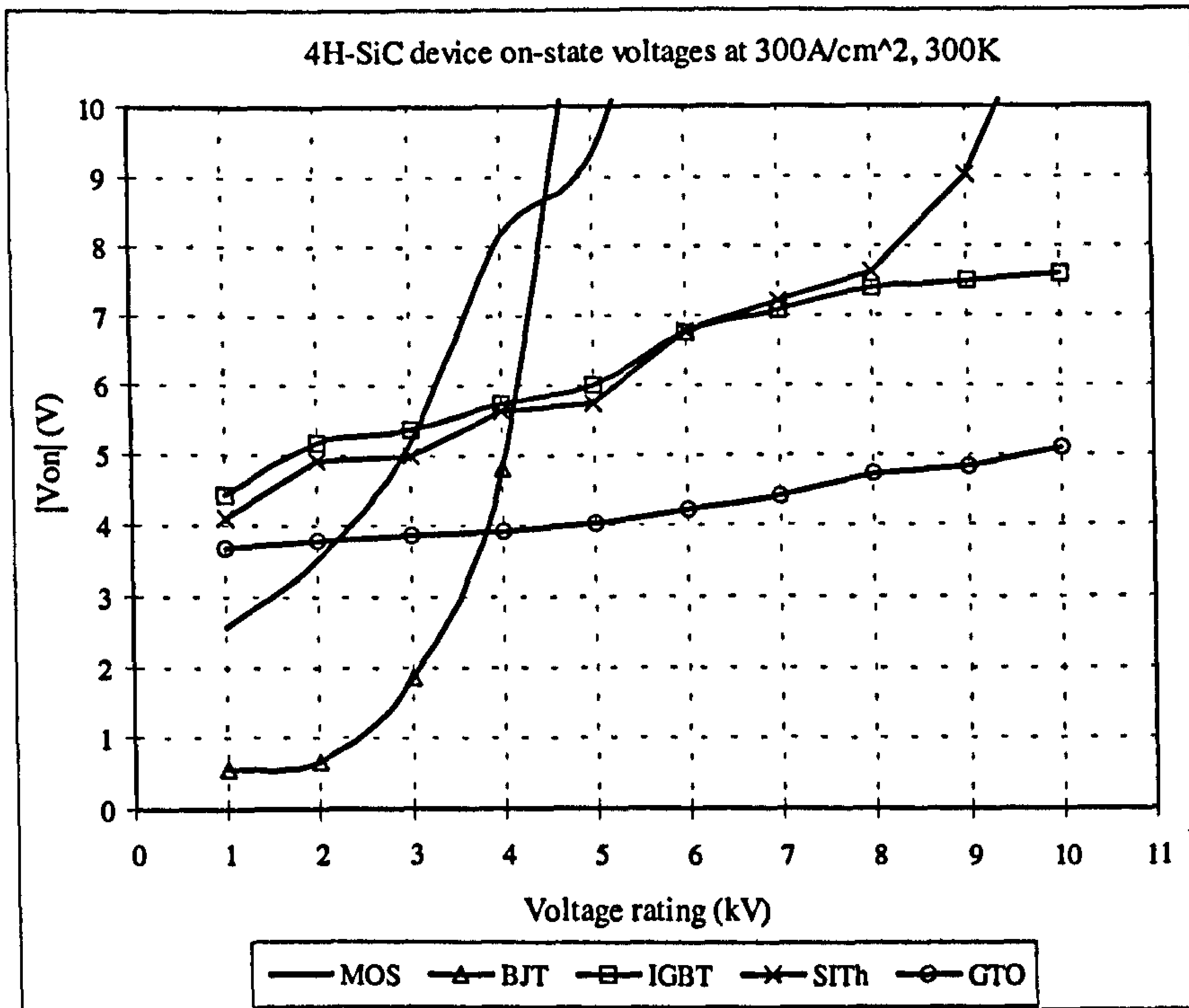

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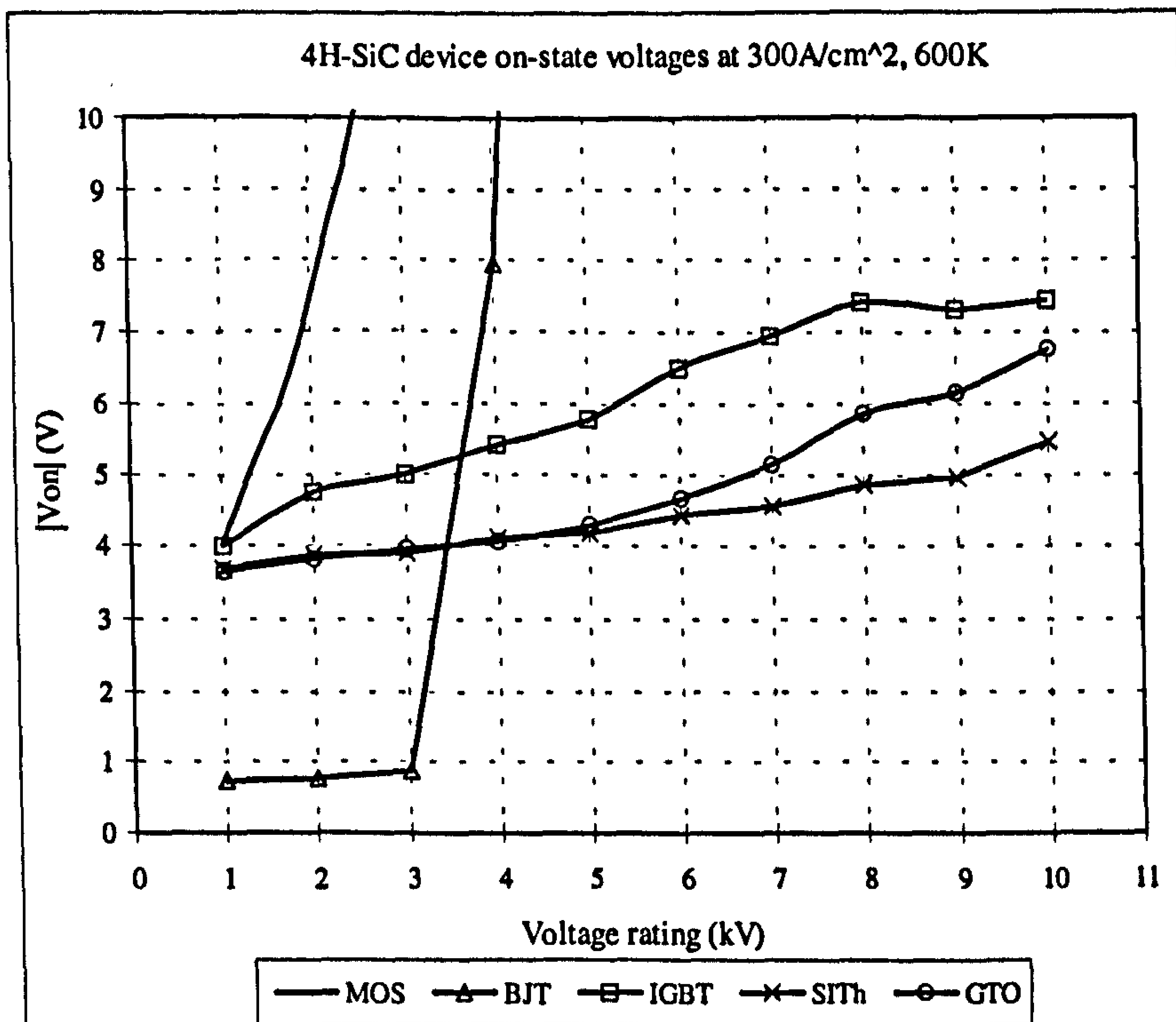


(f)

Figure 7.3 4H-SiC device on-state voltages at (a) $100A/cm^2$, 300K; (b) $100A/cm^2$, 600K; (c) $200A/cm^2$, 300K; (d) $200A/cm^2$, 600K; (e) $300A/cm^2$, 300K and (f) $300A/cm^2$, 600K

SiC MOSFETs:

When simulating 4H-SiC MOSFET characteristics, the average inversion layer electron mobility is set as 100 cm^2/Vs with V_{gs}=15V and V_{ds}=0.1V.

For IGBTs, SIThs and GTOs, the 4H-SiC 2.7 V built-in junction voltage must be exceeded before a substantial current can flow. Hence the forward conducting characteristics of these devices with voltage ratings of less than 5 kV are not as favourable as those of SiC MOSFETs and BJTs. Although the voltage drop of these devices at high current densities is lower, applications with a current density higher than 300 A/cm^2 are not practical due to thermal limitations. However, being majority carrier devices, the current handling ability of MOSFETs has strong negative voltage rating and temperature coefficients. Biased at 3 V and at room temperature, the 1 kV and 10 kV SiC MOSFETs can handle on-state current densities of 346.7 A/cm^2 and 18.2 A/cm^2 respectively. Elevating the temperature to 600 K, these current densities drop to 228 A/cm^2 and 4.9 A/cm^2 respectively. It is worth pointing out that practically, power device operating junction temperatures are above 400 K. Therefore, above 2 kV, the current handling ability of SiC MOSFETs can not compete with SiC bipolar devices.

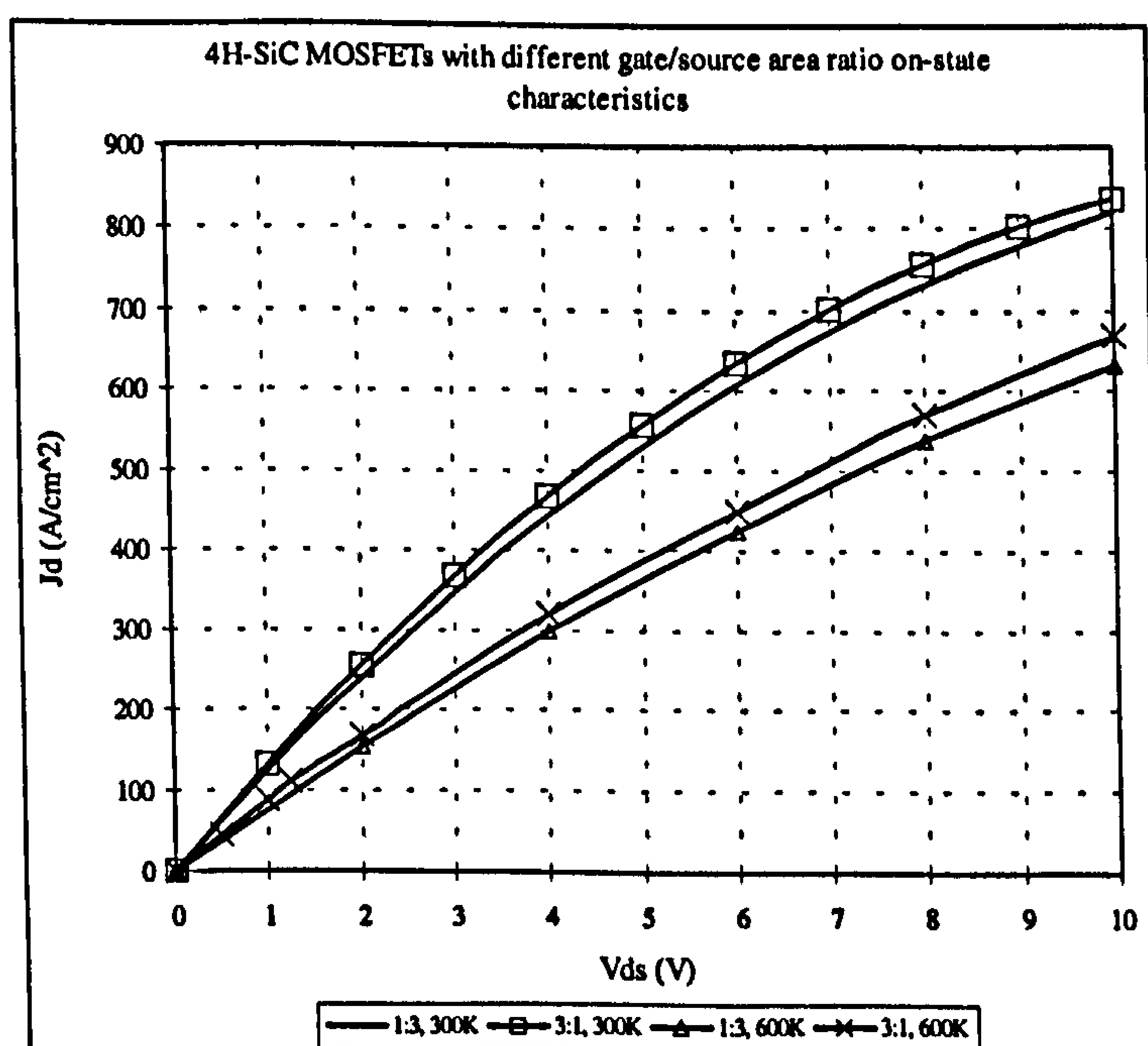


Figure 7.4 4H-SiC MOSFET on-state characteristics with different gate/source area ratio

To investigate gate/source area ratio influence on SiC MOSFET performance, the on-state characteristics of 1 kV SiC UMOSFETs with gate/source area ratios of 1:3 and 3:1 are simulated (Figure 7.4). Obviously, the 4H-SiC MOSFET channel and drift region on-state resistances dominant device on-state resistance, even for a voltage rating of 1 kV, which results in negligible gate/source area ratio effect on device current handling ability.

SiC BJTs:

The conductivity modulation of BJTs in conjuction with the offset of the two back-to-back P-N junction voltages in BJTs, generate lower on-state voltages than other devices when operating in the saturation region, that is, where both the collector and emitter junctions are forward biased. Unfortunately, SiC BJTs have the same problem as Si BJTs, viz., the severe degradation of the current gain with increasing voltage rating. This means BJTs with voltage ratings higher than 4 kV are not viable, assuming a current gain lower than 10 is unacceptable. Beyond 5 kV, BJT on-state voltages increase rapidly with voltage rating. As shown in Fig. 7.2 (e), a base current of 20 A is required for a 10 kV BJT with a collector current of 30 A at room temperature; that is β=1.5 for V_{ce}=3.3 V.

In the voltage range 1 kV to 5 kV, SiC BJTs exhibit better current handling ability than the corresponding SiC MOSFETs. Additionally, their on-state characteristic temperature dependence is not as strong as SiC MOSFETs. As mentioned in Chapter 5, the development of SiC MOSFETs is hampered by gate oxide reliability and low inversion layer mobility. Therefore, the BJT is a promising SiC device to evolve in the near future. The advantages of SiC MOSFETs are ease of operation, wide SOA, lack of second breakdown, and simpler and cheaper gate drive circuitry [7.20]. In the long term, whether SiC MOSFETs or BJTs dominate the application range 1 kV to 4 kV depends on developments in specific device technologies.

SiC IGBTs:

The switching performance of IGBTs is more sensitive to change of carrier lifetime than BJTs. To obtain a good trade-off between conduction and switching performance, IGBT carrier lifetime is varied with voltage rating. τ_0 is 400 ns for 1 kV to 4 kV IGBTs, 600 ns for 5 kV and 6 kV IGBTs, 800 ns for 7 kV and 8 kV IGBTs and 1 μs for 9 kV and 10 kV IGBTs.

The current handling ability of SiC IGBTs is not hampered by voltage rating and temperature as severely as with MOSFETs and BJTs. With a forward current density of 200 A/cm^2, the forward voltages of a 1 kV IGBT and a 10 kV IGBT are 3.96V and 6.83 V at 300 K, and 3.56 V and 6.66 V at 600 K respectively. At typical operating current densities, the IGBT on-state voltages at 300K are slightly higher than at 600K. Several factors influence IGBT conduction ability temperature dependence. The diode component of the voltage drop has a temperature coefficient that is negative at low current density, becoming positive at high current levels. The MOS component has a positive temperature coefficient. As mentioned in Chapter 6, the relative high dopant ionization energies in SiC introduce a degraded injection efficiency at room temperature. The enhanced substrate dopant degree of ionization at higher temperature, hence improved injection efficiency, is the primary reason accounting for the lower on-state voltages at higher temperature. Compared with SiC SIThs, IGBT on-state voltage temperature dependence is relatively small.

Above 4 kV, SiC IGBTs, SIThs and GTOs exhibit better current handling ability than SiC BJTs and MOSFETs. Although in the voltage range simulated, the current handling ability of SiC IGBTs is not as attractive as the other two device types, IGBTs possess advantages such as ease of use, wide SOA, faster switching speed, excellent gate turn off ability and smaller conduction characteristic temperature dependence than SIThs

and GTOs. As will be shown in the following sections, high voltage SiC GTOs and SIThs exhibit some unfavourable application features.

SiC SIThs:

As with IGBTs, carrier lifetime increases from 200 ns to 1 μs with the voltage rating to get a good trade-off between on-state characteristics and switching performance. Considering the higher degree of ionization of donors than acceptors in SiC, the SIThs investigated have a complementary structure (with an N^+ substrate) to the usual Si SIThs (with a P^+ substrate). The P^- drift region doping is set as 1×10^{14} cm^{-3} and the width is varied with voltage rating to support the required blocking voltage.

SIThs behave essentially like a P-i-N diode when the gate is open circuited or reverse biased (for SIThs with an N^+ substrate) or forward biased (for SIThs with a P^+ substrate) with respect to the cathode. But their current handling ability is degraded by the narrowed current path near the gate region due to the presence of the gate grids. As pointed out in Chapter 3, the substrate ohmic resistance is an important current-limiting factor in SiC PiN diodes. This also applies to SiC SIThs with a relatively low voltage rating. However, as voltage rating increases, the drift region voltage drop dominates, hence the anode injection efficiency, drift region doping and width have significant impact on device conduction characteristics. The device on-state characteristics at 300 K degrade more rapidly with voltage rating than at 600 K. In Figure 7.3, from 1 kV to 10 kV, the on-state voltage at 100 A/cm^2 increases from 3.63 V to 8.36 V at 300 K while at 600 K the on-state voltage increases from 3.06 V to 4.29 V. The latter results are mainly caused by the improved donor degree of ionization in the substrate, hence the improved anode injection efficiency at higher temperature. The device on-state voltages at typical operating current densities have a negative temperature dependence, which is large for devices with a

relatively high voltage rating.

As shown in Figure 7.2, generally SIThs have better conduction capability than IGBTs. At 600 K, their current handling ability is similar to or even better than the corresponding SiC GTOs.

SiC GTOs:

The carrier lifetime is 3 μs at 300 K and 1 μs at 600 K when simulating SiC GTO characteristics. The coupling of the "two internal transistors" via their common collector junction produces a self-sustaining condition that leads to current flow with a low on-state voltage. The self-sustaining operation is possible only when the sum of the common base current gains of the two transistors exceeds unity. The current level below which the device is unable to self-sustain current conduction is referred to as the holding current [7.20]. With a carrier lifetime of 1 μs, the GTO holding current densities at room temperature are much higher than the typical operating current densities, making this lifetime level unsuitable at 300 K. As shown in Figure 7.5, the holding current density of a 10 kV SiC GTO with a lifetime of 1 μs is 1040 A/cm^2, which is not a realistic operating current density. The holding current density decreases with voltage rating, but even with a 2 kV GTO, a holding current density of 303 A/cm^2 is observed. As plotted in the same figure, increasing the carrier lifetime to 3 μs at room temperature will solve the problem. Unfortunately, SiC GTOs with a 3 μs carrier lifetime can not be turned off at 600 K, even if the on-state current density is reduced to a low level. Therefore, the carrier lifetime is set as 3 μs at room temperature and 1 μs at 600 K respectively. This device is not for practical use.

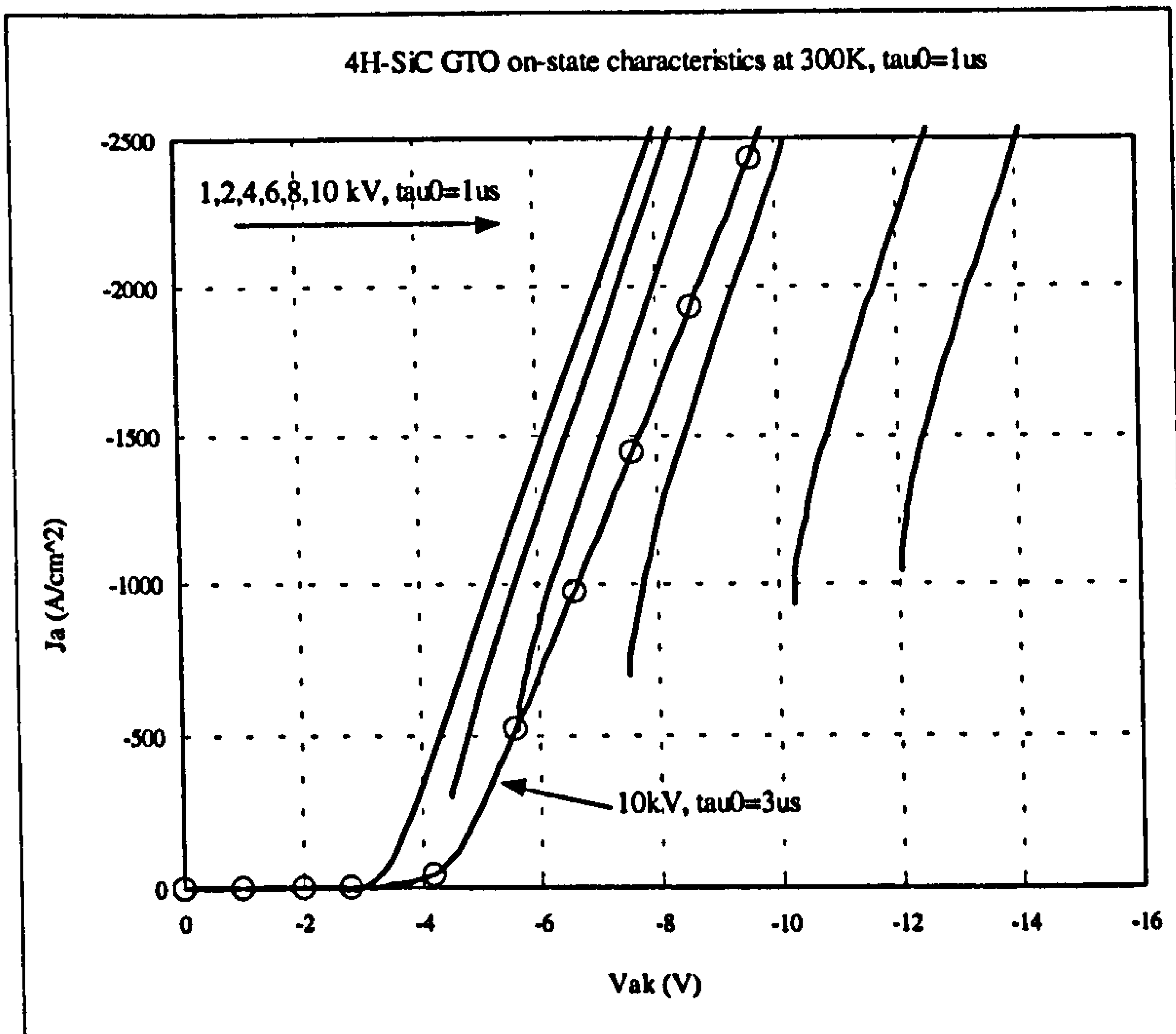


Figure 7.5 4H-SiC GTOs on-state characteristics at 300 K

In the voltage range simulated, SiC GTOs have comparable current handling ability to IGBTs and SITh s.

7.3 Thermal Consideration

In practical use, the current handling ability of a device is limited by the maximum permissible power loss $P_{D,max}$ at a specific junction temperature. If the cooling rate is inadequate to accommodate the junction temperature rise, then thermal runaway occurs. The temperature rise of a junction above ambient temperature is given by:

$$\Delta T = T_j - T_a = (T_j - T_c) + (T_c - T_a) = R_{th,jc} P_D + R_{th,ca} P_D \tag{7.1}$$

$R_{th,ca}$ is determined by the heat conduction method used, thus $R_{th,jc}$ and ΔT_{jc} are utilized to calculate the maximum power loss per unit area of the device:

$$\frac{P_{D,max}}{A} = \frac{T_j - T_c}{R_{th,jc} A} = J_F V_F \tag{7.2}$$

To calculate the maximum continuous forward current density of SiC devices, the maximum permissible power loss must be first calculated using the above equation. The

main component of $R_{th,jc}$ is the thermal resistance from the bottom of the substrate to the case. This depends on the properties of the electrodes and packaging technology. Hence the junction to case thermal resistance per unit area for SiC is chosen as 0.3 Kcm^2/W; a typical value for two-side cooled Si thyristors. The junction temperature is taken as 600 K, which is feasible due to SiC's superior properties. In considering heatsink heat conduction ability, the case temperature is taken as 400 K. Hence the maximum power loss per unit device area at 600 K for SiC devices is 667 W/cm^2.

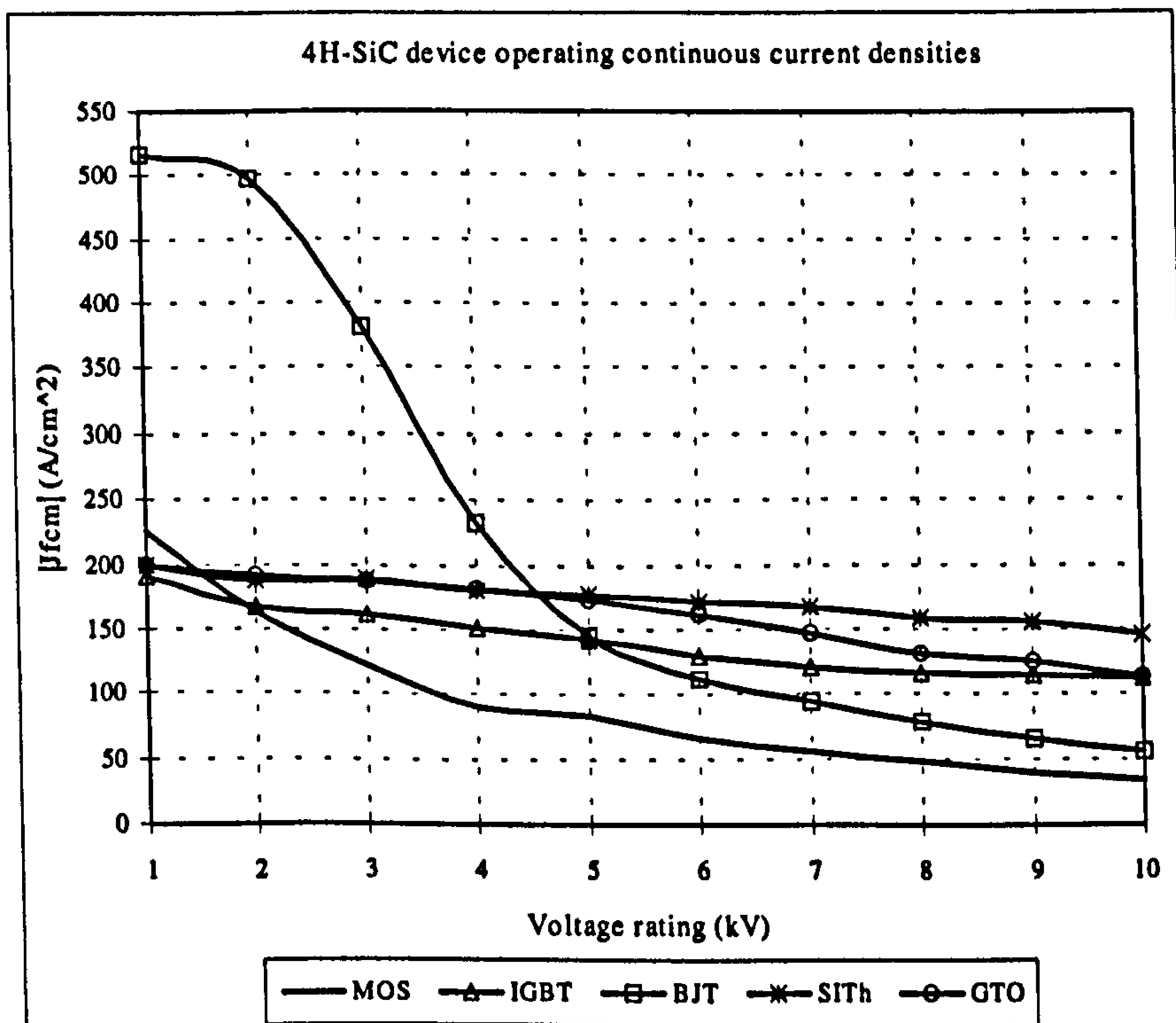


Figure 7.6 4H-SiC device maximum continuous operating current densities

Based on the above calculation, the maximum continuous forward current density J_{fcm} against voltage rating for SiC devices is obtained and plotted in Fig. 7.6. As shown, 1 kV and 2 kV SiC MOSFETs show a higher or comparable J_{fcm} to SiC bipolar devices. The maximum continuous operating current density of 1 kV to 4 kV SiC BJTs is higher than other devices (J_b=20A/cm^2). Although J_{fcm} of the 5 kV SiC BJT is slightly higher than that of the SiC IGBT, the low current gain (β=7.5) makes the BJT non-viable. At and

above 5 kV, SiC IGBTs, SIThs and GTOs are a better choice. Interestingly, SiC SIThs have a higher J_{fcm} than the corresponding SiC GTOs in this voltage range. But their large on-state characteristic variance with temperature at high voltage ratings will limit their practical use. J_{fcm} of SiC GTOs degrades with voltage rating more rapidly than SiC SIThs and IGBTs. As shown, the 10 kV SiC IGBT and GTO have the same value of J_{fcm}.

7.4 Switching Characteristics

The switching characteristics of SiC devices with a resistive load are simulated at 300 K and 600 K. The small current gain of BJTs with a voltage rating higher than 4 kV requires a base current comparable to the on-state current, which is unrealistic practically. Thus, only 1 to 5 kV BJTs are simulated. The applied blocking voltages are chosen as half of the device voltage rating and the on-state current is 1.2 kA. The device carrier lifetimes are the same as those used to investigate the on-state characteristics. The operating current densities are varied with voltage rating to obtain a reasonable on-state voltage drop and not to exceed the maximum permissible power loss $P_{D,max}$ at 600K (as derived in Section 7.3).

In Figures 7.7 and 7.8, the device turn-off times and switching losses versus voltage rating are plotted.

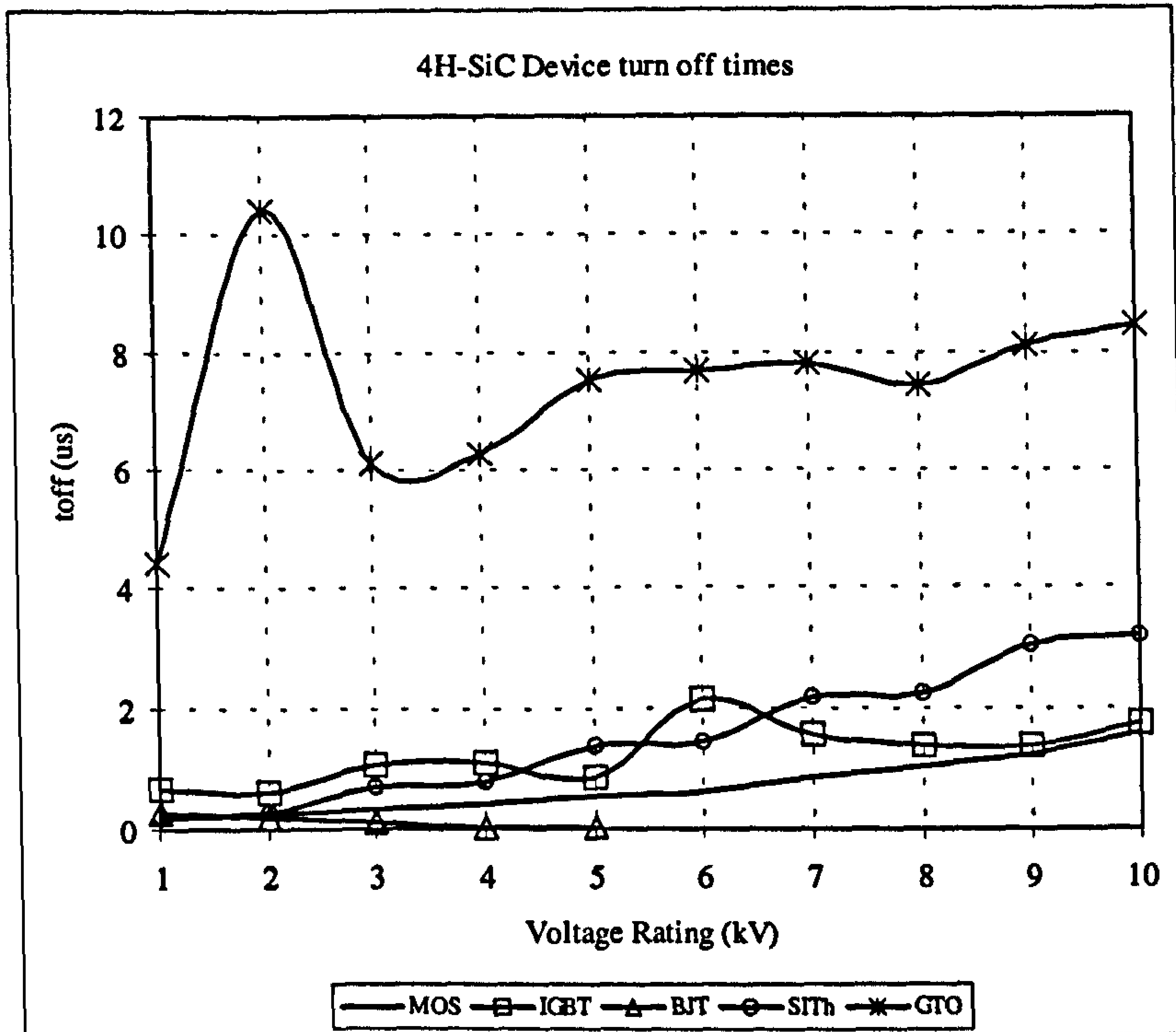
SiC MOSFETs:

The gate circuit voltage is changed from 0 V to 15 V when turning on MOSFETs and vice versa to turn-off. Being a unipolar device, MOSFET switching speed is only limited by capacitance charging or discharging times. Like current handling ability, the switching performance of SiC MOSFETs is also affected by voltage rating. To conduct the same drain current, a MOSFET with a high voltage rating must have a larger area than a low voltage MOSFET because of device conduction capability degradation with increased

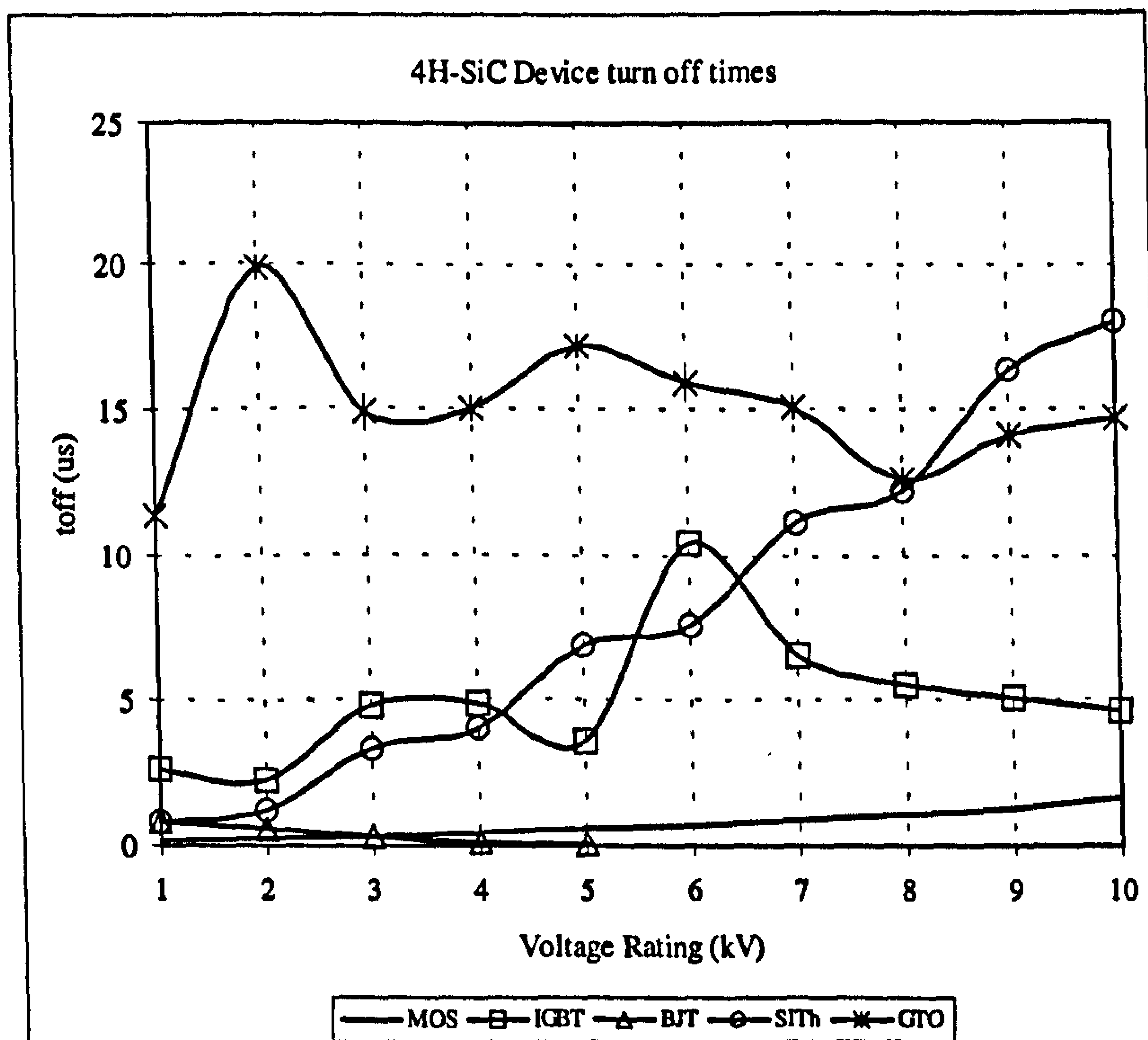
voltage rating. Hence, parasitic capacitances increase with voltage rating, inducing slower switching processes and higher switching losses. The MOSFET turn-on losses are higher than those of IGBTs from 4 kV at 300 K and 3 kV at 600 K respectively. As expected, the MOSFET turn-off times and losses are smaller than those of SiC GTOs, SIThs and IGBTs, especially at elevated temperatures. This is because a large amount of stored carriers must be evacuated from the drift region when turning off bipolar devices. Another beneficial feature of the MOSFET switching characteristics is constant switching speed, independent of temperature.

SiC BJTs:

To switch off power BJTs, a negative base current equal to the on-state base current is usually used. The current gain is varied from 100 for the 1 kV device to 7.5 for the 5 kV device. Of all the devices investigated, the SiC BJT has the smallest turn-off losses and fastest switching speed. This is because during the storage phase when the loss is negligible, the constant negative base current extracts a large amount of excess carriers until the minority carrier concentration in the N^- drift/P base junction reduces to zero. When the forward current begins to fall, few minority carriers remain in the drift region relative to the on-state. This phase completes quickly, resulting in negligible turn-off losses compared to other devices. The turn-on losses of SiC BJTs are also small because of the injection of excess carriers by the constant forward base current. Increasing BJT driving currents during switching reduces the losses and speeds up the switching processes.

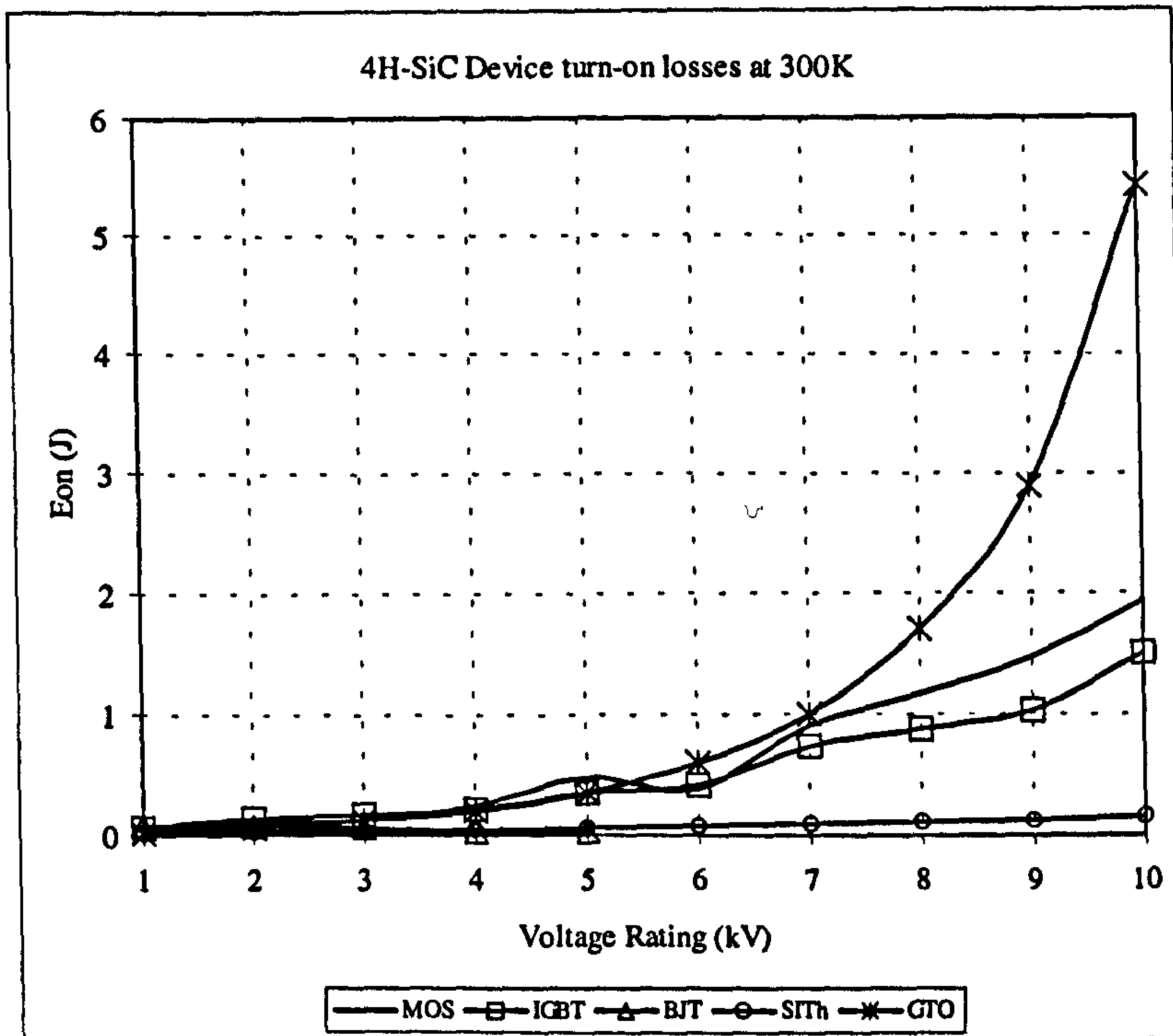


(a)

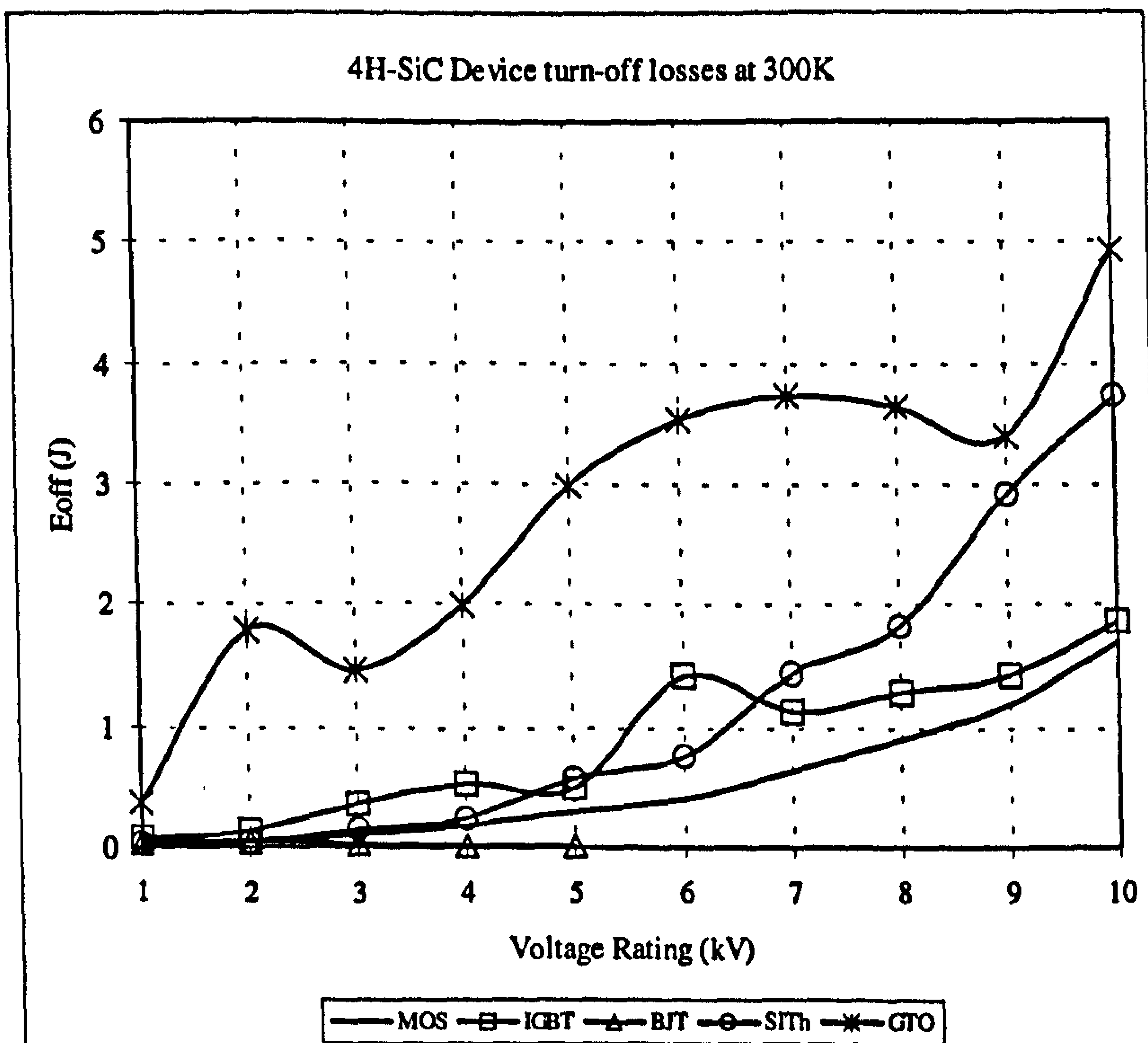


(b)

Figure 7.7. 4H-SiC device turn-off times at (a) 300 K and (b) 600 K



(a)



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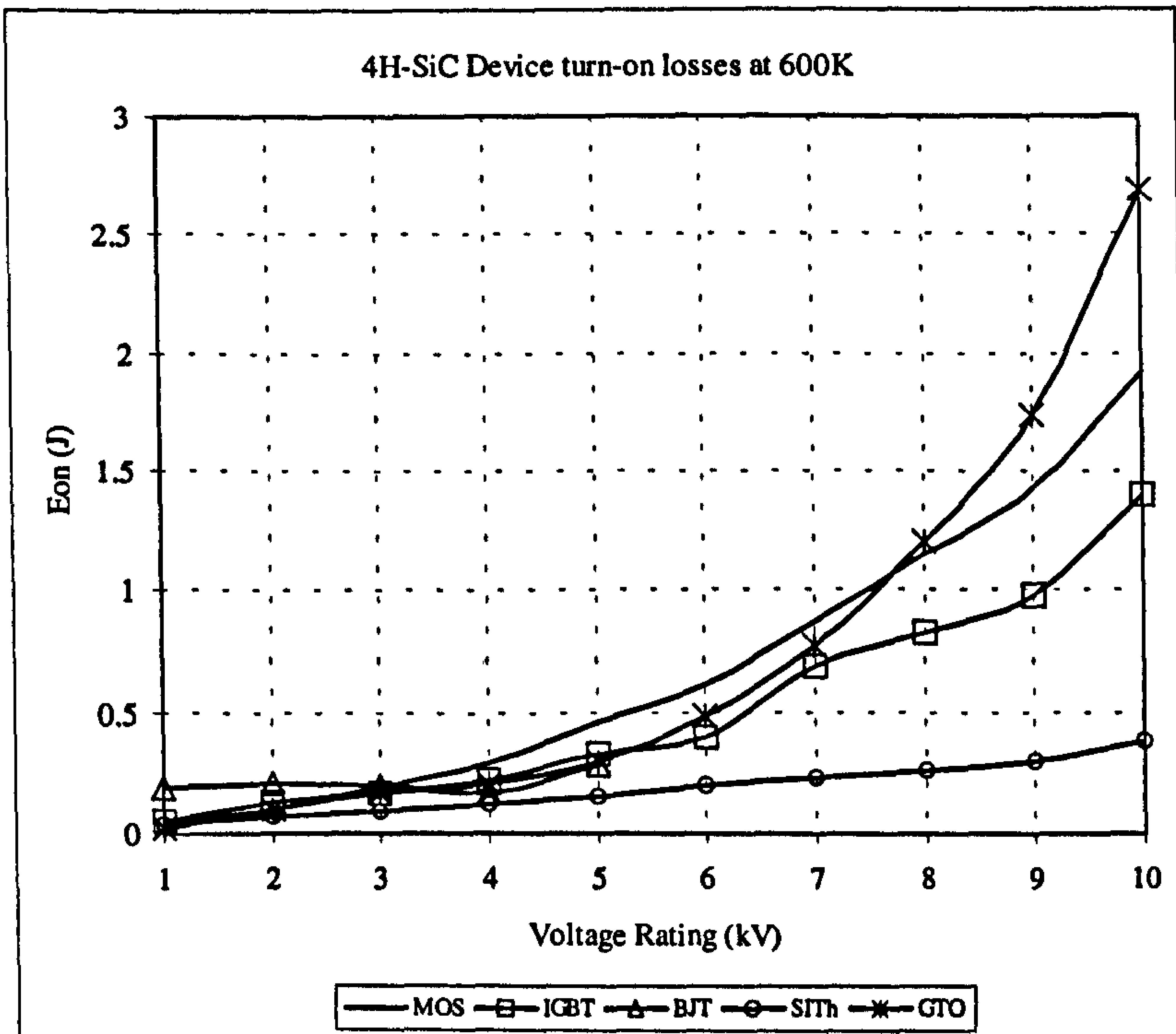

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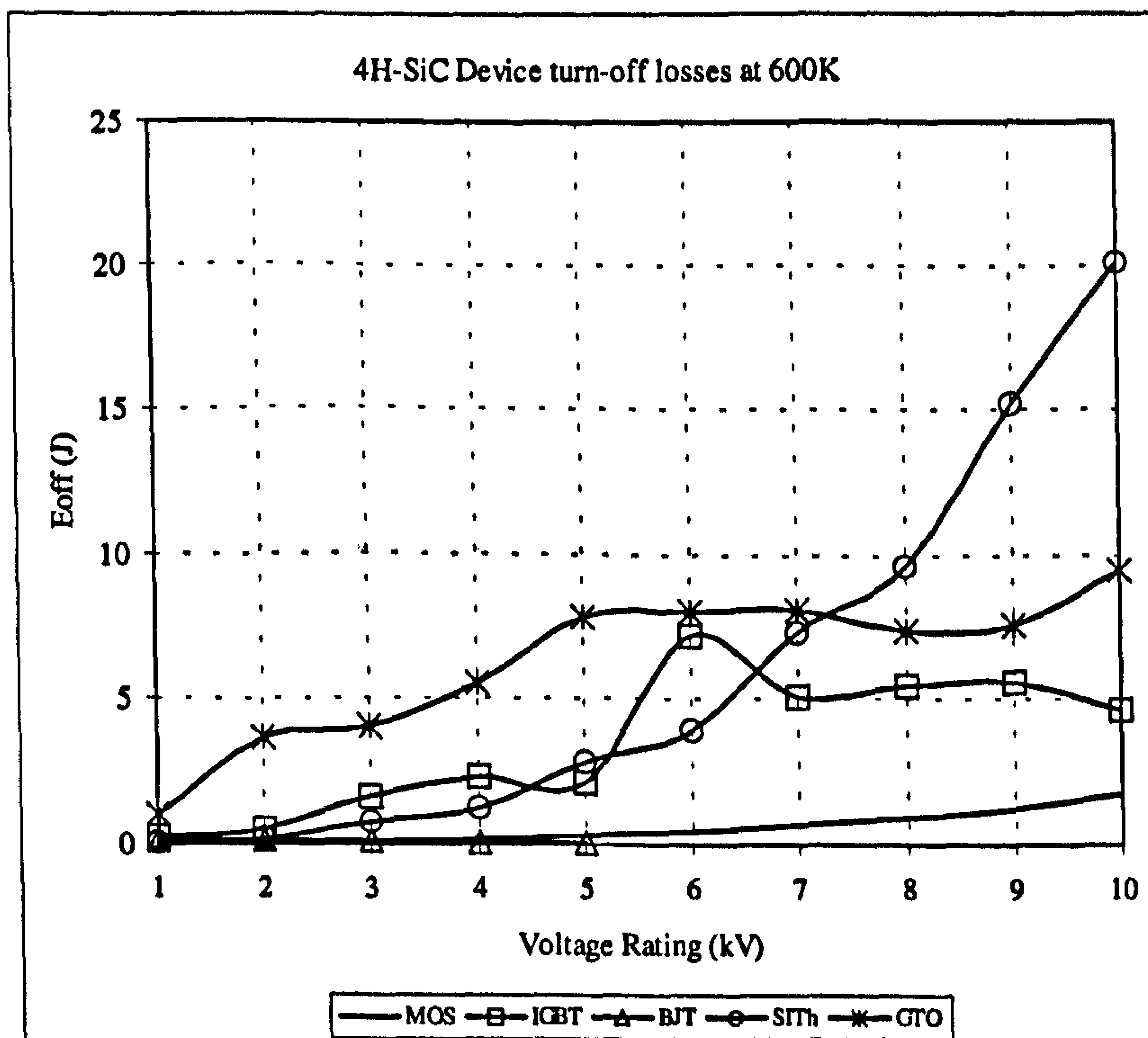

(d)

Figure 7.8 4H-SiC devices switching losses (a) E_{on}, 300 K; (b) E_{off}, 300 K; (c) E_{on}, 600 K and (d) E_{off}, 600 K

SiC IGBTs:

The gate circuit voltage is changed from 0 V to -15 V when turning on and vice versa during turn-off because the IGBTs simulated are P channel IGBTs. The switching losses do not increase with voltage rating monotonously. The IGBT switching losses depend on the drift region width, doping level, operating current densities, etc. The devices with higher voltage rating do not necessarily have higher switching losses since their operating current densities are smaller and the total excess carriers stored in the drift region may be less. Although the devices are designed as punch-through devices, in some cases, the depletion layer edge does not extend to the P^- drift/P buffer junction in turn-off, for the blocking voltage is chosen as half of the voltage rating. Therefore the devices turn off as non punch-through devices and exhibit a long current tail. Generally, SiC IGBTs exhibit better switching performance than SIThs and GTOs.

SiC SIThs:

Snubber circuits modify device V-I switching trajectories thereby keeping operation inside the SOA and reducing device switching losses. When switching Si SIThs, an RCD snubber is usually parallel connected with the device [7.10-7.12]. However, high-speed Si SIThs can be switched off snubberlessly [7.14-7.15]. SiC SIThs have comparable switching speeds to SiC IGBTs and can be turned off safely without the need of a snubber circuit. Hence, in this chapter, no snubber circuits are employed when simulating the switching characteristics of SiC SIThs. During SITh turn-off, significant gate current flows through the gate drive circuit. Parasitic wiring inductance between the gate drive supply and the SITh can not be ignored. To model this practical condition, parasitic inductance of 60 nH is added in the SITh gate drive circuit. To speed up SITh turn-on, a -3 V gate forward bias is applied. The gate drive resistance is 0.25 Ω.

The turn-off current gain, that is, the ratio of anode current to peak gate current, is a parameter used to measure SITh gate turn-off capability. However, due to the greatly enhanced injection efficiency at elevated temperature, the gate turn-off capability of SiC SIThs is very poor. It is found that only with a unity turn-off current gain can the devices be turned off. That is, to turn off a SITh with 1.2 kA anode current, a gate current of 1.2 kA is required. Obviously, this is not practical.

The SITh turn-on losses are the smallest of all the devices considered, but comparable to BJTs at room temperature. SITh turn-off losses are very sensitive to temperature and increase rapidly with increased temperature. At 600 K, above 7 kV ratings, the SITh turn-off losses are much higher than those of GTOs. Compared with IGBTs, their switching performance is poorer.

SiC GTOs:

An RCD snubber circuit is added when simulating GTO switching characteristics. Gate drive voltage sources of 15 V and -15 V are used during the on-state and blocking respectively. Once the GTO is triggered on, there is no need to use gate current. However the existence of the gate current can decrease the on-state voltage. In addition, continuous gate current has the advantage of maintaining the on-state since the latch-on and hold-on currents of GTOs are relatively high. The value of the gate series inductance is varied to control the switching speed. During turn-off, V_{gk} will exceed the applied reverse gate bias due to the presence of gate inductance. A clamp circuit is used to prevent V_{gk} from exceeding -25 V.

Generally the switching speed of GTOs is the slowest amongst the devices simulated. Note that GTO turn-off time ends when the anode current falls to 5% of I_{on}. Actually, it may take much longer for the anode voltage to reach the DC link voltage after

the anode current disappears due to the existence of the snubber. The snubber circuit greatly reduces switching energy dissipated in GTOs. In Figure 7.8, 8 to 10 kV GTOs have smaller switching losses than SIThs at 600 K, but when snubber losses are included, total losses are larger. The snubber values are C=0.44μF and R=5Ω.

7.5 Conclusion and Discussion

In this chapter, the electrical performance of SiC power switching devices has been investigated systematically by simulations. Below 5 kV, SiC MOSFETs and BJTs show better current handling ability than other devices. The current handling ability of the SiC MOSFET is greatly hampered by increased voltage rating and temperature. The degradation of SiC BJT current gain at voltage ratings higher than 4 kV makes it generally unsuitable for high current, high temperature applications because of the need to supply a large continuous base current during the on-state. For these reasons, at voltage ratings higher than 4 kV, SiC IGBTs, SIThs and GTOs are a better choice because of their excellent current handling ability and reasonable switching speed. These devices all have comparable current handling in this high voltage range.

In the voltage range 1 kV to 4 kV, SiC BJTs show better current handling ability and switching performance than the corresponding SiC MOSFETs. This is also verified in Chapter 5. The SiC BJT is a promising candidate to demonstrate the strength of SiC devices in the near future. However, the advantages of MOSFETs, such as simpler and cheaper gate drive circuitry and ease of operation, make them attactive. In contemporary Si technologies, MOS based devices, such as MOSFETs and IGBTs, dominate the power semiconductor market. Although SiC MOSFET technology is hampered by problems such as insulator reliability and low inversion layer moblity, effort continues in the development of SiC MOS technology. In the long term, whether SiC MOSFETs dominate strongly

depends on device fabrication technologies.

Above 4 kV, SiC IGBTs are the best choice although their current handling ability is not as attractive as with SIThs and GTOs. This is because IGBTs have excellent switching characteristics and use simple drive circuitry. Most importantly, SiC IGBTs are easy to use and reliable. SiC SIThs show relatively high on-state voltages at room temperature and poor gate turn-off capability. At elevated temperatures the GTO can not be turned off and at room temperature the holding current is extremely high. These properties are in confilict with carrier lifetime requirements. Therefore, the SiC IGBT is preferred. However, the insulator reliability problem met with SiC MOS system will also hamper the performance of IGBTs.

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CHAPTER 8

ANALYTICAL MODELLING OF SEMICONDUCTOR DEVICES IN CIRCUIT SIMULATIONS

To simulate the behaviour of semiconductor devices, three types of device models are available, viz., physical models, equivalent circuit models and analytical models [8.1]. The Silvaco numerical simulator employed in previous chapters to investigate the performance of SiC devices utilizes physics based semiconductor models. Physical models are based on a description of carrier transport physics, provide a detailed insight into the physical aspects of device operation, and accurately predict device DC, transient and AC operation of devices. Their principal limitation is that they require substantial resources. Equivalent circuit models associate the electrical circuit elements to the device structure (for example, a depletion layer capacitance can be associated with a reverse-biased PN junction). The element value may be obtained by attempting to fit the model's terminal characteristics with measured data or by identifying the element's electrical behaviour with specific physical characteristics of the device structure. This type of model is easy to implement and is usually fast to evaluate. SPICE exclusively uses equivalent circuit models. The main disadvantage is that they are not as accurate as physical and analytical models and are not predictive in nature. Generalised solutions to the semiconductor equations are not available for most devices. Nevertheless, it is possible to obtain closed-form analytical models for a variety of devices, by making suitable approximations. This type of closed-form solution can produce a good representation of power device operation, which occurs at relatively low frequencies (<1MHz), where the field and carrier distributions can be considered as being essentially one-dimensional.

In recent years, research on power semiconductor device models for circuit simulation has intensified [8.2]. This stems from the demand to improve efficiency and reliability in the design and realization of power electronics circuits. A key element for achieving this is the availability of high-quality power device models for circuit simulations. As power circuits move to higher operating frequencies, the detailed switching characteristics of power devices become important, and it is necessary to employ computer-aided design (CAD) methodologies which accurately predict the functionality and reliability of a specific power circuit design. This again means high-quality semiconductor device models for circuit simulation are required.

A number of new power semiconductor device model concepts for trimming basic physical equations to the requirements of a power semiconductor device model for circuit simulation have been proposed [8.3-8.14]. The software industry recognises the need for better CAD tools and models for power semiconductor device modelling. Advances in on-going research are being implemented by software developers [8.2]. For example, the IGBT model proposed by Hefner has been incorporated into Microsim PSpice 8.0.

In this chapter, analytical Si PiN diode models proposed in [8.15-8.16] are modified, implemented and validated in PSpice. Integrated with the PSpice IGBT model as new IGBT module model, the simulation results accurately reflect the practical device performance. The Si power device models are extended to SiC. New challenges facing SiC device modelling are discussed.

Finally, a new unified voltage-controlled switch model is proposed for PSpice. It eliminates discontinuity of the PSpice switch resistance derivatives. Comparison with the PSpice switch verifies that this new model improves simulation speed and convergence.

8.1 Power PiN Diode Models

The actual switching processes in power rectifiers differ greatly from the processes predicted by low-level injection theory. A high voltage PiN structure operating in high level injection is usually assumed typical for most power diodes. During conduction, the drift region is flooded with excess carriers. When the diode is switched off, it takes time for the excess carriers to recombine and be extracted. This results in current and voltage overshoot [8.17-8.19], which must be considered when designing and analysing power circuits, for they cause high power losses and can destroy other circuit components. However, the diode model in PSpice is based on the basic charge control model and is unable to predict switching transients accurately [8.20]. Previously, many attempts have been made to incorporate a carrier diffusion equation solution into the Si power diode model used in circuit simulators [8.4], [8.15-8.16], [8.21-8.24].

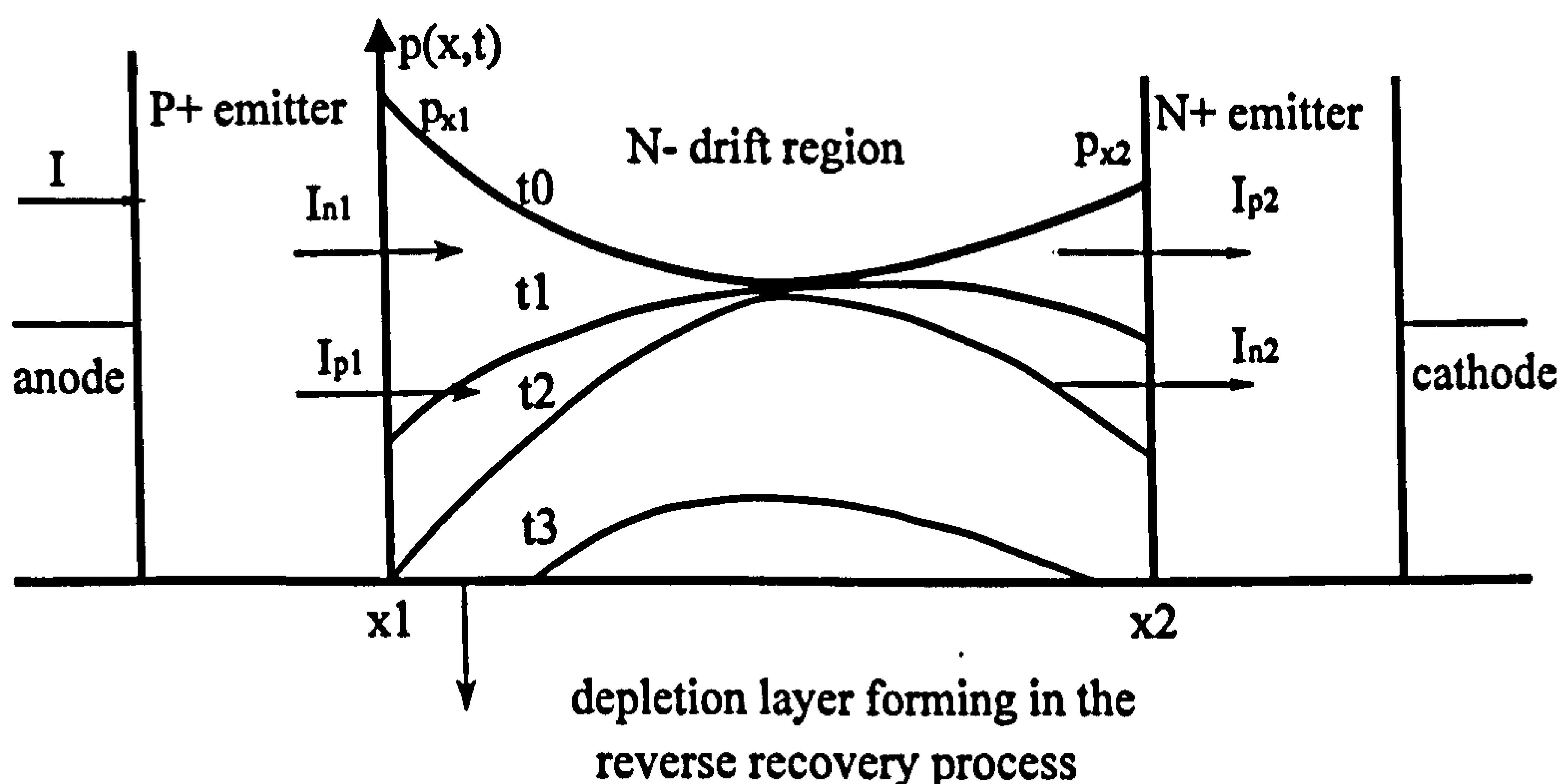
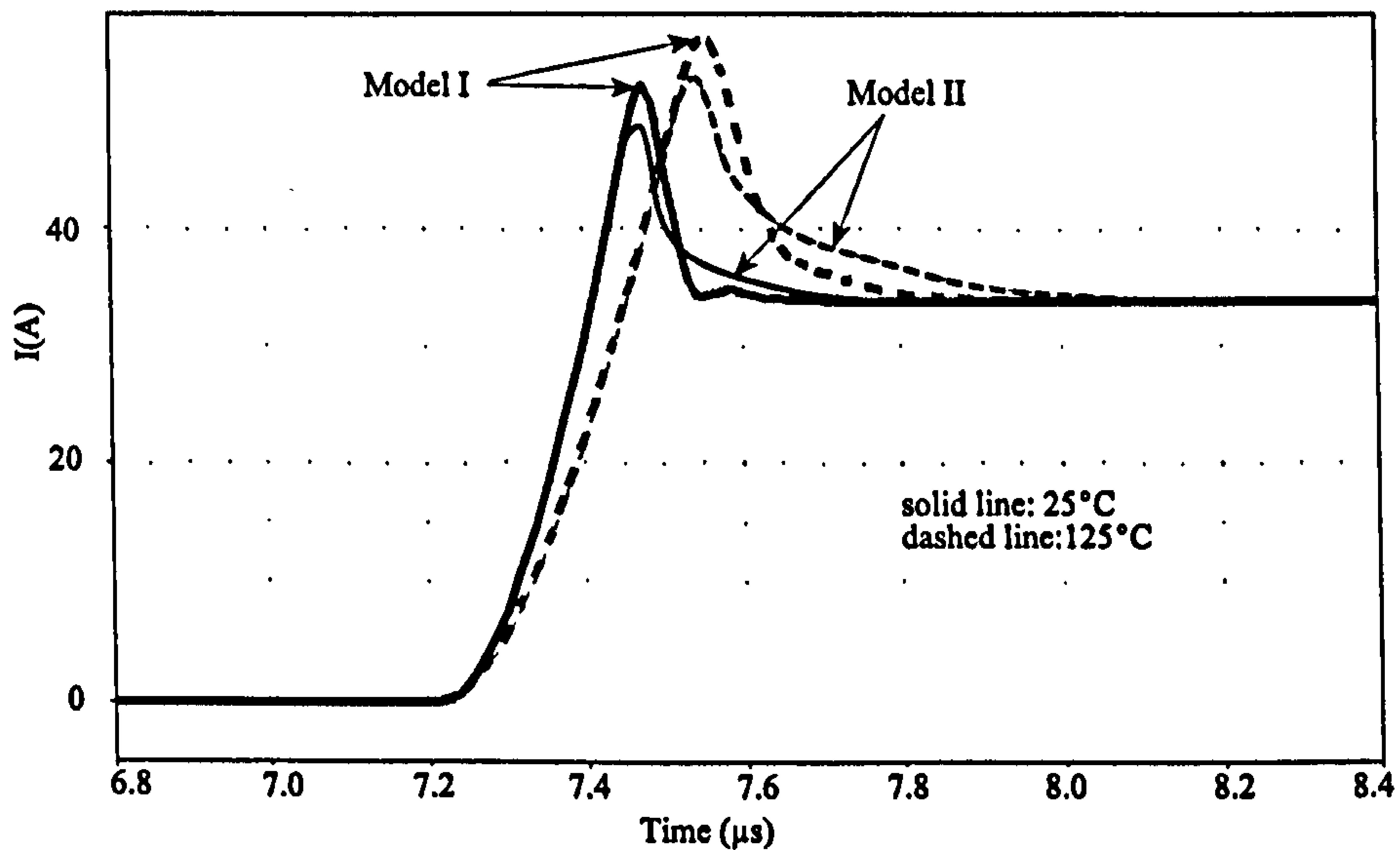


Figure 8.1 Diode structure and carrier distribution in the drift region during switching

As power diodes operate under high-level injection conditions, the steady-state carrier distribution in the drift region has the shape plotted in Figure 8.1. The asymmetry is caused by the inequality of the carrier mobilities. When the diode current reverses during diode reverse recovery, the carrier concentrations slopes at the ends of the drift region

change very quickly because these quantities are related to current density. The quasi-neutrality assumption holds true until the excess carrier concentration drops to zero at x_1, at which time the depletion layer starts to extend gradually from x_1 toward x_2, therein supporting junction reverse voltage. Eventually, all the excess carriers are swept out of the drift region or disappear via recombination.



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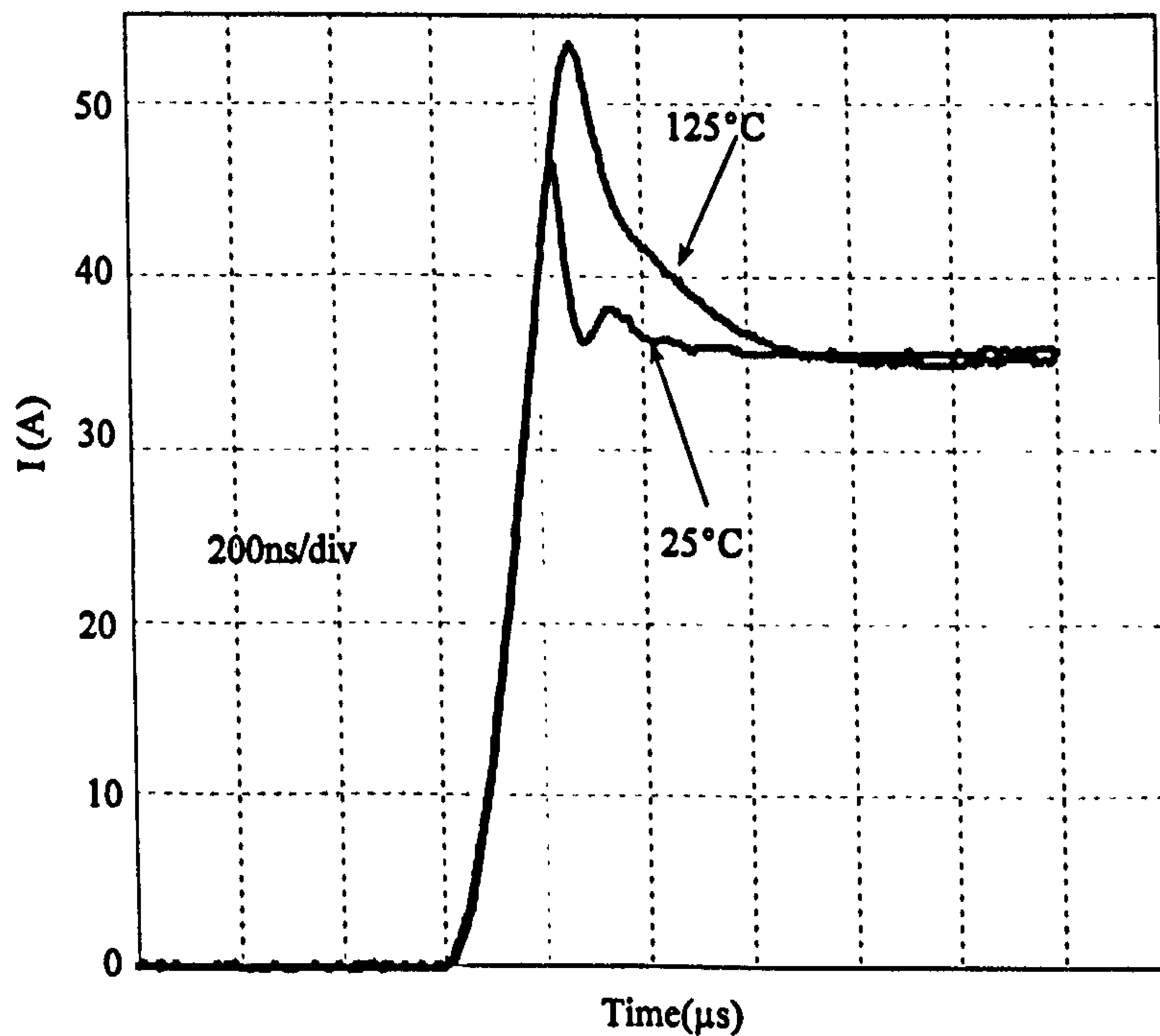


(b)

Figure 8.2 IGBT module turn-on current waveform (a) simulation (b) experimental

Two analytical PiN models obtained by approximating the Laplace transformation solution of the ambipolar diffusion equation [8.15-8.16] are implemented in PSpice for circuit simulations. Modifications are made to include the impact of temperature and doping on carrier mobilities, carrier lifetime and junction built-in voltages, and the effects of emitter doping on injection efficiency. The models are also extended to include reverse blocking characteristics. The complete diode subcircuit netlists are given in Appendix A.

Generally speaking, "Model I" reflects the distributed nature of the device and is more accurate. The carrier concentration at both ends and at the middle point of drift region are represented by node voltages which can be monitored during simulation. However, a switch is required in the model to change the circuit state when the carrier concentration p_{x1} reaches zero, that is, when the space charge layer starts to extend during turn-off or decrease during turn-on. The internal PSpice voltage-controlled switch model causes convergence problems. To solve it, a resistor whose value incorporates p_{x1} is used. This approach is simple and unified, but still may suffer from convergence problems.

"Model II" is derived by truncating the continued-fraction expression in the Laplace domain of the base region carrier distribution and representing the base region as a lumped RC network. It does not provide as much information as Model I, since accuracy is sacrificed for simplicity, reliability and simulation speed. From the circuit designers' viewpoint, Model II is preferred since accuracy is not meaningful when the solution does not converge, as is likely with Model I.

Figure 8.2 shows the PSpice simulation and experimental results of a 1200V, 35 A IGBT/diode module during snubberless turn-on with an inductive load at 300 K and 400 K. At turn-on, circuit behaviour is determined by the diode reverse recovery characteristic and IGBT gate drive conditions. Since the diode model is of primary concern, only turn-on

waveforms are shown. Diode reverse recovery peak current values for Model I are more accurate than for Model II, especially when accounting for temperature change. At room temperature, the shape of the current waveform and the current tail decay time of Model I are closer to the experimental results, than Model II. Model II gives more satisfactory results when elevating the temperature. The shape of Model II reverse recovery currents are all similar, being determined by the model structure and properties.

Figures 8.3 demonstrates the reaction of Model II to varied gate drive conditions for a 600V, 40A IGBT module. Reduction of di/dt and current overshoot with reduced gate drive voltage is modelled. As the gate drive voltage decreases, a significant increase in turn-on delay time and turn-on loss are predicted by the model.

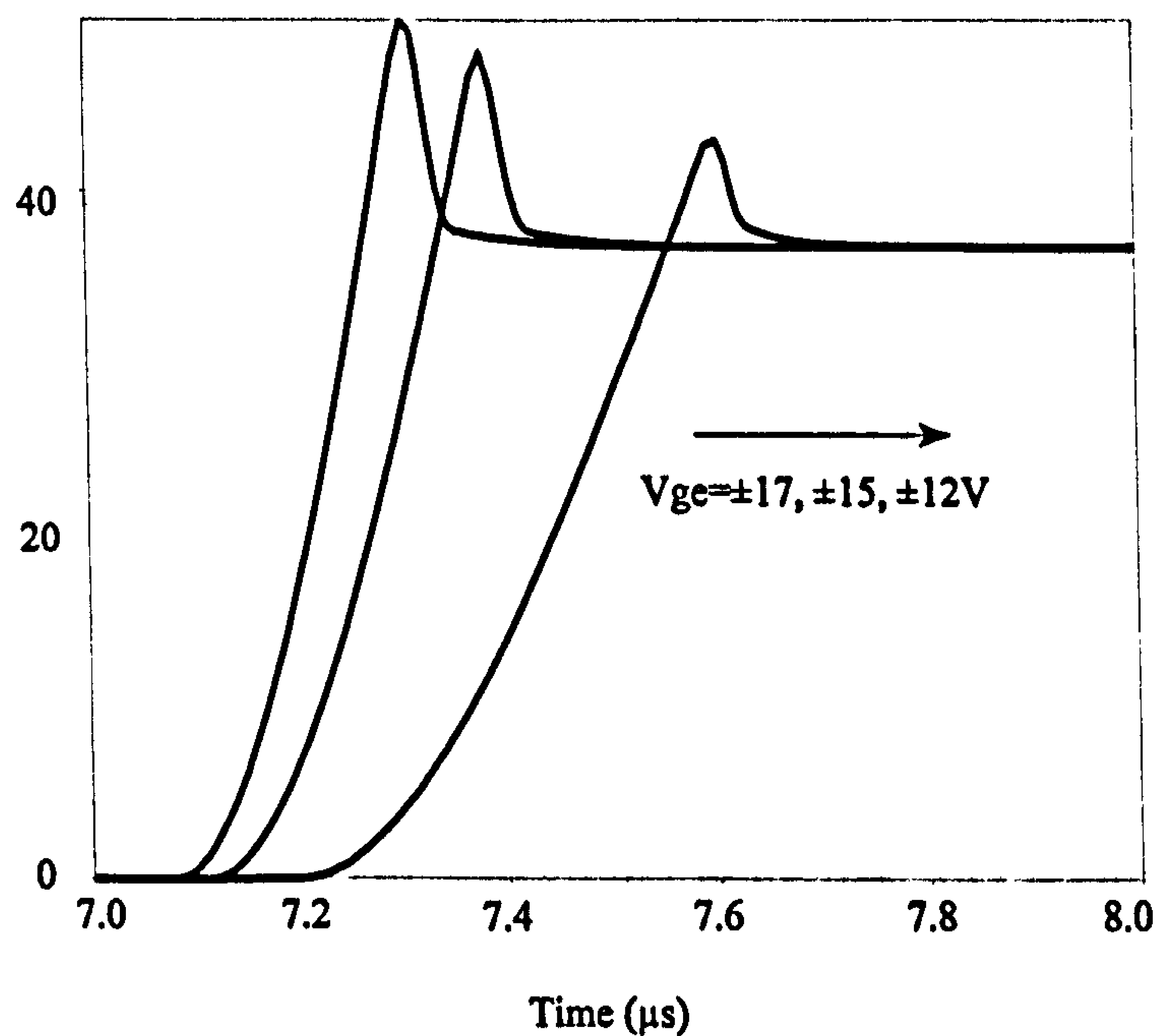
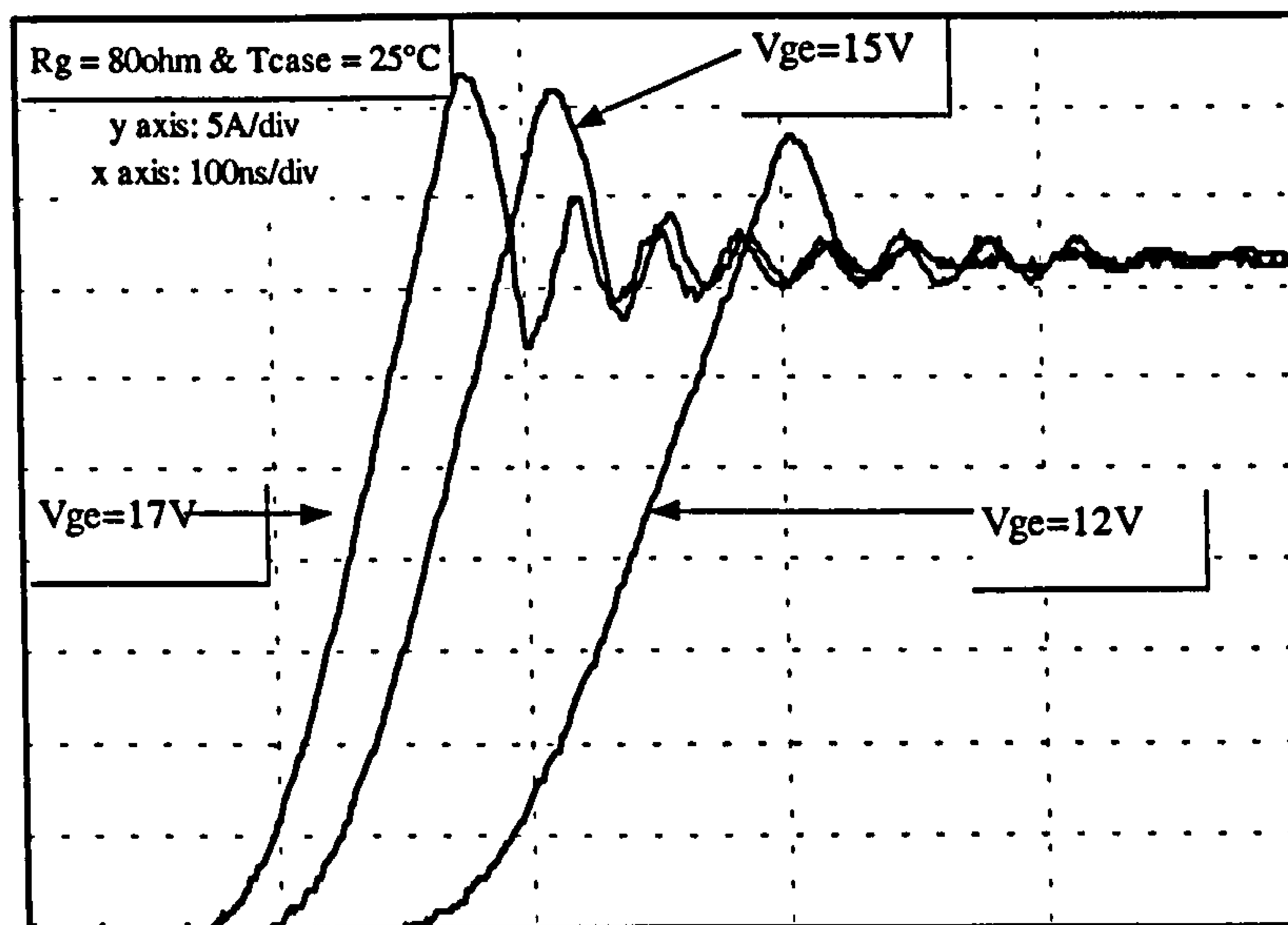


Figure 8.3 (a)



(b)

Figure 8.3 IGBT module turn-on current waveform with different gate drive voltages (a) simulation and (b) experimental

8.2 Power SiC PiN diode Model

With the development of SiC technologies, design and modelling of SiC devices commenced [8.25-8.26]. It is of importance to derive SiC device models for circuit simulations and CAD design. The analytical PiN diode model can also be applied to SiC by adjusting the appropriate material parameters. Model I is employed to implement the 6H-SiC PiN diode model in the circuit shown in Figure 8.4. In Figure 8.5, the simulation results of diode currents and voltages with different P^+ doping, inductance and temperature are presented and compared with numerical simulation results. The device is switched from a typical operating current density of 300A/cm^2 to a reverse block voltage of 600V. All results show good agreement.

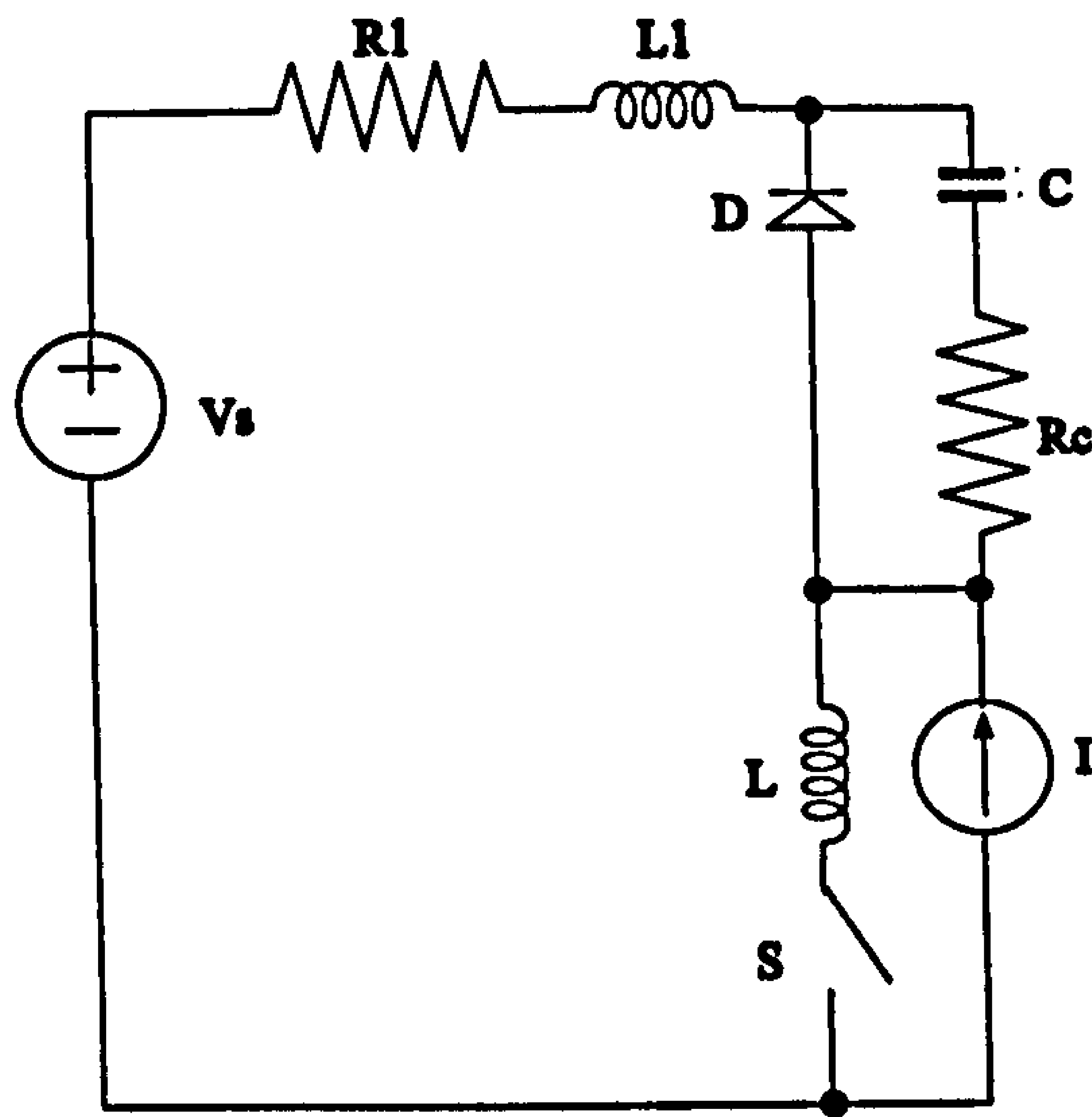


Figure 8.4 Test circuit of SiC PiN diode's switching performance

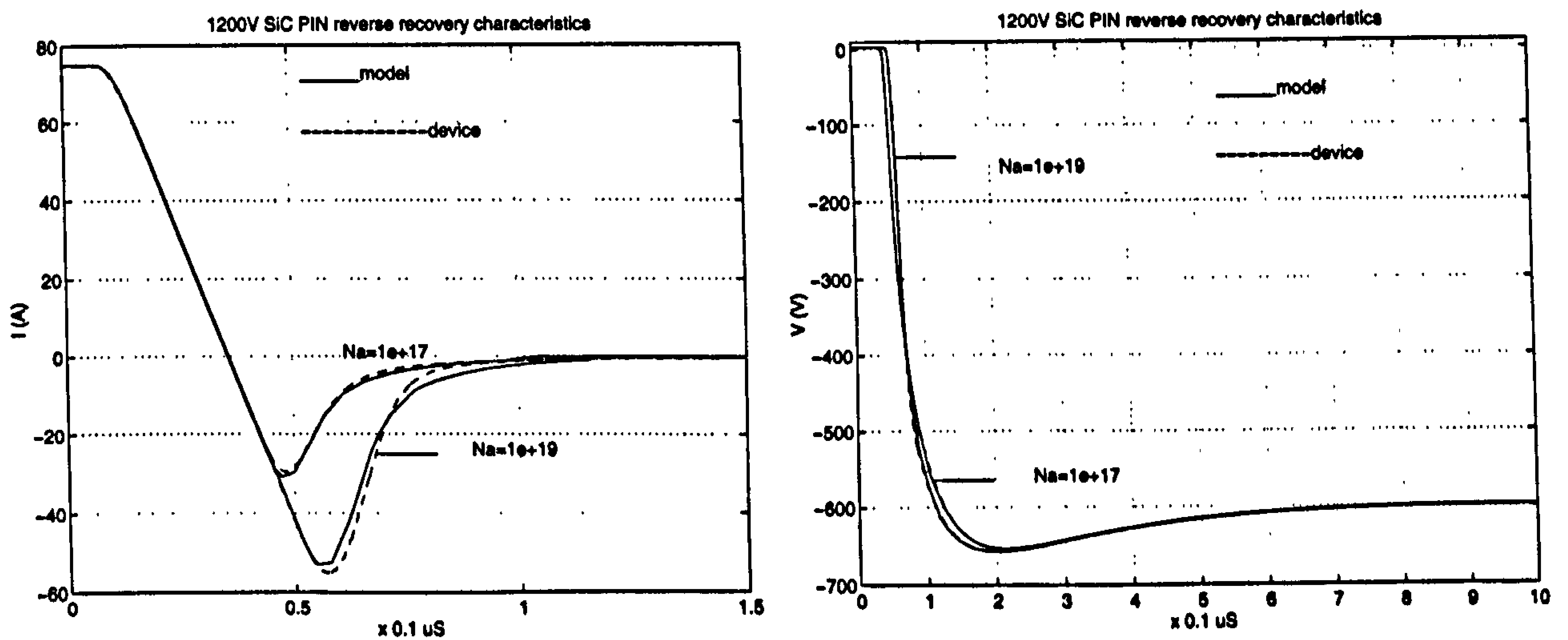


Figure 8.5 (a) $\tau_{n0}=\tau_{p0}=0.02\mu s$, di/dt=3000A/$\mu s$, T=300K

Although Si device models for circuit simulations can be used for SiC by simply changing parameters, more severe convergence problems are expected with SiC models. This is mainly caused by the extremely low equilibrium minority carrier concentration. In analytical models, junction voltage drops are calculated from the minority carrier concentration at junctions, which changes within the range of 10^{-34} to 10^{17} cm^{-3} during switching at room temperature. This large variation causes simulation convergence problems and may cause "spikes" in output waveforms. Certain precautions should be

taken to solve this problem. The internal SPICE diode model is well implemented and exhibits good convergence. It includes an exponential function to calculate the junction voltage. Making use of the the exponential expression in the SPICE diode model alleviates the convergence problem.

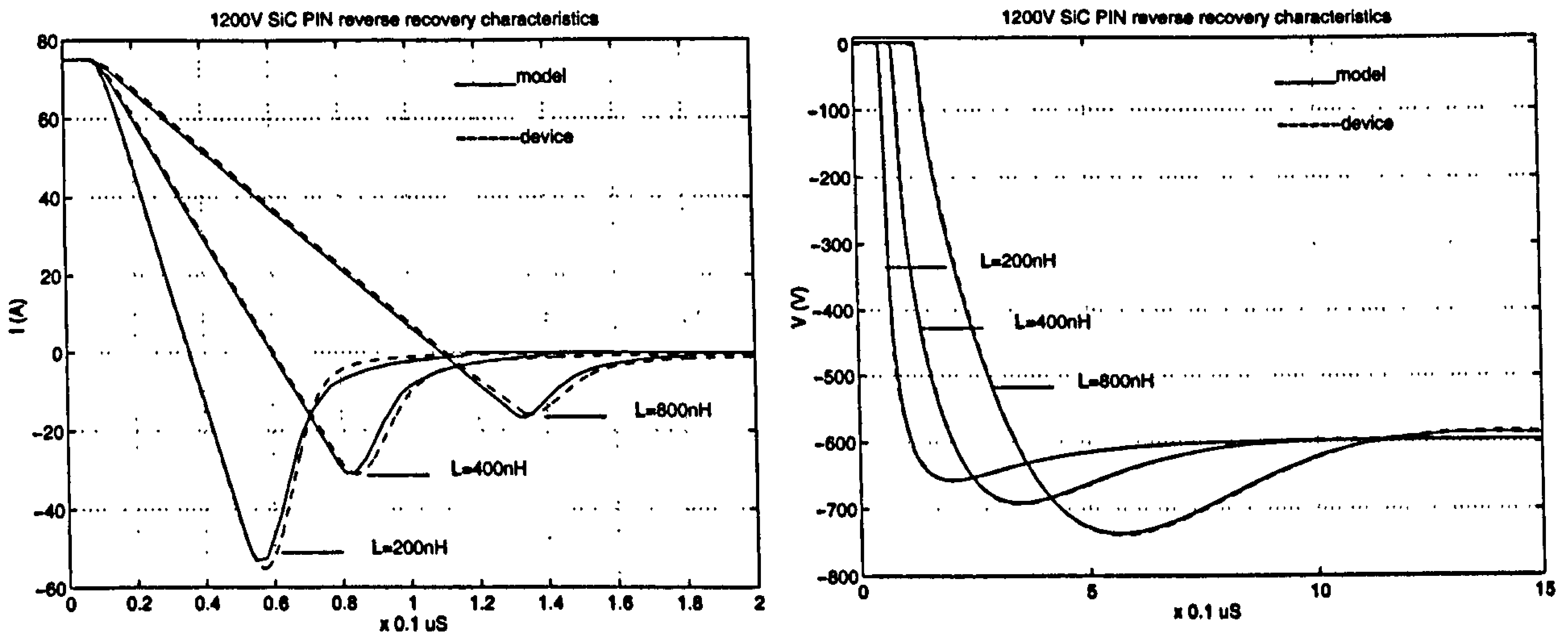
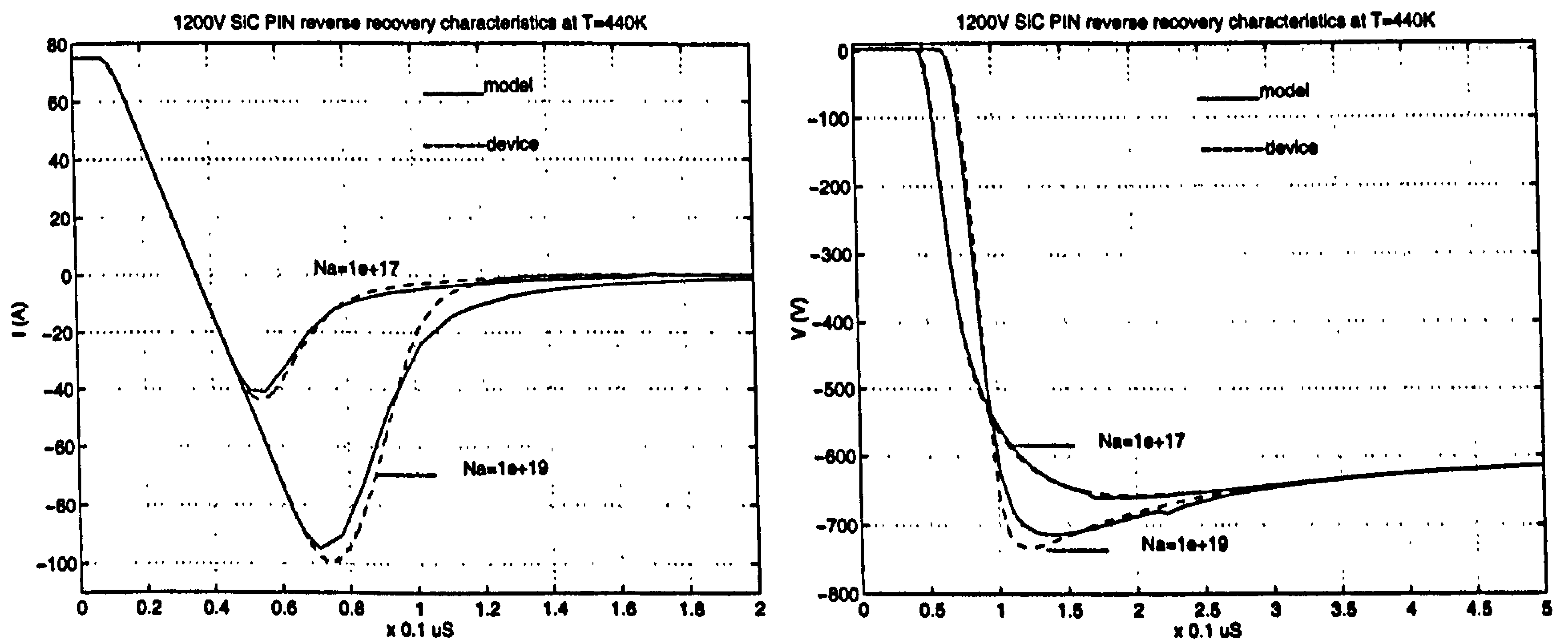


Figure 8.5 (b) $\tau_{n0}=\tau_{p0}=0.02\mu s$, $N_{p+}=1\times10^{19}cm^{-3}$, T=300K



(c) T=440K, $\tau_{n0}=\tau_{p0}=0.02\mu s$, di/dt=3000A/$\mu s$

Figure 8.5 Reverse recovery characteristics of a 1200V 6H-SiC PiN diode

For Schottky diodes, only capacitances and Schottky barrier are critical for modelling because they are unipolar devices and the device physics is relatively simple.

The PSpice internal diode model is adequate for this purpose. Diffusion capacitances in the PSpice diode model can be disabled for only junction capacitances exist in Schottky devices.

8.3 A Novel SPICE Voltage Controlled Switch Model

The circuit simulator PSpice has become a powerful and essential tool for circuit design and analysis. The voltage-controlled switch is a useful device, aiding circuit topology analysis. It is frequently used in switching circuit simulation to replace a real switching device model where accurate switching waveforms are not required. Although conditional statements and piecewise functions are not desirable in a circuit simulation, they are indispensable in many modelling cases. These applications require a simple but functional voltage (or current) controlled switch model.

The resistance (R_s) of the PSpice voltage controlled switch is obtained from the following six piecewise equations which have four parameters V_{on}, V_{off}, R_{on}, R_{off} and one control variable V_c [8.27]:

$$
\begin{aligned}
V_{on}>V_{off} \quad & \begin{cases} R_s=R_{off} & V_c\le V_{off} \\ R_s=\exp\left(L_m+\dfrac{3L_r(V_c-V_m)}{2V_d}-\dfrac{2L_r(V_c-V_m)^3}{V_d^3}\right) & V_{off}<V_c<V_{on} \\ R_s=R_{on} & V_c\ge V_{on} \end{cases} \\
V_{on}<V_{off} \quad & \begin{cases} R_s=R_{on} & V_c\le V_{on} \\ R_s=\exp\left(L_m-\dfrac{3L_r(V_c-V_m)}{2V_d}+\dfrac{2L_r(V_c-V_m)^3}{V_d^3}\right) & V_{on}<V_c<V_{off} \\ R_s=R_{off} & V_c\ge V_{off} \end{cases}
\end{aligned}
\qquad (8.1)
$$

where:

$$
L_m=\frac{1}{2}\ln(R_{on}R_{off}) \qquad L_r=\ln(R_{on}/R_{off}) \qquad V_m=\frac{V_{on}+V_{off}}{2} \qquad V_d=V_{on}-V_{off} \qquad (8.2)
$$

In circuit simulation, continuity of the circuit variables and their derivatives is

commanded to ensure good circuit convergence, especially with transient simulations [8.28]. However, as will be shown, although the derivative of V_c for the PSpice voltage-controlled switch resistance is continuous, it is not derivatable at both $V_c=V_{on}$ and $V_c=V_{off}$. This also means that the second order derivative of $R_s(V_c)$ is discontinuous at these two points. This will increase simulation times and may cause convergence problems with high order circuits. In Section 8.1, a switch is required to implement a power PiN diode model. The switch properties are critical to model convergence. If the PSpice voltage controlled switch model is employed, convergence problems occur frequently.

To improve convergence of the voltage controlled switch, the following new switch model equation is proposed:

$$R_s=\exp(L_m+\frac{1}{2}L_r\tanh(\frac{\lambda(V_c-V_m)}{V_d})) \tag{8.3}$$

where $\lambda>0$ is a parameter controlling the changing rate of R_s between V_{on} and V_{off}. Derivatives of this function exist at any order and approach zero as V_c goes beyond V_{on} and V_{off}. In addition, only one expression covers all cases while the original PSpice voltage-controlled switch model has six expressions, which increase simulation times. Resistance and its first derivative for the PSpice voltage controlled switch model and the proposed model are compared in Figure 8.6. For the PSpice model, the sharp corner of dR_s/dV_c at $V_c=V_{off}$ can be clearly seen, which means the non-existence of a corresponding d^2R_s/dV_c^2. The same is true for $V_c=V_{on}$. For the proposed model, dR_s/dV_c changes smoothly at both V_{on} and V_{off}, which also holds true for the nth derivative of R_s in the range $-\infty<V_c<\infty$. The smoothness of the proposed model will be shown to improve speed and convergency of the voltage (or current) controlled switch.

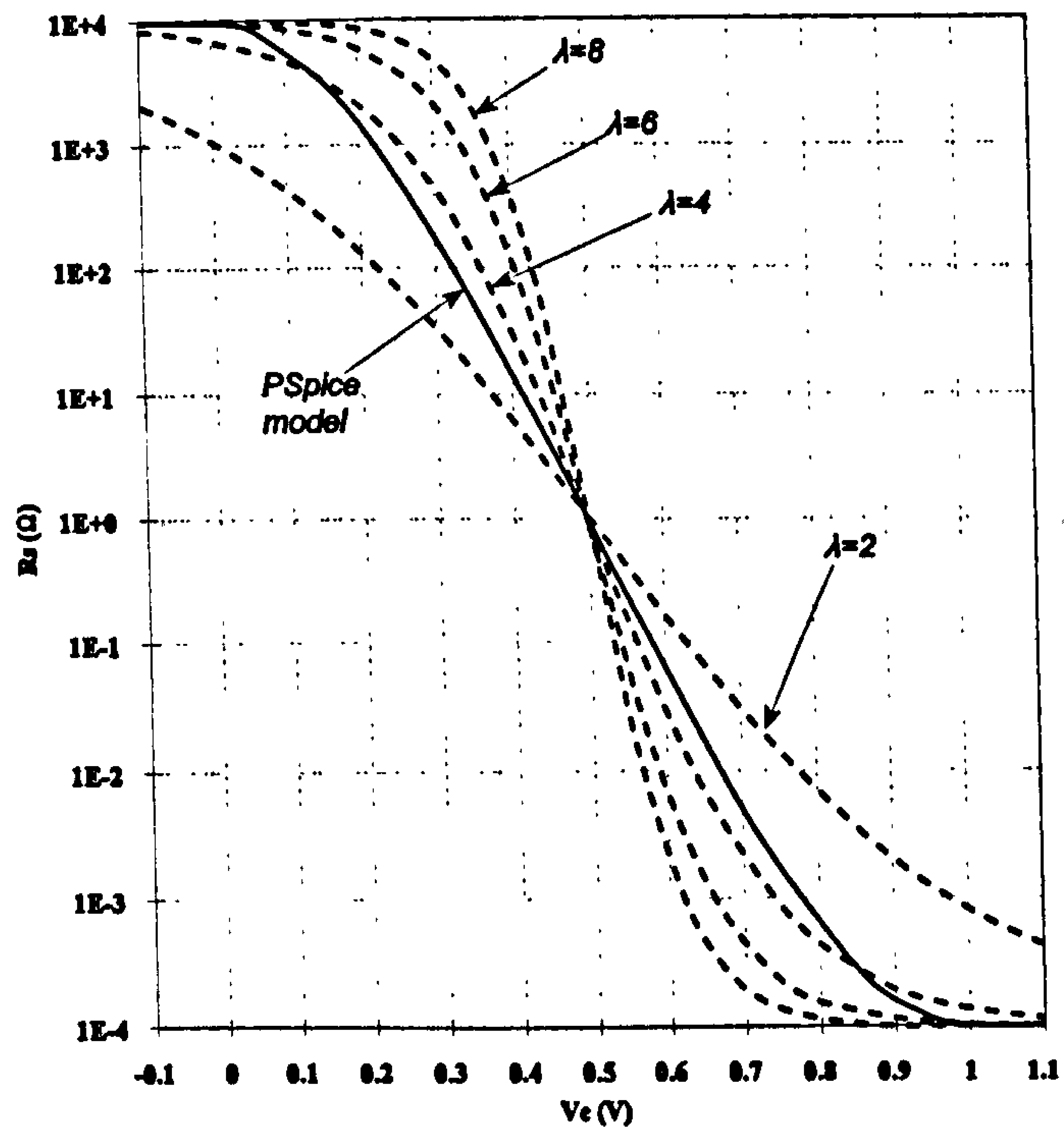
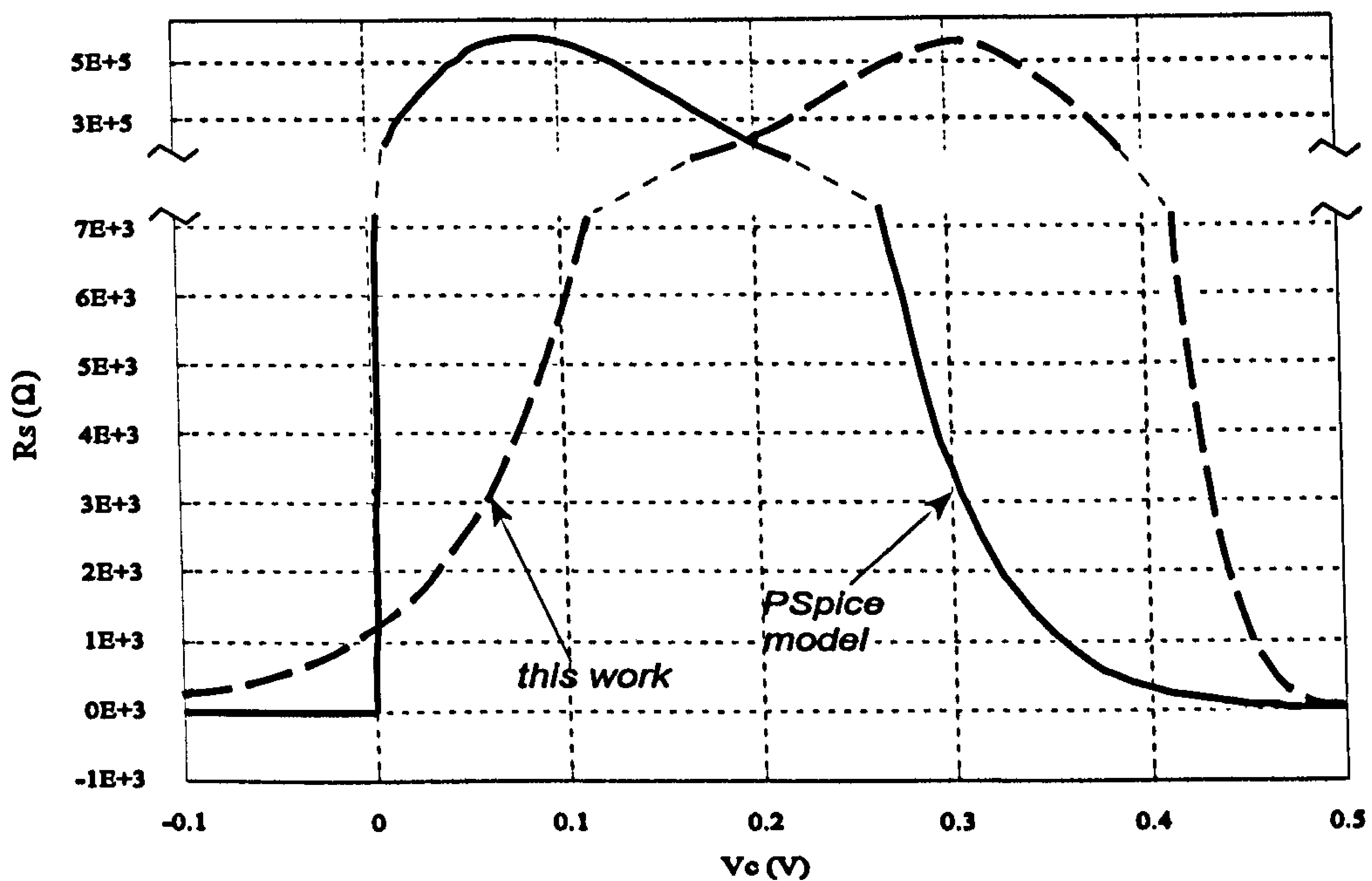


Figure 8.6 (a)



(b)

Figure 8.6 Comparison of the new switch with that from PSpice: (a) R_s versus V_c and (b) dR_s/dV_c versus V_c

The PSpice voltage-controlled switch expressions strictly set the value of the switch resistance to R_{on} at $V_c \geq V_{on}$ and R_{off} at $V_c \leq V_{off}$. However this precision is unnecessary in most practical power applications. The user usually sets R_{on} as an arbitrary very small value

and R_{off} as an arbitrary very large value. As V_c changes from V_{on} to V_{off}, R_s changes from a very small value to a very big value or vice versa. Therefore, if the expressions are changed so that R_s is very close to R_{on} in the vicinity of V_{on} and very close to R_{off} in the vicinity of V_{off} and the error is small enough, it will not affect the accuracy of the simulation. The relative errors of the switch resistance at V_c=V_{on} and V_{off} are 0.07% for λ=8, which is suitable for most cases.

Table 8.1 The simulation time against the trigger angle (PC Pentium 90)

delay α (°)	0	30	60	90	120	150	180	average
PSpice (s)	19.6	20.7	24.5	26.5	23.3	22.1	19.7	22.3
new, λ=8 (s)	15.6	15.7	17.8	18.0	18.4	18.0	15.4	17.1
reduction (%)	20.4	24.2	27.4	32.1	20.7	18.5	22.0	23.6
new, λ=2 (s)	16.0	17.4	16.1	18.8	18.7	17.9	15.5	17.3
reduction (%)	18.3	16.0	34.2	29.0	19.8	18.7	21.4	22.5

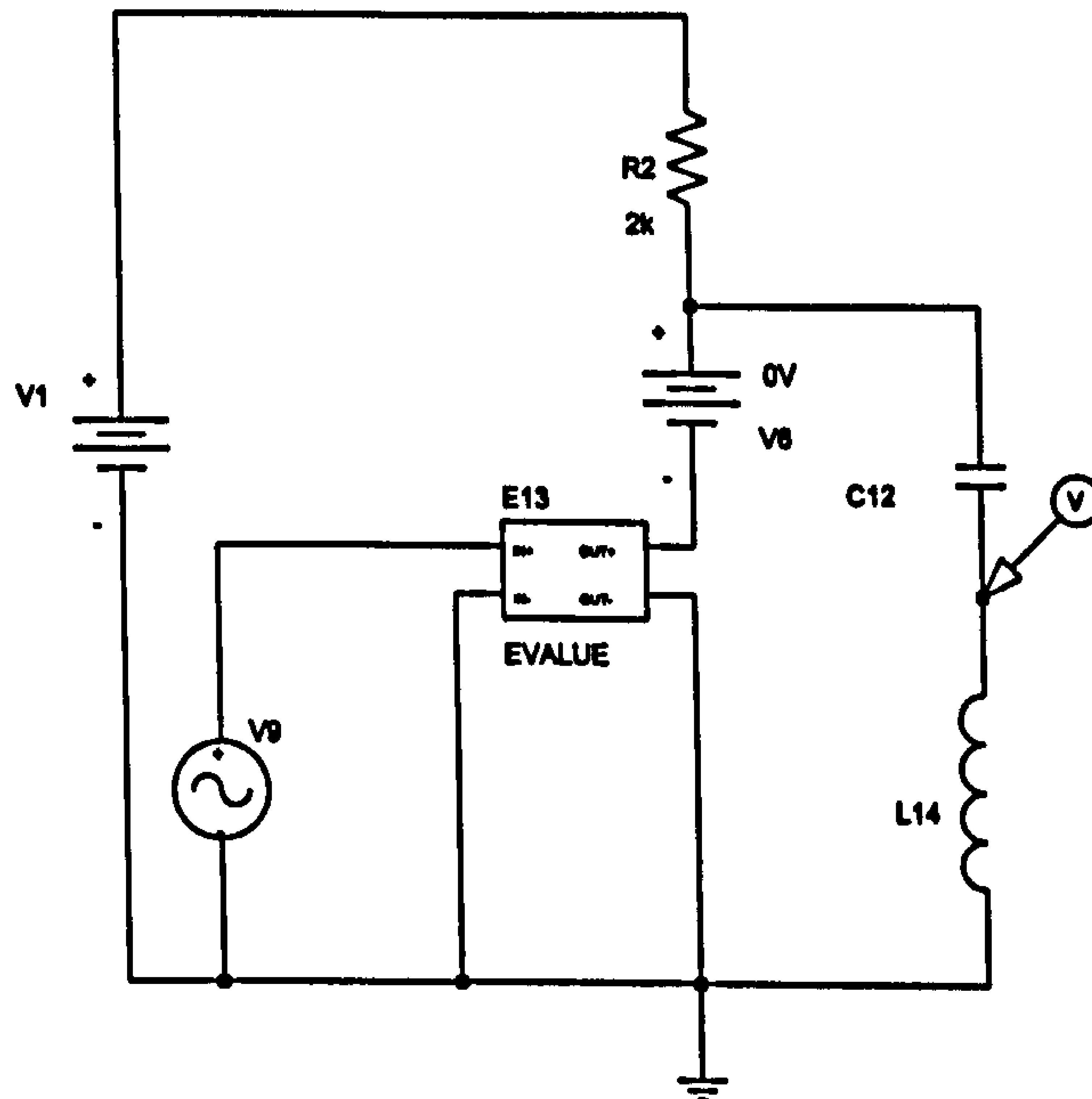
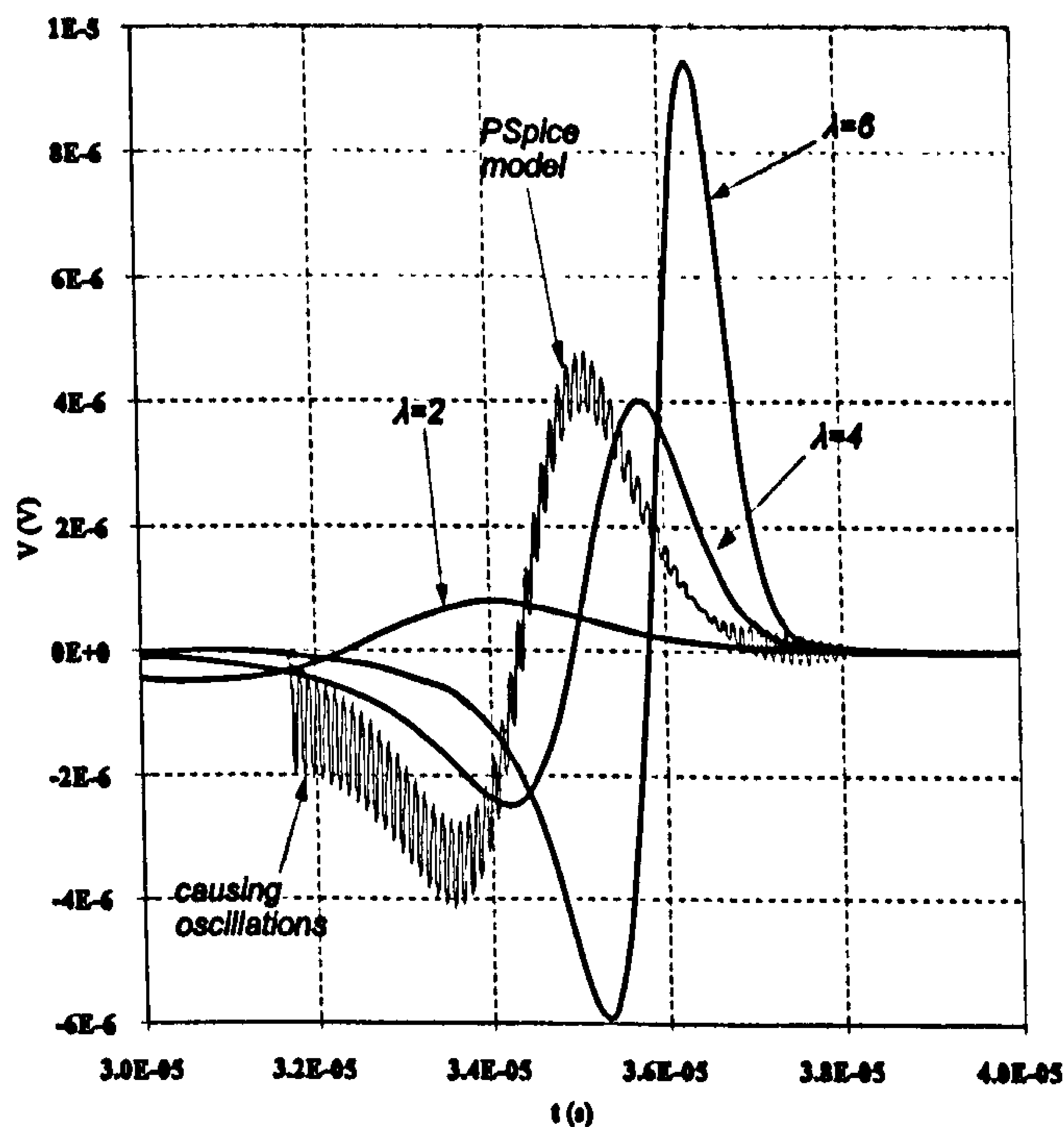


Figure 8.7 Transient testing circuit

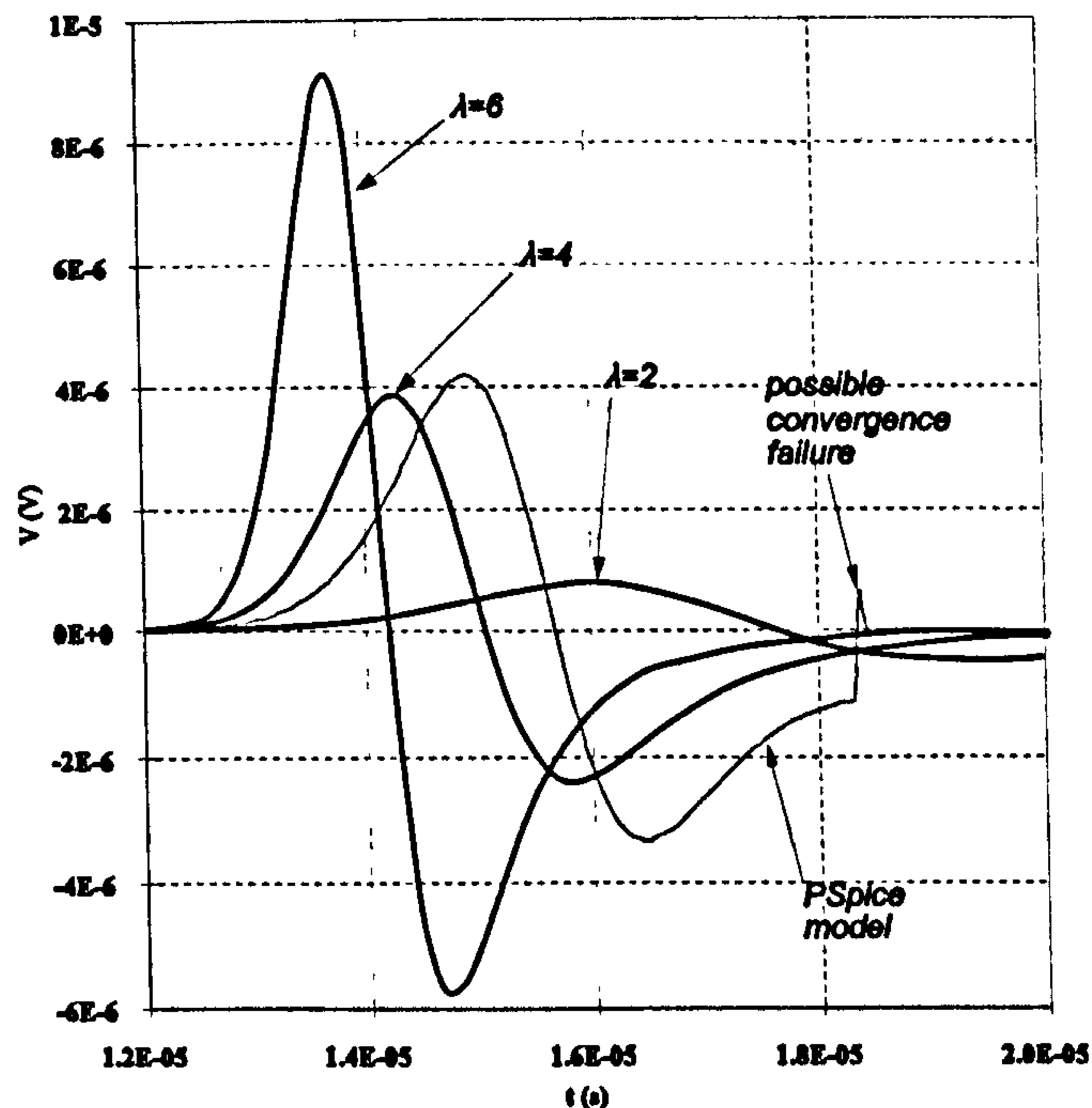
The two switch models with different λ are implemented, as voltage-controlled current sources for comparison with PSpice internal switch model. The switching

waveforms of a 3-phase full bridge controlled AC-DC converter are simulated in a PC with a Pentium 90 MHz processor to compare the models' simulation speed. The voltage-controlled switches are used to replace the real switching devices (thyristors). The simulation times for two switching cycles against the trigger angle, α, are listed in Table 8.1. Obviously, the new switch produces faster simulation times than with the internal PSpice model.

Transient simulation waveforms with the two switches in the logic switching circuit shown in Figure 8.7 are also compared in Figure 8.8. For the proposed model, switching waveforms for three different values of λ (6, 4, and 2) are shown. As the new switch operates, a particular circuit node "V" voltage changes smoothly while abrupt changes occur with the corresponding PSpice switch at turn on and off. As shown in Figure 8.8 the discontinuous change may cause severe oscillation or convergence failure, which is time-consuming. As explained this is caused by the derivative discontinuity of the PSpice piecewise model.



(a)



(b)

Figure 8.8. Switching transient of the two switches: (a) turn-on and (b) turn-off

8.4 Conclusion

In this chapter, two analytical PiN diode models were implemented in PSpice. Compared with experimental data, both reproduce satisfactory results. Although "Model I" is more accurate than "Model II", its relative poor convergence makes it less favourable. A 6H-SiC diode model was also developed and exhibits good agreement with numerical simulation results. The challenge in developing SiC device models for circuit simulations was briefly discussed.

The voltage (or current) controlled switch in PSpice is found to have convergence problems when simulating high order circuits. A new, simple voltage-controlled switch for PSpice is proposed in this chapter. In contrast with the piecewise approach in PSpice, the model has a unified continuous form. It eliminates the discontinuity of the switch resistance derivatives and thus improves simulation speed and convergence. The proposed model is also useful for implementing complex equations into a circuit.

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CHAPTER 9

A NEW STATIC INDUCTION THYRISTOR (SITh) ANALYTICAL MODEL

The Static Induction Thyristor (SITh) or Field-Controlled Diode (FCD) was first introduced by Teszner in the sixties [9.1]. This device is capable of conducting large currents with a low forward-voltage and turns off quickly. Together with high dv/dt and di/dt capabilities, an excellent device is promised for applications such as MHz switching in variable high-frequency generators, direct current transmission and nuclear fusion. After the SITh was first fabricated in 1972, several papers reported Si SI thyristors with blocking voltages of several hundred to several thousand volts and average current ratings of several to hundreds of amperes [9.2]-[9.6]. With the advent of SiC technology, a 4H-SiC SITh has been fabricated with a forward blocking voltage of 300 V [9.7].

To date, only one SITh model has appeared in the literature [9.8]. However, with some unsolved integrations and a time-dependent effective diffusion length, implementation of this model requires complex programming. Hence it is not suitable for circuit simulators such as PSpice.

In this paper an analytical, non quasi-static SITh model is presented, which can be easily implemented in circuit simulators. Being physics based, this model gives accurate results and takes into account device structure parameters and temperature. It is also computationally fast and exhibits good convergence.

The chapter is organized as follows. Firstly, the physical operating mechanisms of the device are examined. Based on this, the basic structure of the model is developed. After presenting the model, it is validated by comparisons with numerical simulations and

published experimental results.

9.1 Understanding SITh Static and Switching Characteristics

9.1.1 Static Characteristics

(i) On-State

A buried-gate SITh cell structure and its equivalent circuit representation is shown in Figure 9.1. In the on-state, the emitter junction of the integral wide base $P^+N^-P^+$ transistor T_1 is forward biased. A large number of excess carriers are injected into the base, hence the resistivity of the base is greatly reduced. The carrier distribution in the base of SIThs is similar to that in IGBTs. However unlike the IGBT, whose collector junction of the integral P^+N^-P transistor is always reverse biased due to the voltage drop in the channel, the collector junction of T_1 is forward biased. As a result the excess carrier concentration at the collector end of the base for the SITh, p_w, is significantly higher than the base doping level, thereby further reducing the resistivity as shown in Figure 9.2. In comparison, the region under the P base of IGBTs is mostly unmodulated since p_w is zero. Generally, for the same base width, doping and lifetime, SIThs have better current density handling ability than IGBTs.

Like PiN diodes, the N^+ cathode region of the SITh injects electrons into the base region between the P^+ gate and N^+ cathode during the on-state, thus modulating the channel resistivity. The P^+ gate and the channel region can be modelled as a JFET operating in the bipolar mode. Electrons flow from the cathode into the base region under the P^+ gate through the channel, providing the base current of the $P^+N^-P^+$ transistor. Due to the high doping level of the P^+ gate, no electrons flow into the P^+ gate. A portion of hole current flows through the P^+ gate and the channel towards the cathode directly. The remaining hole current flows through the P^+ gate to the channel as the gate current of the BMFET (Bipolar

Mode JFET). The short cathode and gate distances result in a uniform and large carrier concentration in this region, hence negligible voltage drop. Thus V_{gk} is comprised of essentially two junction (j3, j4) voltages.

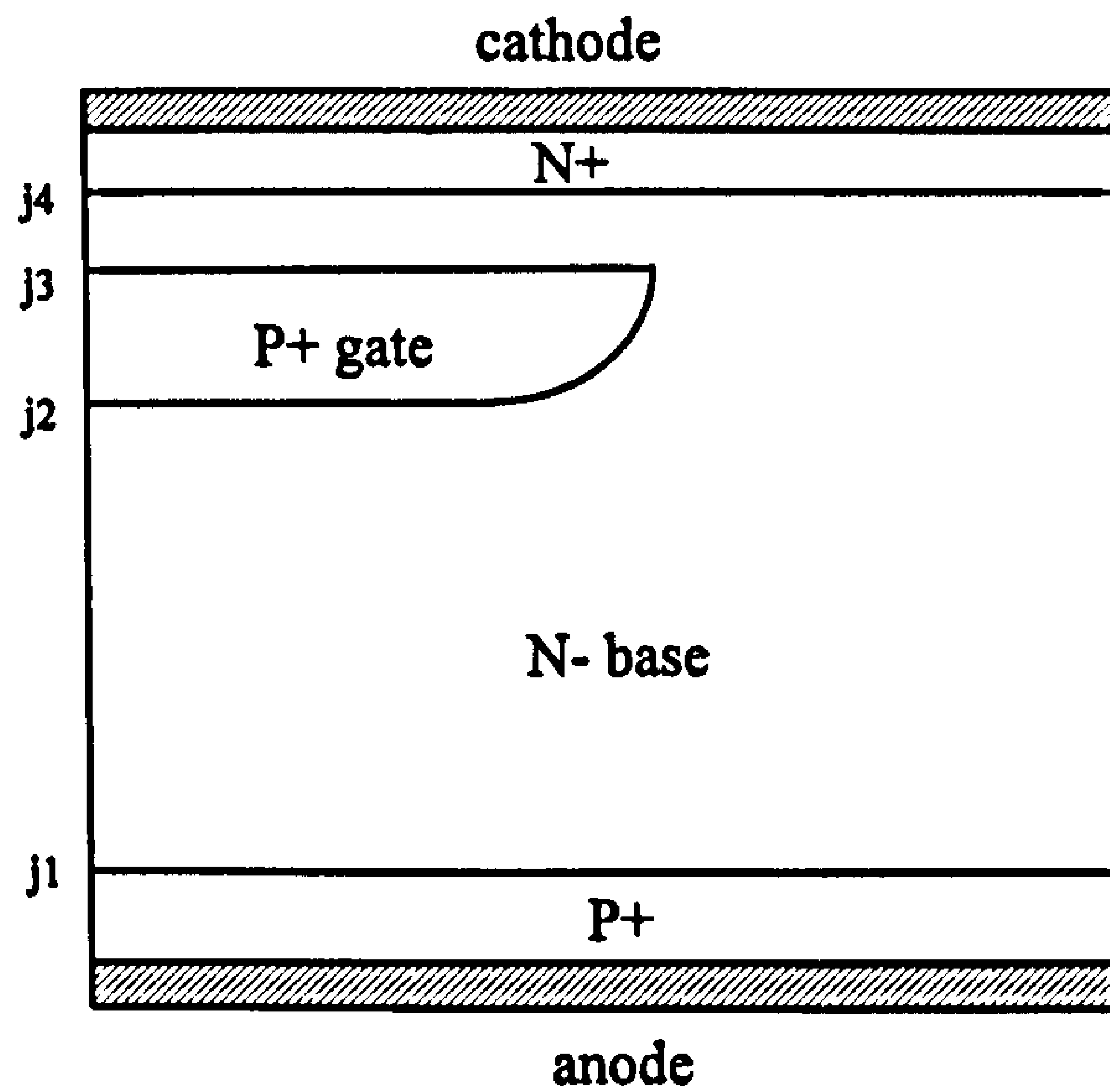


Figure 9.1 (a) Half a cell structure of a Buried-gated SITh

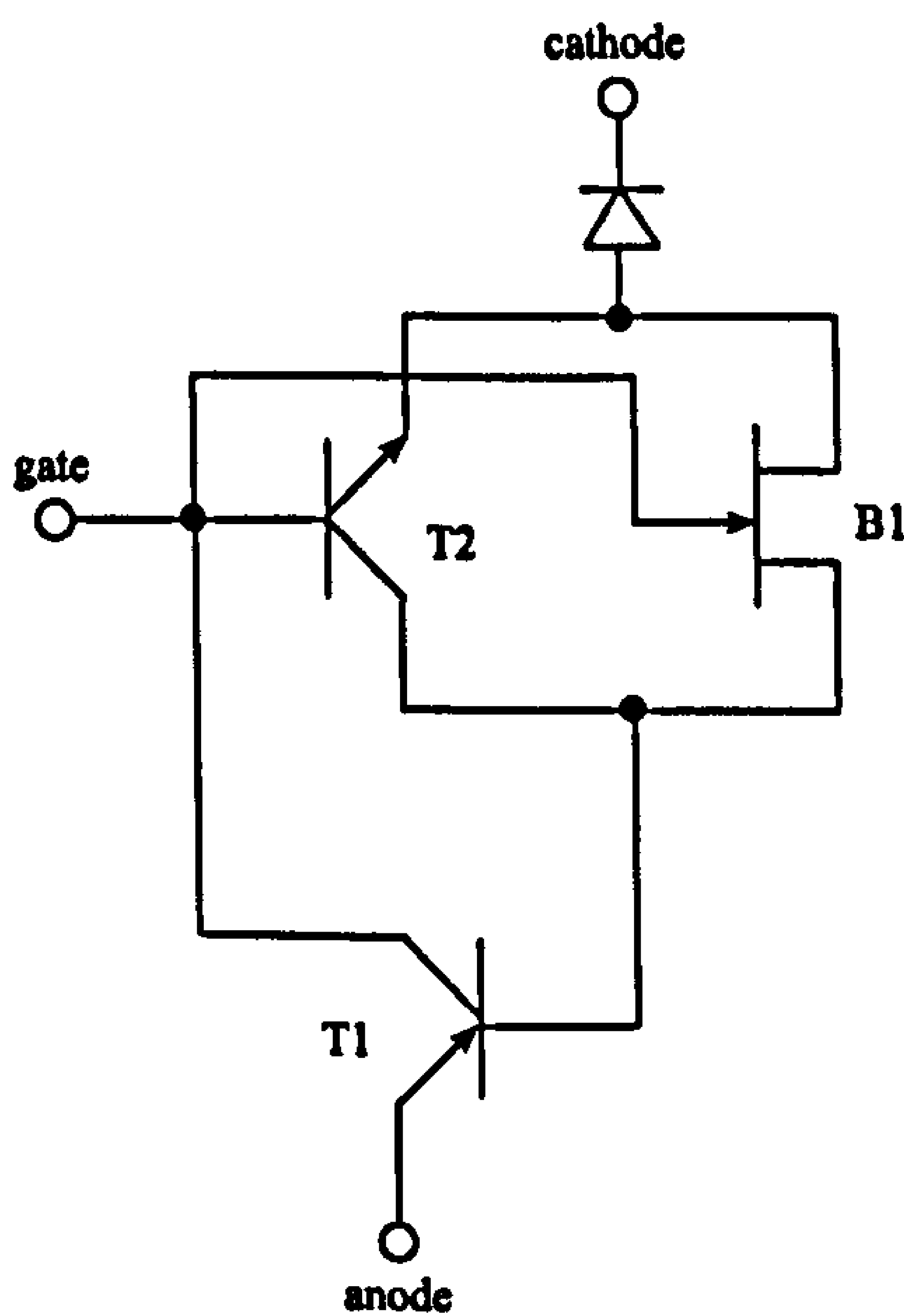


Figure 9.1 (b) Equivalent circuit representation of the device

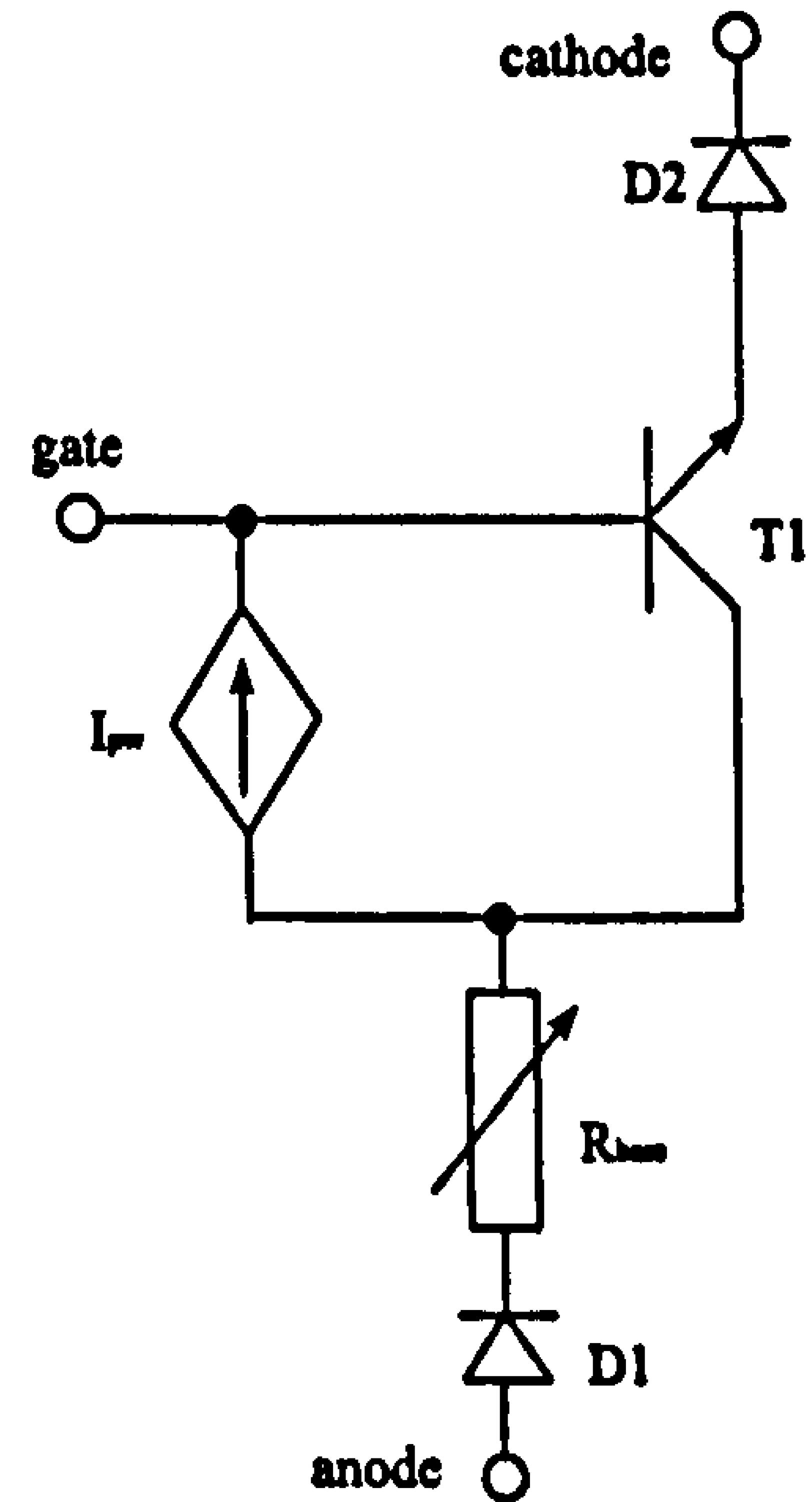


Figure 9.1 (c) Schematic representation of the model structure

(ii) Off-State

If a sufficiently negative voltage is applied to the gate, a depletion layer forms around the P^+ gate and fully cuts off the channel. Hence the SITh can support a high anode

voltage with a small leakage current. The negative gate voltage establishes a potential barrier in the channel which impedes the transport of electrons from the cathode to the anode. Increasing the anode voltage decreases the barrier height until current flow commences. Since larger gate bias voltages increase the channel potential barrier height, anode current flow is shifted to the higher anode voltage until avalanche breakdown of j2 is reached.

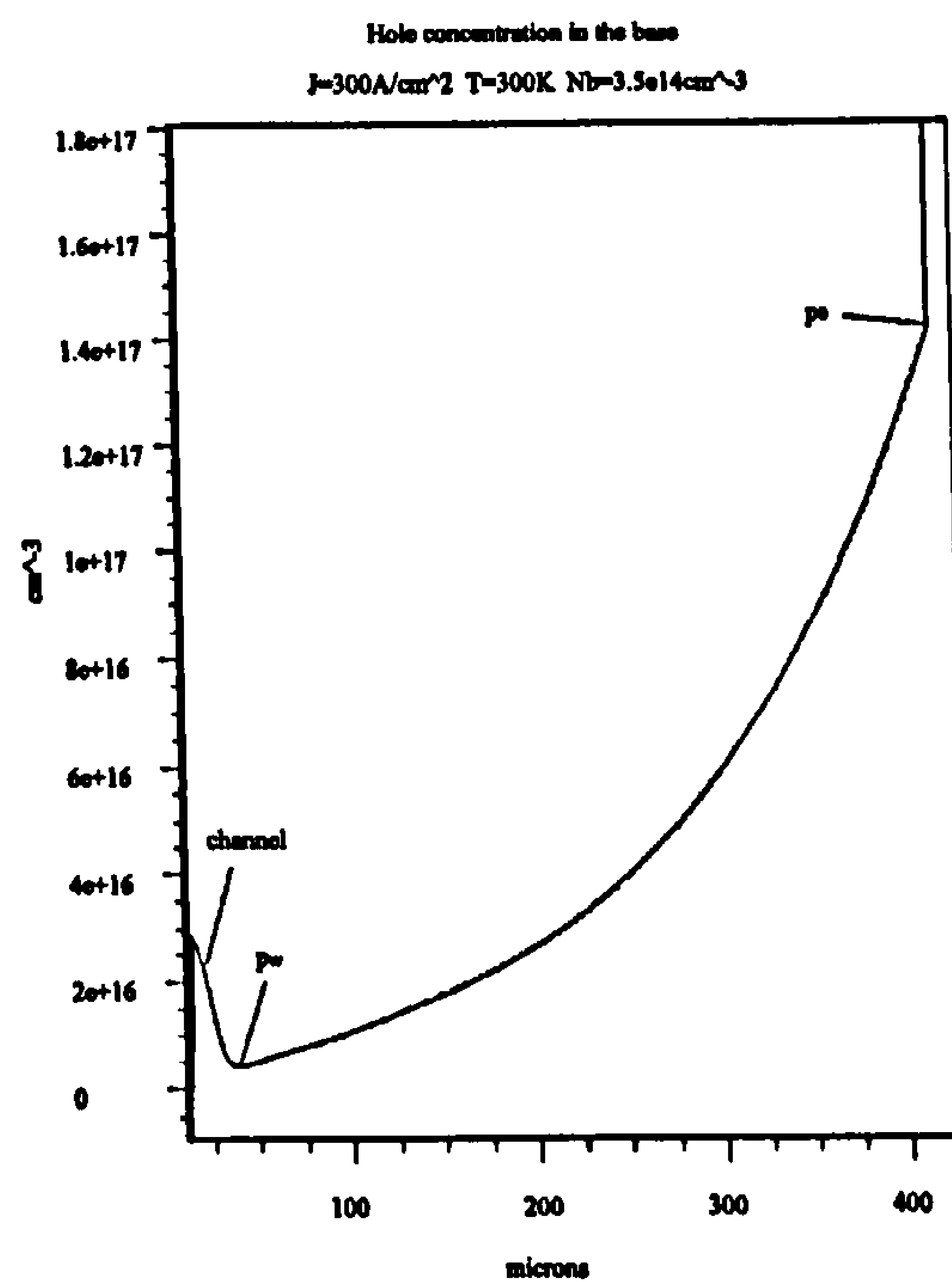


Figure 9.2 Carrier distribution in the base

9.1.2 Switching Characteristics

(i) Turn-Off

To turn off SIThs, a large negative gate current pulse is required. When a negative gate current is applied, the hole current flowing to the cathode region begins to transfer to the gate. This leads to T_2 entering the linear region because the hole current acts as transistor base current. The depletion layer at j2 gradually extends into the channel. A potential barrier is created in the channel, narrowing the channel and removing the excess carriers from the channel. If the gate voltage is sufficiently large, the depletion layer of adjacent gate regions merge in the channel and eventually turn off the electron current flow

in the channel. In spite of no electron current, the hole current continues to flow due to the remaining slowly decaying excess carriers in the base. The removal of the channel current also stops the injection of electrons and holes into the region between the gate and cathode, then the parasitic PiN diode in this region switches off. A sudden gate voltage fall usually occurs at this moment due to the short width of the PiN diode base and the existence of parasitic inductance in the gate drive circuit.

(ii) Turn-On

When the gate-source voltage changes from negative to positive, a SITh switches on rapidly, providing the gate current and voltage drive are sufficient. Initially, the gate-cathode PiN diode turns on and injects electrons from the cathode into the base and channel. The positive gate voltage reduces the potential barrier in the channel, which gradually becomes conductive. When electrons reach j1, the P^+ anode begins to inject holes into the base, providing the base current of T_2. Increasing the base current drives T_2 into saturation. Meanwhile, the voltage supported by j2 falls. Eventually j2 is forward biased and the device is fully turned on.

9.2 Modelling the SITh

9.2.1 Basic Structure of the model

Based on the discussion in Section 9.1, the basic model structure shown in Figure 9.1 (c) can be achieved. The carrier concentration in the base region between the gate and the cathode, hence the junction voltage of j4, is calculated using the junction voltage of j3. The hole current flows into the P^+ gate, providing the base current of the gate transistor. Using carrier concentrations at j1 and j2, the modulated resistance of the wide base and the junction voltage of j1 are obtained. Note only one transistor is needed to model the gate

region. The reason for this and the detailed implementation of the model is explained in the following sections.

9.2.2 Base Region

(i) Currents

Firstly the derivation of the anode current I_a and the hole current under the P^+ gate I_{pw} for a given anode voltage are presented. Because high level injection occurs in the base region in the normal operating current range and to maintain charge neutrality, n≅p, the excess carrier concentration is given by the ambipolar diffusion equation:

$$\frac{\partial^2 p}{\partial x^2}=\frac{p}{L_a^2}+\frac{1}{D_a}\frac{\partial p}{\partial t} \tag{9.1}$$

The origin of the x axis is at the P^+ anode/N^- base junction. By taking the Laplace transform of Equation (9.1) [9.13] and using the boundary conditions: $p(x=0)=p_0$, $p(x=w)=p_w$, the solution of Equation. (9.1) is:

$$P(x)=P_0\frac{\sinh(\frac{W-x}{L_s})}{\sinh(\frac{W}{L_s})}+P_w\frac{\sinh(\frac{x}{L_s})}{\sinh(\frac{W}{L_s})} \tag{9.2}$$

where P(x), P_0 and P_w are the Laplace transforms of p(x), p_0 and p_w respectively and L_s is defined as:

$$L_s=\frac{L_a}{\sqrt{1+\tau_a s}} \tag{9.3}$$

The carrier concentration p_w is important in terms of the modulated base region resistance. Although p_w is significantly larger than the doping level in the on-state, it is still negligible compared to p_0, due to the long base width of a typical high voltage power device. During device turn-off, p_w drops to zero immediately after the anode voltage starts

to rise, while p_0 is almost unchanged. For this reason p_w is set to zero when calculating I_a and I_{nw}, hence, I_{pw}.

By solving (9.2) and the ambipolar transport equation:

$$I_n = \frac{b}{1+b} I_a + qAD_a \frac{\partial p}{\partial x} \tag{9.4}$$

I_a and I_{nw} are obtained from:

$$I_a = \frac{1+b}{b}\left(I_{n0} + Q_0 \frac{2}{k} \frac{z}{\tanh(z)}\right) \tag{9.5}$$

$$I_{nw} = I_{n0} + Q_0 \frac{2}{k} z \frac{\cosh(z)-1}{\sinh(z)} \tag{9.6}$$

where I_{n0} is the electron current at the P^+ anode/N^- base junction (J_1), with $Q_0 = qAp_0w/(2\tau)$, $k = w^2/L_a^2$ and $z = w/L_a$.

Using Pades approximation [9.9], Eqns. (9.5) and (9.6) can be represented by an electrical network [9.9], in which the controlled voltage source Q_0 drives the circuit.

Assuming the quasi-equilibrium approximation is valid in the highly doped anode, recombination in the junction depletion region is neglected and a high level injection condition in the base, I_{n0} is given by the electron diffusion current at the anode side of the junction, with h_p a parameter reflecting the anode structure:

$$I_{n0} = qAh_p p_0^2 \tag{9.7}$$

h_p is a temperature dependent. Because the high voltage SITh anode is usually formed using diffusion, it is difficult to give an explicit expression of this temperature dependence. In this chapter, h_p is modelled as $h_p(300) \times (T/300)^\gamma$, where parameters $h_p(300)$ and γ are obtained by curve fitting.

(ii) Carrier Concentrations

The carrier concentrations p_0 and p_w are computed from the following equations:

$$p_0 = p_{B0}(\exp(\frac{V_{j1}}{V_T}) - 1) \tag{9.8}$$

$$p_w = p_{B0}(\exp(\frac{V_{j2}}{V_T}) - 1) \tag{9.9}$$

Equations (9.8) and (9.9) can be implemented as two non-linear controlled voltage sources. However the exponent functions in these equations introduce a convergence problem into the model. The PSpice internal diode model describes the relationship between diode voltage and diode current as $I = I_s(\exp(V/V_T) - 1)$. More importantly, the internal PSpice function shows good convergence (see Section 8.2). By setting I_s to p_{B0}, p_0 and p_w are implemented as diode currents with the diode voltages equal to the junction voltages V_{j1} and V_{j2}.

(iii) Base Voltage Drop

The voltage drop in the base comprises an ohmic component and a Dember voltage. Since p_w is significantly larger than the background doping level, the Dember voltage component, $-\frac{2}{1+b}\ln\frac{p_0+N_B}{p_w+N_B}$ can be ignored. Using the carrier distribution described in (9.2), modulated base resistance R_{mod} exhibits poor convergence when implemented in PSpice. Instead, the ohmic voltage drop is calculated using the carrier distribution described by:

$$p(x) = p_0 \frac{\sinh(\frac{w-x}{L_a})}{\sinh(\frac{w}{L_a})} + p_w \tag{9.10}$$

Hence,

$$R_{mod} = \frac{2L_a arctanh[\frac{a\ \tanh(w/2L_a)}{c}]}{qA(\mu_n + \mu_p)a} \tag{9.11}$$

$$a=\sqrt{p_w^2+p_0^2 csch^2(\frac{w}{L_a})} \qquad c=p_w+p_0 csch(\frac{w}{L_a})\tanh(\frac{w}{2L_a}) \tag{9.12}$$

The resistance gives a good approximation of the resistance calculated from the carrier distribution in Equation (9.2).

(iv) Moving Boundary Effect

During the anode voltage transition, the quasi-neutral base width w changes with the applied anode voltage. An important phenomenon is the redistribution of the excess carriers as the anode voltage changes. Excess carriers are swept into the narrower quasi-neutral base while the excess carrier charge diminishes slowly via recombination. Differing from the case with a constant quasi-neutral base width, the hole current has a moving boundary redistribution component. Assuming zero electron current and an essentially linear carrier distribution with a small redistribution component during the transient, the hole current at the collector is described in terms of the boundary moving velocity of the IGBT analytical model by Hefner [9.10]:

$$I_{pw}=\frac{1}{1+b}I_a+\frac{2D_a}{w^2}Q-\frac{Q}{3w}\frac{dw}{dt} \tag{9.13}$$

The redistribution component of the hole current $I_{dis}=-\frac{Q}{3w}\frac{dw}{dt}$ is critical in the voltage transient. The net effect of the redistribution component is time-varying capacitance across j2. During device turn-off, the large excess carrier charge Q slows down the boundary moving velocity dw/dt, while during turn-on, Q is small, whence the anode voltage falls rapidly.

In this model, a controlled current source I_{dis} representing the redistribution component is added to the transistor collector junction, together with $I_{pw}=I_a-I_{nw}$, acting as the base current of the gate transistors. A parameter α is introduced ($I_{dis}=-\frac{Q}{\alpha w}\frac{dw}{dt}$) to

account for temperature and structure effects.

The Laplace transform of the base excess carrier charge Q(s) is computed from Eqn. (9.2):

$$Q(s)=qA(p_0+p_w)L_s\tanh(\frac{W}{2L_s}) \tag{9.14}$$

By ignoring the contribution of p_w to the excess carrier charge, Q can be incorporated in the subcircuit calculating I_a and I_{nw}.

9.2.3 Gate region

The PSpice JFET model can not simulate the resistivity modulation of the channel satisfactorily, for it is a unipolar device. Instead, a PSpice internal NPN BJT transistor model is used to simulate the gate region. Thus there are two NPN transistors in parallel in the gate region. To further simplify the model, these two transistors are combined into one transistor. Simulation results show that this approach is acceptable. The transistor junction capacitance parameters C_{jc} and C_{je} are realised using the doping level N_B and N_{epx} and by assuming step junctions:

$$C_{jc}=\sqrt{0.5q\varepsilon_S N_B} \qquad\qquad C_{je}=\sqrt{0.5q\varepsilon_S N_{epx}} \tag{9.15}$$

If the doping of the N^+ cathode is uniform, the junction voltage of j4, V_{j4}, is given by:

$$V_{j4}=V_T\ln(\frac{N_i}{N_{epx}}(\exp(\frac{V_{j3}}{2V_T})-1)+1) \tag{9.16}$$

In this chapter V_{j4} is approximated by:

$$V_{j4}=\beta V_{j3} \tag{9.17}$$

where β is a constant between 0 and 1, accounting for the effects of the N^+ cathode doping profile and the gate region structure.

9.2.4 Forward blocking capability

The anode current in the forward blocking mode is given by an empirical expression [9.11]:

$$I_a = I_0 \exp\left(\frac{q}{kT}(mV_{ak}^n - \alpha V_{gk})\right) \qquad (9.18)$$

where I_0, m, n and α are parameters determined by fitting with experimental results. A PSpice diode model is employed to realise the exponent function in Eqn. (9.18).

9.3 Physical Parameter Modelling

In this section the modelling of physical parameters, namely mobility and lifetime τ, is presented.

9.3.1 Mobility Model

The hole and electron mobilities are modelled as doping level and temperature dependent, by the Caughey-Thomas Equation [9.14]:

$$\mu_n = 55.24 + \frac{1425 \times (\frac{T}{300})^{-2.3} - 55.24}{1 + (\frac{N_D + N_A}{1.072 \times 10^{17}})^{0.73} (\frac{T}{300})^{-3.8}} \quad (\text{cm}^2/\text{Vs}) \qquad (9.19)$$

$$\mu_p = 49.7 + \frac{479.37 \times (\frac{T}{300})^{-2.2} - 49.7}{1 + (\frac{N_D + N_A}{1.606 \times 10^{17}})^{0.7} (\frac{T}{300})^{-3.7}} \quad (\text{cm}^2/\text{Vs}) \qquad (9.20)$$

The carrier-carrier scattering effect is not considered here.

9.3.2 Lifetime Model

The lifetime is modelled as doping level and temperature dependent [9.12]:

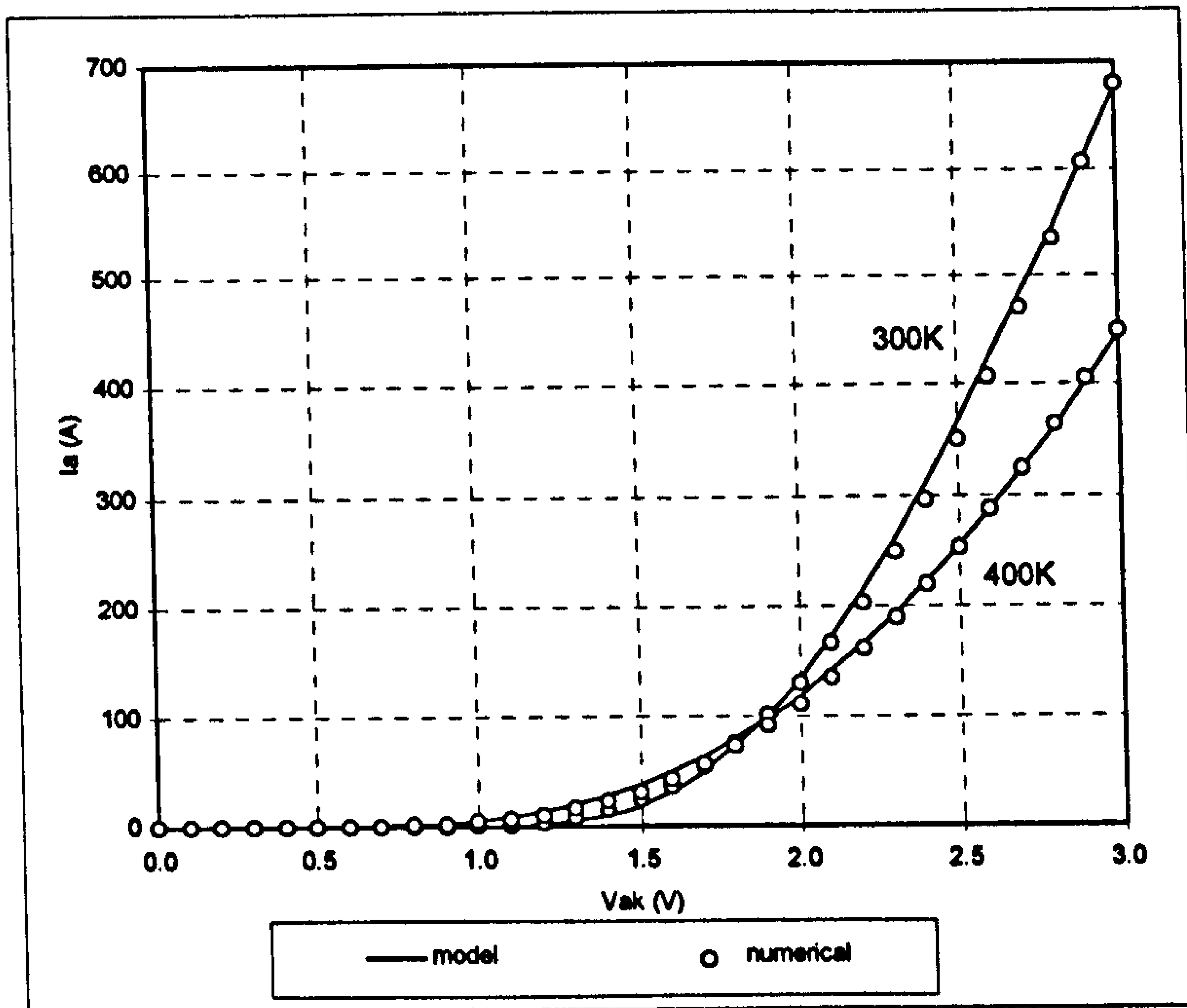
$$\tau_{n,p} = \frac{\tau_{n0,p0}\left(\frac{T}{300}\right)^{2.3}}{1+\frac{N_D+N_A}{5\times10^{16}}} \quad \text{(s)} \quad (9.21)$$

9.4 Model Verification

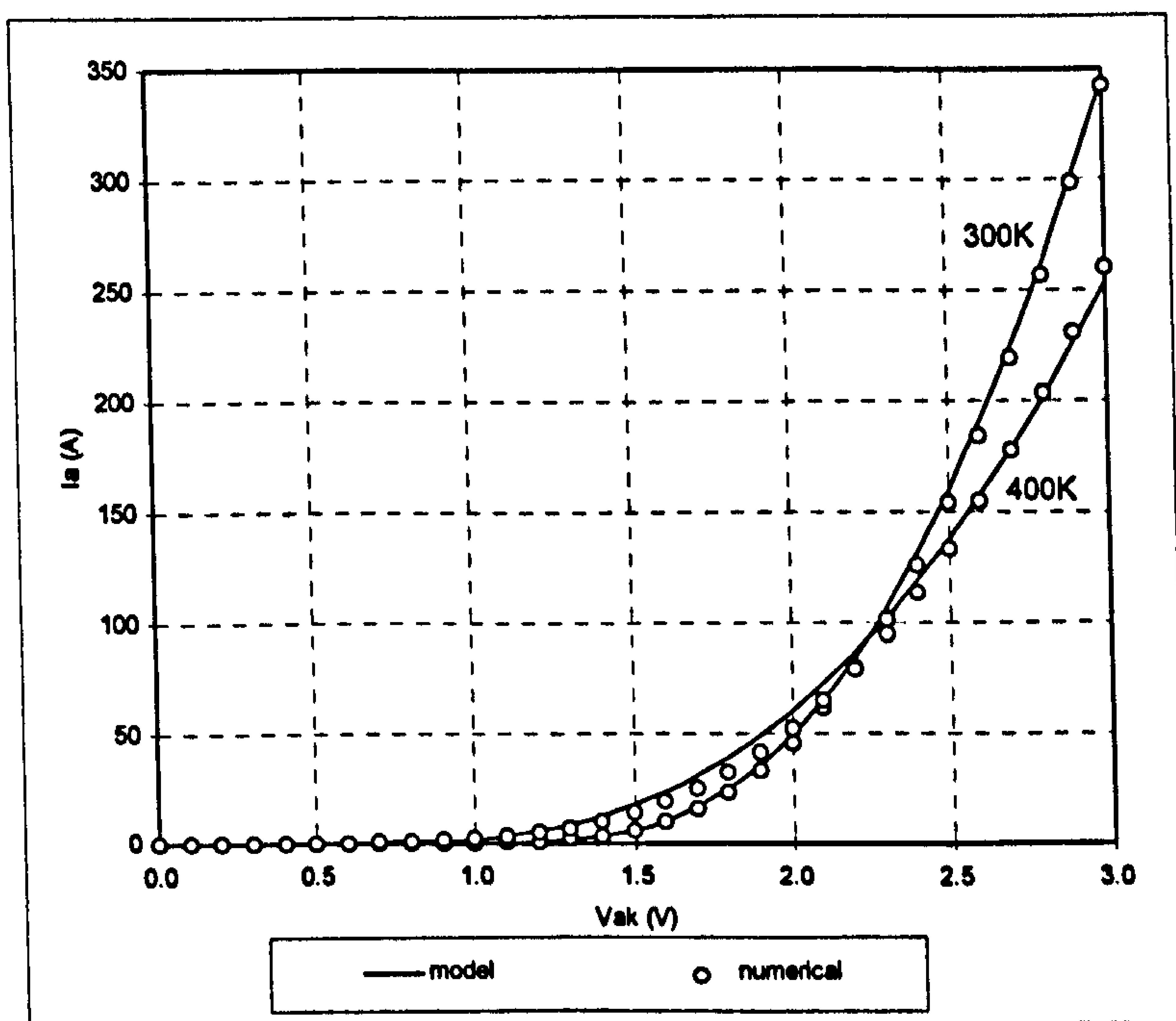
The SITh model is implemented as a subcircuit in PSpice where 21 parameters are needed in the model, including 6 for the NPN transistor. The temperature related parameters XTB and TRC1 are required to account for device temperature change. The complete PSpice model is given in Appendix B. In order to assess model accuracy, comparisons between model, numerical simulation and experiment results are performed.

9.4.1 Model Comparison with numerical simulation results

In Fig. 9.3 the numerical simulation [9.12] results of the static characteristics of a 2300 V SITh are presented. Some important model parameters are listed and defined, with typical values, in Table 9.1. The temperature is varied from 300 K to 400 K as indicated in Figure 9.3. The model simulation results fit well with the numerical simulation results, especially at high current densities. Despite carrier lifetime increase with temperature, the modulated base resistance increases due to reduced carrier mobilities. Hence at high current densities, the anode voltage at T=400 K is larger than at 300 K. At low current densities, the junction voltages V_{j1} and V_{j4}, which decrease with temperature due to the increasing intrinsic carrier concentration, are dominant components. As a result the anode voltage at 400 K is smaller than at 300 K.



(a)

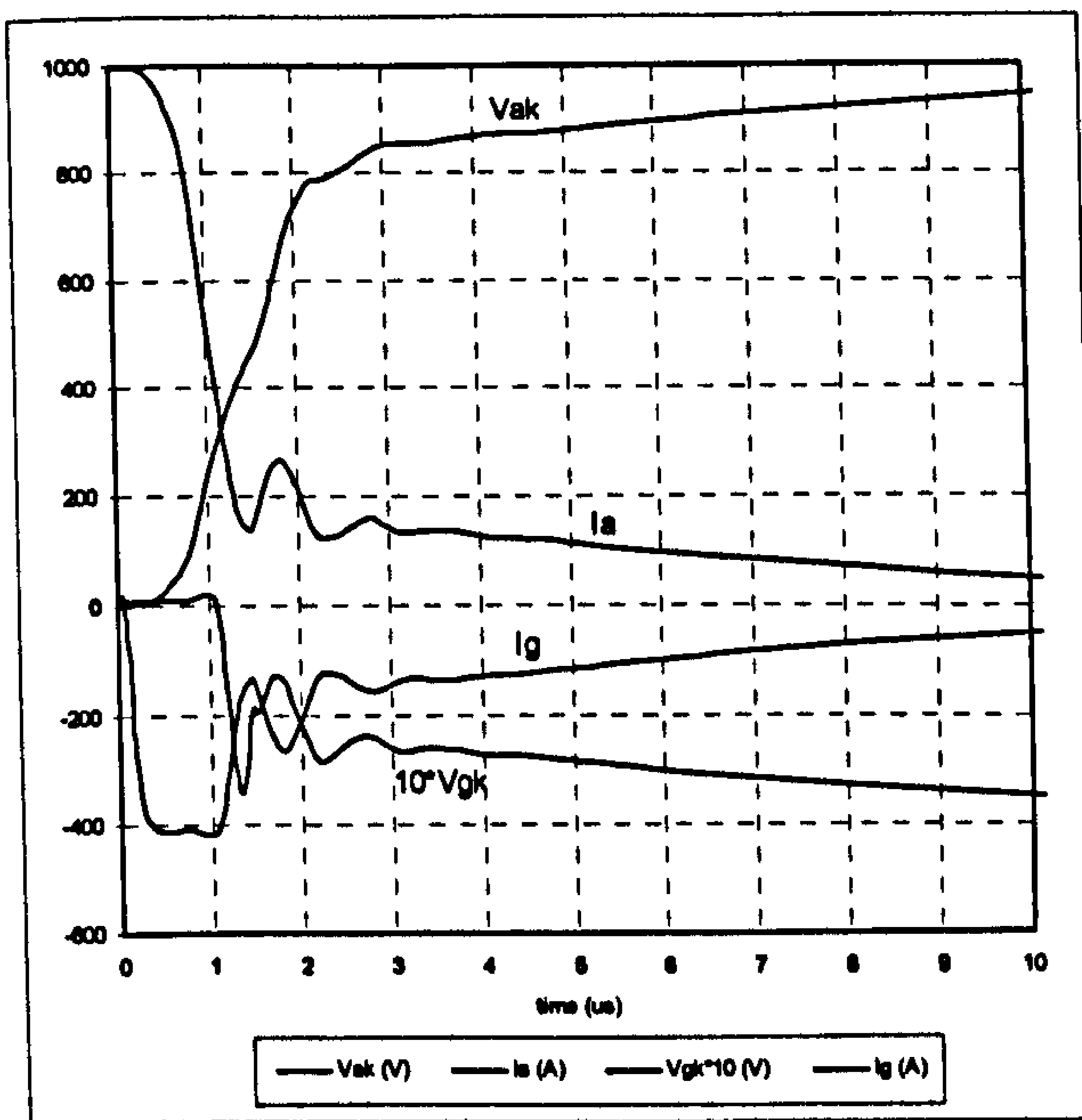


(b)

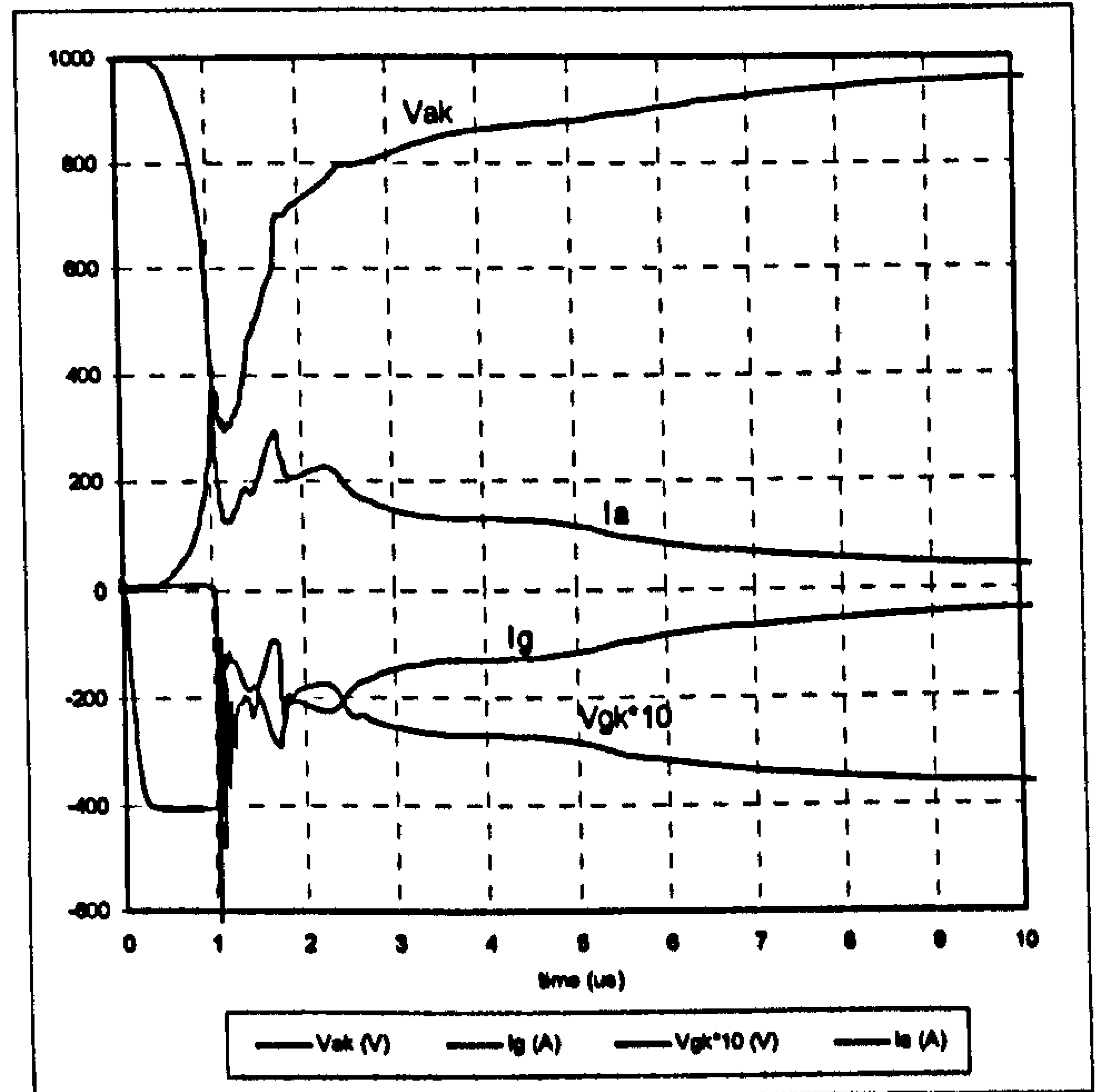
Figure 9.3 SITh on-state characteristics (a) τ_0=3μs and (b) τ_0=2μs

Table 9.1 Device Model Parameters

Symbol	TAUN	NB	NEPX	WB	HPRT	GAMMA	BETA
Definition	electron lifetime	base doping	N epi. doping	base width	h_p at 300K	coefficient for $h_p(T)$	Eqn. (9.17)
Typical Value	3	3.5×10^{13}	2×10^{14}	380	1.69×10^{-14}	-2	0.5
Unit	µs	cm^{-3}	cm^{-3}	µm			



(a)

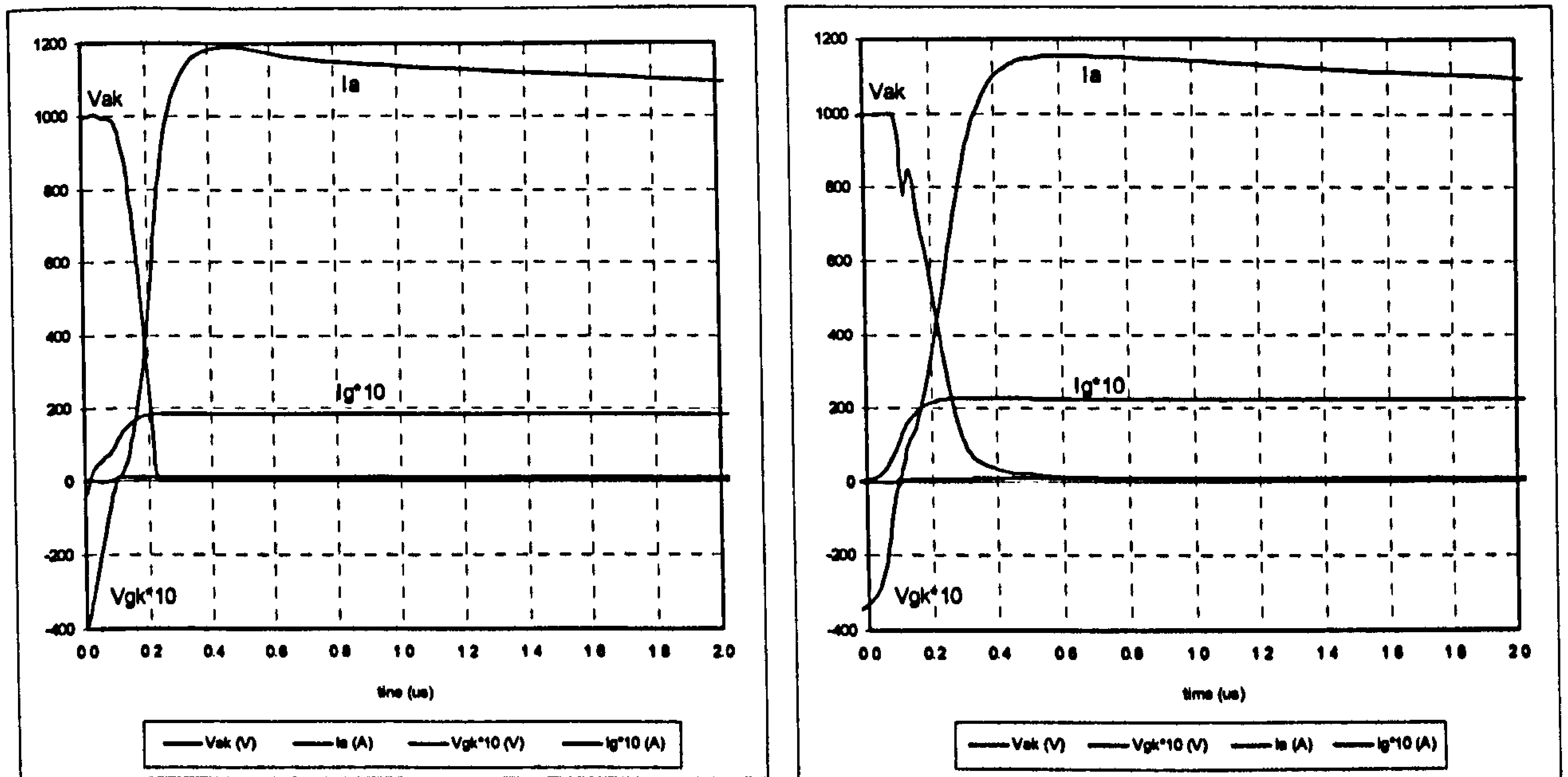


(b)

Figure 9.4 SITh snubbered turn-off characteristics with resistive load, T=300K, τ_0=3µs (a) model and (b) numerical

Figures 9.4 and 9.5 show the switching characteristics of the device at 300 K with a resistive load and an RCD turn-off snubber. The operation current density is 100 A/cm^2. The DC rail voltage is 1 kV and the load resistance is 1 Ω. The snubber resistance and capacitance are 5 Ω and 0.5 µF respectively. As shown, the anode voltage rises slowly during turn-off because the accumulated excess charge must be swept to the narrowed quasi-neutral base and decay. In both simulations, the gate voltage begins to fall after 1 µs. The anode current decays slowly, still having a value of 40 A after 10 µs. During turn-on,

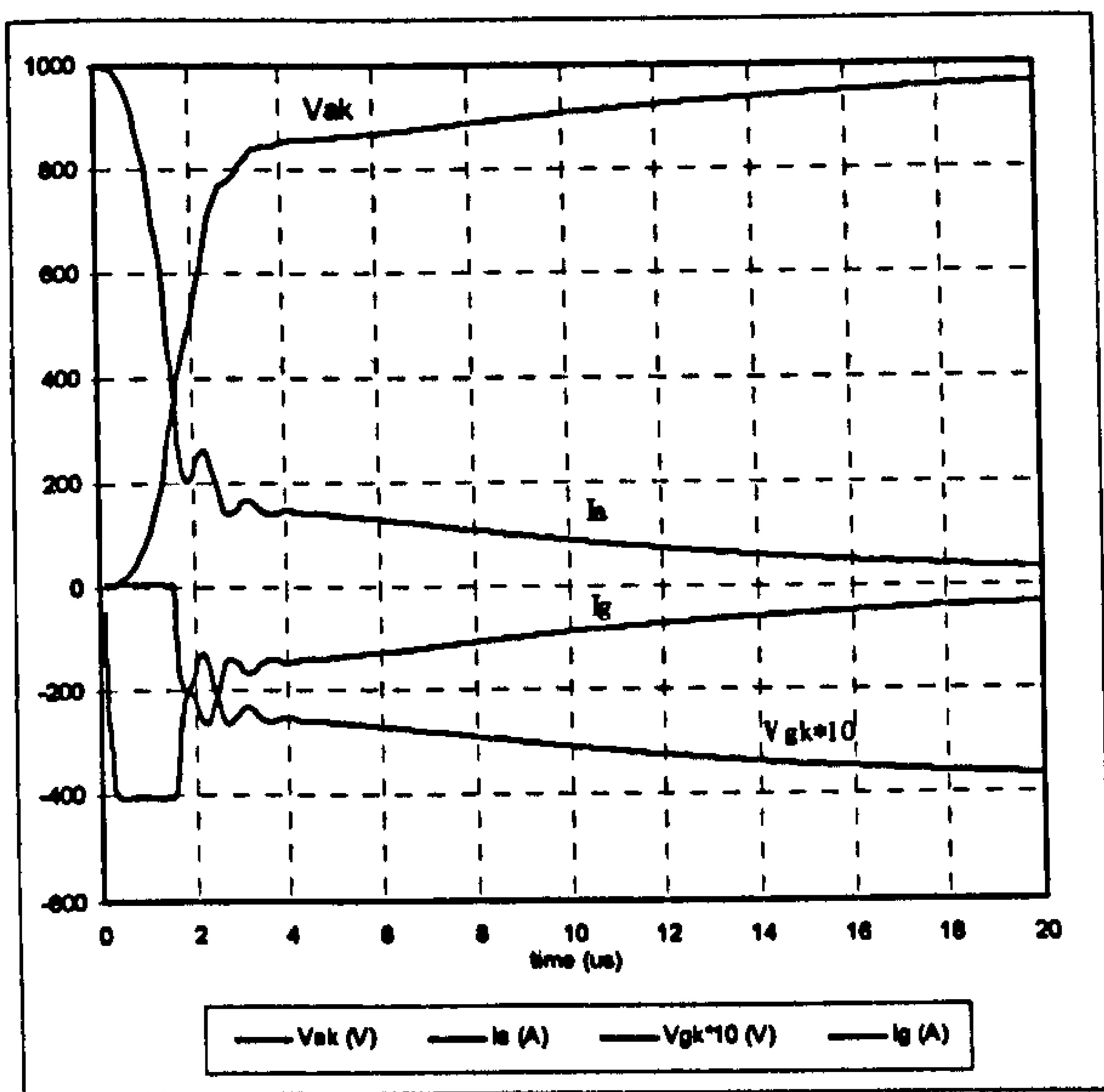
the anode voltage falls rapidly. It takes 250 ns to turn on the device. The exponentially decaying anode current after the anode voltage reaches its static value is attributed to the existence of the snubber capacitor. The simulation turn-off results in Figure 9.6 are at 400K. The gate voltage begins to fall after 1.6 μs and the current tail is 100 A at 10 μs.



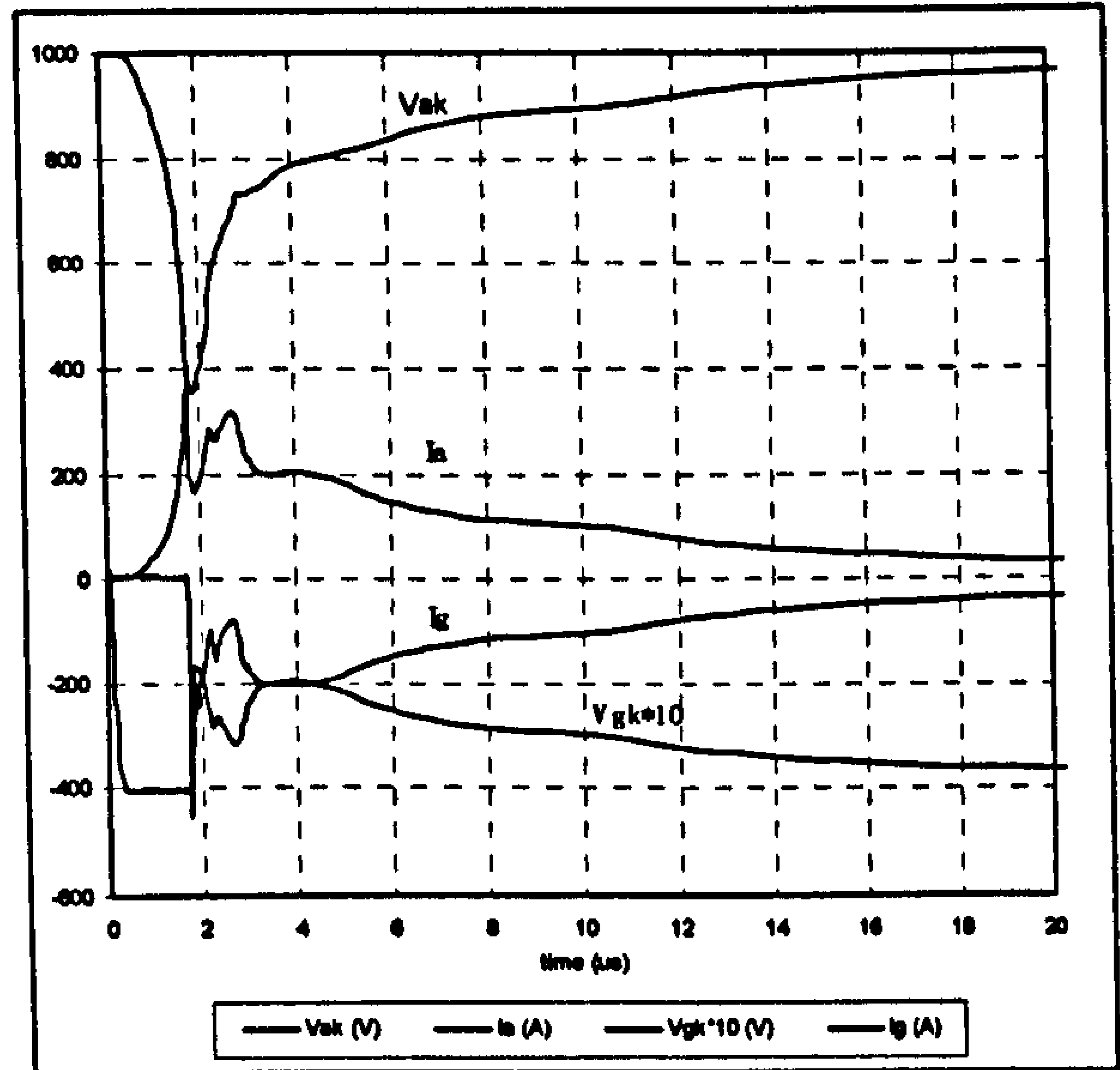
(a) (b)

Figure 9.5 SITh snubbered turn-on characteristics with resistive load, T=300K, τ_0=3μs (a) model and (b) numerical

In power electronics applications, the typical load is an inductive load. Fig. 9.7 shows a fast SITh (600V) snubberless turn-off characteristics with an inductive load. The operation current density is 100 A/cm^2. The DC rail voltage and the load current are 300 V and 300 A respectively. The DC rail voltage must be reduced significantly when a SITh is operating snubberlessly due to the resultant decrease in device SOA. The parasistic inductances in the circuit are minimized to reduce voltage overshoot. It takes 50 ns and 125 ns to turn off the current at 300 K and 400 K respectively.



(a)



(b)

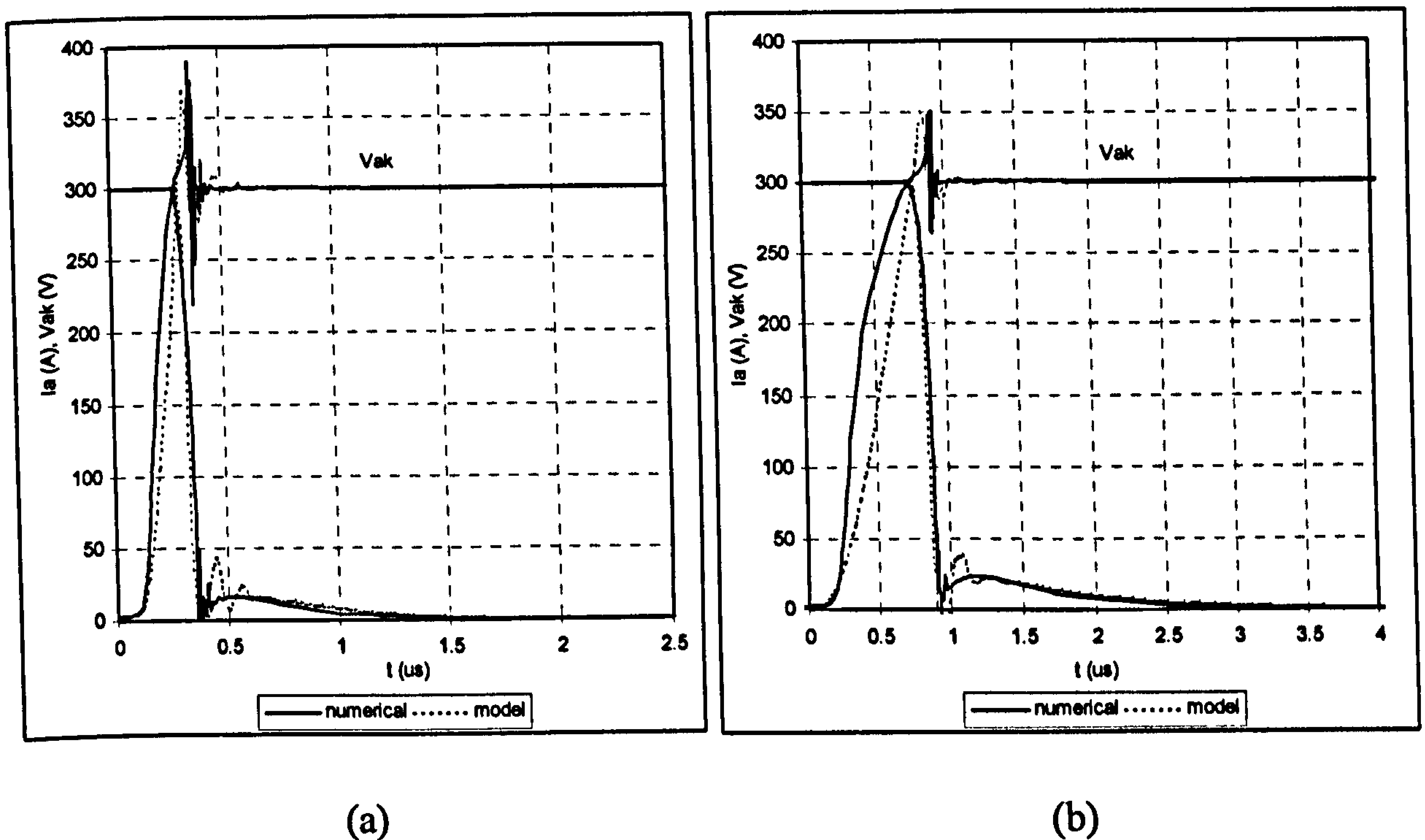
Figure 9.6 SITh snubbered turn-off characteristics with resistive load, T=400K, τ_0=3μs
(a) model and (b) numerical

The model results fit well with the numerical simulation results. The model also has good convergence and a fast simulation speed. With PSpice, it takes 1 second to simulate a turn-off switching cycle with a Pentium Pro 200 PC.

9.4.2 Model Comparisons with Experimental Results

Comparisons of the PSpice simulation and experiment results [9.2] of the device static and dynamic characteristics are presented in Figures 9.8 to 9.10. The base width and the resistivity are 390 μm, 100 Ω·cm for device A and 300 μm, 150 Ω·cm for device B. Device A has on-state anode voltages of 1.5 V and 2.6 V at 300 A and 900 A, while device B has anode voltages of 1.8 V and 3.2 V at the same two currents (Figure 9.8). Both devices have a near zero anode voltage temperature coefficient for the typical operating current range. Figures 9.9 and 9.10 show device snubbered turn-off characteristics with a resistive load. When switched off, device B has a shorter turn-off time than A. Due to the existence of parasitic inductances in the snubber, a voltage spike occurs during the anode voltage rising stage. Device B has a larger voltage spike than A, induced by its faster

switching speed. Device A has a delay time of 2.5 μs and the voltage spike occurs at 3.3 μs. The current tail is 30 A at 10 μs and about 5 A at 20 μs. For device B, the delay time is 2 μs and the voltage spike occurs at 2.7 μs. Its current tail disappears quicker than device A; being zero at 20 μs. In Figure 9.11 the PSpice simulation and experiment results [9.4] of device forward blocking characteristics are compared. The device can block 2.3 kV with a gate bias of 5 V. As shown, the PSpice simulation results are in good agreement with the experiment results.



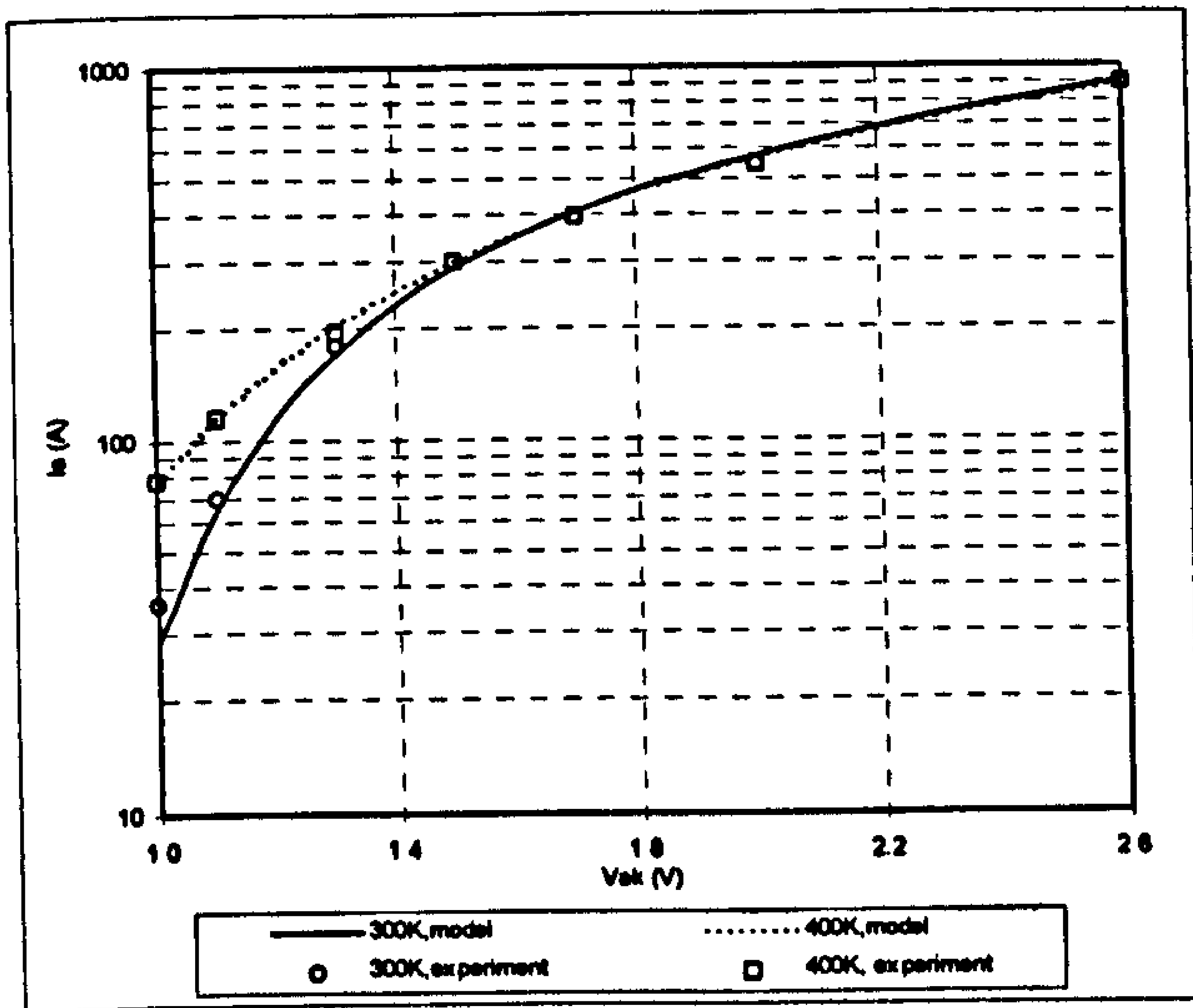
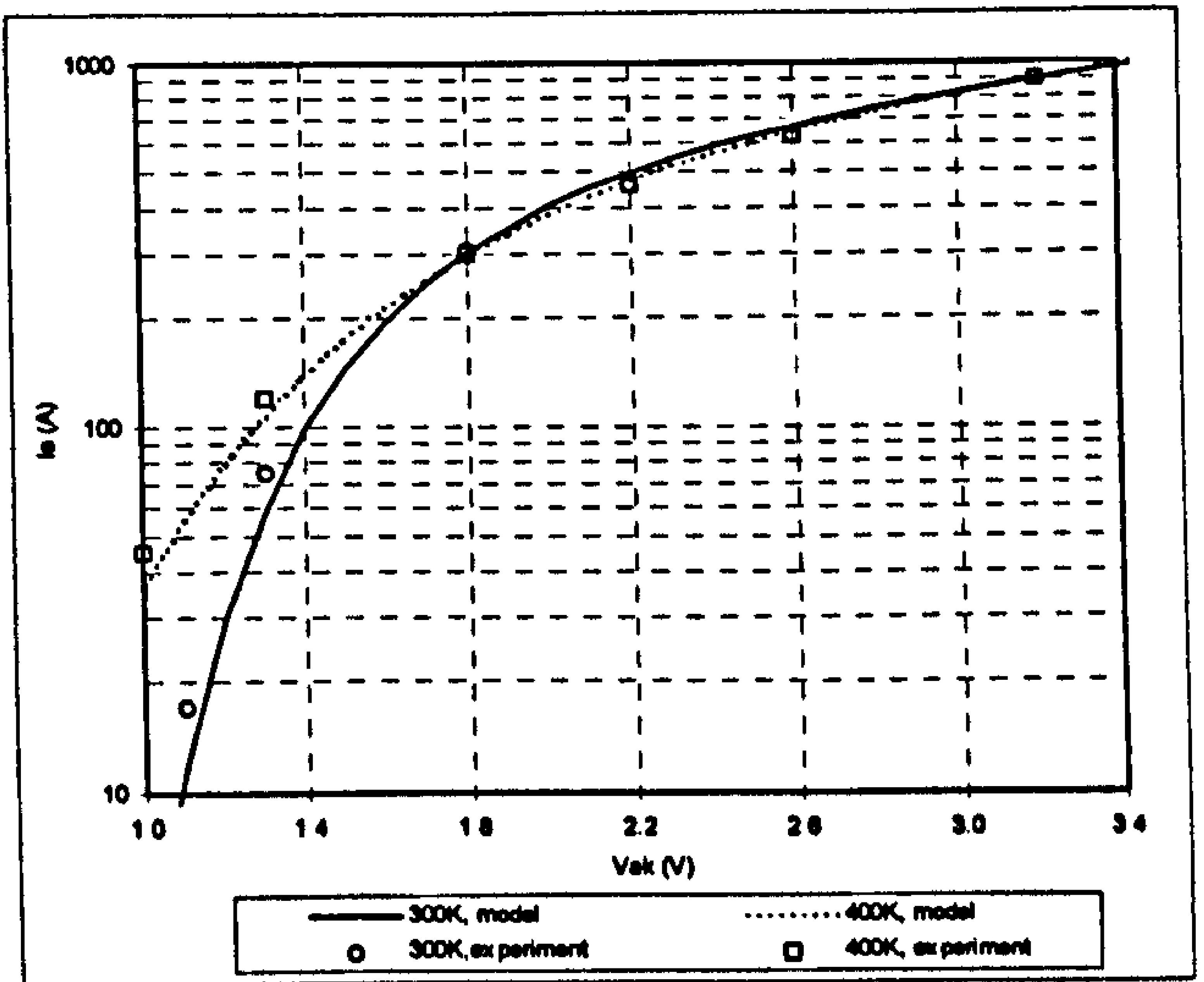
(a) (b)

Figure 9.7 SITh snubberless turn-off characteristics with inductive load, T= (a) 300 K (b) 400 K

9.5 Conclusion

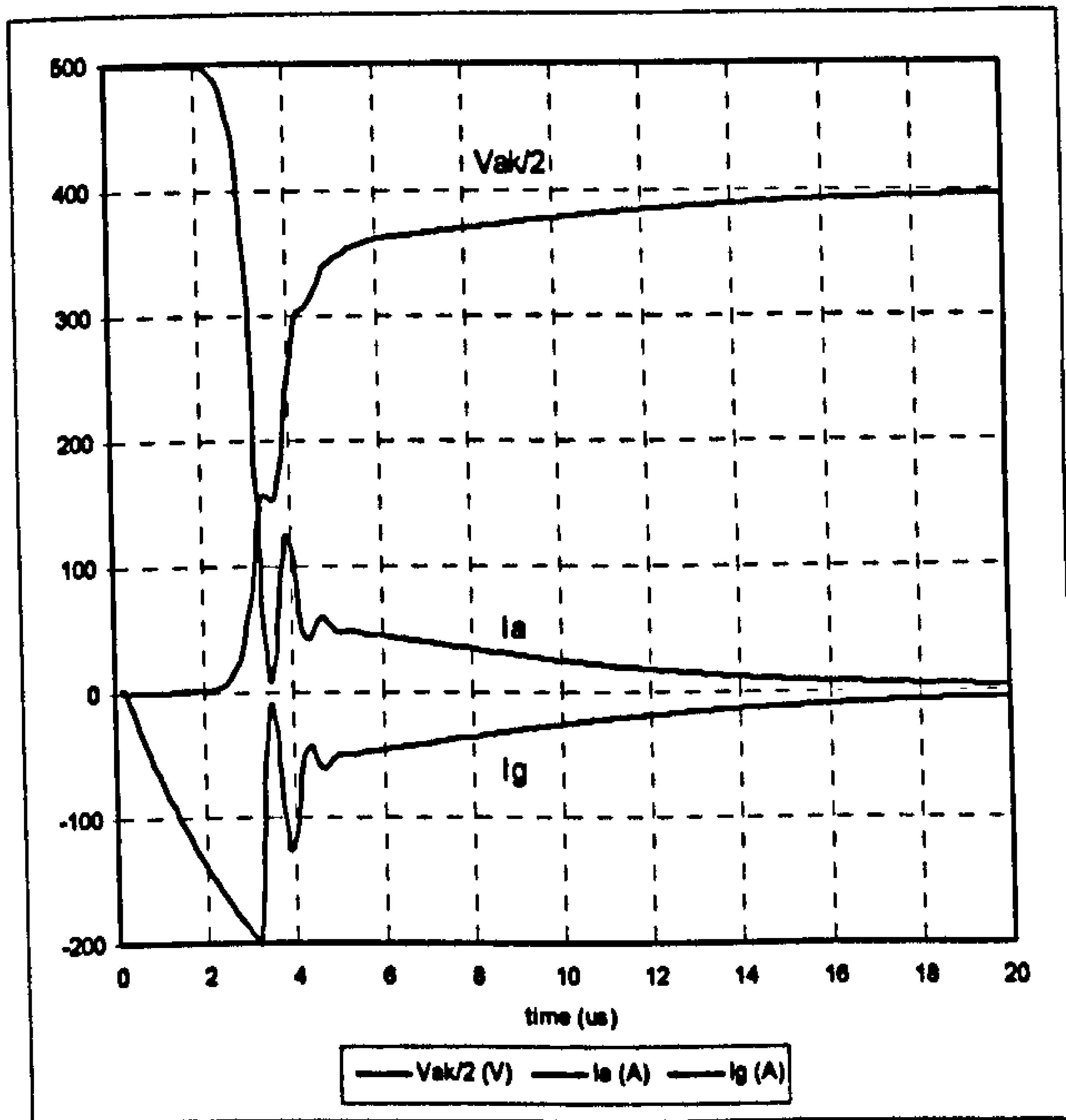
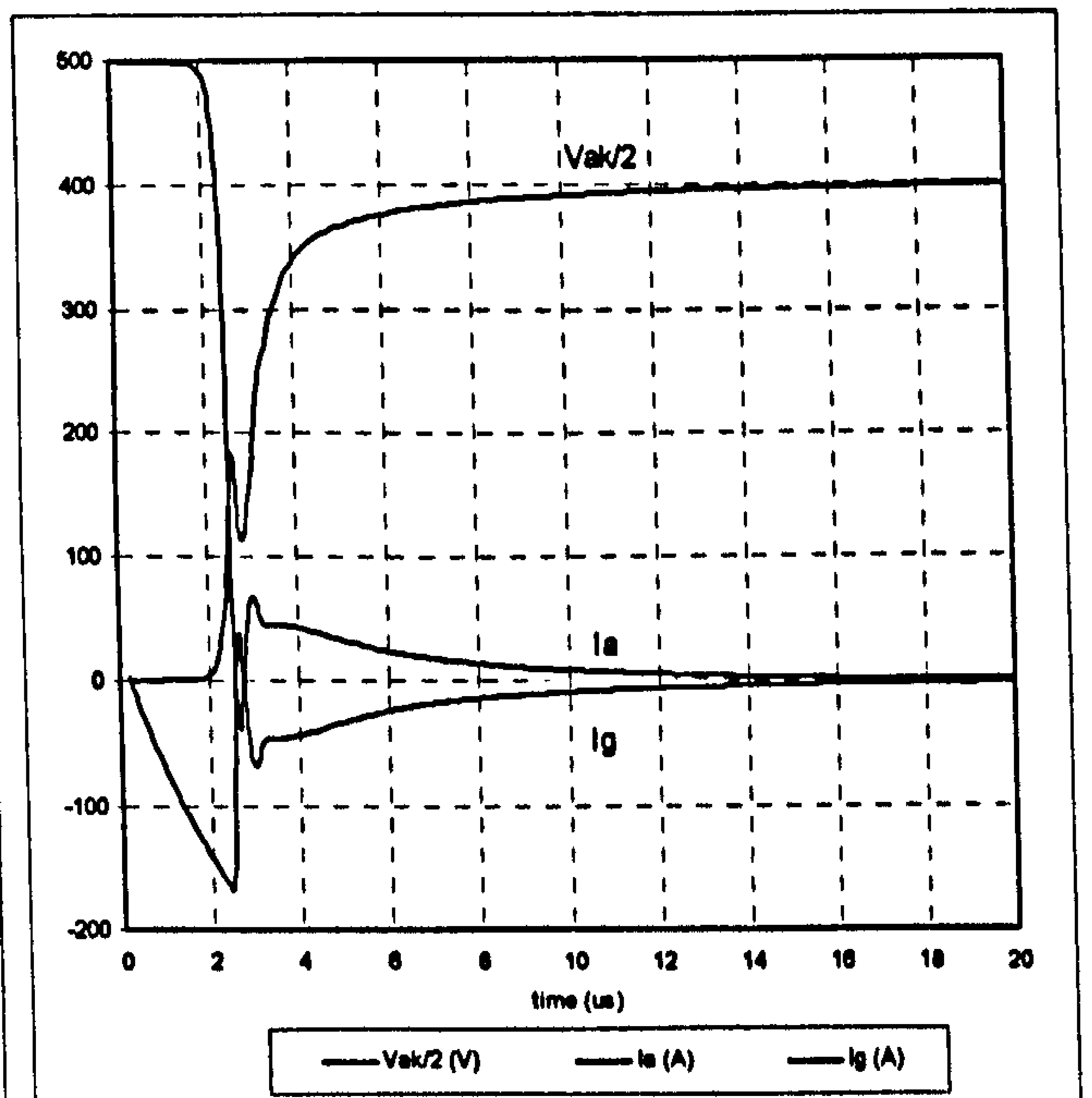
In this paper, an analytical Static Induction Thyristor (SITh) model is proposed based on device internal physics operating mechanisms. The non quasi-static model predicts both device static and dynamic characteristics. The model accounts for effects of device structure, lifetime and temperature. Implemented in PSpice as a subcircuit, model simulation results are compared with numerical simulation and experimental results for

various electrical and thermal conditions. The model exhibits accurate results, good convergence and fast simulation speed. The model is appropriate to both Si and SiC technologies.

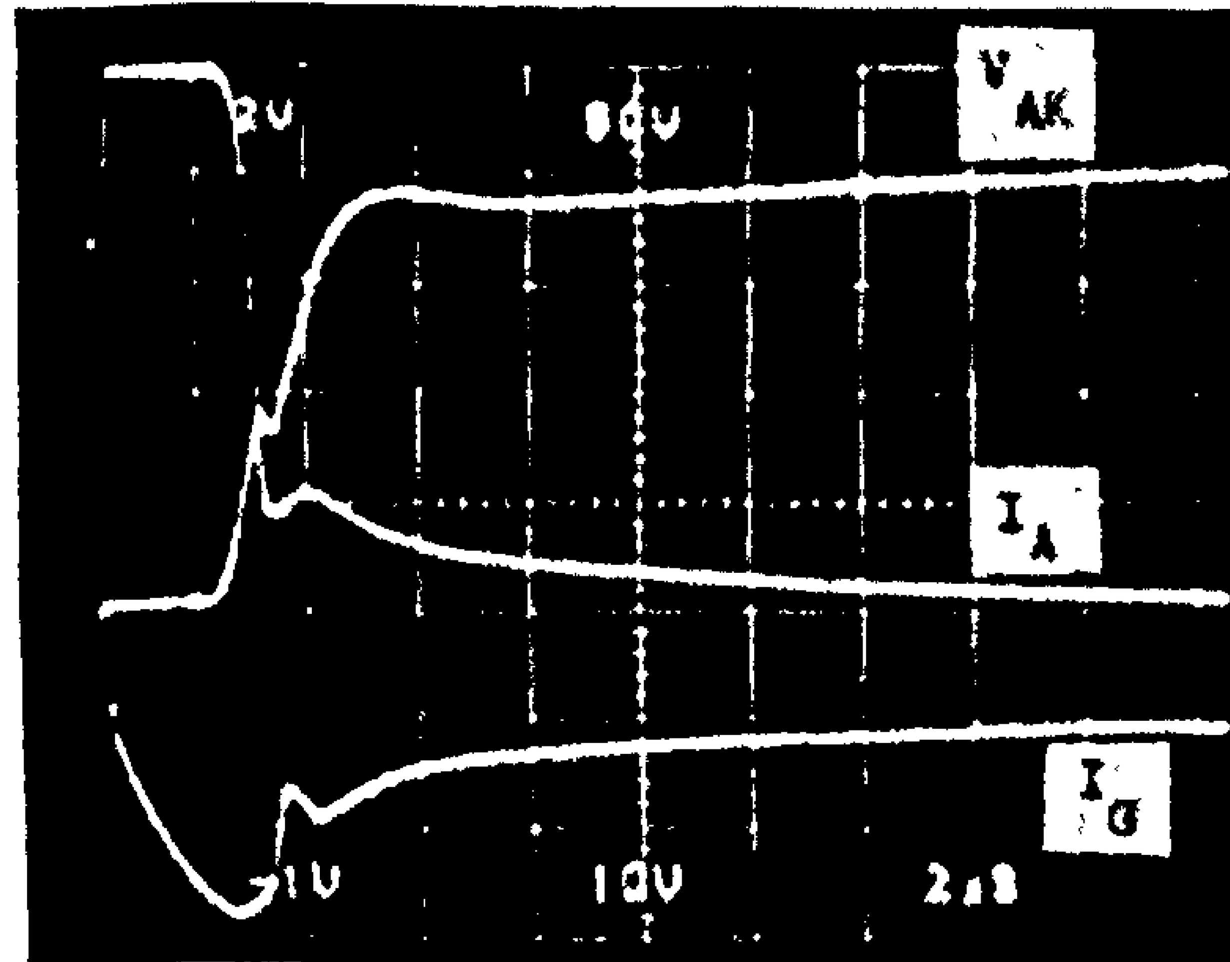
(a) (b)

Figure 9.8 SITh on-state characteristics [9.2] (a) device A and (b) device B

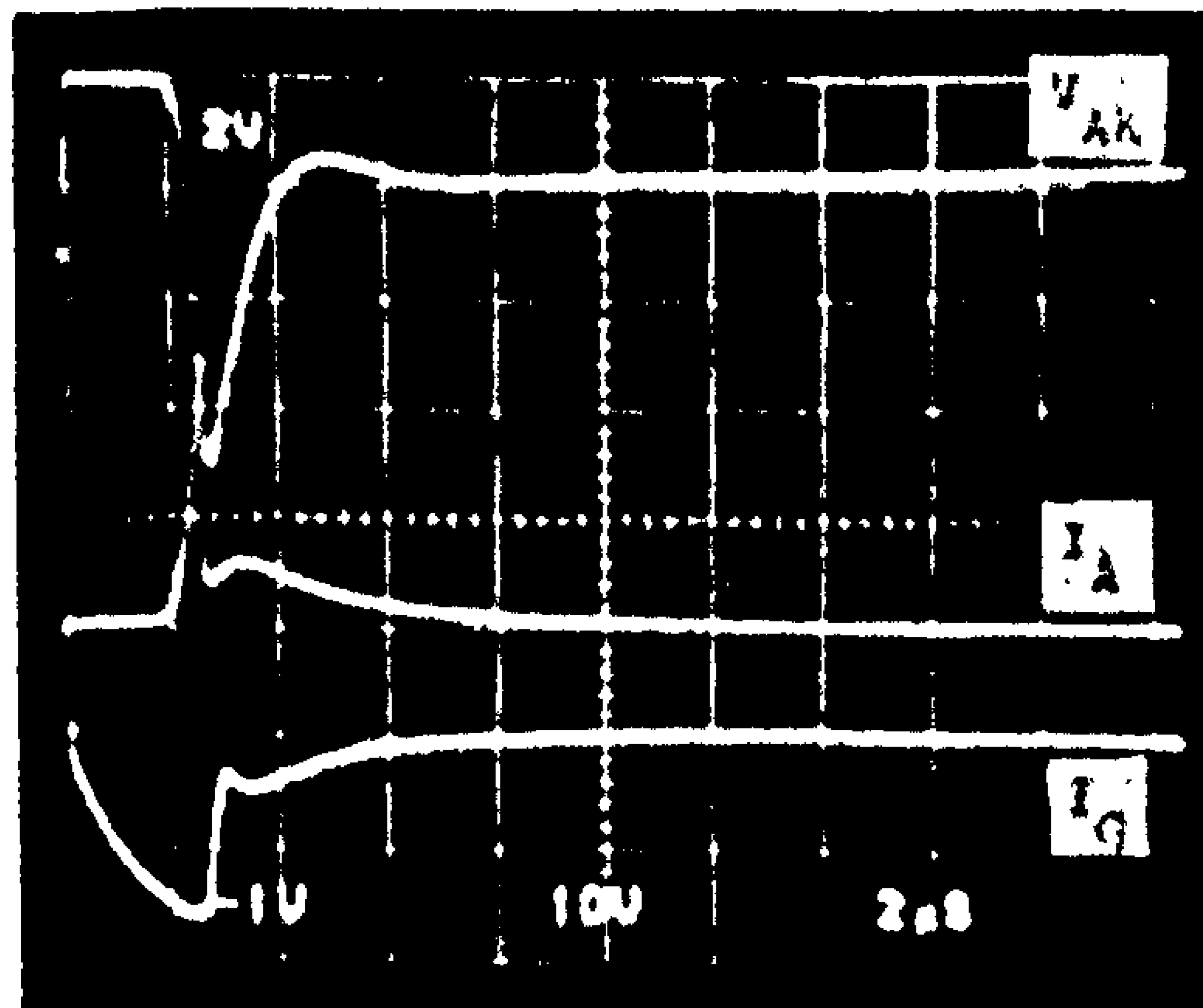



(a) (b)

Figure 9.9 SITh model simulation results of device snubbered turn-off characteristics with resistive load [9.2], (a) device A and (b) device B



(a)



(b)

Figure 9.10 Experimental results of SITh snubbered turn-off characteristics with resistive load [9.2] (a) device A and (b) device B
V_{ak}: 200V/div; I_a: 100A/div; I_g: 100 A/div; hor: 2μs/div

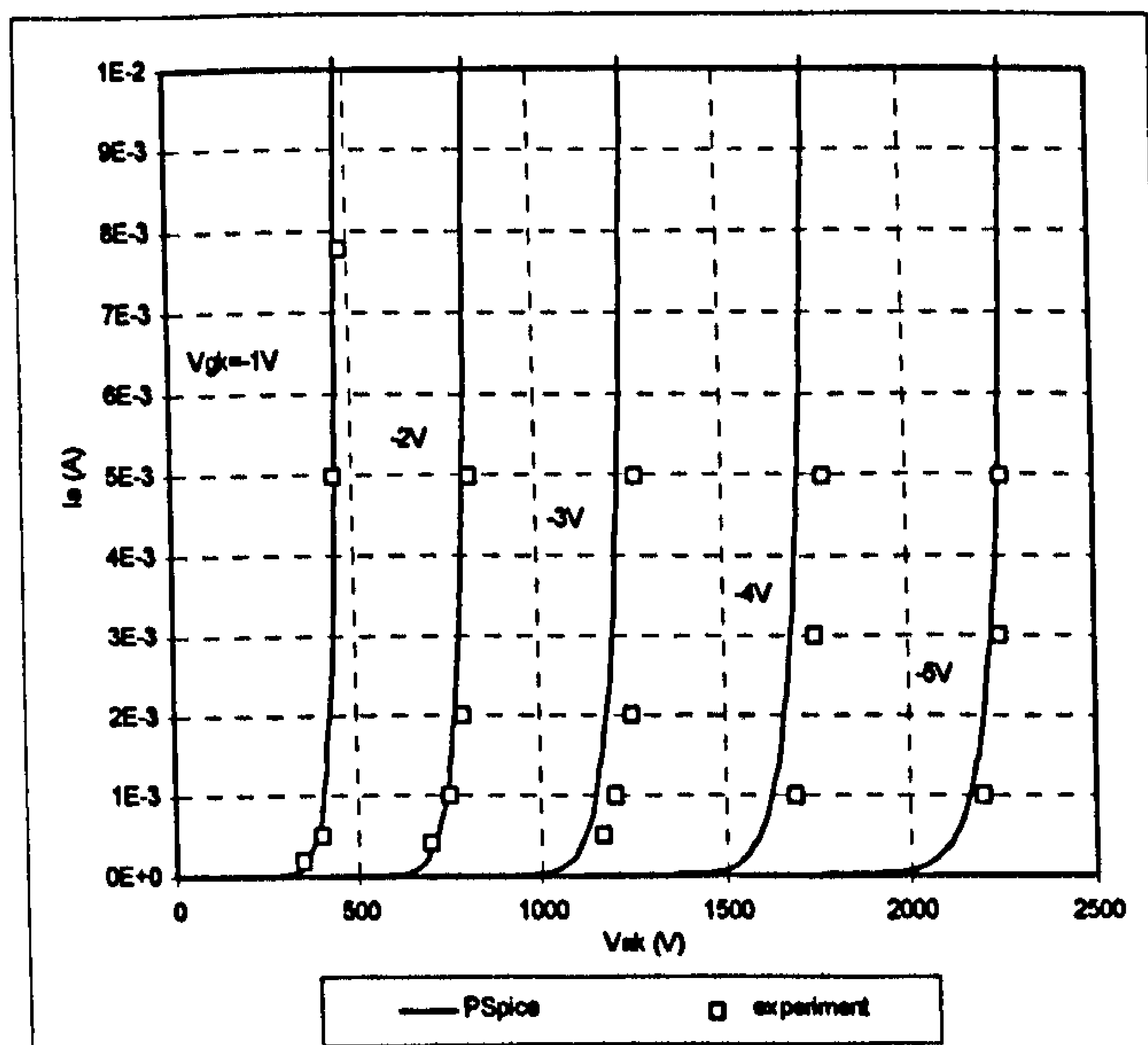


Figure 9.11 Comparison of PSpice simulation and experimental results [9.4] of device forward-blocking characteristics

Reference:

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CHAPTER 10

CONCLUSION

10.1 Concluding Remarks

In this thesis, various SiC devices (SBDs, PiN diodes, MOSFETs, IGBTs and BJTs) were numerically simulated and investigated. Compared with their Si counterparts, they offer better electrical and thermal performance.

It was found that the boundary between the PiN diode being better than the Schottky diode, is above 3 kV and 400 K. The current handling ability of 4H-SiC PiN diodes is better than 6H-SiC PiN diodes, while the switching loss is slightly larger. The substrate series resistances of PiN diodes dominate device on-state resistances, below 12 kV and 10 kV for 4H-SiC and 6H-SiC respectively. After deriving an analytical closed-form expression for 6H-SiC punch-through limited breakdown voltage, an optimum design with minimum base region specific on-state resistance was obtained.

In terms of the insulator reliability, the performance of UMOSFETs is severely hampered, but is superior to Si UMOSFETs. It was shown that decreasing the gate oxide overlap over the N^- drift region and increasing the trench bottom thickness enhances the insulator premature breakdown limited blocking voltage.

The current gain problem of the BJT is greatly alleviated because of the superior properties of SiC. It was found that the NPN BJT is better than the PNP BJT with SiC technology. The BJT has better current handling ability than, and comparable switching speed to, the corresponding 4H-SiC UMOSFET. Considering the relative ease of fabricating a SiC BJT, it is a more suitable candidate than the SiC MOSFET for high voltage (1 kV to 4 kV), high current and high frequency applications in the near future.

Incomplete ionization has significant impact on the performance of SiC devices. The IGBT on-state voltage has small negative temperature dependence at typical operating current densities, while SiC SIThs and GTOs have increased operating current densities at elevated temperature. This on-state voltage negative temperature dependence is not desirable for ensuring current sharing between parallel-connected devices or on large area devices.

Due to the relatively higher ionization energies of acceptors than donors in SiC, the 4H-SiC N-channel TIGBT is not suitable for applications at 300 K-400 K and the P-channel IGBT is a better choice. The multiple implantation technology used to fabricate the base region in DMOS lateral channel IGBTs results in improved device performance. However, the current handling ability of MI IGBTs can not compete with that of TIGBTs in the high operating current density range.

The electrical performance of 4H-SiC switching devices from 1 kV to 10 kV was evaluated systematically. Below 5 kV, SiC MOSFETs and BJTs show better current handling ability than other devices. Above 4 kV, SiC IGBTs are the best choice because they are easy to use and reliable, although their current handling ability is not as attractive as with SIThs and GTOs. The latter has properties not favourable in application due to the relatively large dopant ionization energies in SiC.

Two power PiN diode models were implemented in PSpice. Although 'Model I' is more accurately than 'Model II', its relative poor convergence makes it less usable. A 6H-SiC diode model was also developed and exhibits good agreement with numerical simulation results. A new, simple voltage-controlled switch for PSpice was proposed to improve simulation speed and convergence. An analytical Static Induction Thyristor (SITh) model, based on device internal physics operating mechanisms, was also proposed. The non quasi-static model predicts accurately both static and dynamic device characteristics.

The model exhibits good convergence and fast simulation speed. The model can be used for both Si and SiC devices.

10.2 Contribution by the Author

(i) In this thesis, various device structures were investigated, each with specified models and parameters appropriate to the new material, SiC. Valuable and quantitative information has been obtained, providing guidelines and reference work for future SiC research activities. Interesting phenomena were uncovered from the unique properties of SiC (relatively large ionization energies, high built-in junction voltage, extremely low impurity diffusion coefficient at temperatures when a good surface morphology can be maintained, etc.). These include: the superiority of devices (IGBTs, SIThs, GTOs) with N^+ substrates, as opposed to P^+ substrates counterparts (corresponding Si devices normally use P^+ substrates), large negative on-state voltage temperature dependence of SIThs and GTOs, high SITh on-state voltages and GTO holding current level at room temperature, poor gate turn-off capability of SIThs, etc.

(ii) The non punch-through breakdown voltages versus base doping boundary for UMOSFETs was redrawn, when taking insulator reliability into account. The potential of Bipolar Junction Transistors (BJTs) as an attractive option for SiC devices was uncovered. The best device type for a specific application range was determined by device performance comparison.

(iii) An analytical closed-form solution for 6H-SiC punch through limited breakdown voltage, which can be used to design device base region doping and width with minimum specific on-state resistances and soft recovery PiN diodes, was derived for the first time.

(iv) An accurate analytical 6H-SiC PiN diode model was developed. It was found that Si device models can generally be extended to SiC, but more severe convergence problems are encountered due to the extremely low intrinsic carrier concentration.

(v) Two power PiN diode analytical models were modified and implemented in Pspice. A simple voltage-controlled switch model was presented, which can be used to simulate high order circuits and implement complex equations into a circuit.

(vi) A novel Static Induction Thyristor (SITh) model was proposed, implemented and verified. It has proven useful for computer-aided design of power electronics circuits employing SITHs.

10.3 Suggestions for Future Research

Although the development of SiC device technology has experienced rapid progress in the past few years and several SiC devices have been demonstrated, it was revealed in this thesis that the device performance is not as good as theoretically projected due to many unique properties of the material. However, SiC devices are still superior to their Si counterparts. Replacement of high voltage Si diodes by SiC diodes in power device modules will be realised when large area SiC wafers are available. To demonstrate the potential of SiC devices, the SiC BJT is a promising option in the near future.

The largest SiC impediment encountered is in MOS technology. The poor MOS oxide quality and premature insulator breakdown have prevented the SiC MOSFET from fulfilling its potential. More fundamental research work should be devoted to the MOS channel physics and chemistry. Efforts to bypass this area have proven ineffective.

SiC devices operate at temperatures up to 800 K because of the excellent stability of SiC at high temperature. Nevertheless, current packaging and metal contact materials can not withstand such high temperatures. These constrains may limit the full potential of

SiC. Research seeking new metals and packaging materials that match the superior properties of SiC, is required.

Numerical simulation is a powerful tool for designing devices and understanding device physics. In Chapter two, physical models and material parameters used in numerical simulations are illustrated. Although 4H-SiC is widely used for fabricating power devices, many of the parameters used are taken from 6H-SiC or Si because no such data for 4H-SiC has been reported. Measurements and studies of SiC material parameters and physical models (e.g., channel mobility model) should be carried out so that devices can be modelled more accurately.

It was found that the extremely low SiC intrinsic carrier concentration at low temperatures (room temperature included) introduces convergence problems in numerical and analytical simulations. Special algorithms should be developed to solve this problem, therein achieving an efficient simulation methodology.

Appendix A

PiN Diode Model Subcircuit netlist (Chapter 8)

Model I

```
*MATHEMATICS FUNCTION DEFINITION
.SUBCKT PIN2_6 8 16
.FUNC NNEG(X) (ABS(X)+X)/2
.FUNC SINHH(X) (EXP(X)-EXP(-X))/2
.FUNC COSHH(X) (EXP(X)+EXP(-X))/2
.FUNC TANHH(X) (EXP(X)-EXP(-X))/(EXP(X)+EXP(-X))

*PHYSICAL PARAMETER AND MATHEMATICS CONSTANT DEFINITION

*PARAMETERS GIVEN BY THE USER
.PARAM TAUN=0.4E-7 TAUP={TAUN} A={0.557*0.2} NB=0.4E14 NSUB=1E20 NEMI=1E17 WB=60E-
4 WEMI=10E-4 WSUB=120E-4 BV=600 ISS=2E-8 ISS1=1E-7 NEND=0.97 N0=3E16

*PARAMETERS CALCULATED AUTOMATICALLY
+TAUHL={(TAUP+TAUN)*PWR(T/300,2.3)} EPI=11.8 EPIS={EPI*8.85E-6} VTT={8.62E-5*T}
Q=1.6E-19 DELQ=1.6E-14 PI=3.1415927 TAULNEMI={TAUN/(1+NEMI/5E16)*PWR(T/300,2.3)}
TAULPSUB={TAUP/(1+NSUB/5E16)*PWR(T/300,2.3)}
EG={1.08-4.73*1E-4*T*T/(T+636)} VSAT={2.32E7/(1+0.8*EXP(T/600))}
NI={1.71E19*EXP(-EG/2/VTT)*PWR(T/300,1.5)} SQRNI={NI*NI/1E13} H={WB/2}
MUNB={55.24+(1425*PWR(T/300,-2.3)-55.24)/(1+PWR(T/300,-3.8)*PWR((NB/1.072E17),0.73))}
MUPB={49.7+(479.37*PWR(T/300,-2.2)-49.7)/(1+PWR(T/300,-3.7)*PWR((NB/1.606E17),0.7))}
MUNEMI={55.24+(1425*PWR(T/300,-2.3)-55.24)/(1+PWR(T/300,-3.8)*PWR((NEMI/1.072E17),0.73))}
MUPSUB={49.7+(479.37*PWR(T/300,-2.2)-49.7)/(1+PWR(T/300,-3.7)*PWR((NSUB/1.606E17),0.7))}
MUNSUB={55.24+(1425*PWR(T/300,-2.3)-55.24)/(1+PWR(T/300,-3.8)*PWR((NSUB/1.072E17),0.73))}
DA={2*VTT*MUNB*MUPB/(MUNB+MUPB)} LA={PWR((DA*TAUHL),0.5)}
DNEMI={VTT*MUNEMI} LNEMI={PWR((DNEMI*TAULNEMI),0.5)}
DPSUB={VTT*MUPSUB}LPSUB={PWR((DPSUB*TAULPSUB),0.5)}
DPB={VTT*MUPB} K={H/LA}SQRK={K*K}
HP1={1E13*DNEMI/LNEMI/TANHH(WEMI/LNEMI)/NEMI}
HP2={1E13*LNEMI*TANHH(WEMI/2/LNEMI)/TAULNEMI/NEMI}
HN1={1E13*DPSUB/LPSUB/TANHH(WSUB/LPSUB)/NSUB}
HN2={1E13*LPSUB*TANHH(WSUB/2/LPSUB)/TAULPSUB/NSUB}
HP={HP1+HP2} HN={HN1+HN2} B={MUNB/MUPB}

*CIRCUIT COMPONENT VALUE DEFINITION
```

```
.PARAM RM={H/DA*SINHH(K)/K} LM={H*TAUHL/2/DA*(COSHH(K)-SINHH(K)/K)}
R1={H/DA/SQRK*(1+SQRK/10)/(0.5+SQRK/120)} R2={H/DA*0.24*(1+SQRK/10)}
C1={H/12}C2={5/12*H/PWR((1+SQRK/10),2)}RB={H*1E5/A}
RSUB={WB/Q/1740/N0/A+WSUB/Q/A/NSUB/MUNSUB}

* PIN DIODE SUBCIRCUIT
RT 8 9 {RSUB}
EPIN 9 10 VALUE={V(3)+V(4)+V(5)+V(13)}
VS 10 16 0
GPIN 16 8 VALUE={ISS/(1-PWR(V(8,16)/BV,3))-ISS}
*GPIN 16 8 VALUE={ISS/(1-PWR(V(8,16)/BV,3))-ISS+SQRT(ABS(V(8,16)))*ISS1}

*BASE REGION CARRIER DISTRIBUTION
GL 0 1
+VALUE={B/(1+B)*I(VS)/1.6/A*1E6-HP*V(1)*V(1)}
GR 0 2
+VALUE={1/(1+B)*I(VS)/1.6/A*1E6-HN*V(2)*V(2)}

RA1 1 0 {R1}
CA1 1 0 {C1}
RB1 1 Y1 {R2}
CB1 Y1 0 {C2}

R11 1 Z1 {RM}
L11 Z1 15 {LM}

RA2 15 0 {R1}
CA2 15 0 {C1}
RB2 15 Y2 {R2}
CB2 Y2 0 {C2}

RA3 15 0 {R1}
CA3 15 0 {C1}
RB3 15 Y3 {R2}
CB3 Y3 0 {C2}

R12 15 Z2 {RM}
L12 Z2 2 {LM}

RA4 2 0 {R1}
```

```
CA4 2 0 {C1}
RB4 2 Y4 {R2}
CB4 Y4 0 {C2}

DS1 0 1 DP3
DS2 0 2 DP3

*P-i JUNCTION VOLTAGE
EL 3 0
+VALUE={VTT*LOG((NNEG(V(1))+CON1)*NB/SQRNI)}

*i-N+ JUNCTION VOLTAGE
ER 4 0
+VALUE={VTT*LOG(NNEG(V(2))*1E13/NB+1)}

*BASE VOLTAGE DROP
GB0 0 5
VALUE={I(VS)/DELQ/(MUNB*NB+1E13*(MUNB+MUPB)*((1-NEND)*ABS(V(1)+1E -
1)+NEND*V(15)))}
GB1 0 5
VALUE={I(VS)/DELQ/(MUNB*NB+1E13*(MUNB+MUPB)*(NEND*V(15)+(1-NEND)*ABS(V(2))))}
RD 5 0 {RB}

*REVERSE BIASED SPACE CHARGE REGION VOLTAGE DROP
GX1 0 22 VALUE={B/(1+B)*I(VS)*1E-3/(NNEG(V(15))+1E-3)/A/1.6}
CX1 22 0 1N
ESX1 22 23 VALUE={I(VSX)/PWR(NNEG(V(1))+1E-3,2)}
ESX2 23 24 VALUE={I(VSX)*PWR(V(12)+1E-1,2)}
VSX 24 0 0
RSX1 22 0 1E10
EX 12 0 VALUE={NNEG(-V(22)*1E4)}
RDEX 12 0 1
ESC 13 0 VALUE={(I(VS)/A/VSAT-Q*NB)/EPIS/2*PWR(V(12),2)}
.MODEL DP1 D(IS=1e-8 N=0.5)
.MODEL DP3 D(IS=1E-8 CJO=0.5P)
.ENDS
*End of model PIN2_6
```

Model II (Chapter 8)

```
.FUNC TANHH(X) (EXP(X)-EXP(-X))/(EXP(X)+EXP(-X))

*PHYSICAL AND STRUCTURE PARAMETERS DEFINED BY THE USER
.PARAM      WB=50E-4      NB=1.2E14      NEMI=1E17      WEMI=10E-4      A={0.557*1}
TAUU={0.1U*PWR(T/300,2.8)} XM=0.8E-2 IR=1E-6 VPT=600 N0=3E16 LAM=0.03

*PHYSICAL PARAMETERS CALCULATED AUTOMATICALLY
+EPIS=104.4E-14 Q=1.6E-19
+MUNB={55.24+(1425*PWR(T/300,-2.3)-55.24)/(1+PWR(T/300,-3.8)*PWR((NB/1.072E17),0.73))}
+MUPB={49.7+(479.37*PWR(T/300,-2.2)-49.7)/(1+PWR(T/300,-3.7)*PWR((NB/1.606E17),0.7))}
+MU0=1740 VSAT={2.32E7/(1+0.8*EXP(T/600))}
+VTT={8.62E-5*T} DA={2*VTT*MUNB*MUPB/(MUNB+MUPB)} B={MUNB/MUPB}
+MUNEMI={55.24+(1425*PWR(T/300,-2.3)-55.24)/(1+PWR(T/300,-3.8)*PWR((NEMI/1.072E17),0.73))}
+DNEMI={VTT*MUNEMI}
TAULNEMI={TAUU/2/(1+NEMI/5E16)*PWR(T/300,2.8)} LNEMI={PWR((DNEMI*TAULNEMI),0.5)}
+HP1={DNEMI/LNEMI/TANHH(WEMI/LNEMI)/NEMI}
+HP2={LNEMI*TANHH(WEMI/2/LNEMI)/TAULNEMI/NEMI}
+HP={HP1+HP2}

*CIRCUIT COMPONENT VALUE
.PARAM ISS=1.65e-10 NN=1.06 IKFF=3 PHI=1 IE={(1+B)*Q*A*XM*XM/B/TAUU/TAUU/HP}
+RLIM={WB/A/Q/N0/MU0} VM={WB*WB/MU0/TAUU} REPI={WB/Q/A/NB/MUNB}
+TO={XM*XM/DA} RSC={XM*XM/2/EPIS/A/VSAT} ALFA={TO/TAUU}
*+VM=0.12 REPI=8 TO=13u VPT=1200 RSC=18 LAM=30m ALFA={TO/TAUU}

REPI 10 12 {REPI}
RLIM 10 11 {RLIM}
GRMOD 11 12 VALUE={V(11,12)*((1-LAM)*V(2,3)+LAM*V(2))/VM}
GPIN 12 20 VALUE={I(VS2)}
RPIN 10 20 1E20
GAVL 20 10 VALUE={IR/(1-PWR(V(10,20)/VPT,3))-IR}
EJ 30 0 VALUE={V(12,20)}
VS1 30 31 0
DJ 31 0 DJ
.MODEL DJ D (IS={ISS}IKF={IKFF}N={NN})
E1 1 0 VALUE={I(VS1)}
VS2 1 2 0
EV7 7 0 TABLE {V(2)}=(0 0) (1E15 1E15)
GE 2 0 VALUE={PWR(V(7),2)/IE}
```

```
RP1 2 3 1
CP1 2 3 {TAUU}
EVS2 6 0 TABLE {-I(VS2)}=(0 0) (3E3 3E3)
GRS 3 0
VALUE={3*V(3)/ALFA/PWR(1-SQRT(ABS((PHI+V(20,12)))/(VPT+RSC*V(6))),2)}
RP2 3 4 5
CP2 3 4 {TAUU/5}
*RS3 4 0 {ALFA/7}
GRS3 4 0
VALUE={7*V(4)/ALFA/PWR(1-SQRT(ABS((PHI+V(20,12)))/(VPT+RSC*V(6))),2)}
RP4 4 5 9
CP4 4 5 {TAUU/9}
*RS5 5 0 {ALFA/11}
GRS5 5 0
VALUE={11*V(5)/ALFA/PWR(1-SQRT(ABS((PHI+V(20,12)))/(VPT+RSC*V(6))),2)}
.ENDS
*End of model PIN1_6
```

Appendix B

PSpice SITh Model Subcircuit netlist (Chapter 9)

```
*MATHEMATICAL FUNCTION DEFINITION
.FUNC ATAH(X) {X+PWR(X,3)/3+PWR(X,5)/5+PWR(X,7)/7}
.FUNC NNEG(X) {(ABS(X)+X)/2.0}
.FUNC NPOS(X) {(ABS(X)-X)/2.0}

* PARAMETERS GIVEN BY THE USER
.PARAM T=300 A=10 TAUN=3E-6 NB=3.5E13 NEPX=2E14 WB=380E-4 HPRT=1.69E-14 GAMMA=-2
VBI=1.2 BETA=0.5 I0=1E-9 N1=1.7E-2 N2=0.6 N3=0.27 ALPHA=3

*PARAMETERS CALCULATED AUTOMATICALLY
.PARAM EPIS=1.044E-12 VTT={8.62E-5*T} Q=1.6E-19 TAUHL={2*TAUN*PWR(T/300,2.3)}
+HP={HPRT*PWR(T/300, GAMMA)
+MUNB={55.24+(1425*PWR(T/300,-2.3)-55.24)/(1+PWR(T/300,-3.8)*PWR((NB/1.0+72E17),0.73))}
+MUPB={49.7+(479.37*PWR(T/300,-2.2)-49.7)/(1+PWR(T/300,-3.7)*PWR((NB/1.606E17),0.7))}
+MU0={MUNB+MUPB} IR={Q*A*PWR(WB,2)/(4*HP*PWR(TAUHL,2))}
+DA={2*VTT*MUNB*MUPB/(MUNB+MUPB)} LA={PWR((DA*TAUHL),0.5)}
+B={MUNB/MUPB} PB0={2.1E20/NB} RBASE={WB/A/(MU0*NB*Q)} ALP={PWR(WB/LA,2)}
+CJC0={SQRT(EPIS*Q*NB*0.5)} CJE0={SQRT(EPIS*Q*NEPX*0.5)}

.SUBCKT SITH ANODE GATE CATHODE
EQ0 3 0 VALUE={Q*1E14/TAUHL*A*V(WUD)*I(VE0)/2}
VSE 3 4 0
GEB 4 0 VALUE={PWR(V(3),2)/IR}
GR2 4 0 VALUE={V(4)*2/PWR(V(WUD),2)*PWR(LA,2)}
R1 4 5 1.5
C1 4 5 {TAUHL*2/3}
GR1 5 0 VALUE={V(5)*10/PWR(V(WUD),2)*PWR(LA,2)}
R5 1 0 1
C2 1 0 {TAUHL}
GR4 2 1 VALUE={V(2,1)*12/PWR(V(WUD),2)*PWR(LA,2)}
VSB 3 2 0
GEE 2 0 VALUE={PWR(V(3),2)/IR}

EWUD WUD 0 VALUE={WB-SQRT(2*EPIS*(VBI-V(GATE,GC))/(Q*NB))}
VW WUD WUD1 0
CW WUD1 0 100U
```

```
EP0 10 0 VALUE={V(ANODE,DRIFT)}
VE0 10 11 0
D1 11 0 DP0

EPW 12 0 VALUE={V(GATE,GC)}
VEW 12 13 0
D2 13 0 DPW

EFB 14 0
+VALUE={N1*PWR(NNEG(V(ANODE,CATHODE)),N2)-N3*NPOS(V(GATE,CATHODE))}
VFB 14 15 0
D3 15 0 DFB

EAB AB 0 VALUE={(I(VE0)-I(VEW))/SINH(WB/LA)}
EBB BB 0 VALUE={SQRT(PWR(I(VEW),2)+PWR(V(AB),2))}

GJ1 ANODE DRIFT VALUE={I(VSE)*(1+B)/B}
GBASE DRIFT GC
+VALUE={V(DRIFT,GC)*0.5*(Q*1E14*MU0)*A/LA*V(BB)/ATAH(V(BB)*TANH(WB/2/LA)/(I(VE
W)+V(AB)*TANH(WB/2/LA)))}
REPI DRIFT GC {RBASE}
GIPW GC GATE VALUE={I(VSE)*(1+B)/B-I(VSB)}
GR3 GATE GC VALUE={TAUHL*V(1)/ALPHA/WB*I(VW)*1E4}
QCHAN GC GATE GE PCHAN {A}
EJ3 GE CATHODE VALUE={V(GATE,GE)*BETA}
GBR ANODE CATHODE VALUE={I(VFB)}

.MODEL PCHAN NPN IS=300N NF=1.5 NR=1.38 XTB=10.9 TRC1=-4E-3 RC=3.4E-5 CJC={CJC0}
+CJE={CJE0}
.MODEL DP0 D IS={1E-14*PB0}
.MODEL DPW D IS={1E-14*PB0}
.MODEL DFB D IS={I0}

.ENDS
```

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(b) $\tau_{n0}=\tau_{p0}=0.02\mu s$, $N_{p+}=1\times10^{19}cm^{-3}$, T=300K

(c) T=440K, $\tau_{n0}=\tau_{p0}=0.02\mu s$, di/dt=3000A/$\mu$s

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Figure 9.11 Comparison of PSpice simulation and experimental results [9.4] of device forward-blocking characteristics

Table 9.1 Device Model Parameters

Appendix D

Publications by the Author

Journal Publications:

[1] J. Wang, B. W. Williams, "A Simulation study of high-voltage 4H-SiC IGBTs", Semiconductor Science & Technology, Institute of Physics, 1998, Vol. 13, pp. 806-815

[2] J. Wang, B. W. Williams, "Evaluation of high-voltage 4H-SiC switching devices", IEEE Trans. on Electron Devices, No. 3, Vol. 46, 1999, pp. 589-597

[3] J. Wang, B. W. Williams, "A new Static Induction Thyristor (SITh) analytical model", IEEE Trans. on Power Electronics, Vol. 14, No. 5, 1999, pp.866-876

[4] J. Wang, B. W. Williams, "The 4H-SiC NPN Power Bipolar Junction Transistor", Semiconductor Science & Technology, Institute of Physics, Vol. 14, 1999, pp. 1088-1097

Conference Publications:

[5] J. Wang, B. W. Williams, S. E. Madathil, M. M. Desouza, "Comparison of 5 kV 4H-SiC N-Channel and P-Channel IGBTs", International Conference on Silicon Carbide and Related Material'99, North Carolina, U.S.A., Oct. 10 - Oct. 15, 1999

[6] J. Wang, B. W. Williams, S. E. Madathil, M. M. Desouza, "A Closed-Form Analytical Solution of 6H-SiC Punch-Through PiN diode Breakdown Voltages", International Conference on Silicon Carbide and Related Material'99, North Carolina, U.S.A., Oct. 10 - Oct. 15, 1999

[7] J. Wang, B. W. Williams, S. E. Madathil, M. M. Desouza, "Analytical Modeling of 6H-SiC PiN Diode Reverse Recovery for Circuit Simulation", submitted to EPE-PEMC'2000