Clock-Feedthrough Compensation in MOS Sample-and-Hold Circuits

by

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A thesis submitted to the University of Plymouth in partial fulfilment of the requirement for the degree of

Doctor of Philosophy

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April 2001

Natur und Kunst, sie scheinen sich zu fliehen
Und haben sich, eh man es denkt, gefunden;
Der Widerwille ist auch mir verschwunden,
Und beide scheinen gleich mich anzuziehen.

Es gilt wohl nur ein redliches Bemühen!
Und wenn wir erst in abgemeßnen Stunden
Mit Geist und Fleiß uns an die Kunst gebunden,
Mag frei Natur im Herzen wieder glühen.

So ists mit aller Bildung auch beschaffen:
Vergebens werden ungebundne Geister
Nach der Vollendung reiner Höhe streben.

Wer Großes will, muß sich zusammenraffen;
In der Beschränkung zeigt sich erst der Meister,
Und das Gesetz nur kann uns Freiheit geben.

Johann Wolfgang von Goethe

Abstract

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All MOS sample-and-hold circuits suffer to a greater or lesser extent from clock-feedthrough (CLFT), also called charge-injection. During the transition from sample to hold mode, charge is transferred from an MOS transistor switch onto the hold capacitor, thus the name charge-injection. This error can lead to considerable voltage change across the capacitor, and predicting the extent of the induced error potentials is important to circuit designers.

Previous studies have shown a considerable dependency of CLFT on signal voltage, circuit impedances, clock amplitude and clock fall-time. The focus of this work was on the signal dependency of the CLFT error and on the CLFT induced signal distortion in open-loop sample-and-hold circuits. CLFT was found to have a strongly non-linear, signal dependent, component, which may cause considerable distortion of the sampled signal. The parameters influencing this distortion were established. It was discovered that distortion could be reduced by more than 20dB through careful adjustment of the clock fall-rate.

Several circuit solutions that can help reduce the level of distortion arising from CLFT are presented. These circuits can also reduce the absolute level of CLFT. Simulations showed their effectiveness, which was also proven in silicon. The CLFT reduction methods used in these circuits are easily transferable to other switched-capacitor circuits and are suitable for applications where space is at a premium (as, for example, in analogue neural networks).

A new saturation mode contribution to CLFT was found. It is shown to give rise to increased CLFT under high injection conditions.

Table of Contents

List of Illustrations

List of Tables

List of Symbols

Symbol	Parameter	Unit	Alternative	Default
β	transconductance coefficient	$\mu A/V^2$	10^{-6} A/V^2	
ε_0	permittivity in free space	F/m	C/Vm	8.85418×10^{-12}F/m
ε_{ox}	permittivity in SiO_2	F/m	C/Vm	3.9 ε_0
ε_{Si}	permittivity in Silicon	F/m	C/Vm	11.7 ε_0
γ	Bulk threshold parameter or body effect	$\sqrt{V}$	$V^{1/2}$	
λ	channel-length modulation coefficient	1/V	V^{-1}	
μ	surface mobility	cm^2/Vs	10^{-4} m^2/Vs	
φ_F	Fermi potential or Bulk potential; $\varphi_F = V_t \ln(N_{Sub} / n_i)$	V		$\approx$ 0.3 - 0.5V
τ_0	carrier channel transit time	s		
ζ	dummy integration variable			
C_{GDO}	Gate to Drain overlap capacitance per meter channel width	F/m		
C_{GSO}	Gate to Source overlap capacitance per meter channel width	F/m		
C_h	hold capacitance	F		
C_L	load capacitance present at hold node	F		
C_{ol}	Gate overlap capacitance; $C_{ol} = C_{GDO}W$	F		
C'_{ox}	Gate oxide capacitance per unit area; $C'_{ox} = \varepsilon_{ox}/t_{ox}$	F/μm^2	10^{12} F/m^2	
C_{ox}	Gate to channel capacitance or Gate oxide capacitance; $C_{ox} = WLC'_{ox}$	F	As/V	
g_m	Gate transconductance	S	A/V or 1/Ω	
g_{mb}	Bulk transconductance	S	A/V or 1/Ω	
g_o	output conductance (Drain to Source)	S	A/V or 1/Ω	
i_{ds}	Drain to Source channel current	A		
k_B	Boltzmann constant	J/K		1.38066×10^{-23}J/K
L	effective channel length; $L = L_{drawn} - 2L_D$	μm	10^{-6} m	
L_{drawn}	drawn channel length	μm	10^{-6} m	
L_D	lateral diffusion	μm	10^{-6} m	
n	sub-threshold slope factor (process dependent)			
n_i	intrinsic carrier concentration	1/cm^3	10^6/m^3	$\approx 1.45\times10^{10}$/cm^3 at T = 300K
N_{FS}	fast surface state density	1/cm^{2}V	10^4/m^{2}V	
N_{Sub}	substrate doping concentration	1/cm^3	10^6/m^3	

List of Symbols, continued

	Parameter	Unit	Alternative	Default
p	channel partitioning factor			
q	electron charge	C	As	1.60218×10^{-19}C
Q_{bulk}	bulk charge	C	As	
Q_{gate}	Gate charge	C	As	
Q_{inv}	channel charge	C	As	
$R_{\square}$	sheet resistance	Ω/□	Ω/square	
t_f	clock fall time	s		
t_{ox}	Gate oxide thickness	Å	0.1nm	
t_r	clock rise time	s		
T	absolute temperature	K		≈ 300K at 27°C
U	(clock) fall rate	V/s		
V_{BS}	Bulk to Source voltage	V		
V_D	Drain voltage	V		
V_{DS}	Drain to Source voltage	V		
V_{Dsat}	Saturation voltage; $V_{Dsat} = V_{GS} - V_T$	V		
V_{FB}	flatband voltage	V		
V_G	Gate voltage	V		
V_{GS}	Gate to Source voltage; $V_{GS} = V_G - V_S$	V		
V_h	potential difference across C_h	V		
V_H	clock voltage High	V		
V_{HT}	$V_{HT} = V_H - V_{TH}$	V		
V_{in}	input voltage to the circuit	V		
V_L	clock voltage Low	V		
V_o	circuit output voltage	V		
V_{on}	modified threshold voltage for the weak inversion region; $V_{on} = V_T + nV_t$	V		
V_S	transistor Source voltage	V		
V_t	thermal voltage; $V_t = k_BT/q$	V		≈ 26mV at 300K
V_T	threshold voltage for $V_{BS} \neq 0$	V		
V_{T0}	zero threshold voltage; $V_S = 0$, $V_{BS} = 0$	V		
V_{TH}	switch threshold voltage; $V_{TH} = V_S + V_T$	V		
W	effective channel width	μm	10^{-6}m	

Acknowledgement

I would like to thank the following people for their help and support during the course of this research:

Dr. George Wilson for suggesting the field of study, introducing me to research and for his continuous support over the whole period of my studies.

Bob Kennedy and Keith Jackson for their support in difficult times and their help in securing funding for my test chip.

Dominique Coué who has provided invaluable help in discussing MOS transistor behaviour, in particular sub-threshold mode behaviour.

All the technical and administrative staff within the department:
Dave Groom and Adrian Jerram for their support with the CAD facilities and general computing resources.
Bob Bray, Mike Frise and Lee Williams for their help with the hardware design, production of the printed circuit boards and for their generous loan of equipment.

I would like to thank Terry Donelly and Paul Davey for the generous loan of their high speed sampling oscilloscope which proved invaluable in evaluating the test chip performance.

Also, my special thanks to Kaz!

Authors Declaration

At no time during the registration for the degree of Doctor of Philosophy has the author been registered for any other University award.

This study was financed with the aid of a studentship from the University of Plymouth, School of Electronic, Communication and Electrical Engineering.

Signed .....

Date 10.8.2001

Overview

Clock-feedthrough (CLFT), variously referred to as hold-step, pedestal error, switch glitch, residual charge, switch charge injection or charge feedthrough is a phenomena that occurs in sampled data systems such as analogue neural networks (ANN), sample-and-hold (S&H) circuits, N-path filters, A/D converters, current memory cells and switched capacitor (SC) filters. In these systems CLFT typically gives rise to drift, cross-talk, harmonic distortion and signal dependent offset errors [1], [2]. CLFT is caused by the removal of the mobile inversion layer charges when a MOS transistor switch is being turned off. Of paramount interest to the designer is how these charges distribute across the circuit, and particularly how much of the released charge will end up on the hold capacitor, where it gives rise to a change in voltage. It is this phenomenon that is studied and referred to as clock-feedthrough in this thesis.

The focus of this work was on the signal dependency of CLFT in open-loop S&H circuits that employ n-channel depletion type MOS transistors as switches. This restriction to such basic S&H circuits was quite deliberate, as it was believed, that little additional insight would be gained by studying more complex circuits. One particular issue with increasing circuit complexity is that the number of parameters influencing circuit performance grows disproportionately with circuit complexity, and becomes unmanageable fairly quickly. The potential for interaction between the different parts of the circuits also grows with circuit complexity. All this can make the identification of the causes for an observed behaviour very difficult, if not impossible. The insight gained from the study of simple, open-loop, circuits is, however, easily transferable to more complex systems.

The first chapter of this thesis serves as a introduction to S&H circuits. Sample-and-hold circuit specifications and performance measures are introduced and put into context.

Accuracy limiting factors like distortion and k_BT/C noise are briefly discussed. The MOS transistor and its use as a switch in S&H circuits are also examined. Important non-ideal parameters of the MOSFET, such as the Source-body effect, are introduced and their effect on circuit performance explored.

The second chapter deals with the modelling of CLFT for which a basic knowledge of MOS device physics [3], [4] and some familiarity with MOS transistor equations and SPICE models [5] is required. The major contributions to the modelling of clock-feedthrough are revisited, and the impact of circuit parameters such as clock fall-rate and source impedance on CLFT are discussed. The single-lump model for the basic MOS S&H circuit [6] is introduced and its shortcomings and limitations are examined. CLFT under fast Gate turn-off, [7] to [11], and slow turn-off, [12] to [14], conditions is discussed in some detail. Alternative methods for predicting CLFT such as semi-empirical models [15] and circuit simulators are shown to be capable of producing accurate results.

In the third chapter a new, previously unreported, contribution to CLFT, the saturation mode contribution to CLFT, is presented. It will be shown that this contribution can lead to an increase in the CLFT over and above the levels predicted by the single-lump model.

The fourth chapter looks at the signal dependency of CLFT, and in particular the non-linear voltage dependent component of CLFT that gives rise to distortion on the sampled signal. The parameters influencing this distortion are established, and strategies for reducing it are presented. It was found that distortion could be reduced by more than 20dB through careful adjustment of the clock fall-rate alone.

Chapter five looks at different aspects of circuit implementation on silicon. An overview of CLFT reduction techniques and circuits found in the literature is given. Most of the CLFT compensation schemes found rely on additional elements including amplifiers, capacitors

and switches [6], [16]. The impact of parasitics on circuit performance is highlighted and the influence of device geometry [17] and doping gradients [7] on CLFT is shown.

In the sixth chapter, new circuits that can reduce CLFT and the CLFT related distortion are presented. Circuits that exploit the CLFT's sensitivity to mismatch between Source and Drain terminating impedances are explored in the first part of this chapter. These circuits can reduce levels of CLFT and distortion at very little extra cost (in terms of area). A circuit that reduces and linearises CLFT by minimising the impact of the body effect on the MOS switches' inversion layer charge is introduced in the second part of the chapter. This circuit can, potentially, reduce harmonic distortion, arising from CLFT, by more than two orders of magnitude. The CLFT reduction schemes presented in this chapter require only little additional silicon area and are easily transferable to other circuits.

Chapter seven reports measurement results from a test chip. The measurements are contrasted with simulations and predictions from the CLFT models presented in this thesis. The performance of the circuits from chapter six was evaluated on the test chip. The measured results show good correlation with analytical models and circuit simulations. Integral non-linearity of these S&H circuits from chapter six and of the basic, uncompensated, S&H is shown to be in good agreement with predictions made in chapter four. Tentative evidence for the saturation mode contribution to CLFT is presented. The test chip and test setup are briefly described.

The eighth, and final, chapter of this thesis presents a summary and conclusions of the work carried out. Recommendations for further work are being made.

1. An introduction to sample-and-hold circuits.

Before the literature review a brief outline of the characteristics of sample-and-hold circuits (S&H's) is given with the intention to raise awareness for problems the designer faces when planning and using such a circuit. Fig. 1-2 gives the fundamental, underlying, circuit diagram of any S&H circuit.

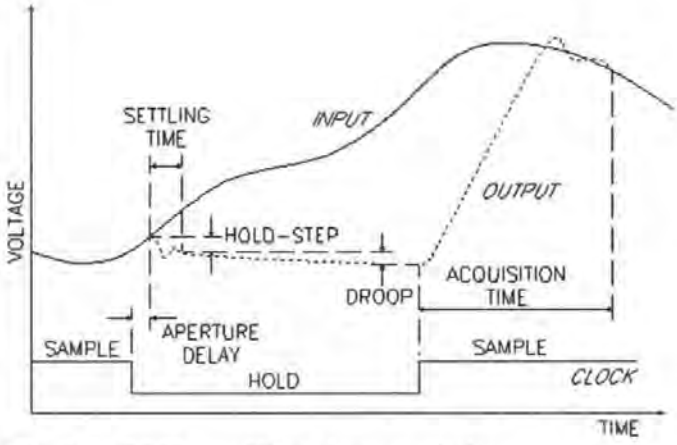

Fig. 1-1: S&H amplifier characteristics.

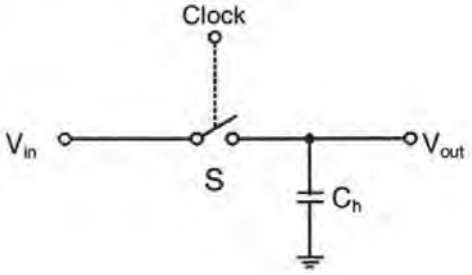

Fig. 1-2: S&H circuit, principle.

Typical input, output and control waveforms of a sample-and-hold amplifier are shown in Fig. 1-1*. Initially, the circuit is in the sampling mode with the output tracking the input. Upon receipt of the hold command it takes a finite amount of time for the switch to open. This is referred to as *aperture delay* and is measured from when the control signal crosses the 50% point, to when the output stops following the input. The aperture delay varies to some extent and this variation is called *aperture jitter*. It arises from noise modulating the phase of the hold command and is commonly expressed as an rms time jitter.

After the switch opens it takes the S&H some time to settle to within a specified error band around the final voltage; this is referred to as *settling time*. Likewise a step change of the

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* The clock in Fig. 1-1 was shown with rise and fall times of zero. In reality the clock will take some time to go from logic high to low and vice versa.

output signal can be observed during this time. It is variously known as *hold-step, charge-injection or clock-feedthrough (CLFT).* This hold-step is caused by charge being transferred from the switch and its control circuit to the hold capacitor during the switch turn-off. In the hold mode any leakage at the holding node will either charge or discharge the hold capacitor C_h, depending on the polarity of the leakage. The resulting rate of change of the output voltage is called *droop rate*. Another non-ideal parameter of S&H circuits in the hold mode is *feedthrough*. It specifies the extent to which a change in input signal is reflected at the output.

When the sampling command is received, it takes considerable time for the circuit to resume tracking. This time, known as *acquisition time,* is defined as the amount of time it takes the S&H to reacquire the analogue input when switching from hold to track mode. The interval starts at the 50% clock transition point and ends when the input signal is reacquired to within a specified error band at the hold capacitor. The acquisition time, t_a, usually consists of three parts: a delay in closing the switch, a slew rate limited portion and a settling time portion. If the 'ON' resistance R_{ON} of the switch is so large that it poses a limit to the acquisition time, then t_a can be found from the required precision (e.g. 0.001 for a precision of one in a thousand) and the RC time constant of the S&H circuit as

$$t_a = \ln\left(\frac{1}{\text{precision}}\right) R_{ON}\, C_h$$

Eqn. 1-1

Other terms that are important when describing a S&H circuit's performance are gain accuracy, slew rate and bandwidth. *Gain accuracy* is expressed as the S&H's deviation in gain from its nominal value. *Slew rate* is the fastest rate at which a S&H's output changes. It is commonly measured in V/s. *Bandwidth* specifies the lowest frequency at which the

S&H's small-signal gain is 3dB lower than its DC gain. For the basic S&H, shown in Fig. 1-2, the bandwidth is simply:

$$f_{-3dB} = \frac{1}{2\pi R_{ON} C_h}$$

Eqn. 1-2

Integral Non-Linearity (INL) 2nd harmonic distortion and 3rd harmonic distortion (HD_2 and HD_3) as well as *Total Harmonic Distortion* (THD) are performance specifications frequently found on S&H datasheets. They give some indication of the non-linearity of a S&H's transfer function, and are derived from either static (INL) or dynamic (HD_2, HD_3 and THD) measurements.

Integral Non-Linearity, is derived from a S&H's static (or DC) transfer characteristic. It is defined as the worst case deviation of the output from an ideal straight line approximation drawn through the end points of the plot and is commonly expressed as a fraction (or percentage) of the full-scale output value:

$$INL = \max\left(\left| \frac{V_{out}(V_{in}) - V_{out}(V_{in,min})}{V_{out}(V_{in,max}) - V_{out}(V_{in,min})} - \frac{V_{in} - V_{in,min}}{V_{in,max} - V_{in,min}} \right| \right) \Bigg|_{V_{in,min} \le V_{in} \le V_{in,max}}$$

Eqn. 1-3

where $V_{in,min}$ and $V_{in,max}$ are the minimum and maximum DC input voltages applied to the circuit, and $V_{out}(V_{in})$ is the circuit's DC output voltage at a particular input voltage, V_{in}.

Sometimes a best-fit straight line (typically employing the linear regression method) is used instead of the end point straight line approximation.

Harmonic distortion may, for example, be measured by applying a pure sine to a circuit's input and measuring the harmonic content of the circuit's output signal with a spectrum analyzer. From this the *Total Harmonic Distortion*, defined as the ratio of the rms sum of

all the output signals' higher harmonic components (2nd harmonic h_2 and higher) to its fundamental component (or 1st harmonic h_1) can be worked out:

$$THD = \frac{\sqrt{\sum_{i=2}^{\infty}(h_i)^2}}{|h_1|}$$

Eqn. 1-4

Even though the definition of THD requires knowledge of all harmonics, in practice it is often sufficient to measure only the first five harmonics to get a reasonably accurate figure for THD.

1.1 Non-linearity and harmonic distortion.

In this section a method is presented for predicting the size of the harmonic distortion (HD) products arising from non-linearities in a circuit's transfer function. This method will allow us to estimate the size of the HD products caused by CLFT, which, as we shall see later, can introduce considerable non-linearity to a S&H circuit's transfer function.

To find the HD products from a circuit's transfer function we must, at first, describe the circuit's transfer function (be it linear or non-linear) in terms of a Taylor expansion, which is also known as a power series expansion:

$$V_{out} = K_0 + K_1 V_{in} + K_2 V_{in}^2 + K_3 V_{in}^3 + K_4 V_{in}^4 + K_5 V_{in}^5 \ldots$$

Eqn. 1-5

Performing a polynomial regression to a circuit's measured transfer characteristic will yield the coefficients, K, for the power series expansion quite readily.

Once the power series coefficients K are known the following equation can be used to estimate the harmonic distortion products up to h_n from a given n-th order power series expansion:

$$h_0 = \frac{V_{in}}{2} \sum_{m=0}^{\infty} \frac{K_{2m}}{2^{2m-1}} \binom{2m}{m} V_{in}^{2m-1}$$

$$h_x = V_{in} \sum_{m=0}^{\infty} \frac{K_{2m+x}}{2^{2m+x-1}} \binom{2m+x}{m} V_{in}^{2m+x-1} \qquad ; \text{ for } 1 \le x \le n$$

Eqn. 1-6

Eqn. 1-6 was derived from a similar expression found in [18]. The equation assumes that a purely sinusoidal input signal of amplitude, V_{in}, with no DC-offset, relative to the point around which the power series was developed for, was applied to the circuit. Any DC-offset on the input signal can be accommodated, if required, by applying an appropriate co-

ordinate transformation to the power series expansion before evaluating Eqn. 1-6, or, indeed, by developing the power series expansion around the desired DC-offset point in the first place.

Of the h_x derived (Eqn. 1-6) only h_2 and higher (i.e. h_x with $x > 1$) are harmonic distortion products. The other two, h_0 and h_1, represent the circuits DC-offset and gain, respectively. Clearly, distortion will only arise, if K_2, and higher, of the Taylor expansion to a circuit's transfer function (Eqn. 1-5) are not zero. A distortion product is said to be dominant if THD is largely determined by it, in which case:

$$THD \cong \frac{h_{dominant}}{h_1}$$

Assuming that a circuit's THD is determined solely by non-linearities present in its static, or DC, transfer characteristic and that only one of the harmonics should be dominant then INL and THD will be linked by the following simple relationship:

$$THD \cong INL$$

Eqn. 1-7

1.2 k_BT/C Noise.

Noise in the S&H circuit of Fig. 1-2 originates from the ON resistance, R_{ON}, of the switch and the source resistance R_{in} of the signal source [2]. Both resistances can, conveniently, be lumped together to form the input resistance R_S of the S&H in sampling mode:

$$R_S = R_{ON} + R_{in}$$

The rms value of the thermal noise voltage generated by R_S is:

$$\overline{v} = \sqrt{4k_B T R_S \Delta f}$$

where Δf represents the bandwidth of the circuit.

During the sampling period, the (thermal) noise generated by R_S is integrated on, and bandwidth limited by, the low-pass filter formed by R_S and C_h. We can thus write:

$$\overline{v}^2 = 4k_B T R_S \int_0^{\infty} \frac{1}{1+(\omega R_S C_h)^2} df$$

Evaluating this equation gives the noise power in the S&H's output signal during the sampling period:

$$\overline{v}^2 = \frac{k_B T}{C_h}.$$

Eqn. 1-8

It is interesting to note that $\overline{v}$ is only dependent on the circuit parameter C_h, but not on R_{ON} or the bandwidth of the S&H. This shows that there is no benefit in reducing R_S below the value required by the circuit's settling time and accuracy requirements (Eqn. 1-1).

Using Eqn. 1-8 and the rms value of the sine wave input signal ($\overline{v}_{in} = \sqrt{0.5}\, V_{in}$, for a sine wave signal of amplitude V_{in}) we can work out the signal to-noise ratio, SNR, of the basic S&H circuit, shown in Fig. 1-2:

$$SNR = 10\log\left(\frac{C_h V_{in}^2}{2k_B T}\right)$$

Eqn. 1-9

Eqn. 1-9 shows that a desired SNR can only be achieved if both the hold capacitor C_h and the input signal V_{in} are sufficiently large. It also shows, that it is possible to trade-off V_{in} against C_h. Increasing V_{in}, however, will improve SNR much more than an equal increase in C_h. This means, that low voltage technologies will need disproportionately larger hold capacitors to achieve the same SNR figures than high voltage technologies.

1.3 The MOS transistor as a switch.

MOSFETs are almost ideal voltage controlled switches. Their turn-on and turn-off times are short (nano-seconds and below), 'ON' resistance is low (from a few Ω to hundreds of Ω, depending on the transistor size), and 'OFF' resistance is high (typically hundreds of MΩ to TΩ). Unfortunately, they give rise to aperture jitter and clock-feedthrough (CLFT). Both errors are the direct result of the MOS transistors operating principles.

In the following sections we will introduce the basic operating principles of the MOS pass-transistor switch and illustrate them with the example of the n-channel enhancement mode MOS transistor (NMOST), unless stated otherwise. Throughout we will use the SPICE Level 1 model [5] (Shichman & Hodges model) wherever possible. This model is based on semiconductor device physics [3], [4], but is simple enough to permit its use in hand calculations and analytical descriptions. Despite its simplicity the SPICE Level 1 model can give adequate descriptions of circuit behaviour, provided one is aware of its limitations. We shall point out the model's limitations where these give rise to significant errors.

1.3.1 The MOS transistor switch, turned 'ON'.

A MOS pass-transistor will be 'ON' when a conducting channel between Source and Drain exists. This conducting channel consists of minority carriers that accumulate under the Gate oxide if the Gate to Source potential, V_{GS}, is sufficiently high and of the right polarity (see Fig. 1-3 below, where the channel is represented by a, cyan coloured, sheet lying directly below the Gate oxide). Of the two channel contacts (implants) the one to which the Gate has the greatest potential difference to is known as Source, the other is called Drain.

In the case of an NMOS transistor the Gate potential must be at least a threshold voltage, V_T, above the transistor's Source potential, V_S, ($V_G \geq V_S + V_T$) for the channel to form (for

a definition of V_T see Eqn. 1-12 below). The reciprocal applies to PMOS transistors, where the threshold voltage is negative and the Gate to Source potential difference, V_{GS}, must therefore be V_T or less ($V_{GS} \leq V_T$) to turn the device 'ON'.

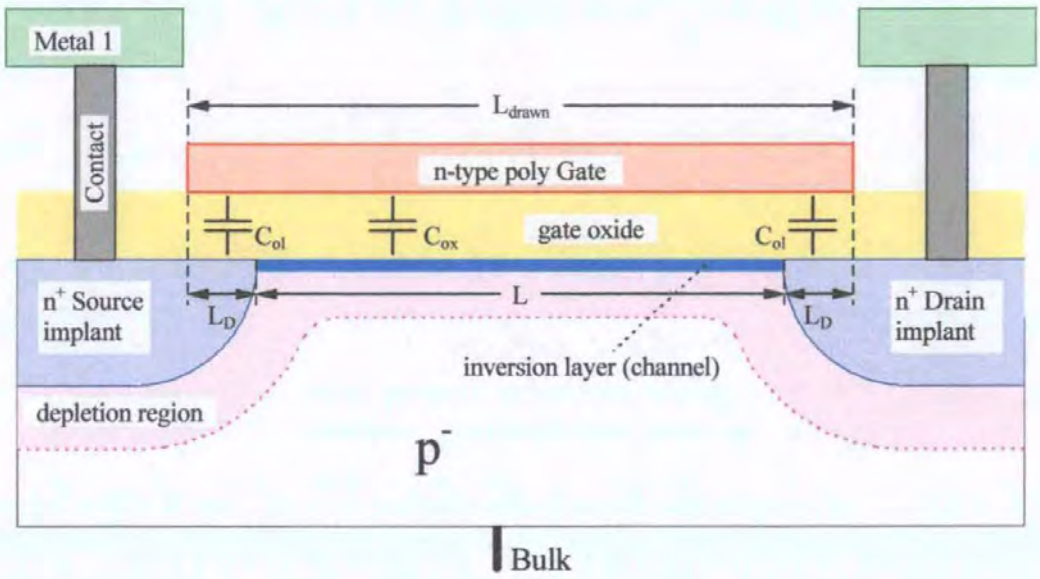


Fig. 1-3: Cross-section of a turned 'ON' NMOS transistor in the linear region.

A MOS pass-transistor that has been turned 'ON' is said to operate in the linear region if $|V_{DS}| < |V_{GS} - V_T|$, i.e. if the voltage drop along its channel is less than the saturation voltage of the channel ($V_{Dsat} = V_{GS} - V_T$). In the linear region, also known as the ohmic or triode region, the transistor will (to first order approximation) behave like a resistor:

$$R_{ON} = \frac{1}{\beta |V_{GS} - V_T|}$$

Eqn. 1-10

where $\beta = \mu C'_{ox} W/L$ and L is the length of the conducting channel that connects Drain and Source, W the width of this channel, μ is the mobility of the charge carriers in the channel, $C'_{ox} = \varepsilon_{ox}/t_{ox}$ the Gate oxide capacitance per unit area, t_{ox} is the oxide thickness and ε_{ox} the Gate oxide's permittivity.

1.3.2 Calculation of a MOSFET's channel charge.

The size of the inversion layer charge, stored in the channel of a NMOS pass-transistor operating in the linear region, i.e. if $V_{DS} < V_{GS} - V_T$, can be worked out easily using the SPICE Level 1 model. Assuming a low voltage drop across the turned 'ON' NMOS pass-transistor, i.e. $V_{DS} \cong 0V$, its respective inversion layer charge Q_{inv} is found as:

$$Q_{inv} = C_{ox}(V_{GS} - V_T)$$

Eqn. 1-11

$C_{ox} = WLC'_{ox} = WL\varepsilon_{ox}/t_{ox}$ is the Gate to channel or Gate oxide capacitance and V_T is the transistor's threshold voltage under the given Source bias:

$$V_T = V_{T0} + \gamma\left(\sqrt{2\varphi_F - V_{BS}} - \sqrt{2\varphi_F}\right)$$

Eqn. 1-12

Here V_{T0} is the transistors threshold voltage at zero Source bias ($V_{BS} = 0V$), γ is its body effect coefficient and φ_F is a material constant of the transistor substrate (Bulk) known as the Bulk potential (sometimes also referred to as the Fermi potential). The equations describing these are:

$$V_{T0} = V_{FB} + 2\varphi_F + \gamma\sqrt{2\varphi_F}$$

Eqn. 1-13

$$\varphi_F = \frac{k_B T}{q} \ln\left(\frac{N_{Sub}}{n_i}\right)$$

Eqn. 1-14

and

$$\gamma = \frac{WL}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_{Sub}}$$

Eqn. 1-15

From Eqn. 1-11 it becomes quite clear that Q_{inv} depends on the MOSFETs terminal potentials. Particularly noteworthy is the threshold voltage's non-linear dependency on the transistors Source and Bulk voltages (Source-Body effect), which, as we shall see later, is one of the sources of distortion in S&H circuits.

In fact, this non-linear dependency of Q_{inv} on V_{BS} arises from the charge stored in the depletion layer which isolates the channel from the substrate (see Fig. 1-3). This becomes quite clear if we express the channel charge as a function of the transistor Gate charge, Q_{gate}, and its depletion layer charge, Q_{bulk}:

$$Q_{inv} = -Q_{gate} - Q_{bulk}$$

Eqn. 1-16

where

$$Q_{gate} = C_{ox}(V_{GS} - V_{FB} - 2\varphi_F) \qquad \text{and} \qquad Q_{bulk} = -WL\sqrt{2\varepsilon_{Si} q N_{sub}(2\varphi_F - V_{BS})}$$

Eqn. 1-17 **Eqn. 1-18**

Eqn. 1-16 to Eqn. 1-18 were derived from Liu and Nagel's quasi-static small-signal capacitance model [19].

1.3.3 MOS transistor switch, turned 'OFF'.

To turn a MOS transistor 'OFF', the conductive channel between the Drain and Source terminals must be removed. For a NMOS transistor this means applying a Gate to Source voltage that is lower than the threshold voltage (i.e. $V_{GS} < V_T$); the reciprocal applies to the PMOS transistor which is turned 'OFF' for $V_{GS} > V_T$.

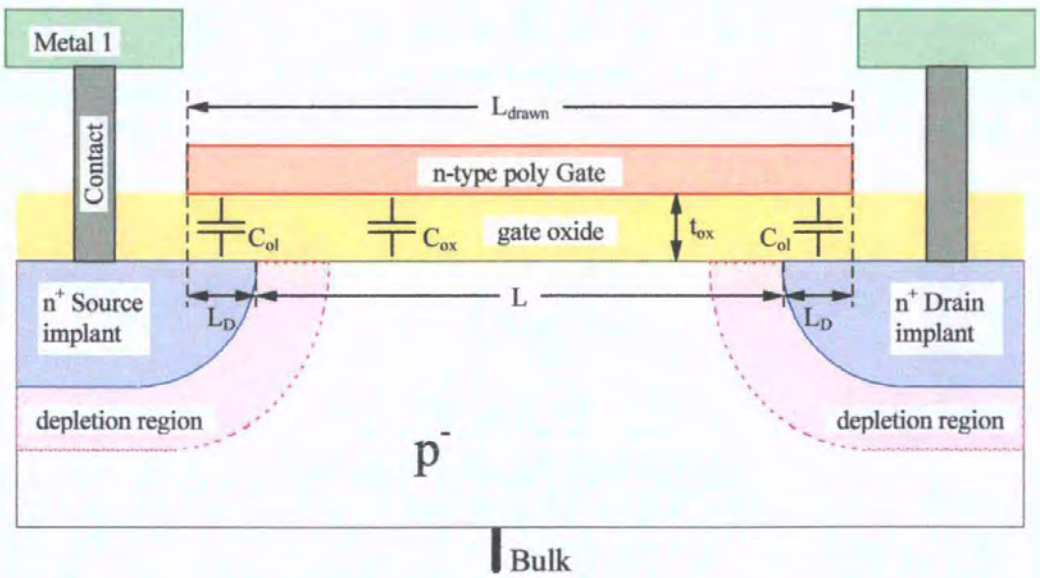


Fig. 1-4: Cross-section of an NMOS transistor when turned 'OFF'.

Fig. 1-4 above, shows a cross-section of an NMOS transistor in the 'OFF' state. We observe that the inversion layer has disappeared and that the Gate oxide capacitance, C_{ox}, now terminates to the Bulk. The MOSFET's Gate would now be completely decoupled from its Source and Drain terminals, if it were not for the, parasitic, Gate-overlap capacitance C_{ol}. This overlap capacitance also contributes to CLFT, as we shall see later. Unfortunately the overlap capacitance can not be made zero, as some Gate to Drain overlap (and Gate to Source overlap) is inherent, and indeed required, for reliable manufacturing of MOS transistors. C_{ol} is a linear capacitance and is determined by the transistor's Gate oxide thickness, t_{ox}, its Gate width W and the process dependent Gate to Drain overlap L_D. C_{ol} could therefore be derived as follows:

$$C_{ol} = \varepsilon_{ox} \frac{W L_D}{t_{ox}}$$

Fringing capacitance associated with the Gate to Drain edge also needs to be included in the calculation of C_{ol}. For short channel devices this can increase the actual value of C_{ol} considerably over and above what was calculated using the equation above.

It is therefore better to use the foundry supplied C_{GSO} and C_{GDO} figures for the calculation of C_{ol}. These (C_{GSO} and C_{GDO} figures) specify the respective Gate to Source and Gate to Drain overlap capacitance per meter gate width, inclusive of any fringing effects. C_{ol} (on the Drain side) is therefore simply:

$$C_{ol} = W C_{GDO}$$

Eqn. 1-19

1.4 Basic S&H circuit with a NMOS switch.

In a practical realisation of the S&H circuit in Fig. 1-2, one could replace the switch with a NMOS transistor (NMOST). This will allow to control the state of the S&H by modulating the transistors Gate potential. A logic high, V_H, applied to the Gate of the NMOST will turn it 'ON' (i.e. closes the switch) and bring the S&H into track mode. When the input signal is fully acquired both the MOS switches' Source and Drain potentials are approximately equal to the S&H's input voltage, and the pass-transistor will be operating in the linear region. A logic low, V_L, on the Gate will turn the NMOST 'OFF' and bring the circuit into hold mode.

1.4.1 An acquisition time imposed lower limit for the size of the NMOS switch.

An important measure of performance for many S&H circuits is the acquisition time t_a. This was shown to be linked to R_{ON} in Eqn. 1-1, which allows us to derive an expression for the maximum acceptable 'ON' resistance R_{ONmax} from the, specified, maximum acceptable acquisition time t_{amax}:

$$R_{ON\,max} = \frac{t_{a\,max}}{\ln\left(\frac{1}{precision}\right)C_{h\,max}} = \frac{1}{\beta_{min}V_{HT\,min}} = \frac{1}{\beta_{min}\left[V_{H\,min} - (V_{in\,max} + V_{T\,max})\right]}$$

For this calculation of R_{ONmax} the manufacturing tolerances and circuit operational limits must be taken into account. This is why the maximum hold capacitance C_{hmax}, the lower limit for the device transconductance β_{min}, the lower limit of the clock high voltage V_{Hmin}, the upper limit for the input voltage V_{inmax} and V_{Tmax} (the maximum threshold voltage at V_{inmax}) must be chosen as input parameters to the calculation.

This imposes a lower limit on the W/L ratio and hence the size of the pass-transistor:

$$\frac{W}{L} \geq \frac{\ln\left(\frac{1}{\text{precision}}\right) C_{h\max}}{\mu C_{ox} t_{a\max}\left[V_{H\min} - (V_{in\max} + V_{T\max})\right]}$$

Eqn. 1-20

1.4.2 Clock-feedthrough.

Turning a MOS switch 'OFF' requires removal of all of the mobile charges that form the conductive channel between the Drain and Source terminals. These charges will exit the transistor by its Source and Drain terminals. Part of the channel charge will flow to the signal source and the remainder will flow to the hold capacitor, causing the voltage across it to change. The mobile channel charges are a major contributor to clock-feedthrough, and parasitic capacitances, such as the Gate overlap capacitance, C_{ol}, contribute the remainder.

CLFT is negative for NMOS devices and positive for PMOS transistors.

1.4.3 Aperture delay and aperture jitter of the NMOS switch.

As soon as the hold command is given the Gate voltage starts to fall. It will take a finite amount of time to complete the transition from high to low. Some time after the transition started the Gate voltage will reach threshold level, at which point the switch opens. This delay, the so called aperture delay, t_{da}, is assumed constant. For a NMOS switch however the real aperture delay, $t_{da,NMOS}$, is longer for low input voltages than for high ones:

$$t_{da,NMOS} = \frac{V_H - (V_{in} + V_T)}{U} \qquad \text{where} \qquad V_T = V_{T0} + \gamma\left(\sqrt{2\varphi_F + V_{in}} - \sqrt{2\varphi_F}\right)$$

We see that $t_{da,NMOS}$ depends on the clock or Gate voltage in sample mode, V_H, the clock fall rate, U, the input signal voltage, V_{in}, and the threshold voltage, V_T. We can also see that V_T, too, is a (non-linear) function of the input voltage. This signal dependency of

$t_{da,NMOS}$ is one of the contributing factors to the uncertainty in the aperture delay that is known as aperture jitter. It has many other contributing factors, such as wideband random noise, thermal noise and power supply noise, but it can be stated that the shorter the clock fall time, the smaller the aperture jitter will be. Fortunately, clock fall times can be made very short (tens of ps to several ns), if required, using on-chip clock generators and buffering.

However, not all applications benefit from short clock fall times, and where large aperture jitter can be tolerated (e.g. in applications where only very slowly changing signals are sampled) the use of long clock fall times may actually be advantageous (as will be shown later in chapters 2 and 4).

1.5 Summary of generic S&H circuit issues.

It has been shown that turn-on transients affect the acquisition time, and thereby the speed, of a S&H circuit, whereas the turn-off transient introduces errors (hold-step and aperture jitter) to the signal path. It was found that a fast turn-off transient is normally beneficial, since it leads to lower aperture delay and aperture jitter.

A large sampling capacitance is often advantageous since it reduces k_BT/C noise, it also leads to lower droop rate in the hold period and reduces the hold-step (i.e. CLFT). A small sampling capacitor, however, is preferable in the sampling period since it results in a shorter acquisition time.

A designer will therefore have to find an acceptable compromise between speed and precision. If, however, the droop rate and/or the hold-step can be decreased by other means than increasing the size of C_h a superior circuit in terms of precision and/or speed will be the result. This, essentially, is what CLFT reduction techniques set out to achieve: extending the range of operation for a given technology.

2. Review of CLFT theory.

This section reviews the major contributions to research on clock-feedthrough. The models and theory presented are based on standard n-channel enhancement MOS transistors, unless stated differently. These devices, referred to as MOSFETs, are inherently symmetrical and are characterised by:

- a uniformly doped channel region.
- identical Drain and Source implants (doping profile and geometry).
- a rectangular channel geometry.
- a zero threshold voltage, V_{T0}, of greater than zero volts ($V_{T0} > 0$).

Another convenient assumption used throughout is that of the hold capacitor being fully charged before the pass-transistor is being turned off. This implies that all transient currents and voltages have settled i.e. the circuit is in a DC like steady-state. The voltage across the pass-transistor switch is then near zero ($V_{DS} \cong 0V$) and it operates in the ohmic, or linear, region.

The review of CLFT theory that follows takes the form of concise summaries of the relevant CLFT models and literature. The emphasis was on qualitative descriptions of the causes and effects of CLFT. This, it was felt, was best suited to fostering insight and understanding into the underlying mechanisms that are governing CLFT. Thus, the number of equations was kept to a minimum. Those that were included were deemed to be either giving a good summary of the proposed models or presenting valuable insights into the parameters that influence CLFT. For further details of these models the reader may wish to consult the references quoted.

The first CLFT model reviewed is the 'classic' single-lump model for the MOS pass-transistor and its application to CLFT in the basic S&H circuit with zero signal source

impedance (Sheu & Hu, 1984 [6]). This model is something of a 'de-facto standard' for the calculation of CLFT in S&H circuits, to which newer models are often compared. It is a relatively simple analytical model that employs the SPICE Level 1 MOSFET model in the description of the circuits' behaviour during pass-transistor turn-off. The single-lump model approximates CLFT behaviour fairly well over a wide range of circuit conditions. However, it does have problems under very fast and very slow switching conditions, and with non-zero signal source impedances. The latter issue is briefly dealt with in section 2.2, which examines CLFT in the basic S&H circuit with non-zero signal source impedance (Sheu & Hu, 1984 [6]).

The discussion of the model for the weak inversion channel charge component to CLFT was included as an example of how effects that were not accounted for in the single-lump model can become important, or even dominant, under slow switching conditions. The model discussed in section 2.6 was put forward by Gu & Chen in 1996 [14], following experiments by Chen et al. (1994 [12], 1995 [13]) which had shown that the single-lump model could be significantly in error under slow switching conditions, due to an additional error charge component, which they attributed to channel charges in weak inversion.

Fast turn-off of the MOS pass-transistor and its effects on CLFT are considered in sections 2.4 and 2.5. Attempts at modelling CLFT under very fast switching conditions, and the related modelling of the MOS pass-transistor's transient behaviour, resulted in complex distributed models that could only be solved numerically, or required the use of two-dimensional device simulators [7] to [9]. These simulations indicated, that under fast turn-off conditions there is simply not enough time for complete removal of all the mobile channel charges while the pass-transistors is being turned-off (Kuo, Dutton & Wooley, 1986 [7] & [17] also Turchetti, Mancini & Masetti, 1986 [9]). With these 'left-behind' channel charges trapped in the channel region, the transistor enters the diffusion mode of

conduction. Some of the trapped inversion layer charges may be lost to the substrate through charge pumping [10], [11]. Both effects had not been considered in the single-lump model for CLFT, which is why it can be in error under fast switching conditions.

The distributed model for the MOS pass-transistor (Kuo, Dutton & Wooley, 1986, [7] & [17]), discussed in section 2.4, includes this diffusion mode of conduction. The distributed model renders the turn-off transients and dynamic CLFT behaviour of MOS S&H circuits fairly accurately, even under very fast switching conditions. Charge pumping [10], [11] will also be discussed in this section.

The two-lump model for the MOS pass-transistor (Kuo, Dutton & Wooley, 1986, [7] & [17]), which is examined in section 2.5, also takes the diffusion mode of conduction into account, albeit in a somewhat cruder form than the distributed model. Nonetheless, it is a very useful model, as it manages to approximate the diffusion mode of conduction in a simple and easily understandable way.

The case of the floating MOS pass-transistor, which is frequently encountered in switched capacitor circuits that rely on charge transfer, such as the SC integrator, was examined by Shieh, Patil and Sheu in 1987. They proposed the single-lump CLFT model for the floating MOS pass-transistor [20] that is reviewed in section 2.3. The model successfully rationalises the complex interactions between the clock fall-rate and the relative Source and Drain load impedances, i.e. the ratio between the capacitances attached to the pass-transistors' Source and Drain terminals. Again, no diffusion mode of conduction or weak inversion contributions were taken into account.

An example of a semi-empirical model for CLFT is included in section 2.7. The model discussed is the one for CLFT in the basic S&H circuit that was put forward by McQuigg in 1983 [15]. The model is simpler and computationally less demanding than the single-

lump model. This is a very useful property for the simulation of large circuits where semi-empirical models can help reduce simulation time considerably. An excellent match between the single-lump model and semi-empirical model can be achieved by carefully adjusting the semi-empirical models' curve fitting coefficients.

A brief discussion of simulators and transistor models follows in section 2.8. The aim of which is to raise awareness to some of the shortcomings of common simulators and MOS models.

Summary and conclusions complete this review of CLFT theory.

2.1 Basic single-lump model.

Sheu and Hu [6] presented an analytical model for the CLFT mechanism of the most basic switched capacitor circuit, the track-and-hold (T&H) amplifier with a single transistor switch and an ideal DC voltage source providing V_{in} (shown in Fig. 2-1).

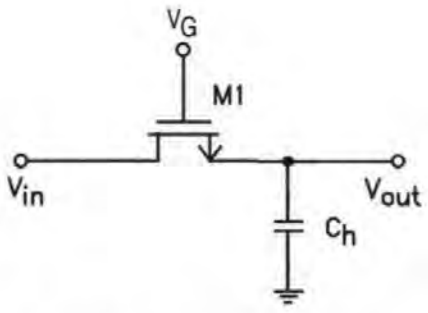


Fig. 2-1: Basic T&H amplifier

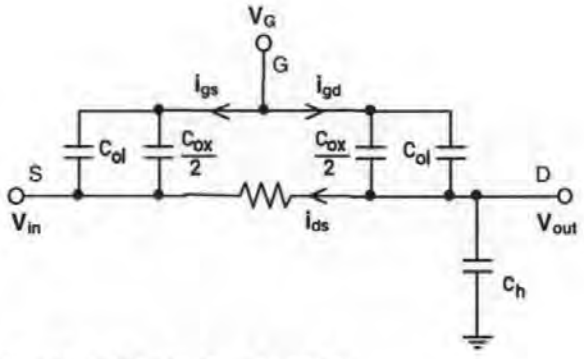


Fig. 2-2: Single-lump model

In their paper they identified three factors that contribute to CLFT:

1. the mobile channel charge Q_{Inv}. It is associated with the Gate oxide capacitance C_{ox}.
2. the charge on the overlap capacitances C_{ol}.
3. a 'compensating' Drain to Source current, i_{ds}, flowing in the conductive channel.

They also noted that turn-off consists of two distinct phases:

Phase 1: $V_H \geq V_G \geq V_S + V_T$

In this phase the transistor is 'ON' and operates in the linear region. As the Gate voltage falls the channel gradually diminishes to the point where the Gate voltage reaches threshold ($V_G = V_S + V_T$), at which the channel disappears. During this period the mobile charges making up the channel (electrons in the case of a NMOS transistor) are driven out of both the Drain and Source ends giving rise to i_{gd} and i_{gs}. This results in the potential v_{ds} changing from the initial zero value and thereby causing a channel current i_{ds} to flow. This i_{ds} cancels i_{gd} to some extent, thereby reducing CLFT.

Phase 2: $V_S + V_T > V_G \geq V_L$

The transistor is 'OFF', however the Gate voltage still continues to fall until it reaches V_L. During this phase only the overlap capacitance C_{ol} will contribute to the CLFT; no conductive channel exists in Phase 2 therefore both C_{ox} and i_{ds} are 0.

2.1.1 Analysis

Assuming $|dV_G/dt| \gg |dv_d/dt|$ (certainly true, since CLFT, i.e. Δv_d, is small compared to ΔV_G) and V_G to be a linear ramp function, starting to fall at t = 0 from V_H towards V_L at a rate U ($V_G = V_H - Ut$), the differential equation for the single-lump model (Fig. 2-2) can be written as:

$$C_h \frac{d v_d}{d t} = -i_{ds} - \left(C_{ol} + \frac{C_{ox}}{2} \right) U$$

Eqn. 2-1

In the present form Eqn. 2-1 can not be solved for v_d, because i_{ds} is an implicit function of v_d. Therefore a suitable expression, describing i_{ds} as an explicit function of v_d, need to be found. For this purpose Sheu and Hu adopted the Shichman & Hodges model (SPICE Level 1 model) of a MOSFET operating in the linear, or so called ohmic, region:

$$i_{ds} = \beta \left(V_{gs} - V_T - \frac{V_{ds}}{2} \right) v_{ds}$$

Eqn. 2-2

Under the condition that $V_{ds} \cong 0$ and V_S is constant ($\therefore v_s = 0$, hence $v_{ds} \equiv v_d$), Eqn. 2-2 simplifies to:

$$i_{ds} = \beta \left(V_{gs} - V_T \right) v_d$$

Eqn. 2-3

We could have arrived at the same equation for i_{ds} by starting with R_{ON} of the MOS switch (Eqn. 1-10). Applying Ohm's Law we find that the current in a MOS switch, is:

$$i_{ds} = \frac{v_d}{R_{ON}}, \text{ where } R_{ON} = \frac{1}{\beta |V_{GS} - V_T|} \text{ and therefore } i_{ds} = \beta(V_{gs} - V_T)v_d,$$

which is identical to Eqn. 2-3.

2.1.1.1 Phase 1

Inserting Eqn. 2-3 into Eqn. 2-1 and solving, gives the description for the time-domain behaviour of v_d during Phase 1 of the turn-off. The derivation of Eqn. 2-4, listing the steps involved in transforming Eqn. 2-1 into Eqn. 2-4, can be found in the Appendix B.

$$v_d(t) = -\sqrt{\pi U \frac{C_h}{2\beta}} \left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_h} \right) e^{\frac{\beta U}{2C_h}\left(t - \frac{V_{HT}}{U}\right)^2} \left[\operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_h}} V_{HT} \right) - \operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_h}} (V_{HT} - Ut) \right) \right]$$

Eqn. 2-4

The CLFT contribution of the first phase is simply $v_d(t)$ at the end of Phase 1, i.e. where V_G reaches threshold ($V_G = V_S + V_T$). This is the case at $t_1 = V_{HT}/U$, consequently $v_d(t_1)$ gives the desired result.

$$v_{d1} = v_d(t_1) = -\sqrt{\frac{\pi U C_h}{2\beta}} \left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_h} \right) \operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_h}} V_{HT} \right)$$

Eqn. 2-5

where

$$\beta = \mu C_{ox}' \frac{W}{L} \qquad U = \frac{V_H - V_G}{t} \qquad V_{HT} = V_H - (V_S + V_T)$$

2.1.1.2 Phase 2

For the whole of the second period both i_{ds} and C_{ox} are assumed to be 0. Applying the same principles as before the expression for the CLFT of Phase 2 is obtained as:

$$v_{d2} = -\frac{C_{ol}}{C_h}(V_S + V_T - V_L)$$

Eqn. 2-6

Here the simplified denominator term C_h was used instead of the complete $C_{ol} + C_h$. The resulting error (an overestimation of CLFT) will be small, if C_h is much larger than C_{ol}.

2.1.1.3 Total clock-feedthrough.

The total CLFT is simply the sum of the Phase 1 and Phase 2 contributions:

$$CLFT = v_{ds} = v_{d1} + v_{d2} \qquad \textbf{Eqn. 2-7}$$

A typical plot of CLFT for different signal voltages and fall rates is shown in Fig. 2-3 below. The circuit parameters were:

$W = 4\mu m$, $L = 3.3\mu m$, $L_D = 0.35\mu m$, $C_h = 2pF$, $t_{ox} = 70nm$, $N_{Sub} = 5\times10^{14}cm^{-3}$, $V_{T0} = 0.6V$,

$V_H = 5V$, $V_L = 0V$ and $\mu_n C'_{ox} = 25\mu A/V^2$.

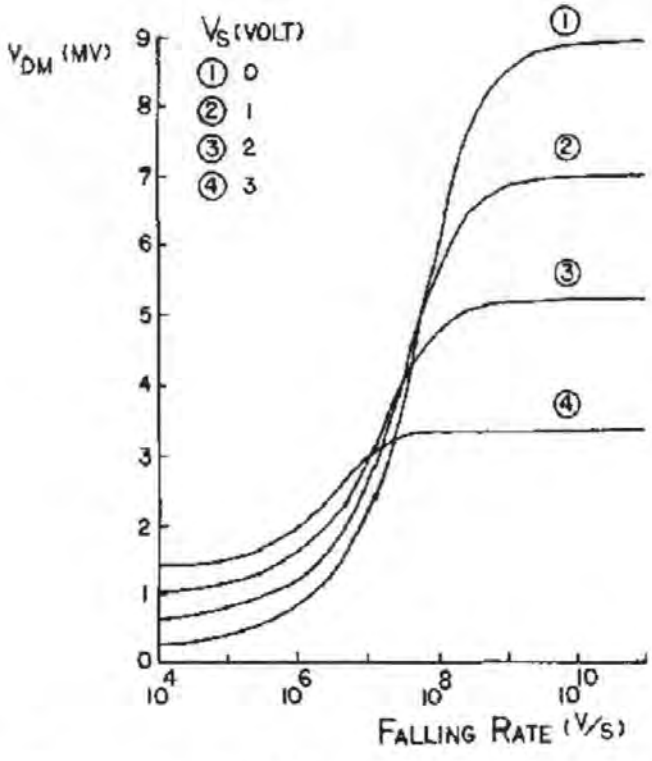


Fig. 2-3: The CLFT voltage as a function of the Gate voltage falling rate for four signal voltage levels. Fig. reproduced from [6].

The plot clearly shows the signal dependency and clock fall rate dependency of CLFT. Particularly interesting are clock fall rates between 10^7V/s and 10^9V/s, which correspond to fall times of between 500ns and 5ns. These show a strongly non-linear relationship

between signal voltage and CLFT, which suggests the presence of significant levels of harmonic distortion in the T&H output signal for these fall times. The plot also shows that CLFT can be much reduced by choosing very slow clock fall rates.

2.1.1.4 Assumptions made in this analysis.

Sheu and Hu based their analysis on the assumptions that:

- the quasi-static approximation holds.
- the charge sheet approximation is appropriate.
- the MOSFET switch was of rectangular shape and uniformly doped.
- second order effects such as:

  a) short and narrow channel effects,

  b) non-linearities of C_{ox} and C_{ol},

  c) charge pumping,

  d) parasitic inductances, resistances and capacitances (other than C_{ol}),

  are negligible.
- V_{in} does not change during turn-off.
- $V_S = V_{in}$, when in effect $V_S = V_h$. This means that the actual i_{ds} is somewhat larger than the one assumed in the model. The single-lump model should therefore overestimate CLFT. The error introduced by this simplification will however remain small as long as $V_{DS} \cong 0$ and therefore $V_{in} \cong V_h$ holds.
- at $t = 0$ the capacitor is fully charged, which means $V_{ds}(t = 0) = 0$ and also $i_{ds}(t = 0) = 0$.
- the source impedance R_S is 0.
- $C_h \gg C_{ol}$ and also $C_h \gg C_{ox}$.
- $v_{ds} \cong 0$ volts throughout the whole of Phase 1 of the turn-off.
- V_G is a linear ramp function falling at a constant rate U from V_H to V_L.
- $|dV_G/dt| \gg |dv_d/dt|$.

- the channel charge splits evenly between Source and Drain, i.e. half of it is associated with the Drain and the other half with the Source node.
- the channel will disappear abruptly at the end of the Phase 1 of turn-off. Related to this are the assumptions that:

  a) sub-threshold mode of conduction is negligible (i.e. the diffusion component of i_{ds} is negligible).

  b) the weak inversion region contribution to CLFT is insignificant.
- the MOSFET does not 'pinch off' at one or both ends while still in strong inversion, i.e. does not enter into the saturation regime or the diffusion mode of conduction during turn-off.
- back-gate bias V_{BS} is constant (during turn-off) and V_T is therefore constant.

$$V_T = V_{T0} + \gamma\left(\sqrt{2\varphi_F - V_{BS}} - \sqrt{2\varphi_F}\right)$$

- the charge-carrier mobility μ is constant.

2.1.1.5 Limitations of the model.

The restrictions imposed on the single-lump model by the assumptions made above mean, that it is only able to predict CLFT accurately for long channel devices driven with medium fast Gate transients, under the condition that CLFT remains small throughout the whole of Phase 1 of turn-off. The single-lump model is expected to somewhat overestimate CLFT, because of the simplification made that $V_S = V_{in}$, when it actually is $V_S = V_{in} + v_d(t)$. For fast transients charge pumping and channel transit time effects, and for slow switching weak inversion (sub-threshold mode) effects may also lessen the models accuracy. Some of the consequences of fast switching are discussed in sections 2.4 and 2.5; and the weak inversion channel charge contribution to CLFT, which becomes more prominent at slow turn-off, is discussed section 2.6.

2.2 Single-lump model extended to $R_S \neq 0\Omega$.

Sheu and Hu realised that the assumption of the signal source impedance R_S being 0Ω, made in the single-lump model (see section 2.1 & [6]) was quite unrealistic, particularly if the input signal to the switch is derived from an on-chip buffer. Such buffer amplifiers, if realised in MOS technology, typically have output impedances of several kΩs or higher. Consequently, they extended their analysis of the basic T&H to include the case $R_S \neq 0\Omega$, [6].

The analytical solution for the case of non zero input resistance ($R_S \neq 0\Omega$) was found to be:

$$\Delta v_d = -\frac{C_{ol}}{C_h}(V_S + V_T - V_L) - U \cdot \left[\frac{C_{ol} + \frac{C_{ox}}{2}}{C_h}\right] \cdot e^{\frac{V_{HT}}{UC_hR_S}} \cdot$$

$$\int_0^{\frac{V_{HT}}{U}} \left[\left[1+\beta R_S(V_{HT} - U\zeta)\right]^{\frac{1}{C_h\beta R_S^2 U}} \cdot \left[2 - \frac{1}{1+\beta R_S(V_{HT} - U\zeta)}\right] \cdot e^{\frac{\zeta}{C_hR_S}}\right] d\zeta$$

Eqn. 2-8

for which, apparently, no closed form solution exists. However, it can be seen that larger R_S will cause more CLFT. This can, at least partly, be overcome by shunting R_S with a capacitor of suitable size, because the capacitor provides the (high frequency) switching transients with a low impedance path to ground. The variable ζ of Eqn. 2-8 is a dummy integration variable whose unit is time.

Fig. 2-4 below (which was reproduced from [6]) clearly shows how providing a shunt capacitor at the input of the T&H circuit can dramatically reduce CLFT under moderate to high source impedance conditions. Circuit parameters were:

$W = 4\mu m$, $L = 3.3\mu m$, $L_D = 0.35\mu m$, $C_h = 2pF$, $t_{ox} = 70nm$, $N_{Sub} = 5\times10^{14}cm^{-3}$, $V_{T0} = 0.6V$,

$V_H = 5V$, $V_L = 0V$, $U = 1V/ns$ and $\mu_n C'_{ox} = 25\mu A/V^2$.

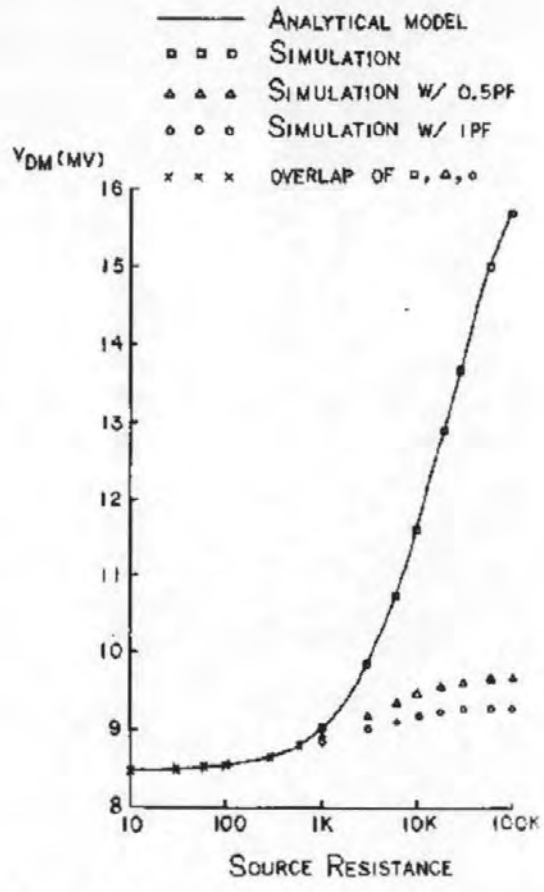


Fig. 2-4: Comparison of the analytic and computer simulated results of the error voltage as a function of source resistance. Computer simulated results with 0.5pF and 1pF capacitance in parallel with R_S are also shown. Reproduced from [6].

2.3 Single-lump model for the floating pass-transistor.

Shieh, Patil and Sheu [20] expanded the single-lump model from section 2.1 to accommodate the case of the floating pass-transistor (Fig. 2-5), which is frequently encountered in switched-capacitor circuits.

Only the CLFT contribution of Phase 1 will be reported on in this section. The contribution of Phase 2 is given by Eqn. 2-6 of the single-lump model (paragraph 2.1.1.2).

Several special cases for the circuit in Fig. 2-5 can be identified:

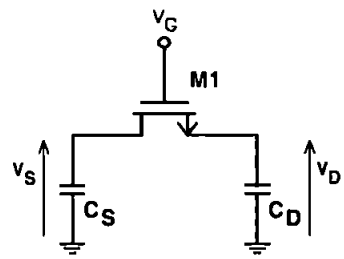


Fig. 2-5: MOS switch with floating Drain and Source.

- $C_S = C_D$:

  $\Delta Q_S = \Delta Q_D$ because the conditions at both nodes are identical; $\therefore \mathbf{\Delta V_S = \Delta V_D}$.

- $C_S \neq C_D$ and high fall rates of V_G:

  $\Delta Q_S = \Delta Q_D$. The short fall time allows for very little communication between C_S and C_D; $\therefore \mathbf{\Delta V_S \neq \Delta V_D}$ due to $C_S \neq C_D$.

- $C_S \neq C_D$ and low fall rates of V_G:

  $\Delta Q_S \neq \Delta Q_D$. A high level of charge sharing between C_S and C_D tends to make $\mathbf{V_S = V_D}$.

For $C_S = C_D$ the channel charge distributes equally between the Source and Drain. Consequently, CLFT is the same for both nodes. This also occurs for fast switching. Here the channel disappears so quickly that there is not enough time for the conductive current (in the channel) to establish charge exchange between C_S and C_D. The channel charge will therefore be equally distributed between the two nodes and the CLFT voltage will depend solely on the size of the respective node capacitance. With very low fall rates the opposite is true. The charges on C_S and C_D can communicate easily, which tends to make $V_S = V_D$.

For any other case the CLFT for each capacitor is found in much the same way as in section 2.1.1, i.e. by assigning half of the Gate charge to each capacitor modified by the charge exchange between the two. The charge exchange is due to the conductive current in the channel, which is a function of v_{ds}.

Hence the CLFT on C_D (at the end of Phase 1) is found to be:

$$v_{dl} = \frac{-1}{C_D}\sqrt{\frac{\pi U}{2\beta}\frac{C_S C_D}{C_S + C_D}}\left(\frac{C_{ox}}{2} + C_{ol}\right)\mathrm{erf}\left(\sqrt{\frac{\beta}{2U}\frac{C_S + C_D}{C_S C_D}}\, V_{HT}\right)$$

Eqn. 2-9

and the CLFT on C_S is:

$$v_{sl} = \frac{-1}{C_S}\sqrt{\frac{\pi U}{2\beta}\frac{C_S C_D}{C_S + C_D}}\left(\frac{C_{ox}}{2} + C_{ol}\right)\mathrm{erf}\left(\sqrt{\frac{\beta}{2U}\frac{C_S + C_D}{C_S C_D}}\, V_{HT}\right)$$

Eqn. 2-10

The total CLFT contribution again is found by adding the Phase 2 contribution, given by Eqn. 2-6 section 2.1.1.2, to Eqn. 2-9 or Eqn. 2-10, depending which node is of interest.

2.4 Distributed model.

Turchetti, Mancini and Masetti [9] as well as Kuo, Dutton and Wooley [7], [17] pointed out that the single-lump model (described in section 2.1) was a quasi-static or steady-state model and therefore not suitable for describing high switching speeds. High switching speed was defined by Kuo et al. as the fall time t_f of the Gate voltage being less than ten times the carrier channel transit time, τ_0, ($t_f < 10\tau_0$), where the charge carrier channel transit time τ_0 is the average time it will take a channel charge to travel the full length of the channel.

$$\tau_0 = \frac{L^2}{\mu V_{GS,max}} \quad \text{where} \quad V_{GS,max} = V_{HT} = V_H - (V_S + V_T)$$

Eqn. 2-11

Under these circumstances the results from the single-lump model are significantly in error, as the plots (Fig. 2-6 and Fig. 2-7) show. These, taken from [7], compare measurements of the basic S&H circuit (Fig. 2-1) to simulations for both fast and slow switching.

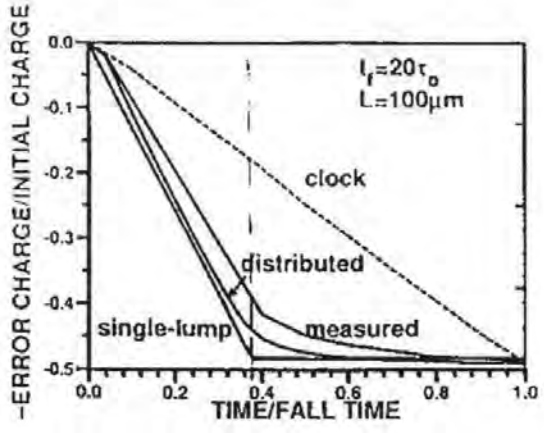


Fig. 2-6: Slow switching (t_f = 900ns) [7].

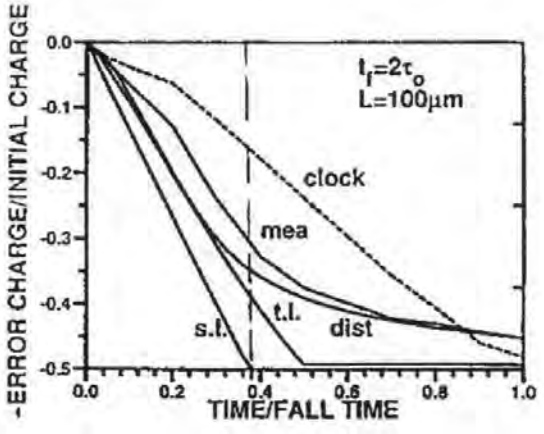


Fig. 2-7: Fast switching (t_f = 90ns) [7].

The test circuit had been manufactured in a 2µm process with the following parameters:

$$W = 100\mu m,\ L = 100\mu m,\ \mu = 500 cm^2/V,\ t_{ox} = 39nm,\ V_{T0} = 0.5V,\ \gamma = 0.3V^{½},\ V_T = 1V,\ V_{in} = 0V,$$

$$V_B = -4V,\ +4V \geq V_G \geq -4V,\ C_h = 210pF$$

For slow switching all models give good representation of the measured (*mea*) behaviour. For fast switching the picture is different. Here the distributed model (*dist*) renders the circuit's behaviour faithfully, whereas the two-lump model, *t.l.* (which will be discussed in section 2.5), and single-lump model, *s.l.* (which was presented in section 2.1), are both in error. This is because the quasi-static approximation, on which both lumped models were based, is violated. Nevertheless, the two-lump model offers considerable improvement over the single-lump model, as explained in section 2.5.

2.4.1 Model description.

The equivalent distributed circuit model of the MOS pass-transistor developed by Kuo et al. does not suffer from the limitations imposed by the quasi-static approximation, because the distributed nature of the real device was taken into account, see Fig. 2-8. In fact, the model is nothing but a simplification of a distributed transistor consisting of N elementary MOS transistors of width W and length L/N all of which are connected in series to imitate a single transistor of length, L, and width, W, where each elementary transistors' point of operation is determined by its very own terminal potentials and currents.

The distributed model of Fig. 2-8 is arrived at, by assuming constant mobility, and neglecting recombination and impact ionisation in the inversion layer as well as weak inversion mode of operation and overlap capacitance. Here the channel is modelled as a series of non-linear voltage controlled resistors, R, each controlled by its individual Gate to Source voltage. The capacitors $C = C_{ox}/N$ represent the distributed Gate capacitance storing the channel charge and the diode J_B models the channel to substrate depletion region in series with the substrate resistivity R_B.

It is through J_B and R_B that the charge pumping current flows to the substrate [10], [11]. Large values for R_B and high built-in voltage for J_B result in low levels of charge pumping.

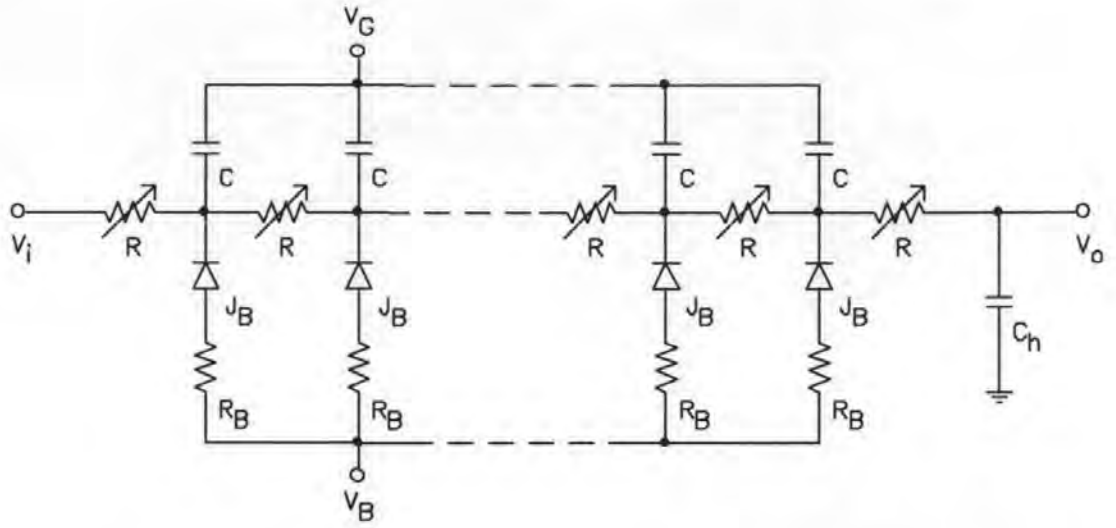


Fig. 2-8: Equivalent distributed circuit model of the S&H amplifier (Fig. 2-1), without parasitics.

For the general case of boundary and initial conditions, the partial differential equation characterising the model (see [7] eqn. (7)) can not be solved analytically, making numerical solution necessary.

2.4.2 Description of the turn-off process.

Fig. 2-9 and Fig. 2-10 are plots of the changes that take place in the charge distribution along the channel during turn-off. These were derived by Kuo, Dutton and Wooley [7] from calculations of the distributed model, that they undertook.

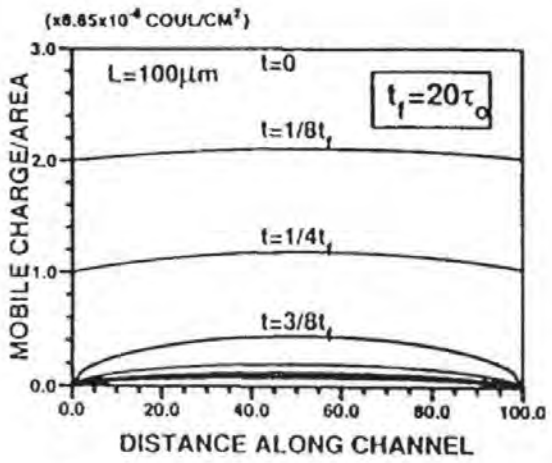


Fig. 2-9: Charge distribution in the inversion layer for slow turn-off [7].

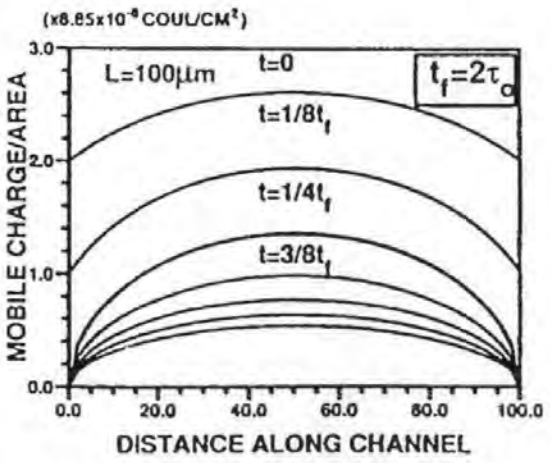


Fig. 2-10: Charge distribution in the inversion layer for fast turn-off [7].

To turn the MOSFET off its Gate voltage, V_G, must fall from the high level, V_H, it was at during the sampling period, to the low level, V_L, of the hold period. In the first period of turn-off the Gate voltage is above the threshold $V_{TH} = V_S + V_T$ and the transistor is working in the linear region. In the case discussed with $V_S = 0V$, $V_T = 1V$ and V_G falling from +4V to -4V at a constant rate, the Gate voltage reaches the threshold voltage at $t = 3/8t_f$, where according to the single-lump model all the channel charge has been evacuated and the transistor enters the 'OFF' state. For slow switching this is very nearly the case with less than 10% of the original charge in the channel remaining (Fig. 2-9). However, for fast switching about a third of the original charge is still left. It was also observed that from $t = 3/8t_f$ onwards the mobile charge at both ends of the channel is zero, implying that no conducting channel exists at these points. This signifies that pinch-off occurs at both ends of the channel effectively trapping the remaining channel charge. For the rest of the turn-off period the transistor stays in this so called diffusion mode of conduction, with the channel pinched-off at both ends.

In this mode the device resembles two back to back connected MOSFETs both operating in the saturation mode (where the centre point acts as a common Source node). The charge removal process is much slower compared to what it was when V_G was above V_T (and the transistor was operating in the linear mode). At the end of the time window ($t = 7/8t_f$) a significant amount of charge (more than 10%) is still left in the channel (Fig. 2-10), which must be removed completely before the MOS transistor finally settles into the 'OFF' state. Channel charge transfer onto the hold capacitor thus continues, until all the charge is evacuated; even after the Gate voltage transient has settled, at V_L.

2.4.3 Observations and issues related to fast turn-off.

2.4.3.1 Steady-state.

The near parabolic charge distribution along the channel during fast switching, observed in Fig. 2-10, is a clear indication that steady-state conditions are violated. In steady-state the channel charge should, under the low V_{DS} condition present, be evenly distributed along the channel, as indeed is the case for ten times slower switching (see Fig. 2-9).

2.4.3.2 Fast switching and channel charge removal.

The fastest removal of the mobile channel charge is through conduction (i.e. when the transistor is in the linear region of operation), which is while V_G is falling towards V_{TH}. At $V_G = V_{TH}$ the charge removal becomes much slower because the MOSFET enters the diffusion mode of conduction in which it stays until all the mobile channel charge has disappeared.

Therefore it would appear that fast switching can be defined as a condition where steady-state conditions are violated i.e. where removal of 'free' channel charge through conduction can not keep up with generation caused by the collapse of the Gate voltage, which means that when the Gate voltage reaches threshold ($V_G = V_{TH}$) a substantial amount of mobile charge is still left in the channel. Because of this we propose to define high speed switching in terms of the time t_{HT} it takes the Gate voltage, V_G, to fall from high, V_H, to threshold, V_{TH} (i.e. the period of time over which removal of charge through conduction can take place), instead of the time t_f it takes the Gate voltage to make the complete transition from high to low.

Using the definitions for the characteristic carrier channel transit time, t_0, under drift dominated conduction conditions and the average charge density in the channel, N(t), at

time t that were given in [21] and Eqn. 1-11 (from chapter 1.3.2) for the channel charge, Q_{inv}, we can derive such a definition. The relevant equations are repeated below:

$$N(t) = N(0)\frac{t_0}{t + t_0}$$

$$t_0 = \frac{\pi L^2 C_{ox}^{'}}{8\mu q N(0)}$$

$$Q_{inv} = qWLN(0) = WLC_{ox}^{'}V_{HT}$$

After some manipulation the following expression that defines fast switching in terms of t_{HT} is arrived at:

$$t_{HT} < \frac{\pi L^2}{8\mu V_{HT}}\left(\frac{100\%}{Q_{\%}} - 1\right)$$

where $Q_{\%}$ is the percentage of Q_{inv} that is deemed acceptable, if left in the channel at the point where the Gate voltage falls below threshold (where $V_G = V_S + V_T$ at which point V_G has fallen by V_{HT}). I.e. $Q_{\%}$ is the percentage of Q_{inv} that may get trapped in the channel and potentially lost to substrate through charge pumping. For $Q_{\%} \ll 100\%$ the expression for t_{HT} may be simplified to:

$$t_{HT} < \frac{\pi L^2}{8\mu V_{HT}}\left(\frac{100\%}{Q_{\%}}\right) = \tau_0 \frac{\pi}{8}\left(\frac{100\%}{Q_{\%}}\right)$$

Eqn. 2-12

This relation is identical to the one given at the start of section 2.4, i.e. $t_f < 10\tau_0$, for $Q_{\%} = 10\%$ and $V_{HT} = (V_H - V_L)3/8$ for which $t_{HT} < 30\tau_0/8$.

Using $t_{HT} = V_{HT}/U$ the following definition of fast switching in terms of clock fall-rate, U, is found:

$$U > \frac{8\mu V_{HT}^2}{\pi L^2}\left(\frac{Q_{\%}}{100\%}\right)$$

Eqn. 2-13

2.4.3.3 CLFT under fast turn-off conditions.

Turchetti, Mancini and Masetti presented a non-quasi-static (NQS) MOSFET model for SPICE which they subsequently used to simulate CLFT in S&H circuits under fast turn-off conditions [9]. Their NQS model was in good agreement with predictions from numerical analysis and the distributed model. Comparison to the single-lump model showed marked differences, particularly at fast turn-off.

Plots comparing these NQS simulation results for the basic S&H circuit of Fig. 2-1 to CLFT predictions made by the single-lump model (section 2.1) are reproduced below. The error voltage plotted, was evaluated at the end of the clock ramp.

Design parameters for the circuit were:

$W = 4\mu m$, $L_{drawn} = 3.3\mu m$, $t_{ox} = 70nm$ the gate capacitance C_G was thus $C_G = C_{PT} = 6.51fF$, $L_D = 0.35\mu m$, $V_{T0} = 0.6V$, $\mu_n = 507cm^2/Vs$, $N_{Sub} = 5\times10^{14}cm^{-3}$; and clock high and low voltages were $V_H = 5V$ and $V_L = 0V$.

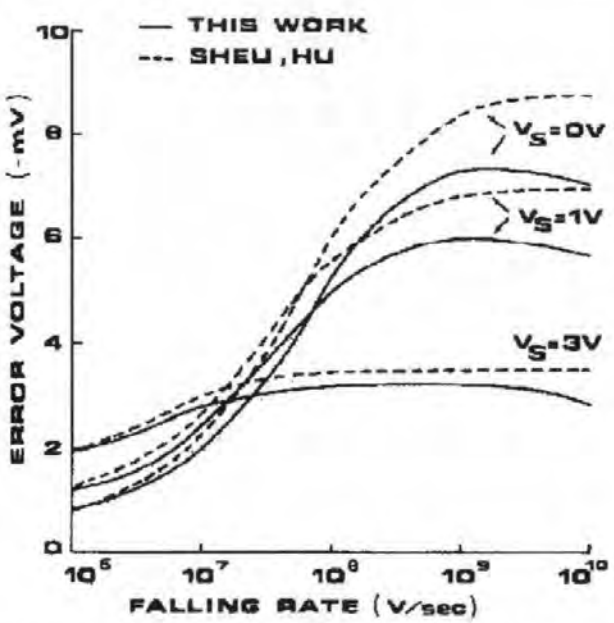


Fig. 2-11: CLFT error at the end of the clock ramp against clock fall-rate with signal voltage as parameter, $C_h = 2pF = 307C_{PT}$. Plot reproduced from [9].

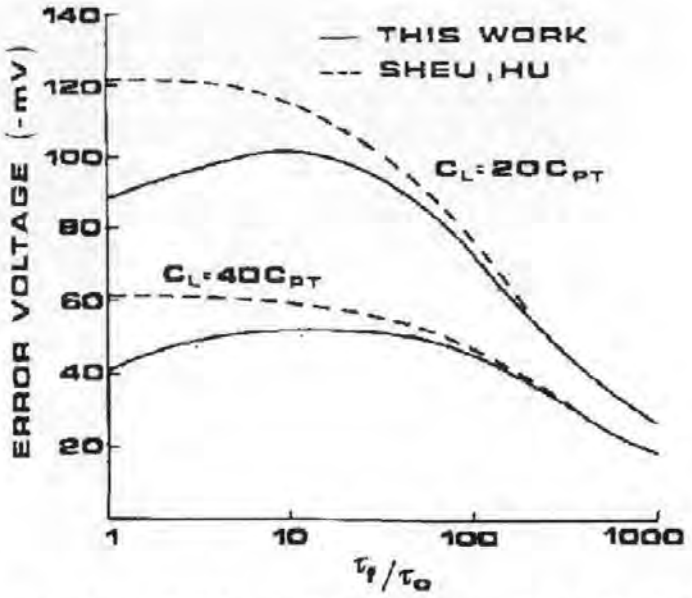


Fig. 2-12: CLFT error at the end of the clock ramp against t_f/τ_0 ratio with $C_h = C_L$ as parameter, $V_S = 0V$ & $\tau_0 = 30.3ps$. Plot reproduced from [9].

These plots clearly show that the single-lump model overestimates the CLFT error when evaluated at the end of the clock ramp, even at relatively slow switching speeds. At higher clock fall-rates the difference between the NQS simulations and the single-lump model becomes even more pronounced.

Of these differences, the peaking of the NQS simulations derived error voltage at $t_f \approx 10\tau_0$, and subsequent reduction in the error voltage for clock fall times shorter than approximately $10\tau_0$, (see Fig. 2-12) can be explained by the release of the trapped inversion layer charges not having been completed at the point where the error voltage was evaluated for these plots, namely at the end of the clock ramp. The single-lump model, being a quasi-static model, can not account for such a delayed release of inversion-layer charges and will therefore overestimate the error voltage at the end of the clock ramp. The expectation is that if CLFT had been evaluated at a fixed time after the start of the clock ramp (e.g. at the end of the clock low period), rather than at the end of the clock ramp, the NQS model would have shown saturation of CLFT at fast fall-times, just like the single-lump model did, albeit at a somewhat lower level.

The markedly lower CLFT levels predicted by the NQS simulations, even at low CLFT levels and relatively slow switching speeds (see Fig. 2-11), arise mainly from differences in the way these two approaches evaluate the channel charge in the pass-transistor during turn-off, and from differences in the side of the MOS switch the transistor's Source terminal is assigned to. In the single-lump model the Source terminal was assigned to the signal source side, whereas the NQS simulation will assign the MOSFET Source terminal correctly to the hold capacitor side. The effect of this is that the single-lump model will assume a smaller 'compensating' channel current i_{ds} for the same v_{ds} across the switch and will also assume a faster collapse of the pass-transistor's V_{GS} and consequently an earlier turning off of the switch. NQS simulations also take the sub-threshold mode of conduction and channel charge inertia into consideration. The combined effect is that NQS simulations predict lower levels of CLFT than the single-lump model.

2.4.3.4 Charge pumping.

During turn-off part of the channel charge may flow to the substrate [10], [11], [22] & [21]. Wegman, et al. [11] found that the amount of channel charge flowing to the substrate $Q_{inj.Bulk}$ was linked to the clock fall-time, t_f, the carrier channel transit time, τ_0, (defined in Eqn. 2-11) and to how close the pass-transistor's Gate voltage, V_G, came to its flat-band voltage, V_{FB} (see Fig. 2-13 below).

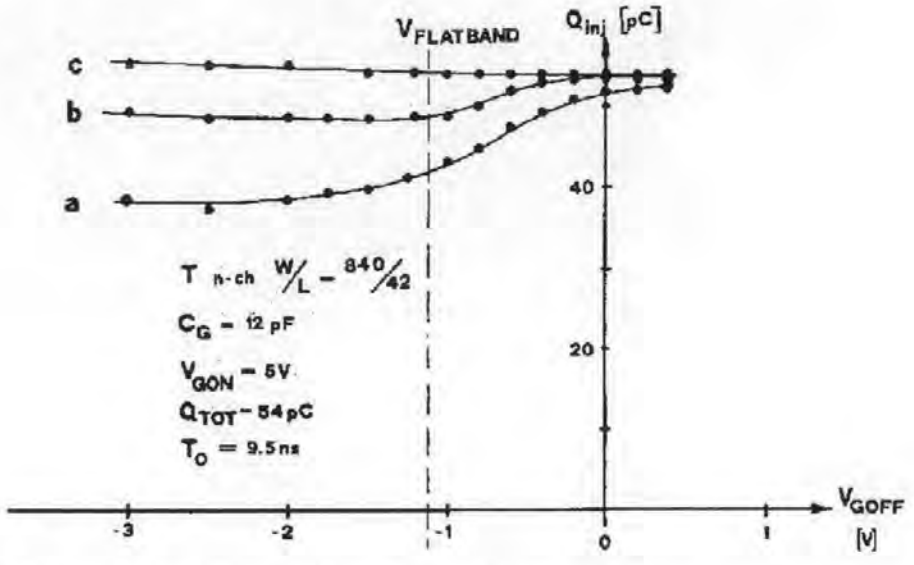


Fig. 2-13: Measured total charge injected Q_{inj} at Drain and Source as a function of the clock low voltage ($V_L = V_{GOFF}$), reproduced from [11].

Measurements had been undertaken on a NMOS floating pass-transistor circuit with: W = 840μm, L = 42μm, ∴ τ_0 = 9.5ns, Q_{inv} = 54pC and V_T = 0.5V. Clock voltage levels were V_H = 5V, V_L = V_{GOFF} and three different clock fall times t_f were considered: a) $t_f = 0.63\tau_0$, b) $t_f = 2.4\tau_0$ and c) $t_f = 42\tau_0$.

They found that virtually none of the channel charge flowed to Bulk if t_f was much longer than τ_0. As t_f approached τ_0 the amount of channel charge diverted to the Bulk became noticeable if the low voltage of the clock, V_L, fell below the substrate voltage. $Q_{inj,Bulk}$ reached a maximum for $V_L \leq V_{FB}$. For $t_f < \tau_0$ the loss of channel charge to the substrate was even more marked, see graph a) of Fig. 2-13. This progressive increase in $Q_{inj,Bulk}$ as V_L approaches V_{FB} can be understood if we consider that, under such fast switching conditions, a significant amount of inversion-layer charge becomes trapped in the channel. Once cut off from the Source and Drain these charges remain effectively trapped in the channel through the Gate oxide on the one side and the depletion region that isolates them from the substrate on the other side. As long as this depletion region remains intact most of the trapped charges will be released through the diffusion mode of conduction to the transistor's Source and Drain (see section 2.4.2) and only few will escape to the substrate. However, if this barrier should disappear, the trapped charges would be free flow to the

substrate instead; and this is exactly what happens when V_G reaches V_{FB} — the depletion region that isolated the trapped charges from the substrate disappears. The thinning of the depletion region (and consequential decrease in its isolation properties) is, of course, a gradual process, which explains the gradual increase in $Q_{inj,Bulk}$ as V_L approaches V_{FB}.

Manufacturing circuits on a weakly doped substrate, and application of the substrate bias via back side contacts only, can also help reduce charge pumping. Kuo et al. [7] found that for their test circuits no more than 5% of the channel charge flowed to substrate (substrate resistivity was 2kΩm and substrate thickness was 400μm); which, as the Gate voltage of their test circuits never fell below V_B, is in line with the observations made in [11]. To prevent latch-up most CMOS circuit layouts will, however, have front side substrate contacts placed near transistors, and will often be manufactured on epi substrate (a low resistivity substrate). Under these low resistivity substrate conditions, higher levels of charge pumping could be expected, especially with large devices [21] and for signal voltages close to the substrate voltage.

2.5 Two-lump model.

Kuo, Dutton and Wooley [7], [17] synthesised the two-lump model (Fig. 2-14) for the basic S&H circuit (Fig. 2-1) from the single-lump model (section 2.1) and their distributed model (discussed in the previous section). This model offers improved precision over the single-lump model because it takes trapping of the channel charge and the resulting diffusion mode of conduction into account. However, it is not quite as precise as the distributed model. But it is also computationally less demanding.

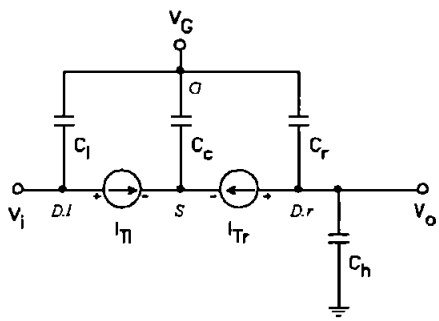


Fig. 2-14: Two-lump model of the S&H circuit (Fig. 2-1), without parasitics.

The equations for the two transport currents are:

$$I_{T,l} = \frac{\mu C_{ox}' W}{pL}\left(V_G - \frac{V_S}{2} - V_T\right)\left(V_{D,l} - V_S\right)$$

Eqn. 2-14

$$I_{T,r} = \frac{\mu C_{ox}' W}{(1-p)L}\left(V_G - \frac{V_{D,r} + V_S}{2} - V_T\right)\left(V_{D,r} - V_S\right)$$

Eqn. 2-15

and the three lumped capacitances are given by:

$$C_l = \frac{C_{ox}}{2p} \qquad C_c = \frac{C_{ox}}{2} \qquad C_r = \frac{C_{ox}}{2(1-p)}$$

The model was found to be the least in error for a channel partitioning factor of p = 0.5.

The main difference between the single- and the two-lump model is that the latter was amended with an additional capacitance C_c at the centre, thus splitting the conducting channel in two. This creates a centre node that can simulate charge trapping. This node also acts as Source for both sections of the model with the potential difference across C_c being $V_c = V_{GS} - V_T$. Thus, it becomes obvious, that the two-lump model will not enter the 'OFF' state unless C_c is fully discharged i.e. $V_c = 0$. In contrast, the single-lump model will cut-off as soon as $V_G = V_o + V_T$. The implications of this are clearly visible in Fig. 2-7, where the two-lump model continues to contribute to CLFT after V_G reached threshold, and the single-lump model stops altogether.

2.5.1 Modes of operation.

For the two-lump model (Fig. 2-14), three regions of operation for each of the two lumped elements can be identified. In order to simplify the analysis $V_{Dl} \equiv V_{Dr}$ was assumed, leaving both lumped elements to work in the same mode of operation. The regions of operation, in the order they are passed through during turn-off, are:

1. $V_{GS} \geq V_T$ and $V_{DS} \leq V_{GS} - V_T$; i.e. $V_c \geq 0$ and $V_{DS} \leq V_c$ (ohmic region):

   The MOSFET is in the linear mode of conduction and the transport currents I_{Tr} and I_{Tl} are found from Eqn. 2-14 and Eqn. 2-15. Accordingly the two-lump model stays in the linear mode of operation until V_{GS} has fallen below V_T, which can be considerable time after $V_G - V_o$ has fallen below V_T (see Fig. 2-7).

2. $V_{GS} \geq V_T$ and $V_{DS} > V_{GS} - V_T$; i.e. $V_c \geq 0$ and $V_{DS} \leq V_c$ (diffusion mode):

   In the diffusion mode of conduction the device acts like two cascaded transistors each working in saturation (see Fig. 2-14) with the centre node still acting as Source. This mode is governed by the following two (saturation mode) equations

$$I_{T,l} = \frac{\mu C'_{ox} W}{2pL}\left(V_G - V_S - V_T\right)^2\left[1 + \lambda\left(V_{D,l} - V_S\right)\right]$$

Eqn. 2-16

$$I_{T,r} = \frac{\mu C'_{ox} W}{2(1-p)L}\left(V_{GS} - V_S - V_T\right)^2\left[1 + \lambda\left(V_{D,r} - V_S\right)\right]$$

Eqn. 2-17

   Charge removal from C_c is much slower now than in the previous phase. The model stays in the diffusion mode until C_c is completely discharged, i.e. $V_{GS} = V_T$. In their calculations Kuo et al neglected this mode entirely [17]. Instead they assumed that both sections were in the linear mode whilst V_c was greater than zero.

3. $V_{GS} < V_T$, $Q_c = 0$:

   Under these conditions all the mobile channel charge is evacuated and the transistor is turned off completely. No transport current flows.

2.5.2 Discussion of the model.

Kuo et al neglected overlap capacitance and charge pumping. This they could do safely because in their experiments large transistors, built on a highly resistive substrate, were used. Also, they did not take the diffusion mode into account. Instead Eqn. 2-14 and Eqn. 2-15, both identical to the SPICE Level 1 model for the Drain current in the linear region, were used to model the respective transport current components throughout the whole of turn-off. Smaller transistors may require that these effects are taken into account.

The two-lump model's channel partitioning factor, p, was arrived at by comparing results to the distributed model. It was found that $p = 0.5$ gave the best agreement between both models, thus $C_l = C_r = \frac{1}{4}C_{ox}$ and $C_c = \frac{1}{2}C_{ox}$ were found to work best [17].

2.5.2.1 Advantages.

The two-lump model approximates the transient behaviour of the pass-transistor more accurately than the single-lump model, because it can recreate the trapping of inversion layer charges, with the resulting prolonged flow of I_{Tl} and I_{Tr} (both may continue to flow for $V_G < V_o + V_T$). Asymmetrical behaviour of non-rectangular shaped and non-uniformly doped MOSFETs (see chapter 5.3 for a description of these devices and their impact on CLFT) can also be modelled much more readily. Also, the two-lump model is computationally less demanding than the distributed model, particularly if the diffusion mode of conduction is not taken into account, as proposed by Kuo et al [17].

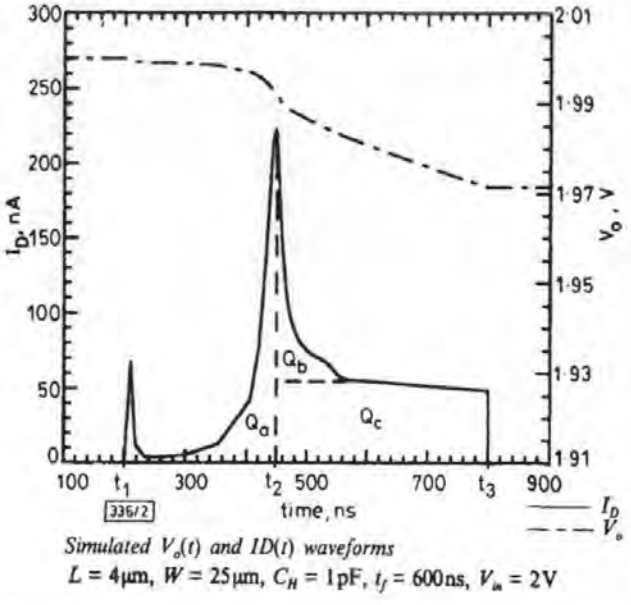
2.5.2.2 Disadvantages.

The two-lump model does not represent the fast transient behaviour of the MOS switch as well as the distributed model; and even though the model is quite simple, its equations can still only be solved numerically.

2.6 Weak inversion channel charge contribution to CLFT.

Chen et al. [12], [13] reported on the observation of a third, previously unaccounted for, CLFT component which they attributed to channel charges in weak inversion. Their observation lead to the development of a new, extended single-lump model for CLFT by Gu and Chen [14], which could account for the newly observed weak inversion channel charge contribution to CLFT. This model was an extension of the single-lump model of Sheu and Hu [6] (reported on in section 2.1) which took only two charge injection components into account; namely Q_1, due to the Gate charge in the strong inversion region, and Q_2, solely due to the overlap capacitance. The new model was verified by mixed-mode simulations and measurements on actual silicon.

2.6.1 Transistor turn-off & identification of the weak inversion CLFT component.



Simulated $V_o(t)$ and $ID(t)$ waveforms
L = 4μm, W = 25μm, C_H = 1pF, t_f = 600ns, V_{in} = 2V

Fig. 2-15: The three charge injection components, reproduced from ref. [12].

At t_1 (see Fig. 2-15) the Gate signal V_G starts to fall from V_H towards V_L. During this first period of switch-off the transistor M1 is 'on' and the channel is assumed to be in strong inversion. The part of the channel charge transferred to the hold capacitor C_h during this phase, shown as Q_a of Fig. 2-15, is identical with Q_1 of the single-lump model.

At t_2 the threshold voltage V_T is reached and M1 enters Phase 2 of the turn-off, which finishes at t_3 where V_G reaches V_L. For the single-lump model the assumption was that the channel was fully depleted after t_2, and that no current could flow from Drain to Source,

since the transistor was 'off'. The Phase 2 contribution Q_2 could therefore only be due to C_{ol}, which implied that the current I_D had to be constant throughout Phase 2 (since V_G was assumed to fall at a constant rate) and $Q_b = 0$. This is clearly not the case, else I_D would have to fall instantaneously from the peak at t_2 to a constant level maintained until the end of turn-off is reached. Chen et al. reasoned that this discrepancy between observations and the single-lump model ($Q_b \neq 0$) was the manifestation of a weak inversion effect.

2.6.2 Modelling of the weak inversion channel charge contribution to CLFT.

In [14] Gu and Chen proposed a quantitative analytical model for CLFT which could explain this weak inversion contribution to CLFT. They arrived at their model by adding a weak inversion CLFT component to the lumped-model of Sheu & Hu [6], which was discussed in section 2.1. This extended lumped-model for CLFT was shown to be in excellent agreement with mixed-mode simulations and measurements performed on S&H integrated in a 1.2μm CMOS process.

The extended lumped-model states that CLFT arises from three distinct charge components being transferred to the hold capacitor while the MOS transistor switch (in the S&H) is being turned off:

$$CLFT = \frac{Q_a + Q_b + Q_c}{C_h}$$

Here the charge components Q_a and Q_c correspond to the lumped-model's Phase 1 and Phase 2 contributions to CLFT, discussed in sections 2.1.1.1 and 2.1.1.2 respectively, and Q_b is the additional weak inversion contribution, for which Gu and Chen [14] proposed the following expression:

$$Q_b = W\frac{Q_I(\phi_{so})L}{2} + W\left(\int_{\frac{L}{2}-\Delta L}^{\frac{L}{2}} Q_I(\phi_s)\,dx - Q_I(\phi_{so})\Delta L\right)$$

Eqn. 2-18

Gu and Chen arrived at this expression by assuming that the amount of channel charge responsible for Q_b could be evaluated singly at the transition between Phase 1 and Phase 2 of the transistor turn-off (which corresponds to t_2 in Fig. 2-15); or in other words at the point where the transistor leaves the strong inversion regime. Half of this channel charge would then flow to the Source and the other half to the Drain, giving rise to Q_b.

For the above assumption to hold the Drain to Source current i_{ds} in the device must be 0 after t_2. This view is compatible with the single-lump model where the transistor was considered in the 'off-state', i.e. $i_{ds} = 0$, after t_2 (see section 2.1), and therefore allows seamless expansion of the single-lump model with Eqn. 2-18.

Two-dimensional device simulations and mixed-mode simulations supported the validity of this assumption. They showed that Drain and Source currents were identical after t_2, implying that no Drain to Source current was flowing in the MOSFET after t_2 (see Fig. 2-16, where I_D is the same size as I_S after t_2).

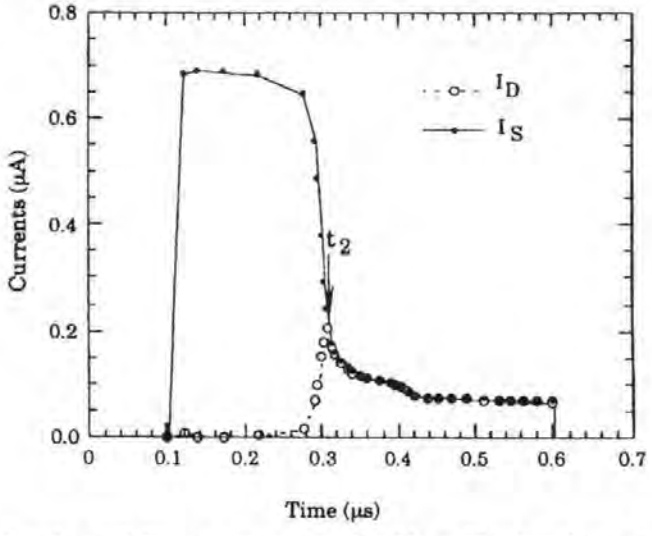


Fig. 2-16: Simulated Drain and Source currents for V_{in} = 2V, L = 2μm and t_f = 500ns; [14].

These simulations also gave evidence that loss of channel charges through recombination of channel electrons with substrate holes was negligible (the recombination current had a value of about 0.1nA). All of which leads to the conclusion that Q_b can indeed be determined by evaluating the amount of channel charge remaining in the device at t_2.

To evaluate the amount of channel charge remaining in the device at t_2 Gu and Chen assumed that the depletion region under the Gate of the MOS transistor could be modelled by splitting into three distinct regions: a Gate modulation region and the Source and Drain modulation regions ΔL (see Fig. 2-17 below).

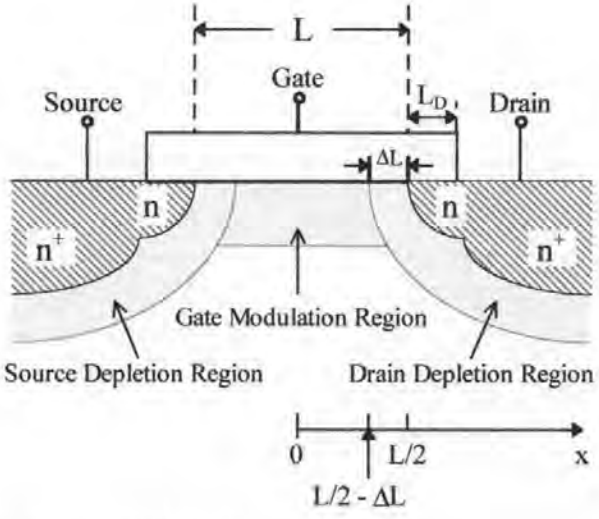


Fig. 2-17: Cross-section of the MOSFET in weak inversion.

Here the Gate modulation region is assumed to be a region of uniform density of channel charge carriers under the Gate of the MOSFET; and the Source and Drain modulation regions ΔL, are the regions in which the charge density increases from the low level in the Gate modulation region to the high levels seen in the Drain and Source implants. These Source and Drain modulation regions ΔL were assumed virtually identical and symmetrical about the mid-channel point of the transistor, which seems reasonable since both the Drain and Source voltages differ only by a relatively small amount, the CLFT.

Evidence for symmetrical channel charge distribution was produced by simulations that showed how surface electron density along the channel changed with time during turn-off. The example given in Fig. 2-18, clearly shows symmetrical charge distribution in the channel during Phase 2 of the transistor turn-off.

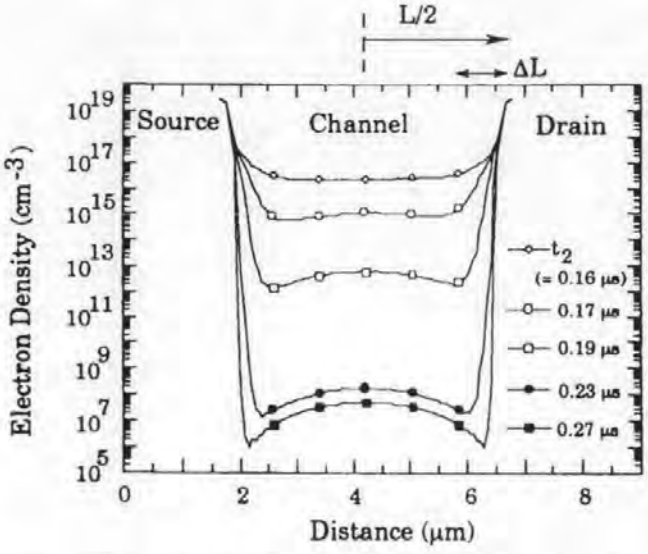


Fig. 2-18: Simulated surface electron density distribution after t_2 for V_{in} = 2V, L = 5μm and t_f = 500ns; reproduced from [14].

Gu and Chen asserted that, because of $N_A \ll N_D$, the length ΔL of the surface depletion region at the Drain could be described using the abrupt depletion approximation (i.e. assuming a one-sided junction):

$$\Delta L = \sqrt{\frac{2\varepsilon_{Si}}{q N_A}(V_{in} + V_{bi} - \phi_{so})}$$

Eqn. 2-19

Here V_{bi} was the built-in potential of the depletion region ΔL; and ϕ_{so} the surface potential in the Gate modulation region (see Fig. 2-17) was expressed as:

$$\phi_{so} = V_{in} + V_T - V_{FB} - \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{Si}N_A}\sqrt{\phi_{so} + \frac{k_B T}{q} e^{\frac{(\phi_{so} - V_{in})q}{k_B T} - 2\ln\left(\frac{N_A}{n_i}\right)}}$$

Eqn. 2-20

Here k_B is the notation chosen for the Boltzmann constant.

Channel charge density Q_I, the other factor affecting Eqn. 2-18, was worked out as follows:

$$Q_I = \sqrt{2q\varepsilon_{Si}N_A}\left(\sqrt{\phi_s + \frac{k_B T}{q} e^{\frac{(\phi_s - V_{in})q}{k_B T} - 2\ln\left(\frac{N_A}{n_i}\right)}} - \sqrt{\phi_s}\right)$$

Eqn. 2-21

Since abrupt depletion approximation had been used for modelling the Drain depletion region, the surface potential, ϕ_s, along the channel could simply be expressed by piecewise linear approximation:

$$\phi_s = \begin{cases} \phi_{so} & , 0 \le x \le \frac{L}{2} - \Delta L \\ \phi_{so} + \frac{qN_A}{2\varepsilon_{Si}}\left(x - \frac{L}{2} + \Delta L\right)^2 & , \frac{L}{2} - \Delta L \le x \le \frac{L}{2} \end{cases}$$

Eqn. 2-22

This description of ϕ_s is continuous along the channel and also differentially continuous at the point of transition, x, between the Gate modulation region and the Drain depletion region ($x = L/2 - \Delta L$).

Simulations of ϕ_s were shown to be in good agreement with Eqn. 2-22. An example plot for ϕ_s at t_2, reproduced in Fig. 2-19, shows that the surface potential in the Gate modulation region is fairly constant, as required by the first line of Eqn. 2-22. It also shows, in accordance with the second line of Eqn. 2-22, ϕ_s rising rapidly from ϕ_{so} to the Drain potential.

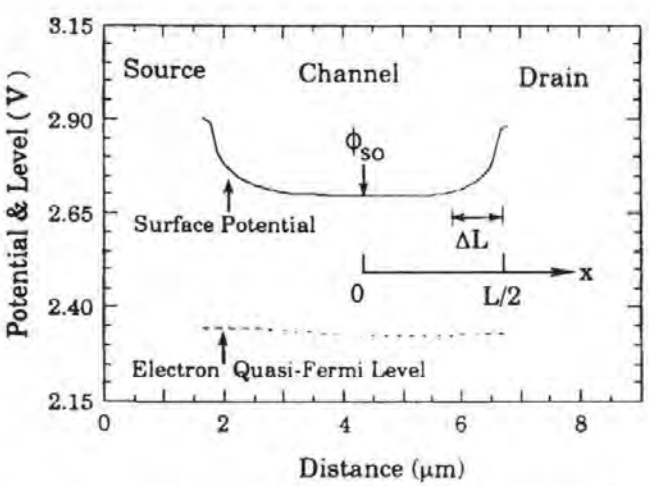


Fig. 2-19: Simulated surface potential and electron quasi-Fermi level for V_{in} = 2V, L = 5μm and t_f = 500ns; reproduced from [14].

A system of equations has now been established that allows evaluation of the amount of channel charge left in the MOS device at t_2. All that is left to do to find Q_b (as expressed in

Eqn. 2-18) is to integrate the channel charge from mid-channel to the edge of the Drain (i.e. from 0 to L/2 in Fig. 2-17).

2.6.3 Comparison of the proposed model to measurements and simulations.

Gu and Chen [14] performed mixed-mode simulations using the two-dimensional device simulation program MEDICI, which supported the attribution of Q_b to channel charges in weak inversion. These simulations indicated that the charge components Q_a and Q_c were modelled correctly by the analytical equations of Sheu & Hu's single-lump model ([6] & section 2.1). Accordingly:

$$Q_a = v_{d1}\, C_h \text{ (from Eqn. 2-5) and } Q_c = v_{d2}\, C_h \text{ (from Eqn. 2-6).}$$

Measurements performed on three basic T&H amplifiers similar to one shown in Fig. 2-1 were also reported in [14]. These circuits were integrated in a 1.2μm twin-well double-metal double-poly CMOS process, having drawn Gate lengths of 2μm, 4μm and 5μm, respectively. Other circuit parameters were:

$$W = 25\mu m,\ t_{ox} = 25nm,\ C_{ol} = 7.76fF,\ N_A = 6.0\times10^{16}cm^{-3},\ V_{FB} = -0.5V,\ V_B = 0V,\ C_h = 1pF,$$

$$2V \geq V_{in} \geq 1V,\ V_H = 5V,\ V_L = 0V,\ V_H \geq V_G \geq V_L.$$

The turn-off transients (on V_G) were linear ramps with fall times between 50ns and 5μs. For the fall rates studied Q_b contributions of between 30% (t_f = 5μs) and 10% (t_f = 50ns) of CLFT were reported for the 25μm×5μm device with V_{in} = 1V. This was in good agreement with both measurements and the proposed model.

2.6.4 Summary and brief analysis of the weak inversion contribution to CLFT.

If Eqn. 2-18 is rewritten, such that its terms are separated according to the part of the transistor from which they arise the expression for Q_b is found as:

$$Q_b = W\frac{L-2\Delta L}{2}Q_I(\phi_{so}) + W\int_{\frac{L}{2}-\Delta L}^{\frac{L}{2}} Q_I(\phi_s)\,dx$$

Eqn. 2-23

Here, the first term is directly proportional to the size of the Gate modulation region, i.e. to both length and width of the transistor; and the second term is proportional to the size of the Drain depletion region, i.e. proportional to the width of the device but independent of its length. It is interesting to note that there are no circuit related terms, like clock fall-time or hold capacitance, to be found in Eqn. 2-23, which means that Q_b is independent of these. Q_b is, however, a function of the transistors channel charge density Q_I (Eqn. 2-21), which increases with V_{in} [14]. As a result Q_b will also increase with V_{in}. If we take, for example, the 25μm×5μm device of section 2.6.3, we find that Q_b will increase from ≈ 9fC to ≈ 12fC if V_{in} is increased from 1V to 2V [14]. This means that the weak inversion contribution to CLFT will be biggest for slow turn-off transients and high signal voltages, where relative size of the C_{ol} contribution to CLFT will also be highest.

The switching speeds encountered in today's mixed-signal designs are about a factor of 1000 faster (t_f is commonly in the range of 50ps to 5ns) than the ones used in the study of the weak inversion effect (where t_f was between 50ns and 5μs). With so much faster switching one would expect the weak inversion contribution to CLFT to make up a significantly smaller percentage of the total CLFT error than the 10% to 30% reported. Since we know that under fast switching conditions approximately 50% of the channel charge will be diverted to the hold capacitor, we can attempt to estimate what proportion of CLFT will be due to Q_b under fast switching conditions. If we take the 25μm×5μm device

from the example above we know that $Q_b \approx 9fC$ for $V_{in} = 1V$. Using the transistor parameters given in section 2.6.3 we find that the error charge on the hold capacitor is approximately 270fC at $V_{in} = 1V$*, meaning that for this device Q_b should be $\approx 3.3\%$ of the total CLFT at 1V, under fast switching conditions.

* $C_{ox} = 157.1fF$, $C_{ol} = 7.76fF$ $V_H = 5V$, $V_L = 0V$ and $V_{TH} \cong 2.05V$ at $V_{in} = 1V$

2.7 Semi-empirical model for CLFT.

A different approach, to those mentioned previously, was taken by David MacQuigg [15]. He developed a semi-empirical model for the basic track-and-hold amplifier (Fig. 2-1). His goal was to find a simple, computationally efficient, equation for the residual charge left on the hold capacitor at the end of the turn-off period, i.e. for CLFT.

2.7.1 Model description.

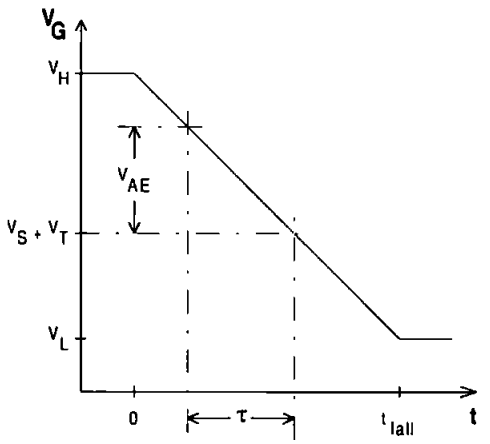


Fig. 2-20: Turn-off transient of the Gate voltage.

MacQuigg started with a simple circuit model, almost identical to the single-lump model (see Fig. 2-2); only, he assumed an idealised transistor switch with $R_{DS} = 0\Omega$ in the sampling period. This led him to identify three regions in the transition from sample to hold mode (see Fig. 2-20). Each region was defined in terms of the net amount of error charge it contributed to CLFT. The first region was contributing zero, the second had net contributions from both channel charge and overlap capacitance, and in the third only the overlap capacitance contributed. This defined the three regions of the model as follows:

1. $V_H \geq V_G > V_{AE} + V_S + V_T$

   $R_{DS} = 0$, $C_{GD} + C_{ol}$ contribute $\therefore Q_1 = 0$; no contribution because of $R_{DS} = 0$.

2. $V_{AE} + V_S + V_T \geq V_G > V_S + V_T$

   $R_{DS} = \infty$, $C_{GD} + C_{ol}$ contribute $\therefore Q_2 = (C_{ol} + C_{GD})\, V_{AE}$

3. $V_S + V_T \geq V_G \geq V_L$

   $R_{DS} = \infty$, only C_{ol} contributes $\therefore Q_3 = C_{ol}\,(V_S + V_T - V_L)$

We see immediately that the third region's contribution is identical to the Phase 2 contribution of the single-lump model (Eqn. 2-6). For the calculation of V_{AE} (which is the only signal dependent term in the second regions contribution) MacQuigg proposed the following equation:

$$V_{AE} = \left[V_{HT}^{b} + \sqrt{\left(\frac{aC_h U}{\beta} \right)^{b}} \right]^{-\frac{1}{b}} V_{HT} \sqrt{\frac{aC_h U}{\beta}}$$

Eqn. 2-24

Thus we arrive at the final expression for CLFT:

$$v_d = \frac{\frac{C_{ox}}{2} + C_{ol}}{C_h} V_{AE} + \frac{C_{ol}}{C_h} (V_S + V_T - V_L)$$

Eqn. 2-25

V_{AE} can be adjusted with the coefficients a and b to provide best fit between calculated and observed CLFT. The coefficient 'a' is included for sub-threshold conduction (a large value for 'a' means a lesser influence, i.e. CLFT reaches maximum for lower fall rates). For high fall rates V_{AE} must approach V_{HT} (an increase in Q_2 is expected since there is less time for the compensating current to flow, thus V_{AE} must increase.). This was accounted for by giving the expression for V_{AE} (Eqn. 2-24) the general form of:

$$V_{AE} = \frac{V_{HT} V(aU)}{V_{HT} + V(aU)}$$

We can now see that V_{AE} approaches V_{HT} for large U (i.e. for $V(aU) \gg V_{HT}$).

The factor 'b' of Eqn. 2-24 adjusts the gradient of this transition. MacQuigg suggested a = 1 and b = 3 for adequate fit. The fall rate of the clock $U = dV_G/dt$ was assumed constant, but need not be.

2.7.2 Comparison with the single-lump model.

A comparison between Sheu & Hu's single-lump model (section 2.1) and MacQuigg's semi-empirical model, shows how well the latter can perform. The difference between the two, taking the single-lump model as reference, is plotted over the absolute fall rate of the Gate voltage (see Fig. 2-21 below). This difference was worked out as follows:

$$\text{difference} = y(x) = (CLFT_{Sheu}(x) - CLFT_{McQuigg}(x))*100\% / CLFT_{Sheu}(x)$$

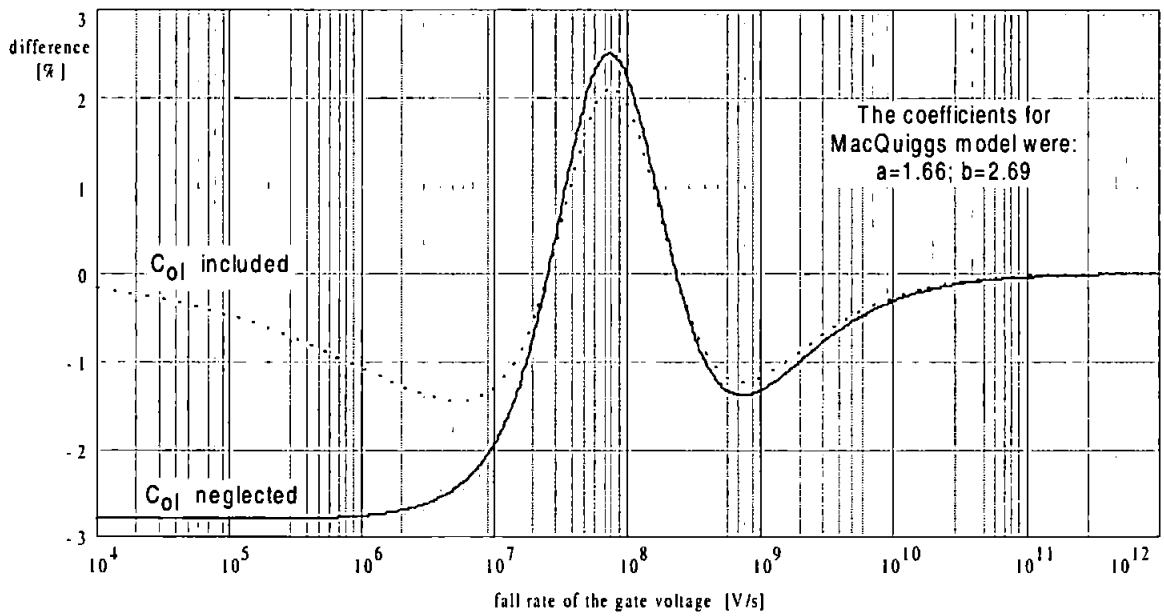


Fig. 2-21: Comparison between the single-lump model and the semi-empirical model.

Here the parameters common to both models were:

C_h = 1pF, C_{ol} = 0.69fF, C_{ox} = 6.5fF, β = 30μS, V_T = 2V, V_H = 5V, V_L = 0V therefore V_{HT} = 3V;

and the curve fitting coefficients for the semi-empirical model were: a = 1.66 and b= 2.69. With these coefficients, excellent agreement between both models was achieved. The difference was less than 3% for C_{ol} = 0, and even smaller if the overlap capacitance C_{ol} was taken into account. If the two models were compared to real circuit behaviour the semi-empirical model may render it better, since it can be adjusted to match observations. For fast switching, for example, the single-lump model may be considerably in error (see section 2.5); this need not be the case for the semi-empirical model which can be made to fit. For very large U both models will yield the same results.

2.8 Use of simulators for estimating CLFT.

Most simulators will estimate CLFT implicitly when performing a transient analysis on a S&H circuit, or indeed on any SC circuit. The only prerequisite for this is that the simulator includes the reduction in channel charge and the transport current in the MOS pass-transistor switch during turn-off in its models. Whether a simulator will also account for the non-linearities in CLFT correctly, depends to a large extend on how the dynamics of a clocked circuit are evaluated, and whether higher-order effects such as, for example, the non-linear voltage-dependency of junction capacitances or the body effect in MOS transistors were included in the models [23].

The type of simulator employed gives some indication about its capabilities. Most analog simulator packages will fall into one of three categories:

1. Two and three dimensional device simulators.
2. Circuit simulators like SPICE and Spectre.
3. Simulators using semi-empirical and empirical models.

Generally speaking, simulators further down the list take fewer boundary conditions into account and make more assumptions and simplifications in the modelling process. Conversely, computational efficiency tends to increase. This is a very desirable property for computer simulation of large circuits, where the use of empirical models can lead to considerable savings in simulation time.

Empirical models are, however, very dependent on the quality of the dataset they were made to fit and can be seriously in error if any parameter falls outside the region over which the model was validated. This is a major disadvantage of empirical models, and one that should be kept in mind when using them. It stems from the way in which empirical models are built. They use mathematical curve fitting functions to approximate the

behaviour observed in the original dataset. Often, no attempt is made at finding a synthesis between device physics and the model. The result is that empirical models can be severely in error if used outside the region of validation; occasionally, they may even fail within these boundaries.

At the other extreme of the spectrum are the physics based numerical analysis packages, the two and three dimensional simulators, whose results are valid under all operating conditions. However, these can be difficult and time consuming to set up, due to the large number of parameters involved. Often, circuit designers will not have access to all the process information required to set up these simulations. Another disadvantage of two and three dimensional simulations is that these require much computer time. However, their big advantage is, that they can offer deep insights into the actual dynamics of transistor turn-off and CLFT, see section 2.6.

Circuit simulators are the design engineers main tool for verifying circuit performance. The models that these employ are often based on the same device level equations, or more advanced and evolved versions of these, than the analytical CLFT models (presented earlier in this chapter) were based upon. The results from simulators that employ such physics based models (i.e. all device simulators and most circuit simulators) should therefore exhibit at least the same level of accuracy as the analytical CLFT models. Normally, one would expect better accuracy from simulators, as their models include more parasitics and higher order effects than were considered in the, simpler, analytical models [6], [24] and [25].

A significant advantage of physics based simulators and models over empirical ones is that physics based models yield qualitatively correct results as long as the underlying physical models are valid and correct and the assumptions made are not violated too badly. Physics based models can, to some degree, even be used for making predictions about circuit

behaviour outside the solution space for which they were intended; as a physics based model will normally show only a gradual deterioration in accuracy, where empirical models may fail catastrophically. The diffusion mode of conduction (discussed in section 2.4) is an example of how a violation in one of these assumptions, namely a break down of the quasi-static approximation under very fast switching conditions [1], can affect the validity of physics based models, and that of physics based circuit simulators.

A feature of many modern circuit simulators is that they employ specialised models for a MOSFET's different modes of operation. SPICE and its derivatives, for example, employ separate model equations to cover the MOS transistor's strong inversion and weak inversion regions (the weak inversion region is also known as sub-threshold region). If a transistor passes from one mode of operation to another these simulators will have to perform model switching. This can lead to discontinuities at the point of transition between the two modes. Modern transistor models like BSIM3 eliminate these discontinuities by incorporating mathematical smoothing functions and curve fitting parameters in the model [26]. The downside of this mathematical 'wizardry' is that the BSIM3 model is something of a hybrid. It is based on device physics, but also contains curve fitting parameters similar to the ones employed in the empirical models. This means that a BSIM3 based transistor model could potentially exhibit some of the 'quirks' of the empirical models (the interested reader may wish to consult [26] for a detailed treatment of these modelling issues).

Absolute accuracy of any model or simulation result is subject to both processing spread, and random/statistical variations of the actual manufacturing process [27], [28] and [29]. Manufacturing tolerances for many parameters (such as oxide thickness, threshold voltage, sheet resistance) are often in the region of between 5% and 40%. Because of these large variations in process parameters only estimates for the typical value, and perhaps the

absolute limits of a circuit's expected CLFT error can realistically be expected from calculations and simulations.

Despite all these limitations, most (physics based) circuit simulators will give reasonably accurate results. Circuit simulators should also provide more accurate results than the analytical models, since they will generally take a greater number of circuit parameters and parasitics into account. Most IC design suites will also allow extracted or back-annotated simulation of the laid out circuit. Such an extracted simulation will typically incorporate estimates of the layout specific parasitic interconnect capacitances, and possibly the metal interconnect, contact and via resistances.

All these factors make circuit simulators an indispensable tool for design and verification of MOS integrated circuits. It also means that results from simulations (particularly extracted simulations) will almost certainly be more accurate than the results gleaned from the analytical models (this view was supported by results from the test chip, discussed in chapter 7, which showed that simulations generally reproduced circuit behaviour more faithfully than the analytical models). However, analytical models do offer valuable insights into the underlying mechanisms that govern a circuits' behaviour, and aid understanding of the circuit. They reveal a circuit's limitations much more readily than simulations and are very useful for developing optimisation strategies and establishing the likely trade-offs that may have to be made.

The interested reader may wish to consult references [3], [4] for further reading on semiconductor physics, references [26] and [1] on device modelling and reference [30] on the SPICE and Spectre circuit simulators. SPICE Level 1 and Level 2 models are explained in more detail in references [5] and [31].

2.9 Summary of CLFT modelling and theory.

The preceding overview of CLFT theory showed that a S&H circuit's transfer characteristic, and its noise and distortion levels, are affected by CLFT. It was found that CLFT adds a non-linearly signal dependent offset component to the sampled signal.

The pass-transistor's Gate-overlap capacitance, C_{ol}, and inversion layer charge, Q_{inv}, were identified as the two main sources of charge that are driving CLFT. Of these the C_{ol} charge is directly proportional to V_{in}, whereas Q_{inv} is a non-linear function of the pass-transistor's Source voltage (see chapter 1.3.2). A further component, the Drain to Source current, i_{ds}, of the pass-transistor was found to be of great importance, too. This transport current, i_{ds}, only flows during Phase 1 of the turn-off, i.e. while the transistor has not entered the cutoff region (while $V_{GS} \geq V_T$). It enables communication between the pass-transistor's Drain and Source terminals and strives to equalise the transistor's Drain and Source potentials.

Dynamic interaction between these three components governs the redistribution of the pass-transistor's Gate charge to its Drain and Source terminals (see section 2.1) during the Phase 1 of the turn-off. It was found that this charge redistribution process is strongly dependent on the actual clock dynamics (clock fall-rate, clock high and clock low voltages), the signal voltage, the dimensions of the MOSFET and the dynamics of the apparent load impedances that are connected to the pass-transistor's Source and Drain terminals [32], [33]. These interactions are complicated by the fact that during turn-off the MOS transistor switch is driven through all modes of operation, and that in each of these modes the transport current is governed by different mechanisms (and therefore model equations).

2.9.1 The two phases of pass-transistor turn-off.

The preceding overview of CLFT theory has shown that two major phases to the pass-transistor turn-off that can be identified. The first phase (Phase 1) is entered when the turn-off transient is initiated by the Gate voltage starting to fall from its high level, V_H, towards its low level, V_L. The device will remain in Phase 1 for as long as a conducting channel exists between its Drain and Source terminals. As the Gate voltage continues to fall, this conducting channel will get progressively weaker and will eventually disappear as the Gate voltage falls below its threshold voltage. At this point the pass-transistor enters the second phase (Phase 2) of turn-off. In this phase the transistor's Drain and Source terminals are no longer connected by a conducting channel and the pass-transistor is said to have turned 'OFF'. The Phase 2, and pass-transistor turn-off, come to an end when the Gate control voltage reaches V_L and all the minority carriers have been removed from the channel region.

Assuming that the channel charge distributes evenly between Drain and Source (50% each) and that, during the whole of the turn-off transient, no significant charge exchange will take place between Drain and Source ($q_{ds} = 0$) then the Phase 1 contribution to CLFT is found to be simply:

$$CLFT_{Phase1} = \frac{C_{ol} + \frac{C_{ox}}{2}}{C_h}\left[V_H - (V_S + V_T)\right]\Bigg|_{q_{ds}=0}$$

Eqn. 2-26

i.e. the potential change that is being induced across the hold capacitor, C_h, by an error charge that amounts to half of the transistor's inversion layer charge, plus the charge that is being released by C_{ol} during Phase 1.

This is the Phase 1 contribution for any balanced S&H circuit where the pass-transistor Drain and Source terminating impedances are identical (the floating pass-transistor with $C_S = C_D$ is an example of such a circuit, see section 2.3). Also it is the limiting case under fast switching conditions, when there is not enough time for a significant charge exchange between the Drain and Source nodes to take place during turn-off (see sections 2.4 and 2.5), i.e. when:

$$\lim_{t_{Phase1} \to 0} q_{ds} = \int_0^{t_{Phase1}} i_{ds}\, dt \cong 0.$$

At slower switching speeds the time spent in Phase 1 is increased and the impact of the transport current i_{ds} on the Phase 1 contribution to CLFT becomes more pronounced. Depending on the relative transient impedances in the circuit i_{ds} can cause the Phase 1 CLFT on the node of interest to be larger or smaller than what Eqn. 2-26 predicts. For the common case of the signal source impedance being much lower than the hold node impedance i_{ds} will reduce the Phase 1 contribution to CLFT, leading to:

$$CLFT_{Phase1} = -\sqrt{\frac{\pi U C_h}{2\beta}} \left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_h} \right) \operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_h}} \left[V_H - (V_S + V_T) \right] \right).$$

Which, incidentally, is the expression for the Phase 1 contribution (Eqn. 2-5) of the single-lump model from section 2.1, repeated here for convenience.

Once the pass-transistor enters the cutoff region (Phase 2 of turn-off, where $V_{GS} < V_T$), only the overlap capacitance will normally continue to contribute to CLFT for as long as the Gate voltage continues to fall. Thus in Phase 2 the C_{ol} is effectively forming a capacitive potential divider with C_h. The Phase 2 contribution is therefore directly proportional to C_h, C_{ol}, the clock low voltage V_L and the threshold point ($V_{TH} = V_S + V_T$) at

which the pass-transistor enters cutoff (see Eqn. 2-6 in section 2.1.1.2 which is repeated below):

$$CLFT_{Phase2} = -\frac{C_{ol}}{C_h}(V_S + V_T - V_L).$$

The final value for the CLFT error is, of course, the sum of both the Phase 1 and the Phase 2 contributions to CLFT.

These equations relied on the simplifying assumption that the pass-transistor stayed in the linear region for the whole of the Phase 1 of turn-off (i.e. that the transistor went from the linear region straight into cutoff; contributions to CLFT from other regions of operation such as weak inversion were considered insignificant). It was also assumed that the quasi-static approximation was not violated. These are reasonable assumptions under most circumstances, except for the limiting conditions of Eqn. 2-5, namely fast switching and slow switching, which are summarised below, or if the pass-transistor enters saturation during turn-off, the implications of which will be discussed later in chapter 3.

2.9.2 The impact of clock fall-time on CLFT.

During turn-off a MOS pass-transistor will pass through a number of different regions of operation as it proceeds from 'ON' to 'OFF'. Which of the modes of operation are entered depends on the relative speed of the gate turn-off transient (i.e. the ratio of t_f to the carrier channel transit time τ_0; $\tau_0 = L^2(\mu V_{HT})^{-1}$ (see section 2.4.3):

1. for fast turn-off speeds ($t_f < 10\tau_0$) the pass-transistor will remain in strong inversion throughout the Phase 1 of turn-off. In fast turn-off the time spent in this phase is so short (the same order of magnitude as the carrier channel transit time τ_0 or less), that not all of the mobile inversion layer charges will have enough time to leave the channel through conduction. The remaining mobile charges will get 'trapped' in the channel region as

both the Gate to Drain and Gate to Source voltages fall below their threshold points. At this point the switch is effectively turned 'OFF' and the pass-transistor enters the diffusion mode of conduction. In this mode the 'trapped' inversion layer charges will relatively slowly 'diffuse' out of the channel region to the Drain and the Source of the device. This diffusion process may take longer than the Gate turn-off transient to finish. The CLFT error may hence continue to increase even after the clock transient has been completed.

2. for normal and slow turn-off speeds ($t_f > 10\tau_0$) the pass-transistor will stay in the linear region for most of the Phase 1 of turn-off. It will then pass through the weak inversion region before finally turning 'OFF' upon entering the depletion region or cutoff. At this point virtually all minority carriers have been removed from the pass-transistor's channel region and the device enters the Phase 2 of turn-off, in which only its C_{ol} will continue to contribute to CLFT for as long as the Gate voltage continues to fall. The effects of weak inversion on CLFT were found to be significant only at low clock fall-rates (for $U \ll \beta V_{HT}^2/2C_h$) and may thus be neglected at higher fall-rates.

2.9.2.1 Fast turn-off.

In a fast turn-off regime, the rate of error charge generation from Q_{inv} and C_{ol} is much higher than the transport current's capacity for potential equalisation between Drain and Source. The transistor will then operate in a (charge dominated) regime, in which an equal proportion of the error charge should go to both the Drain and Source terminals. CLFT is expected to approach the limit predicted by the single-lump model.

In a fast switching regime a substantial amount of channel charge may however be lost to the substrate through charge pumping, in which case the overall level of CLFT would be lower than anticipated by the single-lump model. It was found (see section 2.4.3.4) that charge pumping will normally be negligible if clock fall-times are greater than ten times

the channel transit time τ_0, where $\tau_0 = L^2(\mu V_{HT})^{-1}$. For fall-times approaching τ_0, charge pumping will normally remain quite small, as long as V_L does not fall below V_B.

During fast turn-off, the pass-transistor may also enter the diffusion mode of conduction. It is entered only if the pass-transistor's Gate voltage falls so fast that some, if not most, of the minority carriers (inversion layer charges) do not have enough time to exit the channel through the transistor's Drain and Source terminals before the Gate voltage falls below the threshold voltage V_{TH} at which point the remaining minority carriers become trapped in the channel region. These trapped charges are then released through the so-called diffusion mode of conduction (see section 2.4.2), in which the remaining channel charges are being distributed equally between Drain and Source. The removal of inversion layer charges through diffusion is slower than through conduction. The error on the hold capacitor may therefore continue to increase, even after the clock transient has finished.

Under fast switching conditions the final value of CLFT will thus approach the limit given by the single-lump model; assuming that charge pumping remains insignificant:

$$CLFT = -\frac{C_{ox}}{2C_h}\left[V_H - (V_S + V_T)\right] - \frac{C_{ol}}{C_h}\left[V_H - V_L\right]$$

Eqn. 2-27

2.9.2.2 Slow turn-off.

In a slow turn-off regime i_{ds} can maintain near equal potentials on both Drain and Source nodes throughout Phase 1 of the turn-off. For low clock fall-rates the Phase 1 contribution is therefore expected to approach zero in the limit, as predicted by the single-lump model.

Earlier in section 2.6 the weak inversion charge contribution to CLFT [14] was examined. It was shown to cause an increase in CLFT to above the single-lump model prediction. This difference between prediction and reality arose from the fact that the channel did not

disappear instantaneously at the point where V_{GS} fell below V_T (as assumed in the single-lump model) but gradually diminished with falling V_{GS}. In fact this reduction in channel charge had already started while V_{GS} was still several 100mV above V_T (when the transistor entered moderate inversion), and continued deep into the weak inversion region (where V_{GS} has fallen well below V_T). The effects of this on the error charge generated by the falling Gate voltage and on the transport current component i_{ds}, and therefore on CLFT, are as follows:

1. In moderate inversion and in weak inversion while $V_{GS} \geq V_T$:

   The level of inversion in the channel is somewhat lower than assumed by the single-lump model. This results in a reduction in the amount of error charge that is released over that region and also in a reduction in i_{ds} (both relative to the single-lump models assumptions).

2. In weak inversion with $V_{GS} < V_T$:

   In this region there are a few minority carriers left in the channel. Their numbers will however dwindle as V_{GS} continues to fall (see Appendix A). This means that a higher than anticipated amount of error charge is being released in that region and that some charge exchange between Drain and Source can be maintained by a decreasing i_{ds} (the single-lump model had assumed that the inversion layer had disappeared completely, hence its assumption that $i_{ds} = 0$ and that only C_{ol} continued to contribute to CLFT).

Whether these weak inversion effects will lead to higher or lower CLFT than predicted by the single-lump model depends on the balance between the error charge produced by the weak inversion contribution to CLFT, and the error charge removed through i_{ds} in the weak inversion region (which in some of the literature is also called the sub-threshold mode of conduction). The overall size of the error charge released by Q_{inv} and C_{ol} is, of course, unaffected by weak inversion effects and by the longer clock fall-times t_f of slow switching, except that the error charge is being released over a longer period of time.

However the amount of charge exchanged between Drain and Source through i_{ds} is time-dependent: the longer t_f the more charge can be exchanged. If the clock fall-rate is sufficiently low, the weak inversion current may therefore overcome the 'extra' charge provided by the weak inversion contribution to CLFT. It may even lead to the actual CLFT error being smaller than the one predicted by the single-lump model.

A recent paper by Aghtar, Haslett and Trofimenkoff [24] supports this view. In this paper they present a new closed form analytical model for CLFT that was based on the single-lump model [6] and takes both the weak inversion contribution to CLFT and i_{ds} into account. It was shown to be capable of accurately estimating CLFT down to very slow switching speeds. In their paper [24] they also showed that the weak inversion effects can lead to both higher or lower CLFT than predicted by the single-lump model. The actual outcome was found to be dependent on a variety of process parameters such as substrate doping levels, N_{Sub}, Gate oxide thickness, t_{ox}, flat-band voltage, V_{FB}, and fast surface state density, N_{FS}. Overall, the weak inversion effect was found to become more significant for large Gate-capacitance to hold capacitance ratios (larger pass-transistor, thinner Gate oxide and/or smaller hold node capacitance C_h) and lower clock fall-rates U. The following, much simplified, version of Aghtar's model [24] reveals the relative influence of each of these parameters. It is valid only for low clock fall-rates (i.e. if $U \ll \beta V_{HT}^2/2C_h$) and small V_{DS} (V_{DS} less than $\approx 2V_t$):

$$CLFT \cong \frac{C_{ol}}{C_h}\left[-\left(V_S + V_T + nV_t - V_L\right) + nV_t \ln\left(\frac{\beta(nV_t)^2}{UC_h}\right)\right]$$

Eqn. 2-28

V_t is the thermal voltage ($k_BT/q \approx 25.8mV$ at room temperature), k_B is Boltzmann's constant, and n is a process dependent sub-threshold slope factor; n is generally between 1.0 and 3.0 and may be calculated using the following approximate relationship:

$$n \cong 1 + \frac{qN_{FS}}{C'_{ox}} + \frac{\gamma}{2\sqrt{2\varphi_F - V_{BS}}}$$

Here N_{FS} is the fast surface state density, which is a strongly process dependent parameter.

2.10 Conclusions drawn from the review of CLFT theory.

Several models for CLFT have been presented, most of these for the basic S&H circuit. Almost all of these models were derived from the current continuity equation, leading to a set of differential equations describing the circuit's (and its CLFT error's) transient behaviour. Analytical solution of these differential equations proved all but impossible for any but the simplest case, namely that of the basic S&H circuit which consisted of an ideal signal source, a MOS pass-transistor and an ideal hold capacitor. A closed-form analytical solution for this circuit was the single-lump model [6] presented in section 2.1. It was found that the differential equations for more complex circuits, such as S&H circuits with non-zero input impedance (see section 2.2), could only be solved numerically or with the help of circuit simulators (such as SPICE and Spectre). These simulators were found capable of producing estimates of CLFT that were at least as accurate as many of the analytical models; the added bonus being that circuit simulators can compute CLFT for essentially any circuit topology and complexity just as easily and accurately as for the basic S&H. The use of circuit simulators for predicting a circuit's CLFT error thus appears to be a convenient and viable alternative to the use of analytical models.

2.10.1 The three main contributing factors to CLFT.

The overview of CLFT theory also showed that a S&H circuit's CLFT error was determined mainly by the following three elements (the definitions given below apply to circuits using NMOS pass-transistors as switching devices):

1. The 'error' charge, Q_{err}, stored on the Gate capacitance, C_G, at the beginning of turn-off. It is this Q_{err} that is the source of the CLFT error; if there was no Q_{err} there would be no CLFT. The release of Q_{err}, which is induced by the pass-transistor's falling clock or Gate voltage, V_G, takes place over the whole of the turn-off period, i.e. over the whole of the

clock fall-time, t_f. It initiates the Drain and Source currents, i_d and i_s, which distribute Q_{err} between the S&H circuit's input and output (or hold) nodes:

$$Q_{err} = \Delta V_G C_G = \left(V_H - \left(V_S + V_T\right)\right)C_{ox} + \left(V_H - V_L\right)2C_{ol} = \int_0^{t_f} \left(i_d + i_s\right)dt$$

Eqn. 2-29

2. The relative size of the impedances and capacitances that are connected to the Drain and Source of the pass-transistor, and in particular the transient behaviour that these 'terminating' impedances present to the pass-transistor during turn-off. During turn-off currents i_d and i_s will flow out of the pass-transistor's Drain and Source terminals and into the respective 'terminating' impedances, z_d and z_s. In many S&H circuits $\Delta V_{GS} \cong \Delta V_{GD}$, which means that i_d and i_s will, to first order approximation, be approximately equal. Any mismatch between z_d and z_s, during turn-off, will then give rise to a voltage differential between the pass-transistor's Drain and Source, $v_{ds} = i_d z_d - i_s z_s$, which in turn may give rise to the third component, i_{ds}, described below.

3. A transport current between Drain to Source, i_{ds}, may get induced in the pass-transistor during turn-off. This current, which can only flow while the device is 'ON', tries to keep the potentials on both Drain and Source equal, i.e. attempts to achieve $v_{ds} = 0V$. In S&H circuits where the 'terminating' impedance on the input node is lower than on the output node i_{ds} will reduce CLFT (in these S&H's v_{ds} and CLFT are just two different expressions for the same thing). The amount of charge, q_{ds}, that i_{ds} can carry between Drain and Source is, of course, dependent on the length of time i_{ds} flows (the time t_{ON}) and the magnitude of i_{ds}: $q_{ds} = \int_0^{t_{ON}} i_{ds}\,dt$; where $i_{ds} = R_{ON} v_{ds}$ is a function of the channel 'ON' resistance, R_{ON}, and of v_{ds}.

A fourth factor, the amount of charge that is lost to the substrate through charge pumping, was not included in this list, as it was generally found to be insignificant (see section 2.4.3).

Clearly, CLFT is dependent on the pass-transistor parameters: C_{ox}, C_{ol} and β; the clock parameters: V_H, V_L and t_f; the terminating impedances on both the circuit's input and output (which include the signal source impedance and the hold capacitance, C_h); and the signal dependent threshold voltage $V_{TH} = V_S + V_T$.

2.10.2 Some recommendations for minimising CLFT.

Analysis of the constituent factors of each of the three main contributing factors to CLFT reveals that CLFT can be reduced by:

- increasing the size of the hold capacitor, C_h.
- making $C_G = C_{ox} + 2C_{ol}$ as small as possible.
- reducing the clock fall-rate, U, i.e. using a clock with a long clock fall-time, t_f.
- lowering the 'ON' resistance, R_{ON}, of the pass-transistor, i.e. increasing its transconductance, β.
- reducing the swing of the Gate voltage, $\Delta V_G = V_H - V_L$.
- reducing the signal source impedance, thus making it absorb more of Q_{err}. A shunt capacitor in parallel with a relatively high impedance signal source can help reduce CLFT significantly (see chapter 2.2).

It may be appreciated that the implementation of these recommendations may affect other aspects of circuit performance such as, for example: acquisition time, bandwidth, droop and aperture jitter, and that trade-offs in some circuit performance measures may be necessary to achieve acceptable CLFT performance.

The relative merits of most of these recommendations are explored in the (brief) assessment of the impact of the Gate length, L, on CLFT that follows.

2.10.3 Use of shortest permissible Gate length to minimise CLFT.

It can be shown that CLFT can be minimised if the shortest possible Gate length is chosen for a S&H circuit's pass-transistor (other circuit requirements permitting). This results in the lowest R_{ON} per unit width possible, and hence the smallest Gate area requirement for the realisation of a desired R_{ON} for the pass-transistor. The upper limit of a S&H circuit's CLFT error when expressed as a function of its R_{ON} is found by combining Eqn. 1-10 (R_{ON}) and Eqn. 2-27 (CLFT under fast switching conditions or in circuits with identical Drain and Source loads. This equation assumes $q_{ds} = 0$.):

$$CLFT = -\frac{L^2}{2\mu R_{ON} C_h} - \frac{C_{ol}}{C_h}(V_H - V_L) = -\frac{L^2}{2\mu R_{ON} C_h} - \frac{(V_H - V_L) C_{GSO} L}{\mu C_{ox}' V_{HT} R_{ON} C_h}$$

Eqn. 2-30

where $R_{ON} = \frac{L}{W \mu C_{ox}' V_{HT}}$, $V_{HT} = V_H - (V_S + V_T)$ and $C_{ol} = WC_{GSO}$.

This expression shows that the Phase 1 contribution to CLFT (i.e. the first term of Eqn. 2-30) is proportional to L^2, the C_{ol} contribution to CLFT (i.e. the second term of Eqn. 2-30) is directly proportional to L and both being inversely proportional to R_{ON}. Therefore reducing L, while keeping V_{HT} constant, requires a proportional reduction in W if R_{ON} is to be kept at the desired value; thus resulting in a larger than proportional reduction of the CLFT error. Reducing the swing of V_G by decreasing V_{HT}, whilst keeping R_{ON} and L fixed, necessitates an inversely proportional increase in W ($R_{ON} \propto V_{HT}W$) and overall a small increase in CLFT, which is proportional to the increase in the ratio of $(V_H - V_L)/V_{HT}$. A reduction in ΔV_G by increasing V_L will result in a proportional reduction in the second term

of the above CLFT expression, but will leave the first term unaffected. Finally, increasing C_h will result in a directly proportional reduction in CLFT.

Assuming a certain target acquisition time, t_a, (which will depend on R_{ON} and C_h, see Eqn. 1-1) should be met by the S&H in question, then clearly, the best strategy for minimising CLFT will be to realise the S&H's pass-transistor using the shortest available or permissible Gate length, L. Increasing V_L appears to be a much less effective strategy since it only affects the, C_{ol} related, second term of Eqn. 2-30. The amount by which V_L can be raised is also limited by the lowest signal voltage that may be applied to the circuit, and by the off-state leakage that can be tolerated in the pass-transistor at this voltage (the off-state leakage current can be estimated using the I_{DS} equations for a MOS transistor in weak inversion that are given in Appendix A). Such increased off-state leakage in the pass-transistor may result in increased input signal feedthrough in the hold mode and may also affect droop. Increasing V_{HT} will also result in a small decrease in CLFT (the first term of Eqn. 2-30 will remain constant but the ratio of $(V_H - V_L)/V_{HT}$ in the second term will decrease as V_H is increased and therefore lead to some reduction in CLFT). However, for slow switching, an increase in V_{HT} will lead to a proportional reduction in CLFT (since an increase in V_{HT} leads to a proportional reduction in the W of the pass-transistor, and therefore a proportional reduction in its C_{ol}, which results in a proportional reduction of CLFT; see Eqn. 2-28).

An increase in C_h will not normally lead to any reduction in CLFT, as it will have to be balanced by a proportional decrease in R_{ON} (to keep the circuit's t_a at or below its acceptable t_a limit). If, however, the S&H circuit's pass-transistor were a minimum feature size device, then increasing C_h until the t_a limit was reached would be a worthwhile strategy as it will result in a proportional reduction of CLFT.

3. Saturation mode contribution to CLFT.

In this section a new, previously unreported, contribution to CLFT, the saturation mode contribution to CLFT, is presented. It will be shown that the basic single-lump model [6] presented in chapter 2.1, may underestimate a S&H circuit's CLFT level, due to its failure to take the saturation mode contribution into account. Under low injection conditions (i.e. with low V_{DS} across the pass-transistor during turn-off) the error due to saturation mode was found to be negligible, but under high injection conditions the error may become significant.

3.1 Definition of saturation mode.

For the purpose of this discussion a MOS transistor shall be assumed in saturation, if its Drain to Source current, I_{DS}, has become practically independent of V_{DS}. Otherwise, the transistor shall be assumed operating in the linear region. This definition of saturation mode, and linear mode, encompasses both the strong inversion and the weak inversion operation of a MOSFET. Fig. 3-1 below illustrates this point. It shows I_{DS} as a function of V_{DS} with V_{GS} as parameter for a 8μm by 8μm NMOS transistor realised on the AMS 0.8μm Mixed Signal process (see Appendix E).

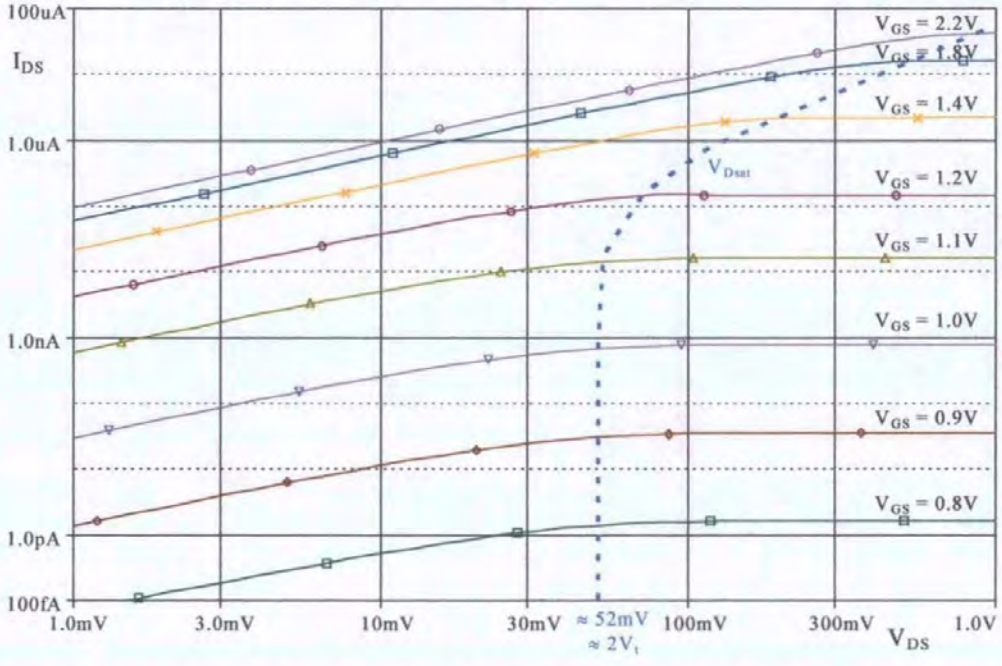


Fig. 3-1: I_{DS} over V_{DS} with V_{GS} as parameter. V_S = 1V, $V_T \cong$ 1.14V and $V_{on} \cong$ 1.19V.

The plot clearly shows that saturation of I_{DS} occurs in both strong inversion and weak inversion. The device was in weak inversion for $V_{GS} \leq V_{on} < 1.19V$.

3.2 Models for I_{DS} in strong inversion and in weak inversion.

In this section we shall concentrate on MOSFET operation in the saturation region under both weak inversion and strong inversion conditions. Operation of the strongly inverted MOS transistor in the linear region has already been discussed in chapter 1.3.1.

3.2.1 I_{DS} in strong inversion.

According to the SPICE Level 1 definition a MOS transistor is considered in saturation if:

$$V_{DS} > V_{Dsat}\,|_{V_{GS}>V_T} \qquad \text{where} \qquad V_{Dsat} = V_{GS} - V_T\,.$$

For V_{DS} smaller than V_{Dsat} the device is considered operating in the linear region (see chapter 1.3.1) and for $V_{GS} < V_T$ it is considered to have turned 'OFF' (see chapter 1.3.3).

In other words, a transistor is in saturation only if V_{GD}, but not V_{GS} has fallen below V_T, i.e. if $V_{GS} > V_T$ and $V_{GD} < V_T$. This means that the inversion layer has all but disappeared near the Drain, and the depletion region extends all the way up to the gate oxide. The Drain end of the transistor operates now in weak inversion, and the channel is said to have 'pinched off'. Fig. 3-2 below depicts this 'pinching off' of the channel at the transistor's Drain end by the encroaching depletion region.

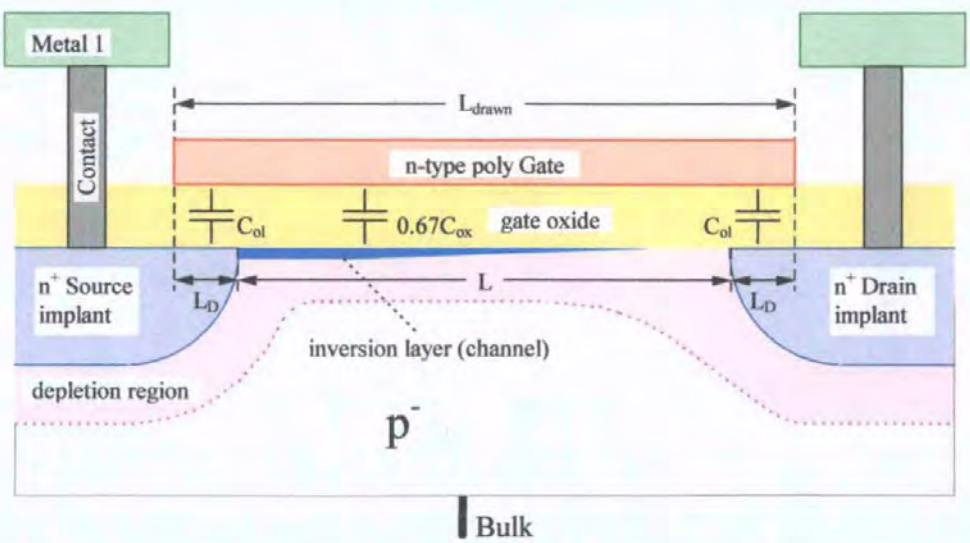


Fig. 3-2: Cross-section of a NMOS transistor in the saturation region.

The effect of 'pinch off' on the channel, and therefore on I_{DS}, is that the Drain is now effectively separated from the channel by a high impedance depletion region. Any increase in the Drain voltage above V_{Dsat} will be almost completely absorbed by the 'pinch off' region, resulting in a virtually constant voltage drop along the rest of the channel, and hence virtually constant I_{DS}. The transport current I_{DS} in the pass-transistor has now become practically independent of V_{DS}, which is reflected in the SPICE Level 1 model [5] for the I_{DS} in saturation:

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Eqn. 3-1

Here λ is the channel-length modulation factor, a process-dependent constant, that is normally much smaller than 1 (for example $\lambda < 0.05V^{-1}$ for a 0.8μm long NMOS transistor realised on the AMS 0.8μm Mixed Signal process). For longer devices λ will be even smaller as it tends to decrease with increasing channel length ($\lambda \propto 1/L$).

For $\lambda V_{DS} \ll 1$ the above expression for I_{DS} may be simplified to:

$$i_{dsat} \equiv \frac{\beta}{2}(V_{gs} - V_T)^2 \Big|_{V_{ds} > V_{gs} - V_T \;\&\; V_{gs} > V_T}$$

Eqn. 3-2

3.2.2 I_{DS} in weak inversion.

According to [1] and [34] the current I_{DS} in the weak inversion region is:

$$I_{DS} \propto \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) e^{\frac{V_{GS} - V_{on}}{nV_t}}$$

Eqn. 3-3

where V_{on} is the modified threshold voltage that applies to a MOSFET in the sub-threshold or weak inversion regime, V_t is the thermal voltage ($V_t = k_B T/q \approx 25.8mV$ at 300K) and n

is the process dependent sub-threshold slope factor (n is commonly in the region of 1 .. 3). V_{on} is given by [34]:

$$V_{on} = V_T + nV_t$$

Eqn. 3-4

From Eqn. 3-3 it is clear that I_{DS} saturates (i.e. becomes independent of V_{DS}) for V_{DS} greater than a few V_t (V_{DS} greater than $\approx 2 .. 3V_t$) [1]. For V_{DS} smaller than this I_{DS} will decrease approximately proportional with V_{DS} [24] (see also Appendix A for a brief overview of MOSFET operation in weak inversion).

A V_{Dsat} for the weak inversion region could be defined as the V_{DS} at the point at which the approximations for I_{DS} in the linear region, I_{dlin}, and in the saturation region, I_{dsat}, intersect (i.e. $V_{Dsat} = V_{DS}$ at the point where $I_{dsat} = I_{dlin}$. The equations for I_{dlin} and I_{dsat} can be found in Appendix A). This definition yields $V_{Dsat} = V_t n/m$ in weak inversion. For many processes $n/m \approx 2$ (m is a process dependent parameter, see Appendix A). Thus a convenient assumption can be made that $V_{Dsat} \cong 2V_t$.

3.2.3 The difference in I_{DS} between linear and saturation mode.

Obviously, saturation mode operation imposes a V_{GS} dependent upper limit on I_{DS} above which it can not rise, no matter how large the actual voltage drop between Drain and Source, V_{DS}. This limiting effect occurs in both weak inversion and strong inversion, the only difference being that in weak inversion saturation occurs at $V_{DS} > V_{Dsat} \cong 2V_t$, whereas in strong inversion it happens for $V_{DS} > V_{Dsat} = V_{GS} - V_T$.

V_{Dsat} has been drawn on Fig. 3-1 as a dotted line that intersects the individual $I_{DS}(V_{GS})$ graphs at the point where $V_{DS} = V_{Dsat}$ for the particular graph. To the left of the dotted line the device clearly operates in the linear region (I_{DS} increases proportional with V_{DS}), and to

the right it clearly operates in the saturation region (I_{DS} is pretty much constant), regardless of whether the device is in strong or weak inversion.

Looking at Fig. 3-1 it becomes clear that ignoring the saturation effect can lead to a serious overestimate of I_{DS} if a simple linear interpolation of I_{DS} from low V_{DS} to higher V_{DS} levels is employed — and this is exactly what most CLFT models do. The single-lump model, for example, employs such an approximation to describe the transport current i_{ds} in the channel throughout Phase 1 of turn-off (see Eqn. 2-3 which is repeated below for convenience):

$$i_{dlin} \cong \beta\left(V_{gs} - V_T\right) V_{ds} \Big|_{V_{ds} < V_{gs} - V_T \;\&\; V_{gs} > V_T}$$

and a similar linear interpolation had been applied to the i_{ds} of a pass-transistor in weak inversion in [24]:

$$i_{dlin} \propto V_{ds}\, e^{\frac{V_{gs} - V_{on}}{nV_t}} \Bigg|_{V_{ds} < V_{Dsat} \;\&\; V_{gs} < V_{on}}$$

Comparing these approximate equations for the transport current in the linear region, i_{dlin}, to the relevant approximations for i_{ds} in the saturation region, i_{dsat}, under identical V_{gs} - V_T bias conditions, reveals the following relationship:

$$\frac{i_{dlin}}{i_{dsat}} \propto \frac{V_{ds}}{V_{Dsat}} \Bigg|_{V_{ds} > V_{Dsat}}$$

Eqn. 3-5

This clearly shows that for a device in saturation, i_{dsat} will always be smaller than i_{dlin} under otherwise identical conditions. Also, it shows that the error is directly proportional to the ratio of V_{ds} to V_{Dsat}, where $V_{Dsat} = V_{gs} - V_T$ in strong inversion, and $V_{Dsat} \cong 2V_t$ in weak inversion.

3.3 The distribution of the channel charge Q_{Inv} in strong inversion.

The 'pinching off' of the channel does not only affect the current flowing in the channel it also affects the distribution of the mobile charges (or inversion layer charge Q_{inv}) in the channel region. This is shown in Fig. 3-2, which gives a much simplified picture of the distribution of channel charge in saturation. It shows that in saturation, all the mobile channel charge is being associated with the pass-transistor's Source terminal and none with the Drain terminal (the Source terminal is always the one of the two channel contacts to which the Gate terminal has the greatest potential difference to and the Drain is the other one). The corresponding Gate to Drain and Gate to Source capacitances (C_{GD} and C_{GS}) of a strongly inverted MOSFET are, according to the SPICE Level 1 model:

$$C_{GS} = \tfrac{2}{3}C_{ox} + C_{ol} \quad \text{and} \quad C_{GD} = C_{ol},$$

when operating in the saturation region ($V_{DS} > V_{Dsat}$ and $V_{GS} > V_T$), and

$$C_{GS} = \tfrac{1}{2}C_{ox} + C_{ol} \quad \text{and} \quad C_{GD} = \tfrac{1}{2}C_{ox} + C_{ol},$$

when operating in the linear region ($V_{DS} < V_{Dsat}$ and $V_{GS} > V_T$).

This clearly shows that for a MOS transistor operating in the saturation region the proportion of the channel charge that is associated with the Source rises by a third whereas the amount of channel charge associated with the Drain drops to zero.

Now for most S&H circuits the side of the pass-transistor connected to the hold capacitor will actually become the transistor's Source during turn-off. This is due to the CLFT error reducing the potential on the hold node relative to the input voltage which was assumed constant. The single-lump model however assumed Source to be on the input side (see chapter 2.1). The consequence is, that the amount of channel charge associated with the hold node is about a third bigger, than assumed by the single-lump model, when a MOS pass-transistor operates in saturation!

3.4 The impact of these saturation mode effects on CLFT.

The transient response of a basic T&H circuit, like the one in Fig. 2-1, was simulated to illustrate the impact of these saturation effects on CLFT. Process parameters from the AMS 0.8μm Mixed Signal process (see Appendix E) were employed in the simulations. The circuit parameters were the same as for the I_{DS} plot of Fig. 3-1:

NMOS pass-transistor with W = 8.0μm, L = 8.0μm, t_{ox} = 16nm, L_D = 0.0μm, C_{ol} = 0.0fF,

V_{in} = 1.0V, V_T = 1.145V, C_h = 0.5pF, V_H = 5V, V_L = 0V and t_f = 1ns.

Three different transient simulations were carried out:

1. A transient run using the single-lump model (which was described in chapter 2.1).

2. A modified SPICE Level 1 simulation in which saturation mode operation was disabled (The simulation simply continued to assume linear region operation for $V_{DS} > V_{Dsat}$). This simulation is akin to the single-lump model, but there are a few important differences:

   a) the complete SPICE Level 1 equation for i_{ds} in the linear region (Eqn. 2-2) is being used, and not the simplified version employed by the single-lump model (Eqn. 2-3).

   b) transistor Source is correctly assigned to the hold node, and not the input side of the circuit (the single-lump model assumed transistor Source on the S&H input side).

3. A simplified SPICE Level 1 simulation of the circuit, which considers both linear and saturation mode operation of the pass-transistor. Again, the transistor Source is assigned to the output (hold capacitor side) of the circuit. The device was assumed to be in saturation for $V_{DS} > V_{GS} - V_T(V_{out})$, where $V_T(V_{out})$ means that V_T was a function of the output voltage, V_{out}.

The transient plots from these simulations are reproduced below. The first plot (Fig. 3-3) shows the transient response of the T&H circuit's CLFT error and the second plot (Fig. 3-4) shows the corresponding current flow to the hold capacitor, C_h.

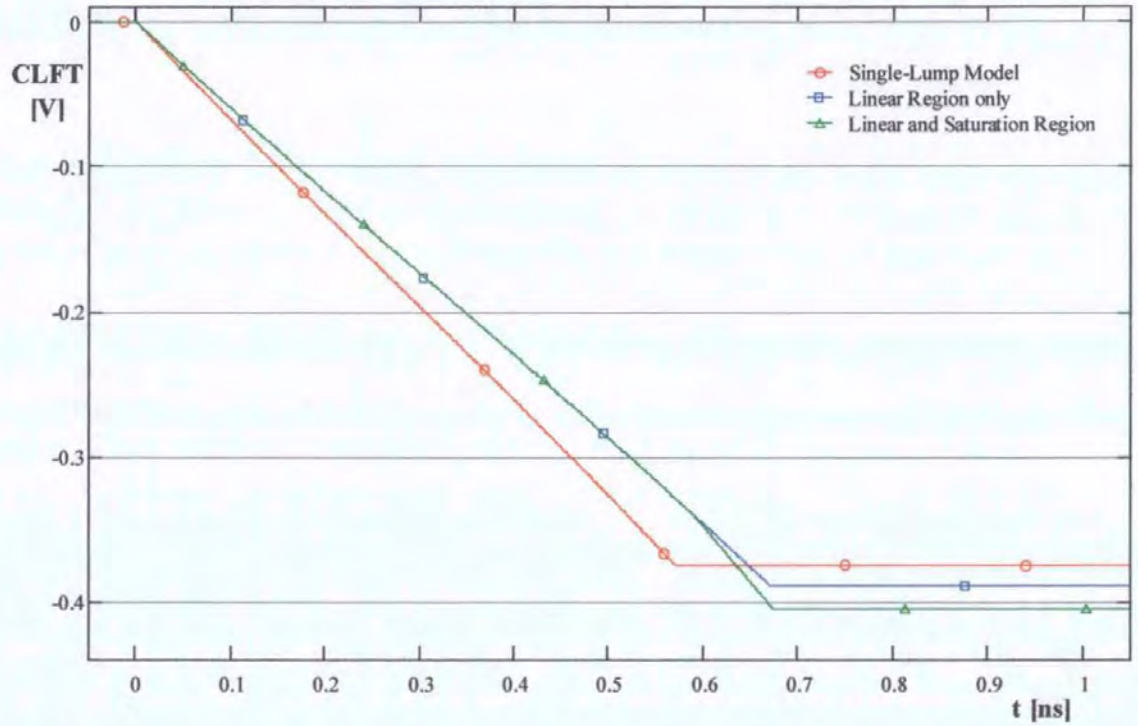


Fig. 3-3: Simulated transient response of the CLFT error under high injection conditions.

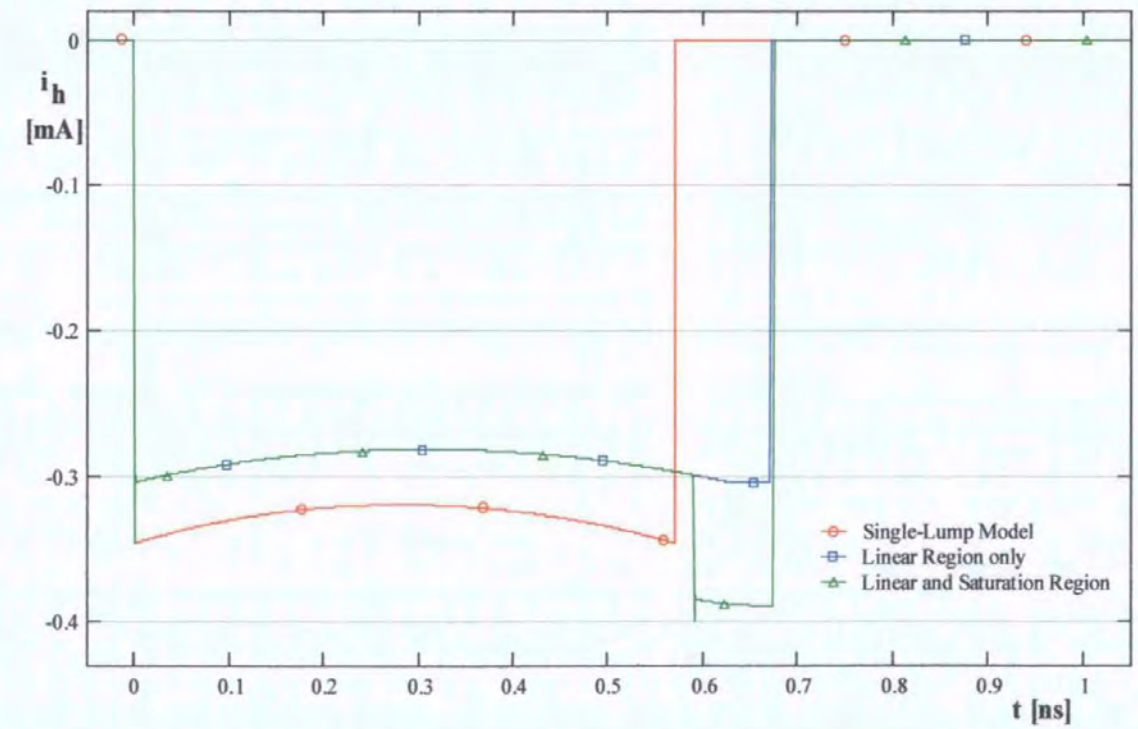


Fig. 3-4: Transient current flow to C_h during turn-off (for the CLFT plots of Fig. 3-3).

On these plots the turn-off starts at t = 0s, after which the pass-transistor's Gate voltage falls from V_H towards V_L, at a constant rate of 5V/ns. At t = 1ns the Gate voltage, V_G, reaches its low voltage, V_L, and turn-off is completed.

The plots show that the single-lump model will enter cut-off about 0.57ns into turn-off. It is at this point that V_G falls below $V_{THin} = V_{in} + V_T(V_{in}) \approx 2.15V$ on the input side of the pass-transistor, and that the single-lump model's i_h becomes zero. Its CLFT error will also have reached its final value, since $C_{ol} = 0$ had been assumed.

For the SPICE based simulations however, the threshold voltage was derived from the output voltage, $V_{THout} = V_{out} + V_T(V_{out}) \cong 1.65V$, where $V_{out} = V_{in} + CLFT$ (the CLFT caused by a NMOS pass-transistor is negative, thus $V_{out} < V_{in}$). For these simulations the pass-transistor remained therefore in strong inversion for approximately another 0.1ns. Most of this 'additional' time was spent in the saturation region. For a S&H, where $|V_{ds}| = |CLFT|$, the pass-transistor will thus be in saturation if the magnitude of the CLFT error is greater than V_{Dsat} (i.e. $|CLFT| > V_{Dsat}$). For Fig. 3-3 and Fig. 3-4 the pass-transistor entered saturation at $V_G = V_{THsat} \cong 2.06V$, where $V_{THsat} = V_{THout} + V_{Dsat}$. As the device enters saturation the current i_h increases by almost a third (see Fig. 3-4), and the CLFT's rate of change accelerates noticeably, i.e. CLFT starts to increase faster when saturation is entered (the blue and the green plots of CLFT on Fig. 3-3 start diverging after the pass-transistor enters saturation).

The net outcome was, that the single-lump model estimated -374.2mV of CLFT, the linear mode only simulation estimated -388.4mV and the SPICE Level 1 simulation (both linear and saturation mode considered) estimated -405.3mV of CLFT error (thus, the linear mode only simulation result was 3.8% greater than the single-lump model's and about 8.3% larger if saturation mode was considered).

3.5 Summary and conclusions for CLFT in saturation mode.

It was found that CLFT was larger than anticipated by the single-lump model, and its derivatives, if a S&H circuit's pass-transistor entered saturation during turn-off.

A NMOS pass-transistor will enter saturation only if $V_{gs} - V_T < -V_{ds}$ for $V_{gs} - V_{on} > 0V$ or if $2V_t < -V_{ds}$ when $V_{gs} - V_{on} < 0V$; i.e. if, while in strong inversion, the Gate overdrive voltage, $V_{gs} - V_T$, falls below the CLFT error voltage or if, in weak inversion, the CLFT error was (or became) greater than approximately $2V_t$. This shows that CLFT must be fairly large before saturation will be entered. In fact, CLFT must be greater than $\approx 2V_t$ for the switching device to go into saturation. In most S&H circuits, CLFT will normally be significantly less than $2V_t$. However, there are some circuits, such as the circuits that are discussed later in chapter 6.1, where CLFT may exceed these limits for a considerable portion of the turn-off transient. Tentative evidence for saturation mode effects was found when such circuits were realised on test silicon (see chapter 7.3).

With the S&H circuit's pass-transistor in saturation the single-lump model, and its derivatives, were found to underestimate CLFT, because they:

1. overestimated the transport current, i_{ds}, flowing in the pass-transistor in saturation.
2. underestimated the amount of channel charge associated with the hold node.
3. assumed that the pass-transistor was in cut-off for $V_G < V_{in} + V_T$ when, in fact, it was for $V_G < V_{out} + V_T$, where $V_{out} = V_{in} + CLFT$. These models therefore underestimated the proportion of the turn-off transient that the pass-transistor would have to be considered 'ON'; i.e. they underestimated the time the device spent in the (strong and weak) inversion regions.

Device simulators such as SPICE and Spectre can account for all of these saturation mode effects. These simulators will automatically switch models when the pass-transistor enters

a new region of operation, and will also assign Source to the correct side of the switching device. Unsurprisingly, results from circuit simulators were found to be more accurate than results from predictions using the single-lump model, when compared to measurements on actual silicon (see chapter 7 on the evaluation of test chip results).

4. Signal dependency of CLFT.

The review of CLFT theory showed CLFT to be signal dependent. In this section the signal dependency of CLFT is analysed. The analysis is based on the single-lump model [6], presented in chapter 2.1, which was shown to give a fair representation of the basic S&H circuit's CLFT error.

Based on this analysis of the signal dependency of CLFT, recommendations are made on how the signal dependency of CLFT can be reduced, and how the CLFT induced distortion may be minimised.

4.1 The INL of S&H circuits.

For the passive type S&H circuits, that are discussed in this thesis, the static performance measures (DC offset, gain error and INL) are all determined by CLFT. In fact, CLFT is the only source of error to affect these. The INL of passive S&H circuits can thus be expressed as a function of CLFT (see chapter 1, for a definition of INL):

$$\mathrm{INL} = \max\left(\left| \frac{\mathrm{CLFT}(V_{in}) - \mathrm{CLFT}(V_{in,min}) - \dfrac{\mathrm{CLFT}(V_{in,max}) - \mathrm{CLFT}(V_{in,min})}{V_{in,max} - V_{in,min}} (V_{in} - V_{in,min})}{V_{in,max} - V_{in,min} + \mathrm{CLFT}(V_{in,max}) - \mathrm{CLFT}(V_{in,min})} \right| \right)$$

where $\mathrm{CLFT}(V_{in})$ is the circuit's CLFT error for a particular DC input voltage, V_{in}, and $V_{in,min} \leq V_{in} \leq V_{in,max}$, i.e. V_{in} is varied between the minimum and maximum DC input voltages applied. Since $\mathrm{CLFT}(V_{in,max})$ - $\mathrm{CLFT}(V_{in,min})$ is normally much less than $V_{in,max}$ - $V_{in,min}$ the following approximate equation may be used instead:

$$\mathrm{INL} \cong \max\left(\left| \frac{\mathrm{CLFT}(V_{in}) - \mathrm{CLFT}(V_{in,min}) - \dfrac{\mathrm{CLFT}(V_{in,max}) - \mathrm{CLFT}(V_{in,min})}{V_{in,max} - V_{in,min}} (V_{in} - V_{in,min})}{V_{in,max} - V_{in,min}} \right| \right)$$

Eqn. 4-1

INL itself is of limited use since it conveys no information about the nature of the non-linearity; it only gives a measure for the magnitude of the distortion. Plots of INL as a function of V_{in} are much more useful. We shall use these to look at the signal dependent non-linearity of CLFT. From Eqn. 4-1:

$$\mathrm{INL}(V_{in}) \cong \frac{\mathrm{CLFT}(V_{in}) - \mathrm{CLFT}(V_{in,min}) - \dfrac{\mathrm{CLFT}(V_{in,max}) - \mathrm{CLFT}(V_{in,min})}{V_{in,max} - V_{in,min}} (V_{in} - V_{in,min})}{V_{in,max} - V_{in,min}}$$

Eqn. 4-2

4.2 The source of the CLFT error's signal dependency.

Inspection of the main contributing factors to CLFT (see chapter 2.10.1) revealed that it was the pass-transistor's threshold voltage, V_{TH}, which gave rise to this signal dependency.

$$V_{TH} = V_{T0} + V_S + \gamma\left(\sqrt{2\varphi_F + V_S - V_B} - \sqrt{2\varphi_F}\right)$$

Analysis of V_{TH} shows that it is composed of a constant term, V_{T0}, a linear term, V_S, (which is directly proportional to the circuit's output voltage) and a, non-linear, square root term (see also Source-Body effect, chapter 1.3.2). Of these the constant and the linear terms have no impact on signal integrity, as they only affect the sampled signal's offset and gain error (see chapter 1.1). The square root term, however, will give rise to harmonic distortion.

It may be appreciated that if V_{SB} was held constant, and therefore independent of V_S, then the square root term of V_{TH} would be constant, too. It (the square root term of V_{TH}) would then only give rise to an additional offset component on the sampled signal, and the non-linear term would have been removed from V_{TH}. This can be achieved by, for example, shorting the Bulk and Source terminals together ($V_{SB} = 0V$ and thus $V_T = V_{T0}$ which, for a given device, is constant). Alternatively, a $V_{SB} \neq 0V$ may be chosen. However, both solutions require that the switch be manufactured in its own, isolated, well. For $V_{SB} \neq 0V$ this will also require the provision of a 'floating' voltage source that maintains V_B at a constant level relative to V_S.

In the next sections we will try to establish if this, or indeed any other measure, can eliminate the signal dependent components from CLFT. For this, the sensitivity of CLFT to changes in the input voltage, V_{in}, is examined, and the Integral Non-linearity (INL) of S&H circuits studied. INL, as shall be seen, is a measure for the magnitude of the distortion arising from CLFT.

4.3 The sensitivity of CLFT to changes in the input voltage.

Holding V_{SB} constant certainly seems to eliminate the non-linear component from V_{TH}. In this section the sensitivity of CLFT to changes in the input voltage V_{in} will be studied. This analysis will be based on the single-lump model for the basic S&H with a NMOS pass-transistor and zero signal source impedance assumed (see chapter 2.1). The single-lump model for the basic S&H was:

$$CLFT = -\sqrt{\frac{\pi UC_h}{2\beta}}\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\mathrm{erf}\left(\sqrt{\frac{\beta}{2UC_h}}\left[V_H-(V_{in}+V_T)\right]\right)-\frac{C_{ol}}{C_h}\left[(V_{in}+V_T)-V_L\right]$$

Eqn. 4-3

Simple inspection of this expression reveals that CLFT is negative, and that it can never become zero (V_H must be greater than $V_{in} + V_T$ and V_L must be less than $V_{in} + V_T$ or else the circuit will not work). CLFT will therefore always introduce a negative offset voltage to the sampled signal.

We also see that the first term on the right side of Eqn. 4-3 increases with V_{in} (i.e. it has a positive V_{in} coefficient), whereas the second term decreases with V_{in} (negative V_{in} coefficient). This implies that there could be a point at which the two V_{in} dependent terms cancel and CLFT will become independent of V_{in}. At this point the differential of CLFT with respect to V_{in} will be zero:

$$0=\frac{dCLFT}{dV_{in}}=\frac{1}{C_h}\left(1+\frac{\gamma}{2\sqrt{2\varphi_F+(V_{in}-V_B)}}\right)\left[\left(C_{ol}+\frac{C_{ox}}{2}\right)e^{-\frac{\beta\left[V_H-(V_{in}+V_T)\right]^2}{2UC_h}}-C_{ol}\right]$$

Eqn. 4-4

This differential equation shows that there must be such a point, but it also shows that this point is a function of V_{in} itself. Holding V_{SB} (here $V_{SB} = V_{in} - V_B$) constant, as suggested in the previous section, will eliminate only part of the signal dependency of $dCLFT/dV_{in}$; namely non-linearly signal dependent square root term of Eqn. 4-4, which arose from the signal dependency of V_T. However, this will not remove the non-linearly signal dependent exponential, which derives from the error function in Eqn. 4-3:

$$\frac{dCLFT}{dV_{in}} = \frac{1}{C_h}\left[\left(C_{ol} + \frac{C_{ox}}{2}\right)e^{-\frac{\beta[V_H-(V_{in}+V_T)]^2}{2UC_h}} - C_{ol}\right]$$

Eqn. 4-5

This equation was arrived at by differentiating Eqn. 4-3 with respect to V_{in} while assuming that V_T was constant and independent of V_{in}, i.e. V_{SB} was assumed constant.

4.3.1 Under which conditions does CLFT become independent of V_{in}?

For CLFT to become signal-independent the right side of Eqn. 4-4 must be zero. Clearly, this can only be achieved if the two terms in the large square bracket cancel, i.e. if:

$$C_{ol} = \left(C_{ol} + \frac{C_{ox}}{2}\right)e^{-\frac{\beta V_{HT}^2}{2UC_h}}$$

Eqn. 4-6

where $V_{HT} = V_H - (V_{in} + V_T)$. The same condition also applies to Eqn. 4-5.

Obviously, there are two ways in which this can be achieved:

1) If $C_{ox} = 0$ and $e^{-\frac{\beta V_{HT}^2}{2UC_h}} = 1$

2) If $\ln\left(1 + \frac{C_{ox}}{2C_{ol}}\right) = \frac{\beta V_{HT}^2}{2UC_h}$

Clearly the first solution can only be achieved if the exponential term evaluates to 1. For this to occur the exponent must be 0. Fortunately, an exponential term of the form e^{-x}, such as the one given, will rapidly saturate for both $x \gg 1$ and $x \ll 1$: $e^{-x} \cong 0$ for $x \gg 1$ and $e^{-x} \cong 1$ for $x \ll 1$; where $x = \beta V^2_{HT}/(2UC_h)$. Resolving these conditions for U, it is found that the exponential evaluates to $\cong 1$ for $U \gg \beta V^2_{HT}/(2C_h)$ and $\cong 0$ for $U \ll \beta V^2_{HT}/(2C_h)$, which, incidentally, are the definitions for fast switching and slow switching used in section 2. The first solution therefore requires that the pass-transistor's Source be on the input side of the S&H circuit and that the pass-transistor remains in saturation throughout turn-off (C_{ox} on the output side of the circuit will then be $\cong 0$ see chapter 3.3) and that $U \gg 0.5\beta V^2_{HT}/C_h$. Application of these conditions to the CLFT equation for fast turn-off (Eqn. 2-27 of chapter 2.9.2.1) shows that, under these conditions, CLFT will become truly independent of V_{in}.

The second implies that signal independent CLFT can be achieved in any number of ways by adjusting any of the equation parameters, β, U, C_{ol}, C_{ox}, C_h, V_H, V_{in} and V_T, such that both sides of the equation become equal. Of all these parameters, U is the only one that can be adjusted without affecting most other circuit performance parameters, such as SNR and acquisition time (see section 1). It therefore is ideally suited for the type of optimisation required.

Solving Eqn. 4-6 for U allows us to calculate the clock fall-rate U_{d0} for which CLFT will become independent of V_{in}:

$$U_{d0} = \left. \frac{\beta V^2_{HT}}{2C_h \ln\left(\frac{C_{ox}}{2C_{ol}} + 1\right)} \right|_{\frac{dCLFT}{dV_{in}} = 0}$$

Eqn. 4-7

Since $C_{ox} = WLC'_{ox}$ and $C_{ol} = WC_{GSO}$ this may also be expressed as:

$$U_{d0} = \left.\frac{W\mu C'_{ox} V_{HT}^2}{2C_h L \ln\left(\frac{C'_{ox} L}{2C_{GSO}} + 1\right)}\right|_{\frac{dCLFT}{dV_S} = 0}$$

Eqn. 4-8

where $C'_{ox} = \varepsilon_{ox}/t_{ox}$. For $C_{ox} \leq C_{ol}$ this equation may be approximated to:

$$U_{d0} \approx \left.\frac{W\mu V_{HT}^2 C_{GSO}}{L^2 C_h}\right|_{\frac{dCLFT}{dV_S} = 0}$$

Eqn. 4-9

This approximation gives a value for U_{d0} that is $\approx 25\%C_{ox}/C_{ol}$ too big, i.e. about 5% too big for $C_{ol} = 5C_{ox}$ and about 25% too big for $C_{ol} = C_{ox}$.

It appears that signal independent CLFT can be achieved for specific combinations of V_{HT} and U_{d0} only: we seem to have found a 'local minima' in the sensitivity of CLFT to V_{in}. A potential solution for signal-independent CLFT would be to make U a function of V_{HT}. Clearly, U would have to track V^2_{HT} exactly (see Eqn. 4-7), which may be possible, but does not appear to be all that easy — the quadratic term suggests that this scheme would be very sensitive to mismatches between V_{HT} and U.

Essentially, the question is, what happens if V_{HT} is constant and independent of V_{in}? Differentiating CLFT with respect to V_{in} for V_{HT} constant yields:

$$\frac{dCLFT}{dV_{in}} = \frac{-C_{ol}}{C_h}\left(1 + \frac{\gamma}{2\sqrt{2\varphi_F + (V_{in} - V_B)}}\right)$$

Eqn. 4-10

Clearly, making V_{HT} signal independent results in the error function term of Eqn. 4-3 becoming independent of V_{in}, which means that it becomes zero on differentiation and

therefore 'falls out' of the differential equation. This in itself is not sufficient to make CLFT independent of V_{in}. Should, however, both V_{HT} and V_{BS} be constant and independent of V_{in} then CLFT will at least be directly proportional to V_{in}:

$$\frac{dCLFT}{dV_{in}} = \frac{-C_{ol}}{C_h}$$

Eqn. 4-11

The presence of $-C_{ol}$ in these two differential equation suggests that the $V_{TL} = V_{TH} - V_L = V_T + V_{in} - V_L$ of Eqn. 4-3 is the cause of this residual signal dependency. Differentiating CLFT with respect to V_{in} for constant V_{TL} gives:

$$\frac{dCLFT}{dV_{in}} = \left(1 + \frac{\gamma}{2\sqrt{2\varphi_F + (V_{in} - V_B)}}\right)\frac{1}{C_h}\left(C_{ol} + \frac{C_{ox}}{2}\right)e^{-\frac{\beta[V_H - (V_{in} + V_T)]^2}{2UC_h}}$$

Eqn. 4-12

Obviously, CLFT will become independent of V_{in}, i.e. $dCLFT/dV_{in} = 0$, if the exponential term of this equation becomes zero, which, as shown at the beginning of this section, will be the case for $U \ll \beta V^2_{HT}/(2C_h)$. Applying V_{TL} constant to the equation for CLFT under slow switching conditions (Eqn. 2-28) shows that CLFT becomes indeed independent of V_{in} for V_{TL} constant and $U \ll \beta V^2_{HT}/(2C_h)$.

The exponential term of Eqn. 4-12 will also evaluate to zero if V_{HT} is constant and independent of V_{in}. CLFT will also become independent of V_{in} both V_{HT} and V_{TL} must therefore be independent of V_{in}. In this case $dCLFT/dV_{in} = 0$, and CLFT will be truly independent of V_{in}, irrespective of the value of U, or any other circuit parameter. An example for a S&H circuit, in which V_H, V_L and V_B were all constant and independent of V_{in}, can be found in [35].

4.3.2 Under which conditions will CLFT be linearly dependent on V_{in}?

A CLFT error that is linearly dependent on V_{in} will not introduce any distortion to the sampled signal; it will only give rise to offset and gain errors.

For CLFT to be linearly dependent on V_{in}, both the 2nd and the 3rd differential of CLFT with respect to V_{in} must be zero. Inspection of the differential equations from the previous section shows that this can only be achieved if V_{SB} is constant and if the exponential term is independent of V_{in}, too. One such case had already been found, namely where both V_{HT} and V_{SB} were constant, and independent of V_{in} (see Eqn. 4-11). This had been derived from $dCLFT/dV_{in}$ with V_{SB} constant, i.e. from Eqn. 4-5.

Other cases may be found, if one considers that the exponential will also become independent of V_{in} for $U \gg \beta V^2_{HT}/(2C_h)$, where it is $\cong 1$ and for $U \ll \beta V^2_{HT}/(2C_h)$, where it evaluates to $\cong 0$. Applying these limiting conditions to Eqn. 4-5 we find that CLFT will be linearly dependent on V_{in} for:

- $U \propto V^2_{HT}/(2C_h)$ and V_{SB} = constant:

$$\frac{dCLFT}{dV_{in}} = \frac{1}{C_h}\left[\left(C_{ol} + \frac{C_{ox}}{2}\right)e^{-\frac{\beta}{2C_h}\frac{V_{HT}^2}{U}} - C_{ol}\right]$$

Eqn. 4-13

- $U \gg \beta V^2_{HT}/(2C_h)$ and V_{SB} = constant:

$$\frac{dCLFT}{dV_{in}} = \frac{C_{ox}}{2C_h}$$

Eqn. 4-14

- $U \ll \beta V^2_{HT}/(2C_h)$ and V_{SB} = constant:

$$\frac{dCLFT}{dV_{in}} = \frac{-C_{ol}}{C_h}$$

Eqn. 4-15

This equation is the same as Eqn. 4-11 for the S&H with constant V_{HT} and constant V_{SB}. The signal dependent component of CLFT for the S&H with both V_{HT} and V_{SB} constant is therefore identical to that of the basic S&H under slow switching conditions (for the S&H with both V_{HT} and V_{SB} constant it applies at any U).

Another case is found for V_{TL} and V_{SB} constant:

$$\frac{dCLFT}{dV_{in}} = \frac{1}{C_h}\left(C_{ol} + \frac{C_{ox}}{2}\right) e^{-\frac{\beta\left[V_H - (V_{in} + V_T)\right]^2}{2UC_h}}$$

Eqn. 4-16

For $U \gg \beta V^2_{HT}/(2C_h)$ and both V_{TL} and V_{SB} constant:

$$\frac{dCLFT}{dV_{in}} = \frac{1}{C_h}\left(\frac{C_{ox}}{2} + C_{ol}\right)$$

Eqn. 4-17

Of these cases the latter will clearly have the greatest signal dependency, as it is proportional to $C_{ol} + C_{ox}/2$. Slow switching conditions or V_{HT} constant will normally yield the smallest signal dependency, since those are proportional to C_{ol}. The signal dependency of Eqn. 4-14 will generally be somewhat larger, since its proportionality factor depends on $C_{ox}/2$ which is normally significantly larger than C_{ol}.

4.3.3 The non-linear signal dependency of CLFT.

In the previous sections, it was found that non-linearity in the CLFT's signal dependency stemmed from the following two factors:

- the exponential term $e^{-\frac{\beta\left[V_H - (V_{in} + V_T)\right]^2}{2UC_h}}$.
- the square root term $\frac{\gamma}{2\sqrt{2\varphi_F + (V_{in} - V_B)}}$.

Distortion of the sampled signal will be greatest where these non-linear terms are at their most sensitive to variations in V_{in} (and smallest where they are at their least sensitive). Interestingly, the exponential term's sensitivity is biggest for large V_{in} (i.e. where V_{HT} is smallest), whereas the square root term's is biggest for $V_{SB} \cong 0V$. Making V_{HT} large by, for example, biasing V_{in} towards lower voltages will therefore reduce distortion arising from the exponential term and biasing $V_{SB} = V_{in} - V_B$ towards higher values will reduce distortion arising from the square root term.

For the AMS 0.8μm process (see Appendix E) for example, the $0.5\gamma(2\varphi_F + V_{SB})^{-0.5}$ term evaluates to 0.407 at $V_{SB} = 0V$, 0.271 at $V_{SB} = 1V$, 0.217 at $V_{SB} = 2V$ and 0.187 at $V_{SB} = 3.0V$. For signals with identical amplitudes, but different V_{SB} bias points, the absolute variation in this square root term works out to 0.19 for $V_{SB} = 0V$ .. 2.0V and 0.084 for $V_{SB} = 1.0V$ .. 3.0V. Clearly, the magnitude of the variation, and therefore distortion, arising from the square root term is reduced for larger V_{SB}.

4.3.3.1 Distortion for V_{SB} constant and independent of V_{in}.

For V_{SB} constant, the square root term becomes independent of V_{in}, and thus disappears from the $dCLFT/dV_{in}$ (for $dCLFT/dV_{in}$ with constant V_{SB} applied see Eqn. 4-5). Distortion is then determined solely by the exponential term. It will be smallest for large V_{HT}, large β and small U. For very small U or very large U the distortion will become zero (i.e. CLFT linearly dependent on V_{in}), as had been shown in the previous section.

4.3.3.2 Distortion for $V_{SB} = V_{in}$.

$V_{SB} = V_{in}$ is probably the most common case encountered in MOS S&H circuit design. For this case, both the exponential and the square root terms will be present in the $dCLFT/dV_{in}$ equation:

$$\frac{dCLFT}{dV_{in}} = \frac{1}{C_h}\left(1+\frac{\gamma}{2\sqrt{2\varphi_F+(V_{in}-V_B)}}\right)\left[\left(C_{ol}+\frac{C_{ox}}{2}\right)e^{-\frac{\beta[V_H-(V_{in}+V_T)]^2}{2UC_h}}-C_{ol}\right]$$

Eqn. 4-18

CLFT will now be non-linearly dependent on V_{in}; except when it becomes independent or linearly dependent on V_{in} (discussed in sections 4.3.1 and 4.3.2 respectively). Earlier it was shown that the exponential term became independent of V_{in}, for any of the following conditions: V_{HT} constant, $U \propto V^2_{HT}$, $U \gg U_x$ and $U \ll U_x$; where $U_x = \beta V^2_{HT}/(2C_h)$. Upon applying these to $dCLFT/dV_{in}$ we find:

- for $U \gg \beta V^2_{HT}/(2C_h)$:

$$\frac{dCLFT}{dV_{in}} = \frac{C_{ox}}{2C_h}\left(1+\frac{\gamma}{2\sqrt{2\varphi_F+(V_{in}-V_B)}}\right)$$

Eqn. 4-19

- for $U \ll \beta V^2_{HT}/(2C_h)$; this differential equation also applies if V_{HT} is constant:

$$\frac{dCLFT}{dV_{in}} = \frac{-C_{ol}}{C_h}\left(1+\frac{\gamma}{2\sqrt{2\varphi_F+(V_{in}-V_B)}}\right)$$

Eqn. 4-20

These two equations present the absolute change in CLFT for a change in V_{in} under fast switching, $U \gg \beta V^2_{HT}/(2C_h)$, and slow switching, $U \ll \beta V^2_{HT}/(2C_h)$, conditions. Both equations are identical, except that Eqn. 4-19 is multiplied by $C_{ox}/2$, whereas Eqn. 4-20 is multiplied by $-C_{ol}$. Since C_{ol} is normally much less than $C_{ox}/2$ the signal dependency, and

distortion, for slow switching will therefore be much lower than for fast switching, something clearly visible in the plots below:

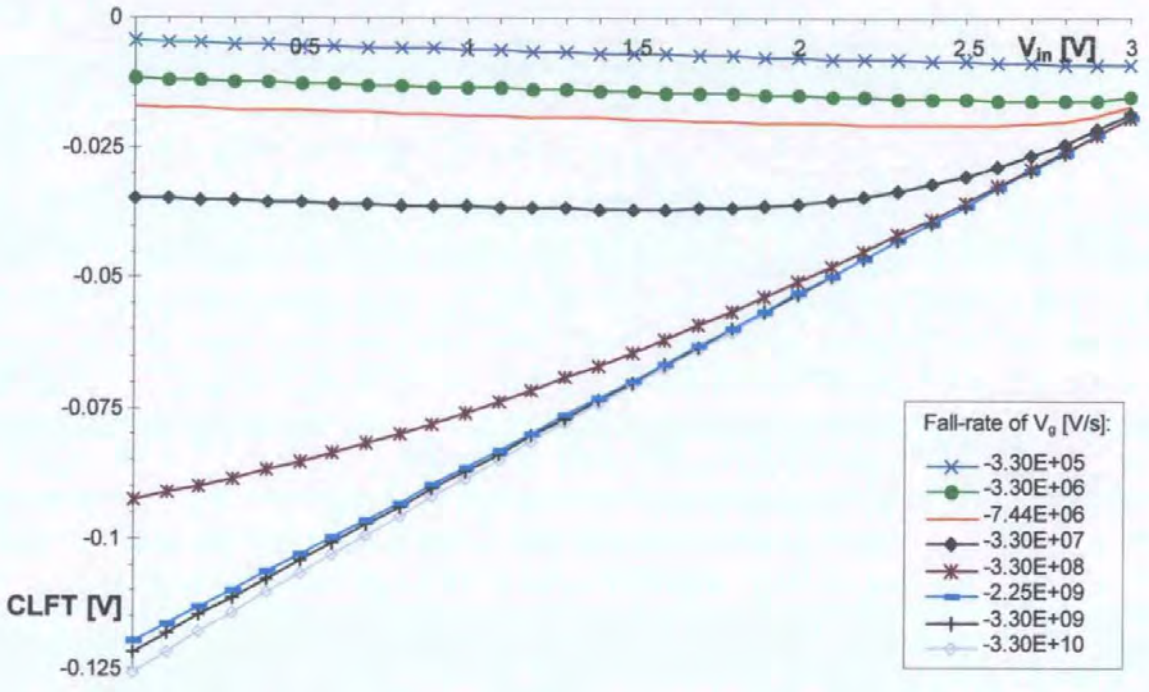


Fig. 4-1: CLFT plots for the basic S&H circuit with $V_H = 5V$ and $V_L = V_B = 0V$.

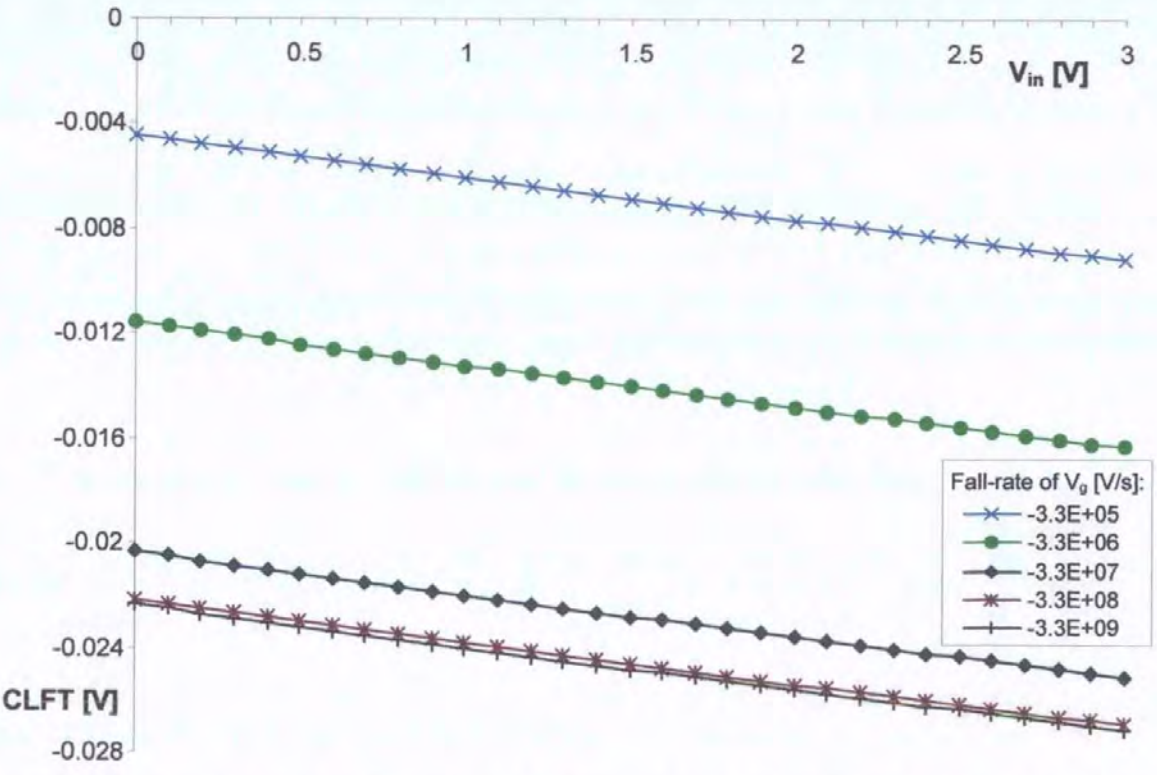


Fig. 4-2: CLFT plots for a V_{HT} controlled S&H circuit with $V_{HT} \cong 0.709V$ and $V_L = V_B = 0V$.

Both CLFT plots were derived from calculations using the single-lump model (Eqn. 4-3). The plot Fig. 4-1 was for a basic S&H circuit (such as the one shown in Fig. 2-1) with a standard digital clock (V_H = 5V, V_L = 0V) applied to the pass-transistor's Gate. Fig. 4-2 was for a S&H circuit in which the $V_{HT} = V_H - (V_{in} + V_T)$ of Eqn. 4-3 was assumed constant, and independent of the input voltage applied. The clock low voltage (the pass-transistors Gate voltage in hold mode) was $V_L = V_B = 0V$.

For both circuits, CLFT was evaluated for a number of different fall-rates, U, of the pass-transistor's Gate voltage, V_g. Parameters for the calculations were:

NMOS pass-transistor with W = 8.0µm, L = 8.0µm, t_{ox} = 16nm, C_{ox} = 138fF, C_{ol} = 3.06fF,

$V_{T0} = 0.844V$, $\beta = 99.5\mu A/V^2$, $\gamma = 0.6749V^{-0.5}$, $\varphi_F = 0.3956V$, $V_L = V_B = 0V$, $C_h = 2.4pF$,

$V_{in} = 0.0V$ .. 3.0V, $V_{HT} = 0.709V$ and U = 330kV/s .. 33GV/s.

The transistor parameters for the calculations were taken from the AMS 0.8µm Mixed Signal process (see Appendix E).

Clearly, just making V_{HT} independent of V_{in} (without relating V_{TL} to V_{in}) can significantly reduce both the CLFT's magnitude and its sensitivity to V_{in}. Another advantage of this strategy is, that the sensitivity of CLFT to V_{in} is independent of U (U only affects the offset component of CLFT, but not its gradient, see Fig. 4-2). This benefit derives from the fact that the parts of Eqn. 4-3 that are dependent on U having become completely independent of V_{in} (as a result of V_{HT} being independent of V_{in}). A S&H circuit that does just that (V_{HT} control, but no V_{TL} control), is presented in chapter 6.2, see Fig. 6-15 c). Measurement results for this linearised S&H circuit are presented in chapter 7.4.

The CLFT plot of the basic S&H (Fig. 4-1) indicates, that under both fast and slow switching conditions CLFT is approximately linearly related to V_{in}. This suggests that INL, and therefore harmonic distortion, will be smallest under these conditions (i.e. for $U \gg U_x$ or $U \ll U_x$, for this circuit $U_x = 0.5\beta V^2_{HT}/C_h$ = 100MV/s, at V_{in} = 1.5V). Between these two

extremes, CLFT seems to be quite non-linear, suggesting a much larger, and very much clock fall-rate dependent INL. CLFT of the V_{HT} controlled S&H appears to be largely linearly dependent on V_{in}, suggesting that its INL is small.

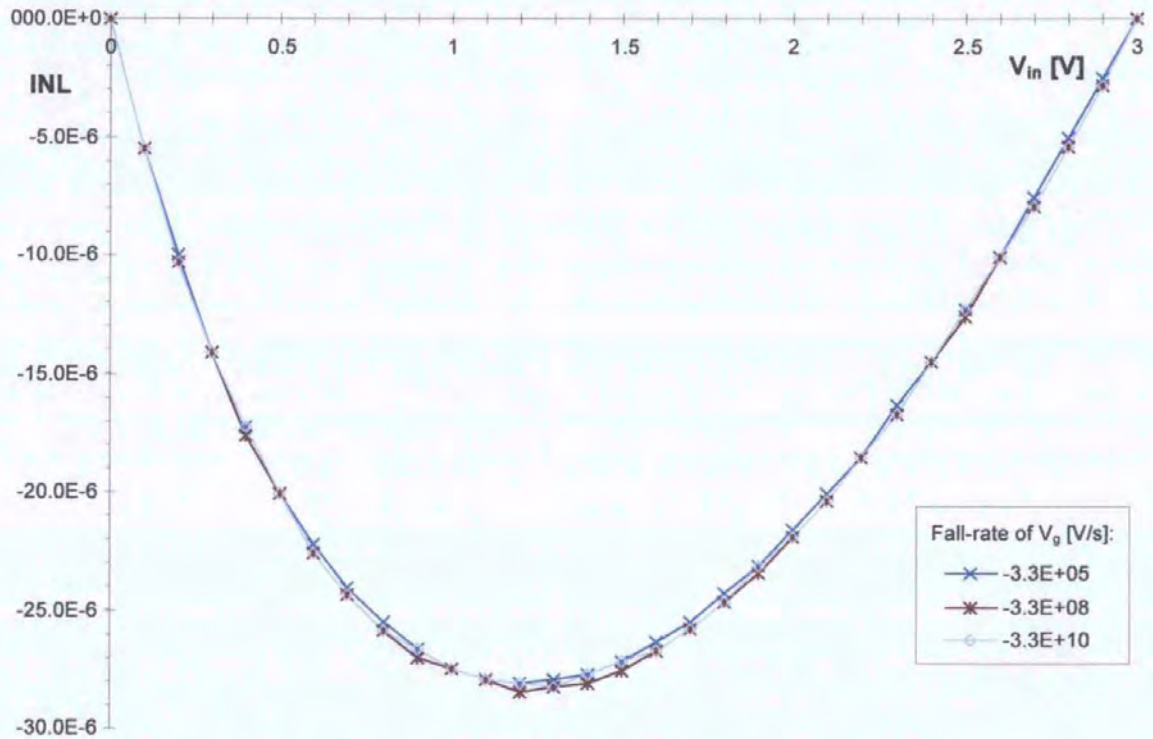


Fig. 4-3: INL plots for the V_{HT} controlled S&H circuit with U as parameter.

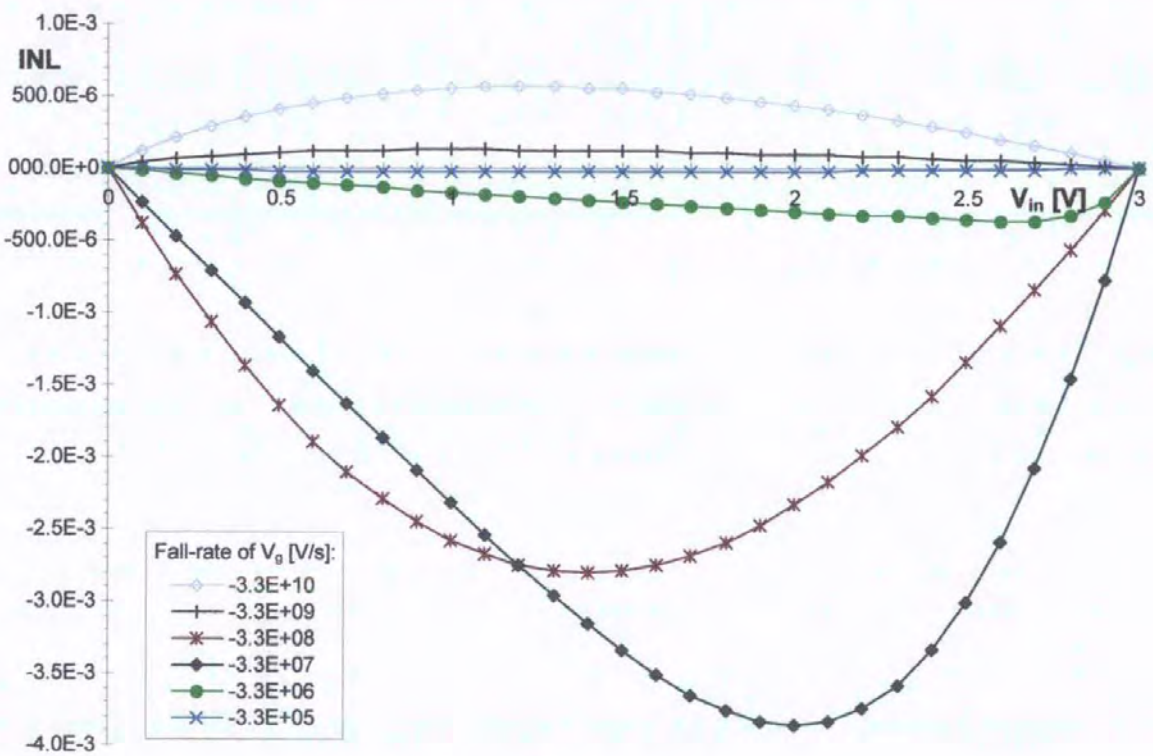


Fig. 4-4: INL plots for the basic S&H circuit with U as parameter.

Clearly, INL of the basic S&H is worst for $U \approx U_x$, and generally much worse than that of the V_{HT} controlled circuit, whose INL is independent of U. Interestingly, the basic S&H's INL can be seen to change sign between U = 3.3GV/s and U = 330MV/s. This suggests that there is a U at which the INL passes through zero. Any value between $V_{in,min}$ and $V_{in,max}$ may be chosen for V_{in} to search for the U at which $INL(V_{in}) = 0$. Choosing the mid-range voltage for V_{in}, i.e. $V_{in} = (V_{in,min} + V_{in,max})/2$, simplifies Eqn. 4-1 to:

$$INL_{MR} \cong \frac{CLFT\left(\frac{V_{in,max} + V_{in,min}}{2}\right) - \frac{CLFT(V_{in,max}) + CLFT(V_{in,min})}{2}}{V_{in,max} - V_{in,min}}$$

Eqn. 4-21

The clock fall-rate, U_{MR0}, at which $INL_{MR} = 0$ can only be found numerically. For the circuit parameters given we find U_{MR0} = 2.418GV/s for the basic S&H. The plot below shows the behaviour of INL for a few U close to U_{MR0}. Also shown are INL plots for slow switching and for V_{HT} constant.

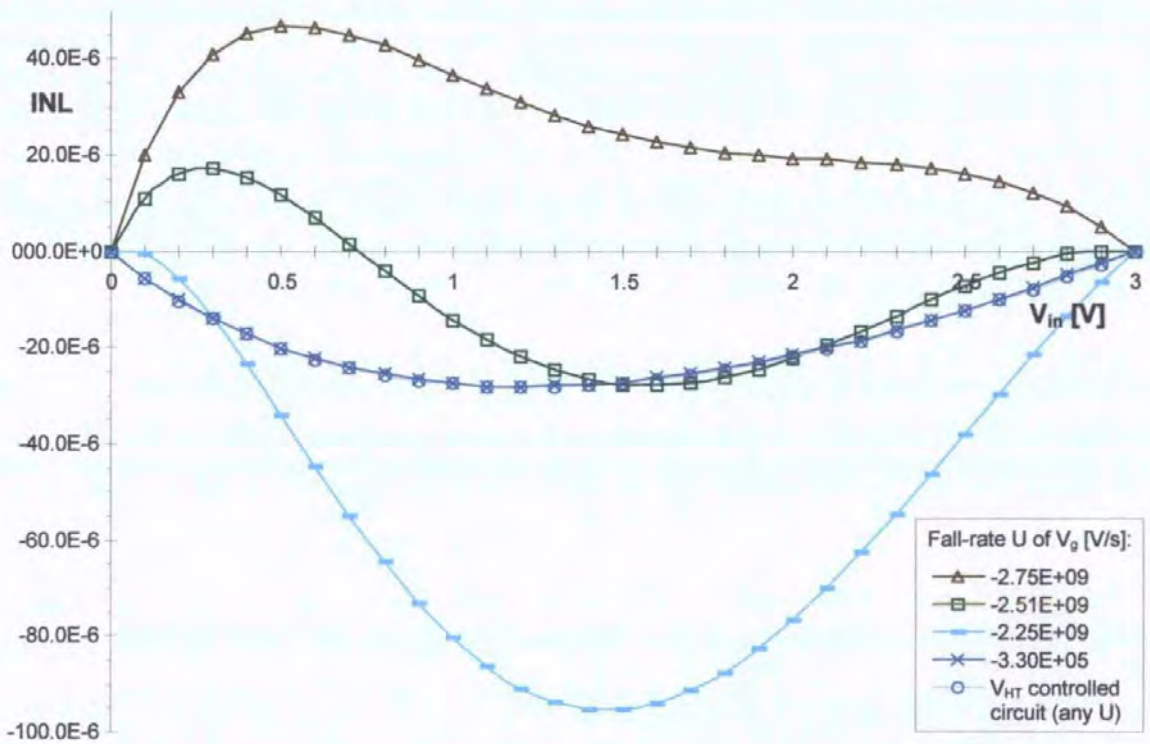


Fig. 4-5: INL plots for the V_{HT} controlled circuit and the basic S&H circuit (detail).

As expected from Eqn. 4-20, the INL for slow switching and for V_{HT} constant are identical. Compared to fast switching, the INL for slow switching, INL_{slow}, clearly is much lower (and the two are of opposite sign), which again had been anticipated by the differential equations (see Eqn. 4-19 and Eqn. 4-20).

Fig. 4-5 shows that U_{MR0} does not necessarily yield the lowest INL. It does, however, give a good initial estimate from which to search for the clock fall-rate U_0 at which INL goes through this local minima, INL_0. The plot also shows INL to be fairly sensitive to U around INL_0. This is not unexpected if one considers that this minima in the INL arises from the approximate cancellation of the two non-linear terms of Eqn. 4-18. At both fast and slow switching speeds the exponential's sensitivity to V_{in} is very small and distortion is determined by the square root term. Between these two extremes the sensitivity of the exponential term to V_{in} will normally be dominant (see Fig. 4-4); but at some point, U_0, the sensitivities of the equation's exponential term and its square root term will approximately cancel, and INL will have a minima, INL_0. Because the maxima, in the sensitivity to V_{in}, of the two terms lie at the opposite extremes of the V_{in} range the cancellation will be incomplete, thus resulting in the distorted INL shapes observable near INL_0. The magnitude of INL_0 is proportional to C_{ox}/C_h: the smaller C_{ox} the smaller INL_0 will be, but also the higher $U_0 \propto C_{ox}/(L^2C_h)$ will be (i.e. $U_0 \propto W/(LC_h)$ and $INL_0 \propto WL/C_h$). In fact, CLFT will be independent of V_{in} for $C_{ox} = 0$ and $U \rightarrow \infty$, as was shown in section 4.3.1. INL_0 will normally be significantly smaller than INL_{slow}, however, it may be larger than INL_{slow} if L is large ($INL_{slow} \propto W/C_h$).

4.3.4 Estimates for the THD and INL arising from CLFT.

From the INL plots it can be seen that, with the exception of $U \approx U_0$, the INL for these S&H circuits is approximately parabolic in shape. This suggests that CLFT causes,

predominantly, 2nd harmonic distortion in the output signal of the S&H, except for $U \approx U_0$, where the 2nd harmonic is reduced and higher order components are dominant. For S&H circuits where CLFT is the dominant source of distortion Eqn. 1-7 may therefore be used to estimate THD from the circuit's INL. A S&H circuit's THD is then (expressed in dB):

$$THD \approx 20\log(INL)$$

For parabolic shaped INL the graph will have its maximum at the mid-range point of V_{in}. Eqn. 4-21 for INL_{MR} may then be used to estimate the INL caused by CLFT. Applying this to the case of fast switching and assuming that $V_B = 0V$ it is found that:

$$INL_{fast} \approx -\frac{\gamma C_{ox}}{4C_h}\frac{\sqrt{2(4\varphi_F + V_{in,max} + V_{in,min})} + \sqrt{2\varphi_F + V_{in,max}} + \sqrt{2\varphi_F + V_{in,min}}}{V_{in,max} - V_{in,min}}$$

Eqn. 4-22

For slow switching, or V_{HT} constant, and $V_B = 0V$:

$$INL_{slow} \approx -\frac{\gamma C_{ol}}{2C_h}\frac{\sqrt{2(4\varphi_F + V_{in,max} + V_{in,min})} + \sqrt{2\varphi_F + V_{in,max}} + \sqrt{2\varphi_F + V_{in,min}}}{V_{in,max} - V_{in,min}}$$

Eqn. 4-23

Clearly, for fast switching and slow switching, the source of the distortion is the non-linear signal dependent component of V_T, which is of the form $\sqrt{2\varphi_F + V_{in} - V_B}$. In section 4.3.3 it was shown that distortion arising from this component will be smallest for large V_{in} (i.e. if the circuit is biased to large V_{SB}), something clearly visible in the plot of INL_{slow} over $V_{in,min}$ shown below. The plot was derived using Eqn. 4-23 and the circuit parameters given in section 4.3.3.2. It is also apparent that distortion reduces if the amplitude of the input signal is reduced and that distortion is inversely proportional to C_h (an increase in C_h leads to a directly proportional decrease in INL). Both equations also show that, the smaller the

pass-transistor the smaller INL will be: for slow switching, and V_{HT} constant, $INL_{slow} \propto W/C_h$ and for fast switching $INL_{fast} \propto WL/C_h$.

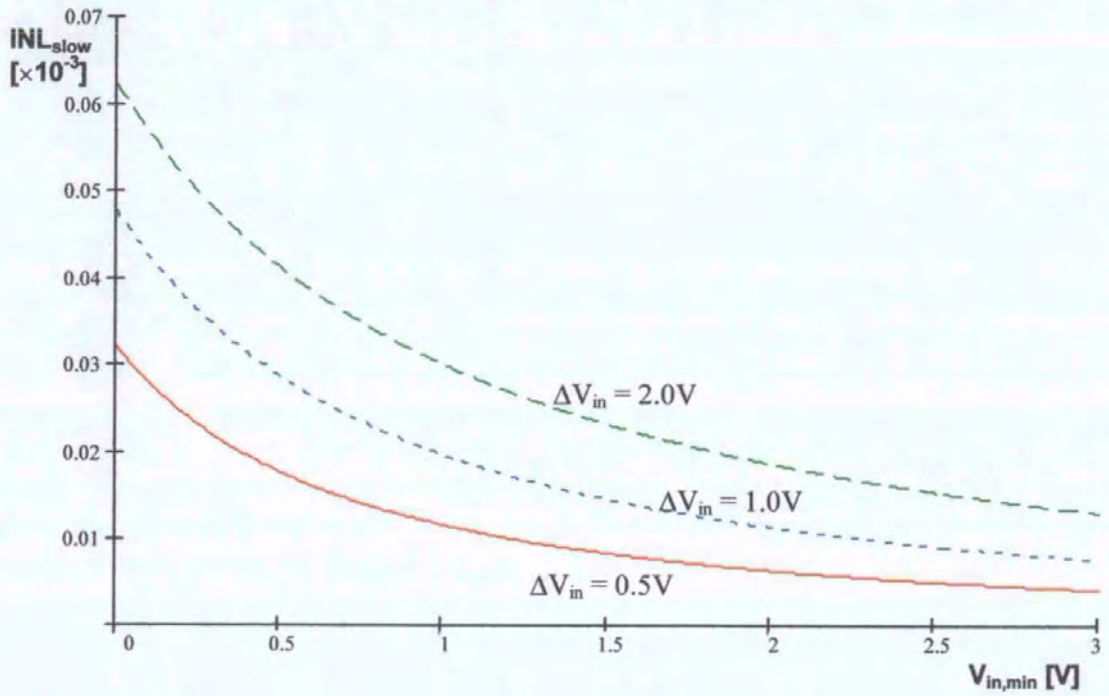


Fig. 4-6: Plot of estimated INL_{slow} with $\Delta V_{in} = V_{in,min} - V_{in,max}$ as parameter.

4.4 Conclusions to signal dependency of CLFT.

In this chapter the signal dependency of CLFT in the basic S&H circuit with zero signal source impedance was investigated. It was found that:

1. CLFT becomes independent of V_{in} if:
   a) both V_{HT} and V_{TL} are constant and independent of V_{in}.
   b) $U \ll \beta V^2_{HT}/(2C_h)$ and V_{TL} is constant and independent of V_{in}.
   c) $U \gg \beta V^2_{HT}/(2C_h)$ and the pass-transistor's Source is on the input side of the S&H circuit and the pass-transistor remains in saturation throughout turn-off (C_{ox} on the output side of the circuit will then be $\cong 0$).
   d) U is related to V_{in}, i.e. if $U = \dfrac{\beta V_{HT}^2}{2C_h \ln\left(\dfrac{C_{ox}}{2C_{ol}} + 1\right)}$; see section 4.3.1.

2. CLFT will become linearly dependent on V_{in} for any of the following conditions if:
   a) both V_{HT} and V_{SB} are constant and independent of V_{in}; $dCLFT/dV_{in}$ is proportional to $-C_{ol}/C_h$.
   b) $U \ll \beta V^2_{HT}/(2C_h)$ and V_{SB} is constant and independent of V_{in}; $dCLFT/dV_{in} \propto -C_{ol}/C_h$.
   c) $U \gg \beta V^2_{HT}/(2C_h)$ and V_{SB} is constant and independent of V_{in}; $dCLFT/dV_{in} \propto C_{ox}/2C_h$.
   d) $U \gg \beta V^2_{HT}/(2C_h)$ and both V_{TL} and V_{SB} are constant and independent of V_{in}. For this $dCLFT/dV_{in}$ will be proportional to $(C_{ol} + C_{ox}/2)/C_h$.
   e) $U \propto V^2_{HT}$ and V_{SB} is constant and independent of V_{in} (see Eqn. 4-5). Here $dCLFT/dV_{in}$ depends also on β and C_h, and may vary between $(C_{ol} + C_{ox}/2)/C_h$ and $-C_{ol}/C_h$.

3. Under any other condition CLFT will introduce a non-linearly signal dependent component to the circuit's output signal. The INL of the S&H will then be non-zero, and the circuit's output signal will experience some harmonic distortion. INL was found to be worst for $U \approx U_x = 0.5\beta V^2_{HT}/C_h$, which thus must be avoided if low levels of distortion are required. INL was generally smallest (see section 4.3.3):

   a) at U_0 where INL goes through a minima, INL_0. Distortion at this point will normally be smaller than for slow switching (or V_{HT} constant), but may however be bigger if L of the pass-transistor is large. $INL_0 \propto WL/C_h$, but increases fairly quickly if U moves away from $U_0 \propto W/(LC_h)$, see section 4.3.3.2.

   b) if V_{SB} is high for V_{HT} being constant and independent of V_{in}; also $INL \propto W/C_h$.

   c) if V_{SB} is high for $U \ll \beta V^2_{HT}/(2C_h)$; $INL \propto W/C_h$ also applies.

   d) if V_{HT} is high for $U < U_0$, a large β also helps, additionally $INL \propto W/C_h$ applies.

   e) if V_{SB} is high for $U > U_0$; here $INL \propto WL/C_h$.

   Of all the harmonic distortion components introduced, the 2nd harmonic distortion was normally the largest; except for $U \approx U_0$, where the 2nd harmonic was reduced, and higher order components were dominant.

5. A brief overview of CLFT reduction schemes.

This chapter looks at the implementation of S&H circuits on silicon.

A brief overview of CLFT reduction schemes is given at the start of this section. This overview was intended only as a very brief introduction to the field. What it attempts is to show the wide variety of circuit solutions and strategies that have been developed to overcome the problem that CLFT presents. Literature references are given, and the schematics for some of the circuits are included in Appendix C.

The overview is followed by a short section listing some of the parasitic effects and processing variations that may degrade a circuit's performance. A concise summary of the dummy compensation technique is included in this section, which illustrates some of these points. Some results from measurements on a circuit using discrete devices are also reported in this section.

The chapter concludes with an examination of the impact that a S&H circuit's pass-transistor channel geometry and channel doping gradients have on the circuit's CLFT performance. It will be shown that use of non-rectangular switching devices, and/or devices with non-uniform doping gradients in the channel region, can lead to significant reductions in CLFT.

5.1 Overview of CLFT reduction techniques for S&H circuits.

Many schemes have been proposed to overcome clock-feedthrough (CLFT). These can be divided into two main groups, according to whether active or passive techniques were used in controlling CLFT. The active CLFT reduction techniques may be subdivided further by the choice of control method, into circuits employing open-loop controls, or circuits using closed-loop control methods.

5.1.1 Passive CLFT reduction techniques.

These circuits do not employ any active circuits, such as, for example, operational amplifiers, in the control of CLFT or inject a charge of opposite polarity onto the hold capacitor in an attempt to reduce, or indeed eliminate, CLFT. Instead, the error voltage is reduced:

1. through the use of a large hold capacitance C_h.

   For a given size switch this has its limitations in that large C_h mean long acquisition times. They also require much chip area, or need to be external, both options tend to make a chip more expensive. Advantages include reduced k_BT/C noise and a reduced droop-rate. For some applications such as auto-zero and offset compensation of amplifiers (where long acquisition times do not normally pose a problem), these benefits may well outweigh the costs.

2. by diverting the error charge away from the hold node. Possible methods are:

   a) use of multi-phase clocking schemes in circuits in which both sides of the sampling capacitor are being switched [36], [37].

      If one of the two sampling switches connects to a fixed reference potential, e.g. GND and the other to a variable potential, e.g. V_{in}, then turning the one at the fixed potential off first will induce a constant CLFT on the hold capacitor C_h. Also it will

break the current path through C_h, and therefore prevent the second switch from inducing any error on C_h. CLFT from such a circuit should, in theory, be signal independent. The presence of parasitics will however limit the performance improvement that is practically achievable. The CLFT rejection achievable is similar to that of the bottom-plate transient suppression device discussed in chapter 6.1.

b) increasing the conductive current in the pass-transistor during turn-off (e.g. by increasing the impedance of the hold node, see chapter 6.1).

c) non-uniform doping of the pass-transistor [17], see section 5.3.2.

d) non-rectangular switching device [7], see section 5.3.1.

e) use of non-constant clock fall-rates instead of the linear fall-rate normally assumed. This could prove advantageous since the turn-off trajectory could be engineered such that the transistor switch will remain proportionally longer in the linear region, thus increasing the time for the 'compensating' transport current to flow, hence reducing CLFT. It may even be possible to achieve signal-independent CLFT in that way (see chapter 4.3.1).

f) using the charge pumping effect [10] (an effect no one seems to have made use of to date).

3. through calibration and correction of the final output signal.

This technique can be used on A/D converters that are laser trimmed during manufacturing, or linearised by other techniques. If the S&H circuit suffering from CLFT is included in the calibration process the non-linearity caused by it may, to some extent, be eliminated and thus increased linearity of the S&H circuit plus A/D converter combination achieved over what was originally permitted by CLFT.

4. by avoiding charge coupling altogether.

Mechanical or other inert switching devices that do not introduce an error charge to the signal path, such as light dependent resistors (LDR) or micro-mechanical devices (MEMS) can potentially avoid charge injection altogether.

5.1.2 Active CLFT reduction techniques.

Active reduction, or control of, CLFT may be achieved through either open-loop or closed-loop control circuitry, the latter are inherently slower. Propagation delay and settling times (mainly of the feedback path) slow these down and may even lead to instability. Saturation of amplifier output stages can occur in some active circuits (often if a feedback loop is broken), which again may lead to longer acquisition times, as saturated amplifiers need considerable time to recover.

5.1.2.1 Open-loop solutions.

Open-loop CLFT reduction circuits often make use of one of the following techniques.

1. compensate or cancel the error charge on the hold capacitor through
   a) dummy compensation [38], [39], [40], [9] & [25], one of the best known and most widely used techniques (see also section 5.2.1).
   b) use of complementary transistors as switching elements (the CMOS transmission gate) [38] and [41] to [43]. During turn-off the two complementary transistors inject charges of opposite polarity onto the hold node. CLFT will thus be reduced, complete cancellation (for one particular input voltage) is possible.

2. hold CLFT constant by
   a) keeping one end of the switch at a fixed potential, quite often ground or virtual earth. This is often the case with integrator type S&H circuits and switched capacitor

integrators [35], [44] & [45], where the switch output is connected to an operational amplifier input, i.e. to virtual earth.

b) developing the sampling clock and the Bulk potential of the switch relative to the sampled signal [35]. Both the sampling clock and the Bulk potential are developed at constant levels above and below the sampled signal (see also section 4.3.1).

3. perform error cancellation on the circuit's (analog) output signal. Examples are

a) the 'Watanabe circuit' [46].

In this circuit CLFT cancellation is achieved by turning a device identical to the pass-transistor 'ON' when the pass-transistor is being turned 'OFF'. On its Source side this additional device is being supplied with a buffered version of the held signal while its Drain side is connected to the hold capacitor through a DC-blocking capacitor (see Appendix C for the circuit diagram).

b) CLFT cancellation using replication circuits [45], [47].

In the circuit described in reference [45] a differential amplifier's reference potential was modified. A voltage equal to the CLFT error was added to the differential amplifiers reference signal (not unlike an offset compensation). The circuit in [45] only eliminated the signal independent component of CLFT from its output.

In [47] the replication technique was applied to switched current circuits. The circuits discussed in this paper can reduce both signal dependent and signal independent CLFT errors in switched current circuits.

c) fully differential circuits, for example the circuit presented in [48].

Differential circuits attenuate any unwanted DC offset and even order harmonic distortion components. However, they do not reduce the magnitude of odd harmonics. The cost is added circuit complexity and larger silicon area.

d) quasi-differential circuits, for example the circuit presented in [49].

The circuit presented in [49] is very interesting, in that the designers went to great lengths to keep the circuit as symmetrical as possible. They even included buffer amplifiers and load cells to make the transient impedances seen by the pass-transistors in the circuit as symmetrical as possible.

4. employ redistribution of the error charge, as in the case of the circuits that employ a Miller enhanced capacitor [50], [51].

5. reduce CLFT induced distortion by linearising CLFT's signal dependent component.

A circuit using this technique is being presented in chapter 6.2.

5.1.2.2 Closed-loop solutions.

Very few examples of the closed-loop approach to CLFT reduction were found in the literature. The methods found employed the following approaches:

1. error feedback.

The feedback compensated current memory cell [52] is an example for this. Initially, a coarse acquisition of the signal is performed. This coarse acquisition results in a output signal that is too large. It is then followed by a fine adjust, in which a feedback network reduces the output signal until the error is within acceptable limits, at which point the feedback network is turned off and the signal is acquired.

2. modification of clock trajectories [42].

This scheme was employed in a SC integrator, where turn-off rate of the PMOS transistor in the CMOS transmission gates was controlled such that the CLFT error generated by the transmission gate was significantly reduced.

3. adaptive clock signal modification in dummy compensated circuits [53].

This scheme was employed in a switched-current circuit, where the delay between the two clocks was adaptively controlled such that the signal independent CLFT error (the offset component) was greatly reduced.

The list is by no means complete. Examples for switched current cells (current memories, dynamic current mirrors, current copiers and the like) and switched capacitor filters were generally not included, if other examples for a particular CLFT compensation technique were found. Schematic diagrams for some of the techniques mentioned in this section are included in Appendix C.

5.2 Effects that can impair the efficacy of CLFT reduction schemes.

On implementation, a CLFT reduction scheme may not perform as predicted by theory or simulations. Some of the possible causes for this mismatch between predictions and actual results are given below:

- parasitic capacitances in integrated circuits can be quite large. The parasitic bottom plate capacitance of an integrated poly-poly capacitor for example is between 10% and 30% of the nominal value, depending on the process used.
- statistical variations across the chip for process parameters like doping levels, oxide thickness and other geometry and processing related effects, can limit the performance of circuits that require matched devices.
- second order effects, non-linearities and failure to take all modes of operation of the underlying device models into account may lead to erroneous CLFT, and transient behaviour predictions. This may lead to the CLFT compensation circuitry 'under', or even 'over' performing, which in some cases may make the CLFT problem even worse. Amongst these second order effects are, voltage dependency of capacitors (often caused by low doping levels or parasitic junction capacitances), and charge pumping in the pass-transistor during turn-off which can lead to lower CLFT levels than expected (charge pumping is neglected in many models).
- non-ideal behaviour of signal sources and other circuit elements. The trajectory of the clock signal could be different from the assumed, or simulated one, and its fall-time could vary much more widely than anticipated, due to temperature and supply voltage variations.
- resistive and capacitive parasitics associated with on-chip interconnects as well as pin inductance and mutual inductance between pins for signals from off-chip sources.

- dielectric absorption in the hold capacitor and/or parasitic capacitances (see section 5.2.3).

5.2.1 An example: Dummy compensation.

The dummy compensation technique [38], [39], [40], [9] & [25] is a good example of how unaccounted effects can diminish a CLFT compensation technique's effectiveness.

Dummy compensation is based on the idea that half of a pass-transistor's channel charge flows to the Source, and the other half to the Drain. If a charge of exactly half the original channel charge and opposite polarity were then injected onto the hold node CLFT should be eliminated altogether. This can theoretically be achieved by using a dummy transistor M1d (a short-circuited transistor) with half the Gate area of the switching device M1 (see Fig. 5-1). The dummy device is driven by a clock, complementary to the switch clock. Under ideal conditions, it would not matter how the halving the Gate area of M1d was achieved. In reality, the parasitic overlap capacitance (mainly caused by lateral diffusion of the Drain and Source implants under the Gate and fringing effects on the Gate edge) must be taken into account. Half-width dummy devices give therefore better results, because they have essentially the same overlap capacitance as the switch. Other effects that reduce CLFT, and thus lead to over-compensation, include charge pumping and the conductive current flow in the switch during turn-off. Device mismatch and delay between the two clocks can lead to either over-compensation or under-compensation of CLFT. Perfect cancellation of CLFT over the whole input signal range was found to be impossible [38], [39]. The best that can be achieved is cancellation of

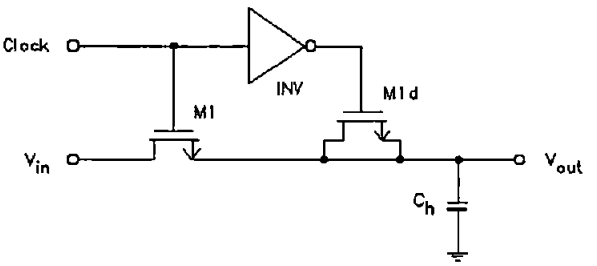


Fig. 5-1: Dummy compensation, principle.

CLFT at one particular input voltage [38]. This is also illustrated by measurements performed on a dummy compensated circuit that follow below.

5.2.2 Test results from a dummy compensated S&H circuit using discrete devices.

CLFT voltages of a S&H circuit that employed a half-width dummy compensation (for diagram see Fig. 5-1) and an uncompensated S&H circuit are plotted in Fig. 5-2. The circuit was realised using discrete devices. Of the devices used the MOSFETs were SD214 type NMOS transistors from Siliconix, and the clock buffer circuit was a 74HC4049, which is a standard digital high speed CMOS inverting bus driver. The hold capacitor was a 220pF polystyrene capacitor. Rise-times and fall-times of around 3ns for a 0V to 5V swing of the clock signals were achieved. Two discrete SD214, that were connected in parallel (W = 2, L = 1), served as the pass-transistor (switching device). The dummy was created by shorting Drain and Source of a single SD214 together. A brief description and schematic of this test circuit have been enclosed in the Appendix D.

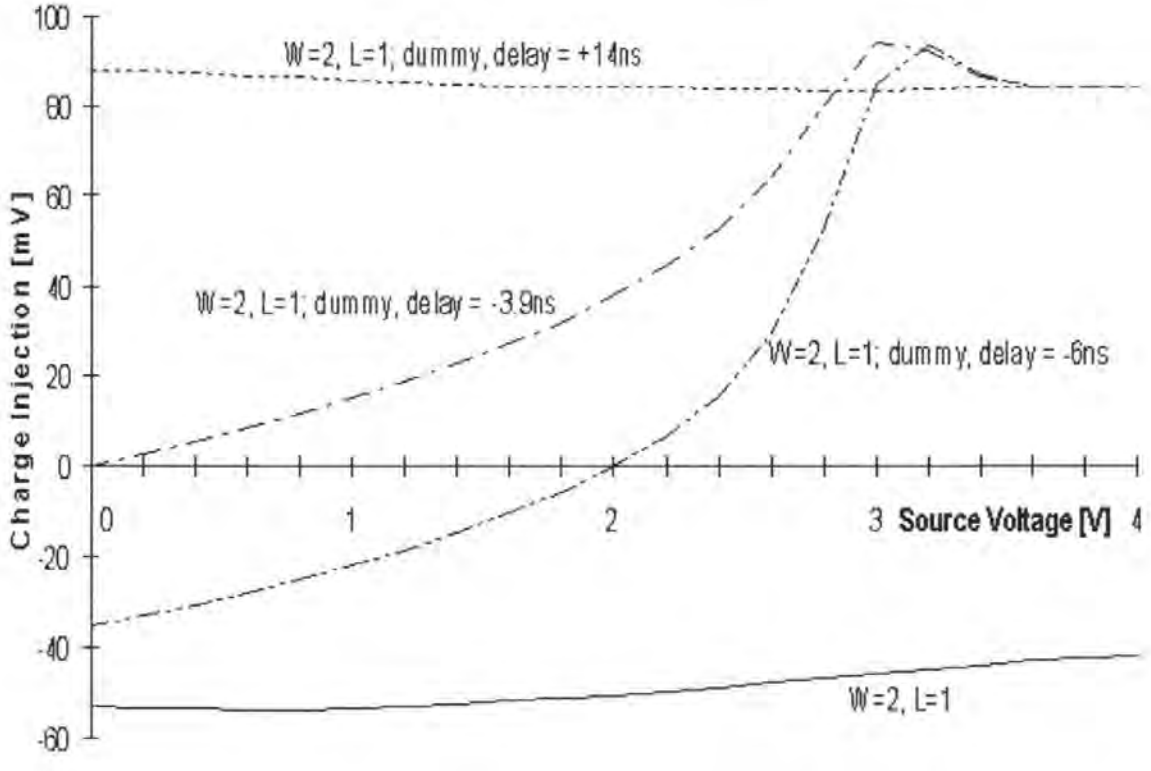


Fig. 5-2: Measured CLFT for half-width dummy compensation.

The graph clearly shows that, under the conditions of the experiment, dummy compensation actually worsened the signal dependency of CLFT. Undoubtedly it can be used to eliminate CLFT for a desired input through adjusting the delay between dummy clock and switch clock. However in doing so, CLFT becomes much more signal dependent as the graphs clearly show. A notable exception was the case of a dummy clock delay of +14ns. Here CLFT was positive, and the signal dependency of CLFT was reduced, but its magnitude was almost double the size of CLFT in the uncompensated circuit.

5.2.3 Droop rate and dielectric absorption.

On this test circuit a most peculiar behaviour of the droop was observed for all circuit configurations and input voltages tested. Peculiar, as it deviated substantially from the expected waveform (see Fig. 5-3 below). The expectation was that droop (i.e. the loss of charge on the hold capacitor when in hold mode) would approximately follow an exponential curve, until the capacitor was fully discharged. However, reality proved to be quite different. After the turn-off transient had finished the voltage across the hold capacitor settled briefly at a CLFT determined low of -40mV before recovering roughly +5mV in about 10μs (see Fig. 5-3 below). This recovery was in the region of 4mV to 5mV (about 10% to 15% of the CLFT voltage) for all input voltages, and was always opposing the CLFT induced error voltage.

The most likely explanation for this behaviour was dielectric absorption [54] in the hold capacitor. Dielectric absorption is also known as capacitor soakage [55]. It is a dynamic error in the transient response of a capacitor, and arises from the fact that not all of the dielectric polarisation in the capacitor may take place immediately when a capacitor is charged or discharged. Consequently, there can be an appreciable residual charge (voltage), with a relatively long time constant, which opposes a fast change in the capacitor voltage. Dielectric absorption does not appear to be an issue with the linear capacitors that are

available on mixed signal processes, such as poly-poly capacitors or metal-insulator-metal capacitors.

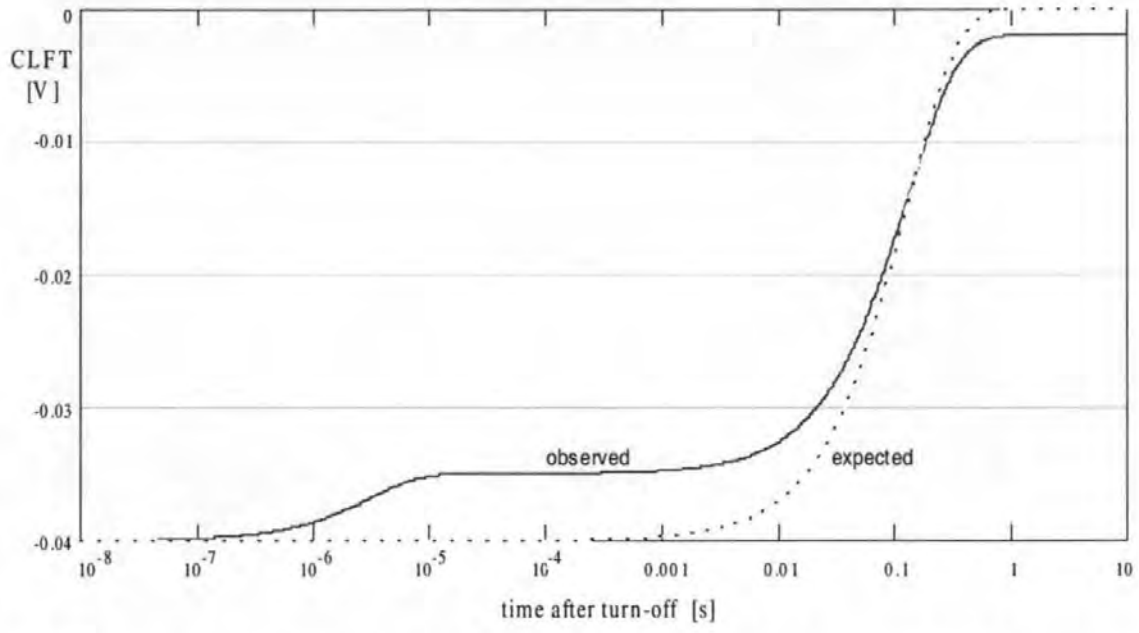


Fig. 5-3: Comparison between expected and observed droop for the example of the uncompensated S&H circuit with a single SD214 as switch (W = 1, L = 1) and $V_{in} = 0$.

5.3 Non-rectangular shapes and non-uniform doping.

Kuo, Dutton and Wooley achieved CLFT reduction on the basic S&H circuit (see Fig. 2-1) with non-uniformly doped [7] and semicircular [17] MOS switching device. For semicircular devices they reported CLFT up to a factor of 3.2 less, compared to rectangular N-channel MOSFET with identical Gate area and length. The improvement was fall time independent. With non-uniform doping, the improvement was much less. It was between 10% and 50%, for the fall times studied. Maximum reduction was achieved with slow switching.

5.3.1 Non-rectangular shapes.

As previously mentioned a fall time independent improvement of CLFT for semicircular MOSFETs was reported by Kuo et al [17]. They found that large ratios of outer to inner circumference gave maximal CLFT reduction (Fig. 5-4).

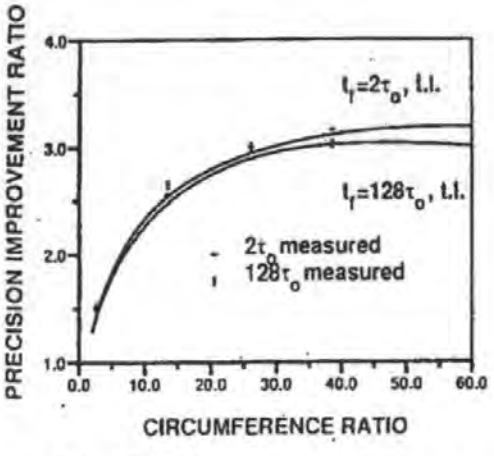


Fig. 5-4: CLFT improvement of semi-circular over rectangular MOSFETs [17].

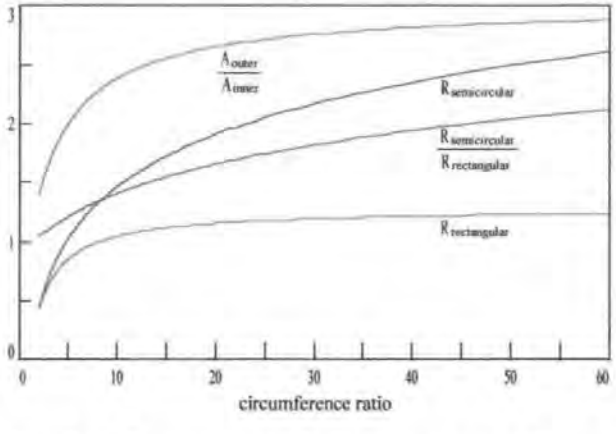


Fig. 5-5: Comparison of key parameters of rectangular and semicircular shapes.

5.3.1.1 Reasons why CLFT reduces as the circumference ratio increases.

Assuming the usual split of the channel charge at L/2 (half way along the channel) between Drain and Source, a ratio of the two charges can be defined. This ratio is identical to the area ratio A_{outer}/A_{inner}, which approaches 3 for large circumference ratios (see Fig. 5-5). It

can be seen that almost three times as much charge is associated with the outer contact than with the inner.

$$A_{rect} = WL$$

$$A_{semicirc} = \pi r_i^2((r_i/r_o)^2 - 1)/2 = WL; \text{ where } W = \pi r_i(r_i/r_o + 1)/2 \text{ and } L = r_i(r_i/r_o - 1)$$

For channel resistance a similar, asymmetrical, effect is noted. The resistance increases towards the inner contact (Fig. 5-5), making it more difficult for the channel charges to travel in this direction. The preferred direction of travel of these is thus towards the outer (wider) contact, meaning that during turn-off even more channel charge leaves the transistor through the outer channel contact than assigned by the L/2 channel partitioning. Examination of the channel charge distribution during turn-off (see Fig. 5-6 below) confirms this reasoning.

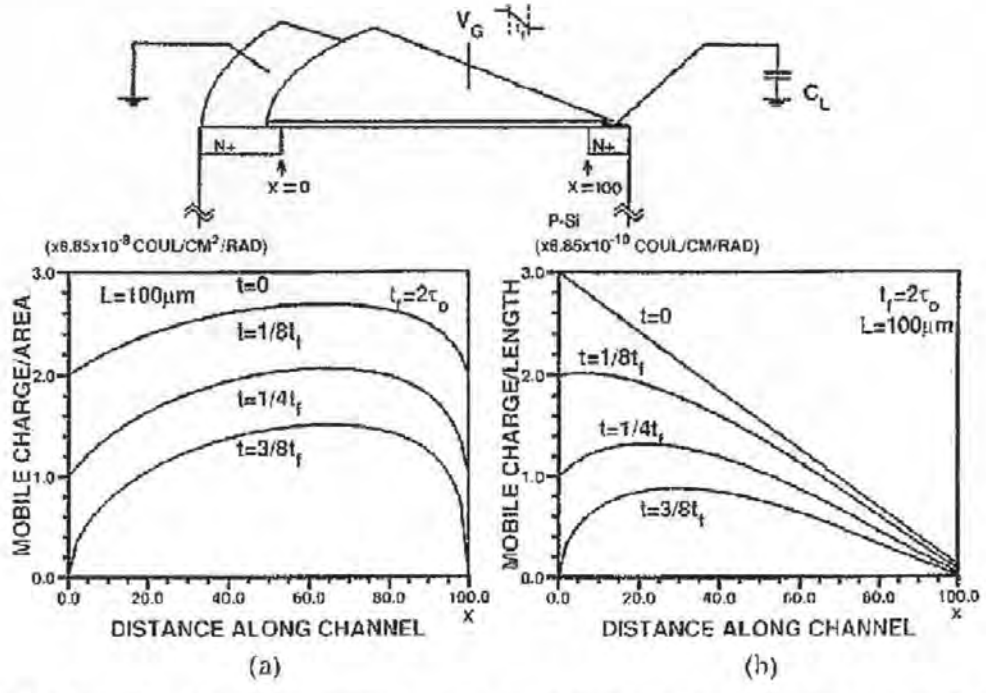


Fig. 5-6: Profiles of mobile charge distribution along the channel of a circular geometry pass-transistor during turn-off (reproduced from [17]). C_h = 210pF, t_f = 100ns. (a) Mobile charge density per unit area. (b) Mobile charge density per unit length.

These plots show that charge accumulates near the inner contact during turn-off, thus increasing the charge density in this area. This repels other electrons driving them in the

direction of the outer contact, where charge density is lowest. For faster switching charge accumulation worsens, therefore increasing CLFT reduction even further (see Fig. 5-4, where CLFT improvement is shown to be higher for $t_f = 2\tau_0$ than for $t_f = 128\tau_0$; where τ_0 is the carrier channel transit time as defined in Eqn. 2-11).

5.3.1.2 Other advantages of asymmetrical MOS switches.

The narrow inner contact of the semicircular device is desirable, because it results in a small overlap capacitance hence in reduced CLFT.

A small circumference of the inner contact also implies a small 'Source' implant area which means that the junction area of the parasitic diode (implant to Bulk) is small. The junction leakage current and parasitic junction capacitance of this diode (both proportional to the junction area) will consequently be small. A small leakage current gives a low droop rate and a small junction capacitance is advantageous for many circuits, especially for the proposed TSD circuits (presented in chapter 6.1).

The width of the inner contact can, obviously, be no less than the minimum feature size, thus imposing a lower limit to these beneficial effects.

5.3.1.3 Disadvantages of non-rectangular MOS switches.

Non-rectangular devices exhibit higher 'ON' resistance than rectangular devices of identical channel length and area, entailing longer acquisition times for S&H circuits that utilise them as switching devices.

Modelling of CLFT and transient behaviour is also more demanding, because the single-lump model of Sheu and Hu [6] is not adequate, consequently requiring the use of the more evolved two-lump model. Circuit simulators such as SPICE or Spectre do not normally provide models for non-rectangular devices. Any such device tends to be approximated by

a rectangular device of equal Gate-length and Gate-area, when running simulations on extracted circuits containing such odd shaped devices.

5.3.2 Non-uniform doping.

For non-uniform doping of the channel region Kuo et al [7] reported some improvement over the normal case of uniform doping. Judging from Fig. 5-7 the relative CLFT improvement would have been in the range of 10% to 50%. However, expressed in terms of absolute error charge, it seems that the reduction was fairly constant. Between 1.3pC and 1.7pC for the ¾ standard, and 2.1pC to 2.6pC reduction for the ¼ standard n-channel MOSFET were calculated for a hold capacitor of 210pF. This is interesting, because it means that the reduction in error charge appears to be independent of clock fall time.

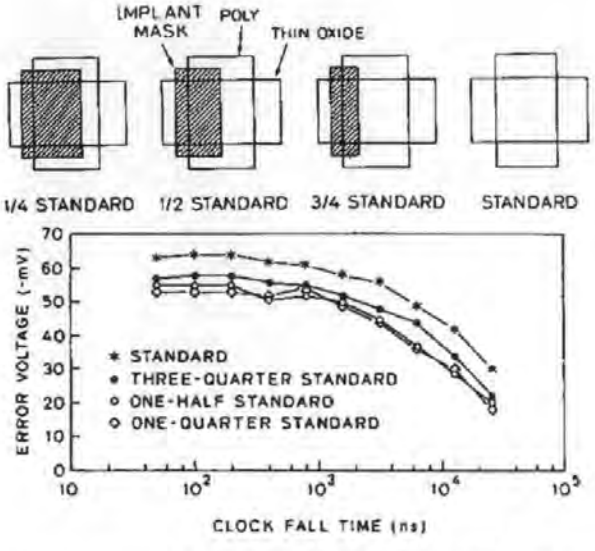


Fig. 5-7: Partially doped pass-transistors and their induced CLFT; taken from [7].

The experimental circuits were manufactured in a 2μm CMOS process with the circuit parameters being as follows:

$$W = 100\mu m,\ L = 100\mu m,\ \mu = 500 cm^2/V,\ t_{ox} = 39nm,\ V_{T0} = 0.5V,\ V_{T0,masked} \approx 0V,\ \gamma = 0.3V^{½},$$

$$V_{in} = 0V,\ V_B = -4V,\ +4V \geq V_G \geq -4V,\ C_h = 210pF;\ \text{hence, } V_T = 1V \text{ and } V_{T,masked} \approx 0.5V.$$

With this, the total channel charge for the standard device is found at 26.6pC. For the ¼ standard 29.9pC, ½ standard 28.8pC and ¾ standard 27.7pC. The choice of large

MOSFETs (2500 times the area of the smallest possible transistor) enabled Kuo et al to neglect short-channel effects and overlap capacitance in their analysis of the experiments.

Non-uniform doping was achieved by partly masking the boron channel implant that was used to adjust the threshold level of the n-channel transistor (see Fig. 5-7). This lead to a lower threshold voltage, V_{T0}, in the masked part of the channel. CLFT was reduced if the part with the lower V_{T0} was connected to the signal source.

This phenomenon can be explained as follows: During turn-off the electrons that created the channel are leaving the MOSFET because the Gate voltage that maintained the channel collapses. Since electrons are attracted to high potentials they will seek out these and travel towards them. In a FET these are the Drain and the Source. If the potential in the channel close to the input side can be sustained at a higher level, compared to the hold capacitor, the preferred direction of travel for the electrons will be towards the input; fewer electrons will therefore reach the load resulting in lower CLFT.

A device level explanation is that this technique effectively creates two transistors with different V_{T0} in series. The transistor with the lower threshold voltage is more strongly inverted, and therefore is a better conductor. This leads to more channel electrons choosing it as their escape path. Thus, CLFT will be reduced, if this side is connected to the signal source (even though the total channel charge of non-uniformly doped devices was higher than of the uniformly doped MOSFET).

The reasons why CLFT is reduced, if the side with the higher threshold voltage is connected to the hold capacitor, C_h, are as follows: As the Gate voltage falls, this part of the transistor cuts off first, effectively isolating C_h from the rest of the circuit. Therefore, none of the excessive charge (due to the lowered V_{T0}) can reach the hold node. Since the conductivity of the composite device is higher than the standard device's (its, on average,

more strongly inverted) a larger compensating current can be expected to flow. Hence CLFT is reduced.

5.3.3 Consequences of asymmetrical behaviour for modelling.

Normal device models, such as those used in SPICE, are based on rectangular shaped, uniformly doped, and hence symmetrical MOSFETs. Non-rectangular shaped MOS transistors however exhibit asymmetrical behaviour in both their transient and DC behaviour.

The effects of device asymmetry on transient behaviour, and hence on CLFT, have been presented in this section. The consequences for DC behaviour were described by B. Riccò [56] for the example of trapezoidal MOSFETs. He found that output conductance in saturation, $g_{o,sat}$, was higher in the forward direction (narrow Source, wide Drain), than in the reverse direction (wide Source and narrow Drain). Clearly, a non-rectangular NMOS device with the narrow end connected to the hold capacitor will exhibit a lower 'ON' resistance for charging than for discharging of the hold capacitor, i.e. charging is faster than discharging. In PMOS FETs the effect is reversed. A similar behaviour could be expected from the non-uniform doped pass-transistor, however, no data to support this hypothesis is available.

SPICE and other circuit simulators do not model these asymmetrical MOSFETs correctly. The distributed model can emulate all aspects of non-symmetrical behaviour for these devices if threshold voltage and channel width are taken into account [7], [17]. To some extent this is also true for the two-lump model, although precision is not as good.

5.3.4 Considerations for circuit integration.

Non-rectangular devices will always have to be bigger than a quadratic minimum feature size MOS transistor, simply because of photolithographic restrictions which stipulate that any shape smaller than the minimum feature size can not be reproduced. In addition, many processes have a restriction that patterns can only be constructed from straight lines, 90° and 45° angles. Hence, rounded shapes, such as circles and semicircles can only be created by means of approximation; good approximation leads automatically to large devices. In modern deep sub-micron processes, the difference in size between square and circular devices may not be all that big, as corners tend to be much more rounded, anyway (due to photolithographic resolution issues).

An advantage of the non-uniform doping approach is that it can be adopted for minimum feature size devices. This is because the approach taken is to partly mask the channel implant used to adjust the zero threshold voltage of the pass-transistor. This threshold mask, perforated over the channel area of the NMOS transistors (where raising the threshold voltage above zero is desired) and covering the PMOS transistors completely (threshold voltage must remain below zero), can be placed such that it covers the part of the n-channel MOSFET's Gate area (Fig. 5-7), where lower threshold voltage is desired. The perforated area will have to comply with the minimum feature size requirement, but can be offset against the Gate area such that only part of it comes to lie over the channel; the rest will lie over the Source implant. Commonly, design rules allow much finer steps for this offset i.e. for placing objects relative to each other, or for increasing an object's size over the minimum feature size.

6. Proposed S&H circuits with reduced CLFT error.

New circuits that have the potential of reducing the error voltage at very little extra cost are presented.

Circuits that exploit the CLFT's sensitivity to mismatch between the pass-transistor's Source and Drain terminating impedances are presented. These circuits employ 'transient suppression devices' which increase the impedance of the S&H circuits output node. The circuits can reduce levels of CLFT and distortion at very little extra cost (in terms of circuit area).

A circuit that linearises CLFT by minimising the impact of the body effect on the MOS switches' inversion layer charge is introduced. This circuit can, potentially, reduce the harmonic distortion arising from CLFT by more than two orders of magnitude. Additional benefits include a constant aperture delay and reduced aperture jitter.

The CLFT reduction schemes presented are easily transferable to other circuit configurations.

6.1 CLFT reduction using transient suppression devices.

The circuits suggested are based on the idea that an increase in the conductive current in the pass-transistor during turn-off reduces CLFT. For a given switch this can be achieved only through an increase in the voltage v_{ds} across it. In other words the potential at the hold node must deviate even further from the input voltage, V_{in}, than would normally be caused by CLFT. This can be done by either reducing the size of the hold capacitance or through increasing the impedance of the hold node, or indeed a combination of both. Unfortunately, this technique can reduce CLFT only as long as a transport current, i_{ds}, can flow in the pass-transistor's channel (i.e. between its Drain and Source). This, as we have seen in chapter 2, only happens during Phase 1 of turn-off, i.e. while the transistor's Gate voltage is above threshold ($V_{TH} = V_S + V_T$). The CLFT component for V_G below V_{TH} (the Phase 2 of turn-off), which is mainly due to the overlap capacitance, remains virtually unaffected.

6.1.1 Theoretically achievable CLFT improvement.

Obviously, the biggest reduction in CLFT could be achieved if the error charge could be prevented from reaching the hold capacitor, C_h. For this, the pass-transistor must, somehow, be disconnected from C_h during turn-off (it will only be necessary to disconnect it from C_h during turn-off, as the error charge transfer only takes place during that time). The output load seen by the pass-transistor, Z_L, would then be infinitely large, and all the error charge generated during the Phase 1 of turn-off would be diverted away from C_h and onto the signal source. That this must be so becomes immediately clear when one considers that the pass-transistor will be 'ON' throughout the Phase 1. Now, because of $Z_L = \infty$ no current can flow into the load and hence no charge transferred onto C_h. All the error charge released during Phase 1 must thus flow to the signal source.

The Phase 2 contribution, which was solely due to the overlap capacitance, C_{ol}, can not be diverted to the signal source in this way, simply because the pass-transistor is now 'OFF' and no conducting path exists between the hold node and the signal source. The C_{ol} terminal on the hold node side is now effectively floating, and C_{ol} must thus retain its charge. At some point after the end of turn-off C_h will be 'reconnected' to the pass-transistor and the error charge stored on C_{ol} will be redistributed between C_{ol} and C_h. The final CLFT error on the circuit output, v_{out}, is therefore:

$$v_{out} = (V_{TH} - V_L)\frac{C_{ol}}{C_{ol} + C_h}$$

Eqn. 6-1

which, incidentally, is the same as the CLFT error under slow switching conditions.

6.1.2 Realistically achievable CLFT reduction.

A 'transient suppression device' (TSD) inserted in series with the hold capacitor C_h (see Fig. 6-1) can prevent fast transients (i.e. the error charge) from reaching C_h. How such a device can be realised is discussed later in section 6.1.3.

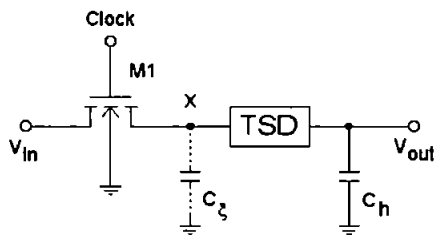


Fig. 6-1: The TSD technique.

In real circuits, especially in integrated circuits, there will always be a parasitic capacitance, C_ξ, associated with the intermediate node x between the switch and the TSD (see Fig. 6-1). This C_ξ ultimately limits the CLFT reduction achievable with this technique, since it acts as a hold capacitor during turn-off, while the actual C_h is effectively disconnected from the switch M1 by the TSD. The residual charge stored on C_ξ can be found from the CLFT equation of the single-lump model (Eqn. 2-7). The TSD will allow communication between node x and C_h after the Gate turn-off transient

has settled. The error charge stored on C_ξ will then be redistributed between C_ξ and C_h, and the final error voltage on the hold capacitance (the CLFT of the S&H with TSD) is:

$$CLFT_{TSD} = \frac{C_{ol} + C_\xi}{C_{ol} + C_\xi + C_h} CLFT_{SL}\left(C_{ol} + C_\xi\right)$$

Eqn. 6-2

where $CLFT_{SL}(C_{ol} + C_\xi)$ is the CLFT contribution predicted by the single-lump model (see Eqn. 2-7) for a hold capacitance of $C_{ol} + C_\xi$, and C_{ol} is the Gate overlap capacitance of the pass-transistor M1, which appears in parallel with C_ξ. C_{ol} may be neglected if $C_\xi \gg C_{ol}$.

6.1.2.1 Predicted improvement.

Fig. 6-2 to Fig. 6-7 show how much CLFT reduction can potentially be achieved with this 'TSD technique'. These plots were derived from calculations made for the basic S&H circuit (depicted in Fig. 2-1) and a TSD enhanced circuit, such as the one shown in Fig. 6-1. CLFT calculations were based on Eqn. 2-7 for the unmodified circuit and Eqn. 6-2 for the TSD enhanced circuit. The former was taken as reference against which the TSD improved circuit could be compared. For the purpose of these calculations it was assumed that the TSD disconnected the hold capacitor completely from the pass-transistor during turn-off. Two different calculations were performed. In the first one it was assumed that the total capacitance of the hold mode, C_L, was the same for both circuits (see Eqn. 6-3 and the corresponding plots Fig. 6-2, Fig. 6-4 and Fig. 6-5); in the second it was assumed that the parasitic C_ξ of the TSD was an additional capacitance, that had not been present in the unmodified circuit, and that the C_L of the TSD circuit increased to $C_L = C_h + C_\xi$, while C_L for the reference circuit was assumed unchanged at $C_L = C_h$ (Eqn. 6-4 with Fig. 6-3, Fig. 6-6 and Fig. 6-7).

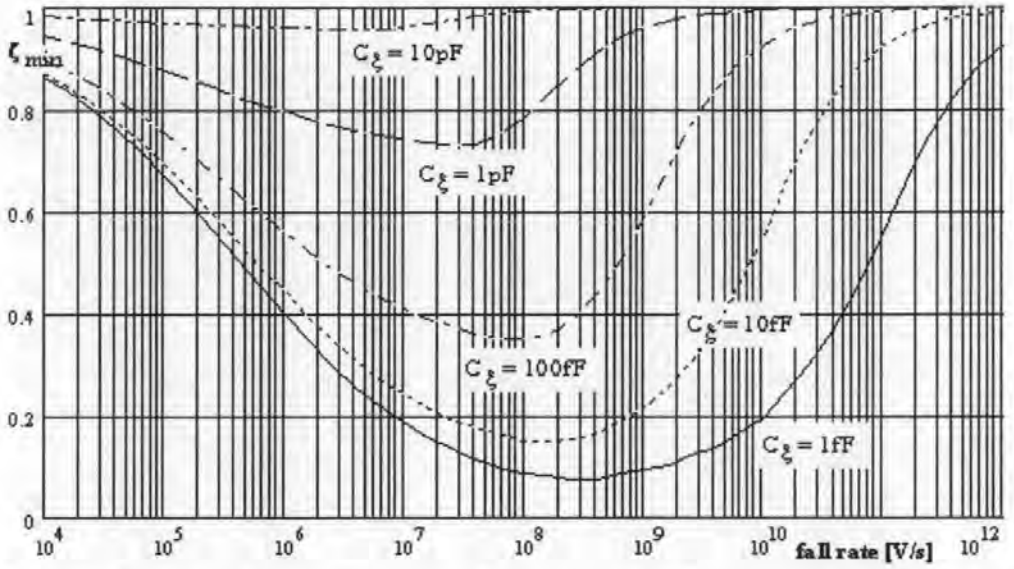


Fig. 6-2: Plot of CLFT reduction ζ_{min} versus fall rate, with C_ξ as parameter; C_h = 1.0pF, C_{ol} = 0.69fF and $C_L = C_h + C_\xi$ for both TSD circuit and reference circuit.

$$\xi_{min} = \frac{CLFT_{TSD}}{CLFT_{SL}(C_h + C_\xi)}$$

Eqn. 6-3

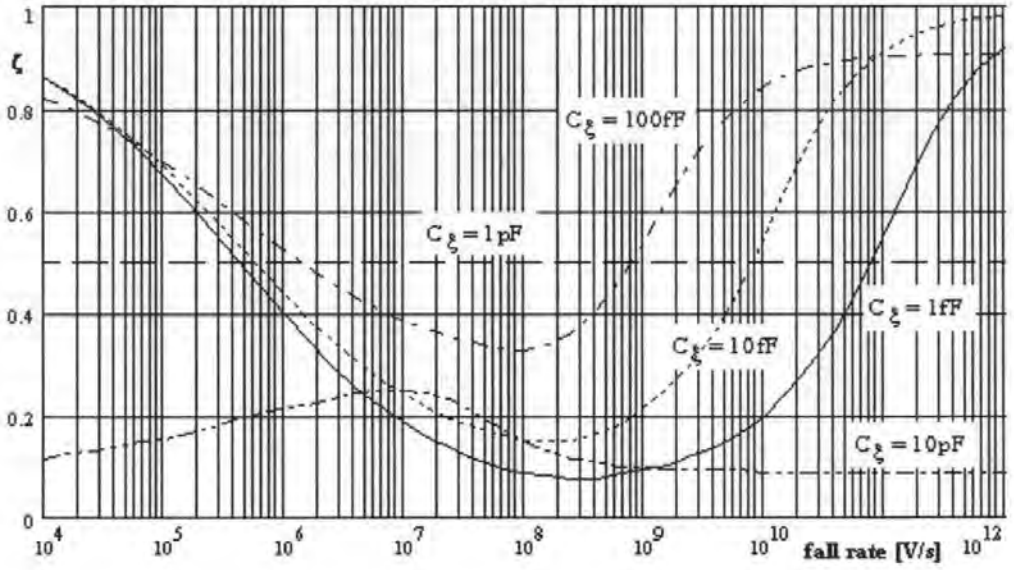


Fig. 6-3: Plot of CLFT reduction ζ versus fall rate, with C_ξ as parameter; C_h = 1.0pF, C_{ol} = 0.69fF, $C_L = C_h + C_\xi$ for TSD circuit and $C_L = C_h$ for the reference circuit.

$$\xi = \frac{CLFT_{TSD}}{CLFT_{SL}(C_h)}$$

Eqn. 6-4

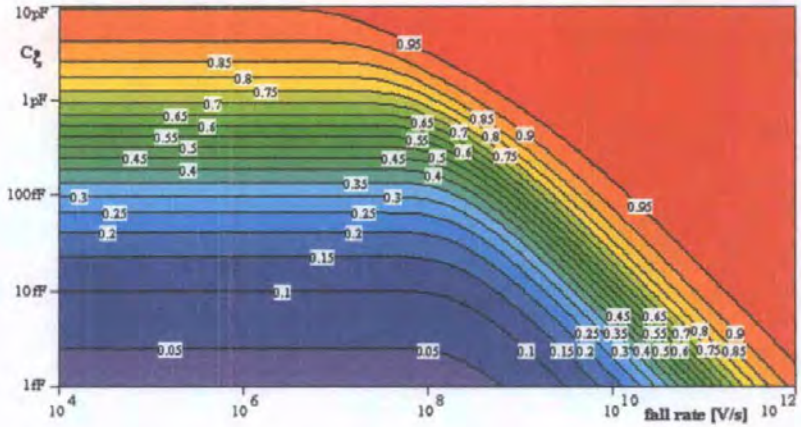


Fig. 6-4: CLFT reduction ζ_{min} over C_ξ and fall rate; C_h = 1.0pF, C_{ol} = 0 and $C_L = C_h + C_\xi$ for both TSD circuit and reference circuit.

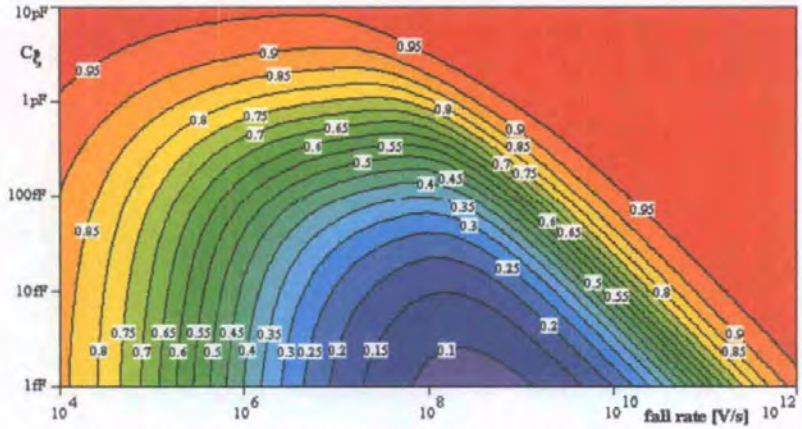


Fig. 6-5: CLFT reduction ζ_{min} over C_ξ and fall rate; C_h = 1.0pF, C_{ol} = 0.69fF and $C_L = C_h + C_\xi$ for both TSD circuit and reference circuit.

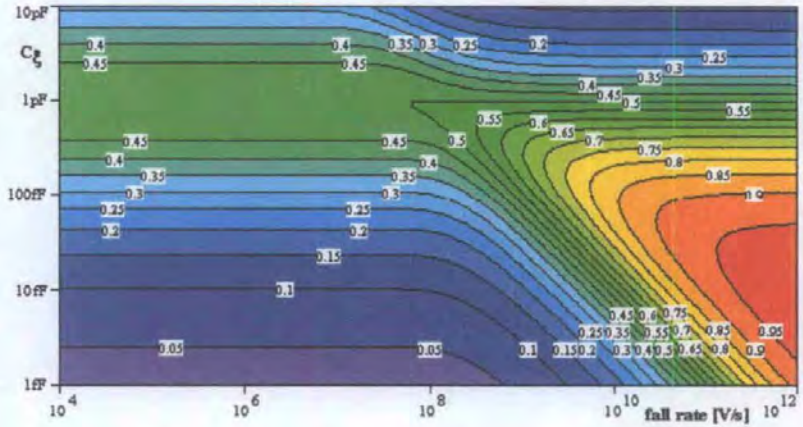


Fig. 6-6: CLFT reduction ζ over C_ξ and fall rate; C_h = 1.0pF, C_{ol} = 0, $C_L = C_h + C_\xi$ for TSD circuit and $C_L = C_h$ for the reference circuit.

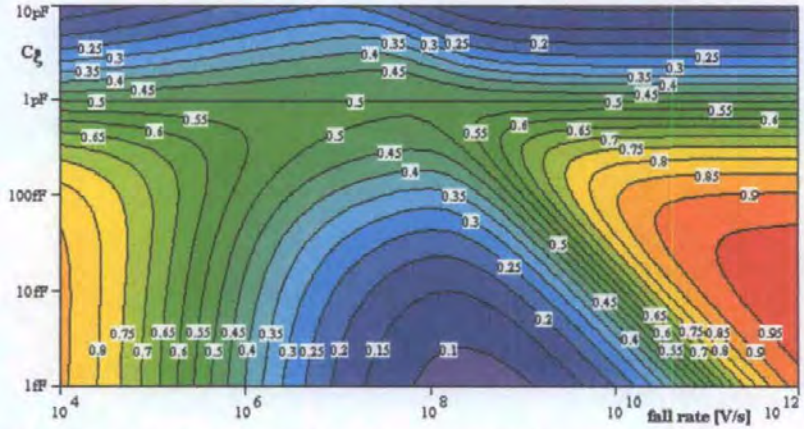


Fig. 6-7: CLFT reduction ζ over C_ξ and fall rate; C_h = 1.0pF, C_{ol} = 0.69fF, $C_L = C_h + C_\xi$ for TSD circuit and $C_L = C_h$ for the reference circuit.

From these plots it can be seen that the TSD improved circuit exhibits lower CLFT than the conventional circuit under most switching conditions, and that it never produces higher CLFT, which in itself is quite important.

Parameters for the calculations were:

C_h = 1pF, C_ξ = 1fF .. 10pF, C_{ol} = 0.69fF, C_{ox} = 6.5fF, β = 30μS, V_{T0} = 0.6V, V_H = 5V, V_L = 0V and V_{in} = 0V, corresponding to a MOS pass-transistor of size: L = 3.3μm, W = 4μm, L_D = 0.35μm, t_{ox} = 70nm.

For realistically achievable C_ξ (i.e. C_ξ between 10fF and 100fF), and with the overlap capacitance of the pass-transistor taken into account, CLFT levels of up to six times lower than in the basic S&H circuit were calculated (Fig. 6-2 and Fig. 6-5). With C_{ol} = 0 (i.e. for long pass-transistors, where C_{ox} is much greater than C_{ol}) the improvement was even greater: CLFT was more than an order of magnitude lower than for the unchanged circuit (Fig. 6-4). The greatest reductions were achieved in the medium fall-time region (which was between $\approx 10^7$ .. 10^9V/s for the S&H circuit given). This is not surprising, since the potential for increased error charge flow to the signal source is significantly less under both fast and slow switching conditions:

- For slow switching, the Phase 1 contribution to CLFT is already near zero ($CLFT_{Phase1} \approx 0$, see chapter 2.9.2.2 on slow turn-off), and thus can not be reduced much further.
- For fast switching, the time in Phase 1 of turn-off is so short that only insignificant amounts of charge can flow between the input and output of the S&H during that time ($q_{ds} \approx 0$, see chapter 2.9.2.1 on fast turn-off) — even very large ratios of C_ξ to C_h can not induce large enough q_{ds} to have a significant impact on CLFT.

Simulations in PSpice and experiments carried out on a test-chip (reported on later in chapter 7.3) showed that significant CLFT reductions can be achieved with this technique.

Some examples of possible TSD realisations are discussed in the sections following. The relative strengths and weaknesses of each circuit are explored and estimates for C_ξ developed. This figure for C_ξ may subsequently be applied to Eqn. 6-2 to arrive at an initial estimate for the CLFT reduction achievable (Eqn. 6-2 assumes negligible conduction in the TSD and may therefore be over-optimistic). More realistic predictions of CLFT reduction can be achieved using circuit simulators, as they include a greater number of parasitic effects in their calculations, such as forward biasing of junction diodes (which had not been considered in the simple model of Eqn. 6-2).

6.1.3 Transient suppression devices.

The first and foremost requirement for transient suppression devices (TSD) must be that they are suitable for integration in standard CMOS processes. Also they should be small and simple and have no adverse effects on the switched circuits performance. Besides these, rather obvious considerations, other conditions must be fulfilled for the TSD to work efficiently:

- the (transient) capacitance measured at node x must be smaller than the hold capacitance, preferably $C_\xi \ll C_h$. The smaller C_ξ is the more effective the circuit will be in suppressing the Phase 1 contribution to CLFT (see Eqn. 6-2). Ideally $C_\xi = 0$.
- the TSD must not let the error charge propagate to the output, or it must at least attenuate it significantly.
- the fall time of the switch's Gate voltage must not be shorter than its channel transit time, i.e. it may not enter diffusion mode during turn-off. This ensures that i_{ds} can redirect the Phase 1 contribution to CLFT to the signal source side.

6.1.3.1 RC low-pass load.

Low-pass circuits meet the basic requirement for a TSD i.e. they attenuate fast transients. However, many low-pass circuits are not well suited for integrated circuit technology, some because they are difficult to integrate on silicon (like LC structures), others because they require many components for their realisation. The RC low-pass (R-TSD), which can be realised by simply inserting an ohmic resistor between the pass-transistor and the hold capacitor (see Fig. 6-8), is well suited for integration, since ohmic resistors are readily available in most MOS processes.

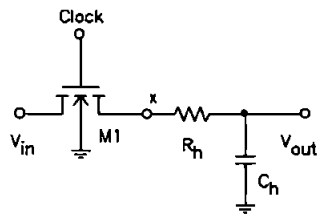
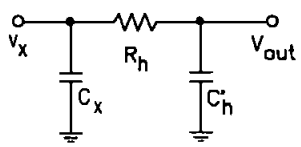


Fig. 6-8: RC load.



Small-signal equivalent circuit of the load in Fig. 6-8.

$$C'_h = C_h + C_{out}$$

$$C_\xi = C_x = C_{sb,M1} + C_R$$

$$\tau_h = R_h C'_h$$

Ohmic resistors of several tens of kΩ can be realised quite easily (without using too much silicon area), hence making time constants of several tens of ns easily achievable.

If, for example, the transistor switch in a S&H circuit is turned off in 1ns and the hold capacitance is 1pF, then a resistance R_h of 10kΩ is sufficient enough to reduce CLFT to a third of its former level, as shown in Fig. 6-10. Moreover, the plot also shows that the larger R_h, and thus the time constant τ_h compared to the fall time, t_f, of the clock signal is, the better the CLFT reduction is. Nevertheless, a total rejection of the error charge can not be achieved with the RC low-pass, because this would require R_h to be infinite. It can also be concluded that, whilst attenuating CLFT, the RC low-pass also causes the acquisition time of the circuit to increase.

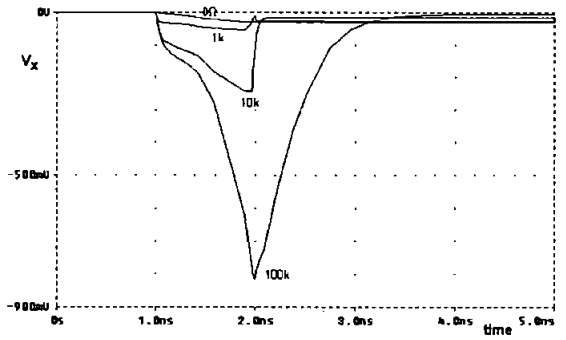


Fig. 6-9: PSpice simulation of v_x.

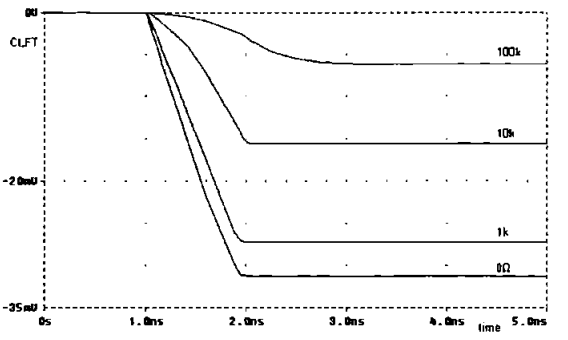


Fig. 6-10: PSpice simulation of CLFT.

These PSpice simulations were conducted on the circuit of Fig. 6-8 with device dimensions as follows:

$$W = 3.0\mu m,\ L = 3.0\mu m,\ L_D = 0.35\mu m,\ t_{ox} = 70nm,\ \beta = 24.75\mu S,\ V_{T0} = 0.6V,\ C_h = 1pF,$$

$$t_f = 1ns,\ 5V \geq V_G \geq 0V,\ V_{in} = 0V \text{ and with } R_h \text{ as parameter.}$$

The simulations clearly show the principle of operation of the TSD technique. With increasing load impedance the potential v_x (at node x) deviates, during turn-off, ever further from the hold potential (as shown in Fig. 6-9), thus increasing the conductive current in M1. This leads to less error charge reaching C_h, which results in lower CLFT (Fig. 6-10). Another advantage of the R-TSD technique is, that no spurious signals appear on the output as the pass-transistor is being turned off. This is in contrast to other circuits where glitches several times larger than the CLFT voltage may appear on the output.

6.1.3.2 MOS transistor TSD.

In the circuit presented below a MOS transistor, inserted between the pass-transistor and the hold capacitor, acts as the TSD. The circuit diagram (shown in Fig. 6-11) was drawn for t = 0+, the moment after the Gate voltage of the transistor M1 began to fall. At this point in time M1 already started extracting current from both the input and node x, resulting in v_x falling (V_{in} is assumed to be constant). As a consequence, node x assumes the lower potential of M2's two channel terminals, thus serving as its 'Source'. (If M2 were PMOS node x would become its 'Drain'). All transistor parameters in the equations below

are assumed to be associated with the TSD, M2, unless indicated otherwise by a M1 in the subscript; i.e. C_{ol} is the Gate overlap capacitance of M2, whereas $C_{ol,M1}$ is the overlap capacitance of M1.

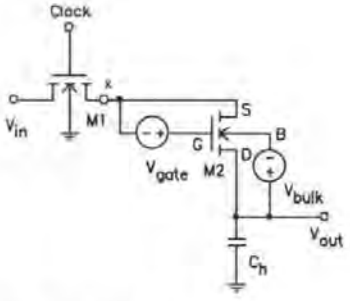
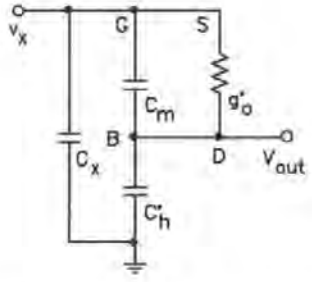


Fig. 6-11: MOSFET TSD.



Small-signal equivalent circuit of the load in Fig. 6-11.

$$C_m = C_{gd} + C_{gb} + C_{sb} + C_{sd} + C_{ol}$$

$$g'_o = g_o + g_{mb}$$

$$C_x = C_{ol,M1} + C_{sb,M1} + C_{Vgate}$$

$$C'_h = C_h + C_{out} + C_{well}$$

$$C_\xi = C_x + C'_h C_m / (C'_h + C_m)$$

and for $C'_h \gg C_m$:

$$C_\xi \cong C_x + C_m$$

Care must be taken to keep the parasitic capacitance C_ξ (at node x) as small as possible. The Bulk was consequently connected to the Drain rather than the Source, thus keeping the substantial Bulk to substrate capacitance, C_{well}, away from node x.

Due to the presence of C_m in parallel with the MOS TSD, the final error voltage on the hold capacitance can not be calculated using Eqn. 6-2. For this circuit, or indeed any other TSD circuit with a significant parasitic in parallel with the TSD, the final CLFT error is:

$$CLFT_{TSD} = CLFT_{SL}(C_\xi)\frac{C_\xi}{C_x + C_h'}$$

Eqn. 6-5

where $C_{ol,M1}$ is already included in C_x.

The main difficulty with this circuit is in keeping the transistor M2 biased into the strong inversion region under all possible operating conditions. External biasing with a floating voltage source V_{gate} (as shown in Fig. 6-11) is one, however, not the best, option available to realise this, as it results in higher CLFT due to the unavoidable increase of the parasitic C_x and thus C_ξ. Alternatively, either depletion or floating gate MOSFETs could be used for

M2 thus avoiding the need for external biasing altogether and consequently maintaining C_ξ small.

A consequence of the particular arrangement (Fig. 6-11) was that, for the case of V_{bulk} being zero, V_{BS} was positive and equal to V_{DS}. This meant that during turn-off and when discharging C_h the parasitic Bulk to Source diode was biased in the forward direction. For sufficiently high V_{DS} (in excess of the built-in junction potential) this diode may start to conduct and thus limiting the CLFT reduction that is achievable.

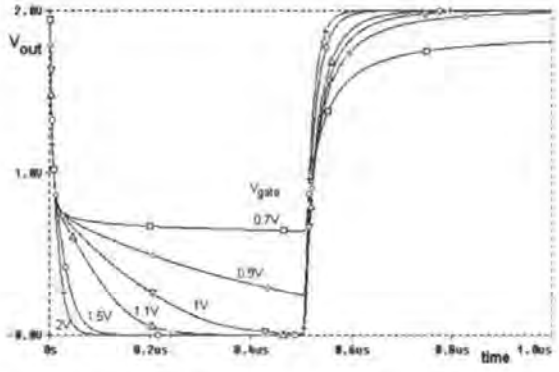


Fig. 6-12: Simulated transient response.

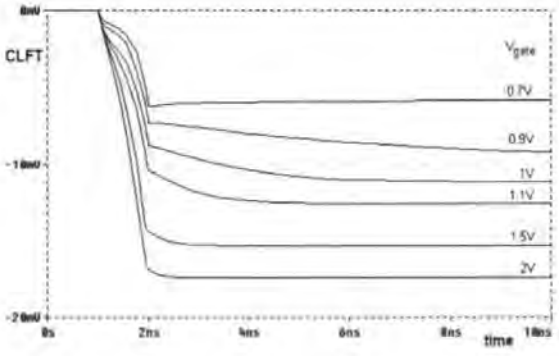


Fig. 6-13: PSpice simulation of CLFT.

The above PSpice simulations were conducted on the circuit of Fig. 6-11. Circuit parameters were the same as in the R-TSD simulation:

$$W = 3.0\mu m,\ L = 3.0\mu m,\ L_D = 0.35\mu m,\ t_{ox} = 70nm,\ \beta = 24.75\mu S,\ V_{T0} = 0.6V,\ C_h = 1pF,$$

$$t_f = 1ns,\ 5V \geq V_G \geq 0V,\ V_{bulk} = 0V \text{ and with } V_{gate} \text{ as parameter.}$$

In the simulation of Fig. 6-12 a square-wave input signal of 1MHz switching between 0V and 2V was applied and for Fig. 6-13 the input voltage V_{in} was 0V.

The graph Fig. 6-13 shows that with V_{gate} decreasing, i.e. increasing channel resistance, CLFT decreases. At V_{gate} = 1.5V the CLFT is reduced by 50% (compared to the CLFT for $R_h = 0\Omega$ in Fig. 6-10); and for V_{gate} a little less than 1V CLFT is reduced by two thirds.

As was the case with the R-TSD, the MOS transistor TSD also affects the acquisition time of the S&H circuit adversely, i.e. makes it longer. This effect is clearly visible in Fig. 6-12, where for V_{gate} = 1.5V the output takes less than 200ns to follow a 2V step change of the input signal. With V_{gate} = 1.0V the same action requires more than 500ns to complete.

6.1.3.3 Bottom-plate MOS transistor TSD.

In the circuit presented in Fig. 6-14, below, the MOS transistor TSD was inserted between the bottom-plate of the hold capacitor and ground (GND). This arrangement is particularly suitable for realisation in standard CMOS processes, where depletion devices or floating gate MOS transistors, are not always available.

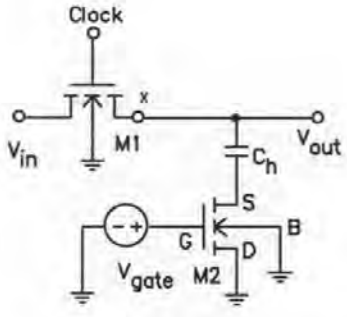
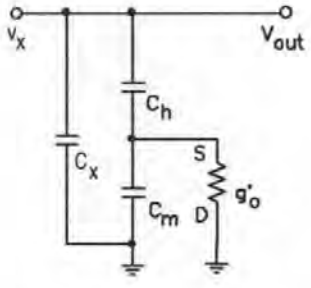


Fig. 6-14: Alternative FET TSD arrangement.



Small-signal equivalent circuit of the load in Fig. 6-14.

$C_m = C_{bb} + C_{sd} + C_{sb} + C_{sg} + C_{ol}$

C_{bb} = bottom-plate capacitance of C_h.

$g'_o = g_o + g_{mb}$

$C_x = C_{ol,M1} + C_{sb,M1} + C_{out}$

$C_\xi = C_x + C_h C_m / (C_h + C_m)$

for $C_h \gg C_m$:

$C_\xi \cong C_x + C_m$

The circuit diagram, was drawn for t = 0+, immediately after the Gate voltage of the transistor M1 began to fall. At this point, M1 already started extracting current from both the input and node x, resulting in v_x falling (V_{in} was assumed to be constant). The side of M2 that was connected to C_h will therefore become the transistor's Source during turn-off.

CLFT error for this circuit is:

$$CLFT_{TSD} = CLFT_{SL}(C_\xi)\frac{C_\xi}{C_x + C_h}$$

Eqn. 6-6

where $C_{ol,M1}$ (the overlap capacitance of M1) had been included in C_x.

For circuits in which C_{hb} and C_h are dominant ($C_x \approx 0$ and $C_m \cong C_{hb}$) the following approximation may be used instead:

$$CLFT_{TSD} = \frac{C_{hb}}{C_h + C_{hb}} CLFT_{SL}\left(\frac{C_h C_{hb}}{C_h + C_{hb}}\right)$$

Eqn. 6-7

A consequence of this particular arrangement (Fig. 6-14) is that V_{BS} of M2 will be positive and equal to its V_{DS} during turn-off. The parasitic Bulk to Source diode of M2 therefore gets biased in the forward direction and may, for sufficiently high V_{DS}, start to conduct, thus limiting the CLFT reduction that is achievable.

C_{hb}, the bottom-plate capacitance of C_h, presents another limiting factor to the CLFT reduction available with this arrangement, as this can very easily become the biggest parasitic contributing to C_ξ. This is particularly true for circuits with large C_h, as C_{hb} is often between 3% and 30% of C_h. Any capacitive loading on the output, C_{out}, such as the input capacitance of a following buffer amplifier can have a similar effect on C_ξ.

A further potential disadvantage is that the output voltage of the circuit exhibits a, potentially large, CLFT induced transient excursion during turn-off, similar to the one observed on the internal node x of the R-TSD (see Fig. 6-9). The worst-case magnitude of this transient can be estimated using Eqn. 6-1, where C_h is replaced by C_ξ and C_{ol} is that of the pass-transistor M1. It may reach several tenths of volt, but must not become so large that the Bulk to Source diode of M2 starts conducting in the forward direction ($V_{BS,M2} > V_F$), or the TSD will effectively be bypassed by this diode and thus limited in performance. The reduction in CLFT achieved by the circuit will then be limited by V_F.

However, the big advantage of the circuit is, that it is realisable on any MOS process, and that very large load impedances can be achieved using only a very small silicon area (M2

could be a minimum feature size device). In fact a technique similar to this is used in the so-called bottom-plate sampling, a multi-phase clocking scheme where M2 is simply being turned off before M1; see item 2.a) of chapter 5.1.1 and references [36], [37] on the use of multi-phase clocks in SC circuits.

A TSD circuit similar to this one was realised on the test chip, the results of which are presented in chapter 7.3. The measurements were found to be in good agreement with predictions made using Eqn. 6-2.

6.1.4 Summary of CLFT reduction circuits using TSDs.

TSDs work by increasing the impedance of the hold node. Because of this more of the error charge will get diverted to the, lower impedance, signal source side of the circuit and CLFT will thus be reduced. For the TSD to be effective $C_h \gg C_\xi$ is essential. Also important is that the impedance of the TSD is high during turn-off; ideally this should be infinite (i.e. present an open circuit) during turn-off.

A TSD may be placed either between the pass-transistor and the hold capacitor or between the bottom-plate of the hold capacitor and its reference potential, which is often ground (GND). Large excursions on V_{out} should be expected during turn-off if the TSD is placed between C_h and GND and V_{out} is taken from the top plate of C_h (such as in Fig. 6-14). With the TSD between the pass-transistor and C_h (as in Fig. 6-8 and Fig. 6-11) these excursions will be absorbed by the TSD and will not reach the output of the circuit. Another issue with placing the TSD any place other than directly after the output of the pass-transistor is that this may lead to an increase in the parasitic capacitance C_ξ at its output, and, therefore, reduced efficiency of the TSD (see sections 6.1.2, 6.1.3.2 and 6.1.3.3).

MOS transistors may be used as TSD. They allow realisation of large impedances using only very little silicon area. Small area also means that only a small additional parasitic

capacitance will be introduced to the circuit by the TSD. This can help maximise the CLFT reduction achievable with TSDs. One limitation of circuits using transistors as TSDs is, that the transient deviation of V_x must not be so large that the Bulk to Source diode of the TSD starts conducting in the forward direction ($V_{BS} > V_F$), or the TSD will effectively be bypassed by this diode and thus limited in performance.

6.2 A S&H circuit with linearised CLFT.

A S&H circuit with much reduced levels of signal distortion is presented. In this circuit the variation in CLFT is linearly related to the input signal. This is in contrast to the conventional approach to CLFT control, where the main goal is to achieve a reduction in the size of the CLFT error. A reduction in the signal dependent distortion caused by CLFT is often no more than just a welcome by-product of the CLFT's magnitude reduction.

Here, the objective was to find a S&H circuit that exhibited reduced levels of signal distortion arising from CLFT. It was decided that the best way to achieve this was by devising a circuit that in some way 'linearised' CLFT, i.e. made CLFT linearly related to the input signal. Such a 'linearised' CLFT will not introduce any error to the held signal, other than gain and DC-offset errors, which do not give rise to harmonic distortion and can easily be eliminated via offset and gain adjustments.

In the following sections a switching scheme based on this approach is presented, and the resulting CLFT performance is contrasted with those for the basic S&H circuit and the dummy compensated S&H circuit. Simulation shows, that the scheme can reduce THD by more than two orders of magnitude compared to the uncompensated S&H circuit. Results from measurements on test silicon (see chapter 7.4) showed good agreement between predictions and actual circuit performance.

6.2.1 Proposed CLFT linearisation strategy.

The proposed strategy aims to make CLFT vary linearly with the applied signal level. This is achieved by controlling the switches' Gate voltage V_G during the "ON" state, such that its mobile channel charge, and thus its "ON" resistance R_{ON}, is kept constant and independent on V_{in}. This control of the channel charge is accomplished by maintaining the Gate overdrive (i.e. $V_{HT} = V_{GS} - V_T$) for a turned on switch constant, irrespective of any

changes in V_{in}. Where this can be achieved both the fraction of the mobile channel charge exiting from the transistor to the hold node, and the quantity of charge conducted during turn-off, will be constant (assuming that the terminal impedances seen by the transistor are not themselves signal dependent).

The switch is turned off by reducing the Gate-Bulk potential to zero. This method gives maximum signal handling capability, and ensures that the switch stays "OFF" for any permissible input signal. However, it does introduce a signal dependent component to CLFT, through the charge coupled onto the hold capacitance C_h via the pass-transistor's overlap capacitance C_{ol}. This component is identical to the "OFF-region" contribution to CLFT in the basic S&H circuit (see chapter 2.1, Eqn. 2-6). Thus, CLFT of the proposed circuit will exhibit a residual signal dependency that is proportional to the ratio of C_{ol} to C_h. Earlier in chapter 4 it was shown that such a scheme can significantly reduce the non-linear signal-dependency of the Phase 1 contribution to CLFT.

6.2.2 Suggested circuit implementation of the CLFT linearisation strategy.

The proposed linearisation strategy can be implemented as shown in Fig. 6-15c. In sampling mode the Gate overdrive of this circuit, $V_{HT} = V_{GS} + V_T$, is independent of V_{in} and proportional to I_{bias}. Provided that I_{bias} is fixed it follows that V_{HT} will also be constant.

Following the approach presented in chapter 2.1, estimates for the CLFT of the proposed circuit can be found as:

$$CLFT = v_1 + v_2$$

Eqn. 6-8

where

$$v_1 = -\sqrt{\frac{\pi U C_h}{2\beta_1}}\,\frac{C_{ol1} + \frac{C_{ox1}}{2}}{C_h}\,\mathrm{erf}\left[\sqrt{\frac{\beta_1}{2UC_h}}\left(V_{T2} - V_{T1} + \sqrt{\frac{2I_{bias}}{\beta_2}}\right)\right]$$

Eqn. 6-9

is the contribution to CLFT while $V_{GS1} \geq V_{T1}$ and

$$v_2 = -\frac{C_{ol1}}{C_h}(V_{in} + V_{T1})$$

Eqn. 6-10

is the pass-transistor's contribution for $V_{GS1} < V_{T1}$. The integer numbers in the subscripts identify the transistor to which a parameter refers to (e.g. C_{ol1} is the Gate-to-Drain overlap capacitance of the pass-transistor M1).

The threshold voltage of transistors M1 and M2 can, to first order approximation, be expressed as (see Eqn. 1-12, chapter 1.3.2):

$$V_T = V_{T0} + \gamma\left(\sqrt{2\varphi_F + V_{in}} - \sqrt{2\varphi_F}\right)$$

which implies that both V_{T1} and V_{T2}, are the only non-linearly signal dependent terms in Eqn. 6-9 and Eqn. 6-10. It may be appreciated that Eqn. 6-9 becomes independent of V_{in} if $V_{T1} = V_{T2}$, which, for equal-sized, matched transistors M1 and M2, is the case*. For matched transistors $\beta_1 = \beta_2$ also applies and CLFT for the proposed circuit will then be:

$$CLFT = -\sqrt{\frac{\pi UC_h}{2\beta_1}}\frac{C_{ol1} + \frac{C_{ox1}}{2}}{C_h}\,\mathrm{erf}\left(\sqrt{\frac{I_{bias}}{UC_h}}\right) - \frac{C_{ol1}}{C_h}(V_{in} + V_{T1})$$

Eqn. 6-11

The single largest contributing element to CLFT (the channel charge contribution) has now been reduced to a constant level, and therefore, no longer gives rise to distortion. The only signal dependent terms left are V_{T1} and V_{in} of which the, linear, V_{in} term will clearly be the dominant term, i.e. the one with the stronger signal dependency. Nevertheless, V_{T1} will

---

* In the proposed circuit only the currents through, and therefore the V_{DS} across, M1 and M2 differ ($V_{DS1} \approx 0V$, $V_{DS2} \approx 2V$). This, according to the SPICE Level 2 model for the threshold voltage [5], [31] results in a slightly lower V_{T2} than V_{T1}, which results in a slightly lower CLFT. The effect, however, is negligibly small.

introduce a small non-linear component to the residual CLFT. This could be avoided by coupling the switching transistors' Bulk potential to the input voltage and realising a constant Gate voltage swing as in [35] and [57]. However, the resulting circuits are much more complex and suffer from reduced signal handling capability.

6.2.3 Simulation results.

Three circuits have been simulated: the basic S&H circuit without compensation (Fig. 6-15a), the dummy compensated S&H circuit of Fig. 6-15b and the linearised S&H circuit of Fig. 6-15c, which is based on the proposed technique.

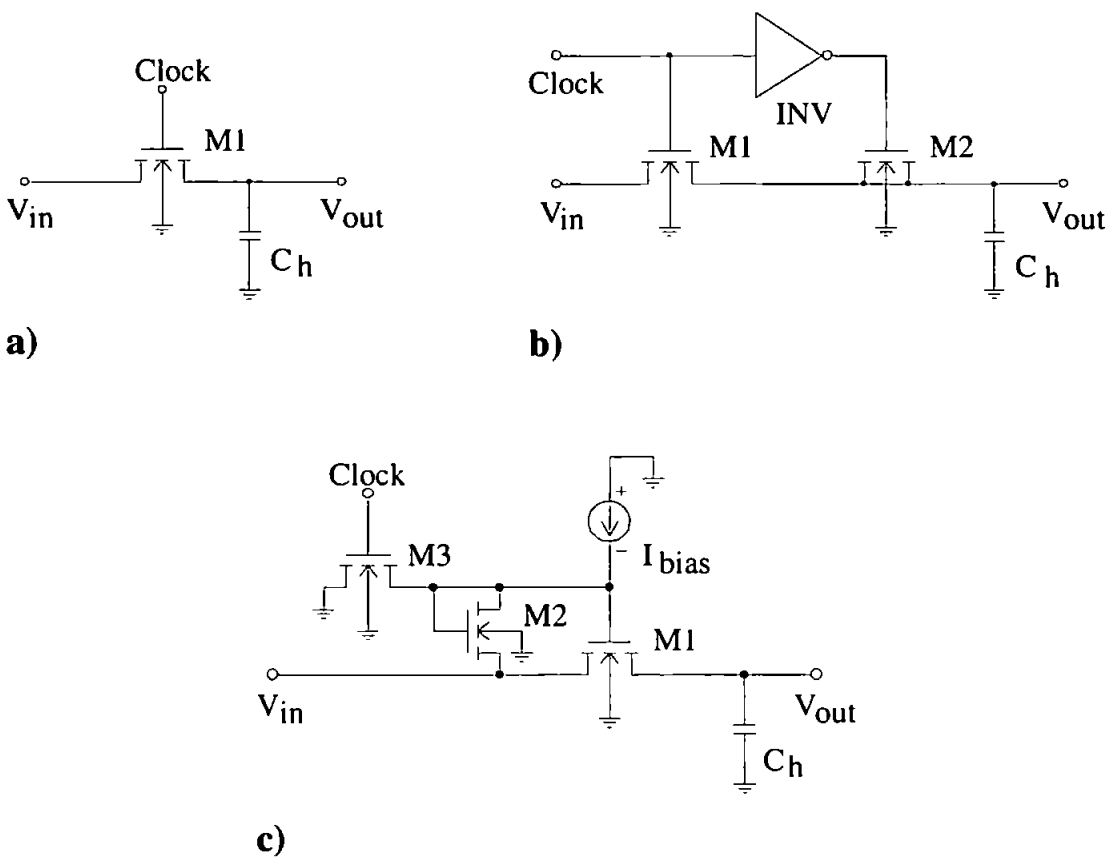


Fig. 6-15: S&H circuits compared:

a) basic, uncompensated circuit;

b) dummy compensated circuit;

c) proposed CLFT linearised S&H circuit.

Simulations have been performed using the PSpice Level 3 model for the MIETEC 2μm process. Circuit parameters were:

$$V_{T0} = 0.86V, \gamma = 0.26V^{0.5}, \mu = 611.4cm^2/Vs, \varphi_F = 0.31V, t_{ox} = 40.3nm, L_D = 0.22\mu m,$$

$$C_h = 1pF, V_H = 5V, V_L = 0V, U = 10^9V/s, I_{bias} = 17\mu A \text{ and } V_{in} = 0V \text{ .. } 3V.$$

All transistors were W = 4.8μm by L = 2.4μm, except for the half-width dummy (M2, Fig. 6-15b) which was a minimum feature size device, i.e. W = 2.4μm and L = 2.4μm. All clocks had constant fall-rates, U, and complementary clocks were used in the simulation of the dummy compensated circuit. The results of these simulations are reproduced in the figure below.

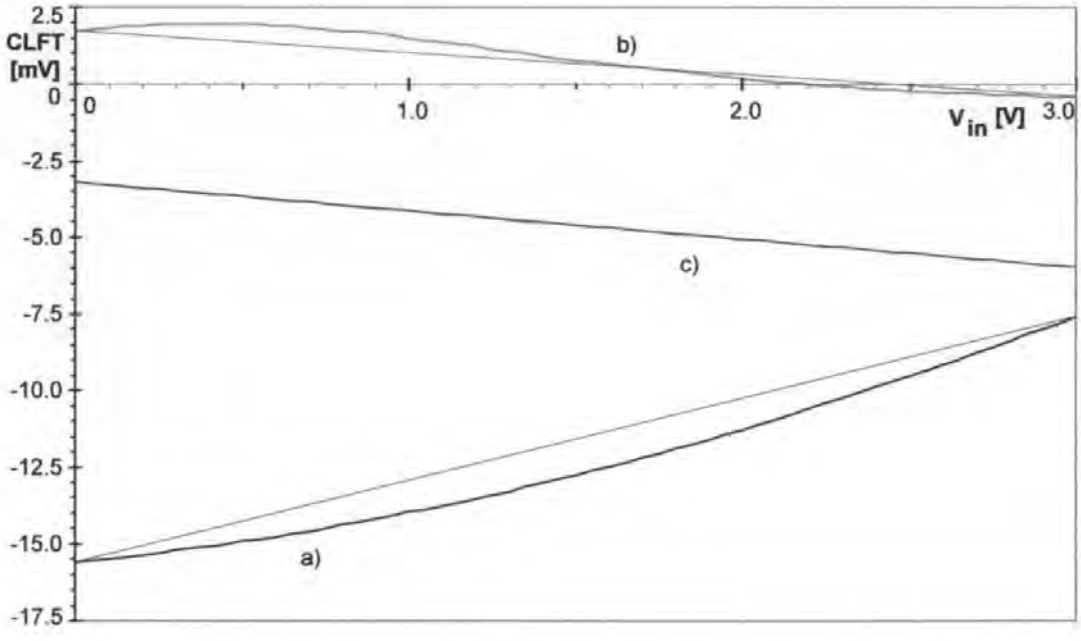


Fig. 6-16: Simulation results for CLFT versus signal level, with a DC input signal.

a): CLFT for circuit Fig. 6-15a)

b): CLFT for circuit Fig. 6-15b)

c): CLFT for circuit Fig. 6-16c).

For the uncompensated circuit, CLFT was found to vary between a minimum of -15.6mV at V_{in} = 0V and a maximum of -7.6mV at V_{in} = 3V whilst for the dummy compensated circuit the CLFT maximum was +2.0mV at V_{in} = 0.4V and minimum -0.4mV at V_{in} = 3V.

For the proposed structure CLFT ranged from -3.2mV at V_{in} = 0V to -6.0mV at V_{in} = 3V. In comparison with the performance of the uncompensated S&H circuit, dummy compensation reduced the absolute variation of CLFT by a factor of 3.3, whereas the proposed scheme gave a 2.9 fold improvement.

As previously noted, we are not so much concerned with the CLFT absolute values, but rather the non-linear variations in CLFT. The end-point straight line approximations included in Fig. 6-16 (the dotted lines drawn between the end-points of each graph) show that the proposed scheme virtually eliminates such variations, therefore, greatly improves the performance over the uncompensated and the dummy compensated S&H circuits. To support this observation the total harmonic distortion (THD), introduced by these S&H circuits, was examined. For this the sampling of a full-scale 1kHz sine-wave signal (i.e. with 1.5V amplitude and +1.5V offset) at a sampling rate of 64kS/s was simulated. The levels of THD and the corresponding harmonics found are listed in Table 6-1 below.

Harmonic No.	Uncompensated circuit Fig. 6-15a)	Dummy compensated circuit Fig. 6-15b)	Proposed circuit Fig. 6-15c)	Calculated for the proposed circuit using Eqns. 1-4 to 1-6 and Eqn. 6-11
2	-68dB	-86dB	-111dB	-101dB
3	-98dB	-76dB	-126dB	-115dB
4	-106dB	-86dB	-136dB	-127dB
5	-121dB	-104dB	-142dB	-138dB
THD	-68dB	-74dB	-110dB	-101dB

Table 6-1: Simulation results for THD and harmonics on a full-scale 1kHz sine-wave signal, sampled at 64kS/s.

The reduction in THD was more than two orders of magnitude over the uncompensated circuit, and more than a factor of 60 over the dummy compensated circuit. The agreement between simulation and mathematical description (Eqn. 6-11) of the proposed scheme is

reasonable. The 9dB difference between the two (see Table 6-1) is not a serious concern since it appears at very low levels of THD, and may simply have been the result of modelling tolerances: the calculation and simulation did not employ the same transistor models (the simulation utilised a SPICE Level 3 model and the calculation employed a SPICE Level 1 model).

It should be noted that, according to Eqn. 6-11, the signal dependent component of CLFT for the proposed scheme, and therefore its contribution to THD, is independent of the clock fall-rate. Other advantages of the proposed circuit include a reduction in aperture jitter, a benefit that derives from the independence of V_{HT} on V_{in}: if the fall rate, U, of V_{G1} is constant then the time spent in the "ON" region during turn-off will be constant i.e. the aperture delay will be constant). Furthermore, only a single clock signal is needed (the dummy compensation scheme requires two clock inputs), and minimum feature size devices can be used throughout. This reduces CLFT, and possibly area consumption (the dummy compensation also requires that the switching device is approximately twice as wide as the dummy device). It will be appreciated that, if the circuit was implemented as suggested the signal source must sink I_{bias}, which may not always be acceptable. Variations of this circuit in which the signal source does not have to sink I_{bias} can be realised easily. An example of such a circuit is shown below:

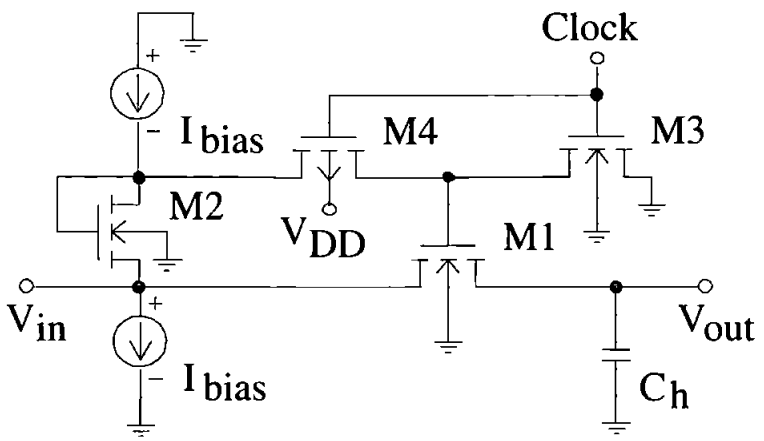


Fig. 6-17: Example of a CLFT linearised S&H circuit with reduced DC loading of the signal source.

6.2.4 Summary and conclusions for the S&H circuit with linearised CLFT.

It has been shown that the detrimental effects of the CLFT's non-linear signal dependency on SC circuits can be greatly reduced by maintaining the pass-transistor's channel charge constant, i.e. making its "ON" resistance independent of its Source potential.

A simple circuit that significantly reduces distortion introduced by the sampling process has been presented. The proposed scheme's CLFT exhibits a near linear signal dependency that can be described in terms of a DC offset and a gain error, both of which could be compensated for in either pre-processing or post-processing, if deemed necessary (e.g. with auto-zero and automated gain control facilities). This signal dependent component of CLFT was, to first order approximation, found to be independent of the clock fall-rate. Simulation in PSpice indicate that the simple analytical model (Eqn. 6-11) adequately predicts the CLFT, and CLFT induced distortion, of the proposed circuit. This was also confirmed by measurements on test silicon, the results of which are reported later in chapter 7.4).

Other benefits are that the proposed circuit's aperture delay is independent of V_{in} (assuming a constant fall rate U of V_{GI} the time spent in the "ON" region during turn-off must be constant since V_{HT} is constant) and that its aperture jitter should also be reduced (a benefit that derives from the independence of V_{HT} on V_{in}; see chapter 1.4.3). Furthermore, the circuit uses only one type of transistor and does not require separate wells, making it suitable for any MOS technology.

7. Measurement results from the test chip.

Measurement results from a custom IC, realised on the AMS 0.8μm mixed-signal CMOS process, are presented. These are compared to results from PSpice transient simulations, which employed a BSIM3v2 transistor model, and CLFT calculations which employed the circuit-relevant analytical models presented in this thesis. Reasonable agreement between measurements, calculations and simulations is shown. The PSpice simulations using the BSIM3v2 model tended to track observed behaviour more closely than the CLFT calculations, which used the less sophisticated SPICE Level 1 model parameters.

Results from three different S&H configurations are being reported in this chapter: the basic S&H, the linearised S&H (which was presented in chapter 6.2) and S&H circuits that employ BP-TSD (see chapter 6.1.3.3).

The results from the basic S&H circuit show the predictions about the CLFT induced distortion made in chapter 4 to be valid.

Results from the linearised S&H indicate that this circuit can reduce CLFT induced distortion significantly. It was found that INL $\equiv$ 0 could be achieved for specific clock fall-rates, U. This result was anticipated by the PSpice simulations, but not by the analytical model (Eqn. 6-11) which predicted INL of the linearised circuit to be independent of U.

The evaluation of the S&H with BP-TSD showed the circuit to perform as expected. The CLFT reduction achieved was close to predictions from both PSpice simulations and the analytical model (Eqn. 6-7). Compared to PSpice simulations, the analytical model was found to consistently overestimate the maximum level of CLFT reduction that could be achieved with the BP-TSD. This could be attributed to the saturation mode contribution to CLFT (see chapter 3), which had not been considered in the analytical models for CLFT.

7.1 Description of the test-chip and measurement setup.

The test-chip was manufactured through the EUROPRACTICE program. It was realised on the AMS CYE process, a twin-well 0.8μm mixed-signal CMOS process (see Appendix E for process specifications) on p-epi substrate. The floorplan and the pin-assignment of the test-chip have been included in Appendix F, and detailed schematic diagrams for the IC can be found in Appendix G.

The test-chip expected the S&H input voltage, V_{in}, and the bias current for the linearised S&H, I_{bias}, to be supplied from external sources. The clock signal could come from either external or an on-chip ramp generator. The external clock generator used could provide clock signals with constant fall-rates of between 333MV/s and 325kV/s. The fall-rate of the on-chip ramp generator was programmed by an external current, I_{clk}. The higher this current the higher the fall-rate was. With this internal ramp generator fall-rates of between an estimated 31GV/s and 1.3MV/s could be produced. Fall-rates up to 1.5GV/s were verified by measurements (fall-rates greater than about 1.5GV/s could not be verified due to bandwidth limitations of the equipment used).

The output voltage from the S&H circuits was buffered and level shifted using PMOS source followers and single-stage operational amplifiers in unity gain configuration before bringing the signal off-chip.

For each of the S&H circuits investigated three combinations of pass-transistor size and hold capacitor size were realised on the test-chip, with a view that the maximum CLFT of each of the circuits would be in the region of 30mV to 40mV (the maximum value of CLFT was chosen as the main design criteria for the S&H circuits due to accuracy considerations and limitations of the available measuring equipment):

1. Minimum size transistor: $W_{drawn} = 2.0\mu m$, $L_{drawn} = 0.8\mu m$ and $C_h = 0.1pF$.

2. Long and narrow transistor: W_{drawn} = 2.0μm, L_{drawn} = 8.15μm and C_h = 15×0.1pF except for the linearised S&H where C_h = 2×0.1pF.
3. Large, square transistor: W_{drawn} = 8.8μm, L_{drawn} = 8.15μm and C_h = 80×0.1pF except for the linearised S&H where C_h = 24×0.1pF.

Batch characterisation data provided by the foundry showed that the actual test silicon was close to typical (see Appendix E). Thus all PSpice simulations results presented in this chapter were derived from the, foundry supplied, BSIM3v2 model for typical, and all analytical model calculations employed the following transistor parameters, again derived from typical: V_{T0} = 0.844V, γ = 0.6749$V^{-0.5}$, φ_F = 0.3956V, V_L = V_B = 0V and V_H = 5V. The remaining parameters, which vary with transistor size, are listed below:

1. For a minimum size transistor: W = 1.2μm, L = 0.66μm, β = 181.1μA/V^2, C_{ox} = 1.708fF and C_{ol} = 0.694fF.
2. For a long and narrow device: W = 1.2μm, L = 8.0μm, β = 14.92μA/V^2, C_{ox} = 20.73fF and C_{ol} = 0.694fF.
3. For a large, square transistor: W = 8.0μm, L = 8.0μm, β = 99.5μA/V^2, C_{ox} = 138.2fF and C_{ol} = 3.055fF.

The parasitic extraction tool in the Mentor Graphics design suite, that was used for the layout of the test-chip, did not work at the time. Back-annotation of layout parasitics into the circuit designs thus could not be performed. Manual estimates of the bottom-plate capacitance were used instead in the assessment of the BP-TSD. For all other circuits the parasitics were assumed negligibly small.

Some error in the absolute levels of CLFT derived from PSpice simulation and calculations can therefore be expected when comparing these to measured data. In circuits using small devices these discrepancies will be worse than in circuits using large devices; because

processing variations and parasitics are disproportionately larger for small geometries than for large geometries (e.g. a change in gate length of 0.1μm represents a variation of 12.5% for a 0.8μm long device, whereas it presents only a 1.25% variation for a 8μm long device). For this reason most results presented in this chapter will be from circuits using large geometry pass-transistors.

7.1.1 The test-rig.

A circuit specific test-rig was designed and built for evaluating the test-chip. This test-rig consisted of supply regulators, voltage references, 16-bit D/A converters, buffer amplifiers and voltage to current converters. These provided power, the DC input voltage for evaluating the S&H circuits, V_{in}, and the bias currents for the test-chip. The test-rig also provided high-speed buffer amplifiers and 16-bit A/D converters for buffering and measuring the test-chip's S&H output signals. Opto-couplers and some control circuitry facilitated interfacing of the test-rig to a PC, which controlled the measurements and stored the raw data for further processing. The circuit diagrams of this test-rig may be found in Appendix H and a brief description of the setup is included in Appendix I.

The test-rig could provide V_{in} between -0.1V and 4.9V, which could be increased in steps of 76.3μV. The LSB size of the test-rig's A/D converters, used for measuring the S&H output voltage, was 62.5μV. INL of these A/D converters was specified at $< \pm 0.004\%$ of full-scale range (by the manufacturer), corresponding to an INL of $< \pm 164\mu V$.

The external clock source employed was capable of producing clock signals with constant fall-rates of between 333MV/s and 325kV/s. The clock high voltage was $V_H = 5.0V$ and the clock low voltage was $V_L = 0V$.

7.1.2 The CLFT measurements.

Only DC input voltages were applied to the test-chip. S&H output voltages were measured both just before the sample to hold transition and after it. Each measurement was averaged over 8 consecutive A/D conversions, and 11 sample-to-hold transitions were performed for each test point (i.e. for a particular setting of U, V_{in} and I_{bias} if applicable). Data was collected from 9 ICs and averaged. Each testpoint consisted therefore of the averaged results from a total of 792 A/D conversions.

Taking two sets of measurements for each sample-to-hold transition, one just prior to the transition and one immediately after it, makes it possible to calculate two separate transfer characteristics for each S&H: one for the sample mode, or track mode, and one for the hold mode. Non-linearities introduced by circuit elements common to both measurements such as the S&H output buffer amplifiers and A/D converters will affect both transfer characteristics in the same way. In fact, the only difference between the two transfer characteristics arises from the CLFT error. Therefore finding CLFT could not be easier: it simply is the difference between the circuit's output voltage in track mode and its output voltage in hold mode. This difference needs to be corrected for any gain error in the signal path (which can be found from the track mode transfer characteristic) to arrive at the true value for CLFT.

7.2 Evaluation of the basic S&H circuits.

The measured INL and CLFT data from two basic S&H circuits is presented. These two circuits differ only in the size of the pass-transistors and hold capacitors they employ.

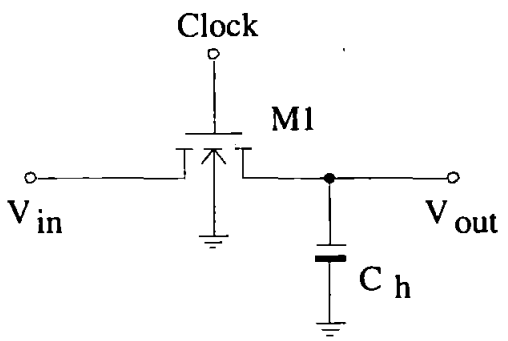
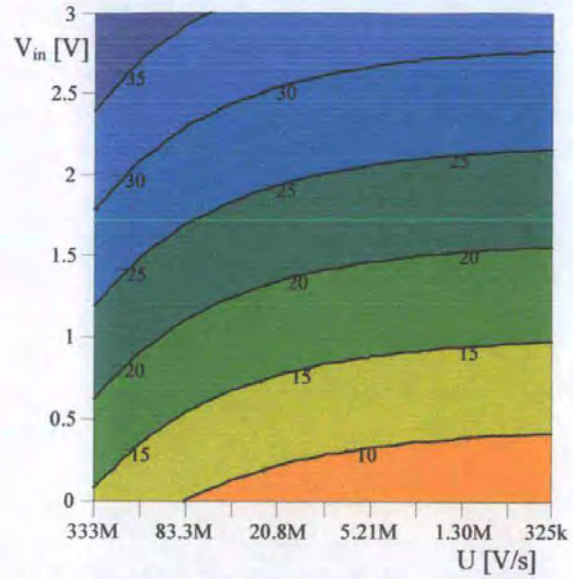


Fig. 7-1: Schematic for the test-chip's basic S&H circuits.

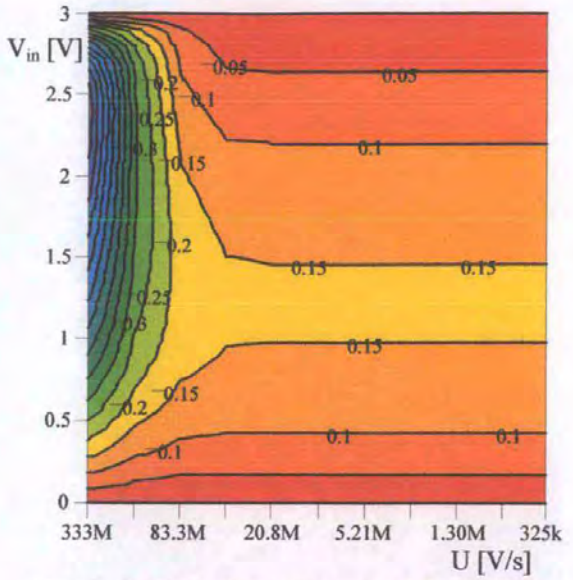
One circuit was a S&H with minimum feature-size pass-transistor (drawn dimensions were W_{drawn} = 2.0μm, L_{drawn} = 0.8μm) and C_h =0.1pF; the other S&H employed a large, square, pass-transistor (drawn dimensions were W_{drawn} = 8.8μm, L_{drawn} = 8.15μm) and C_h = 8.0pF. The measured data from both circuits is compared to results derived from calculations using the single-lump model and to data from PSpice transient simulations. The parameters used in the single-lump model calculations were the ones listed earlier in section 7.1, and the PSpice calculations employed a, foundry supplied, BSIM3v2 model.

7.2.1 Measured results using an off-chip clock source.

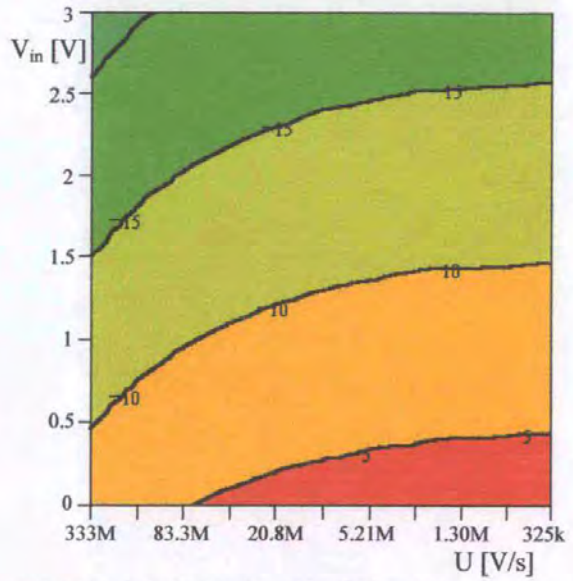
Contour plots of CLFT and INL data for the two basic S&H circuits are shown on the next two pages. The clock for the measurements was supplied from an off-chip source. Plots for the S&H with the minimum feature-size pass-transistor are reproduced in Fig. 7-2, and for the S&H with the large, square pass-transistor in Fig. 7-3. The six plots in each figure are arranged in columns. The three plots in the first column show CLFT for: the single-lump model, PSpice simulations and measurement results. The INL plots in the second column are, again, in the same order.



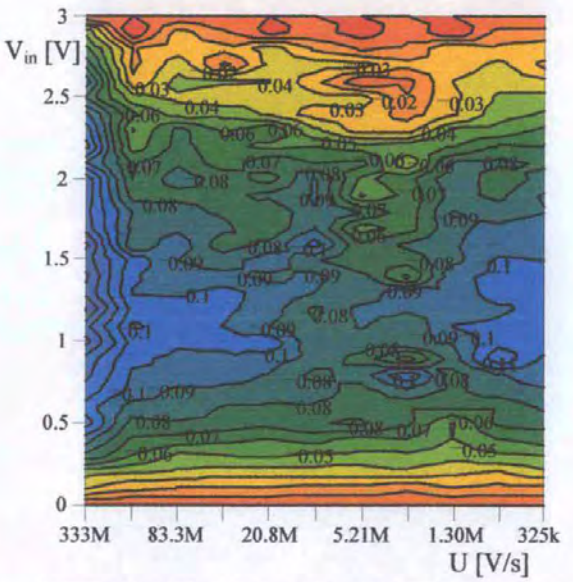
a) CLFT [mV], single-lump model calculation



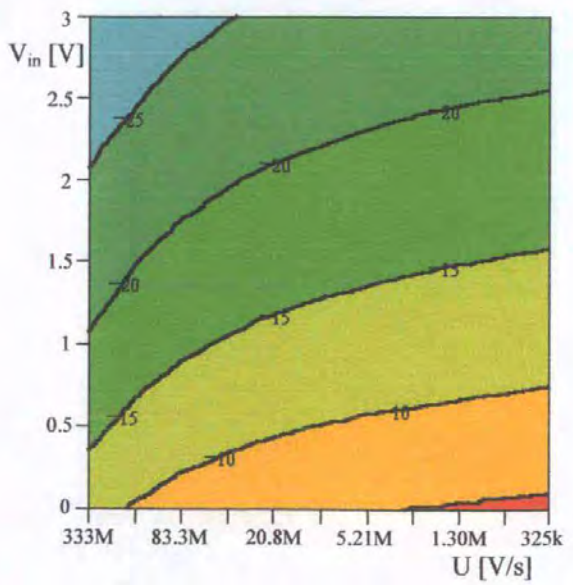
b) INL [0.1%], single-lump model calculation



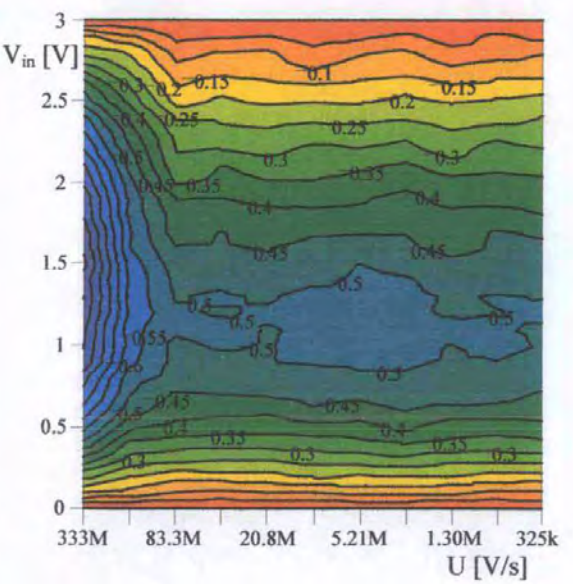
c) CLFT [mV], PSpice simulation (BSIM3v2)



d) INL [0.1%], PSpice simulation (BSIM3v2)

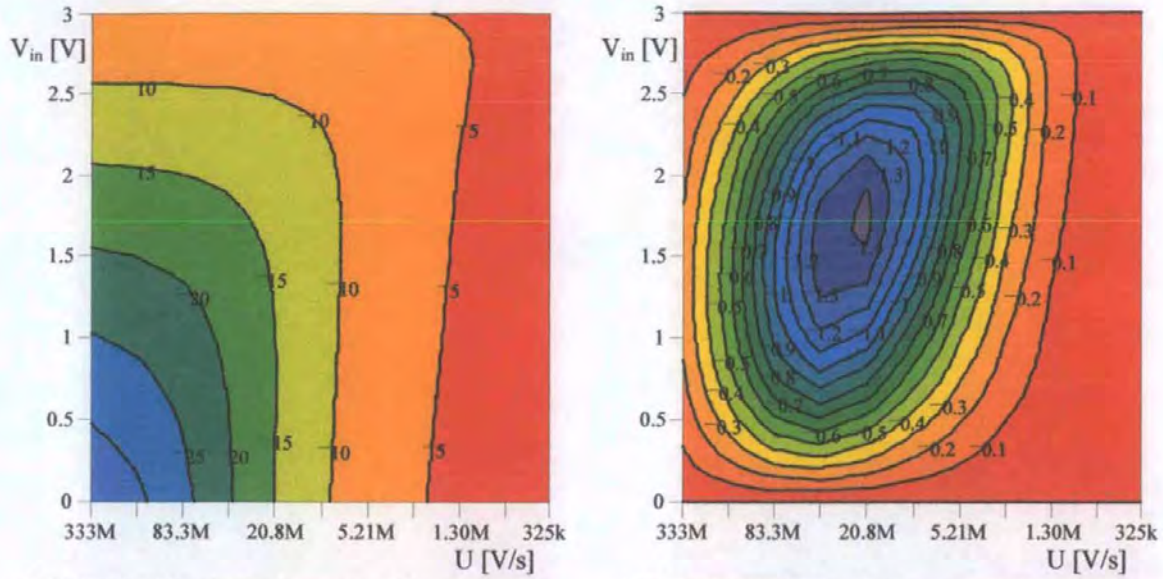


e) CLFT [mV], measured



f) INL [0.1%], measured

Fig. 7-2: CLFT and INL for the basic S&H with W = 2.0μm, L = 0.8μm and C_h = 0.1pF.



a) CLFT [mV], single-lump model calculation

b) INL [0.1%], single-lump model calculation

c) CLFT [mV], PSpice simulation (BSIM3v2)

d) INL [0.1%], PSpice simulation (BSIM3v2)

e) CLFT [mV], measured

f) INL [0.1%], measured

Fig. 7-3: CLFT and INL for the basic S&H with W = 8.0μm, L = 8.0μm and C_h = 8.0pF.

Considering that all parasitics were assumed negligibly small, there clearly is a very good match between measurements, simulations and calculations, for the S&H with a large pass-transistor. The largest difference between the plots clearly is at low U, where the sensitivity of CLFT to V_{in} is noticeably larger for the measured data than for the predictions. This is clearly visible in the plot below, which combines the CLFT results from measurements, simulations and calculations for U = 325kV/s in one plot:

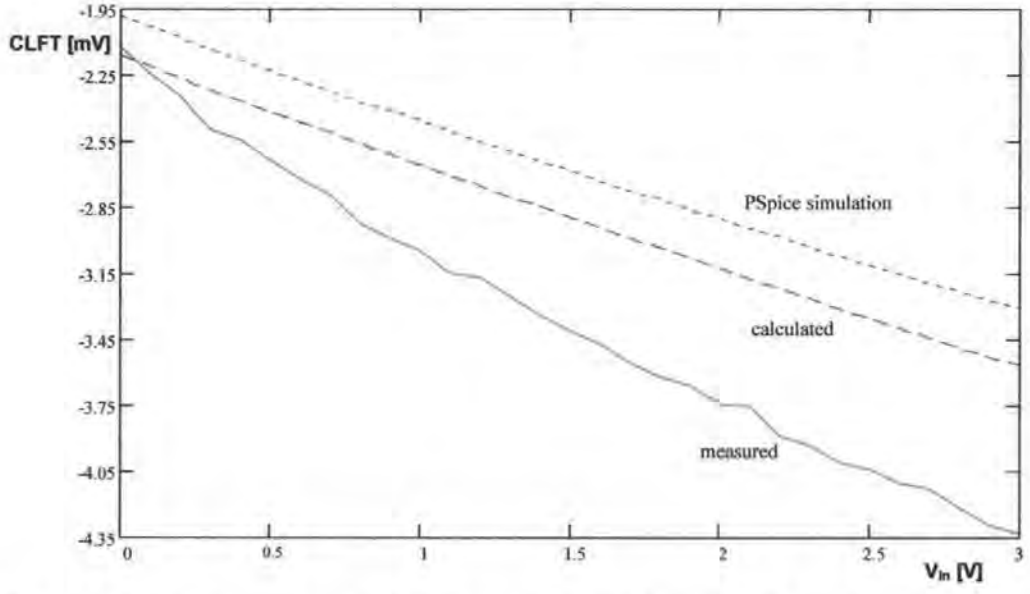


Fig. 7-4: CLFT for the basic S&H at U = 325kV/s; W = 8.0μm, L = 8.0μm and C_h = 8.0pF.

The steeper gradient of the measured CLFT can be explained by a larger than anticipated C_{ol} contribution: at low U the dCLFT/dVin is proportional to $-C_{ol}$ (see chapter 4.3.3.2). The actual C_{ol} for this S&H circuit appears to be about 50% larger than assumed in the calculations and simulations.

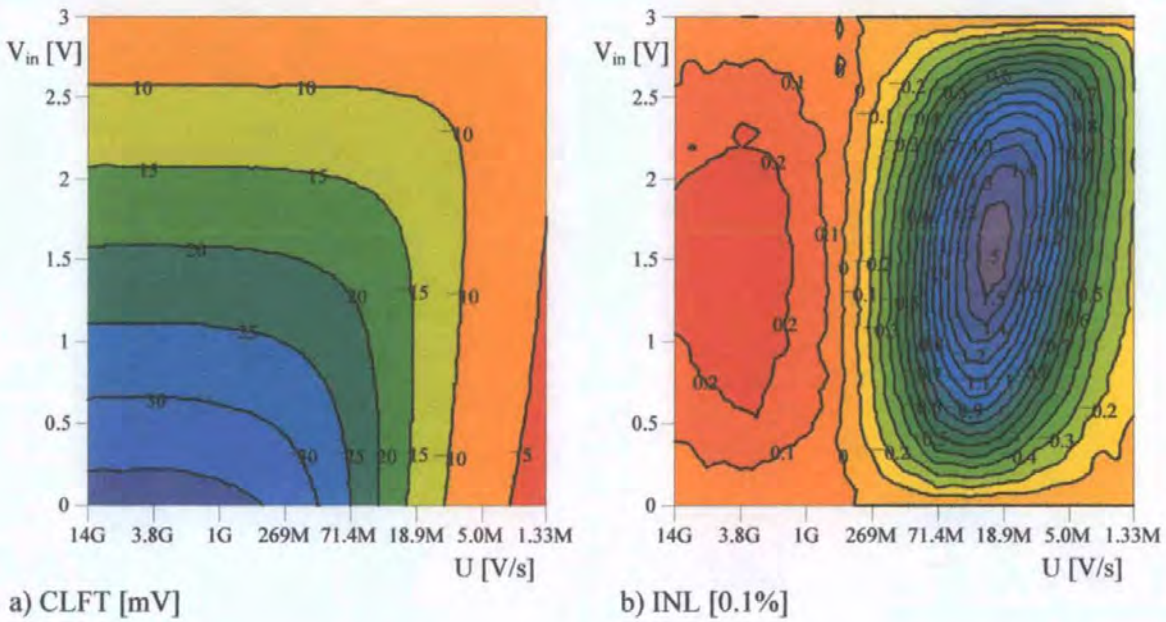
The plots for the S&H with the minimum feature size pass-transistor show much greater deviation between measured and predicted CLFT (see Fig. 7-2). The overall behaviour of CLFT appears to be modelled correctly, but the magnitude of CLFT is either too large (single-lump model) or too small (PSpice simulation). This is even more apparent in the INL plots for the circuit. Here, the relative behaviour of the INL is recreated faithfully, but

the magnitude is approximately a factor of 5 too small for the PSpice simulation and about a factor of 3.4 too small for the single-lump model calculations.

Because of this large discrepancy between measured and predicted behaviour, in the S&H using minimum feature size devices, results for the other S&H circuits (the S&H with BP-TSD, and the linearised S&H) will be reported only for circuits using large devices.

7.2.2 Measured results using the on-chip ramp generator.

The plots in this section show measured performance of the basic S&H when employing the on-chip ramp generator as a clock source.



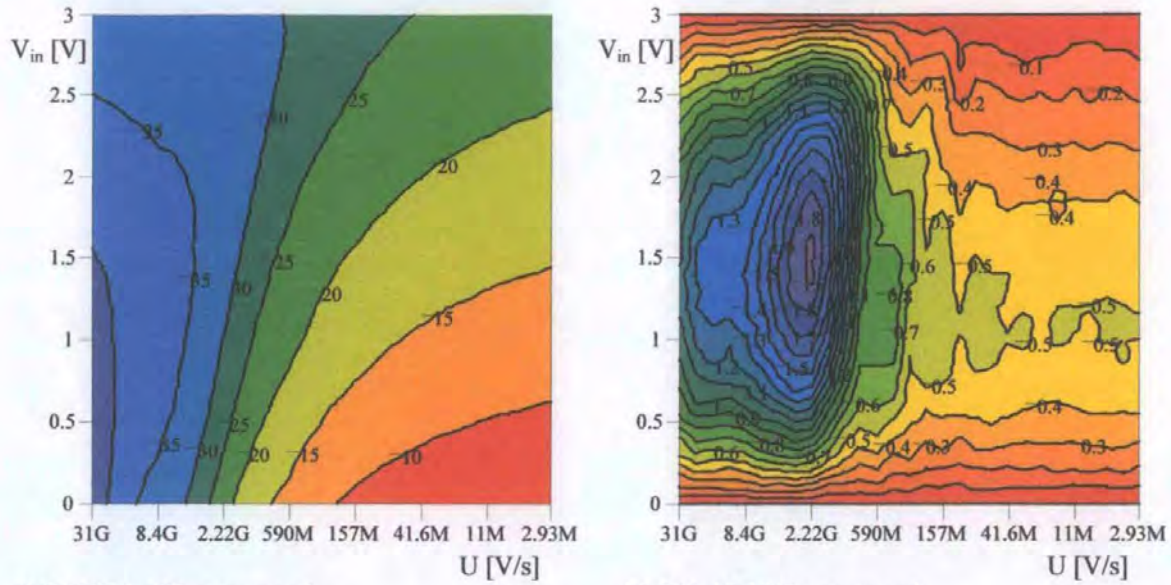
a) CLFT [mV] b) INL [0.1%]

Fig. 7-5: Measured results for CLFT and INL of the basic S&H circuits using the on-chip ramp generator; W = 8.0μm, L = 8.0μm and C_h = 8.0pF.

The INL plot clearly shows INL changing sign from positive to negative at $U_0 \approx 520$MV/s, which is not far off from an initial estimate $U_{MR0} = 750$MV/s which is found by solving $INL_{MR} = 0$ for U (for INL_{MR} see Eqn. 4-21).

The INL plots, (Fig. 7-3 and Fig. 7-5) also show that the recommendations for minimising distortion, made in chapter 4, are valid. Clearly, INL is smallest at U_0, but it is also fairly

sensitive to U, particularly for $U < U_0$. Low U are definitely best if small INL and low sensitivity to U is required. The next best solution is to use very high U. This may not always be achievable, especially for short channel devices, where U well in excess of 30GV/s (corresponding to $t_f < 160$ps) are required as the next figure shows:



a) CLFT [mV], measured

b) INL [0.1%], measured

Fig. 7-6: Measured results for CLFT and INL of the basic S&H circuits using the on-chip ramp generator; W = 1.2μm, L = 0.66μm and C_h = 0.1pF.

The actual condition for fast turn-off, as defined in chapter 4, was $U \gg 0.5\beta V^2_{HT}/C_h$. Assuming V_{in} = 1.5V this relation evaluates to U » 4.5GV/s for the S&H with the minimum feature size pass-transistor ($\beta = 181.1\mu A/V^2$ and C_h = 0.1pF), and U » 31MV/s for the S&H with the large, square, pass-transistor ($\beta = 99.5\mu A/V^2$ and C_h = 8.0pF). The INL plots show, that $U \approx 0.5\beta V^2_{HT}/C_h$ must be avoided if low INL (and low distortion) are to be achieved.

7.3 Evaluation of the bottom-plate TSD S&H circuit.

S&H circuits employing a bottom-plate TSD (BP-TSD) were realised on the test chip. The BP-TSD was a minimum feature size NMOS transistor whose Gate voltage was controlled by an external current source, I_{bias}. The schematic diagram for the circuits is shown below.

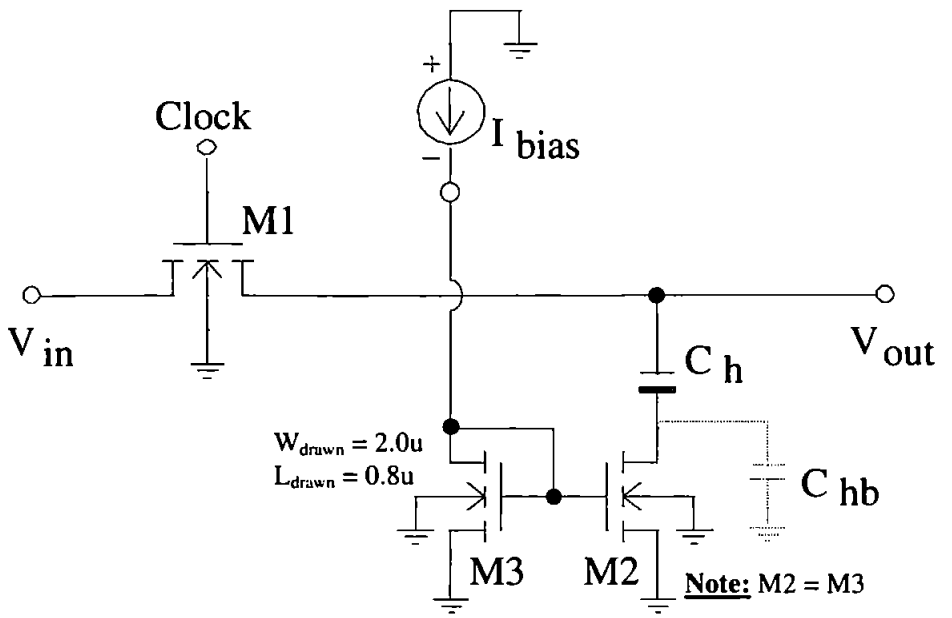


Fig. 7-7: Schematic for the test-chip's S&H circuits that employ BP-TSD.

The data reported on in this section was derived from measurements, calculations and simulations on a circuit using a large geometry pass-transistor, M1, with W_{draw} = 8.80μm, L_{draw} = 8.15μm. The circuit's hold capacitance, C_h, and its bottom-plate capacitance, C_{hb}, were estimated from the actual layout geometry data and the factory provided area and fringing capacitance data: C_h = 8.48pF, C_{hb} = 1.26pF. Other parasitics were assumed to be negligibly small. The bias current, I_{bias}, and clock applied to the circuit, came from off-chip sources. Clock fall-rates, U, between 333MV/s and 325kV/s were applied; V_H = 5V and V_L = 0V were used throughout. The CLFT reduction plots below show the relative magnitude of the CLFT for I_{bias} = 25nA compared to CLFT measurements from the basic S&H (i.e. with no TSD present).

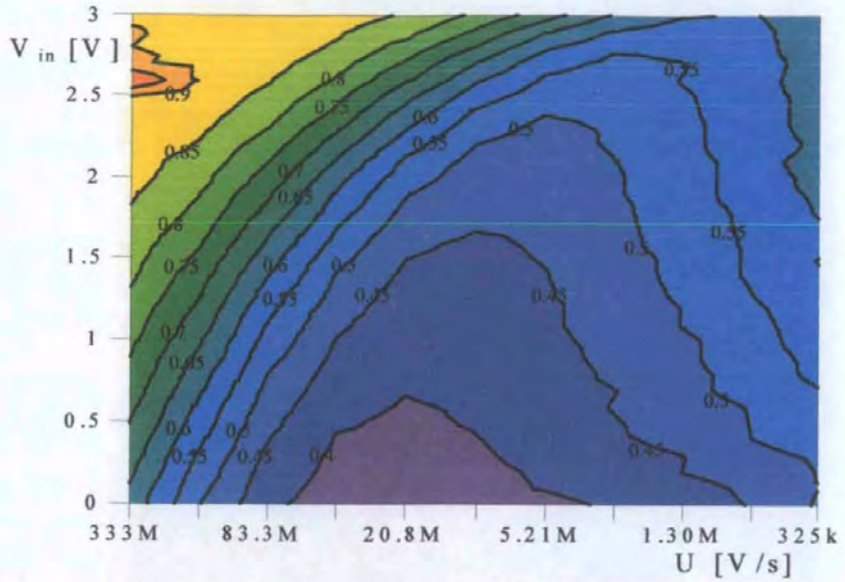


Fig. 7-8: Measured CLFT reduction for BP-TSD with I_{bias} = 25nA.

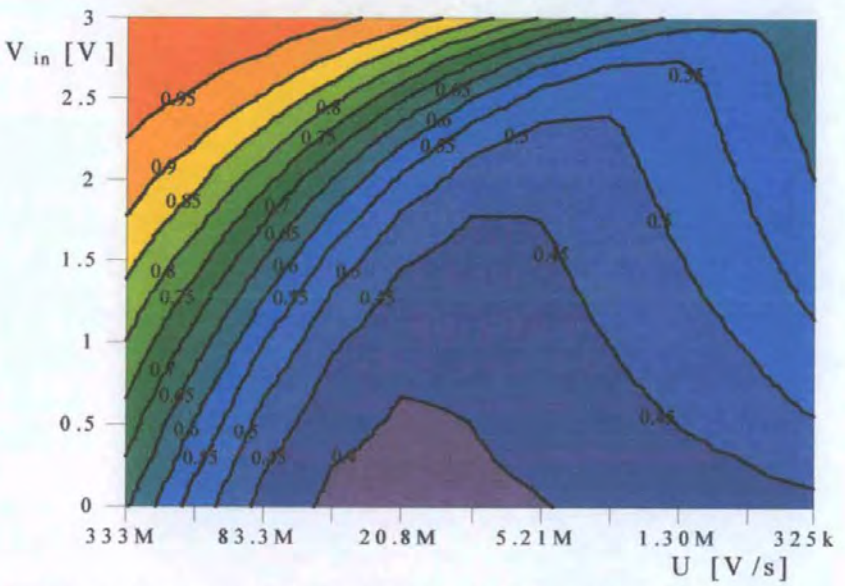


Fig. 7-9: BSIM3v2 simulation result for BP-TSD with I_{bias} = 25nA.

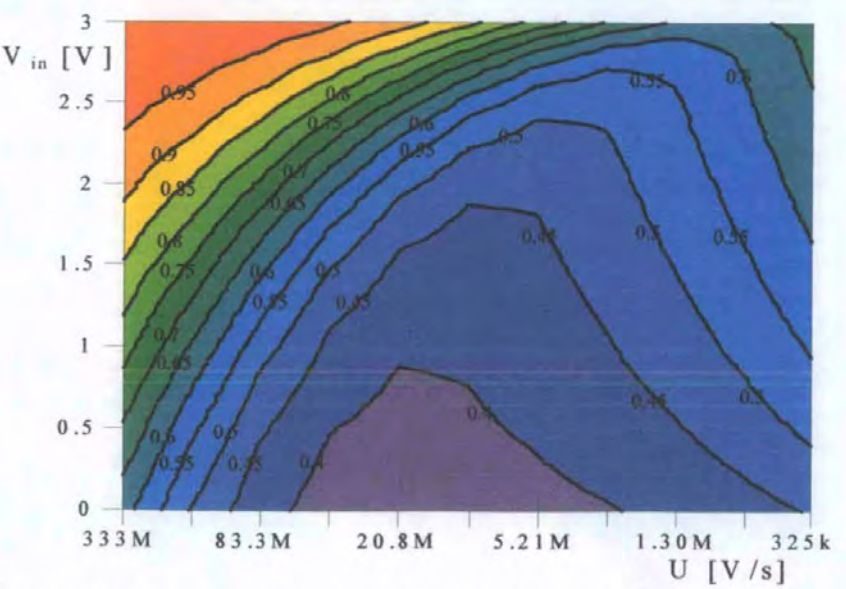


Fig. 7-10: CLFT reduction predicted by the analytical BP-TSD model (Eqn. 6-7).

Clearly, the measured data agrees remarkably well with predictions, even though calculations and simulations were only based on estimates of component size. Despite the overall agreement of the results there are some differences apparent, too. In particular the TSD model appears to be somewhat over optimistic in its estimate of the achievable reduction. This is especially noticeable for low V_{in} and $U \approx 20MV/s$, where the maximum reduction was achieved. Here the PSpice simulation (BSIM3v2 model) appears to be closer to the measured result. This difference between the TSD model and simulation results can be explained largely by saturation mode effects as the following two plots show:

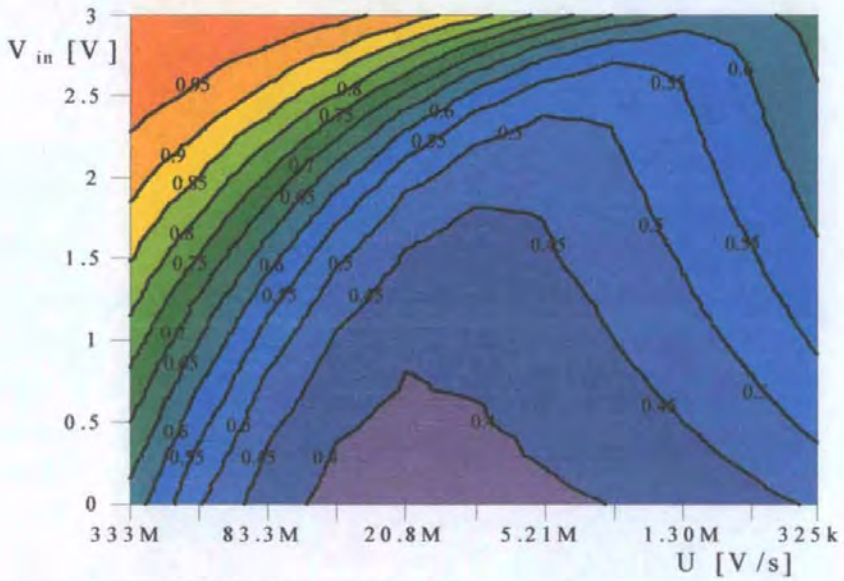


Fig. 7-11: Predicted CLFT reduction with only linear mode operation of M1 considered.

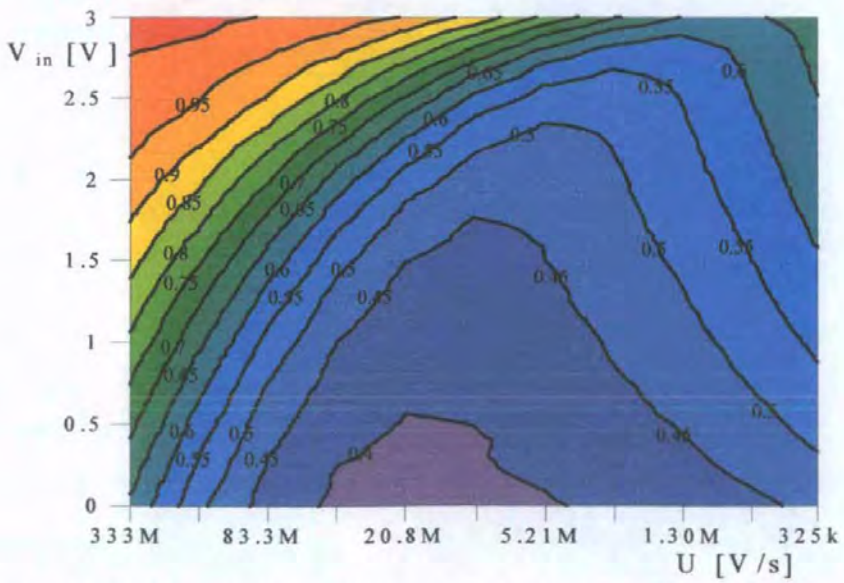


Fig. 7-12: Predicted CLFT reduction with linear and saturation mode of M1 considered.

These two plots were derived from transient simulations similar to the ones described in chapter 3.4, where the impact of saturation mode on CLFT was examined. The first plot (Fig. 7-11) was derived from transient simulations of the circuit using a cut-down version of the SPICE Level 1 model which considered only two regions of operation: the linear and the cut-off region. This linear mode only model is identical to the one used in the development of the single-lump model (from which the analytical BP-TSD model of Eqn. 6-7 had been derived). Essentially, the only difference between this simulation and the analytical BP-TSD model of Eqn. 6-7 was that the transient simulation assigned the pass-transistor's Source terminal to the hold node, whereas the single-lump model (and therefore the BP-TSD model) incorrectly assumed that M1's Source terminal was on the input side during turn-off. This difference in the assignment of M1's Source leads to a small difference of the CLFT reduction plots for the BP-TSD model (Fig. 7-10), and the linear mode only transient simulation (Fig. 7-11) at low V_{in} and U ≈ 20MV/s (where the BP-TSD predicts slightly more reduction in CLFT than the linear mode only simulation does). Apart from this small difference the two plots are clearly identical.

Similarly, the results from transient simulations that used a SPICE Level 1 model of the pass-transistor, in which both linear and saturation mode were considered, (Fig. 7-12) and the results of PSpice transient simulations which used the BSIM3v2 model (Fig. 7-9) were almost identical. Here, the two plots differ only in the slow switching region (i.e. for U ≤ 2.6MV/s), where weak inversion effects, not considered in the Level 1 model, improve the effectiveness of the BP-TSD.

Overall, the PSpice BSIM3v2 transient simulation and the SPICE Level 1 transient simulation with both linear and saturation mode considered come closest to the measured result. Both the BP-TSD model and the linear mode only simulation are somewhat over-optimistic in their predictions of the maximum CLFT reduction achievable. This is

consistent with the latter two methods failing to take the saturation mode contribution to CLFT into account (see chapter 3).

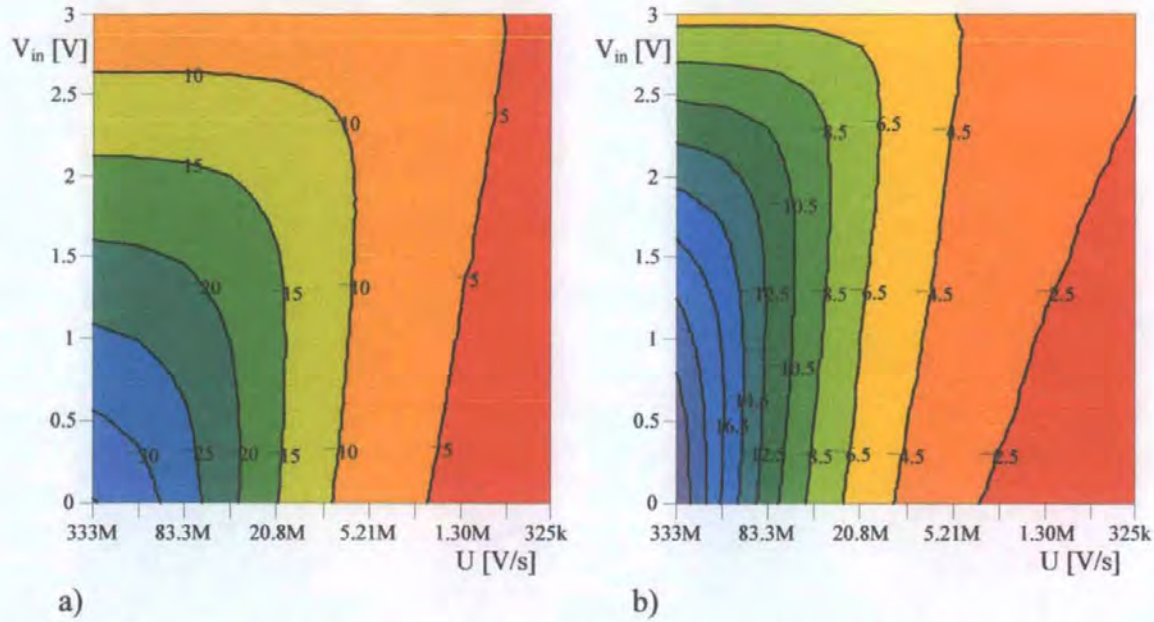


Fig. 7-13: Measured CLFT [mV] for a) basic S&H without a BP-TSD, b) S&H with BP-TSD and I_{bias} = 25nA.

Considering that the CLFT error voltage of the basic S&H without a TSD (shown in Fig. 7-13 a) above) was only about -15mV at the point where the maximum reduction occurred (measured maximum reduction was 2.67 at U = 20.8MV/s, V_{in} = 0V), and that the ratio of C_h/C_{hb} was only about 6.7, it can be seen that the saturation mode contribution to CLFT can have a noticeable impact on the improvement achievable with TSD, even at small levels of CLFT and for small C_h/C_{hb}.

Much larger C_h/C_{hb} of ≈ 25, could have been achieved if C_h had been realised from large capacitor structures rather than the 80 × 0.1pF capacitor array used on the test-chip. For C_h/C_{hb} = 25, i.e. C_h = 8.48pF and C_{hb} = 0.339pF, a greater than four-fold reduction in CLFT could have been expected as the two plots below show. Here, the impact of saturation mode effects on CLFT is much more apparent. For example, at U = 20.8MV/s

the BP-TSD model predicts a greater than four-fold reduction in CLFT for $V_{in} \leq 1.0V$, whereas the SPICE Level 1 simulation predicts this only for $V_{in} \leq 0.5V$.

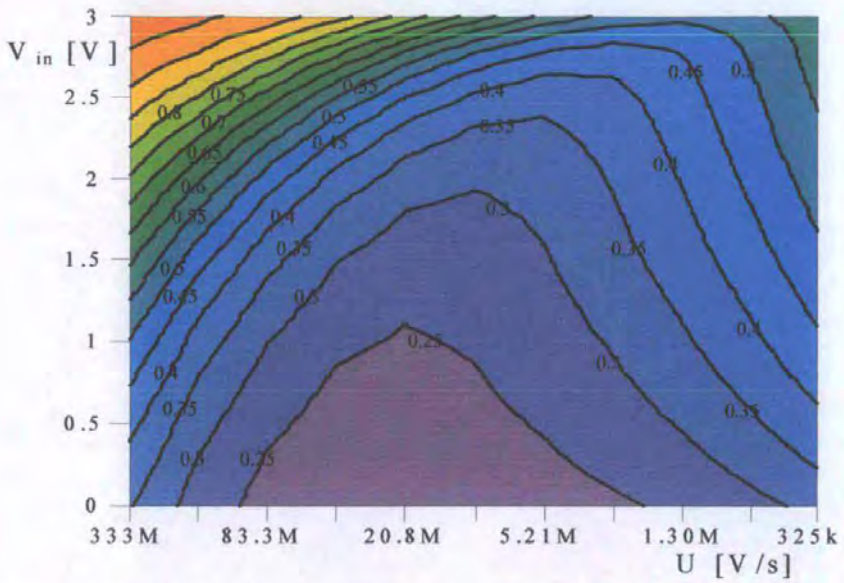


Fig. 7-14: CLFT reduction predicted by the analytical BP-TSD model for C_{hb} = 0.339pF.

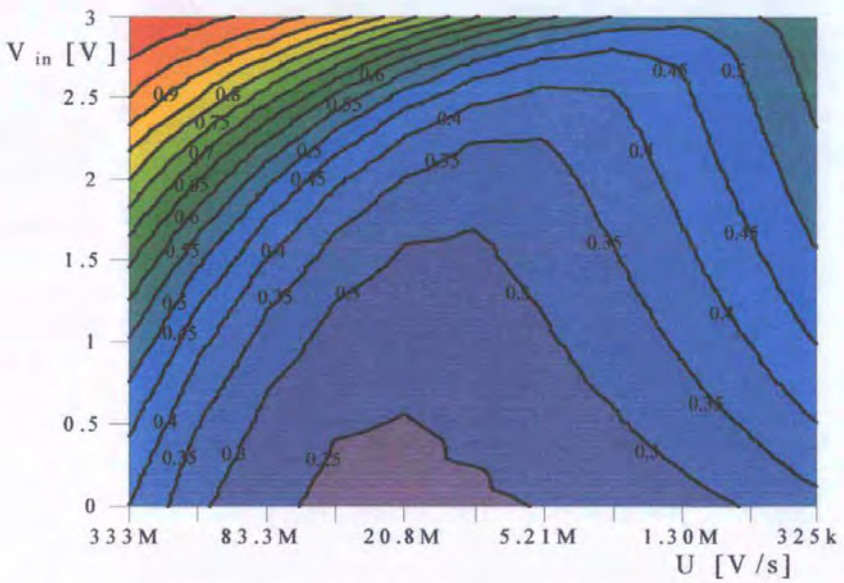


Fig. 7-15: CLFT reduction with linear and saturation mode considered, C_{hb} = 0.339pF.

S&H circuits, and SC circuits, that use bottom-plate sampling, or other multi-phase clocking schemes, in which the switch on the ground side (or bottom-plate) of the sampling capacitor (i.e. the bottom-plate switch) is turned-off before a signal-side switch in the same path, such as the circuit's described in [36] and [37], may also enter saturation mode and thus prove less effective than anticipated by the simple CLFT models (which ignored

saturation mode effects). It is therefore important that simulations, or calculations, of circuits that employ bottom-plate sampling, other multi-phase clocking schemes, or TSDs include saturation mode effects in their models of the pass-transistor.

Another issue that concerns both BP-TSD and bottom-plate sampling is, that these CLFT reduction methods move the point of worst-case INL to higher clock fall-rates. The two INL plots below show this shift toward higher U clearly. The one on the left shows the measured INL of the basic S&H without a TSD or bottom-plate switching, and the one on the right shows the measured INL of the S&H with BP-TSD and I_{bias} = 25nA.

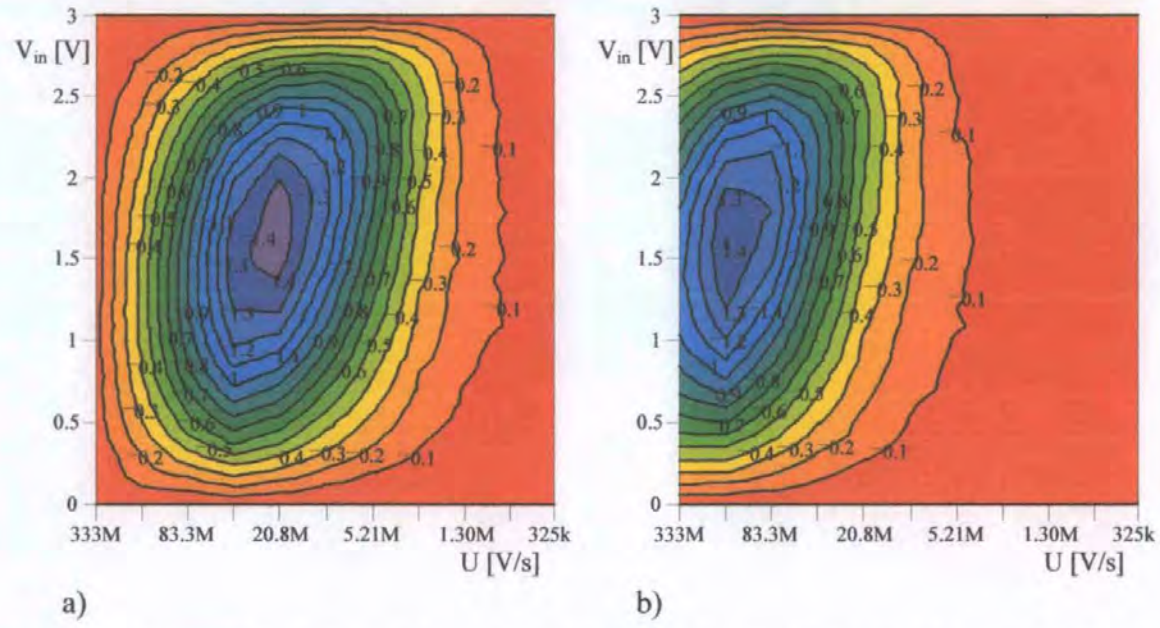


Fig. 7-16: Measured INL [0.1%] for a) basic S&H without a BP-TSD, b) S&H with BP-TSD and I_{bias} = 25nA.

Such a shift in INL to higher U is clearly beneficial in circuits where low to medium U are acceptable, as it leads to improved performance at these lower fall-rates (both INL and CLFT are lower; measured INL at U = 325kV/s was -0.0058% for the S&H with BP-TSD, and -0.00713% for the basic S&H). Alternatively, it allows the use of higher U while still meeting the desired performance specifications (the INL plot of S&H with the BP-TSD appears to be moved to U about 7 times higher than in the basic S&H).

For circuits that combine high clock fall-rates and BP-TSD (or bottom-plate sampling) this shift of the worst-case INL point to higher U may actually lead to increased distortion, while the level of CLFT is actually reduced. Fig. 7-13 shows this reduction in the absolute level of CLFT clearly (which is as much as a factor of 1.6 for U = 333MV/s). INL, in contrast has increased from less than -0.01% to almost -0.11% (a more than ten-fold increase in INL), as Fig. 7-16 shows.

7.4 Evaluation of the linearised S&H circuit.

The merits of the V_{HT} controlled, or linearised, S&H circuit were discussed earlier in chapter 4 and chapter 6.2 and an analytical model for the circuit's CLFT behaviour (Eqn. 6-11) was derived. This model predicted that for such a S&H the distortion arising from CLFT would be independent of U.

Linearised S&H circuits, similar to that discussed in chapter 6.2, were realised on the test-chip. The schematic diagram for these S&H circuits is shown below. The clock signal, V_{in}, and I_{bias} (which controls the circuit's V_{HT} voltage) were all supplied from off-chip sources.

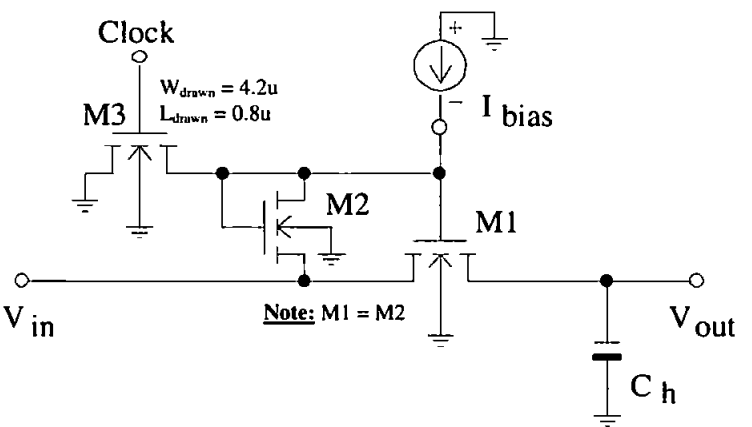
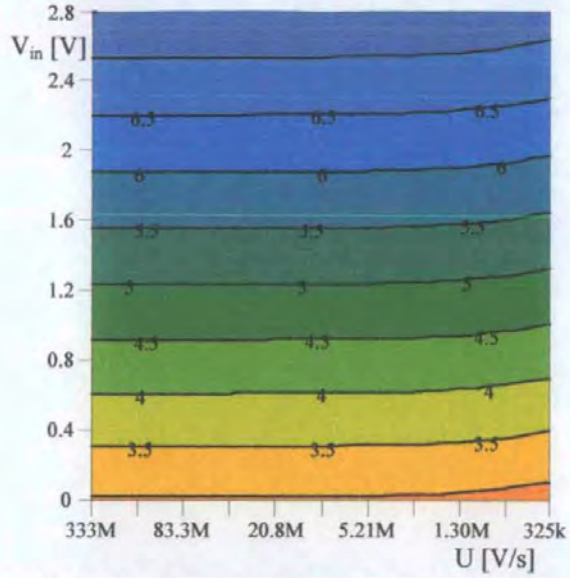
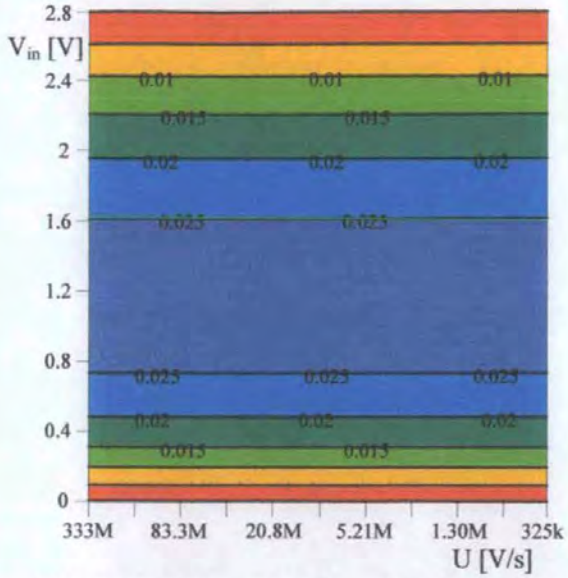


Fig. 7-17: Schematic for the test-chip's linearised S&H circuits.

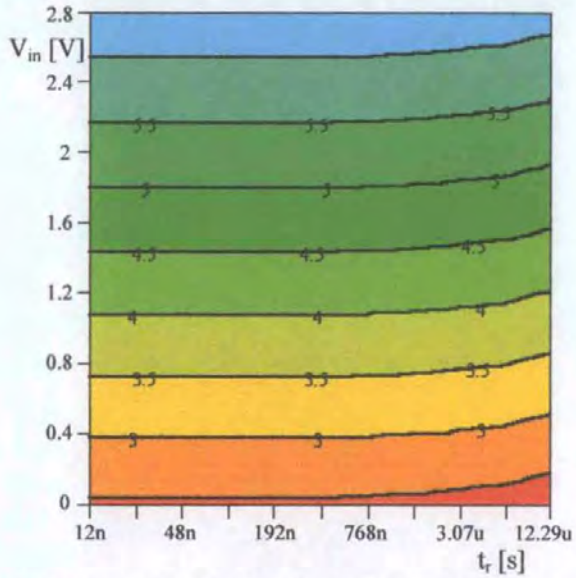
The data reported was derived from measurements, calculations and simulations performed on a linearised S&H circuit which employed a large geometry pass-transistor, M1 (W_{draw} = 8.80μm, L_{draw} = 8.15μm). The transistor parameters used in the calculations are the ones listed in section 7.1, I_{bias} was between 200nA and 25μA and C_h = 2.4pF. For PSpice simulations and measurements a clock with U between 333MV/s and 325kV/s was applied to the gate of M3 (the sample-to-hold transition for this circuit was on the rising edge of the clock). For the calculations (which used Eqn. 6-11) it was assumed that the Gate voltage of M1, $V_{G,M1}$, experienced the same rate of change as the input clock did (this assumption was made, simply because the exact fall-rate of $V_{G,M1}$ was not known, and could not be measured, since $V_{G,M1}$ was an inaccessible, chip internal, signal.



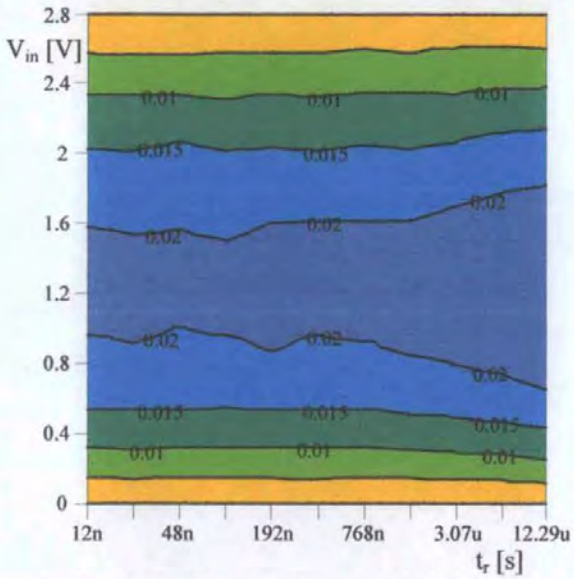
a) CLFT [mV], analytical model (Eqn. 6-11)



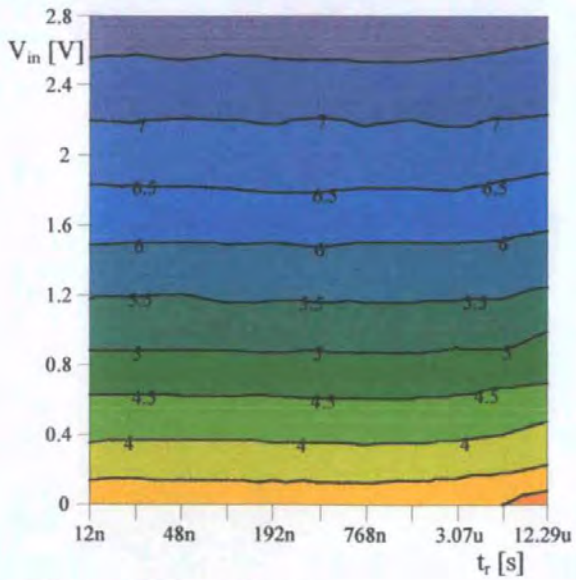
b) INL [0.1%], analytical model (Eqn. 6-11)



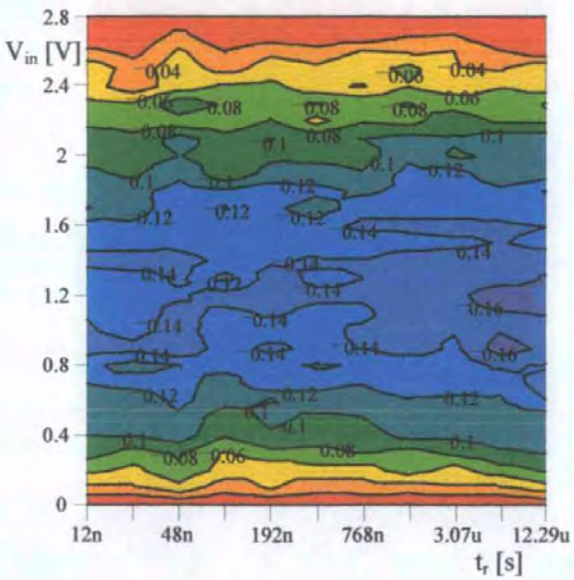
c) CLFT [mV], PSpice simulation (BSIM3v2)



d) INL [0.1%], PSpice simulation (BSIM3v2)

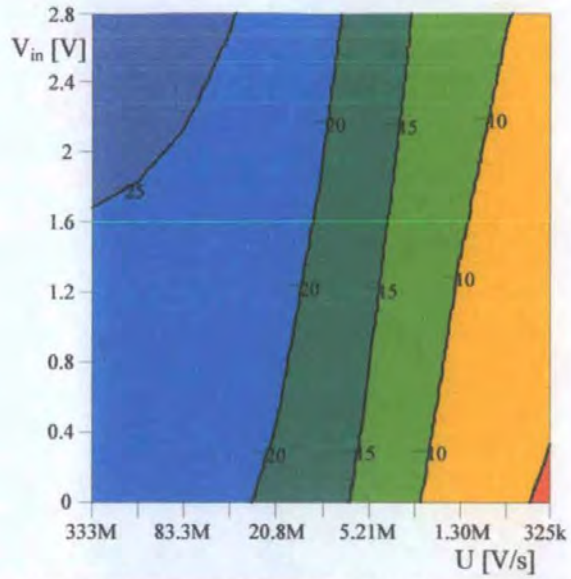


e) CLFT [mV], measured

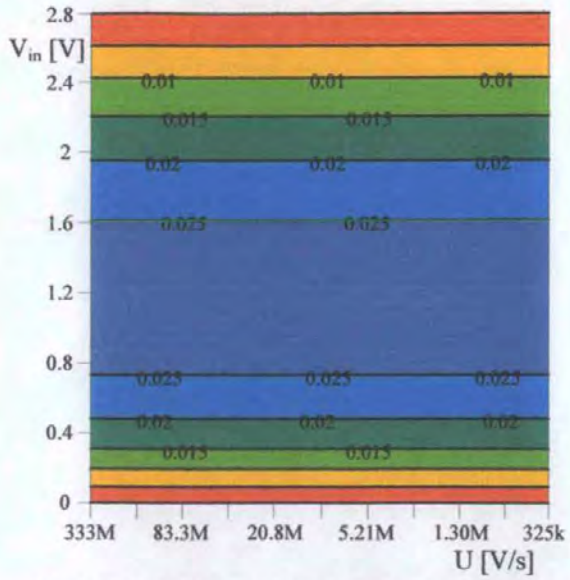


f) INL [0.1%], measured

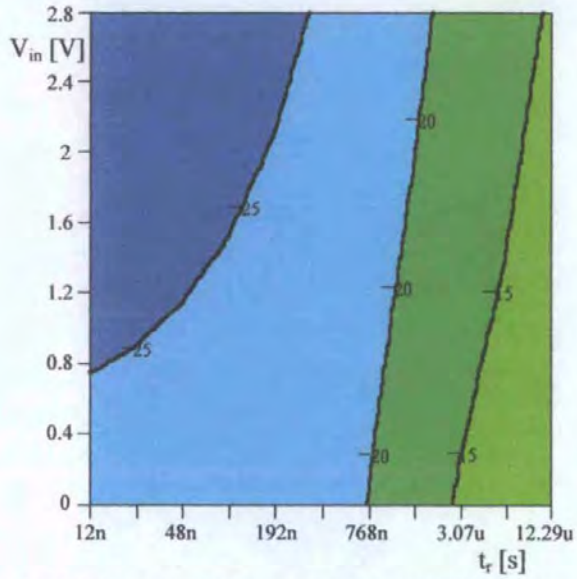
Fig. 7-18: CLFT and INL of the linearised S&H; W = L = 8μm, C_h = 2.4pF & I_{bias} = 200nA.



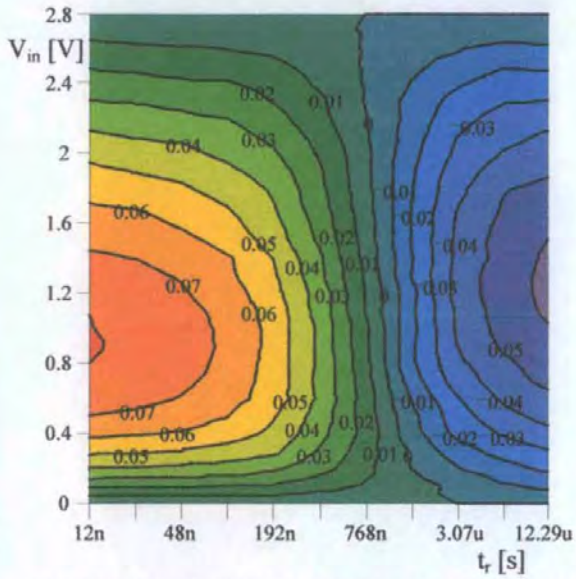
a) CLFT [mV], analytical model (Eqn. 6-11)



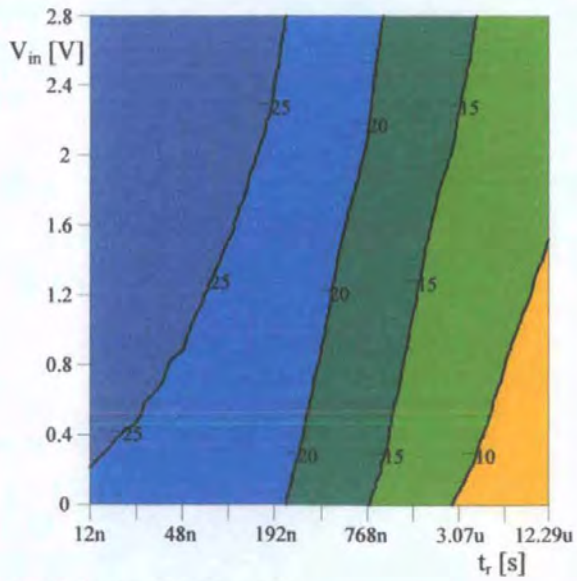
b) INL [0.1%], analytical model (Eqn. 6-11)



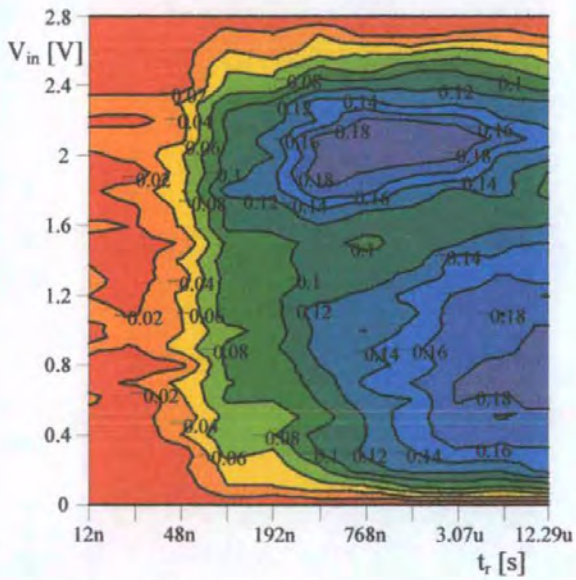
c) CLFT [mV], PSpice simulation (BSIM3v2)



d) INL [0.1%], PSpice simulation (BSIM3v2)



e) CLFT [mV], measured



f) INL [0.1%], measured

Fig. 7-19: CLFT and INL of the linearised S&H; W = L = 8μm, C_h = 2.4pF & I_{bias} = 25μA.

At low bias currents the circuit clearly behaves as anticipated by Eqn. 6-11 (see Fig. 7-18 for I_{bias} = 200nA). The INL may be larger than predicted, but this is consistent with measurements from the BP-TSD and the basic S&H, where INL was also larger than predicted. Here, the measured INL is approximately -0.0153% (rising to -0.0173% at low U), the PSpice simulation predicts -0.00214% (rising to -0.00242% at low U) and Eqn. 6-11 estimates -0.00278% (i.e. measured INL is about a factor of 7.7 larger than predicted by the PSpice simulation, and 5.5 larger than calculated from Eqn. 6-11).

A direct comparison of the linearised S&H's INL to that of the S&H with BP-TSD shows that the linearised circuits' INL was about 3 times larger (i.e. -0.0173% compared to -0.0058% for the S&H with BP-TSD at U = 325kV/s). This was expected, as INL $\propto 1/C_h$ (see chapter 4); and the C_h of the linearised S&H was 3.3 times smaller than the circuit's with the BP-TSD (C_h = 8.0pF compared to C_h = 2.4pF for the linearised S&H).

The picture is somewhat different for I_{bias} = 25μA, where the INL of the linearised circuit exhibits some sensitivity to U (see Fig. 7-19). Interestingly, this sensitivity of INL to U is very similar to the one observed in the basic S&H (see Fig. 7-5); only the magnitude of the effect is much reduced. Earlier, in chapter 4, it was shown that for the basic S&H, this sensitivity of INL to U arose only if V_{HT} was signal dependent.

Clearly, the V_{HT} of the linearised S&H can not be totally independent of V_{in}, otherwise INL would be independent of U. The plots of Fig. 7-19 show that this sensitivity of INL to U was anticipated by the PSpice simulations, but not by the analytical model (which assumed that the circuit's V_{HT} was independent of V_{in}, and therefore, that changes in U would only cause a change in the circuit's DC offset, but no change in INL, see chapter 6.2).

The INL of the linearised S&H with I_{bias} = 25μA was measured at between -0.0024% (at fast rise-times, t_r, of the external clock) and -0.0204% (at slow t_r), while the PSpice

simulation predicted INL between +0.00809% and -0.00622%, and Eqn. 6-11 estimated INL at -0.00278%, for the range of U tested.

Far from being a nuisance this sensitivity of INL to U can be beneficial, as it makes further reduction of INL possible. The plot of PSpice simulation results for a linearised S&H circuit with fall-rate control of the pass-transistor gate voltage, $V_{g,M1}$, shows this benefit clearly (see Fig. 7-20 below). In this simulation, the fall-rate of $V_{g,M1}$ was controlled, rather than the rise-time, t_r, of the clock voltage that was applied to the gate of M3, $V_{g,M3}$, (the latter method had been chosen for the circuit implemented on test-silicon).

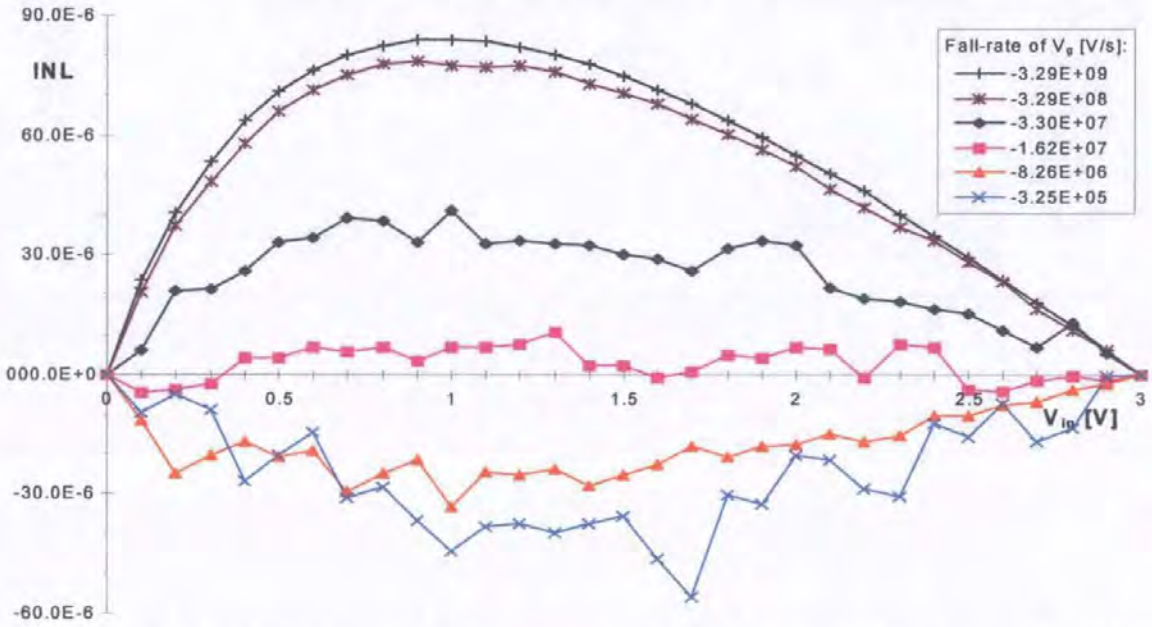


Fig. 7-20: INL plot derived from PSpice simulation of the linearised S&H circuit; C_h = 2.4pF, $V_L = V_B$ = 0V and I_{bias} = 25μA. Here U of $V_{g,M1}$ was controlled, rather than t_r of $V_{g,M3}$.

Comparison of this plot to the PSpice simulation result of Fig. 7-19 shows that both predict identical levels of INL at the extremes of fast and slow switching. The plots also show that INL appears not to exceed these bounds for any U between these two extremes. This is an important difference to the basic S&H, where INL went through a much larger maximum, between these two extremes (see INL plot Fig. 4-4, which is for a basic S&H which used identical C_h and pass-transistor to the ones used for the simulation of Fig. 7-20). The

magnitude of the INL for fast switching is also much reduced if compared to the basic S&H's. Furthermore the linearised circuit's sensitivity of INL to U appears to be significantly smaller than the basic S&H's, as comparison of Fig. 7-20 to Fig. 4-5 shows.

All these are very useful properties, as they suggest that a significant further reduction in INL could be achieved by tuning U. The circuit biasing current also offers some control over INL, as the PSpice simulation result for the test-circuit's linearised S&H with I_{bias} = 12.5μA shows:

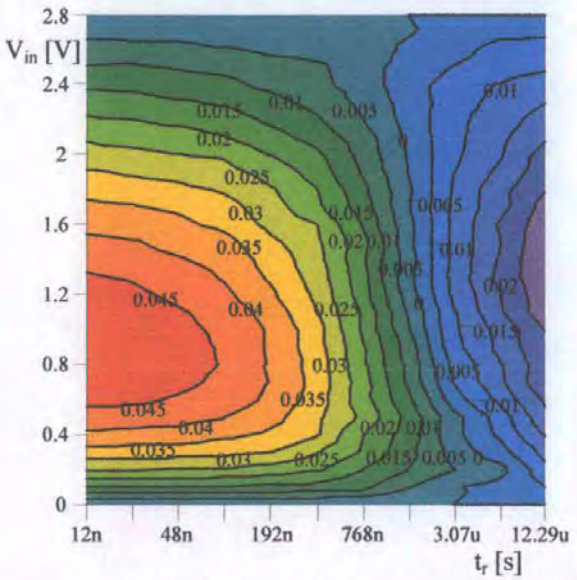


Figure 7-21: INL [0.1%] of the linearised S&H; W = L = 8μm, C_h = 2.4pF & I_{bias} = 12.5μA.

The INL of the linearised S&H clearly is much reduced (compared to that of the basic S&H). The measurements performed on the circuit show, that significant further reduction in INL can be achieved by manipulating U and I_{bias}. It is suggested that further work be undertaken on this circuit idea, with the view to find an optimal solution for INL reduction.

8. Summary and Conclusions

In summary, the clock-feedthrough phenomenon was introduced and its impact on the signal integrity of sample-and-hold circuits was studied. Analytical models for predicting CLFT were presented and their validity was confirmed by both circuit level simulations (using PSpice) and measurements on a test-chip. The test-chip was realised on a 0.8μm mixed-signal CMOS process.

A general introduction to S&H circuits, indicating the specific performance measures that apply was given. The notion of the MOS transistor as a switch was introduced, and it was shown that the INL of a basic S&H (a S&H that consists only of a pass-transistor and a hold capacitor) was determined purely by CLFT. Thus, the INL of such a circuit was found to be a measure for the distortion that CLFT introduces to the sampled signal.

A review of the relevant literature showed considerable non-linear signal dependency of CLFT. The single-lump model (an analytical, closed form solution, for the CLFT error of the basic S&H) was found to give an adequate description of CLFT. Some deterioration in the model's accuracy was shown to occur at both high and low clock fall-rates. The model's increased error at low fall-rates was attributed to weak inversion effects in the pass-transistor. At high fall-rates, the deterioration of the single-lump models arose from the pass-transistor entering the diffusion mode of conduction and from charge pumping effects.

Also, in the course of this work it was discovered that saturation mode effects could adversely affect the accuracy of the single-lump model. This newly discovered, and previously unreported, saturation mode contribution to CLFT was shown to increase CLFT above the level predicted by the single-lump model. Measurements on a test chip showed that S&H circuits using TSD exhibited levels of CLFT that were higher than those

predicted by analysis based on the single-lump model. This saturation mode contribution to CLFT will also affect SC circuits that employ multi-phase clocking schemes (such as 'bottom-plate sampling'), which are a special case of the class 'S&H circuit with TSD'. Again, CLFT will be larger than anticipated, if the saturation mode contribution to CLFT is neglected in the analysis of these circuits.

Measurements showed that the use of TSD caused an increase in INL, if high clock fall-rates were employed. For low clock fall-rates the INL decreased.

The signal dependency of CLFT was analysed. It was found that CLFT introduces offset, gain and non-linearly signal dependent errors to the S&H output signal. This non-linearly signal dependent component of CLFT was identified as the source of INL in the basic S&H. Analysis of CLFT showed that both the gain error and INL, can be reduced, or indeed eliminated, by proper choice of circuit parameters such as pass-transistor size, hold capacitance, Bulk voltage, clock fall-rate and the clock high and clock low voltages. Combinations of these parameters were identified for which CLFT will become independent of the input voltage. Other combinations for which CLFT will be linearly dependent on the input voltage were also identified. For circuit applications where these methods could not be employed, recommendations and guidelines were established for how best to reduce INL.

It was shown that careful choice of the clock fall-rate alone can significantly reduce INL. A clock fall-rate can be identified at which INL will go through a minimum. PSpice simulations and measurements on the test-chip confirmed the existence of such a minimum.

New circuit ideas for reducing CLFT, and the CLFT induced INL, were presented. The previously mentioned TSD was one of these. The other was the linearised S&H circuit. In

this circuit the pass-transistor's Gate voltage was developed such that its Gate overdrive voltage in sample mode, V_{HT}, was constant and independent of the input voltage ($V_{HT} = V_{GS} - V_T$). Analytical models were developed for both the S&H with TSD and the linearised S&H. Simulations in PSpice and measurements on the test-chip showed good correlation with the analytical models on the whole.

8.1 Recommendations for further work.

Several fields of work have been identified which could be investigated in further research:

- In the course of this work the saturation mode contribution to CLFT was discovered (see chapter 3). This contribution to CLFT appears to reduce the CLFT reduction that can be achieved with TSD, bottom-plate sampling, or other multi-phase clocking schemes. The impact of the saturation mode contribution to CLFT on the performance of SC circuits, in particular on circuits that employ multi-phase clocking schemes, should be investigated further. It is expected that SC circuits with larger hold capacitance to bottom-plate capacitance ratios than achieved on the test chip will suffer more from this effect.

- The impact of clock fall-rate on the INL, and therefore distortion, of SC circuits that employ bottom-plate sampling (or other multi-phase clocking schemes) should be investigated further. Measurements on the BP-TSD circuits of the test-chip indicate that the INL of such circuits will be clock fall-rate dependent, and that bottom-plate sampling might lead to increased INL.

- The application of clock fall-rate control to S&H, and other SC circuits, with a view of reducing the CLFT induced distortion in these circuits. The analysis of the CLFT's signal dependency showed that significant reductions should be achievable (see chapter 4). Results from measurements on the proposed linearised S&H (see chapter 6.2 and chapter 7.4) indicate that application of clock fall-rate control to this linearised circuit might be particularly useful, and that very low levels of INL should be achievable. It is envisaged that circuits which 'tune out' CLFT induced distortion (i.e. INL), by automatically adjusting the clock fall-rate could be developed. This technique may prove also useful for SI circuits and other SC circuits, such as SC integrators and filters.

- The impact of hold node impedance and of signal-source impedance on the INL of S&H circuits should be investigated further. Measurements, and simulations, on S&H with BP-TSD showed that the increased hold node impedance of these circuits caused a deterioration in INL at higher clock fall-rates. It is expected that increased signal-source impedance will do the opposite and improve INL at higher clock fall-rates.

- The effectiveness of the CLFT reduction techniques, and the applicability of analysis and models presented in this thesis (which were based on simple long-channel models of the MOSFET) to deep sub-micron technologies could be investigated. Measurements performed on a S&H using a pass-transistor with L = 0.66μm and W = 1.2μm indicate that the results are relevant to sub-micron technologies.

- Investigation into the reasons why, at low clock fall-rates, the measured INL was consistently higher than the INL predicted by the PSpice simulations and the analytical model calculations could prove very fruitful.

List of Abbreviations

Abbreviation	Full Text
ANN	Analogue Neural Network
BP-TSD	Bottom-Plate TSD
CLFT	Clock-Feedthrough
INL	Integral Non-Linearity
MOST	MOS transistor
PT	Pass-Transistor
S&H	Sample-and-Hold circuit
SC	Switched-Capacitor
SI	Switched-Current
T&H	Track-and-Hold circuit
THD	Total Harmonic Distortion
TSD	Transient Suppression Device

Glossary

Term	Explanation
Acquisition time	*Acquisition time* is defined as the amount of time it takes a S&H to reacquire the analogue input when switching from hold to track mode. The interval starts at the 50% clock transition point and ends when the input signal is reacquired to within a specified error band at the hold capacitor.
Aperture delay	The *aperture delay* is measured from when the control signal crosses the 50% point to when the output stops following the input. Another, similar, measure that is sometimes used is the *effective aperture delay*. It is the time between when the control signal crosses the 50% point to when the input signal was equal to the held value. Aperture delay is often determined for the mid-range point of a full-scale input signal. The delay can be positive or negative, depending on whether the digital or analog path delay is longer. A positive figure means that the analog delay is shorter than the clock delay, i.e. the hold signal will be late.
Aperture jitter	*Aperture jitter* or *aperture uncertainty* is expressed as an rms time jitter. It is the result of noise modulating the phase of the hold command. The noise source can be a combination of wideband random noise, thermal noise, power supply noise and digital noise resulting from poor grounding (e.g. ground bounce).

Bandwidth	*Bandwidth* specifies the (lowest) frequency at which a S&H circuits' small-signal gain is 3dB lower than its DC gain. This definition assumes that the S&H circuit exhibits low-pass behaviour.
Capacitor soakage	see *dielectric absorption.*
Dielectric absorption	*Dielectric absorption* is a dynamic error. It refers to the fact that not all of the dielectric polarisation takes place immediately when a capacitor is charged or discharged. Consequently there can be an appreciable residual charge (voltage) with a relatively long time constant, which can affect the final capacitor voltage appreciably. *Dielectric absorption* should be taken into consideration when choosing a capacitor for precision SC applications, as the effect is influenced by the type of dielectric material used. The effect is less than 0.01% for Teflon, but may be several percent for ceramic and Mylar capacitors. The specification of this parameter is the residual voltage measured approximately one second after a capacitor is discharged (according to Ray Stata; "Operational Integrators"; Analog Dialogue; vol. 1.; no 1; April 1967; published by Analog Devices, Inc., USA).
Droop rate	*Droop rate* is the rate of change of an S&H's output voltage, when the S&H is in hold mode.

Feedthrough	*Feedthrough* is a measures for the extent to which a change in input signal is reflected at the output of the S&H, while the S&H is in hold mode.
Gain accuracy	*Gain accuracy* characterises the deviation in gain from its nominal value.
Hold-step	The step change of the output signal that can be observed during the transition from sample to hold, is known as *hold-step*. The hold-step is caused by charge being transferred from the switch and its control circuit to the hold capacitor during the switch turn-off.
Integral Non-Linearity	*Integral non-linearity* specifies the worst case deviation of the output from an ideal straight line approximation drawn through the end points of the static (or DC) transfer characteristics plot. It is commonly expressed in percent of the full-scale value of the output swing. Sometimes a best-fit straight line approximation (typically using the least-squares fit algorithm) instead of the end point straight line approximation is used.
Settling time	After the switch opens it takes the S&H some time to settle to within a specified error band around the final voltage; this is referred to as *settling time*.

Slew rate	*Slew rate* is the fastest, large-signal, rate of change that can be observed at a circuits output. It is commonly measured in V/s.
Total Harmonic Distortion	*Total harmonic distortion* is the rms sum of a signals' harmonics (2nd harmonic and higher) divided by the signals fundamental component (1st harmonic).

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Appendices

A. The MOS transistor in weak inversion.

An N-channel MOSFET is considered in weak inversion if $V_{GS} \leq V_{on}$; where V_{on} is the modified threshold voltage that applies to a MOSFET in the weak inversion region (which is also known as sub-threshold region). In reference [34] V_{on} was defined as:

$$V_{on} = V_T + nV_t .$$

Eqn. A-1

V_t is the thermal voltage ($k_BT/q \approx 25.8mV$ at 300K) and n is the process dependent sub-threshold slope factor (n is commonly in the range of between 1.0 and 3.0), which can be estimated using the following equation:

$$n = 1 + \frac{qN_{FS}}{C'_{ox}} + \frac{\gamma}{2\sqrt{2\varphi_F - V_{BS}}}$$

Eqn. A-2

Here q represents the electron charge, N_{FS} the (strongly process dependent) fast surface state density, γ the body effect parameter, C'_{ox} the Gate oxide capacitance per unit area, φ_F the Fermi potential and V_{BS} the Bulk-Source potential.

For a MOS transistor in weak inversion the total charge of the minority carriers in the channel region and consequently the Gate-Source capacitance C_{gs} decreases exponentially with the Gate-Source voltage V_{GS}. For small Drain-Source voltages V_{DS} where the proportion of the transistor's inversion layer charge associated with the Source Q_S is approximately the same as the proportion associated with the Drain Q_D the Gate-Drain capacitance C_{gd} will be approximately the same as C_{gs}. Under this condition ($Q_S \approx Q_D$) the C_{gs} in the weak inversion region (i.e. for $V_{GS} \leq V_{on}$) may be calculated using the following approximation [24]:

$$C_{gs} = C_{gsm} e^{\frac{V_{GS} - V_{on}}{nV_t}}$$

Eqn. A-3

where C_{gsm} is the Gate-Source capacitance for $V_{GS} = V_{on}$.

Since it has been established that there will be minority carriers present in the channel region in weak inversion there will also be some transport current I_{ds} flowing. Like C_{gs} this current decreases exponentially with V_{GS}:

$$I_{ds} = I_0 \left(1 - e^{-\frac{mV_{DS}}{nV_t}} \right) e^{\frac{V_{GS} - V_{on}}{nV_t}}$$

Eqn. A-4

where I_0 is the saturation current in the device on the threshold to weak inversion, i.e. at $V_{GS} = V_{on}$ with $V_{DS} \gg V_t$:

$$I_0 = \frac{\beta (nV_t)^2}{m}$$

Eqn. A-5

and m:

$$m = 1 + \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}}$$

Eqn. A-6

m is generally in the region of 1 to 2. For modern sub-micron processes $m \approx 1$ (e.g. for the AMS process, detailed in Appendix E, m = 1.41 .. 1.19 for V_{SB} = 0V .. 3.0V).

From Eqn. A-4 it becomes clear that I_{ds} saturates (i.e. becomes independent of V_{DS}) for V_{DS} greater than a few V_t ($\approx 2..3V_t$) [1] and may therefore be approximated by:

$$I_{dsat} \cong I_0 e^{\frac{V_{GS} - V_{on}}{nV_t}}$$

Eqn. A-7

For V_{DS} much smaller than that I_{ds} will decrease approximately proportional with V_{DS}:

$$I_{dlin} \cong \beta n V_t V_{DS} e^{\frac{V_{GS} - V_{on}}{nV_t}}$$

Eqn. A-8

The interested reader may wish to consult references [1] & [34] for a more detailed discussion of MOS transistor operation in the weak inversion region.

B. Derivation of the differential equation given in [6].

Solution to the differential equation of Sheu & Hu, 1984:

First the expression for i_d must be fully expanded to expose the time dependency of i_d:

$$i_d = \beta \cdot (v_{gs} - V_T) \cdot v_d$$

which expressed in terms of V_{HT} and U is:

$$i_d = \beta \cdot (V_{HT} - U \cdot t) \cdot v_d \tag{1}$$

(because of $v_{gs} = V_H - V_S - U \cdot t$ and $V_{HT} = V_H - V_S - V_T$)

To find the solution to the following differential equation (which was given in the paper)

$$C_h \cdot \frac{d}{dt} v_d = -i_d - \left(C_{ol} + \frac{C_{ox}}{2} \right) \cdot U \tag{2}$$

i_d must be substituted with the time-dependent expression (1):

$$C_h \cdot \frac{d}{dt} v_d = -\beta \cdot (V_{HT} - U \cdot t) \cdot v_d - \left(C_{ol} + \frac{C_{ox}}{2} \right) \cdot U \tag{3}$$

This is a non-homogeneous linear differential equation ("inhomogene Differentialgleichung") of the form $y' + p(x) \cdot y = q(x)$ that can be solved in a two-step operation. First the time-dependent part of the expression i.e. the homogeneous differential equation ("homogene Differentialgleichung") is solved $y' + p(x) \cdot y = 0$ then the method of variation of parameters ("Variation der Konstanten") is applied to arrive at the specific solution ("partikulaere oder spezielle Loesung") of the differential equation. See Kreyszig, pp. 33 and my own "Handgeschriebene Formelsammlung Mathematik: Zu Loesungsvefahren fuer spezielle Dgln. '-lineare Dgln.' ".

Discarding the constant term we get the time-dependent expression (homogeneous differential equation):

$$C_h \cdot \frac{d}{dt} v_d = -\beta \cdot (V_{HT} - U \cdot t) \cdot v_d$$

Bringing all terms containing v_d to one side:

$$\frac{dv_d}{v_d} = \frac{\beta \cdot U}{C_h} \cdot \left(t - \frac{V_{HT}}{U} \right) \cdot dt$$

and then integrating both sides (with respect to the respective derivative)

$$\int \frac{1}{v_d}\,dv_d = \int \frac{\beta \cdot U}{C_h} \cdot \left(t - \frac{V_{HT}}{U}\right) dt$$

yields

$$\ln(v_d) = \frac{\beta \cdot U}{2 \cdot C_h} \cdot \left(t - \frac{V_{HT}}{U}\right)^2 + K_1$$

Raising both sides into the exponent of e leads to

$$e^{\ln(v_d)} = e^{\frac{\beta \cdot U}{2 \cdot C_h} \cdot \left(t - \frac{V_{HT}}{U}\right)^2 + K_1} = e^{\frac{\beta \cdot U}{2 \cdot C_h} \cdot \left(t - \frac{V_{HT}}{U}\right)^2} \cdot e^{K_1}$$

K_1, being a constant, can for convenience be written as $K_1 = \ln(K)$, resulting in the following solution for v_d:

$$v_d(t) = K \cdot e^{\frac{\beta \cdot U}{2 \cdot C_h} \cdot \left(t - \frac{V_{HT}}{U}\right)^2} \qquad (4)$$

; here v_d is written as $v_d(t)$ to express explicitly that it is a function of time.

Now the method of variation of parameters is applied to find an expression describing K.

The following steps are involved in this process:

- first $\frac{d}{dt} v_d(t)$ must be found.
- the solution to it is then substituted into (3)
- and K is determined by integrating the resulting expression with respect to t.

To find $\frac{d}{dt} v_d$ we must differentiate (4) with respect to t. In this particular case the following steps are involved in finding the solution to the differential equation:

First the product rule is applied { K' X + X' K }:

$$\frac{d}{dt} v_d = \frac{d}{dt} K \cdot e^{a \cdot f(t)^2} = e^{a \cdot f(t)^2} \cdot \frac{d}{dt} K + K \cdot \frac{d}{dt} e^{a \cdot f(t)^2}$$

Then the chain rule is applied twice

$$\frac{d}{dt} e^{a \cdot f(t)^2} = a \cdot e^{a \cdot f(t)^2} \cdot \frac{d}{dt} f(t)^2 \quad \text{and} \quad \frac{d}{dt} f(t)^2 = 2 \cdot \frac{d}{dt} f(t)$$

before, finally, $\frac{d}{dt}f(t)$ is solved, where $f(t)=\left(t-\frac{V_{HT}}{U}\right)$ and $a=\frac{\beta\cdot U}{2\cdot C_h}$

We have now found the solution to $\frac{d}{dt}v_d$ as:

$$\frac{d}{dt}v_d=e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}\cdot\left[\frac{d}{dt}K+K\cdot\frac{2\cdot\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)\right]$$

Inserting this into (3) and solving for K (i.e. bring all terms containing K to one side of the expression) gives:

$$\left[C_h\cdot\frac{d}{dt}K+K\cdot\beta\cdot U\cdot\left(t-\frac{V_{HT}}{U}\right)\right]\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}=-\beta\cdot\left(V_{HT}-U\cdot t\right)\cdot v_d-\left(C_{ol}+\frac{C_{ox}}{2}\right)\cdot U$$

Substituting (4) for v_d gives

$$\left[C_h\cdot\frac{d}{dt}K+\beta\cdot K\cdot U\cdot\left(t-\frac{V_{HT}}{U}\right)\right]\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}=-\beta\cdot\left(V_{HT}-U\cdot t\right)\cdot K\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}-\left(C_{ol}+\frac{C_{ox}}{2}\right)\cdot U$$

which is, after bringing all the terms containing K to the left side:

$$\left[C_h\cdot\frac{d}{dt}K+\beta\cdot K\cdot\left(U\cdot t-V_{HT}\right)+\beta\cdot K\cdot\left(V_{HT}-U\cdot t\right)\right]\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}=-U\cdot\left(C_{ol}+\frac{C_{ox}}{2}\right)$$

Since $\beta\cdot K\cdot\left(U\cdot t-V_{HT}\right)+\beta\cdot K\cdot\left(V_{HT}-U\cdot t\right)=0$ this term can be written as:

$$\frac{d}{dt}K\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}=-U\cdot\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)$$

From which we derive the following expression for $\frac{d}{dt}K$:

$$\frac{d}{dt}K=-\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot U\cdot e^{\frac{-\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}$$

Integrating with respect to t we arrive at the following expression for K:

$$K = -\left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_h}\right) \cdot U \cdot \int_0^t e^{\frac{-\beta}{2 \cdot U \cdot C_h} \cdot \left(U \cdot t - V_{HT}\right)^2} dt \qquad (5)$$

; here we are using the term $\left(U \cdot t - V_{HT}\right)^2$ in the exponent since it will allow us to perform the following substitutions more easily.

Performing two consecutive substitutions of the integration variable on expression (5) leads to the desired expression for K.

The first substitution is based on the relationship

$$\int_a^b f(g(t)) \cdot \frac{d}{dt} g(t)\, dt = \int_{g(a)}^{g(b)} f(y)\, dy$$

wherein $y = g(t) = U \cdot t - V_{HT}$; $a = 0$; $b = t$ and consequently $dy = \frac{d}{dt} g(t) \cdot dt = U \cdot dt$.

This means that the following, actual, substitutions can be performed on (5):

$$U \cdot t - V_{HT} = y \quad \text{and} \quad dt = \frac{1}{U} \cdot dy$$

The new integration boundaries of (5) are now:

$$t = U \cdot t - V_{HT} \quad \text{and} \quad 0 = -V_{HT}$$

And the new expression for K (after the first substitution) is:

$$K = -\left(\frac{C_{ol} + \frac{C_{ox}}{2}}{C_h}\right) \cdot \int_{-V_{HT}}^{U \cdot t - V_{HT}} e^{\frac{-\beta}{2 \cdot U \cdot C_h} \cdot y^2} dy \qquad (5a)$$

Now the second substitution, based on the following relationships, can be made:

$$\int_\alpha^\beta f(z)\, dz = \int_{invg(\alpha)}^{invg(\beta)} f(z) \cdot \frac{d}{dy} z\, dy = \int_{invg(\alpha)}^{invg(\beta)} f(g(y)) \cdot \frac{d}{dy} g(y)\, dy$$

where

$$z = y \cdot \sqrt{\frac{\beta}{2 \cdot U \cdot C_h}}; \quad dz = \sqrt{\frac{\beta}{2 \cdot U \cdot C_h}} \cdot dy; \quad \alpha = -V_{HT}; \quad \beta = U \cdot t - V_{HT} \quad \text{and} \quad y = invg(z) = \sqrt{\frac{2 \cdot U \cdot C_h}{\beta}} \cdot z$$

Leading to the following, actual, substitutions in (5a):

$$y\cdot\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}=z \quad \text{and} \quad dy=\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot dz$$

The new integration boundaries for (5a) are now:

$$-\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot V_{HT}\ ;\ \text{for the lower boundary, and}$$

$$\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot\left(U\cdot t - V_{HT}\right);\ \text{for the upper boundary.}$$

The final expression for K is therefore:

$$K=-\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot\int_{-\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}}^{\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(U\cdot t - V_{HT}\right)} e^{-z^2}\,dz \qquad (6)$$

The same result for K could have been arrived at by just a single substitution in (5):

The transformation would again be based on the relationship

$$\int_a^b f(g(t))\cdot\frac{d}{dt}g(t)\,dt=\int_{g(a)}^{g(b)} f(y)\,dy$$

but this time $z=g(t)=\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(U\cdot t - V_{HT}\right)$ and $dz=\frac{d}{dt}g(t)\cdot dt=\frac{1}{U}\cdot\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot dt.$

Resulting in the following, new, integration boundaries:

$$t=\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(U\cdot t - V_{HT}\right) \quad \text{and} \quad 0=-\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}$$

Substituting these into (5) leads again to expression (6):

$$K=-\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot\int_{-\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}}^{\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(U\cdot t - V_{HT}\right)} e^{-z^2}\,dz$$

Since $\int e^{-z^2}\,dz = \frac{1}{2}\cdot\sqrt{\pi}\cdot\mathrm{erf}(z)$ it must follow that (6) can be rewritten as:

$$K = -\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot\sqrt{\frac{2\cdot U\cdot C_h}{\beta}}\cdot\frac{\sqrt{\pi}}{2}\cdot\left[\mathrm{erf}\left[\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(U\cdot t - V_{HT}\right)\right] - \mathrm{erf}\left(-\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}\right)\right]$$

which, because of $-\mathrm{erf}(-z)=\mathrm{erf}(z)$, can be arranged in the form

$$K = -\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot\sqrt{\frac{\pi\cdot U\cdot C_h}{2\cdot\beta}}\cdot\left[\mathrm{erf}\left[\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(U\cdot t - V_{HT}\right)\right] + \mathrm{erf}\left(\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}\right)\right]$$

or indeed as

$$K = -\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot\sqrt{\frac{\pi\cdot U\cdot C_h}{2\cdot\beta}}\cdot\left[\mathrm{erf}\left(\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}\right) - \mathrm{erf}\left[\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(V_{HT} - U\cdot t\right)\right]\right]$$

Inserting this equation for K into (4) yields the desired expression for $v_d(t)$:

$$v_d(t) = -\left(\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\right)\cdot\sqrt{\frac{\pi\cdot U\cdot C_h}{2\cdot\beta}}\cdot\left[\mathrm{erf}\left(\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}\right) - \mathrm{erf}\left[\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(V_{HT} - U\cdot t\right)\right]\right]\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}$$

which can be rewritten in the form used by Sheu & Hu, 1984:

$$v_d(t) = -\sqrt{\frac{\pi\cdot U\cdot C_h}{2\cdot\beta}}\cdot\frac{C_{ol}+\frac{C_{ox}}{2}}{C_h}\cdot e^{\frac{\beta\cdot U}{2\cdot C_h}\cdot\left(t-\frac{V_{HT}}{U}\right)^2}\cdot\left[\mathrm{erf}\left(\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot V_{HT}\right) - \mathrm{erf}\left[\sqrt{\frac{\beta}{2\cdot U\cdot C_h}}\cdot\left(V_{HT} - U\cdot t\right)\right]\right]$$

C. Examples of CLFT compensated circuits.

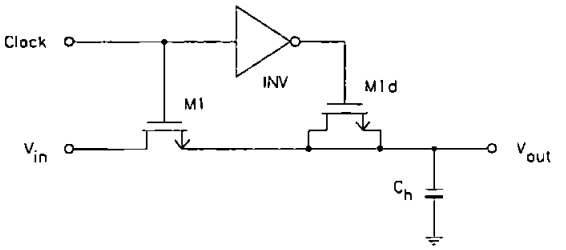


Fig. C-1: Dummy compensated open-loop track-and-hold circuit [39], [40].

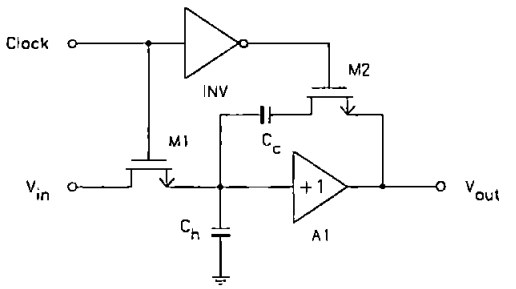


Fig. C-2: Clock-feedthrough compensated open-loop S&H amplifier ('Watanabe circuit') [46].

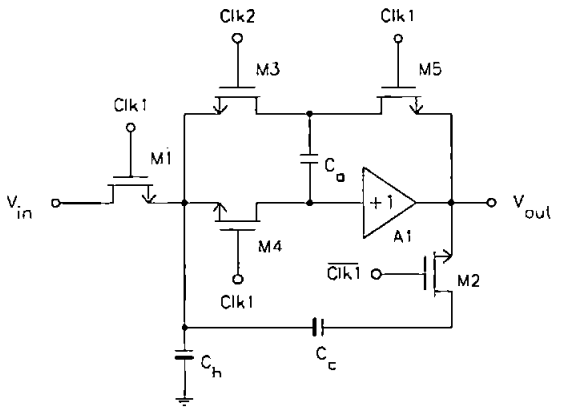


Fig. C-3: Gain-error, offset and clock-feedthrough compensated version of the 'Watanabe circuit' [46].

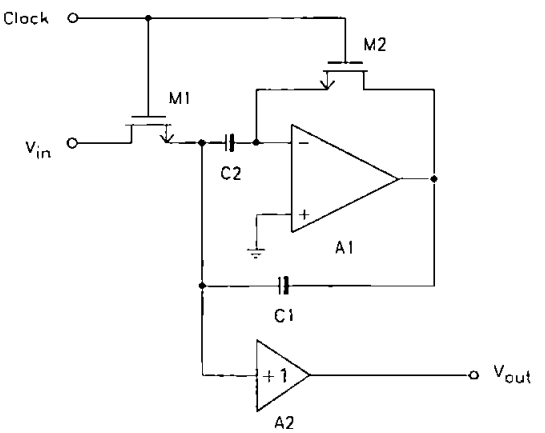


Fig. C-4: Miller-enhanced track-and-hold circuit [50].

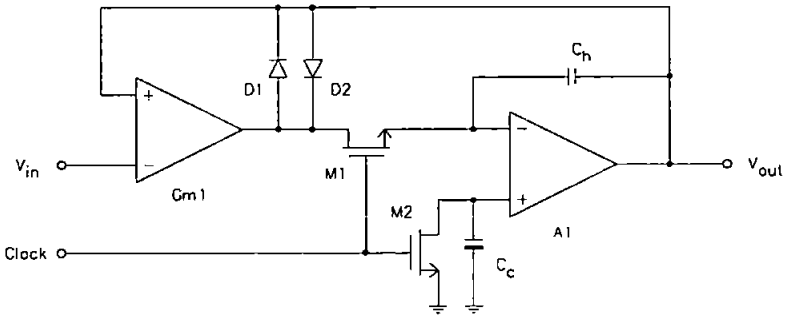


Fig. C-5: Clock-feedthrough compensated integrator-type track-and-hold amplifier [45].

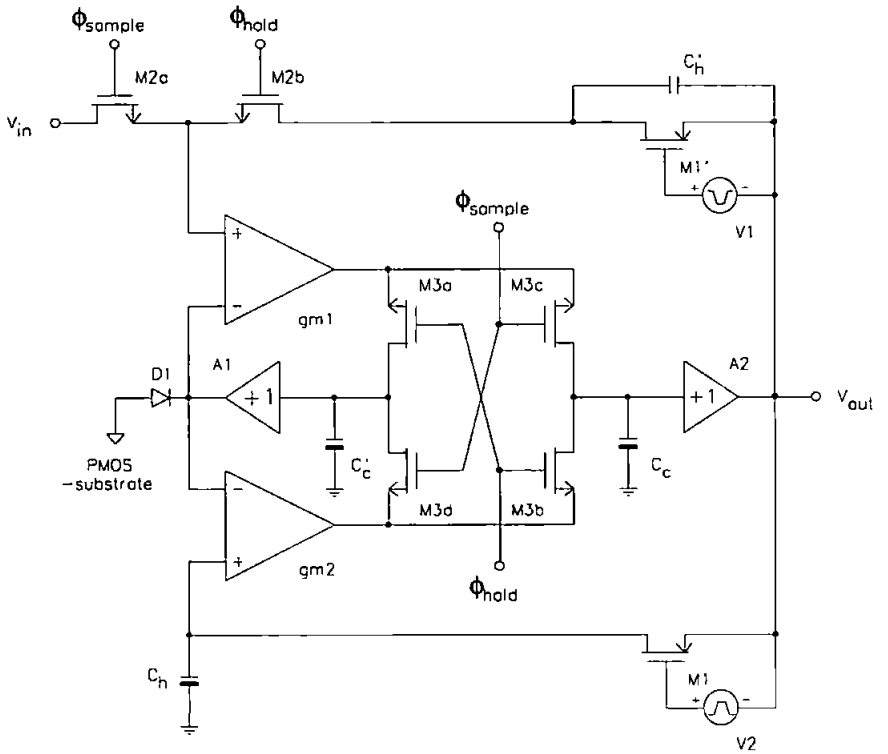


Fig. C-6: S&H amplifier [35].

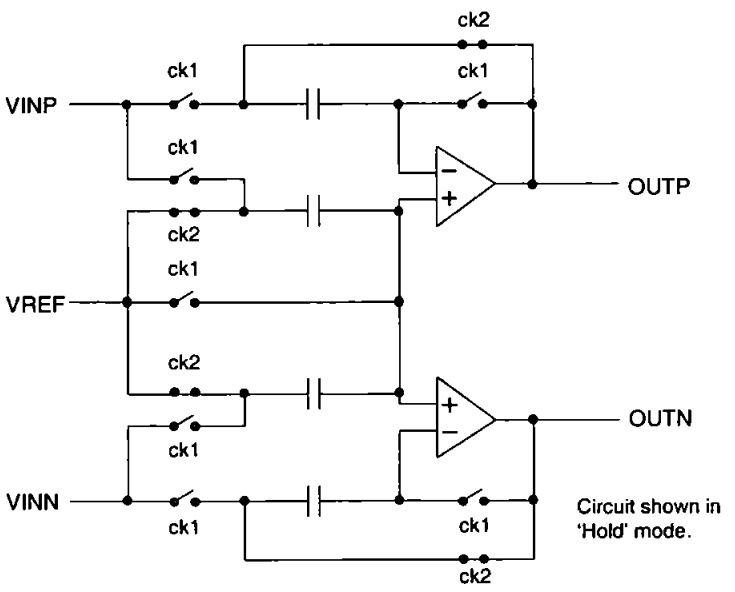


Fig. C-7: Fully differential T&H circuit.

D. Schematics of the test circuit using discrete devices.

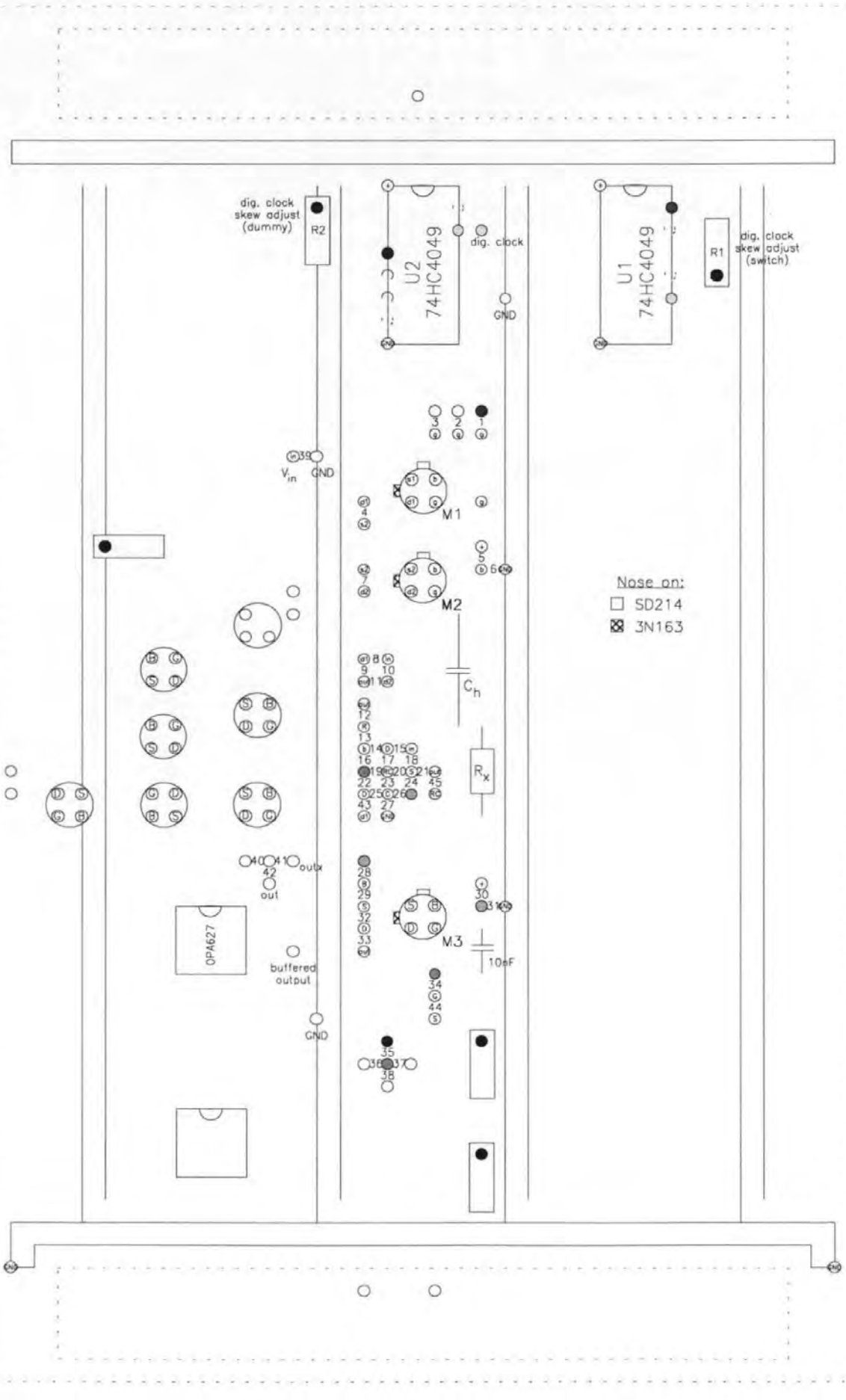


Fig. D-1: Board layout of test circuit using discrete devices.

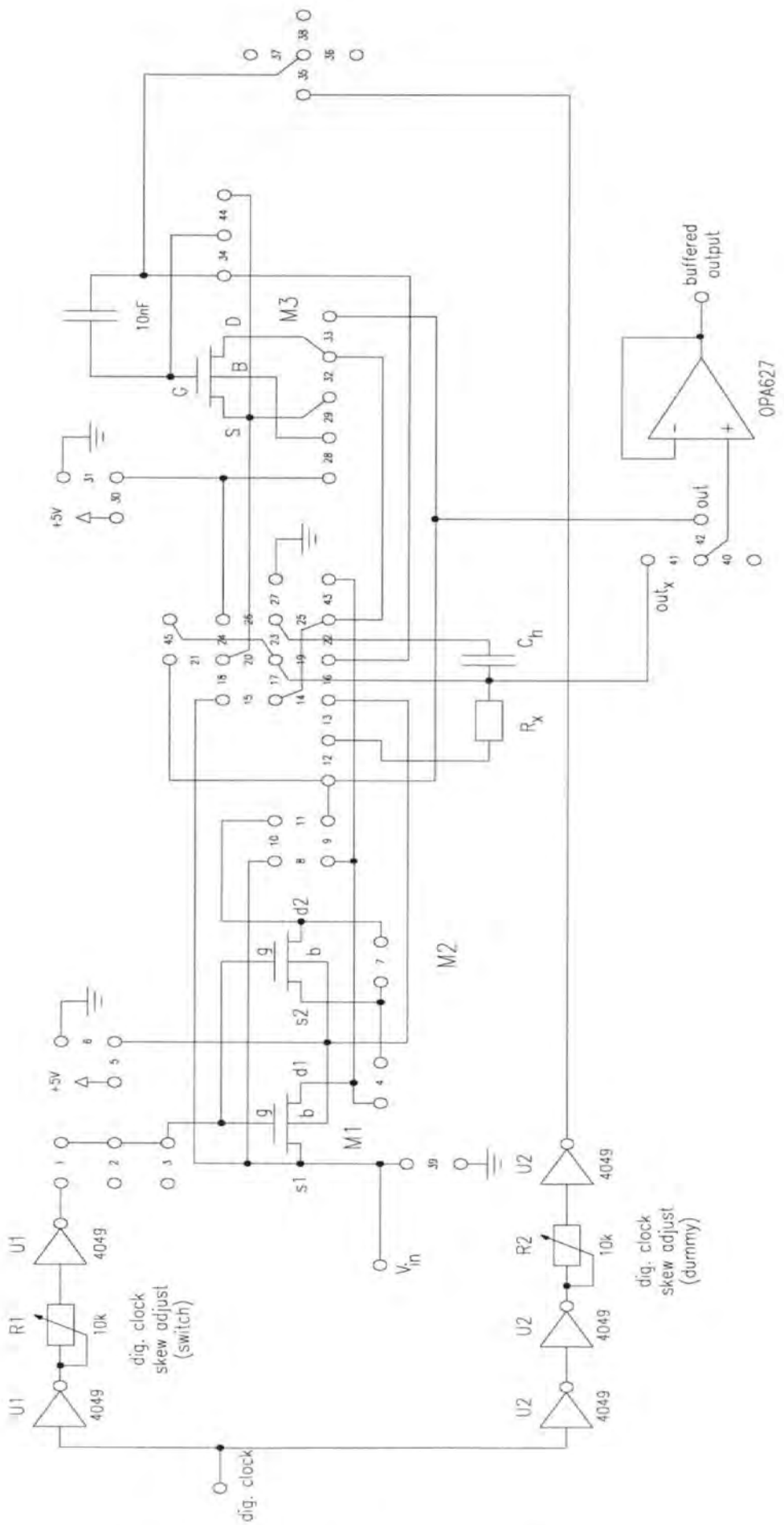


Fig. D-2: Schematic of the test circuit using discrete devices.

How to set the jumper links for configuring the board

Size of the switching device:	N-MOSFET	P-MOSFET
W=1, L=1	6, 7, 9	5, 7, 9
W=1, L=2	6, 4, 11	5, 4, 11
W=2, L=1	6, 4, 9, 10	5, 4, 9, 10

Compensation circuit:	N-MOSFET	P-MOSFET
No compensation	27, 45, (31, 24, 28, 32, 44/{34&35*})[a]	27, 45, (30, 24, 28, 32, 44/{34&35*})[a]
"half-width dummy"	31, 17, {21&33}[b], 27+, 28, 34, 35*	30, 17, {21&33}[b], 27+, 28, 34, 35*
"half-length dummy" open source	31, 45+17+33[c], 27+, 28, 34, 35*	30, 45+17+33[c], 27, 28, 34, 35*
"half-length dummy" open drain	31, 45, 20, 27+, 28, 34, 35*	30, 45, 20, 27, 28, 34, 35*
CMOS, uncompensated	N.A.	30, 17+45[d], 18, 27, 28, 33, 34, 35*
No. 1	31, 42, 19, 24, 25, 28[e], 34[f], 45	30, 19, 24, 25, 28[e], 34[f], 42, 45
No. 2	31, 22, 20, 27+, 28[e], 33, 34[f]	30, 20, 22, 27/26, 28[e], 33, 34[f]
No. 3	(31), 20, 22, 27, 29[e], 33, 34[f]	30, 20, 22, 27/26, 29[e], 33, 34[f]
No. 4	12, 27, (31, 24, 28, 32, 44/{34&35*})[a]	12, 27, (31, 24, 28, 32, 44/{34&35*})[a]
No. 5	31, 16, 20, 27+, 28, 33, 34	30, 16, 20, 27, 28, 33, 34
No. 6 (switch: W=1, L=2)	(31), 18, 27, 29, 43, 44, 45	(30), 18, 27, 29, 43, 44, 45
No. 7 (switch: W=1, L=2)	31, 18, 27+, 28, 43, 44, 45	30, 27, 28, 43, 43,.44, 45
No. 8 (switch: W=1, L=2)	31, 24, 27, 28, 43, 44, 45	30, 24, 27, 28, 43, 44, 45

Notes:

Normally jumper 41 will be closed to connect 'out_x' to the input of the buffer amplifier.

It is advisable to set the jumpers in ( ) to keep changes in the layout to a minimum. They are not necessary for the functioning of the circuit.

[a] leaving jumper 31(*30*) open will take M3 completely out of the circuit; jumper 44 must be closed.
with jumper 31(*30*) closed and:
-jumper 44 closed (34 and 35 open), all terminals of M3 are connected to GND (+5*V*).
-jumper 34 and 35* closed (44 open), the gate of M3 is then connected to the dummy clock and all other terminals of M3 are connected to GND (+5*V*).

[b] instead of jumpers 21&33 jumpers 21&32 or 32&45 could be closed.

[c] the three jumpers can be closed in the following configurations:
17&33, 45&17, 45&33, **45&17&33**

[d] jumper 17 or 45 or 17&45 set.

[e] instead of the jumper a voltage source may be inserted. Here it is used to change the bulk potential and therefore the level of inversion, i.e. the channel resistance can be changed.

[f] if a voltage source instead of a jumper is inserted the gate voltage of M3 can be controlled. This has the same effect as if the threshold voltage of the device was changed.

* Here complementary clocks are used. In case of
digital clock: jumpers 1 and 35
"analogue clock": jumpers 2 and 36
need to be closed.

+ for a NMOS "compensating" device jumper 26 could be closed instead. This should not make any difference. The reason being that jumper 27 connects the capacitor directly to GND, whereas jumper 26 makes a connection to the bulk terminal of the "compensating" device (which, in the case of a NMOS device, is tied to the lowest potential in a circuit, i.e. GND).

E. Important parameters of the AMS 0.8μm process (CYE).

Important parameters of the AMS 0.8µm twin well, double poly, double metal mixed-signal CMOS process (CYE) on p-epi substrate.

Parameter	NMOS	PMOS
Min. transistor width (drawn; electrical)	2µm; W_{eff} = 1.2±0.4µm (33%)	2µm; W_{eff} = 1.2±0.4µm (33%)
Min. transistor length (drawn; electrical)	0.8µm; L_{eff} = 0.66±0.11µm (17%)	0.8µm; L_{eff} = 0.79±0.11µm (14%)
Typ. V_{T0} at W/L = 2µ/0.8µ; 20µ/0.8µ; 20µ/20µ	0.75V; 0.72±0.10V; 0.82±0.07V	-0.74V; -0.71±0.08V; -0.75±0.06V
Surface mobility, μ_0	463cm^2/Vs	167cm^2/Vs
Body effect γ for a 20µ/20µ device	0.73±0.09V^{½}	0.45±0.04V^{½}
Charge carrier channel transit time, $\tau_0 = L^2/\mu(V_{GS}-V_T)$	23.1ps×V/µm^2	64.6ps×V/µm^2
Well doping density, N_{SUB}	7.4×10^{16} 1/cm^3	2.8×10^{16} 1/cm^3
Fast surface state density, N_{FS}	0.835×10^{12} 1/cm^{2}V	0.483×10^{12} 1/cm^{2}V
sub-threshold slope factor, n	2.03 .. 1.81 for V_{SB} = 0V .. 3V	1.63 .. 1.49 for V_{BS} = 0V .. 3V
Gate oxide capacitance per unit area, C'_{ox} (t_{ox} = 16±1nm)	2.16±0.13fF/µm^2 (6%)	2.16±0.13fF/µm^2 (6%)
Gate-Source overlap capacitance, C_{GSO}	0.35±0.1fF/µm (29%)	0.35±0.1fF/µm (29%)
Gate-Drain overlap capacitance, C_{GDO}	0.35±0.1fF/µm (29%)	0.35±0.1fF/µm (29%)
Gate-Bulk overlap capacitance, C_{GBO}	0.15±0.03fF/µm (20%)	0.15±0.03fF/µm (20%)
Max. Source-Bulk capacitance, C_{SB0}	0.29fF/µm^2 + 0.23fF/µm	0.49fF/µm^2 + 0.21aF/µm
Gate cap. of a min. size transistor in saturation (V_{GS} = 5V, V_{DS} = 0V, V_{BS} = 0V)	C_{ox} = 1.71fF, C_{ol} = 0.7fF	C_{ox} = 2.05fF, C_{ol} = 0.7fF
'ON-resistance' of a min. size transistor (V_{GS} = 5V, V_S = 0V, V_{DS} = 1mV)	2.5kΩ	8.3kΩ
Saturation current, L = 0.8µm ($\|V_{GS}\|$ = 5V, $\|V_{BS}\|$ = 0V & $\|V_{DS}\|$ = 5.5V)	400µA/µm	195µA/µm
Minimum $V_{DS,breakdown}$, L = 0.8µm	9V	-8V

Note: Typical Reverse Breakdown Voltages are: N^+ to P^- = 17V, P^+ to N^- = 15V and N^- to P^- = 45V
Minimum Breakdown Voltages: Gate oxide = 12V, Poly2-Poly1 = 20V

Type	Area Capacitance	Perimeter Capacitance
Poly2 - Poly1 (Oxide thickness: 19.5±1.5nm)	1.77+0.15-0.12fF/µm2 (8%)	0.2±0.01fF/µm (5%)
Poly - Substrate	66±5aF/µm^2 (8%)	48±2aF/µm (4%)
Ratio of Poly - Poly to parasitic capacitance	27 : 1	4.2 : 1
Metal1 - Substrate	29.5±2.5aF/µm^2	43.5±1.5aF/µm
Metal2 - Substrate	16.5±2.5aF/µm^2	42±3aF/µm
Metal1 - Metal2	35+9-7aF/µm^2	51.5±4.5aF/µm
Metal1 - Poly1	53.5±4.5aF/µm^2	51±2aF/µm
Metal2 - Poly1	21+5-3aF/µm^2	45±3aF/µm

Note: Typical coupling capacitances between two parallel shapes at min. spacing are
Poly1 = 40aF/µm, Metal1 = 50aF/µm & Metal2 = 70aF/µm

Type	Sheet Resistance	Temperature Coefficient
Poly1 resistance	23+5-3Ω/□ (+22-13%)	0.9 10^{-3} 1/K
Poly2 resistance	27±6Ω/□ (±22%)	0.8 10^{-3} 1/K
N-well resistance	1.2k±0.2kΩ/□ (±17%)	6.5 10^{-3} 1/K

Comparison of measured batch data from the actual production run of the UoP01FXF test chip to process specification parameters for the AMS 0.8μm double poly, double metal CMOS process (CYE).

NMOS transistor	Measured for batch	Specification, typical
Effective width for 2μm drawn, W_{eff}	1.250μm	1.2μm
Effective length for 0.8μm drawn, L_{eff}	0.613μm	0.66μm
Poly field threshold voltage	15V	>12V
V_{T0} for W/L = 20μ/0.8μ	0.638V	0.72V
V_{T0} for W/L = 20μ/20μ	0.841V	0.82V
Substrate doping density, $N_{SUB} = (\gamma C'_{ox})^2/2q\varepsilon_{Si}$	7.81×10^{16} 1/cm^3	7.4×10^{16} 1/cm^3
Body effect γ for a 20μ/20μ device	0.756V^{½}	0.73V^{½}
Surface mobility, $\mu_0 = KP/C'_{ox}$	463.8cm^2/Vs	463cm^2/Vs
Transconductance coefficient, $KP = \mu C'_{ox}$	98.8μS/V	100μS/V
Gate oxide capacitance per unit area, $C'_{ox} = \varepsilon_{ox}/t_{ox}$	2.130fF/μm^2	2.16fF/μm^2
Gate oxide thickness, t_{ox}	16.2nm	16nm
Saturation current, L = 0.8μm ($\|V_{GS}\|$ = 5V, $\|V_{BS}\|$ = 0V & $\|V_{DS}\|$ = 5.5V)	421μA/μm	400μA/μm
$V_{DS,breakdown}$ for L = 0.8μm	14.2V	13.0V

Poly2 - Poly1 capacitor	Measured for batch	Specification, typical
Area capacitance	1.766fF/μm^2	1.77fF/μm^2
Oxide thickness	19.56nm	19.5nm

Sheet Resistance	Measured for batch	Specification, typical
Poly1	23.4Ω/□	23Ω/□
Poly2	26.5Ω/□	27Ω/□
N-well	1.14kΩ/□	1.2kΩ/□

Sheet Geometry data	Measured for batch	Specification, typical
Poly1 width	0.793μm	0.81μm
Poly2 width	1.89μm	1.9μm
N-well width	3.07μm	3.3μm

F. Floorplan and pin assignment for the custom IC.

Floorplan for the Test Chip UoP01FXF

The floorplan to the experimental IC, shown in Fig. F-1, reveals the locations of the different cells on the die.

The pad cells, corner cells and the *Control Word Register's* nuclear cells (DFAQ, NA2 & IN1) are proprietary 5V digital standard cells for the AMS 0.8µm CMOS process (CYE). These cells were supplied with the AMS HitKit for Mentor Graphics.

All other cells were designed and laid out by the author. The circuit diagrams of these full-custom cells are located further in the back of this section.

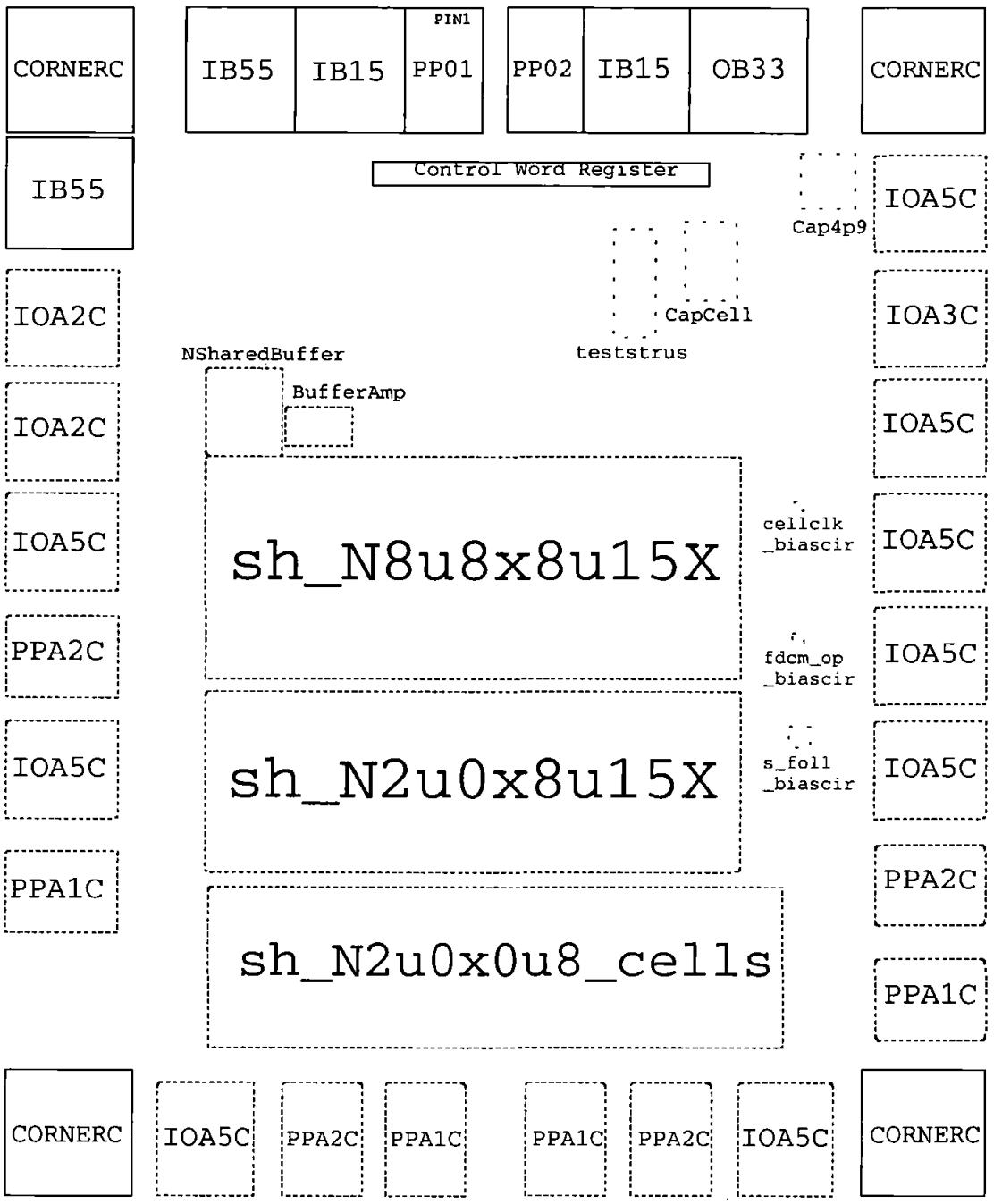


Fig. F-1: Floorplan for the test chip.

Pin-Assignment for the Test Chip UoP01FXF

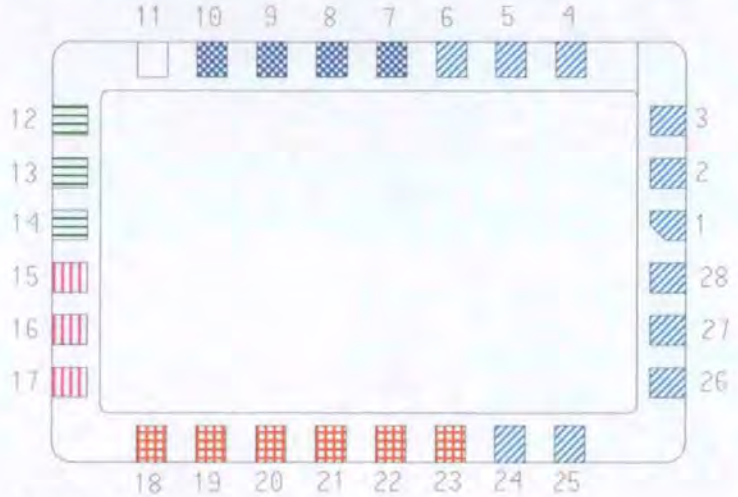


Fig. F-2: Pinout for the test chip.

Pin	Port	Function
1	CLKGND *	GND for the 'control word register', clock circuits ('_clk'),'CapCell' & 'teststrus'.
2	Din	Serial input of the *control word*.
3	EN	Enable input. H = setup determined by *control word*. L = all test circuits disabled.
4	Reset	Reset input. L = all Bits of the *control word* are set to L.
5	preclk ◊	Connects to all circuits whose names end in '_Bal', '_RGND', '_RCh' & 'teststrus' and to the input impedance controlled subcircuits (from now on referred to as '_RIn').
6	clk +	The signal the S&H gate signal is derived from.
7	Cap ♣	Connects to all '_Bal' blocks and to the outputs of the separate top level 'BufferAmp' and 'NSharedBuffer' circuits (which were included for performance evaluation).
8	5VBuf	VDD supply for the circuit select function ('Sel' port) on all 'fdcm_op_Isink' blocks.
9	IN	Signal input to all S&Hs and toplevel cells 'teststrus', 'NSharedBuffer' & 'BufferAmp'.
10	AGND *	GND input to the analogue part of the S&H circuits (excluding Buffer amplifiers)
11	Substrate *	This Pin is bonded to the chip substrate (the back of the chip), not to a pad on the chip!
12	out1 ♥	Output from the 'basic S&H', '_PCap' and the left side of the '_Bal' circuit blocks. Also output for the 'sh_N2u0x8u15_RGND' and 'sh_N8u8x8u15_RGND' blocks.
13	6VBuf1	VDD supply for the output buffer stages connected to **out1**.
14	Buf1GND *	GND for the **out1** output buffer stages ('BufferAmp' blocks).
15	Buf2GND *	GND for the **out2** output buffer stages ('BufferAmp' blocks).
16	6VBuf2	VDD supply for the output buffer stages connected to **out2**.
17	out2 ♥	Output from the '_RCh', '_RIn' and right side of the '_Bal' circuit blocks. Also output for the 'sh_N2u0x0u8_RGND' block.
18	SFGND *	GND for the first stage of all the buffer chains (wired to **Vs** port on all 's_foll' blocks).
19	6VSF	VDD supply of the first stage in all buffer chains (the **Vd** port on the 's_foll' blocks).
20	SFBias	Bias input for all PMOS source followers ('s_foll'). Draw 100 to 300µA from pin.
21	BufBias	Bias input for all output buffers ('BufferAmp'). Inject 50 to 100µA into pin.
22	ClkSpeed	Fall rate adjust for all local clock generators. Inject up to 2mA into pin.
23	capin ♣	Wired to all '_Bal', '_PCap' circuit blocks and to the 'teststrus' block.
24	clkprobe	Clock sense output. A 50÷1 (approx.) capacitive divider connected to the gate of the active S&H switch. Output capacitance is about 5pF.
25	1V •	Wired to the **Cap** port on the 'CapCell' block AND ALSO supplying 1V to the inverters driving the **Sel** port on all the 's_foll' blocks. APPLY GND TO 6VSF AND SFBias WHILE ACCESSING 'CapCell'.
26	Dout	Serial output of the *control word*. (Read *control word* back for verification purposes).
27	DClk	Data clock. The *control word* is transferred serially into, and out of, the 15-Bit FIFO control register. Data is accepted on the rising edge of DClk.
28	5VClk	VDD supply to 'control word register', clock circuits ('_clk'),'CapCell' & 'teststrus'.

Notes:

!!! Signals applied to the IC must not exceed 5V or GND !!!
(The power lines 6VSF, 6VBuf1 & 6VBuf2 are the only lines that may carry up to 6V).

The different patterned pin/pad symbols on the drawing of the bonding pad arrangement indicate the separate I/O groups. Input signal range for each group's signal pads is determined by the potentials applied to the group's power supply pads. The protection diodes on the signal pads will clamp signals to each group's respective supply potentials.

* All GND lines/pads are tied together in two ways: Directly, via the chips' scribe line metalisation and indirectly, via the substrate (the lowest potential in the circuit must be connected to the P-substrate).

+ clk:

⇒ *Local* Bit = H: The falling edge is locally generated and the clock signal applied to the S&H gate is inverted relative to the clk input.

⇒ *Local* Bit = L:

- For '_RCh' circuits the gate signal is inverted with respect to clk.
- For any other circuit clk gets applied directly to the S&H gate, i.e. its not being modified at all.

◊ preclk:

⇒ If any '_Bal' block is selected: Apply a clock with a very slow fall rate to isolate the balanced S&H from the signal input **IN** before actually switching the S&H off (with the **clk** input).

⇒ With a '_RGND' block selected: The current into the **preclk** pin controls the resistance of the transistor connecting the S&H's hold capacitor to GND.

⇒ With an '_RIn' block selected: The current into the **preclk** pin controls the ON resistance of the transistor on the input side of the S&H switch (i.e. increased impedance of the signal source). Current is returned via the **IN** pin.

⇒ With a '_RCh' block selected: The current into the **preclk** pin controls the ON resistance of the S&H's switch. Current is returned via the **IN** pin.

⇒ For the 'teststrus' selected: Same as for '_RCh', however both terminals of the switch are externally available (**IN** & **capin**).

Currents up to 0.5mA, at potentials up to 5V, may be injected into the preclk pin. This input is clamped to 5VClk and CLKGND via the pads input protection circuit.

♠ Cap:

⇒ For a '_Bal' block selected this pin controls the switch that connects the reference capacitor to the hold-capacitor on the right-hand side of the S&H arrangement (H: ref. cap. is connected).

⇒ Output for the top level 'BufferAmp' cell.

⇒ Output for the top level 'NSharedBuffer' cell.

♥ out1 & out2:

⇒ See the *control word* selection matrix for which output gets activated when.

♣ capin:

⇒ On the '_PCAP' block the pin is wired to the B, S & D terminals of the PMOS transistor that is acting as the hold capacitor in this circuit.

⇒ The bottom plate of the '_Bal' blocks reference capacitor (0.1pF) is wired to this pin.

⇒ For the 'teststrus' this is the output pin of the respective R_{ON} controlled switch.

♦ 1V:

⇒ supply for the inverters driving the **Sel** port on all the 's_foll' blocks.

⇒ connected to the selected plate of a 4.9pF capacitor (49 × 0.1pF capacitor array) while the 'CapCell' block is selected.

CAUTION: The source follower circuits ('s_foll') may accidentally get turned on while performing parameter extraction on the 'CapCell'. In this case a great many circuits may draw substantial bias current which could cause the IC to overheat. Thus, when evaluating 'CapCell', it is best to tie 6VSF and SFBias to GND; in which case all internal nodes (in the inverters driving the **Sel** port on the 's_foll' blocks, the 's_foll' and the 's_foll_biascir' blocks) other than 1V will be at GND potential, preventing any part of these circuits from turning on so long as none of these gets selected via an incorrectly set *control word*.

The Control Word

The *control word* is 15 Bits long. Each Bit controls one line of the ICs internal control bus. The 15 lines on the bus are, in this order, *Local!*, *Col1!* to *Col8!* and *Row1!* to *Row6!*. Here the exclamation mark '!' at the end of a name indicates that the signal is low-active.

- *Local!* is set by the *control words* left-most Bit (the last to be clocked in). It indicates whether the falling edge of the clock shall be generated locally, or whether the external clock signal, *clk*, is applied directly to the S&H gate. It is generated locally if the corresponding Bit of the *control word* is set (H).
- *Col1!* to *Col8!* are set by the *control words* next eight Bits.
- *Row1!* to *Row6!* are set by the *control words* final six Bits.

Please note that the *control word* is inverted before being applied to the control bus. Thus if the *Local* Bit in the *control word* is H the *Local!* line will be L and therefore active.

Circuit Selection Matrix

The different circuits on the chip are selected by setting the appropriate Bits in the command word. The effect of the different Bits on the circuit configuration are as follows:

- *Row5* selects the toplevel cell 'BufferAmp'. No other line/Bit is involved in this selection.
- *Row6* selects the toplevel cell 'NSharedBuffer'. No other line/Bit is involved in this selection.
- *Col8* is not connected (N.C.) to any circuit, i.e. is redundant.
- All other cells are addressed in cross-bar fashion - a selection is made by activating one *Row* and one *Col* line/Bit. The matrix below shows what circuit is addressed by which combination.

Col / Row	1	2	3	4	5	6	7
1 sh_N2u0x0u8	out1 & out2 _Bal, sym.	N.C.	out1 S&H	out2 _RGND	out1 _PCap	out2 _RCh	N.C.
2 sh_N2u0x8u15	out1 & out2 _Bal, sym.	out1 & out2 _Bal, asym.	out1 S&H	out2 _RIn	out1 _PCap	out2 _RCh	out1 _RGND
3 sh_N8u8x8u15	out1 & out2 _Bal, sym.	out1 & out2 _Bal, asym.	out1 S&H	out2 _RIn	out1 _PCap	out2 _RCh	out1 _RGND
4	Top Plate CapCell	Bottom Plate CapCell	N.C.	25u0x1u5 teststrus	8u8x8u15	2u0x8u15	2u0x0u8

Notes:

No precautions have been taken to prevent multiple-circuit selections. It is therefore, in principle, possible to activate all cells together by setting all Bits in the command word H. This causes permanent damage to the circuit and must be avoided.

!!! SELECTION OF MORE THAN ONE CIRCUIT MAY RESULT IN THE DESTRUCTION OF THE IC !!!

sym.:

refers to the symmetrical arrangement of the bulk contacts around the device. A guardring type bulk contact implant was employed to collect as many of the charge-pumping generated charges as possible. Due to the symmetrical nature of the hold capacitor arrangement and the bulk implant CLFT should be identical on both hold capacitors (balanced), regardless of switching speed.

asym.:

refers to the asymmetrical arrangement of the bulk contacts around the device. The bulk contact forms a U shape enclosing only the switches Source implant. It is expected that this arrangement will display a different charge-pumping behaviour, i.e. that for higher switching speeds CLFT on the two hold capacitors should become unbalanced, as different amounts of charge get diverted from the source end and from the drain end of the switch to the bulk/substrate.

List of signals that may be applied to the IC.

Port / Cell	RCL Bit#s	Din	EN	Reset	preclk	clk	Cap	IN	Substrate	out1	out2	6VSF	SFBias	BufBias	ClkSpeed	capin	clkprobe	IV	Dout	DClk
Pin Number	-	2	3	4	5	6	7	9	11	12	17	19	20	21	22	23	24	25	26	27
RESET	-	x	x	L	x	x	x	x	x	z	z	x	x	x	x	x	z	x	L	x
Control Word Transfer	-	D_n	L	H	x	x	x	x	x	z	z	x	x	x	x	x	z	x	D_{15}	↑
2u0x0u8_sym	11s	L	H	H	$c_{\searrow}$	ck	H/L	V_{in}	G/Z	q	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	v_c	↓	IV	D_{15}	L
2u0x0u8_S&H	13s	L	H	H	x	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
2u0x0u8_RGND	14s	L	H	H	$I_{\rightarrow}$	ck	x	V_{in}	G/Z	z	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
2u0x0u8_PCap	15s	L	H	H	x	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	5V	↓	IV	D_{15}	L
2u0x0u8_RCh	16s	L	H	H	$I_{\rightarrow}$	c↑	x	V_{in}	G/Z	z	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
2u0x8u15_sym	21s	L	H	H	$c_{\searrow}$	ck	H/L	V_{in}	G/Z	q	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	v_c	↓	IV	D_{15}	L
2u0x8u15_asym	22s	L	H	H	$c_{\searrow}$	ck	H/L	V_{in}	G/Z	q	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	v_c	↓	IV	D_{15}	L
2u0x8u15_S&H	23s	L	H	H	x	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
2u0x8u15_RIn	24s	L	H	H	$I_{\rightarrow}$	ck	x	V_{in}	G/Z	z	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
2u0x8u15_PCap	25s	L	H	H	x	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	5V	↓	IV	D_{15}	L
2u0x8u15_RCh	26s	L	H	H	$I_{\rightarrow}$	c↑	x	V_{in}	G/Z	z	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
2u0x8u15_RGND	27s	L	H	H	$I_{\rightarrow}$	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
8u8x8u15_sym	31s	L	H	H	$c_{\searrow}$	ck	H/L	V_{in}	G/Z	q	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	v_c	↓	IV	D_{15}	L
8u8x8u15_asym	32s	L	H	H	$c_{\searrow}$	ck	H/L	V_{in}	G/Z	q	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	v_c	↓	IV	D_{15}	L
8u8x8u15_S&H	33s	L	H	H	x	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
8u8x8u15_RIn	34s	L	H	H	$I_{\rightarrow}$	ck	x	V_{in}	G/Z	z	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
8u8x8u15_PCap	35s	L	H	H	x	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	5V	↓	IV	D_{15}	L
8u8x8u15_RCh	36s	L	H	H	$I_{\rightarrow}$	c↑	x	V_{in}	G/Z	z	q	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
8u8x8u15_RGND	37s	L	H	H	$I_{\rightarrow}$	ck	x	V_{in}	G/Z	q	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	$I_{\rightarrow}$	x	↓	IV	D_{15}	L
CapCell Top Plate	41x	L	H	H	x	x	x	x	G/Z	z	z	0V	x	x	x	x	z	C_x	D_{15}	L
CapCell Bottom Plate	42x	L	H	H	x	x	x	x	G/Z	z	z	0V	x	x	x	x	z	C_x	D_{15}	L
teststrus 25u0x1u5	44x	L	H	H	$I_{\rightarrow}$	x	x	V_{in}	G/Z	z	z	6V	x	x	x	R_{ON}	z	IV	D_{15}	L
teststrus 8u8x8u15	45x	L	H	H	$I_{\rightarrow}$	x	x	V_{in}	G/Z	z	z	6V	x	x	x	R_{ON}	z	IV	D_{15}	L
teststrus 2u0x8u15	46x	L	H	H	$I_{\rightarrow}$	x	x	V_{in}	G/Z	z	z	6V	x	x	x	R_{ON}	z	IV	D_{15}	L
teststrus 2u0x0u8	47x	L	H	H	$I_{\rightarrow}$	x	x	V_{in}	G/Z	z	z	6V	x	x	x	R_{ON}	z	IV	D_{15}	L
BufferAmp	5xx	L	H	H	x	x	q	V_{in}	G/Z	z	z	6V	x	$I_{\rightarrow}$	x	x	z	IV	D_{15}	L
NSharedBuffer	6xx	L	H	H	x	x	q	V_{in}	G/Z	z	z	6V	$I_{\leftarrow}$	$I_{\rightarrow}$	x	x	z	IV	D_{15}	L

Table F-1: Signals to and from the IC.

Notes:

- All GND pins (pin number: 1, 10, 14, 15 & 18, i.e. ports: CLKGND, AGND, Buf1GND, Buf2GND & SFGND) must be connect to GND at all times.
- +5V power pins (pins number 8 & 28, i.e. ports 5VBuf & 5VClk) must always be supplied with +5V.
- +6V power pins (number 13 & 16, i.e. ports 6VBuf1 & 6VBuf2) must always be supplied with +6V.
- Normal typeface indicates an input type or a passive-type port.
- *Italics indicate an active-output type port.*
- **Boldface indicates a bi-directional port; i.e. one which, depending on the control word, may either be input or output.**

Legend to Table F-1:

RCL — The first number of the "RCL Bit#s" stands for the 'Row' number, followed by the 'Col' number that must be selected to activate a particular cell. It concludes with the 'Local' bit. Bit order in the "RCL", starting with the MSB, is: R6 R5 R4 | R3 R2 R1 C8 | C7 C6 C5 C4 | C3 C2 C1 Local.
(E.g. to select the 2u0x0u8_PCap cell the control word must be 220h (hexadecimal) for Local = L and 221h for Local = H).
CARE MUST BE TAKEN TO SELECT ONLY ONE CELL, THE IC MIGHT GET DESTROYED OTHERWISE.

s — set 'Local' bit to logic H to enable the internal (local) ramp generator.

I← — Current injected into the pin.

I→ — Current flowing out of the pin.

↑ — Data is accepted on the rising edge of the clock.

↓ — The falling edge of the S&H gate signal appears on this, passive, output.

$c_{\searrow}$ — A clock with a slow falling edge. The transition must settle before the main clock may change state.

c↑ — The S&H gate signal is inverted to the clk input signal (track-hold transition on ↑ of clk input).

ck — The main clock:
Local = L: The clk input signal is applied directly to the S&H gate (track-hold transition on ↓ of clk input).
Local = H: The S&H gate signal is "local" and inverted with respect to the clk input signal (track-hold transition on ↑ of clk input).

L — Logic L (GND)

H — Logic H (+5V)

H/L — Either H or L may be applied to the pin. With 'H' applied an additional 0.1pF capacitor is switched in between the output side of the '_sym' or '_asym' circuit that is selected and the 'capin' pin. With 'L' applied the additional capacitor is removed and the '_sym' or '_asym' circuit is now exactly symmetrical with regards to the circuit elements connected to the pass-transistor drain and source.

G/Z — Pin may be grounded or left floating.

z — *An output in a high impedance state.*

q — *An active output.*

x — Means either an undetermined output or a 'don't care' input.

v_c — Depending on the test, either a DC or AC voltage may be applied to this pin.

C_x — The capacitance of the device under test may be measured on this pin.

R_{ON} — The ON resistance of the device under test may be measured between this and the IN pin.

Please refer to the section "Pin-Assignment for the test chip" for further information on the different uses that the IC pins have.

G. Schematics of the custom integrated circuit.

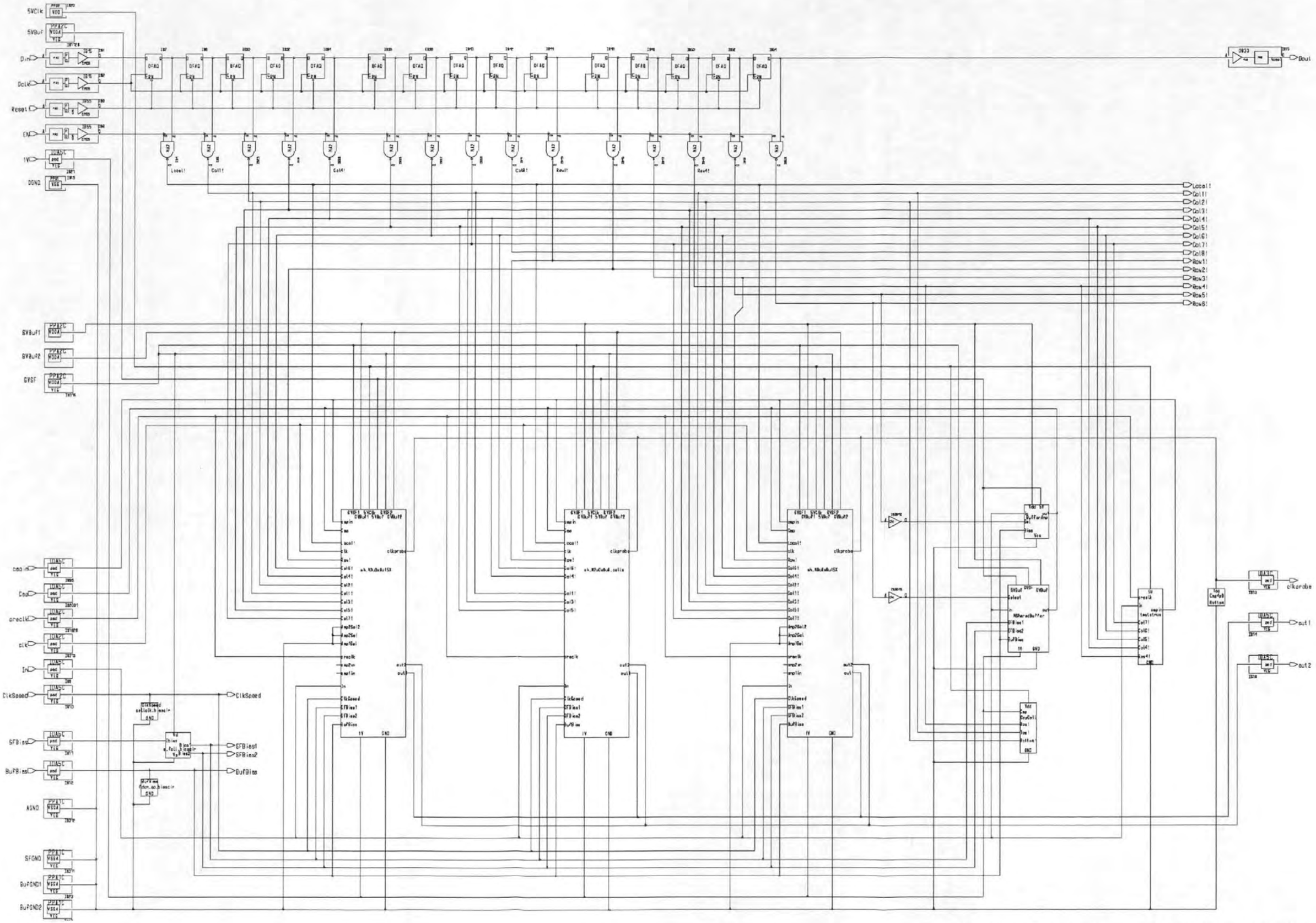


Fig. G-1: Top-level schematic of the test chip, UoP01FXF

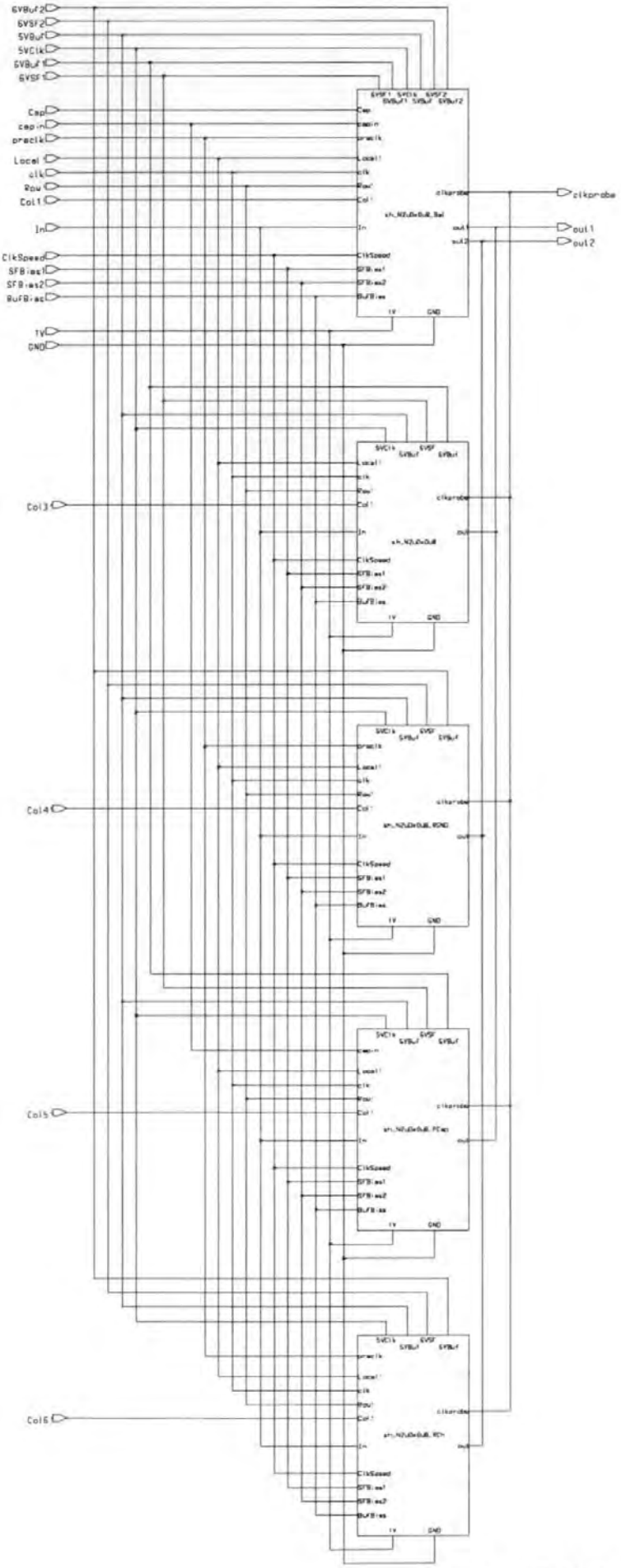


Fig. G-2: sh_N2u0x0u8_cells

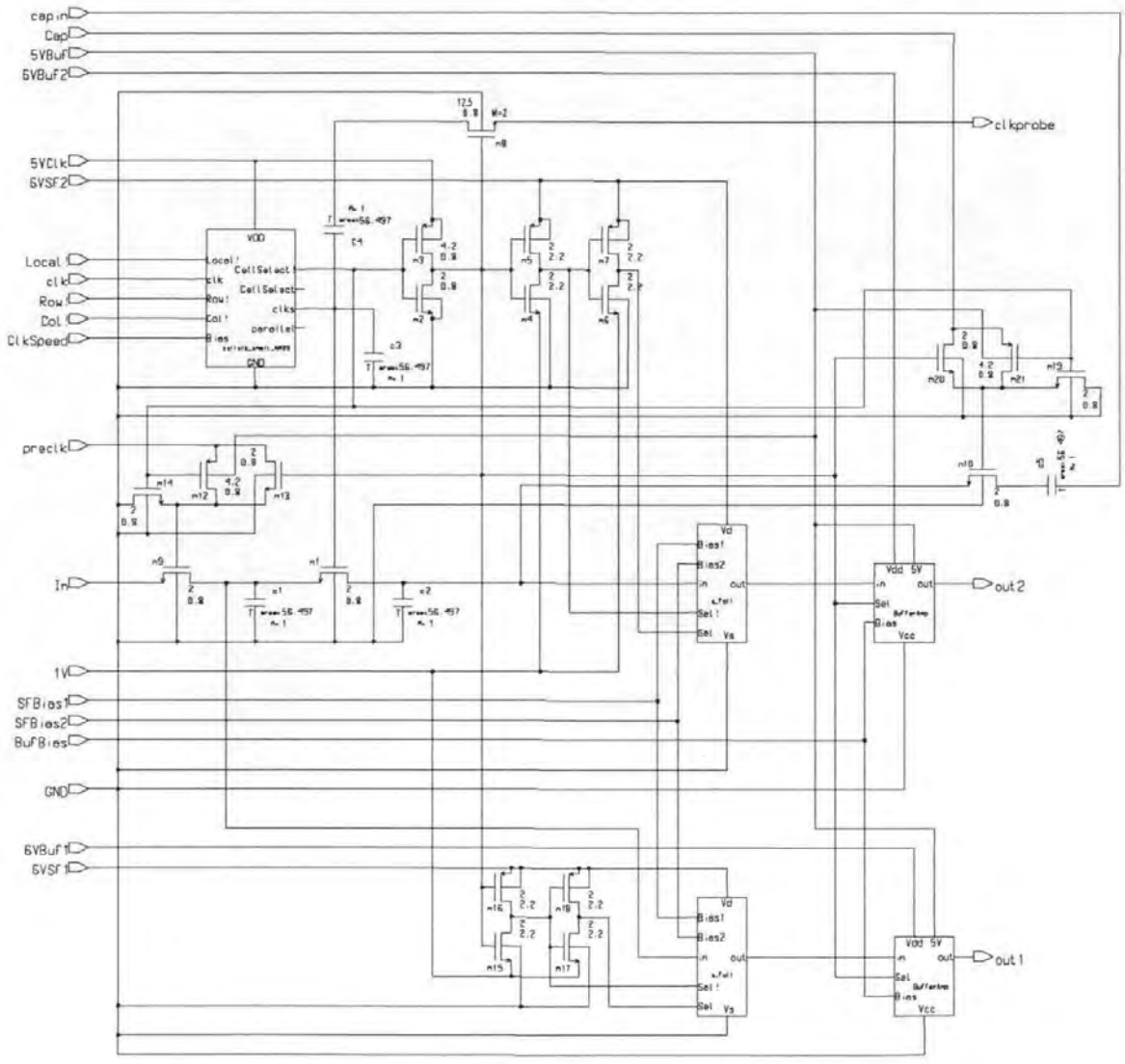


Fig. G-3: sh_N2u0x0u8_Bal

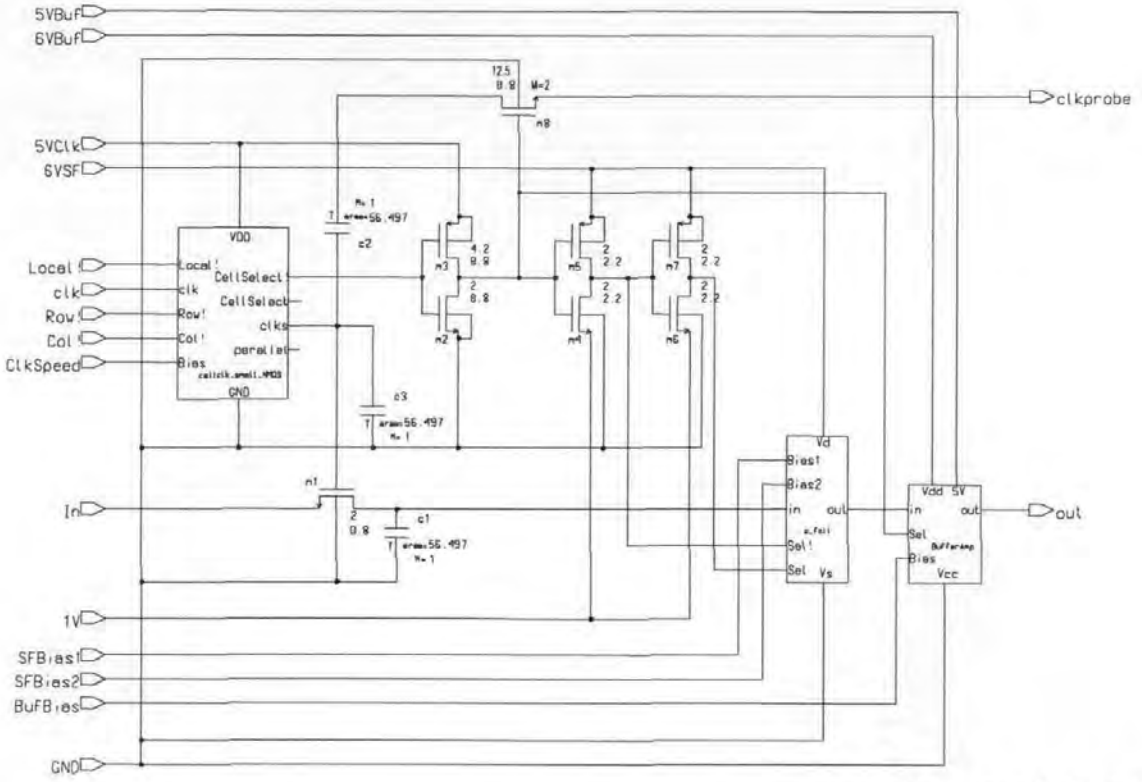


Fig. G-4: sh_N2u0x0u8

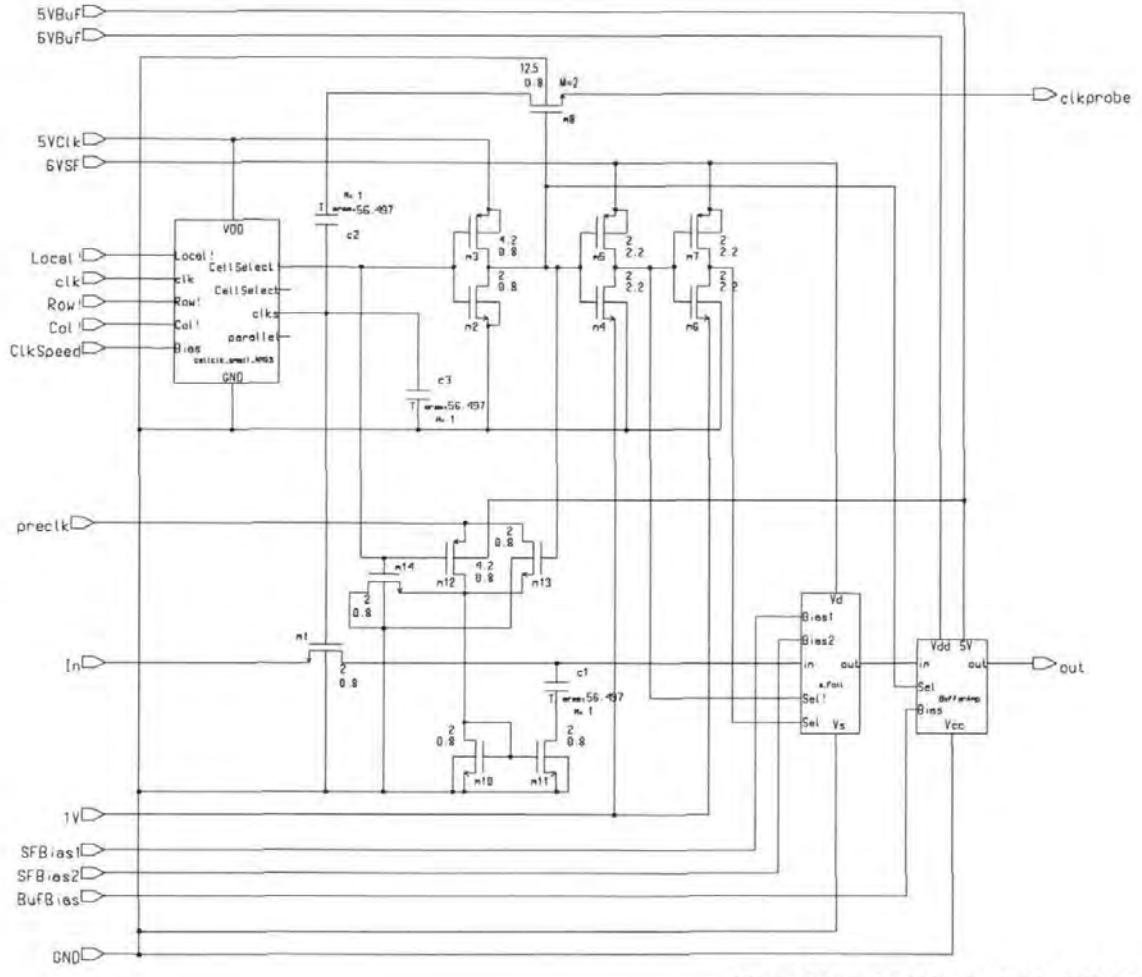


Fig. G-5: sh_N2u0x0u8_RGND

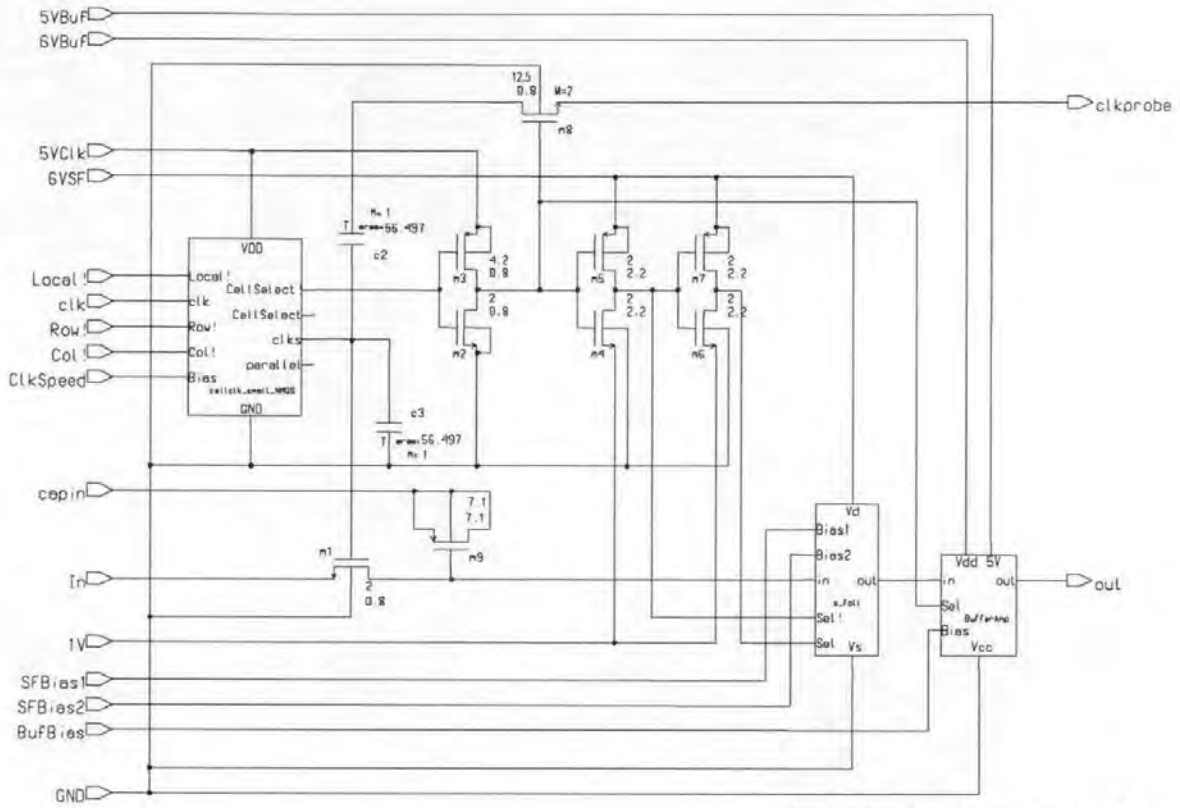


Fig. G-6: sh_N2u0x0u8_PCap

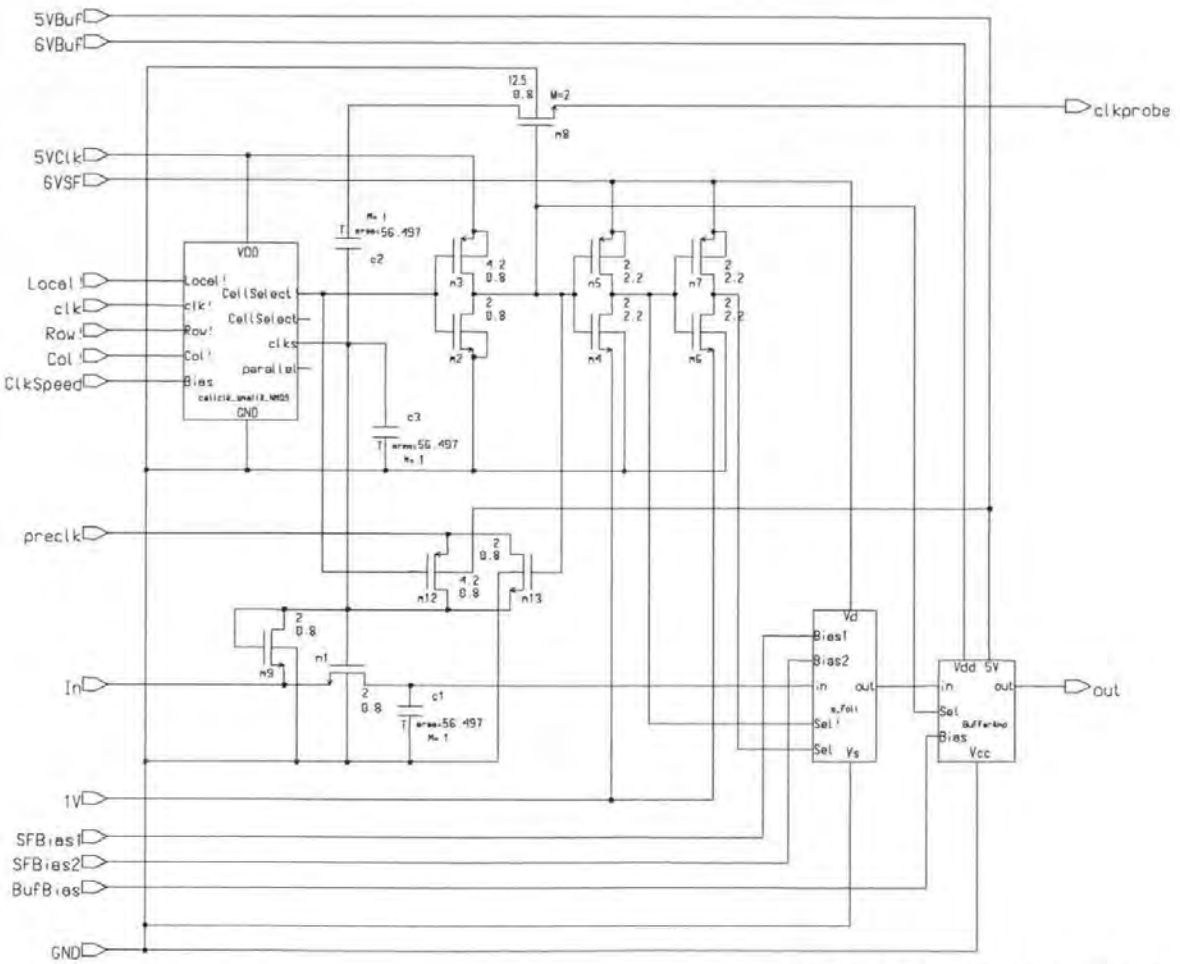


Fig. G-7: sh_N2u0x0u8_RCh

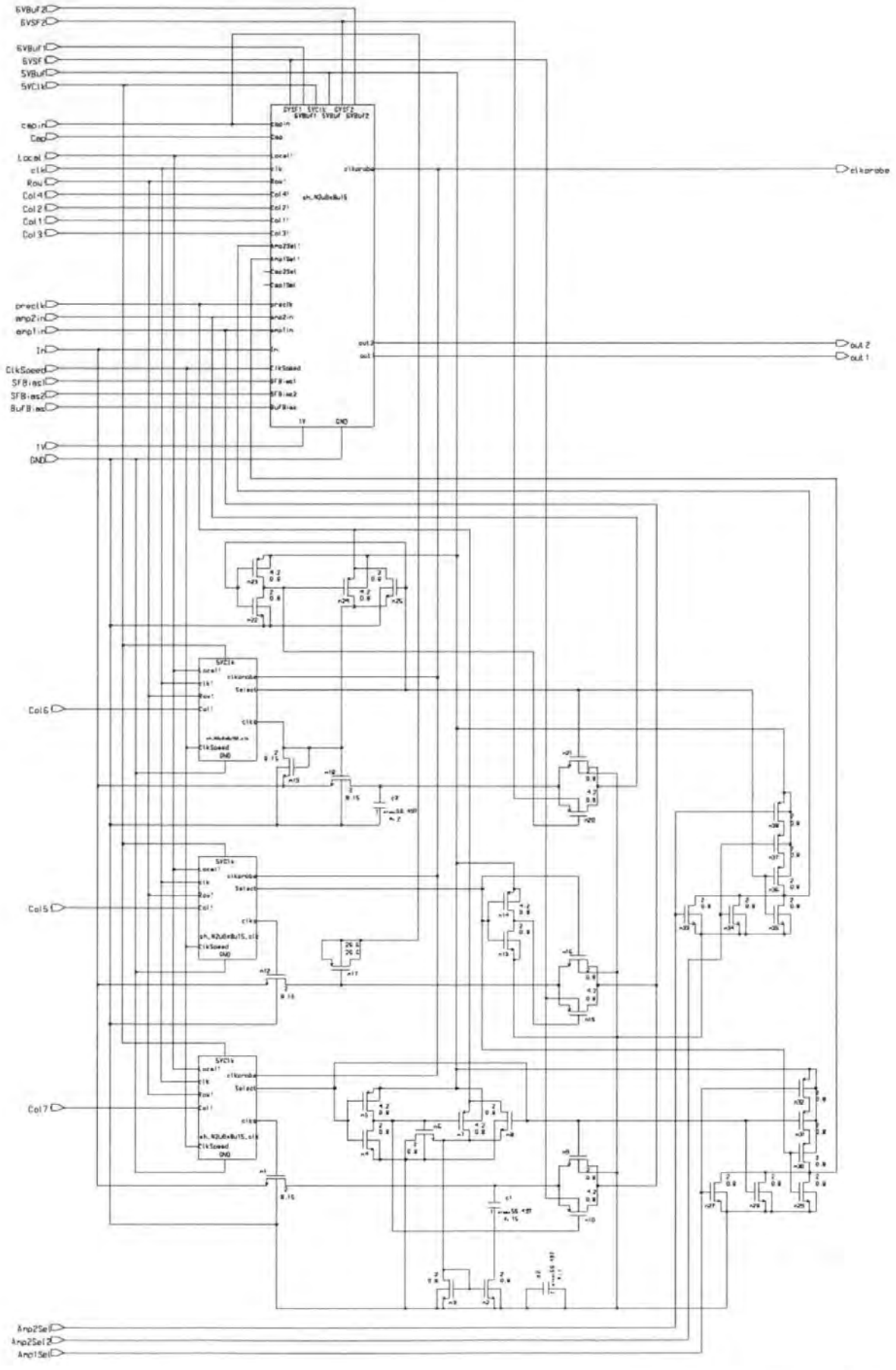


Fig. G-8: sh_N2u0x8u15X

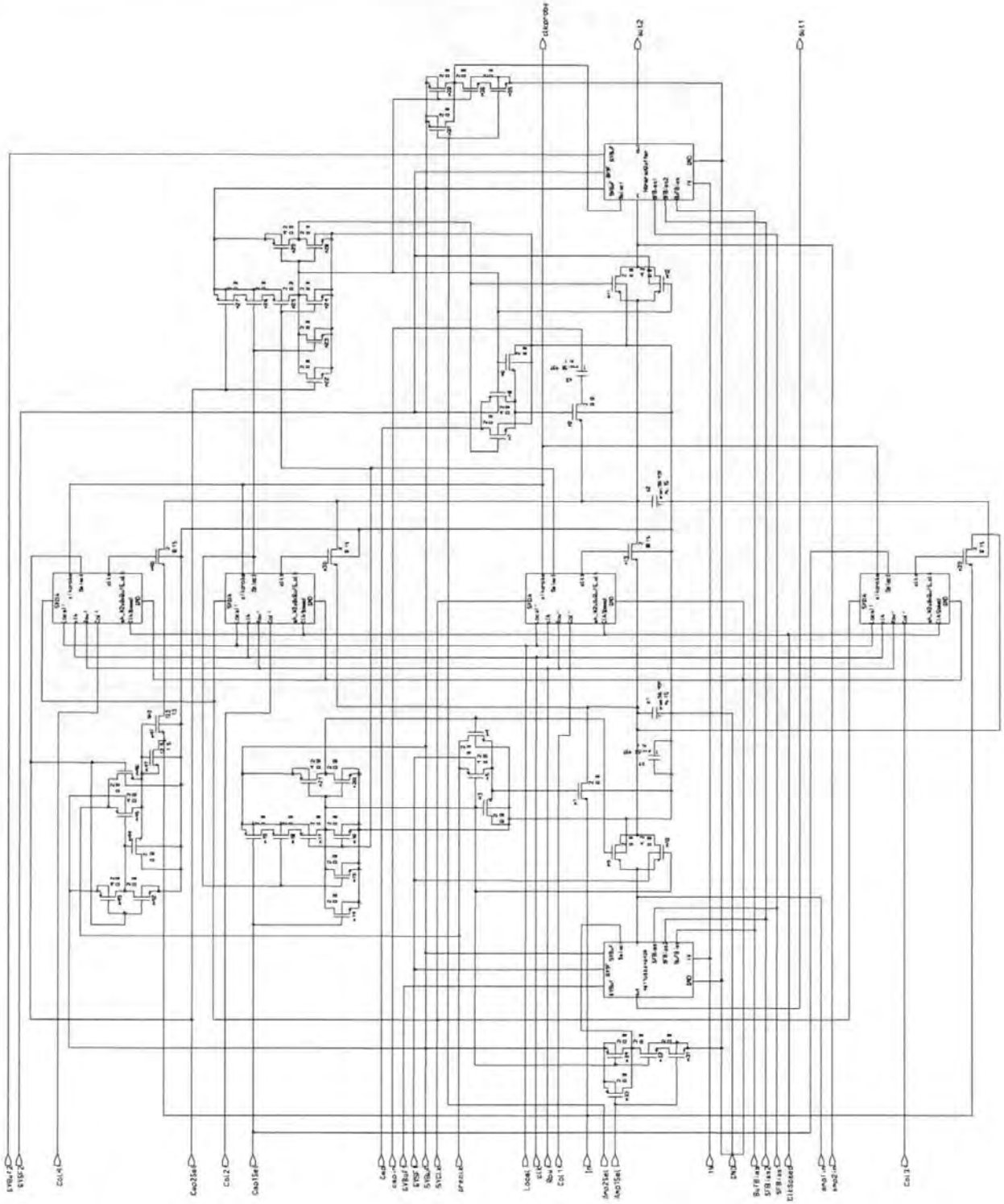


Fig. G-9: sh_N2u0x8u15

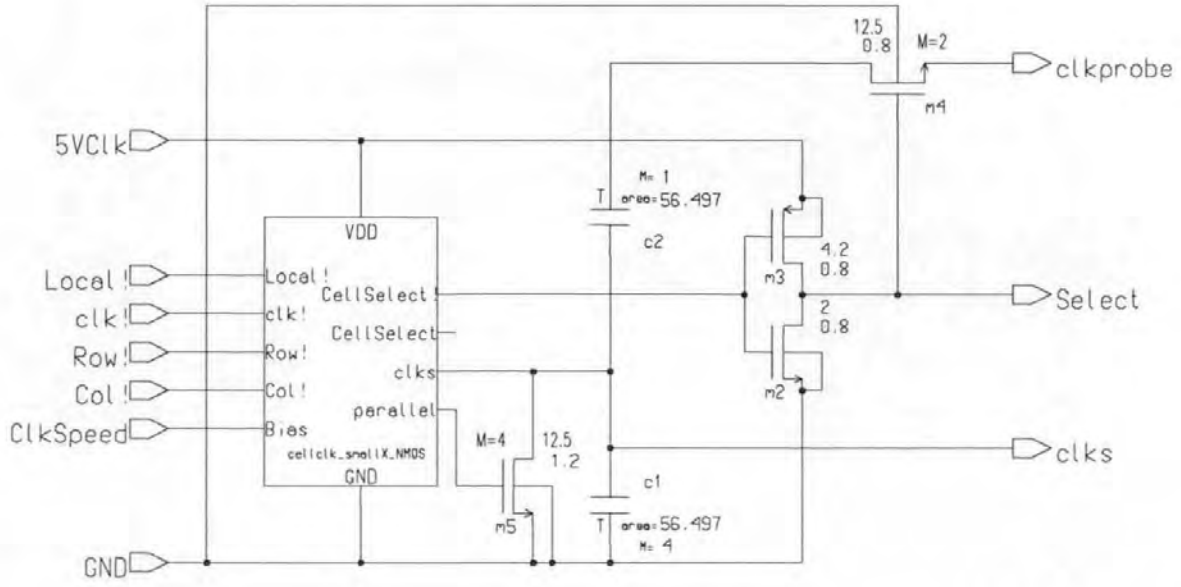


Fig. G-10: sh_N2u0x8u15X_clk

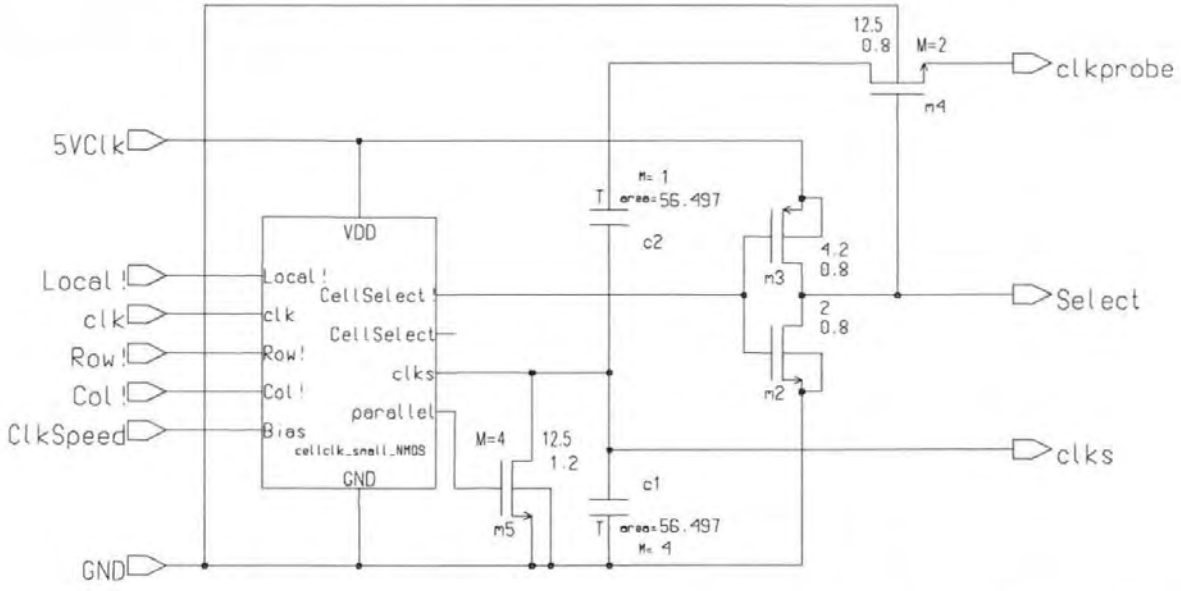


Fig. G-11: sh_N2u0x8u15_clk

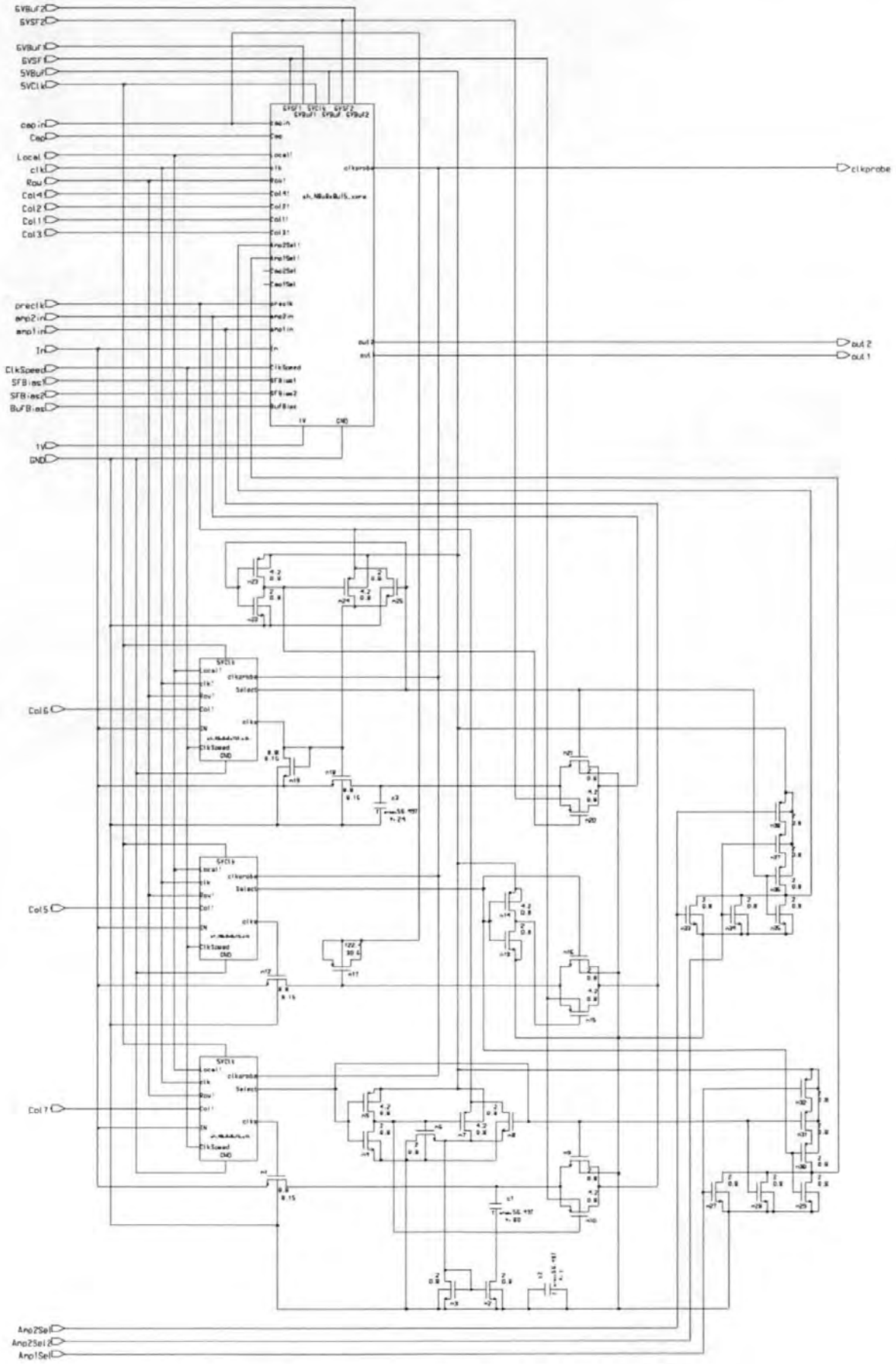


Fig. G-12: sh_N8u8x8u15X

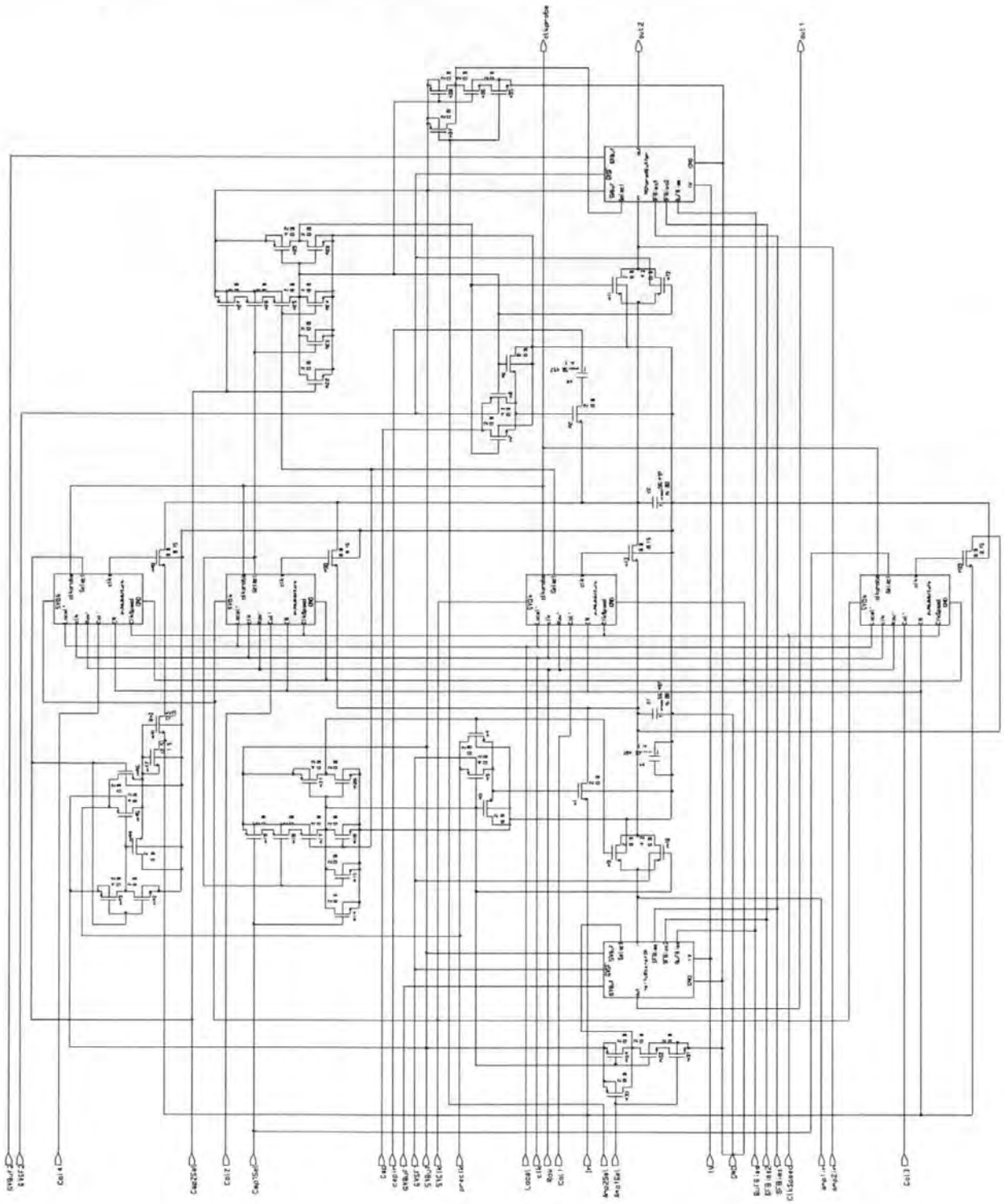


Fig. G-13: sh_N8u8x8u15_core

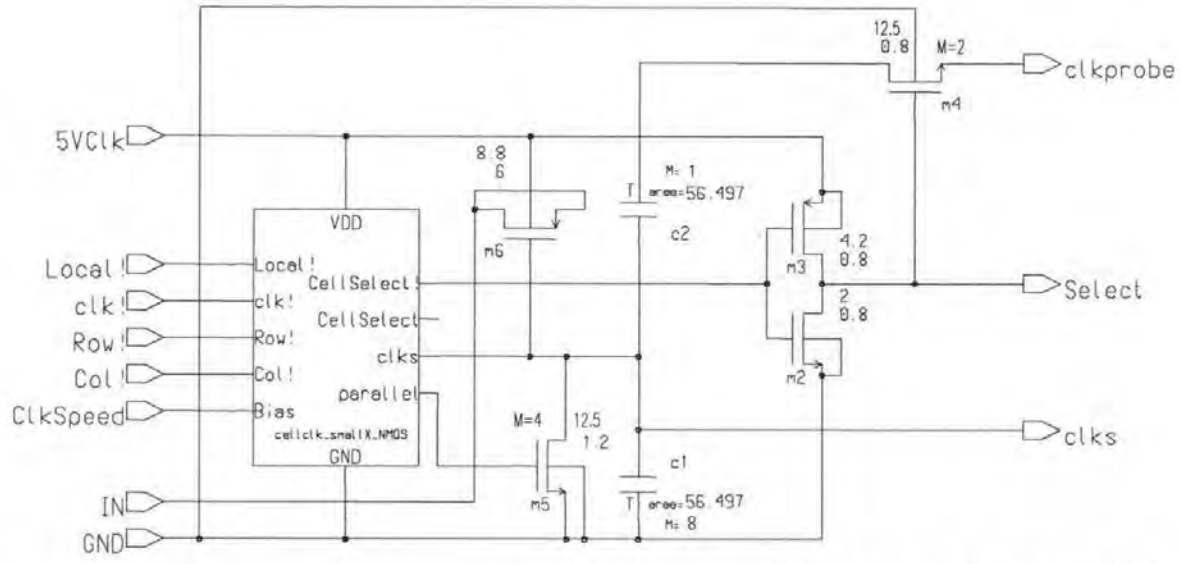


Fig. G-14: sh_N8u8x8u15X_clk

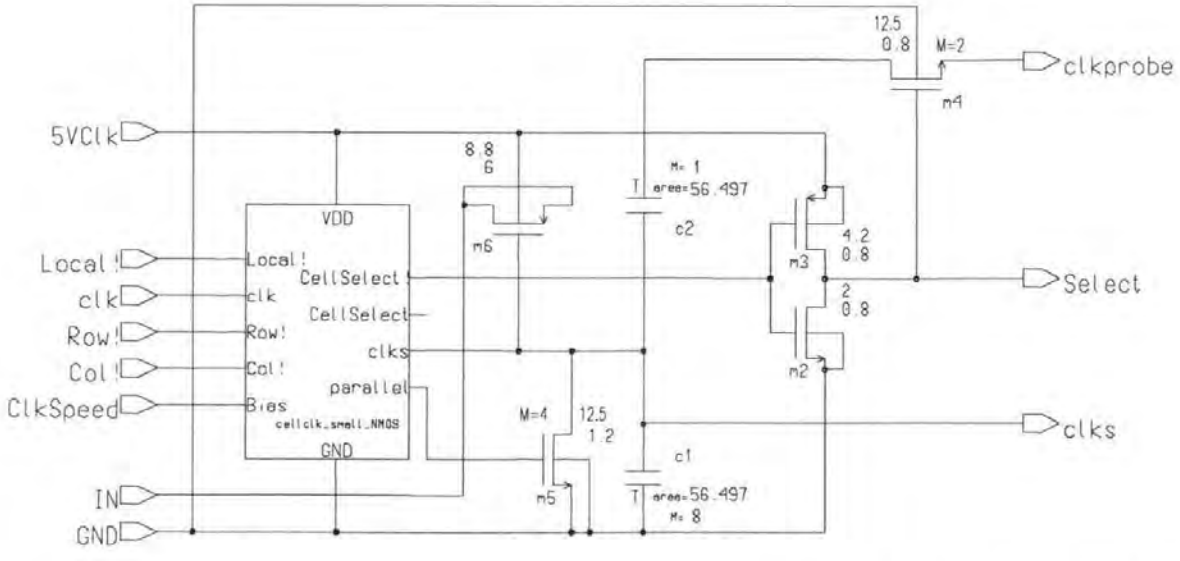


Fig. G-15: sh_N8u8x8u15_clk

Basic Cells

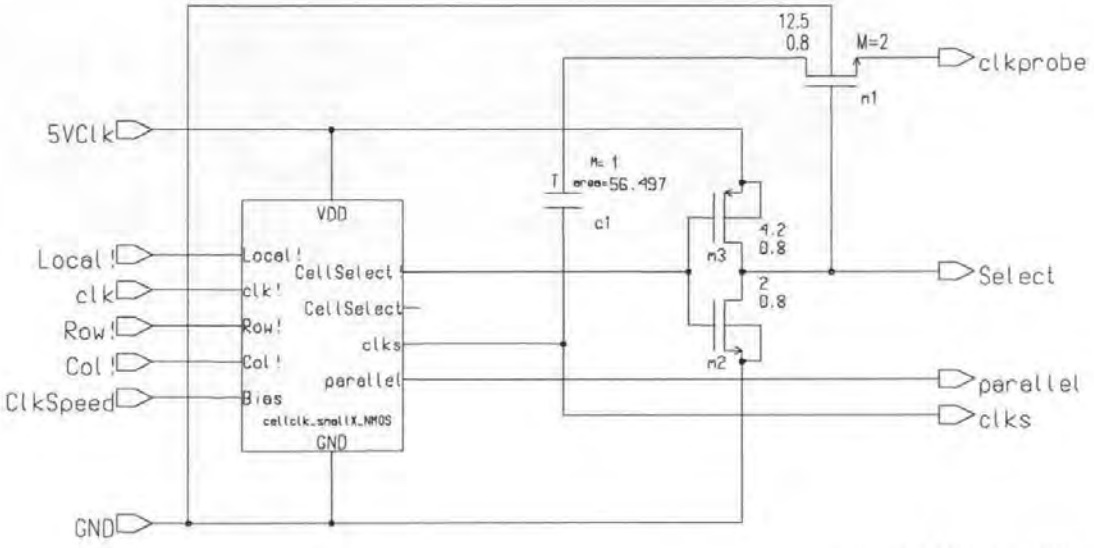


Fig. G-16: sh_NX_clk

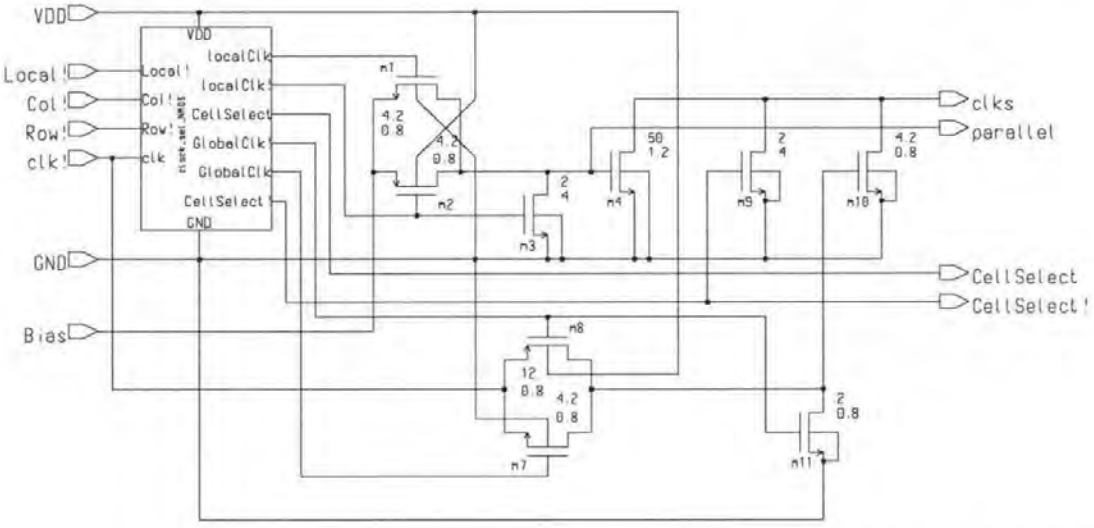


Fig. G-17: cellclk_smallX_NMOS

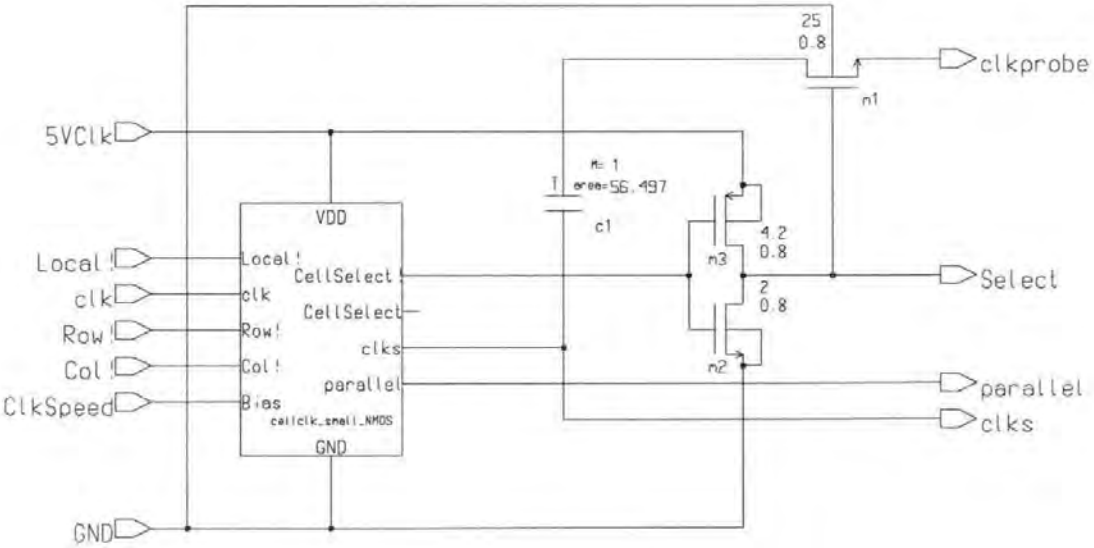


Fig. G-18: sh_N_clk

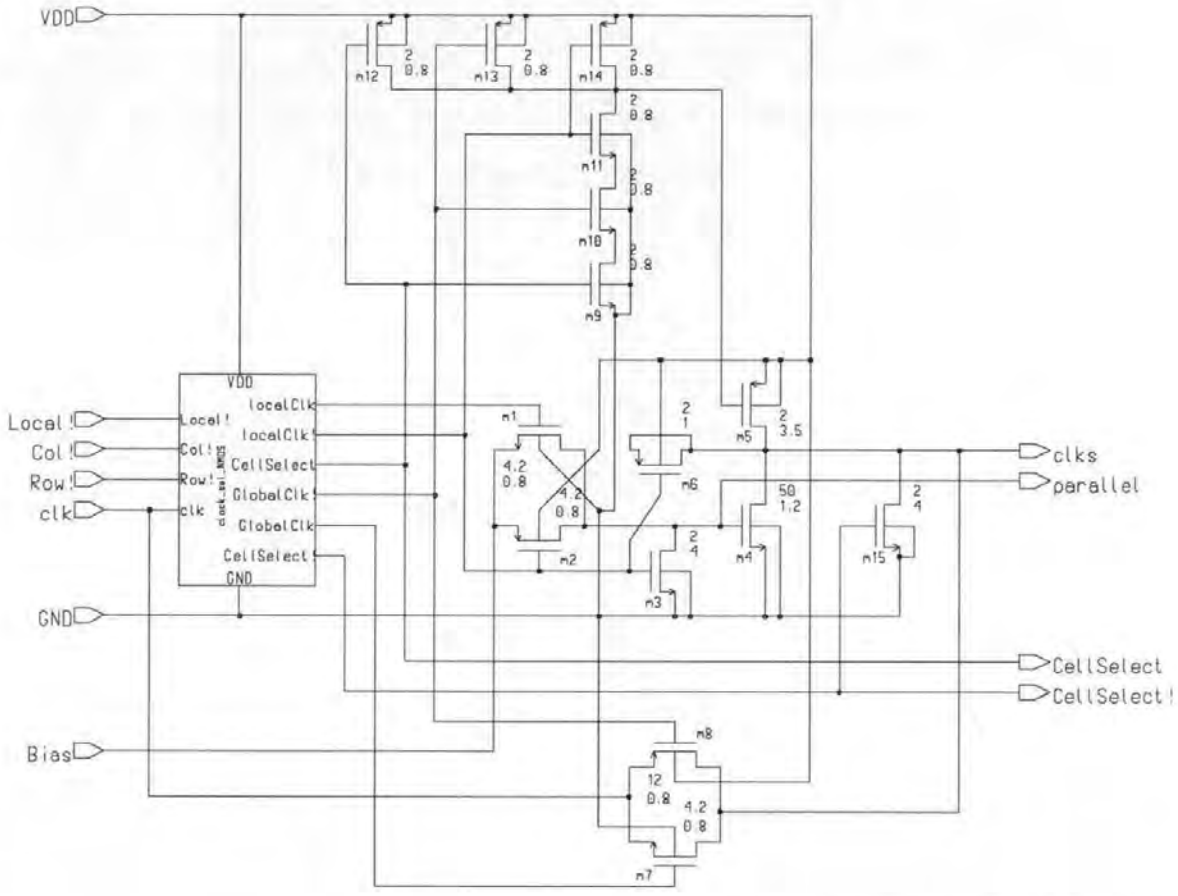


Fig. G-19: cellclk_small_NMOS

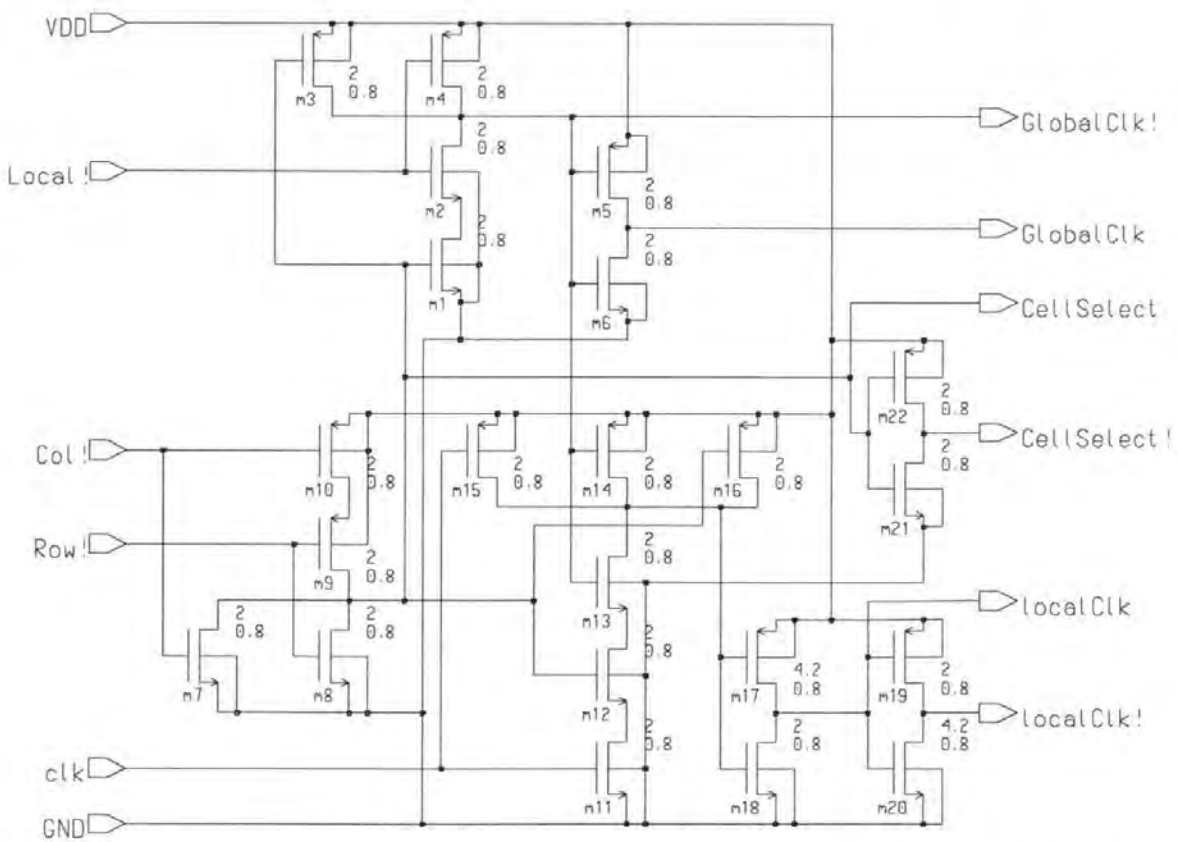


Fig. G-20: clock_sel_NMOS

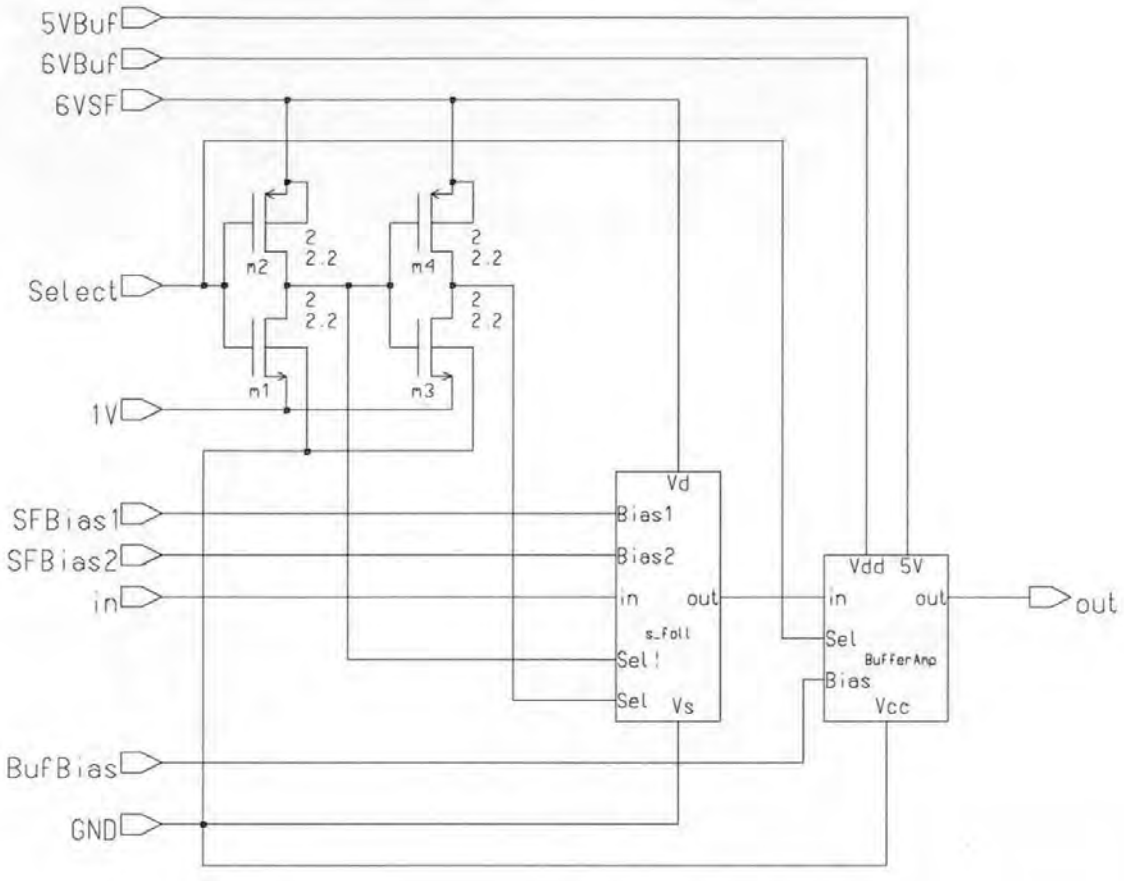


Fig. G-21: NSharedBuffer

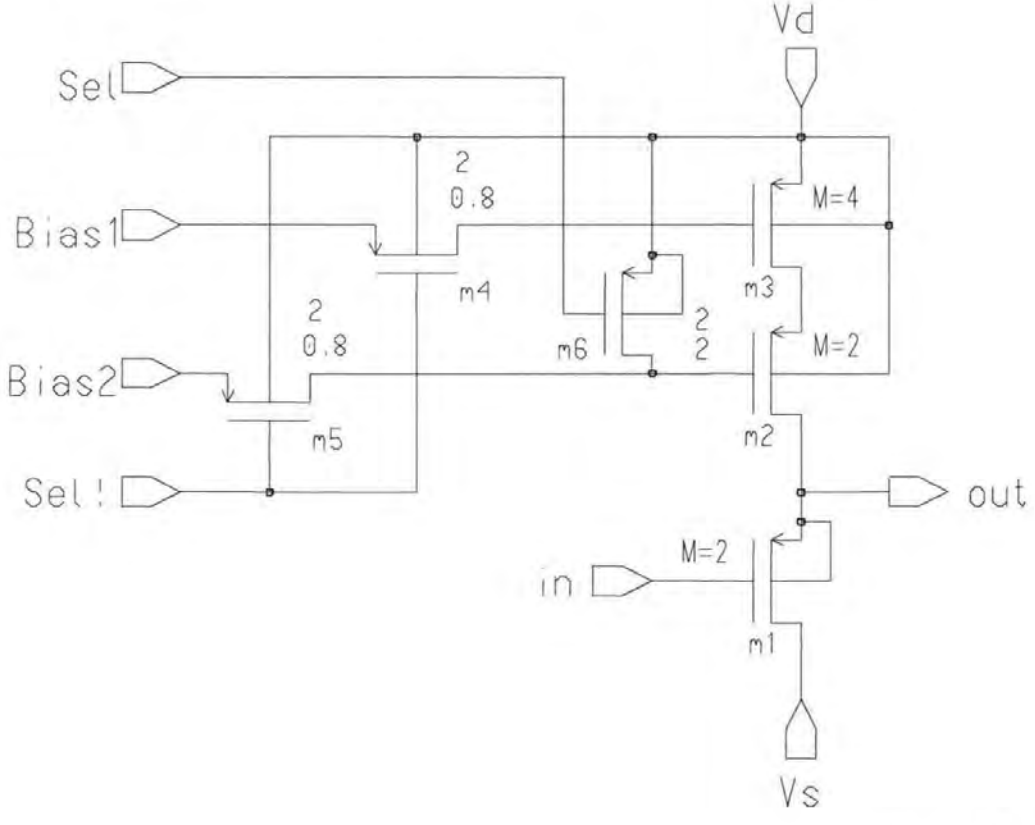


Fig. G-22: s_foll

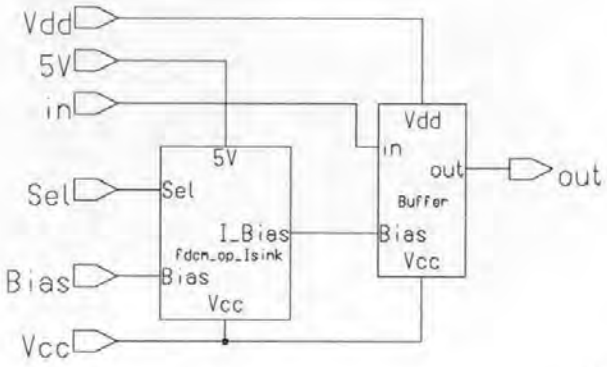


Fig. G-23: BufferAmp

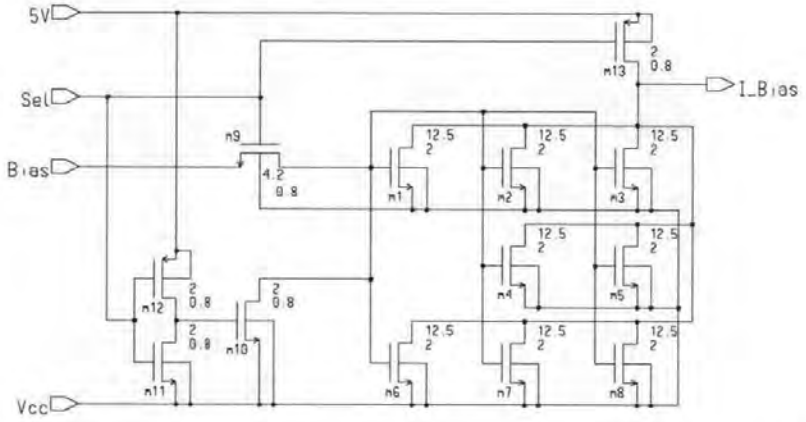


Fig. G-24: fdcm_op_Isink

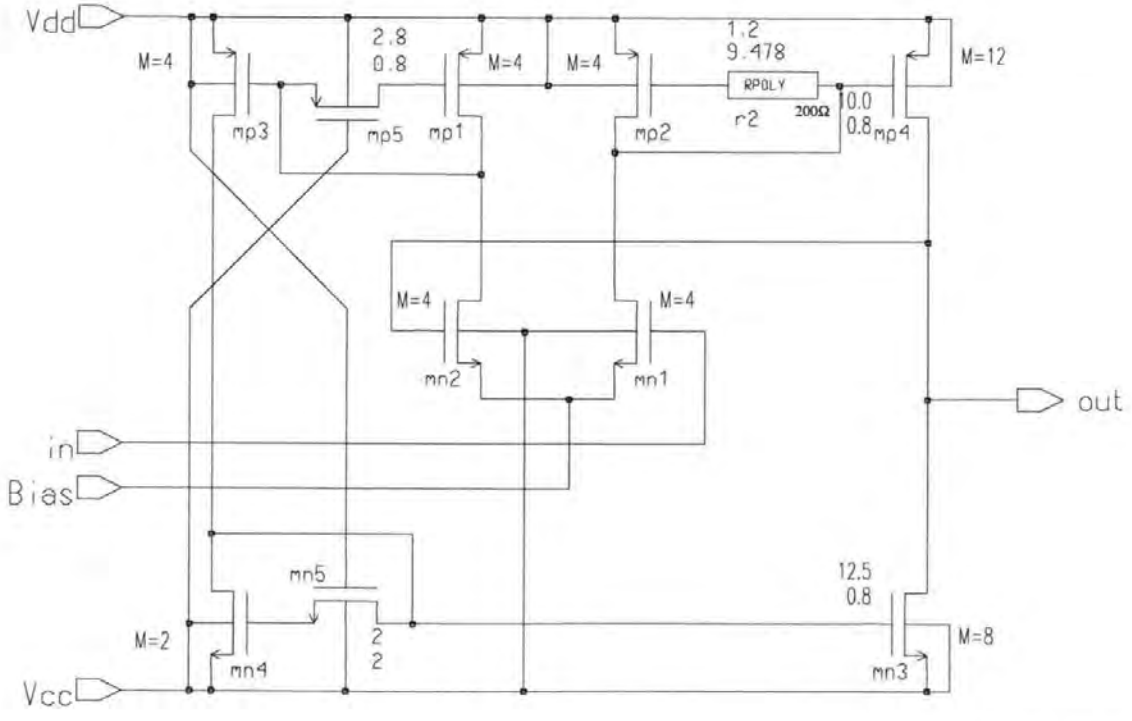


Fig. G-25: Buffer

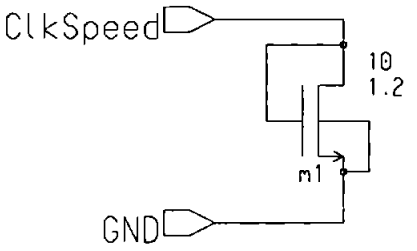


Fig. G-26: cellclk_biascir

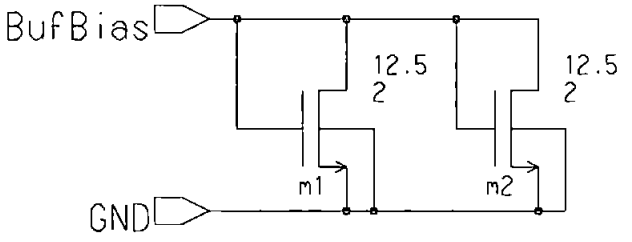


Fig. G-27: fdcm_op_biascir

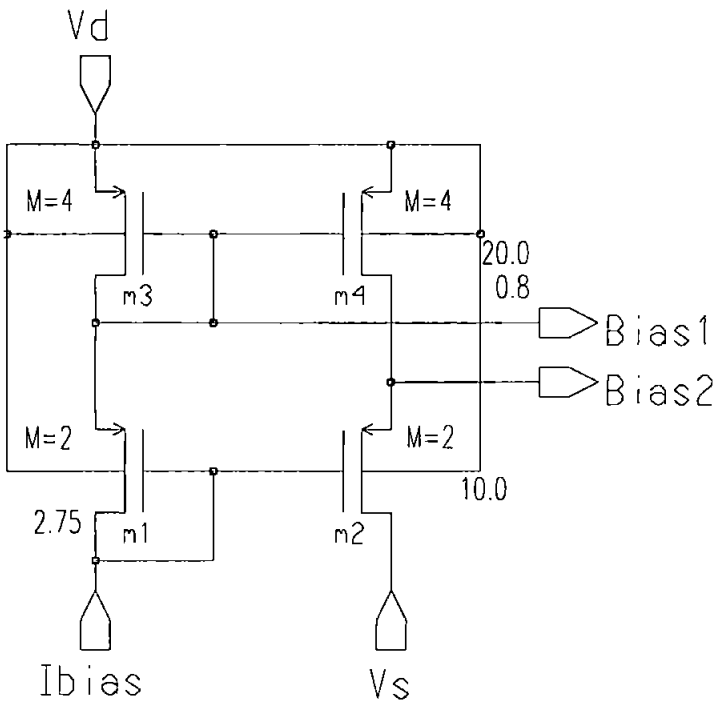


Fig. G-28: s_foll_biascir

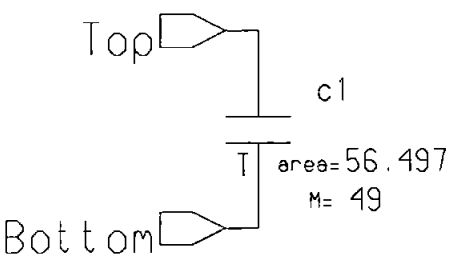


Fig. G-29: Cap4p9

Circuits
for
Process Parameter Determination

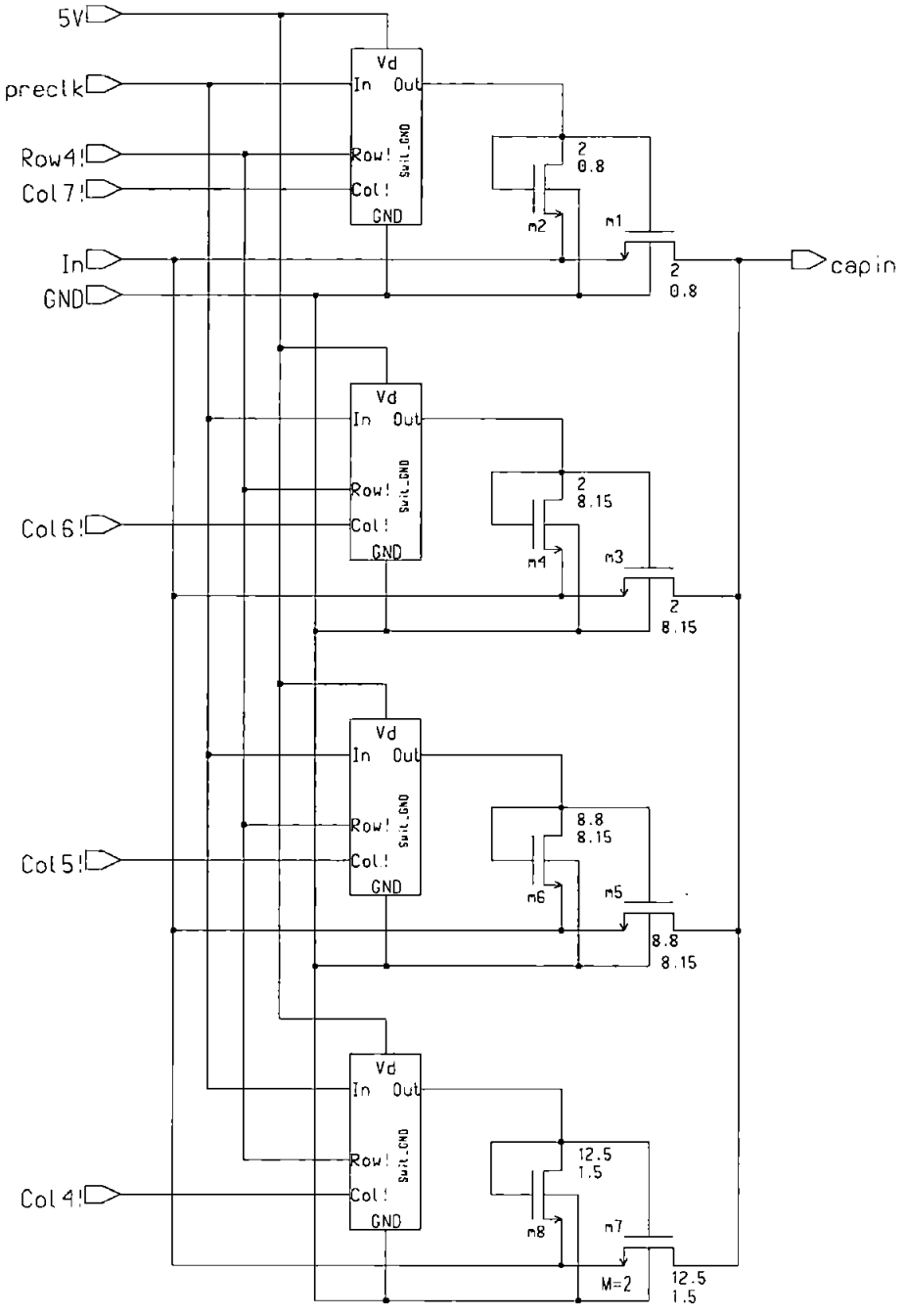


Fig. G-30: teststrus

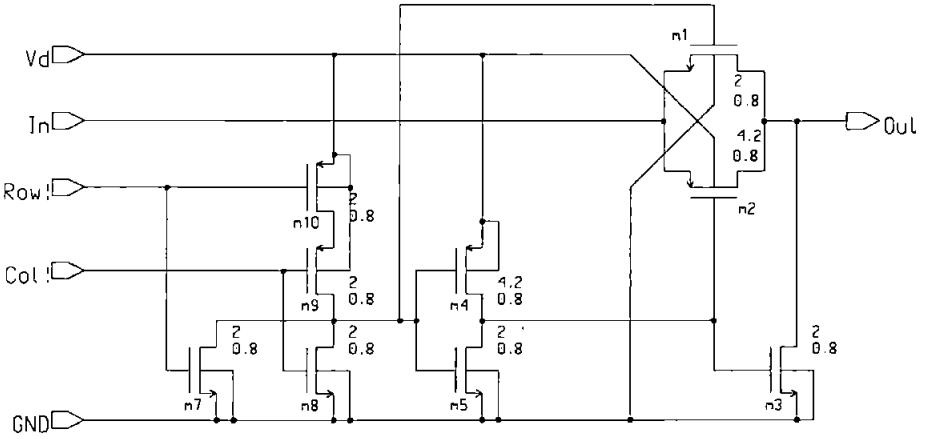


Fig. G-31: Swit_GND

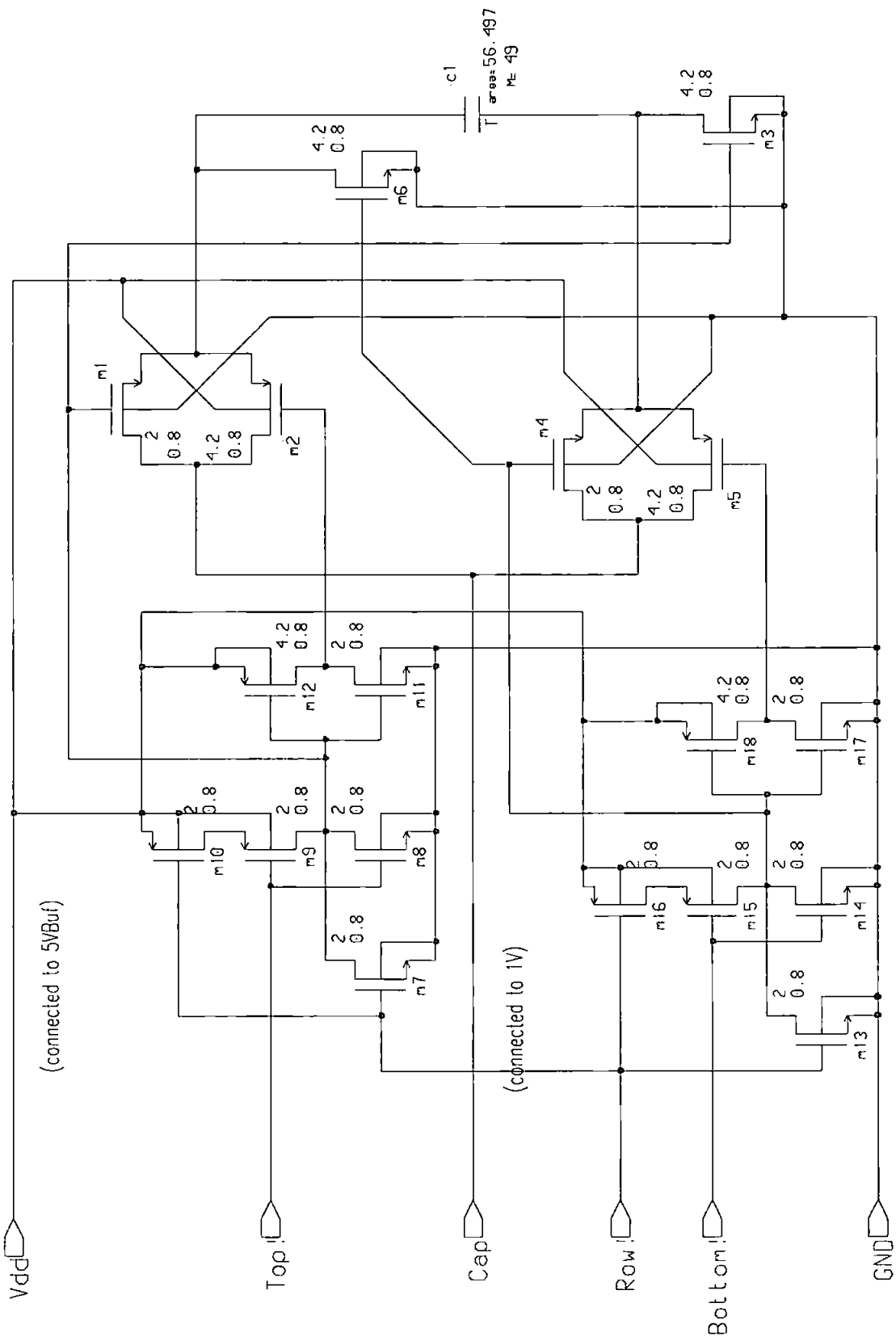
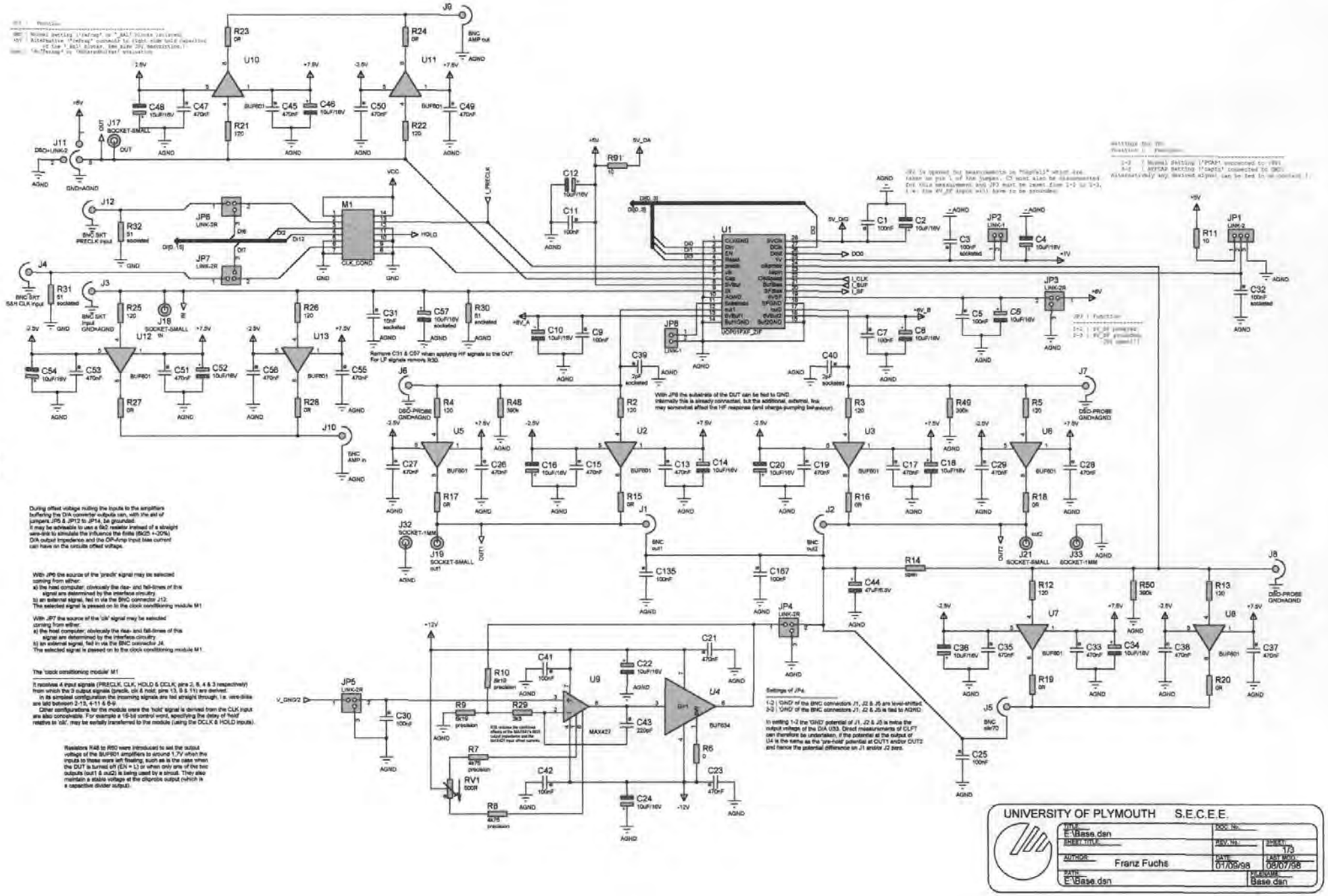
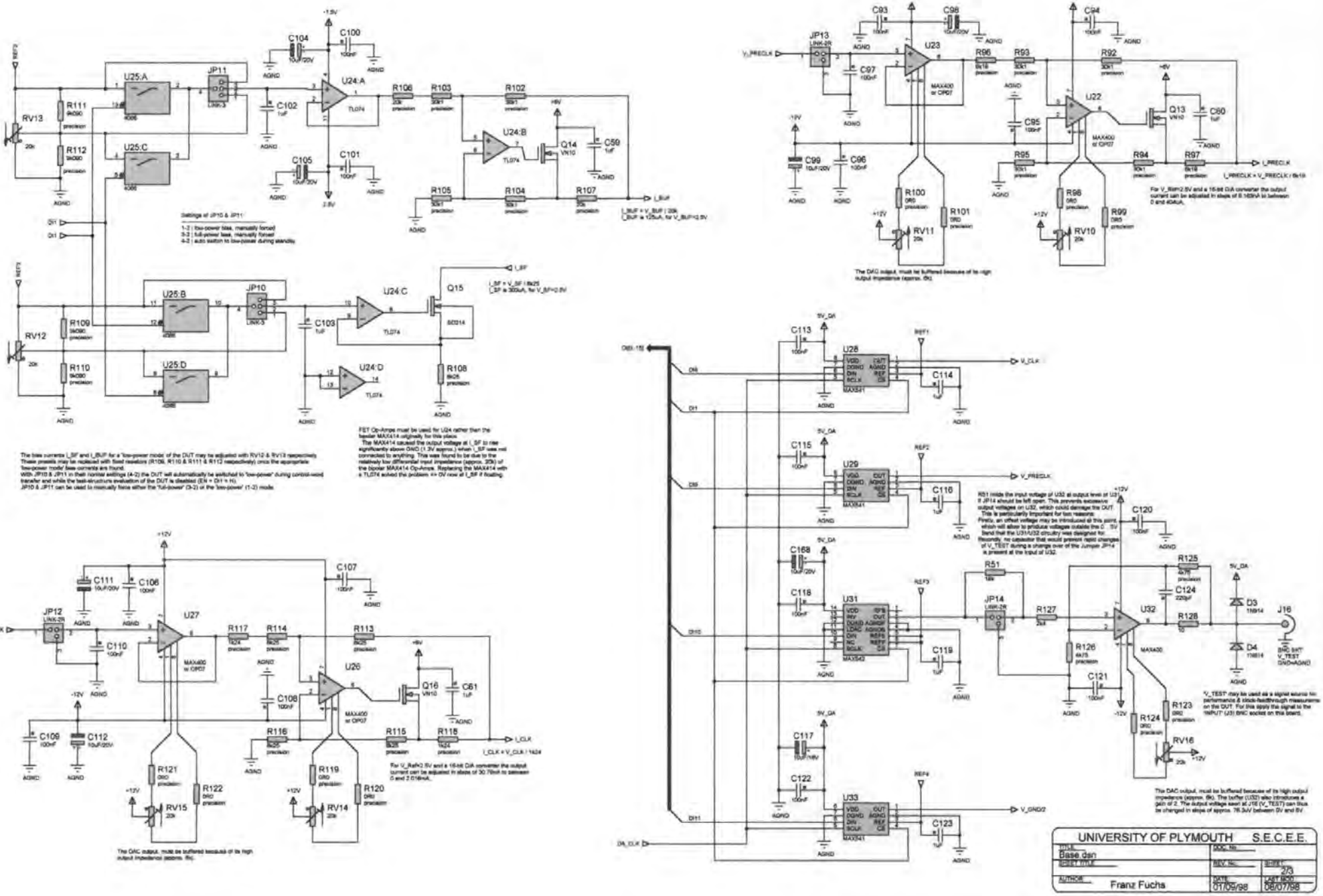


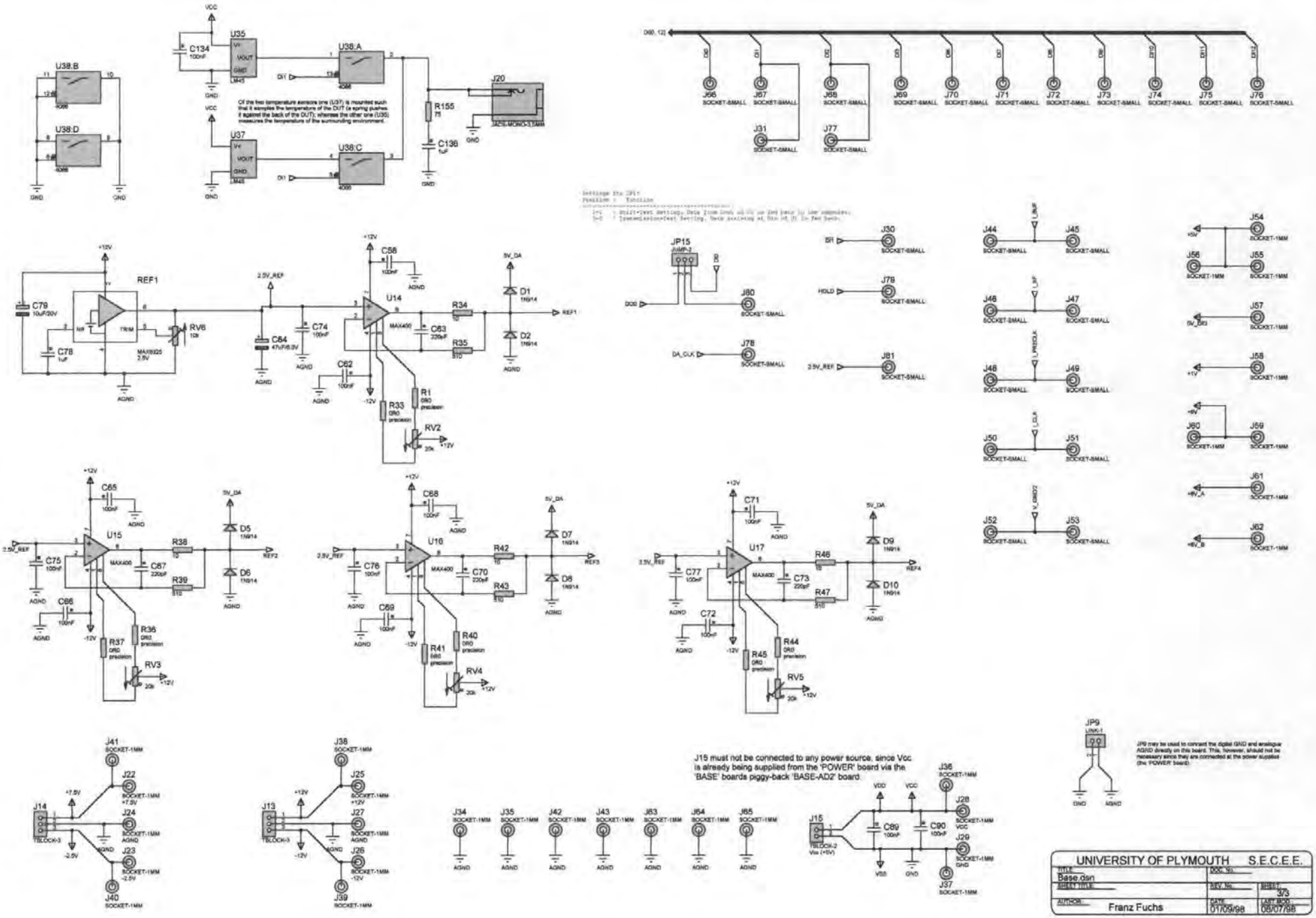
Fig. G-32: CapCell

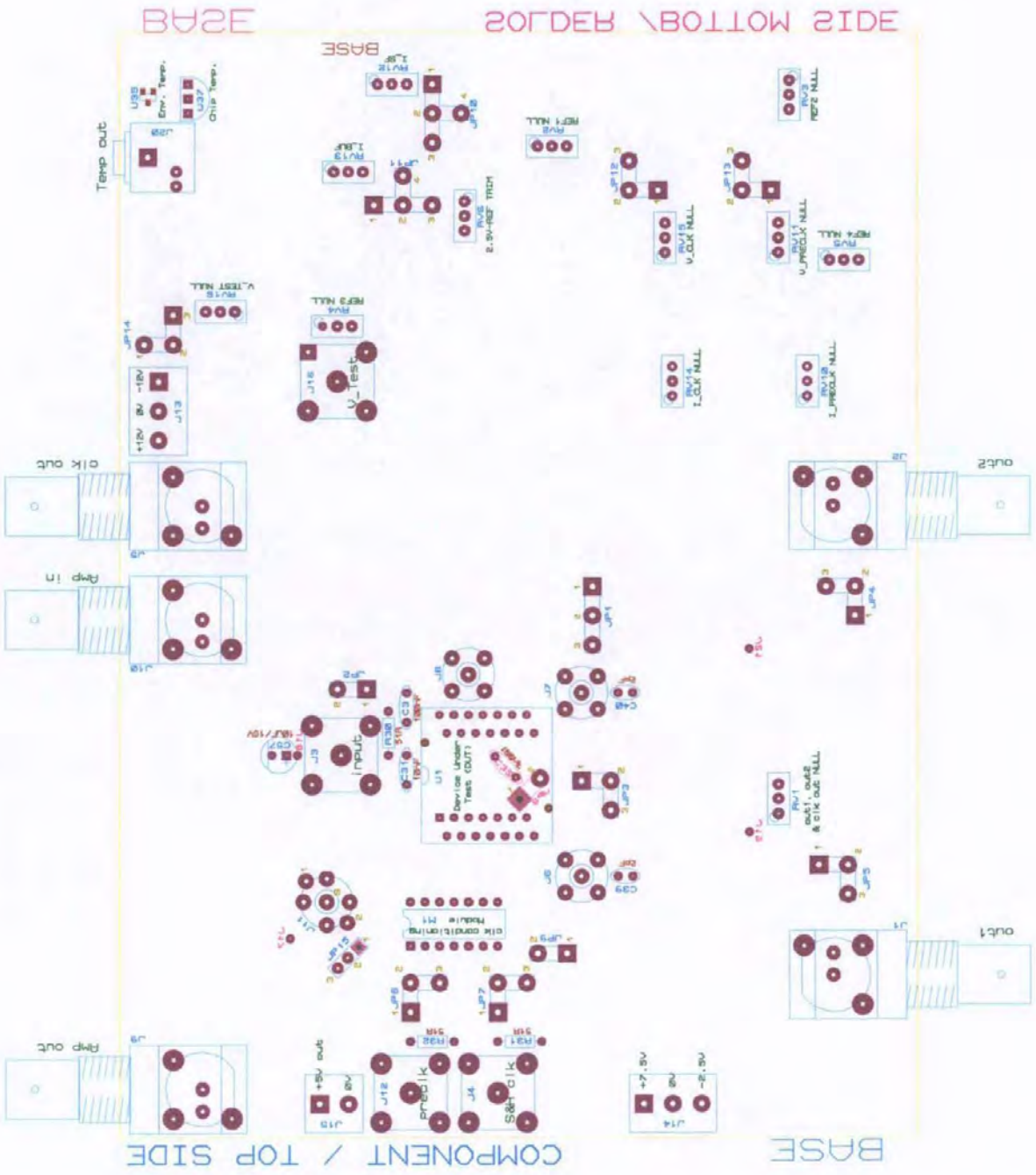
H. Schematics for the custom IC test-rig.

Schematics for the Base Board of the test-rig (BASE.DSN).


UNIVERSITY OF PLYMOUTH S.E.C.E.E.
TITLE: E:\Base.dsn
DOC. NO.:
SHEET: 1/3
AUTHOR: Franz Fuchs
DATE: 01/09/98
LAST MOD: 08/07/98
PATH: E:\Base.dsn
FILENAME: Base.dsn
During offset voltage nulling the inputs to the amplifiers buffering the D/A converter outputs can, with the aid of jumpers JP5 & JP12 to JP14, be grounded.
It may be advisable to use a 6kΩ resistor instead of a straight wire-link to simulate the influence the finite (6kΩ +-20%) D/A output impedance and the OP-Amp input bias current can have on the circuits offset voltage.
With JP6 the source of the 'preclk' signal may be selected coming from either:
a) the host computer; obviously the rise- and fall-times of this signal are determined by the interface circuitry.
b) an external signal, fed in via the BNC connector J12.
The selected signal is passed on to the clock conditioning module M1.
With JP7 the source of the 'clk' signal may be selected coming from either:
a) the host computer; obviously the rise- and fall-times of this signal are determined by the interface circuitry.
b) an external signal, fed in via the BNC connector J4.
The selected signal is passed on to the clock conditioning module M1.
The 'clock conditioning module' M1
It receives 4 input signals (PRECLK, CLK, HOLD & DCLK; pins 2, 5, 4 & 3 respectively) from which the 3 output signals (preclk, clk & hold; pins 13, 9 & 11) are derived.
In its simplest configuration the incoming signals are fed straight through, i.e. wire-links are laid between 2-13, 4-11 & 5-9.
Other configurations for this module were the 'hold' signal is derived from the CLK input are also conceivable. For example a 16-bit control word, specifying the delay of 'hold' relative to 'clk', may be serially transferred to the module (using the DCLK & HOLD inputs).
Resistors R48 to R50 were introduced to set the output voltage of the BUF601 amplifiers to around 1.7V when the inputs to those were left floating, such as is the case when the DUT is turned off (EN = L) or when only one of the two outputs (out1 & out2) is being used by a circuit. They also maintain a stable voltage at the dtlprobe output (which is a capacitive divider output).
Remove C31 & C57 when applying HF signals to the OUT. For LF signals remove R30.
With JP8 the substrate of the DUT can be tied to GND. Internally this is already connected, but the additional, external, link may somewhat affect the HF response (and charge-pumping behaviour).
Settings of JP4:
1-2 | 'GND' of the BNC connectors J1, J2 & J5 are level-shifted.
2-3 | 'GND' of the BNC connectors J1, J2 & J5 is tied to AGND.
In setting 1-2 the 'GND' potential of J1, J2 & J5 is twice the output voltage of the D/A U33. Direct measurements of CLF7 can therefore be undertaken, if the potential at the output of U4 is the same as the 'pre-hold' potential at OUT1 and/or OUT2 and hence the potential difference on J1 and/or J2 zero.

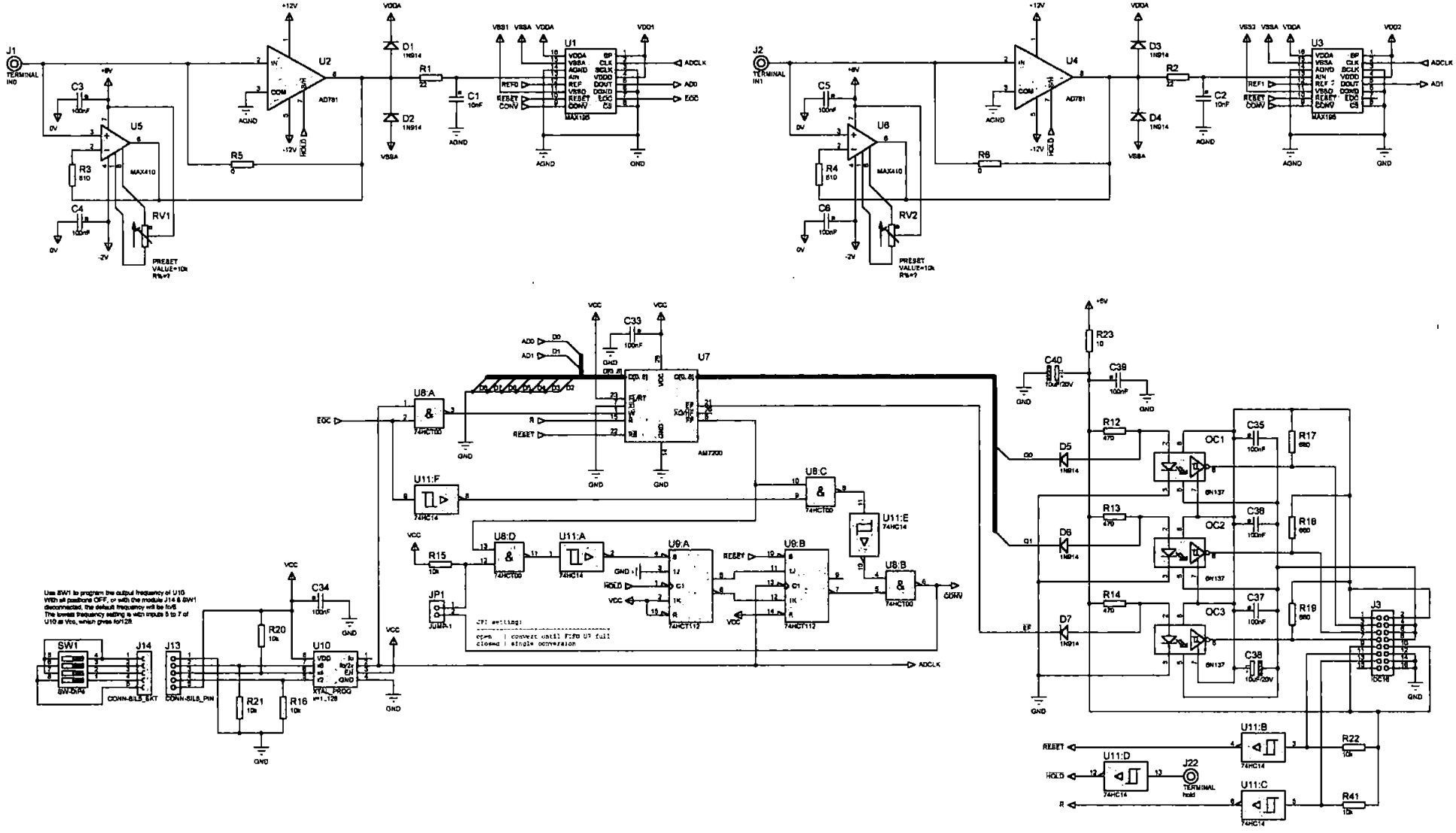

U25:A
U25:C
U25:B
U25:D
JP11
JP10
U24:A
U24:B
U24:C
U24:D
RV13
RV12
Q14
Q15
C59
C61
C100
C101
C102
C103
C104
C105
R102
R103
R104
R105
R106
R107
R108
R109
R110
R111
R112
I_BUF
I_SF
U23
U22
JP13
C93
C94
C95
C96
C97
C98
C99
Q13
C60
R92
R93
R94
R95
R96
R97
R99
R100
R101
RV10
RV11
V_PRECLK
I_PRECLK
U26
U27
JP12
C106
C107
C108
C109
C110
C111
C112
R113
R114
R115
R116
R117
R118
R119
R120
R121
R122
RV14
RV15
V_CLK
I_CLK
U28
U29
U31
U32
U33
JP14
C113
C114
C115
C116
C117
C118
C119
C120
C121
C122
C123
C124
R123
R124
R125
R126
R127
R128
R51
RV16
D3
D4
J16
V_REF2
V_GND/2
DA_CLK
D0
D1
D9
D10
D11


U38:B
U38:D
U35
U37
U38:A
U38:C
C134
C136
R155
J20
Of the two temperature sensors one (U37) is mounted such that it samples the temperature of the DUT (a spring pushes it against the back of the DUT), whereas the other one (U35) measures the temperature of the surrounding environment.
J66
J67
J68
J69
J70
J71
J72
J73
J74
J75
J76
J31
J77
REF1
C79
C78
RV6
C64
C74
C62
U14
C58
C63
C61
R34
R35
R1
R33
RV2
D1
D2
JP15
J80
J78
J81
J30
J79
J44
J45
J46
J47
J48
J49
J50
J51
J52
J53
J54
J55
J56
J57
J58
J59
J60
J61
J62
U15
C65
C75
C87
C86
R38
R39
R36
R37
RV3
D5
D6
U16
C68
C76
C70
C69
R42
R43
R40
R41
RV4
D7
D8
U17
C71
C77
C73
C72
R46
R47
R44
R45
RV5
D9
D10
J41
J22
J24
J23
J40
J14
J38
J25
J27
J26
J39
J13
J34
J35
J42
J43
J63
J64
J65
J15
C89
C90
J36
J28
J29
J37
JP9
J15 must not be connected to any power source, since Vcc is already being supplied from the 'POWER' board via the 'BASE' boards piggy-back 'BASE-AD2' board.
JP9 may be used to connect the digital GND and analogue AGND directly on this board. This, however, should not be necessary since they are connected at the power supplies (the 'POWER' board).
UNIVERSITY OF PLYMOUTH S.E.C.E.E.
TITLE Base.dsn
SHEET TITLE
AUTHOR Franz Fuchs
DOC. NO.
REV. No.
SHEET 3/3
DATE 01/09/98
LAST MOD. 08/07/98



Location of presets, modules, sockets, connectors and jumper-links on the Base Board.

Schematics for the Analog/Digital converter board (AD2.DSN).



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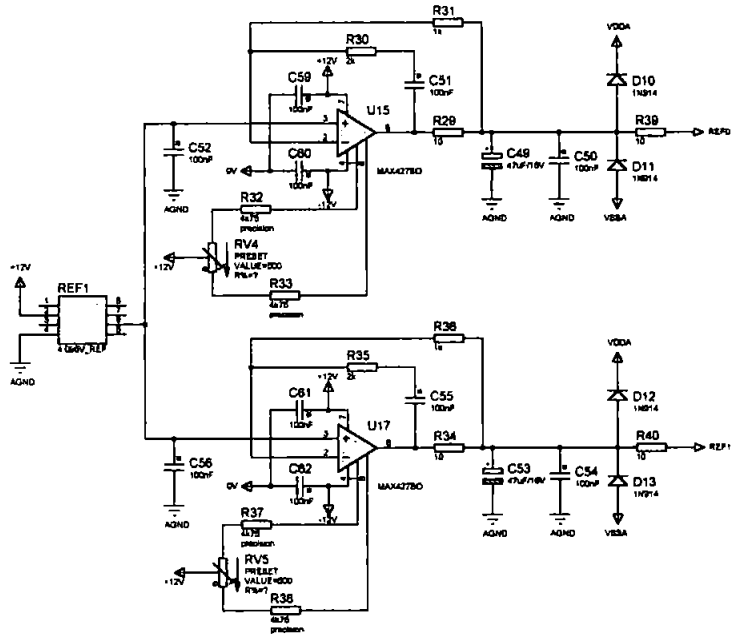

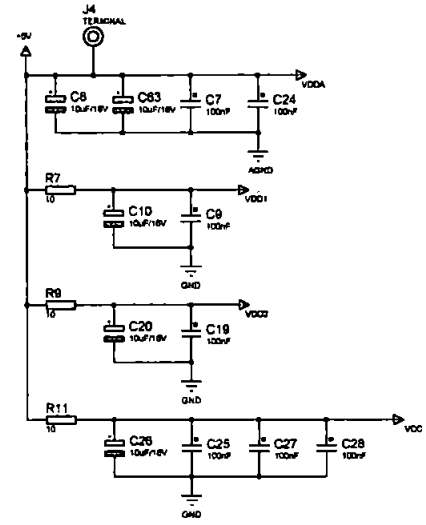

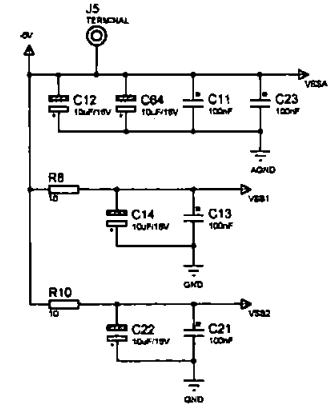

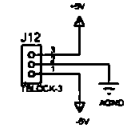

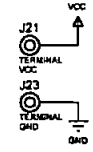

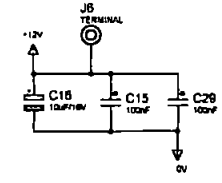

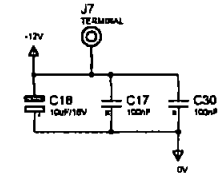

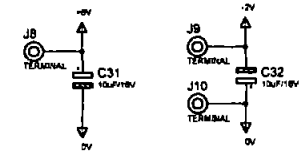

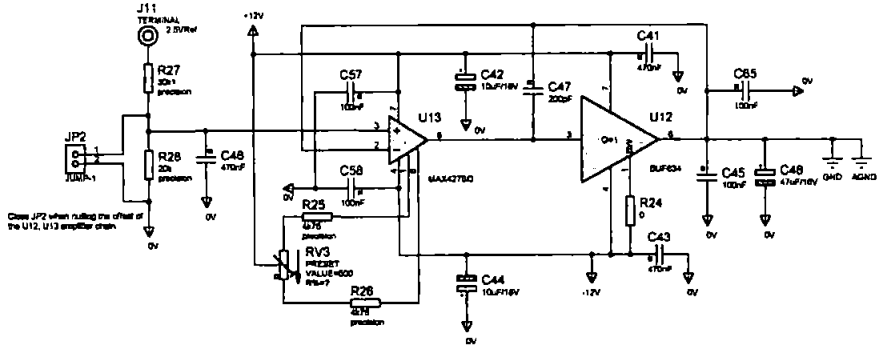

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AUTHOR: Franz Fuchs	DATE: 01/24/98	LAST MOD: 12/12/00
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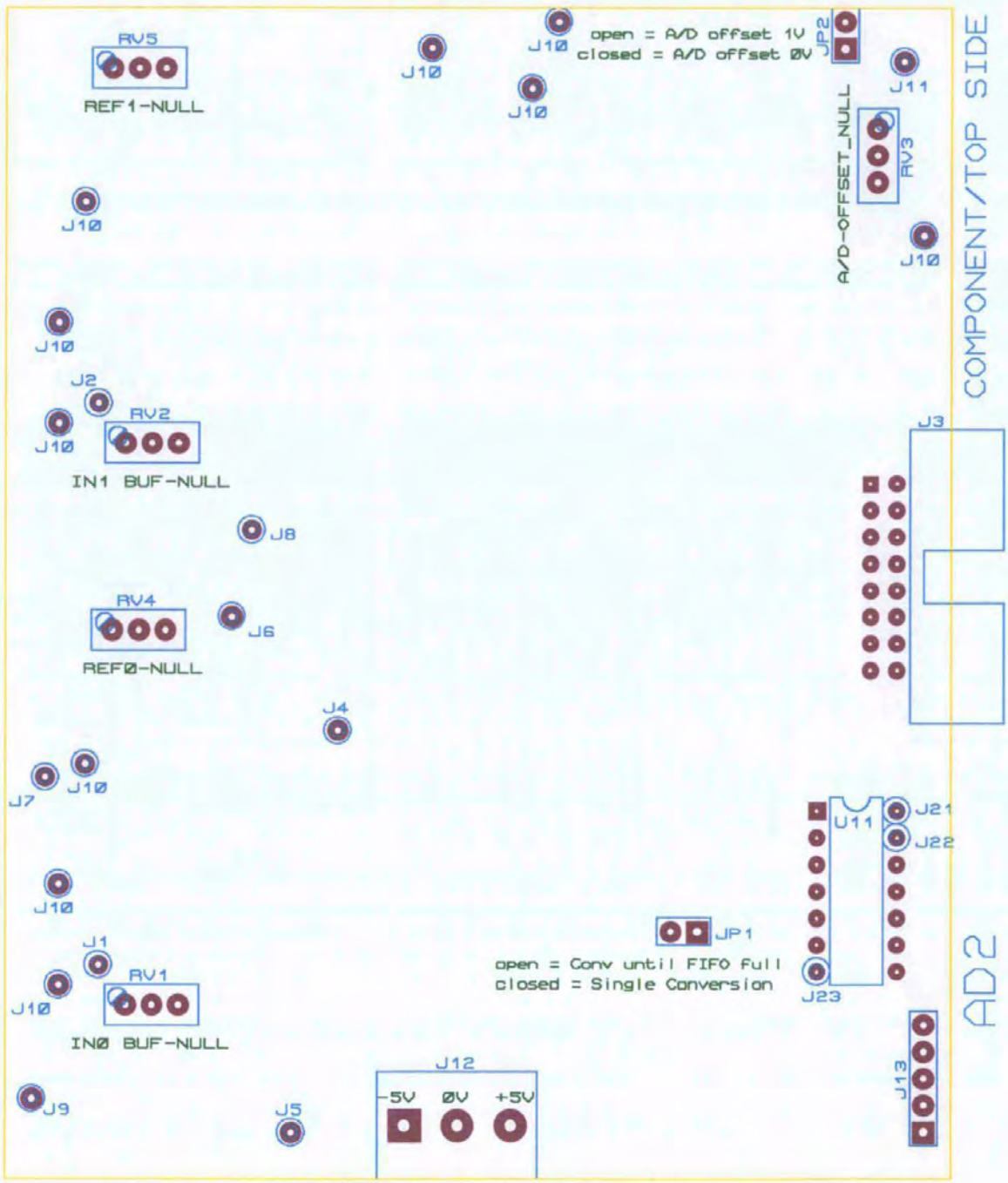
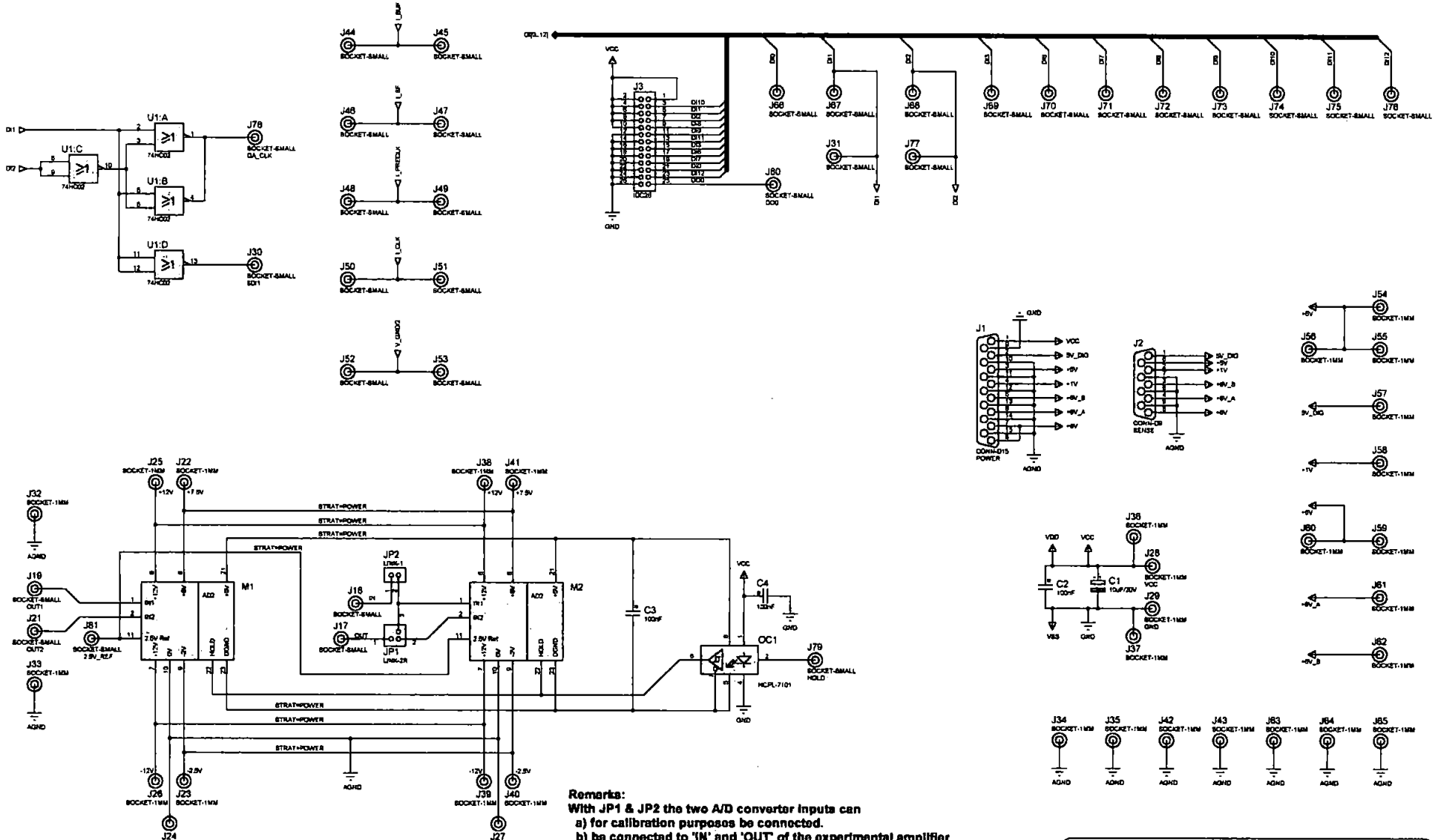


Location of presets, connectors, sockets and jumper-links on the A/D converter board.

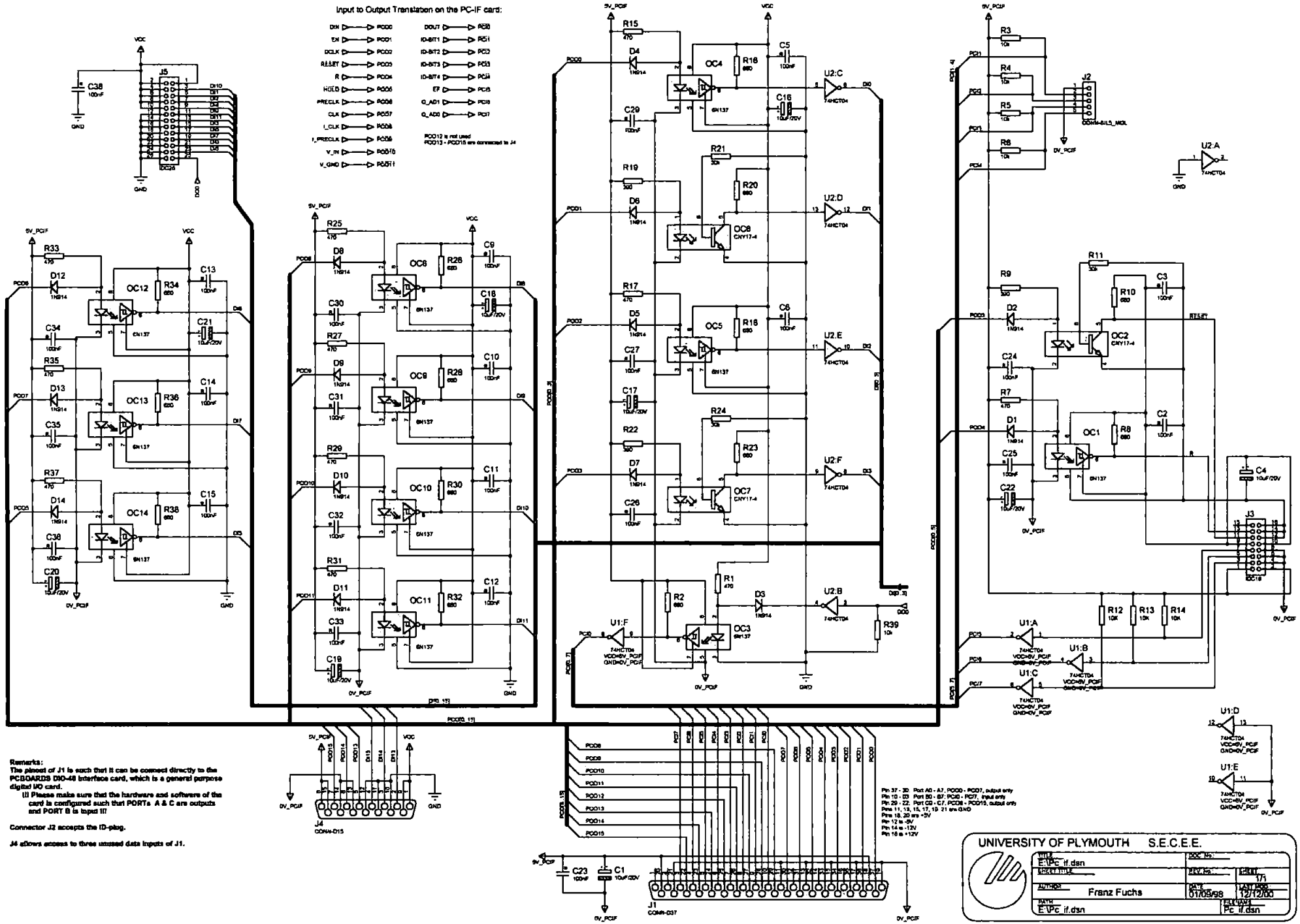
Schematic for the Analog/Digital converter to Base Board interface board (Base-AD2.DSN).

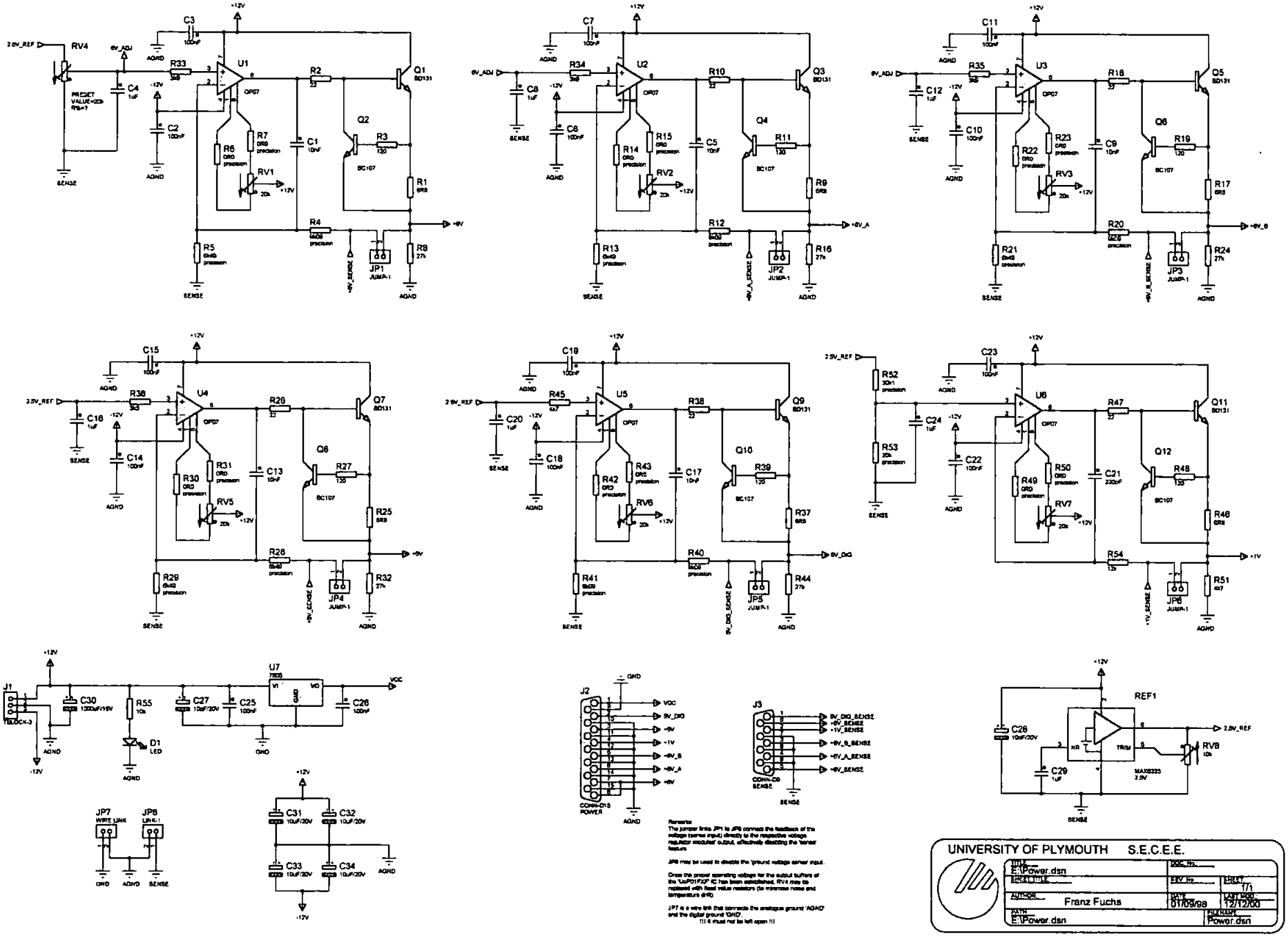


Remarks:
With JP1 & JP2 the two A/D converter inputs can
a) for calibration purposes be connected.
b) be connected to 'IN' and 'OUT' of the experimental amplifier structures (BufferAmp & NSharedBuffer) on the UoP01FXF IC.
c) probe any two signals using test leads that can be plugged into the 1mm jumper-link sockets.

UNIVERSITY OF PLYMOUTH S.E.C.E.E.		
TITLE: E:\Base-ad2.dsn	DOC No.	
SHEET TITLE	REV No.	SHEET 171
AUTHOR: Franz Fuchs	DATE: 01/09/98	LAST MOD. 12/12/00
PATH: E:\Base-ad2.dsn	FILENAME: Base-ad2.dsn	

Schematics for the Computer Interface board and the Power Supply board (PC_IF.DSN & POWER.DSN).


Input to Output Translation on the PC-IF card:
DIN
EN
DCLK
RESET
R
HOLD
PRECLK
CLK
I_CLK
I_PRECLK
V_IN
V_GND
DOUT
ID-BIT1
ID-BIT2
ID-BIT3
ID-BIT4
EF
Q_AD1
Q_AD0
PD12 is not used
PD13 - PD15 are connected to J4
Remarks:
The pinout of J1 is such that it can be connect directly to the PCBGARDS D90-48 interface card, which is a general purpose digital I/O card.
!!! Please make sure that the hardware and software of the card is configured such that PORTs A & C are outputs and PORT B is input !!!
Connector J2 accepts the ID-plug.
J4 allows access to three unused data inputs of J1.
UNIVERSITY OF PLYMOUTH S.E.C.E.E.
Franz Fuchs
E:\Pc if.dsn
01/05/98
12/12/00


RV4
U1
U2
U3
U4
U5
U6
U7
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
REF1
J1
J2
J3
D1
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
UNIVERSITY OF PLYMOUTH S.E.C.E.E.
Franz Fuchs
E:\Power.dsn
01/09/98
12/12/00

I. Jumper and passive components settings for the custom IC test-rig.

Custom IC Test-Rig Configuration

Board Config. / Cell/ Action	Chip-Control Word (in hex-format) Add 1 if the Local-Bit is set.	JP1 cap in	JP2 IV	JP3 6VSF	JP4 BNC GND	JP5 V_GND	JP6 prec lk	JP7 clk	JP8 Subst.	JP9 GND Link	JP10 I_SF	JP11 I_BUF	JP12 I_CLK	JP13 I_PRECLK	JP14 V_TEST	JP15 Dout	J11 Cap	C31 IV	C311 Input	C312 cap in	C39 DUT out1	C40 DUT out2	C57 Input	R30 Input	R31 clk	R32 prec lk	M1 CLK_COND
Board Name	-	Base																									
RESET	-	x	x	x	1^3	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Shift Test	0101	x	x	x	1^3	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
2u0x0u8_sym	0202	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	c_{13}
2u0x0u8_S&H	0208	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	x_{13}
2u0x0u8_RGND	0210	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
2u0x0u8_PCap	0220	1	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	x_{13}
2u0x0u8_RCh	0240	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
2u0x8u15_sym	0402	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	c_{13}
2u0x8u15_asym	0404	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	c_{13}
2u0x8u15_S&H	0408	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	x_{13}
2u0x8u15_RIn	0410	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
2u0x8u15_PCap	0420	1	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	x_{13}
2u0x8u15_RCh	0440	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
2u0x8u15_RGND	0480	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
8u8x8u15_sym	0802	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	c_{13}
8u8x8u15_asym	0804	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	c_{13}
8u8x8u15_S&H	0808	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	x_{13}
8u8x8u15_RIn	0810	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
8u8x8u15_PCap	0820	1	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	x_{13}
8u8x8u15_RCh	0840	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}
8u8x8u15_RGND	0880	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	p	p	o	o	p	o	p	p	z_{13}

Table I-1: Jumper and passive component settings for the S&H evaluation with a DC input signal taken from J16 and applied to J3 (DUT Input).

Board Config. / Cell/ Action	Chip-Control Word (in hex-format) Add 1 to it if the Local-Bit is set.	JP1 cap in	JP2 1V	JP3 6VSF	JP4 BNC GND	JP5 V_GND	JP6 prec lk	JP7 clk	JP8 Subst.	JP9 GND Link	JP10 I_SF	JP11 I_BUF	JP12 I_CLK	JP13 I_PRECLK	JP14 V_TEST	JP15 Dout	J11 Cap	C33 1V	C31 Input	C32 cap in	C39 DUT out1	C40 DUT out2	C57 Input	R30 Input	R31 clk	R32 prec lk	M1 CLK_COND
Board Name	-	Base																									
RESET	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Shift Test	0101	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
2u0x0u8_sym	0202	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	o	p	o	o	o	o	p	p	c_{13}
2u0x0u8_S&H	0208	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	x_{13}
2u0x0u8_RGND	0210	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
2u0x0u8_PCap	0220	1	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	x_{13}
2u0x0u8_RCh	0240	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
2u0x8u15_sym	0402	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	o	p	o	o	o	o	p	p	c_{13}
2u0x8u15_asym	0404	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	o	p	o	o	o	o	p	p	c_{13}
2u0x8u15_S&H	0408	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	x_{13}
2u0x8u15_RIn	0410	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
2u0x8u15_PCap	0420	1	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	x_{13}
2u0x8u15_RCh	0440	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
2u0x8u15_RGND	0480	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
8u8x8u15_sym	0802	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	o	p	o	o	o	o	p	p	c_{13}
8u8x8u15_asym	0804	3	c	1	1^3	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	o	p	o	o	o	o	p	p	c_{13}
8u8x8u15_S&H	0808	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	x_{13}
8u8x8u15_RIn	0810	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
8u8x8u15_PCap	0820	1	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	x_{13}
8u8x8u15_RCh	0840	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}
8u8x8u15_RGND	0880	x	c	1	1^3	1	x	3^1	c^o	o	3^1	3^1	1	1	1	1	2	p	o	p	o	o	o	o	p	p	z_{13}

Table I-2: Jumper and passive component settings for the S&H evaluation with an AC signal; applied to J3 (DUT Input).

Board Config. / Cell/ Action	Chip-Control Word (in hex-format) Add 1 to it if the Local-Bit is set.	JP1 capin	JP2 IV	JP3 6VSF	JP4 BNC GND	JP5 V_GND	JP6 preclk	JP7 clk	JP8 Subst.	JP9 GND Link	JP10 I_SF	JP11 I_BUF	JP12 I_CLK	JP13 I_PRECLK	JP14 V_TEST	JP15 Dout	J11 Cap	C33 IV	C31 Input	C32 capin	C39 DUT out1	C40 DUT out2	C57 Input	R30 Input	R31 clk	R32 preclk	M1 CLK_COND
Board Name	-	Base																									
RESET	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Board Calibration	0101	x	x	x	x	3	x	x	x	x	x	x	3	3	3	3	x	x	x	x	x	x	x	x	x	x	o
2u0x0u8_sym	0202	3	c	1	1	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	
2u0x8u15_sym	0402	3	c	1	1	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	
2u0x8u15_asym	0404	3	c	1	1	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	
8u8x8u15_sym	0802	3	c	1	1	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	
8u8x8u15_asym	0804	3	c	1	1	1	3^1	3^1	c^o	o	3^1	3^1	1	1	1	1	2^1	p	p	p	o	o	p	o	p	p	
CapCell Top Plate	1002	x	1^*	3	x	1	x	x	x	o	x	x	1	1	1	1	2	o	x	x	o	o	x	x	p	p	x
CapCell Bottom Plate	1004	x	1^*	3	x	1	x	x	x	o	x	x	1	1	1	1	2	o	x	x	o	o	x	x	p	p	x
teststrus 25u0x1u5_R	1010	2^*	c	1	x	1	x	x	x	o	x	x	1	1	1	1	2	p	o	o	o	o	o	o	p	p	z_{13}
teststrus 8u8x8u15_R	1020	2^*	c	1	x	1	x	x	x	o	x	x	1	1	1	1	2	p	o	o	o	o	o	o	p	p	z_{13}
teststrus 2u0x8u15_R	1040	2^*	c	1	x	1	x	x	x	o	x	x	1	1	1	1	2	p	o	o	o	o	o	o	p	p	z_{13}
teststrus 2u0x0u8_R	1080	2^*	c	1	x	1	x	x	x	o	x	x	1	1	1	1	2	p	o	o	o	o	o	o	p	p	z_{13}
BufferAmp	2000	x	c	1	x	1	x	x	x	o	3^1	3^1	1	1	1	1	o	p	o	x	o	o	o	*p*	p	p	x
NSharedBuffer	4000	x	c	1	x	1	x	x	x	o	3^1	3^1	1	1	1	1	o	p	o	x	o	o	o	*p*	p	p	x

Table I-3: Jumper and passive component settings for the evaluation of Circuit and Process parameters.

Legend for Table I-1 to Table I-3:

c	Jumper closed.
c^o	Jumper normally closed, but may in an alternative setting be left open.
c_{13}	Pin 13 or Jumper on CLK_COND module carrying the "preclk" connected/closed.
o	Jumper open or device not present.
p	Device present.
x	Don't care.
x_{13}	Don't care condition for Pin 13 or Jumper on CLK_COND module carrying the "preclk".
z_{13}	Pin 13 or Jumper on CLK_COND module carrying the "preclk" isolated/open.
1	Jumper-Link must be in position 1-2.
1^3	Jumper-Link normally in position 1-2 may in an alternative setting be in position 3-2.
1^*	Capacitance of CapCell available between Pin 1 of the Jumper and AGND.
2	Jumper-Link must be in position 2-S.
2^*	Channel-Impedance of "teststrus" available between Pin 2 of the Jumper and "Input" (J3).
3	Jumper-Link must be in position 3-2.
2^1	Jumper-Link normally in position 2-S may in an alternative setting be in position 1-S.
3^1	Jumper-Link normally in position 3-2 may in an alternative setting be in position 1-2.

Signed .....