Indian Journal of Geo Marine Sciences
Vol. 48 (05), May 2019, pp. 716-723

A grid-connected asymmetrical cascaded H-bridge 81 level inverter with single PV unit and voltage splitting multi winding isolation transformer in marine applications

Sivagama Sundari Meenakshi Sundaram[1] & Selvaperumal Sundramoorthy[2]*

[1]Department of Electrical and Electronics Engineering, Amrita College of Engineering & Technology, Nagercoil, Tamilnadu, India

[2]Department of Electrical and Electronics Engineering, Syed Ammal Engineering College, Ramanathapuram, Tamilnadu, India.

*[E-mail: perumal.om@gmail.com]

Received 09 September 2017; revised 02 May 2018

In this paper, an asymmetrical cascaded H-bridge 81 level inverter powered by a single photo voltaic (PV) unit is presented. The PV unit drives an interleaved soft switched boost converter that drives a simple three level inverter, which in turn drives a multiple secondary winding transformer. The AC output of the four isolated secondary windings of the transformer is rectified and filtered to deliver four isolated DC voltages in the ratio 1:3:9:27. The system incorporates maximum power point tracking at the front end boost DC-DC converter level. Overall reduced THD is achieved by strategically spacing on the time axis, for each AC cycle, the discrete voltage levels of the 81 level inverter. The mathematical formulation, the results of simulation in the MATLAB/SIMULINK environment and the results of experimental verifications are provided.

[**Keywords:** Interleaved soft switched boost converter; Photovoltaic power generation; Multilevel inverter; Maximum power point tracking; Harmonic mitigation; Power quality]

Introduction

Photovoltaic power conversion systems (PVPCS) are becoming very popular because of their advantages. Despite the initial cost, the PVPCS are encouraged in both domestic and industrial sectors. Considering the initial cost and vast range of power capacities ranging from few tens of watts to several hundred megawatts, it is therefore necessary that PVPCS are operated in the most efficient manner. There are three issues associated with the overall efficiency of any PVPCS: The maximum power tracking (MPPT) incorporated into any of the power conversion stages, the electrical efficiency of the power conversion stages and the handling of harmonics if the overall output is AC[1].

Typically, in a simple PVPCS with a single DC-to-DC converter, with a front-end buck, boost, or buck boost converter it is possible that the PV panels are not delivering continuous power by virtue of the switching nature of the converter. This does not justify full utilization of the installed capacity. If, for example, the front-end DC-to-DC converter is of the buck or the buck boost configuration, then the PV panels are electrically disconnected from the rest of the system during the off periods of the PWM switching signals. In an average day of 12 hours, over which the solar irradiation is available at different degrees, if the average duty cycle of the PWM based converters are just 50%, then the PV panel is essentially working only for a period of six hours. Besides, the DC-to-DC converters of the generic types exhibit a large ripple contained in the DC output voltage and require large passive filter devices. These two issues are addressed in this paper by adopting an interleaved boost conversion system with two sets of interleaved boost converters. The interleaving of two boost converters naturally leads to twice the switching losses, and this issue is addressed by employing soft switching of the two-converter switches[2].

In the scheme presented in this paper, apart from an intermediate inverter, transformer and rectifier stages, the final stage of the power conversion employs a set of four numbers of cascaded H bridge units. Various topologies for multilevel inverters have been proposed over the years. Common ones are: Diode-clamped[3,4,5,6,7,8], flying capacitor[9], cascaded H-bridge, and modified H-bridge multilevel[10,11,12,13,14]. Cascaded H bridges need isolated DC power sources

and in this particular application since there were four cascaded H bridges, four isolated DC voltage sources were needed.

In this system of power conversion, only a single photovoltaic panel was used and this single DC source split up into four isolated DC voltage sources. For this purpose, we used an intermediate DC to AC conversion system employing a single H-bridge inverter unit with appropriate passive filtering devices to ensure minimal hysteresis and eddy current losses in the multi secondary transformer that comes after the single H-bridge inverter. The four isolated DC voltages are required to be in the ratio 1:3:9:27, which was achieved by using the appropriate transformer secondary turns. The four secondary windings of the transformer individually drive four full wave rectifier units.

Multilevel inverters offer AC voltages of waveform closer to the sinusoidal waveform with reduced THD. Minimization of THD can be achieved by adopting different pulse width modulation techniques, such as the Sinusoidal PWM (SPWM) and the Space Vector PWM (SVPWM). The SPWM and the SVPWM belong to the high frequency PWM category that incurs large switching losses; these methods are not suitable for low power PVPCS. For efficient power conversion with minimal THD in the AC output, the inverter should operate at low switching frequency. Low switching frequency operated step modulation schemes are more suitable for multi-level inverters for low and medium power ranges of PVPCS.

In a step-modulated cascaded multilevel inverter, the output AC voltage waveform is synthesized in steps of the various levels of DC voltages with durations of each step strategically distributed over the time axis throughout the positive and negative half cycles. For step-modulated cascaded H-bridge inverters with few DC voltage levels, typically 5, 7, 9 or 11 levels, it is sufficient to estimate only the durations of applications of these fewer levels of DC voltages. In such cases, the timing or switching instants pertaining to the multilevel of DC voltages are estimated using offline techniques or online techniques.

However, in this research, a multilevel inverter with steps as large as 81 were proposed. As such, it was not possible to estimate such a large number of switching angles as may be required; and hence the SHE PWM strategy of mitigation of selected harmonics cannot be applied. However, a simple but novel scheme was adopted in this paper. The distribution of the durations of the 81 levels of DC voltages was decided based on the sine law with the highest level enjoying the maximum duration, gradually falling towards the zero level according law.

An asymmetrical cascaded multilevel inverter shown in Figure 1 can be defined as a multilevel converter fed by a set of DC voltage source where at least one of them is different from the other one. The main advantage of an asymmetrical multilevel converter is that it uses less number of semiconductor switches than that with symmetrical topology. One interest of the asymmetrical configurations is that the number of levels is higher with the same number of cells.

Figure 2 shows the block diagram of the proposed method. The PV unit drives an interleaved soft switched boost converter (ISSBC) that drives a simple three-level inverter, which drives a multiple secondary winding transformer. A transformer with a single primary winding and four secondary windings was used. The number of turns in the primary winding was 81 and the number of secondary winding turns was 1, 3, 9 and 27. The two switches of the ISSBC were operated with the same duty cycle, as the load

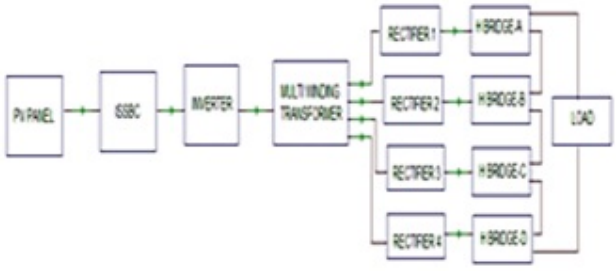

Fig. 1 — Asymmetrical cascaded multilevel inverter for marine applications

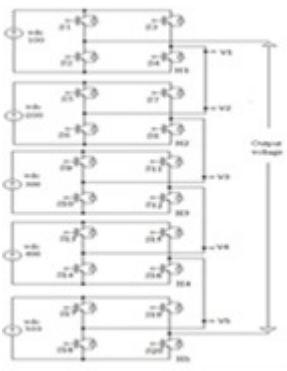

Fig. 2 — Block diagram of multiloop interleaved control

and source side scenario is the same for the interleaved sections of the ISSBC. The two switches of the ISSBC were operated with the zero voltage switching (ZVS) strategy for which additional resonant inductors and capacitors were used. Next to the ISSBC in the power conversion chain comes the intermediate three-level inverter. An H bridge arrangement of MOSFET switches was employed and the inverter worked at a nominal frequency of 2 KHz. Such a high frequency was selected so that a ferrite core transformer with more power density could be used to reduce the size of this stage. Since the power rating of the PV panel used was 125 watts, an inverter with sufficient rating was used with switching devices and the filter components. In this ISSBC unit MPPT algorithm was implemented. The duty cycles for the two switches would be the same and as dictated by the incremental conductance MPPT algorithm. The AC output of the four isolated secondary windings of the transformer was rectified and filtered to deliver four isolated DC voltages in the ratio 1:3:9:27. The system incorporated maximum power point tracking (MPPT) at the front-end boost DC-DC converter level.

Photovoltaic Panel

The photovoltaic panel can be treated as a variable power capacity DC generator with variations in power sourcing abilities dictated every moment by the insolation level and temperature prevailing at the moment of consideration. If the solar insolation and the temperature are considered practically constants then the power output will also be practically constant. For maximum transfer of power from a source to a load it is essential that the load impedance match with the source impedance. If the actual load impedance cannot be made equal to the source impedance then a loss-free impedance matching arrangement has to be introduced in between the source and the load.

In practice, the DC-to-DC converters that find place in between the source and load in typical PVPCS essentially match the resistance on the source and load sides ensuring maximum flow of power from the source to the load.

With reference to the I-V characteristics shown in Figure 3 and the P-V characteristics of the photovoltaic panel shown in Figure 4, it is obvious that at various insolation levels, there exists a point in the PV curve where the power is maximum and corresponding to that voltage there exists a current pertaining to maximum power in the V-I curve. If the particular voltage and the current are maintained at the corresponding insolation level then maximum power is obtained. Of the many available techniques for MPPT, the incremental conductance method is a more deterministic method and this method has been adopted for the marine application[15,16,17,18,19,20,21,22,23,24]. With reference to the PV characteristics, it can be noted that the point of maximum power is where the rate of change of power is zero with respect to change in the voltage. That is, MPP occurs when $\frac{dp}{dv}$=0.

This implies that $\frac{dp}{dv}=\frac{Idv}{dv}+\frac{vdi}{dv}$ and hence $\frac{dp}{dv}=I+\frac{vdi}{dv}$ and further at MPP. Since at MPP $\frac{dp}{dv}=0$; $I+\frac{Vdi}{dv}=0$; that results in the condition of MPP to occur when $\frac{di}{dv}=-\frac{I}{V}$. If this condition is satisfied for a particular duty cycle the duty cycle is not disturbed. However, if $\frac{di}{dv}>-\frac{I}{V}$ the duty cycle will be increased and if $\frac{di}{dv}<-\frac{I}{V}$ then duty cycle will be reduced.

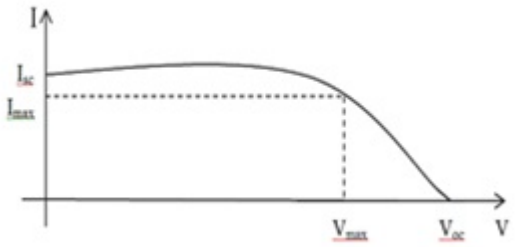

Fig. 3 — PV current voltage curve

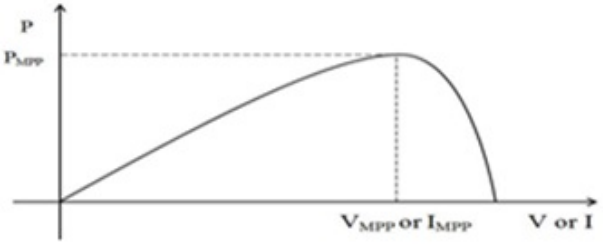

Fig. 4 — PV power curve

Mathematical Formulation

The circuit arrangement consists of five numbers of cascaded H-bridges inverter units. These inverter units are operated with a set of 20 gating pulses derived from a control unit. The control unit sends out the gating pulses in accordance with the timing rule. The output of the cascaded H-bridge inverter consists of 81 levels. If equally spaced the waveform will be triangular. What we needed was a waveform nearer to a sinusoidal wave, 81 voltage levels were applied in accordance with a certain law that makes the waveform closer to a sinusoidal waveform. The easiest way was to switch on the DC levels in accordance to the rate of change of voltage that occurs in a sinusoidal wave.

The rate of change of voltage levels in a sinusoidal waveform can be given by the expression $\frac{d(VmSinwt)}{dt}$ = V_m Coswt. Therefore, at the zero crossing, the rate of change of voltage will be maximum with a factor of multiplication of 1 and as the wave progresses the duration of each voltage level will be for longer $\frac{dp}{dv} = I + \frac{vdi}{dv}$ and further at MPP. Since at MPP $\frac{dp}{dv} = 0$; $I + \frac{Vdi}{dv} = 0$ that results in the condition of MPP to occur when $\frac{di}{dv} = -\frac{I}{V}$. If this condition is satisfied for a particular duty, cycle the duty cycle is not disturbed. However, if $\frac{di}{dv} > -\frac{I}{V}$ the duty cycle will be increased and if $\frac{di}{dv} < -\frac{I}{V}$ then duty cycle will be reduced durations. Considering the requirement of the quarter wave symmetry of the synthesized multilevel output of the inverter, the number of levels in all the quarters of a cycle will be equal and it should be equal to 81 including the zero voltage level. For a 50 Hz output, a period of 5 ms will be shared by the 81 levels in each quarter of a cycle. However, the duration of presence of each level is not the same.

Since the topology is a case of cascading a number of voltages in series, it can be viewed that each level is like a DC source coming in series entering into the chain one after the other with the zero level always present and the maximum level coming in series only for a short period of time. The zero level is there in series for the entire 5 ms period in every quarter of a cycle. The next level (=1V), which enters into the series chain a little later will be in series for a period less than 5 ms. The delay δ for each level in entering into the series chain is denoted by δ_i where i vary between 0 and 80. Thus, δ_0 is the delay for the 0 V level and δ_{80} is the delay for the 81st level. The delay δ for each level can be given by a general expression, δ_i=sin ((π/2)*(i/81)) (1)

According to the above equation, the duration of existence of each voltage level in the cascaded chain can be derived and it is clear that the zero level comes into the series chain with zero delay and exists there all throughout the 5 ms period of a quarter waves. The inclusion of the 80th level is delayed by a factor of δ_{81}=sin ((π/2)*(80/81)) =80/81 = 0.988 and this voltage level exists in the series voltage chain for a period of (1-80/81)*5 ms.

Simulation Results

The performance of the cascaded H-bridge 81-level inverter powered with PV unit is determined through MATLAB/SIMULINK software. The main blocks of the entire works are: Photovoltaic panel interleaved soft switched boost converter, intermediate inverter, Multi winding transformer and 81-level inverter topology. The control sections are incremental conductance MPPT unit, output voltage regulating unit and timing or switching unit for the multi-level inverter. The elements and the parameters considered for simulation are presented in Table 1.

The simulation model of grid-connected PV system is shown in Figure 5, and the subsystem is shown in Figure 6. The simulation model of proposed asymmetrical cascaded H-bridge 81-level inverter topology is shown in Figure 7. The output voltage

Table —1 Simulation parameters

Parameters	Values
No. of H-Bridges	4
No. of Power electronic Switches	5
DC source voltage for individual H- bridges A,B,C and D	10V,30V.90V, 270V
Fundamental frequency	50Hz
No. of Diodes	4
Insolation Input	900W/sq.m
Short circuit current	65.4A
Open circuit voltage	46V
No. of multi-winding transformer	4
Current at P_{max}	59.4A
Voltage at P_{max}	36V

Fig. 5 — Simulink model of PV system

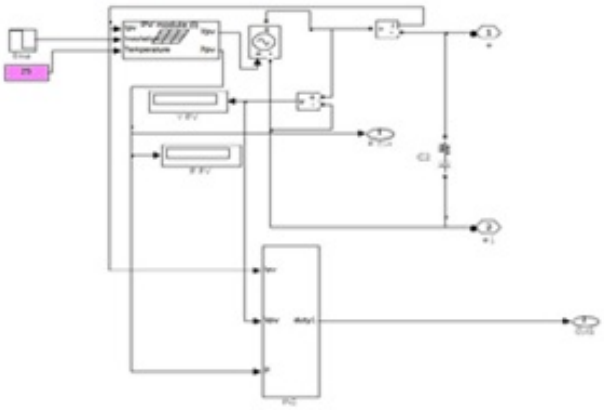

Fig. 6 — Simulink model of PV sub-system

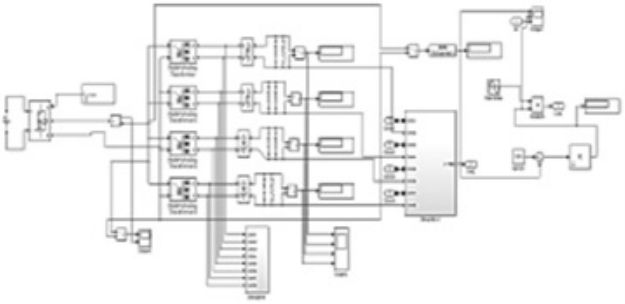

Fig. 7 — Proposed topology

and current waveform of the proposed topology are shown in Figure 8&9. Figure 10, which shows the harmonic spectrum of the inverter output current, confirms the results where the simulated value of current THD is 1.68%. Table 2 shows modulation index versus RMS voltage for 3,9,27 and 81 levels. Table 3 shows modulation index versus voltage THD (%) for 3,9,27 and 81 levels. Figure 11 shows the modulation index versus voltage THD (%) graph for 3,9,27 and 81 levels.

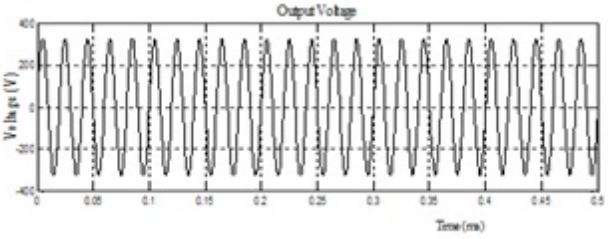

Fig. 8 — Output voltage waveform.

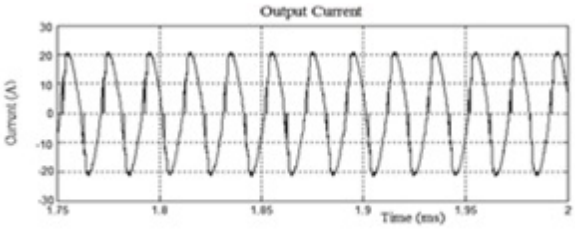

Fig. 9 — Output current waveform

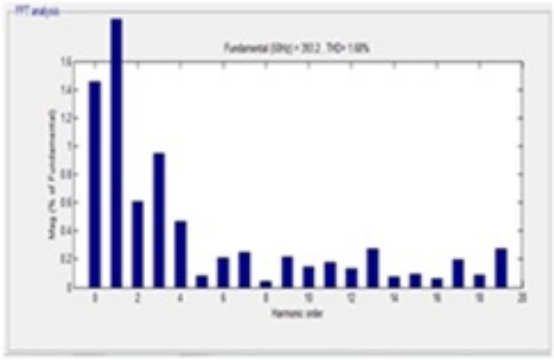

Fig. 10 — Harmonic spectrum of output current

Table 2 — Modulation index versus RMS voltage

Modulation Index	Fundamental RMS Voltage			
	3 Level	9 Level	27 Level	81 Level
1	322	385.5	396	397.1
0.9	282.4	352.6	366.2	366.2
0.8	235	308.2	324	324
0.7	198.2	245.5	276.	274.4
0.6	181.2	212.3	243.1	243.1
0.5	161.8	183.4	199.3	199.3

Table 3 — Modulation index versus voltage THD (%)

Modulation Index	Voltage THD (%)			
	3 Level	9 Level	27 Level	81 Level
1	29.57	9.35	3.43	1.95
0.9	29.59	9.38	3.47	1.91
0.8	29.6	9.41	3.52	1.89
0.7	29.62	9.44	3.55	1.86
0.6	29.63	9.46	3.59	1.8
0.5	29.66	9.48	3.62	1.76

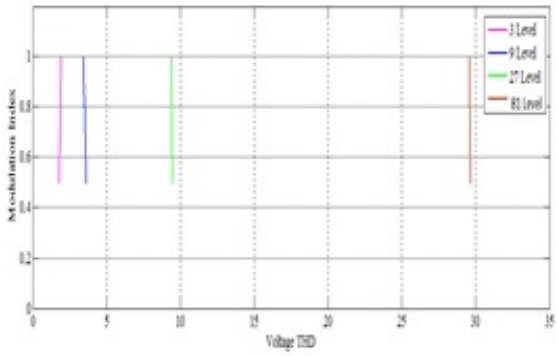

Fig. 11 — Modulation index versus voltage THD (%) graph

Table 4 ─ Voltage levels

Level	Logic	Components	Resultant
0	0	0	0
1	1	4.242V	4.242V
2	3-1	12.726V-4.242V	8.484V
3	3	12.726V	12.726V
…….	…….	…….	…….
…….	…….	…….	…….
80	80	114.534+38.178 +12.726+4.242V	169.68V

Experimental Results

An experimental verification to validate the proposed 81-level inverter and is shown in Figure 11. The main sub-systems of the experimental hardware set-up are solar photovoltaic panel (250 W & 22.2 V), boost converter, single phase H-bridge inverter, multi output transformer 230/81, 27, 9, 3 Rectifier and filter units and cascaded H-bridge inverters (4 Nos).

The solar photovoltaic panel of power rating 250 W is used as the main power source. The specifications of the panel at 1000 w/m^2 and 25 ^{0}C are P_{max} = 250 W, V_{oc} = 44.4V, V_{pmax} = 34.4 V, I_{pmax} = 7.27A, I_{sc} = 9.385 A.

The boost converter was used to boost this voltage to the required high level. Sliding mode control was used to control the boost converter to ensure maximum power point tracking. The nominal value of the output DC voltage of the boost converter appearing across the DC input terminals of the single-phase inverter is around 250 V. The single-phase H-bridge inverter inverts this DC link voltage to a single phase AC at 50 Hz. Followed by the inverter is a T connected low pass filter (Table 4)

The AC output of the single-phase inverter is fed to the single-phase transformer with four separate AC output voltages. The four AC voltages are 3V, 9V, 27 V and 81V. Each of the four-cascaded H-bridges was constructed using MOSFETs IRF 840. The output of each of the H bridges was connected in series. The entire control mechanism was implemented using PIC micro controller 16F877A. For the control of the four MOSFETS of the four bridges, 16 control bits are required. Two ports of the PIC micro controller PORT B and PORT C were used for this purpose. The 16 output bits of the micro controller were fed to the gate terminals of the MOSFETs through 16 opto couplers. IC MCT2E is used for this purpose. For powering up the MCT2E ICs on the output side, separate individual and isolated DC power sources were used.

Fig. 12 — Experimental prototype

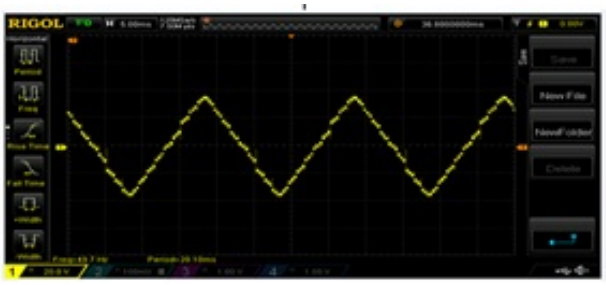

Fig. 13 — Output voltage waveform

The four individual voltages in the order of 1:3:9:27 were rectified and filtered using the 1N40007 bridge rectifiers, and each output filtered with 2200 MFD capacitors and the filtered DC voltages amounts to 3*1.414 = 4.242 V , 9*1.414 = 12.726 V, 27 * 1.414 = 38.178 V, 81*1.414 =114.534 V, respectively.

The peak value obtained in the forty-one level inverter is 169.68 V. Thus, the maximum obtainable RMS value of the fundamental AC wave of 50 Hz will be = ((4 *V_{dc})/pi) MI/1.414 V. With MI = 1, the output AC voltage at 50 Hz becomes 4*169.68 /3.14/1.414 V = 152.8 V.

Figure 12 shows the output voltage waveform. Figure 13 shows the output current waveform.

Fig. 14 — Output current waveform

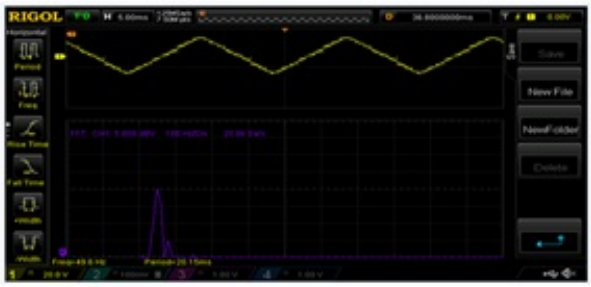

Fig. 15 — Harmonic spectrum of output voltage

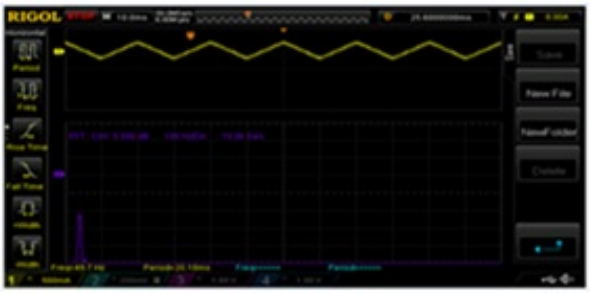

Fig. 16 — Harmonic spectrum of output current

Table 5 — Parameters of the cascaded H-Bridge inverter

Parameters	Values
No. of H-bridge levels	4
No. of Switches MOSFET IRF840 – 16 Nos.	500V,8A
Fundamental frequency	50Hz
Photovoltaic panel	250W
Multi-winding output transformer	230/81,27,9,3 V
Opto-couplers MCT2E (16 Nos.)	30V,3A
Filter Capacitor	2200µF
Transformers (1 No.)	0-24V,2A
Resistor	0.2 Ohm
Lamp	60W
Transformers (3 Nos. for each individual H-bridge)	6V-0-6V,500mA

Figure 14, 15 and 16 shows the harmonic spectrum of the inverter output voltage and output current.

The elements and the parameters considered for implementation are presented in Table 5. Table 6 gives a comparison of THD of the output current; it is clear that the results of simulation are nearer to the experimental results.

Table 6 — Comparison of the output current

Current THD(%)	
Experimental	Simulation
1.92	1.68

Conclusion

In this paper, an asymmetrical configuration of cascaded H-bridge 81-level inverter for grid connected PV system has been presented which is used in industrial and marine applications. The mathematical formulations have been provided and the performance of the proposed inverter topology was simulated using MATLAB. It may be concluded from the simulation and experimental results that the cascaded H-bridge 81-level inverter provides output with reduced total harmonic distortion by strategically spacing on the time axis for each AC cycle.

Acknowledgement

Authors are grateful to Dr.Chinnadurai Abdullah, Correspondent, Syed Ammal Engineering College, Ramanathapuram, Tamil Nadu, India, for providing facilities and encouragement to carry out the above research work.

References

1 Daher, S., Schmid, J., Fernando, L. and Antunes, M, "Multilevel inverter topologies for stand-alone PV systems", *IEEE Transactions on Industrial Electronics*.Vol.55,No.7, pp.2703-2712, July 2008.

2 Doo-Yong Jung, Young-HyokJi, Sang-Hoon Park, Yong-Chae Jung, and Chung-Yuen Won, "Interleaved Soft-Switching Boost Converter for Photovoltaic Power-Generation System", *IEEE Transactions on Power Electronics,*Vol. 26, No. 4, pp. 1137-1145, April 2011.

3 Roseline, P., Ramesh, B. and Manga Lakshmi Ch, V.V., "Performance Analysis of Twenty Seven Level Asymmetrical Cascaded H-Bridge Multilevel Inverter Fed Three Phase Induction Motor Drive", International Journal of Engineering and Advanced technology, Vol. 4, No. 4, pp. 724-738, Oct 2014.

4 Phani Deepthi, D. and Gandi, Vinay kumar, "A Novel Simplified Single-Phase and Three phase Multistring Multilevel Inverter topology for Distributed Energy Resources", *International Journal of Engineering Research,* Volume No.3, Issue No.4, pp : 206-208 01 April 2014.Vol. 2, Issue 3,pp. 661-665, May - Jun 2012.

5 Sajith, P.C. and Sunitha, K., "Asymmetrical Cascaded 15-Level Inverter Using Single DC-Source", *Journal of Power Electronics*, Vol. 14, No.1, pp. 48-60, January 2014.

6 Li, Y., Vilathgamuwa, D.M. and Loh, P.C., " Design, analysis, and real time testing of a controller for multi bus micro grid system", *IEEE Transactions on Power Electronics,* Vol. 19, No. 5, pp. 1195-1204, Sept. 2004.

7 Jingang Han, Tengfei Yang, DongkaiPeng and Tianzhen Wang, "Capacitor Model predictive control for asymmetrical cascaded H-Bridge multilevel grid-connected inverter with flying", *in Proceeding of IECON 2014*, pp. 1611 – 1616, Nov 2014.

8 Anuradha Singh, Mohit Jain, Suman Singh, "Analysis of THD and Output Voltage for Seven Level Asymmetrical Cascaded H-Bridge Multilevel Inverter using LSCPWM Technique", *International Journal of Computer Applications*, Vol. 112, No. 1, pp.1-6, Feb 2015.

9 Alireza Nami, Firuz Zare Frede Blaabjer and Arindam Ghosh, "A Hybrid Cascade Converter Topology With Series-Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells", *IEEE Transactions on Power Electronics,* Vol 26,No.1,pp. 51-65, January 2011.

10 Anusha, B., Satyanarayana, K., Manga Lakshmi Ch, V. V., "Performance Analysis of Twenty Seven Level POD Modulation based Cascaded H-Bridge Multi Level Inverter Topology", *International Journal of Engineering and Innovative Technology*, Vol. 5, Issue 5, pp.25-31, December 2015.

11 Akanksha Kaiwartya, Abhijit Mondal, Shailesh Deshmukh, "Design of Grid Connected H-Bridge Multi level Inverter with PV System", *International Journal of Science, Engineering and Technology Research* , Vol. 4, Issue 12, pp. 4048-4051, December 2015.

12 Balasundaram, G., Arumugam, S., Dinakaran, C., "Design and simulation of single phase cascaded multilevel grid connected inverter using photovoltaic system", *Journal of Chemical and Pharmaceutical Science,* Vol. 8, Issue 2, pp. 441-449, June 2015.

13 Shaik Abdul Farooq, Bhanu, M., "Photovoltaic System With Various Multilevel Converters", *International Journal of Engineering & Science Research*, Vol.2, Issue 11, pp. 1612-1623, Nov 212.

14 Dhivya Balakrishnan, Dhamodharan Shanmugam, K.Indiradevi, "Modified Multilevel Inverter Topology for Grid Connected PV Systems", *American Journal of Engineering Research*, Vol. 2, Issue 10, pp.378-384, 2013.

15 Gomathy, V., Selvaperumal, S., "Fault Detection and Classification with Optimization Techniques for a Three-Phase Single-Inverter Circuit", *Journal of Power Electronics*, 16, no. 3 (2016) 1097-1109.

16 Selvaperumal, S., Pugazhenthi, P., Nedumal, Amudha, A., "Closed loop performance investigation of various controllers based chopper fed DC drive in marine applications", *Indian Journal of Geo-Marine Sciences (IJMS)*, 46(2017) 1044-1051.

17 Selvaperumal, S., Vijayarajan, S., Pugazhenthi, P. Nedumal, Prabhakar, G., Nagarajan, R., "Performance Investigation of Genetic Algorithm Based LCL Resonant Converter in Marine Applications", *Indian Journal of Geo-Marine Sciences (IJMS)*, 45(2016) 1377-1388.

18 Rajmohan, Rajalaksmi, Vairamani, Rajasekaran., Selvaperumal, S., "Reactive power compensation and harmonic mitigation through quasi Z source converter for marine applications", *Indian Journal of Geo-Marine Sciences (IJMS)*, 45(2016) 897-910.

19 Selvaperumal, S., and Christober Asir Rajan, C., "Design and experimental investigation of a full bridge series-parallel resonant inverter", *Electronics Computer Technology (ICECT), 2011 3rd International Conference on*. Vol. 2. IEEE, 2011

20 Selvaperumal, S., Muralidharan, S., Nedumal Pugazhenthi, P., Prabhakar, G., Nazare, J., Parthiban, P.G., Karuppa Samy, P., "Performance Investigation of SHE PWM Implementation of GA Based LCL Resonant Inverter in Marine Applications", *Indian Journal of Geo-Marine Sciences (IJMS)*, 46(2017) 1889-1898.

21 Kavitha, I., Selvaperumal, S., Pugazhenthi, P.N., Mohamed Rajithkhan, A., Jagatheesan, R., "Performance Investigation of PI Controller based Chopper fed DC Drive", *Applied Mechanics & Materials* 573 (2014).

22 Selvaperumal, S., and Christober Asir Rajan, C., "Micro-Controller Based LCC Resonant Converter Analysis, Design, and Simulation Results", *International Journal of Computer and Electrical Engineering*, 1, no. 3 (2009) 323-326.

23 Antony Albert, AV, Rajasekaran, V, Selvaperumal., S, "Harmonic elimination of H-bridge seven level inverter", *Eur J Sci Res*, 65(2011) 594-600.

24 Bindu, J, Selvaperumal, S, Muralidharan, S, Muhaidheen. M, "Genetic algorithm based selective harmonic elimination in PWM AC-AC converter", *2011 International Conference on Recent Advancements in Electrical, Electronics and Control Engineering*. Vol. 1. IEEE, 2011.