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New CMOS based current follower and its applications to inductor simulator and band-pass filter

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A new CMOS based current follower (CF) with externally controllable *X* terminal intrinsic resistor has been proposed in this manuscript. Also, a new electronically tunable grounded inductor simulator using only a grounded capacitor has been proposed. The inductor simulator does not need any external resistors. It can be tuned electronically by changing a control voltage. However, it has a single active component matching condition. The simulations results are given in order to demonstrate the performance of the circuits.

Keywords: Current follower, Voltage follower, Inductor simulator, Band-pass filter

1 Introduction

The use of current-mode (CM) active devices such as second-generation current conveyors (CCIIs) has some potential advantages for example greater dynamic range, wider bandwidth, etc. when compared to their voltage-mode (VM) counter parts for instance operational amplifiers (OAs)[1-3]. Nevertheless, CCIIs have both non-ideal current gain and voltage gain effects which restrain some circuit performance properties such as slew rate, bandwidth and dynamic ranges[4-15]. Therefore, the active devices known as voltage followers (VFs) and current followers (CFs) can be preferred to design of analog integrated circuits (ICs) instead of CCIIs in order to avoid both non-ideal gains effects. Besides, design of analog circuits with CFs and VFs can provide more simplicity and more performance such as wider bandwidth, lower power consumption.

A VF has only non-ideal voltage gain effects while a CF has only non-ideal current gain effects. A number of analog circuits such as oscillators[4,5] a negative impedance converter (NIC)[6],analog filters[7-21]and some simulated inductors[22-54] using various active devices have been presented from past to present in open literature. However, the presented simulated inductors suffer from one or more of the following drawbacks:

(i) Complex internal structure[22,31,34,37,38,41,43,44,48-54]
(ii) External passive resistors[22,24-26,29-37,40,43,44,46-54]
(iii) Excessive number of active device[23-27,29,32,35]
(iv) Lack of electronically controllability[24-26,29-40,43-51]
(v) OAs[42]
(vi) Floating capacitors[27,30,31,33,34,36,37,40,42-44,46,49-51]

In this paper, a new CMOS based voltage controlled dual output CF (VCDO-CF) with *X* terminal intrinsic resistor and a new electronically tunable grounded inductor simulator are proposed. The inductor simulator is composed of a VCDO-CF and a simple voltage controlled VF (VCVF) with externally controllable X terminal intrinsic resistor. Furthermore, it does not require any external passive resistors. In other words, the inductance value of it can be adjusted externally by changing a control voltage. Also, it employs a grounded capacitor; thus, it is suitable for integrated circuit fabrication[52-54]. Nonetheless, it needs a single active element matching constraint. The simulation results are given to demonstrate the performance of the grounded inductor simulator and its band-pass filter application.

2 Proposed Current Follower and Simple Voltage Follower

In non-ideal conditions, the matrix equations for a VCDO-CF and a VCVF are given as, respectively:

$$\begin{bmatrix} V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} R_X & 0 & 0 \\ \alpha & 0 & 0 \\ -\gamma & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad \ldots (1a)$$

$$\begin{bmatrix} I_Y \\ V_X \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \beta & R_X \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix} \quad \ldots (1b)$$

It is seen from Eq. (1) that α is non-ideal current gain of the $Z+$ terminal of the VCDO-CF, γ is

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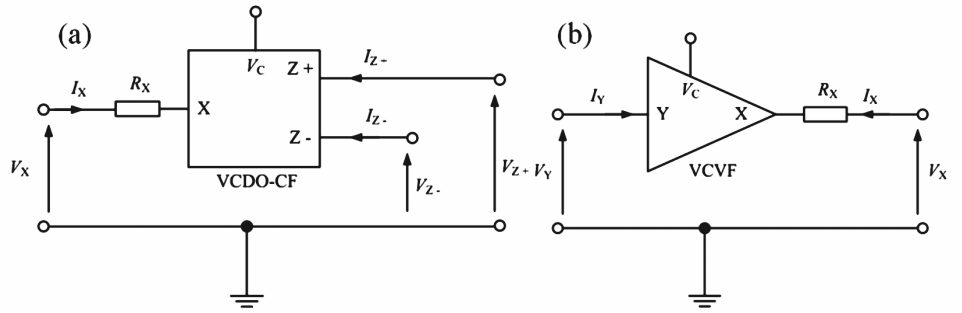

Fig. 1 — (a) VCDO-CF representation (b) VCVF representation

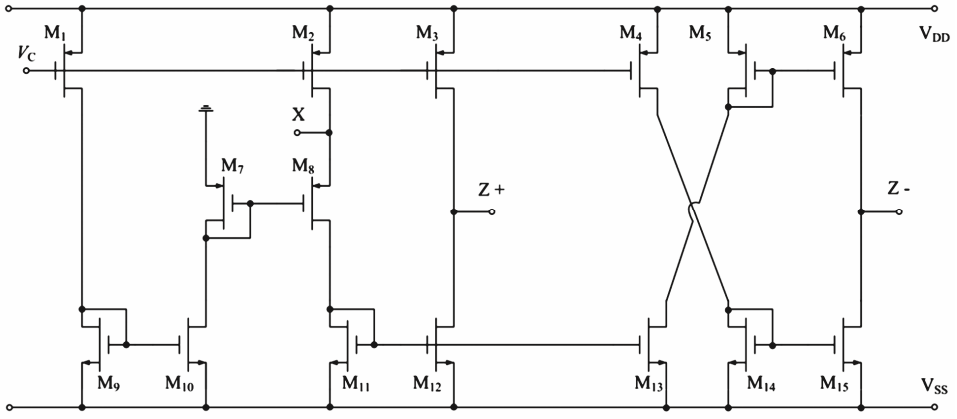

Fig. 2 — The proposed CMOS based VCDO-CF

non-ideal current gain of the *Z*- terminal of the VCDO-CF, β is non-ideal voltage gain of the VCVF and R_X is the *X* terminal intrinsic resistor of the VCDO-CF and VCVF. In ideal conditions, current gain of the *Z*+ terminal of the VCDO-CF and voltage gain of the VCVF are equal to unity. Also, current gain of the Z- terminal of the VCDO-CF is equal to two. The symbolic representation of the VCDO-CF and VCVF are shown in Figs 1(a) and 1(b), respectively.

Internal structure of the proposed VCDO-CF is shown in Fig. 2 and internal structure of a simple VCVF[55] is depicted in Fig. 3. Dimensions of the proposed VCDO-CF are given in Table 1. Also, aspect ratios of the PMOS transistors of the simple VCVF are chosen as $(W/L)_1=(W/L)_2=24\mu m/0.75\mu m$.

All the MOS transistors are operated in saturation region. Also, all the bulks are connected to relevant sources. Transconductances of the NMOS and PMOS transistors are g_{mN} and g_{mP}, respectively. Further, output conductances of the NMOS and PMOS transistors are g_{dsN} and g_{dsP}, respectively. It is assumed that transconductances of all the PMOS and NMOS transistors much greater than their corresponding output conductances ($g_{mN,P}>>g_{dsN,P}$). Some assumptions are performed for the proposed VCDO-CF as follows:

Table 1 —Transistor sizes of the proposed VCDO-CF in Fig. 2

Transistor type	Transistors	*W* (μm)	*L* (μm)
PMOS	M_1-M_5, M_7-M_8	24	0.75
	M_6	48	0.75
NMOS	M_9-M_{14}	50	3
	M_{15}	100	3

$$g_{mM1} = g_{mM2} = \ldots\ldots\ldots = g_{mM5} = g_{mM7} = g_{mM8} = g_{mP}$$
$$g_{mM6} = 2g_{mP}$$
$$g_{mM9} = g_{mM10} = \ldots\ldots\ldots = g_{mM14} = g_{mN}$$
$$g_{mM15} = 2g_{mN} \quad \ldots (2)$$

Similarly, some assumptions are performed for the simple VCVF as $g_{mM1} = g_{mM2} = g_{mP}$. Consequently, *X* terminal intrinsic resistor of both VCDO-CF and VCVF are found as:

$$R_X \cong \frac{1}{g_{mP}} \quad \ldots (3)$$

Transconductance of the PMOS transistor can be calculated as:

$$g_{mP} = \mu_P C_{ox} \left(\frac{W}{L}\right)_P (V_{DD} - V_C - |V_{TP}|)^2 \quad \ldots (4)$$

where μ_P is hole mobility, C_{ox} is oxide capacitance, $(W/L)_P$ is transistor aspect ratio of PMOS, V_{TP} is threshold voltage of PMOS, V_C is control voltage and V_{DD} is positive power supply voltage[56].

3 The Simulated Inductor and VM Band-pass Filter Application

Impedance of the proposed inductor given in Fig. 4 can be computed as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR_{X1}R_{X2} + R_{X1} - R_{X2} \quad \ldots (5)$$

In Eq. (5), if $R_{X1} = R_{X2}$ is selected, the impedance of the proposed inductor simulator turns to:

$$Z_{in} = sCR_{X1}R_{X2} = \frac{sC}{g_{mP}^2} \quad \ldots (6)$$

The impedance of the proposed inductor including non-ideal gain effects is evaluated as:

$$Z_{in} = \frac{sCR_{X1}R_{X2} + R_{X1} + R_{X2}(1-\gamma)}{\alpha\beta} \quad \ldots (7)$$

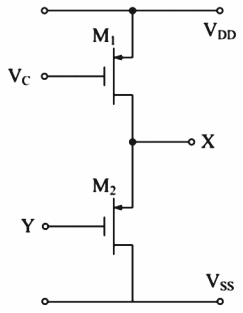

Fig. 3 — Simple VCVF[55]

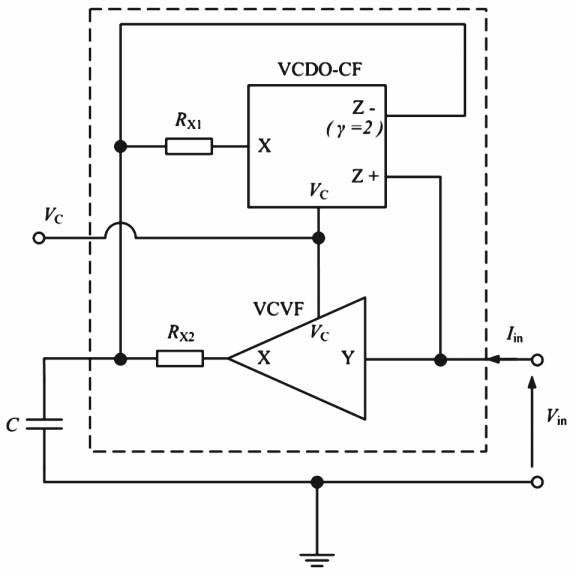

Fig. 4 — The proposed grounded inductor simulator employing a grounded capacitor

In Fig. 5, a VM band-pass (BP) filter with passive circuit elements is shown. The proposed simulated inductor is replaced instead of the passive inductor to examine performance and workability. Transfer function of the BP filter is given as in the following:

$$\frac{V_{out}}{V_{in}} = \frac{s\dfrac{1}{C_f R_f}}{s^2 + s\dfrac{1}{C_f R_f} + \dfrac{1}{LC_f}} \quad \ldots (8)$$

Quality factor (Q) and angular resonance frequency (ω_0) are respectively found as follows:

$$Q = R_f\sqrt{\frac{C_f}{L}} \quad \ldots (9a)$$

$$\omega_0 = \frac{1}{\sqrt{LC_f}} \quad \ldots (9b)$$

4 Simulation Results

0.25 µm standard CMOS technology parameters[57] with ±1.25V symmetrical DC power supply voltages are used in all the simulations. The MOS internal structures of the VCDO-CF and VCVF respectively shown in Figs 2 and 3 are used in all simulations. DC current transfer characteristic of the VCDO-CF in accordance with control voltage is given in Fig. 6. The VCDO-CF

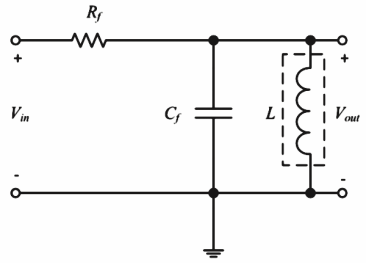

Fig. 5 — VM band-pass filter realization with R, L and C components

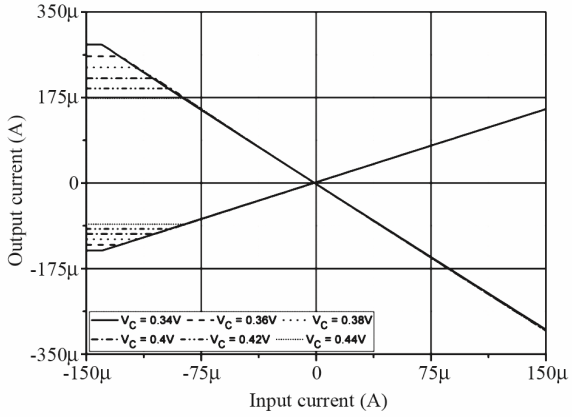

Fig. 6 — DC output current of the VCDO-CF changes with respect to control voltages and input currents

operates properly between 80 µA and 120 µA. Also, *X* terminal intrinsic resistor values of each of the VCDO-CF and VCVF can be changed between 1.66 kΩ (V_C = 0.34 V) and 2.1 kΩ (V_C = 0.44 V) by adjusting control voltages as illustrated in Fig. 7. In Fig. 8, the tunability of the proposed grounded inductor simulator with V_C and *C* is given.

C=100 pF, R_f =20 kΩ and C_f=12.2 pF are chosen in all the simulations below. Not only center frequency (f_0) but also *Q* and bandwidth (BW) change with V_C as indicated in Table 2. Total power dissipation changes versus V_C are given in Fig. 9. It is observed from Fig. 9 that as the control voltage increases, power dissipation decreases. f_0 of the VM BP filter changes with V_C as shown in Fig. 10.

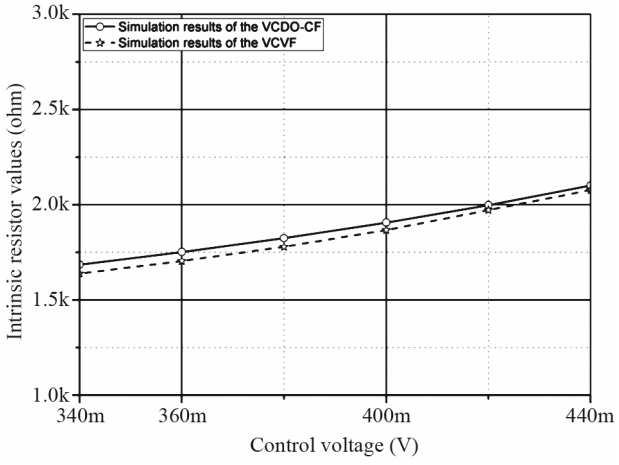

Fig. 7 — *X* terminal intrinsic resistors of the VCDO-CF and VCVF with respect to control voltage

V_C=0.4 V is used in all the following simulations. In Fig. 11, gains of an ideal BP filter and a non-ideal BP filter are given. The total harmonic distortion (THD) changes for the VM BP filter versus applied peak sinusoidal input signals are given in Fig. 12. It is seen from Fig. 12 that THD values are low enough. The input and output noise changes of the VM BP filter is given in Fig. 13.

Monte Carlo (MC) analysis for 100 runs is performed by changing 25% of C_f values of the BP filter. Simulation results for the center frequency of the BP filter related with MC analysis are given Fig. 14. About 700 kHz change in f_0 can be observed from Fig. 14.

Table 2 — f_0, *Q* and bandwidth change with control voltages

	V_C = 0.38 V	V_C = 0.4 V	V_C = 0.42 V	V_C = 0.44 V
f_0 (MHz)	2.85	2.75	2.66	2.57
Q	3.34	3.55	3.69	3.73
BW (kHz)	851	775	720	688

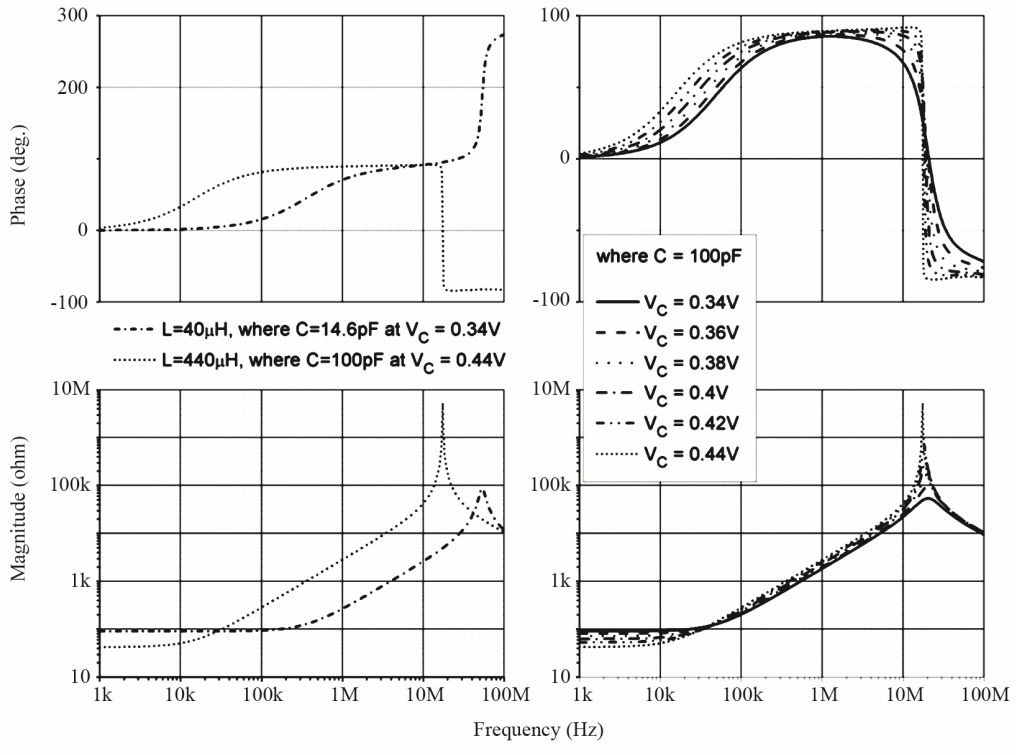

Fig. 8 — Phase and magnitude of the impedance of the proposed inductor simulator with V_C and *C* against frequency

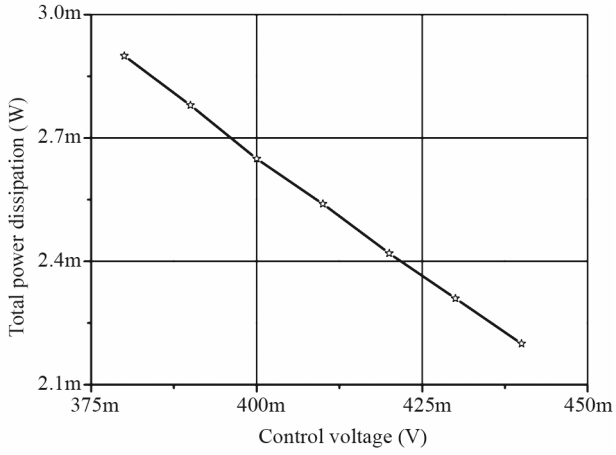

Fig. 9 — Total power dissipation changes vs control voltage

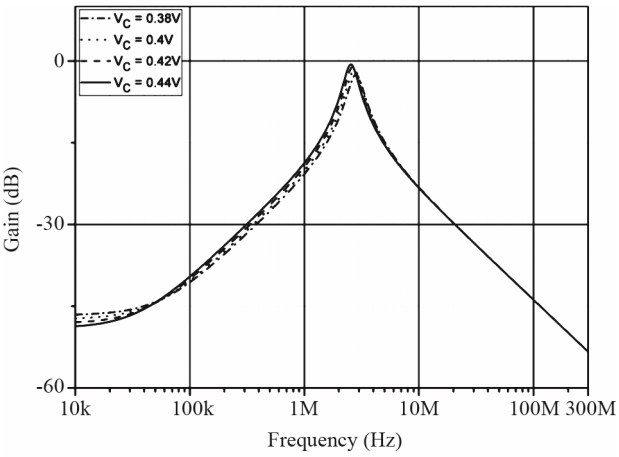

Fig. 10 — Gain change with control voltage vs frequency

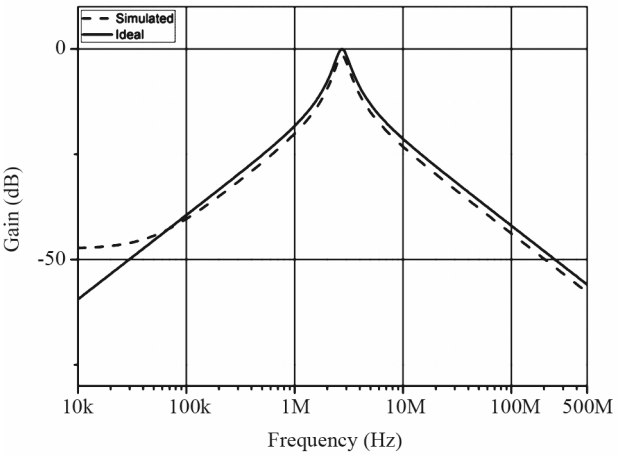

Fig. 11 — Ideal and simulated BP filter gains with respect to frequency

It is important to note that ideal and simulation results are close to each other but the difference between them arises from frequency dependent non-ideal gains and parasitic impedances of the VCDO-CF and VCVF.

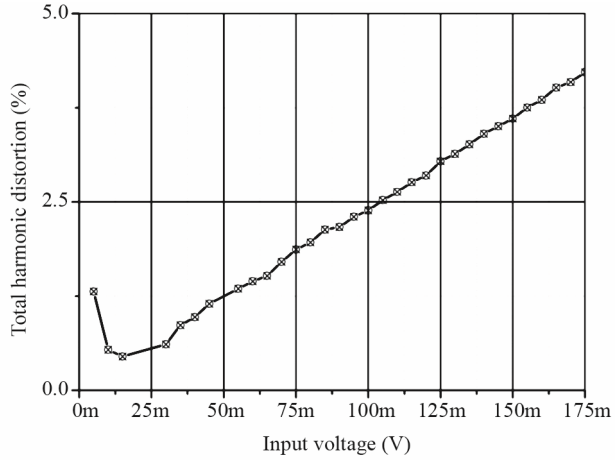

Fig. 12 — Total harmonic distortion variation against peak values of sinusoidal input signals

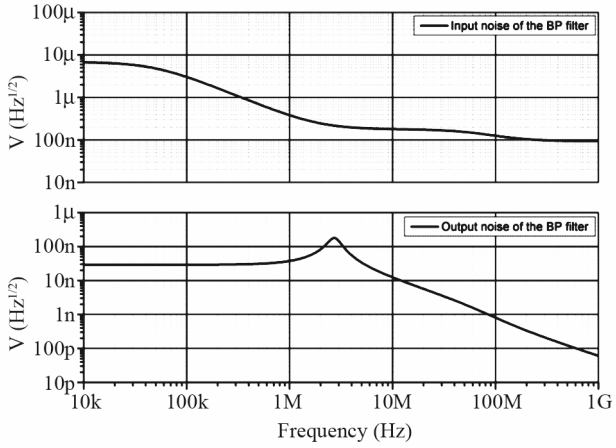

Fig. 13 — Input and output noise changes vs frequency

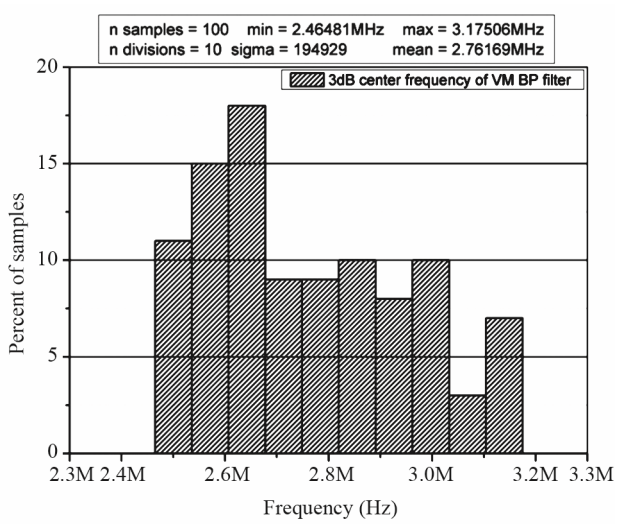

Fig. 14 — MC analysis of the VM BP filter

5 Conclusions

In this work, a new CMOS based VCDO-CF is proposed. Furthermore, a new electronically tunable grounded inductor simulator by using the VCDO-CF and a simple VCVF is proposed. The inductance value of the grounded inductor simulator can be adjusted externally by changing a control voltage. Also, it employs a grounded capacitor; thus, it is suitable for integrated circuit fabrication. Nonetheless, it needs a single active element matching constraint. The simulation results verify the claimed theory well.

References

1 Ferri G & Guerrini N C, *Low-voltage low-power CMOS current conveyors*, (Kluwer, London, U K), 2003.
2 Wilson B, *IEE P-Circ Syst Dev*, 137 (1990) 63.
3 Wilson B, *Int J Electron*, 73 (1992) 573.
4 Senani R & Gupta S S, *IEICE Electron Exp*, 1 (2004) 404.
5 Gupta S S & Senani R, *Analog Integr Circuits Signal Process*, 46 (2006) 111.
6 Keskin A U & Toker A, *Analog Integr Circuits Signal Process*, 41 (2004) 85.
7 Celma S, Sabadell J & Martinez P, *Electron Lett*, 31 (1995) 1817.
8 Alzaher H A & Ismail M, *Electron Lett*, 35 (1999) 2198.
9 Weng R M, Lai J R & Lee M H, *Int J Electron*, 87 (2000) 57.
10 Chang C M, *Int J Electron,* 88 (2001) 23.
11 Salama K, *Int J Electron Commun (AEU)*, 56 (2002) 289.
12 Gupta S S & Senani R, *Int J Electron*, 93 (2006) 769.
13 Tangsrirat W & Pukkalanun T, *Int J Electron Commun (AEU)*, 63 (2009) 416.
14 Senani R & Gupta S S, *Radioeng*, 20 (2011).
15 Tangsrirat W & Bunruang K, *Indian J Pure Appl Phys*, 50 (2012) 133.
16 Prasad D, Bhaskar D R & Srivastava M, *Indian J Pure Appl Phys*, 51 (2013) 864.
17 Tangsrirat W, Channumsin O & Pukkalanun T, *Indian J Pure Appl Phys*, 51 (2013) 516.
18 Tangsrirat W & Channumsin O, *Indian J Pure Appl Phys*, 49 (2011) 703.
19 Kumar P, Pal K & Gupta G K, *Indian J Pure Appl Phys*, 44 (2006) 398.
20 Sharma S, Pal K, Rajput S S, Mangotra L K & Jamuar S S, *Indian J Pure Appl Phys*, 47 (2009) 149.
21 Tangsrirat W & Channumsin O, *Indian J Pure Appl Phys*, 49 (2001) 137.
22 Toker A, Zeki A & Cicekoglu O, *Int J Electron*, 88 (2001) 517.
23 Alzaher H & Tasadduq N, *CMOS digitally programmable inductance*, International conference on microelectronics (ICM '06), Dhahran, 16-19 December 2006.
24 Sanchez-Lopez C, Castro-Hernandez A & Perez-Trejo A, *IEICE Electron Exp*, 5 (2008) 657.
25 Sanchez-Lopez C, Castro-Hernandez A & Perez-Trejo A, *Implementation of Chua's circuit with UGCs*, International conference on microelectronics (ICM 2008), Sharjah, 14-17 December 2008.
26 Sanchez-Lopez C, Trejo-Guerra R & Tlelo-Cuautle E, *Simulation of Chua's chaotic oscillator using unity-gain cells*, Proceedings of the 7th international caribbean conference on devices, circuits and systems, Cancun, 28-30 April 2008.
27 Alpaslan H & Yuce E, *Indian J Pure Appl Phys*, 51(2013) 651.
28 Alpaslan H & Yuce E, *Indian J Eng Mater Sci*, 20 (2013) 35.
29 Cicekoglu M O, *Int J Electron*, 85 (1998) 455.
30 Kuntman H, Gulsoy M & Cicekoglu O, *Microelectron J*, 31 (2000) 245.
31 Cam U, Kacar F, Cicekoglu O, Kuntman H & Kuntman A, *Int J Electron Commun (AEÜ)*, 57 (2003) 287.
32 Gift S J G, *Int J Electron*, 91 (2004) 477.
33 Yuce E, Minaei S & Cicekoglu O, *ETRI*, 27 (2005) 427-432.
34 Yuce E, *Int J Electron*, 94 (2007) 317.
35 Yuce E, *IEEE Trans Instrum Meas*, 57 (2008) 1079.
36 Yuce E, *Analog Integr Circuits Signal Process*, 59 (2009) 77.
37 Kacar F & Yesil A, *Microelectronics*, 41 (2010) 632.
38 Herencsar N, Koton J & Vrba K, *Elektrorrevue*, 1 (2010) 24.
39 Prasad D, Bhaskar D R & Singh A K, *Radioengineering*, 19 (2010) 194.
40 Kacar F & Kuntman H, *Radioengineering*, 20 (2011) 627.
41 Siripongdee S, Kwawsibsam A & Jaikla W, *Current controlled current-mode universal filter using CCCCTAs*, International conference on electrical machines and systems (ICEMS), Beijing, 20-23 August 2011.
42 Maundy B & Gift S J G, *Int J Electron*, 98 (2011) 555.
43 Metin B, *Radioeng*, 20 (2011) 614.
44 Myderrizi I, Minaei S & Yuce E, *Microelectronics*, 42 (2011) 1074.
45 Prasad D, Bhaskar D R & Pushkar K L, *Hindawi pub corp active and passive electronic components*, 101432, 2011.
46 Abuelma'atti M T, *Analog Integr Circuits Signal Process*, 71 (2012) 95.
47 Ibrahim M A, Minaei S & Yuce E, *Radioengineering*, 21 (2012) 3.
48 Metin B, *Int J Electron*, 99 (2012) 1027.
49 Arslan E, Metin B, Herenscar N & Koton J, *High performance wideband CMOS CCI with high voltage swing*, 11th International conference on development and application systems, Romania, 17-19 May. 2012.
50 Metin B, Herenscar N & Koton J, *DCCII based inductance simulator circuits with minimum number of element*, 23th Conference radioelektronika, Czech Republic, 16-17 April 2013.
51 Yuce E, Minaei S & Cicekoglu O, *IEEE Trans Circuits Syst I, Reg Papers*, 53 (2006) 2860.
52 Yuce E, *Int J Electron Commun (AEÜ)*, 61 (2007) 453.
53 Yuce E, *Analog Integr Circuits Signal Process*, 49 (2006) 161.
54 Yuce E, *Int J Electron*, 93 (2006) 679.
55 Bruun E, *Int J Electron*, 78 (1995) 911-923.
56 Sedra A S & Smith K C, *Microelectronic circuits,* 6th edition, (Oxford University Press, USA), 2011.
57 http://www.tannereda.com.