Dynamic OverSampling Ratio Sigma-Delta Modulation for the Control of Switching Power Converter

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Abstract— **The common algorithm used to control DC-AC switching power converters is Pulse Width Modulation. This work presents the use of Dynamic Oversamplig Ratio Sigma-Delta modulators for the control of the switches of DC-AC switching power converters. The proposed control algorithm presents the advantage of a reduction of conducted electromagnetic interferences with respect to Pulse Width Modulation. A prototype of a DC-AC switching power converter has been implemented.**

Keywords-DC-AC converters; sigma-delta modulation

I. INTRODUCTION

In recent years a great interest exists on alternative and clean energy sources, such as solar energy or energy coming from the wind. These energy sources require a DC-AC power conversion in order to be connected to the electric network (grid-connected) or to supply motors or electronic appliances (stand-alone connection). As a consequence, the demand of switch mode power supply (SMPS) and the research for the improvement of SMPS performances increased.

A wide variety of SMPS topologies has been invented [1-4] and Digital Pulse Width Modulation (DPWM) is a widely used technique for the control of SMPS. An increase in commutation frequency of the DPWM improves the precision and the performances of the SMPS. On the other hand it causes stress in the switching power devices, reduction in power efficiency, due to the commutation loss, and electromagnetic interferences (EMI) conducted and irradiated intrinsic in SMPS. The ΣΔ modulator is used in DC-DC switching power converters with the aim of reducing EMI, obtained by spreading the noise spectrum [5-6]. A new technique called dynamic oversampling ratio (DOSR), has been introduced to impose a minimum and maximum value on the switching frequency of the ΣΔ modulator output. DOSR-ΣΔ modulators have been used in DC-DC power converters [7]. This paper presents a control algorithm based on ΣΔ modulation and DOSR-ΣΔ for the control of switching DC-AC converters for stand-alone and grid-connected connections.

II. ΣΔ MODULATION

ΣΔ modulation is usually applied in analogue to digital and digital to analogue conversion, and in digital signal processing (DSP) to reduce the number of bits of a binary representation without reducing the signal information. The parameters characterizing ΣΔ performances are mainly three:

- the oversampling ratio (OSR), defined as the ratio between the clock frequency driving the modulator and the input signal Nyquist frequency;
- the order of modulator, corresponding to the number of integrator stages;
- the resolution of the quantizer.

As for DPWM, one bit ΣΔ modulators can be used to control power cells in switching mode power supply. Both modulators produce a binary signal with an average value related to the input signal amplitude. The output of DPWM is a square wave of fixed frequency and variable duty cycle, while the output of ΣΔ is a pseudo-periodic sequence of impulses and variable average value. The one bit quantizer adopted in the modulators produces a quantization noise added to the output signal. Since the quantization noise power of a single bit quantizer is very high, to avoid information loss in modulated signal, techniques like oversampling and/or noise shaping must be used. Oversampling used in both DPWM and ΣΔ modulators avoids the loss of information in the output signal [3], spreading the quantization noise over a wider band.

The difference between DPWM and ΣΔ is mainly related to noise shaping: DPWM spreads the noise uniformly across the band, while ΣΔ shapes the noise, reducing its level to lower frequencies and increasing it to higher frequencies like a high pass filter.

III. SMPS ARCHITECTURE

The proposed technique consists essentially in replacing the traditional DPWM controller of the SMPS with a ΣΔ modulator or a DOSR-ΣΔ modulator. The control can be applied to all the topologies used for SMPS, with grid-connected or stand-alone connection. In the stand-alone connection the SMPS must supply energy to the load. In the grid-connected application the SMPS must send energy to the energy network in the most efficient way; the SMPS must be synchronized to the network.

Without losing any generality, we will refer to the scheme of the SMPS in open loop connection reported in Figure 1, where the first stage is a step-down followed by a full bridge, controlled by a ΣΔ modulator. In the closed-loop connection the controller uses the information coming from the feedback that can be the current on the inductance (current-mode) or the output voltage (voltage-mode).

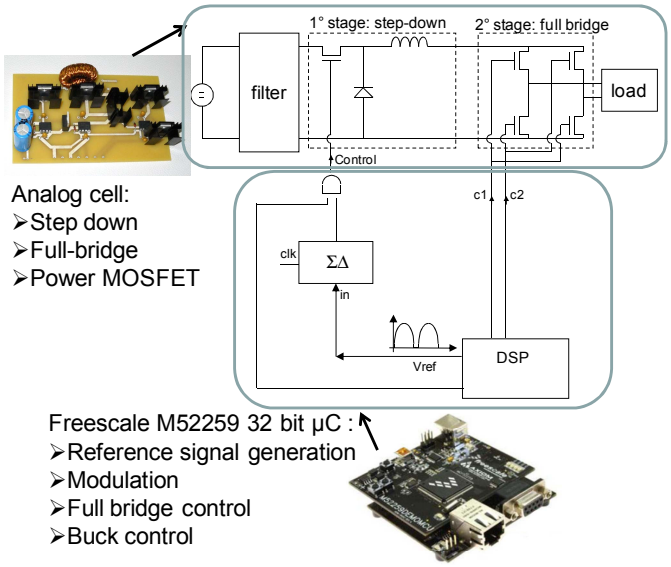

Figure 1. Hardware prototype of the DC-AC converter: analog cell (the first stage is a step-down followed by a full bridge) and microcontroller

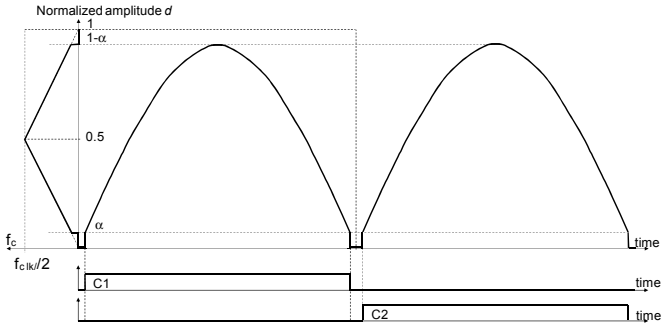

Figure 2. Control signals C1 and C2 of the H-bridge, desired output signal on the top side, and average switching frequency of the output of the ΣΔ modulator on the left side

The output of the ΣΔ modulator is a single bit that switches on or off the power MOSFET with an average value depending on the ΣΔ input signal. In the open loop connection the input signal is the amplitude of a sinusoid directly generated by a DSP or a microcontroller. Usually the full bridge switches are not driven on and off at the same time, in order to avoid the possibility of a short circuit generation. The desired shapes of the control signals, *c1* and *c2* indicated in Figure 1, are therefore non overlapping, as reported in Figure 2. Figure 2 shows the consequent distortion in the reference sinusoidal signal, that the DSP sends as input to the ΣΔ modulator.

The average switching frequency $\overline{f_{sw}}$ of the ΣΔ modulator output depends on the normalized amplitude *d* of the input signal and on the modulator clock frequency f_{clk} with the following relationship [7]:

$$\overline{f_{sw}} = \begin{cases} d \cdot f_{clk} & d < 0.5 \\ (1-d) \cdot f_{clk} & d \geq 0.5 \end{cases} \qquad (1)$$

When *d*=0.5, $\overline{f_{sw}}$ has its maximum value equal to $f_{clk}/2$. The function $\overline{f_{sw}}$ is symmetric with respect to *d*=0.5. The value of $\overline{f_{sw}}$, as a function of the desired output voltage amplitude, is shown on the left side of Figure 2. The following relationship reports the in-band SNR of an ideal ΣΔ modulator [3]:

$$SNR = 10\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) - 10\log\left(\frac{\pi^{2Q}}{2Q+1}\right) + 10(2Q+1)\log(OSR) \quad [dB] \qquad (2)$$

where σ_x^2 is the input signal power and σ_e^2 is the quantization noise power, that depend on the number of bits N of the quantizer and quantization step Δ in the following way:

$$10\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) \approx 10\log\left(\frac{\left(\frac{2^N\Delta}{2}\right)^2}{\frac{\Delta^2}{12}}\right) = 6.02N + 1.76 \qquad (3)$$

Q is the order of the ΣΔ modulator, OSR is the over sampling ratio defined as:

$$OSR = \frac{f_{clk}}{2f_b} \qquad (4)$$

where f_b is the Nyquist bandwidth of the signal and f_{clk} is the clock frequency of the modulator.

Combining equations (2), (3) and (4) for a second order ΣΔ modulator and an one bit quantizer, we obtain the following :

$$SNR = 6.02 - 11{,}14 + 50\log\frac{f_{clk}}{2f_b} \quad [dB] \qquad (5)$$

In our design the clock frequency f_{clk} has been chosen equal to 200 kHz, as a consequence, considering equation (1), the switching frequency f_{sw} of the output of the ΣΔ varies between 0 and 100 kHz, with an average value of about 45 kHz, as it has been be obtained by the numerical simulations. The SMPS with a ΣΔ modulator has been compared with a SMPS with a 20 kHz clock frequency DPWM.

The main problem concerning ΣΔ based controllers is that the average switching frequency can vary over a wide range like expressed in equation (1). When the duty cycle δ of the modulator is close to 0.5, the average switching frequency becomes too high, reducing power cell efficiency. Conversely, when the duty cycle δ of the modulator is close to 0 or to 1, the average switching frequency becomes too low, compromising system stability. To solve this problem, the OSR has been varied dynamically depending on the desired output signal value, such that the average switching frequency is confined in a specific range (20-30 kHz in our design) for a wide interval of the duty cycle, as shown with a continuous line in Figures 3 and 4.

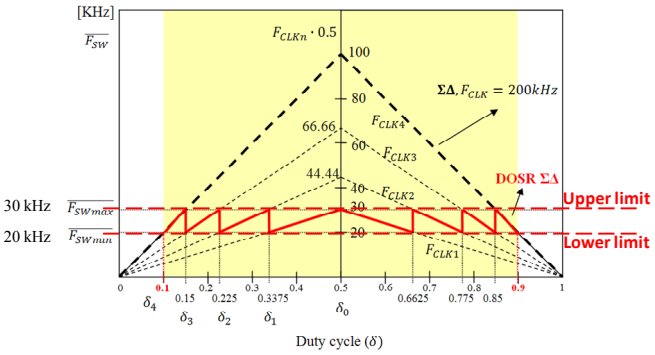

Figure 3. Average switching frequency of the DOSR-ΣΔ modulator

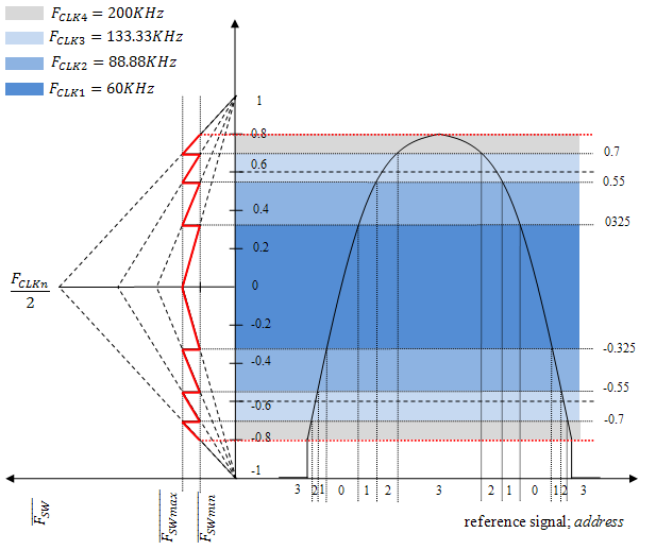

Figure 4. Desired output signal on the right side and consequent average switching frequency of the output of the DOSR-ΣΔ modulator on the left side

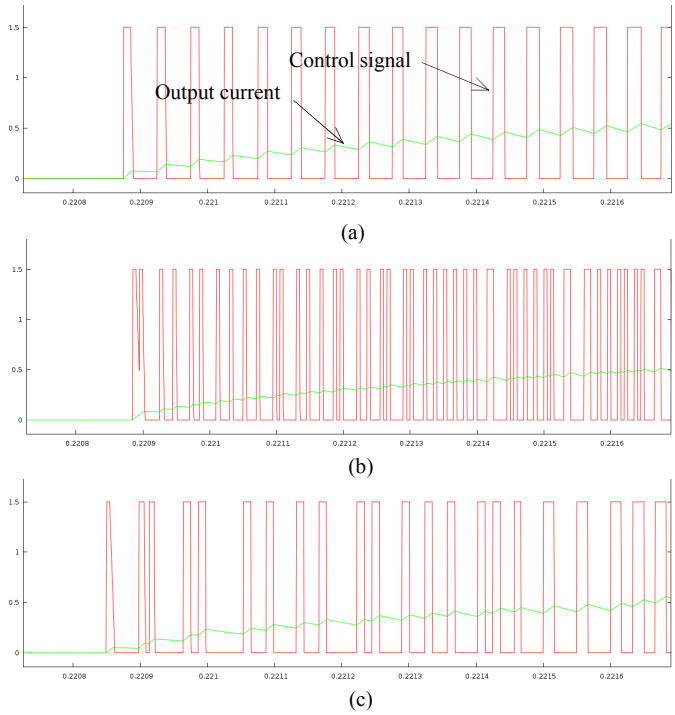

Figure 5. Output currents and control signals as a function of time obtained with the numerical simulations using DPWM (a), ΣΔ (b) and DOSR-ΣΔ (c).

	DPWM	ΣΔ	DOSR ΣΔ
Average commutations per period	336	994	384

Table 1. Average commutations per period.

IV. Numerical Simulations and Experimental Results

Three power converters with DOSR-ΣΔ, ΣΔ modulator and DPWM control in open loop and closed loop configurations, stand alone and grid connected have been simulated using the mixed signal simulation environment SystemC-WMS. The SystemC-WMS (Wave Mixed Signal) library has been recently presented [8], implementing a simple SystemC extension to allow mixed-signal modelling and simulation.

In order to explain how the three different control algorithms work, Figure 5 shows the output currents and the control signals as a function of the time, obtained with the numerical simulations using DPWM, ΣΔ and DOSR-ΣΔ, respectively. The PWM is a periodic signal, while the ΣΔ, and DOSR-ΣΔ are pseudoperiodic signals whose average commutation frequency depends on the amplitude of the desired signal, as indicated in Figures 3-4. Table 1 reports the average commutations per period.

The circuit has been implemented using analog components for the H-bridge, power MOSFET, diode and inductance, and the DPWM, ΣΔ and DOSR-ΣΔ controllers have been implemented using a 32 bit microcontroller in the commercial M52259 demoboard, as shown in Figure 1.

Figure 6 shows the output current with DOSR-ΣΔ control obtained from numerical simulations, on the top, and from experiments, in the bottom. In the Figure the crossover distortion of the ouput signal due to the non overlapping control signals is evident, but the noise ripple is reduced. Similar results have been obtained for a DPWM and ΣΔ control. The accuracy of the output signal with respect to the desired sinusoid is usually expressed in terms of root mean square error (rms_{error}) or total harmonic distortion (THD), defined in equations (6) and (7) respectively.

$$rms_{error}(\%) = \frac{rms\ (out\ -desired\ \_out)}{\max(desired\ \_out)} \quad (6)$$

$$THD = \frac{\sum\ power\ of\ the\ harmonics}{Power\ of\ the\ fundamental\ harmonic} = \frac{P_2 + P_3 ... + P_n}{P_1} \quad (7)$$

Another fundamental parameter of a power converter is the efficiency η, defined as follow:

$$\eta = P_{out} / P_{in} \quad (8)$$

Being the desired output voltage a sinusoid, the input current absorbed by the DC-AC converter is not constant during time, and the input power changes during time.

Therefore the minimum and maximum efficiency η_{min} and η_{max} have been calculated.

Table 2 reports the minimum and maximum efficiency, the rms_{error} and THD obtained from experimental measurements using DPWM, ΣΔ and DOSR-ΣΔ controls. The accuracy of the desired sinusoid expressed in terms of rms_{error} and THD is good for the three configurations. The accuracy obtained by the ΣΔ control is better, due to the higher clock frequency of the controller that causes an higher value of the average commutations per period, as reported in Figure 5. The efficiencies of ΣΔ and DOSR-ΣΔ power converters are comparable and better than the DPWM efficiency.

Finally, Figures 6-8 show the experimental output current waveforms and spectra for DPWM, ΣΔ and DOSR-ΣΔ modulation in open loop configuration. A peak in the DPWM spectrum at 20 kHz is evident. It is due to the fact that the DPWM output is a periodic signal with the same frequency of the clock of the modulator. Conversely, being the output of the ΣΔ and DOSR-ΣΔ modulators a pseudo-periodic signal, the noise spectrum is spread in a higher frequency band, as expected. The peak at the PWM frequency causes a not negligible electromagnetic interference in the case of DPWM, conversely the peach is reduced of one decade in the case of ΣΔ and DOSR-ΣΔ modulators.

V. CONCLUSIONS

The work presents the innovative use of Dynamic Oversampling ratio Sigma-Delta and Sigma-Delta modulators compared with DPWM modulators for the control of the switches of DC-AC switching power converters. The experimental results confirmed an improvement in power efficiency, in precision of the output waveform and a strong advantage in spreading the noise to higher frequency. Therefore, the proposed control algorithm presents advantages in the reduction of conducted electromagnetic interferences with respect to Digital Pulse Width Modulation. Dynamic Oversampling ratio Sigma-Delta obtains the same good results of the Sigma-Delta modulator with a reduced number of commutations of the power MOSFET, with a consequent improvement in efficiency and extension of the life of the component.

REFERENCES

[1] N Ned Mohan, Tore M. Undeland, William P. Robbins, "Power Electronics: Converters, Applications, and Design, 3rd Edition". Ed. Wiley, November 2002

[2] Bellar, M.D.; Wu, T.S.; Tchamdjou, A.; Mahdavi, J.; Ehsani, M.; , "A review of soft-switched DC-AC converters," Industry Applications, IEEE Transactions on , vol.34, no.4, pp.847-860, Jul/Aug 1998

[3] Aziz, P.M.; Sorensen, H.V.; vn der Spiegel, J.; , "An overview of sigma-delta converters," Signal Processing Magazine, IEEE , vol.13, no.1, pp.61-84, Jan 1996

[4] M. H. Rashid, Power Electronics Handbook. Academic Press, 2001.

[5] Dunlap, S.K.; Fiez, T.S.; , "A noise-shaped switching power supply using a delta-sigma modulator," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.51, no.6, pp. 1051- 1061, June 2004

[6] S.Orcioni, R.D'Aparo, M.Conti, "A switching mode power supply with digital pulse density modulation control", Proc. of ECCTD 2007, Sevilla, Spain, August 27-30, 2007.

[7] M.Conti, S.Orcioni, R. d'Aparo, "Dynamic OSR Sigma Delta Controller for Monolithic Switching Converters", Proc. of SPIE'09, 4–6 May 2009, Dresden, Germany.

[8] S. Orcioni, G. Biagetti, and M. Conti, "SystemC-WMS: Mixed signal simulation based on wave exchanges," in Applications of Specification and Design Languages for SoCs, ser. ChDL, A. Vachoux, Ed. Springer, 2006, ch. 10, pp. 171–185, selected papers from FDL 2005.

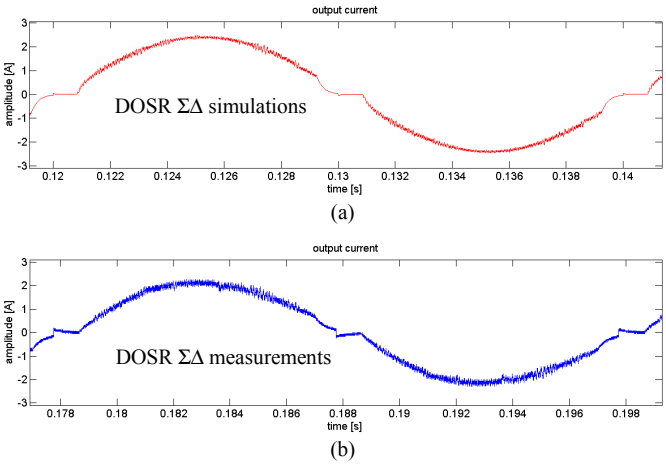

Figure 6. Numerical simulation (a) and experimental measurements (b) of the output current using DOSR-ΣΔ modulation in open loop configuration

Modulation	η_{min}	η_{max}	rms_{error}	THD
DPWM	0.827	0.920	4.97%	1.78%
ΣΔ	0.831	0.925	4.42%	1.29%
DOSR-ΣΔ	0.844	0.929	4.55%	1.61%

Table 2. Efficiency, rms_{error} and THD obtained from experiments.

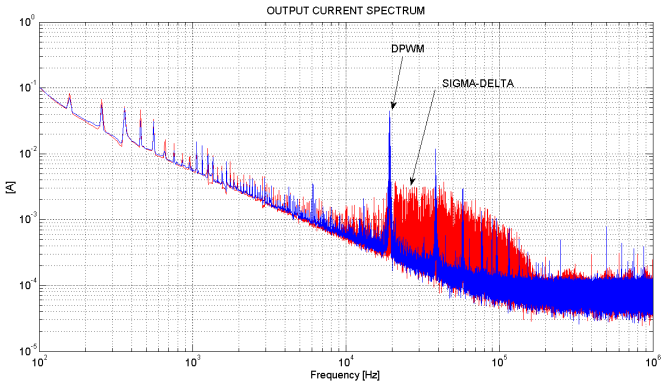

Figure 7. Output current spectrum for DPWM and ΣΔ modulation in open loop configuration. Experimental results.

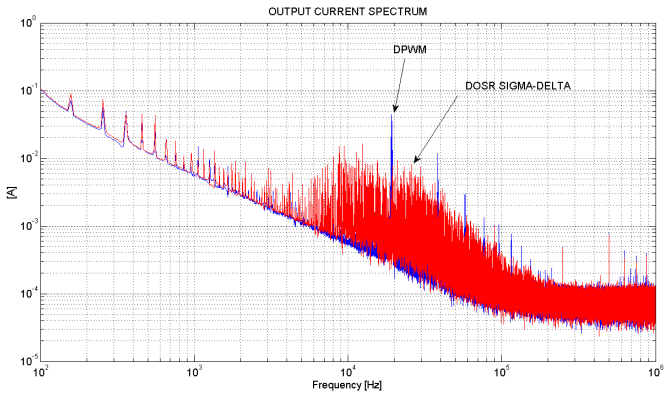

Figure 8. Output current spectrum for DPWM and DOSR-ΣΔ modulation in open loop configuration. Experimental results