A SINGLE CHIP IF FM/AM DECODER USING A SIGMA-DELTA ANALOG-DIGITAL CONVERTER

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Abstract: *This paper describes a digital radio demodulator for broadcast AM/FM receiver applications. The IC is comprised of a Sigma-Delta A/D converter and a digital AM/FM demodulator. The Sigma-Delta modulator converts the standard 10.7MHz IF signal, allowing the use of digital channel-select filtering, providing improved performance over analog filtering. Subsequent demodulation and signal processing are performed digitally, allowing flexibility in the algorithms employed and greater integration with other digital circuitry in the system. There is also a software element to the system, as the stereo decoder and RDS decoding functions are implemented by DSP off-chip rather than on dedicated hardware. Behavioural-level simulations of the system are presented, which show it meets the requirements of 80 dB SNR for stereo FM input signals over a 150 kHz bandwidth.*

1.0 Introduction

Traditionally, radio systems have been analog-component based and any digitizing of the signal occurs at the signal output, at audio frequencies. Lately, there has been interest in the two-chip approach to radio reception and demodulation [1, 2]. In these systems the first chip, the tuner chip, receives and mixes the received signal to an intermediate frequency (IF), commonly 10.7 MHz. The second chip then digitizes the IF signal, allowing digital channel-select filtering and demodulation, which means that greater adjacent channel rejection is possible. Sophisticated demodulation algorithms can be implemented more efficiently than would be possible in the analog domain and the radio is more easily integrated with other digital entertainment and communications systems [2]. The design presented here includes an IF frequency Sigma-Delta ($\Sigma\Delta$) modulator based analog-digital converter and a digital FM/AM demodulator (Figure 1). Section 4 will detail how to split the stero FM signal and to extract left, right and RDS signals.

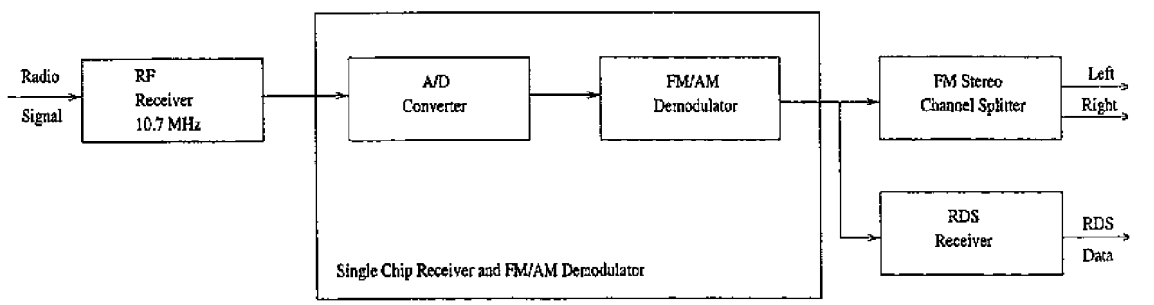

FIGURE 1. Digital Radio Receiver

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2.0 IF Analog-to-Digital Convertor

A block diagram of the IF sampling A/D converter [4] is shown in Figure 2 below.

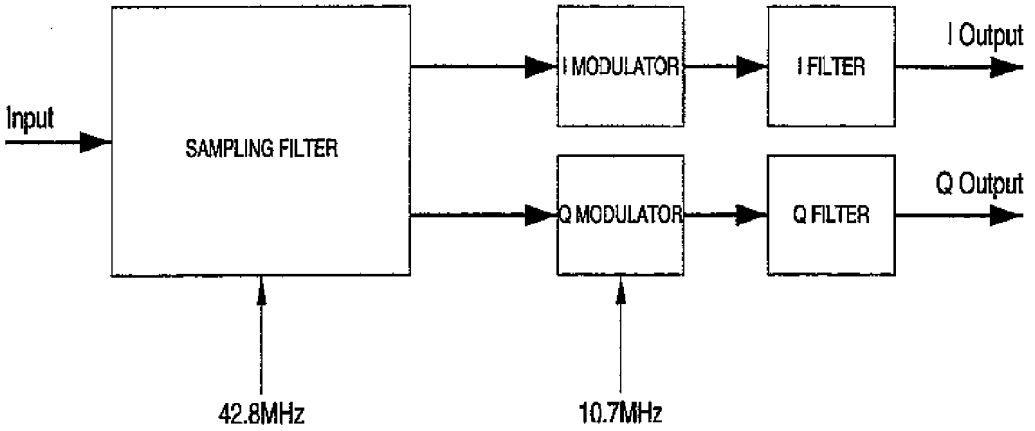

FIGURE 2. IF Sampling Sigma-Delta A/D Converter

The 10.7MHz input is sampled at 42.8MHz by the Sampling Filter block in Figure 2. The samples are modulated by 1, 0, -1, 0 and 0, 1, 0, -1 sequences to generate In-phase (I) and Quadrature (Q) components and averaged to reduce the sample rate to 10.7MHz and remove aliases at multiples of this frequency. The A/D conversion is carried out by the I and Q modulators and the outputs digitally filtered by the I and Q filters in Figure 2. These are modified $Sinc^3$ filters which restore the quadrature relationship between the channels. This architecture is more efficient than conventional bandpass $\Sigma\Delta$ modulators, because the modulator clock rate is independent of the IF frequency and lowpass modulators are about half as complex as bandpass modulators of the same noise-shaping order.

The diagram in Figure 2 shows a pair of modulators, one each for the I and Q paths; however, for good matching between the two paths, a single modulator is used, clocked at 21.4MHz. The modulator itself is a second-order 17-level model which provides the necessary 80dB resolution and 150kHz bandwidth. A version of dynamic element matching (DEM) (e.g. see [6]) is used to reduce the effects of DAC nonlinearity on modulator performance.

3.0 FM/AM Demodulator

Most digital FM demodulation techniques use either the Foster-Seeley Method or digital phase-lock loops. However there are difficulties with these techniques, requiring either extensive numerical processing or large look-up tables. Recently a different approach using a quadri-correlator has been suggested by Song and Park [3]. This approach does not require a digital PLL, and due to the good AM suppression ability of this procedure, no additional amplitude control circuitry is needed. The FM message signal can be extracted from the in-phase and quadrature components using a simple numerical approach that does not suffer from numerical errors other than discrete-time differentiation errors.

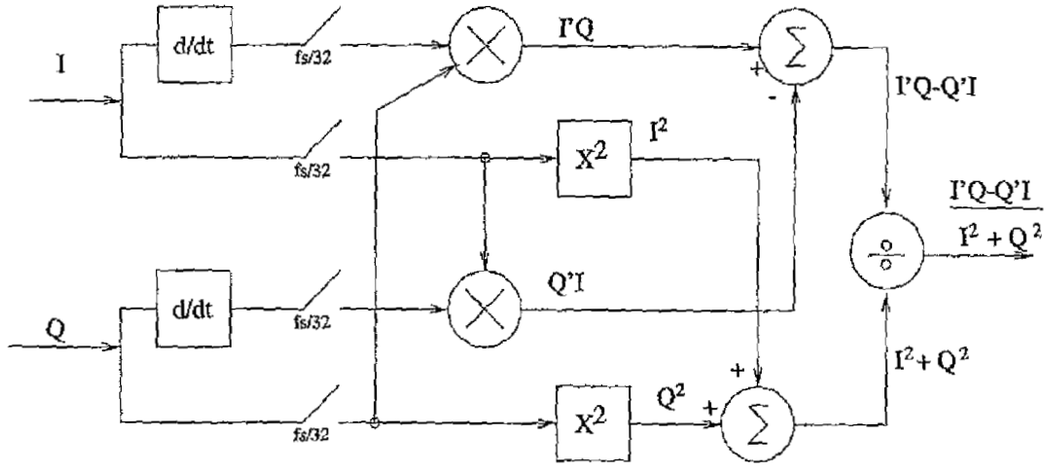

FIGURE 3. A structural overview of an FM Demodulator as suggested by Park et al.

The structure of the demodulator is shown in Figure 3. Given the I and Q components of the signal, differentiated signals are produced. Both the differentiated signals and the original signals are then decimated. The decimated signals are multiplied with each other and themselves to produce IdQ, QdI, I^2 and Q^2 terms. This requires the use of wide multipliers (24 bit) which are expensive in terms of gates. These products are combined and then used in a divider to produce the decoded FM output. As the numerator of the divider is much smaller than the denominator, steps need to be taken to ensure 16 significant bits of resolution. It is possible to either scale up the numerator or scale down the denominator. Scaling up the numerator has the problem of increasing the size of the divider, where scaling down reduces the information content of the denominator, resulting in increased noise. In our application, a 39 bit divider was eventually chosen. One advantage of this approach is that the denominator of the divider, if square-rooted, is the decoded output of an AM modulated signal.

Given the basic structure of the decoder it is possible to incorporate the $sinc^3$ filter with the differentiator. $Sinc^3$ filters can be split across the decimating switch, with integrators at the high frequency end, and differentiators on the low frequency side. To obtain a differentiated signal for either the I or Q channels, , all that is needed is to tap of a new path before the last integrator on the high frequency side. This signal when passed through the triple differentiation of the $sinc^3$ filter produces an effective differentiator. In our system a second-order differentiator was implemented.

Finally the low frequency section of the decoder, the differentiators for the $sinc^3$, the multipliers and adders, were all multiplexed to produce a more compact implementation. The final implementation requires approximately 24,000 gates.

4.0 Stereo and RDS Decoding

The demodulated FM signal has left and right (L, R) signals, encoded as L+R and L-R components. The L-R is modulated to a 38kHz subcarrier and RDS (Radio Data System) information may also be present on a 57kHz subcarrier. A DPLL is used to generate the 19kHz and 38kHz tone signals, that allows the L+R and L-R to be added coherently; as well as the 57kHz tone for the RDS signal. In the present implementation, decoding of these components will be performed in software running on a DSP core. This allows the possibility of other features being added, such as multi-path fading cancellation.

5.0 Results

The behavioural-level performance of the system has matched design specifications. System SNR exceeds 80dB for a 150 kHz bandwidth with no noticeable harmonic distortion. The output from a sample FM modulated stereo signal can be seen in the figure below. In practice, the quality of the input signal will be the determining factor in the quality of the output signal. The FM/AM decoder block has been sized at 24k gates in a 0.25 micron process, roughly estimated at 0.75 mm^2. The analog section is estimated to be < 1 mm^2 in area.

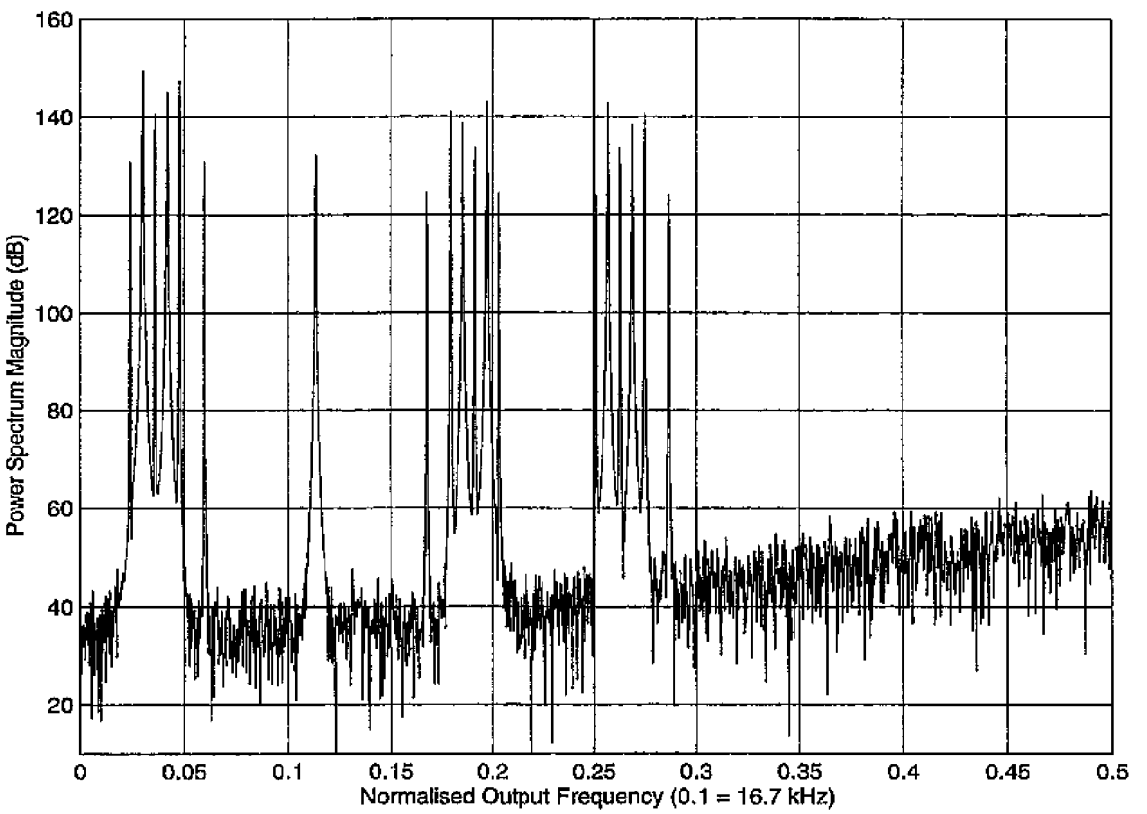

FIGURE 4. Output of FM/AM demodulator block, pilot tone of -20dB at 19kHz

6.0 Conclusions

The design presented in this paper has shown that it is possible to provide high performance low harmonic distortion AM and FM demodulation using a single chip. This has many possible applications in current systems and also in future systems, such as digital FM, where the input signal is required to interface directly with DSP components. This design also shows that it is possible to provide high performance cost effective channel select filtering using bandpass sigma-delta modulator based converters .

7.0 References

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