Hierarchical DFT with Combinational Scan Compression, Partition Chain and RPCT

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Abstract—**Modular and hierarchical based test architecture are the two of the most common testing techniques used in complex SoC designs. However, modular test architectures uses an expensive (in terms of silicon area) test wrapper around each block. On the other hand hierarchical test architecture requires additional effort at block level to isolate each block from surrounding blocks and a TAM to perform scan compression. In this paper, we analyze the limitations of the modular test architecture. Based on the analysis, we propose a test plan for hierarchical test architecture by integrating partition chain, combinational scan compression and (RPCT) reduced pin count test. Experimental results show that approximately 50% of DFT area can be reduced using the partition chain as compared to standard test wrapper. It also demonstrates the feasibility of the proposed test plan using a commercial ATPG tool.**

I. INTRODUCTION

When testing a multicore System on Chip (SoC) design, the testing principles and DFT strategies involved in such a complex design depends on the information of system level architecture. One of the important challenges in complex SoC testing has been accurate description and realization of system level architecture design of chip. Two most commonly observed Design for Test (DFT) strategies are modular and hierarchical methodologies [1] [2] [3] [5] and [16]. Both the ideas were manifested by understanding the plug-n-play nature of the Intellectual Property (IP) cores, which highlights the heterogeneity in the level of integration and also functional role of each IP block play in a SoC design. As time-to-market is the dominant factor in the core-based design, the integration of reusable cores becomes an obligatory process in the SoC design. In some case the system level integrators may not have sufficient information about the cores as it will be provided either as a hard IP or as an encrypted core. In such scenario, the system integrators have to rely on the test sets provided along with cores. In addition, cores are at times deeply embedded in hierarchical SoC design. These issues necessitate the need for effective core isolation and efficient test access mechanisms (TAMs) to transport test patterns from the input and to the output pins of the chip. One possible solution will be the modular testing [1]. The divide and conquer approach of the modular testing allows the system integrator to distribute the DFT implementation across cores with appropriate core isolation and TAMs there by reducing the overall time required to integrate the DFT implementation. It also increases the test efficiency in terms of test generation time and test data volume. Modular testing uses IEEE P1500 wrapper around each cores for isolating core during the test mode. The main purpose of 1500 is to standardize the interconnection between the core

under test and the system top level in a way to facilitate the reusability of the core. The wrappers of all cores are then connected to SoC pins through the TAMs. Scan compression is a process wherein smaller numbers of long scan chains are converted in to a large number of smaller scan chains. It is done using the decompressor at the input side and a compactor at the output side. The decompressor expands the compressed test stimulus in to the scan chains, whereas compactor converts a long output response into short signatures. Fig.1 shows modular scan architecture with wrapper and scan compression.
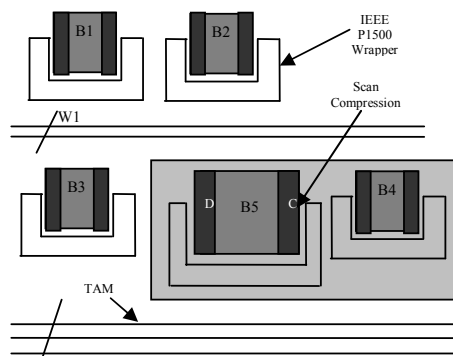

Figure 1.   Modular SoC Testing

With SoC, designs are becoming more hierarchically organized, there have been some attempts to develop hierarchical DFT [4] [5] [16]. An interesting feature of the hierarchical DFT is that it efficiently makes use of the natural partition of the system architecture and follows the same system level integration flow as that of a modular test procedure.
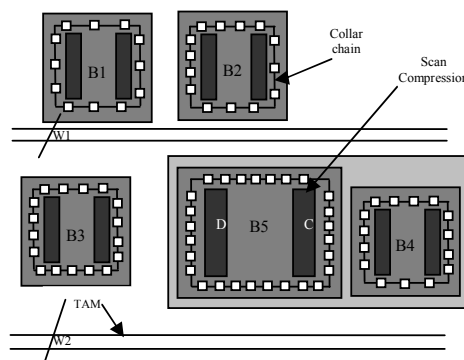

Figure 2.   Hierarchical DFT for SoC Design

It differs from the modular approach in the way the blocks are isolated from each other and this requires extra block level work. In hierarchical DFT, each core is isolated using a collar chain. Fig.2 shows the Hierarchical DFT for SoC design. A collar chain is formed using the scan flops present along the boundary of the core. The method proposed in [5] first locates scan flops present in the boundary core that can be used for isolation purposes, and then stitches them into collar chains. Hence there is no additional area cost overhead due to core isolation. Collar chains can be used to test the user defined logics (UDL) present between the cores. The contributions of this paper are of two fold: 1) we estimate the test cost for three different test architectures and highlight the limitations of the modular test architectures; 2) we propose a test plan wherein we incorporate the combinational compression [12] [23], collar chain [5] and reduced pin count test [20] into hierarchical test architecture.

In this paper, we refer partition chain proposed in [5] as the collar chain. To illustrate this, we consider SoC platform based on ISCAS 89 benchmark circuits to perform the hierarchical scan test. We first discuss limitations of the modular scan architecture, and then we discuss the related work in hierarchical scan testing. Next, we describe the proposed test plan for hierarchical test architecture. Finally, we provide experimental results, and conclusion and future work.

II. LIMITATIONS OF MODULAR TEST ARCHITECTURE

The test wrapper and TAM are the two important features of modular scan test. With the increase system complexity, scan compression has also become part of the modular approach. Design of test wrapper and TAMs are mostly inter dependent on each other. This is evident from equation (1), where parallel scan chains (*pchains*), and the primary I/Os (PI & PO) constitute the TAMs. When test wrapper is used on block, it allows the user to perform scan compression for each block and generate the test patterns concurrently [3], but this comes at the cost of silicon area; there will be a significant increase in the test wrapper area overhead for blocks with larger numbers of ports on the boundary. Approximate test collar area utilized by the IEEE P1500 wrapper (expressed in terms NAND gates) was given in [6], is shown below.

$$Wrapper\ Area = 135 + (pchains*5) + ((\Sigma PI+PO)*14) \qquad (1)$$

Equation (1) shows that there will be an increase in test area when the number of I/O's are large in number. Hence modular scan architecture with test wrapper is very expensive in terms of silicon area overhead. To substantiate this statement, the work presented in [7] clearly proves that IEEE P1500 wrapper is not suitable for their designs which requires high bandwidth and has large number of I/Os. Similarly the work presented in [8] also examines test strategies for unwrapped logic blocks and wrapped cores in the SoC design without compromising the fault coverage. The idea presented in [9] tries to reduce the area overhead of test collar by using the shared and dedicated isolation ring. However it is performed only on the IEEE P1500 standard based wrapper and requires a proprietary DFT tool to perform this optimization. Another critical factor in the scan test is the scan compression. Generally scan compression

technique are more modular in nature [19] and are utilized in the system architecture either in a distributed style or by centralized approach. Centralized compression (*Daisy-chain Test Architecture*) can cause more routing congestion and is less flexible as far as test scheduling is concerned (since all the blocks in a test architecture should be tested at the same time). Moreover it does not facilitate easy plug and play approach in case of redundant routing in the design. Distributed compression (*Star Test Architecture*) helps to reduce the routing congestion thereby reducing the huge localized signal fan-out but this is achieved at the cost of increased circuitry in the test architecture. While the limitations are: increased test pattern count, vulnerability to X's propagation, and will not achieve the same compression as centralized compression scheme. In addition, it is limited by the number of pins available on a chip. The *Hybrid Test Architecture* is a combination of the distributed and centralized test architecture. It allows reusability of blocks and does not add DFT logic to the test architecture, but requires long scan paths. To analyze the feasibility of these modular test architectures in terms DFT area overhead, we estimate the test cost by varying the test structures (number of block partitions) in a modular test architecture of about 11 million gates using the cost model presented in [10]. Table.1 shows some of the test cost functions used in the test cost calculation.

Table.1 Test Cost Function

Cost Functions	Source Literature / Assumption	Value / Equation
Die area	TSMC	160,000 gates/ mm^2
Defect Density	Ref.10	0.002/ mm^2
Gate Count	ITRS	11 Million Gates
Yield	Assumption	0.95
Wafer Cost	Assumption	€750
Die Cost	Ref.10	Wafer cost / (Dies/wafer * Yield)
# of I/Os	Assumption	25
# of flops for 1M gates	EE times	0.05 M flops
Area of the wire	Ref.11	$W_n*(\Sigma\ \omega(n) * \ell(n))$
Compression Ratio	Assumption	300x – 60x
Compression Logic Area	Mentor EDT Manual	25 gates per internal scan chain
Wrapper Area	Ref.6	135+(pchains*5)+((ΣPI+PO)*14)

Equation (2) includes the major factors which affect the DFT area. The test costs curve is plotted with area as the critical parameter for the three test architectures.

$$DFT\ Area = A_{scan\ cell} + A_{Compression\ Logic} + A_{Wrapper} + A_{Scan\ wire} \qquad (2)$$
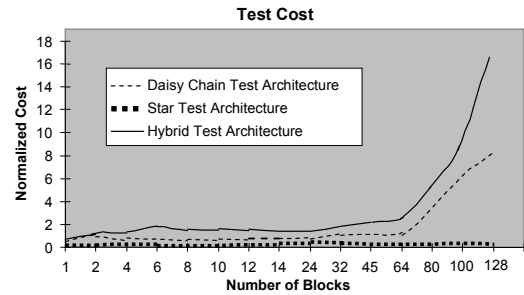

Figure 3. DFT Cost Plot for Different Test Architectures

It is clear from fig.3 that the advantages of daisy and hybrid approaches are negated when used in modular test architecture; due to the drastic increase in area overhead cost caused by high routing congestions and increased DFT logic. Sometimes area overhead cost can offset the other benefits of scan compression such as test time reduction, lesser pattern count etc. Star architecture is economical in terms of overall DFT area but this comes at the cost of lesser compression and increased compression logic area. This, in turn, increases the need for two or multi-level scan compression. It also raises the question whether is it possible to design a test architecture that still works even when redundant blocks or routing system are removed. The answer to this question would be a hierarchical approach, as it not only satisfies the modular requirements; it is also economical in terms of area overhead cost and is flexible enough to accommodate a more advanced DFT strategy developed by the user.

III. RELATED WORK

In recent years, there has been more attention to hierarchical DFT methods for complex designs, due to its simplistic and cost effective approach. Most of the papers found in the literature, have addressed the hierarchical SoC designs using modular approach. In all the cases [1] [14] and [15], the advocated hierarchical test architecture is based on IEEE P1500 wrapper to provide block isolation. Multi level TAMs were used to address the issues related to test time and area overhead in hierarchical SoC design. In [4] [5] [8] and [13], block isolation techniques were explored without using the standardized test wrapper in hierarchical test architectures. The technique proposed in [5] makes use of the registers present near the I/O's of the design, by converting it into an isolating ring around the block. This isolation incurs no extra area overhead. In [8] and [13] techniques have been proposed to decrease the collar cells, thereby reducing the timing and area, however both the techniques incurs extra logic in the functional path.

In [4], a testing procedure was proposed for unwrapped blocks in a hierarchical scan testing. It is performed by analyzing the interaction between the partitions based on the fact that additional test modes were introduced to increase the coverage. The work presented in [5] was enhanced in [16] by including the ac test, sequential compression technique, and test scheduling techniques. However this done by adding extra logic in the functional path. In addition the sequential compression technique used in [16] increases the area overhead and the complexity of the test architecture. Similar work presented in [17], proposes an algorithm for the isolation technique, in which it utilizes the existing registers, around the I/Os of the block, to create the test collar. However, in this case, it does not have the requirement that the I/O ports need to be registered.

In [19], TAMs were utilized in a combinational scan compression to reduce the test data volume and test time. Unification of TAMs and scan compression was experimented in [19] mainly to overcome the limitations of the existing combination compression techniques in a hierarchical test architecture. However it was not clear how test collar

optimization can be performed in conjunction with scan compression. In this paper, we take in account all the issues pertaining to hierarchical test architectures and propose an SoC test plan that integrates the block isolation, combinational compression and reduced pin count boundary scan technique.

IV. HIERARCHICAL DFT METHODOLOGY

The architecture for the proposed test plan is shown in fig.4. We choose the block isolation technique proposed in [5] as it utilizes the flops in the design to construct the test collar chain therefore it is economic in terms of area overhead. For a complex hierarchy SoC, scan compression needs to be applied to each partitioned block, as a global approach may not be feasible in such a scenario. Scan compression can be achieved either by sequential or combinational approaches. It is widely believed that sequential compression can achieve higher compression than the combinational approach since it uses better encoding techniques. However the difference is getting narrow because of the recent advances reported in the combinational approach [18].
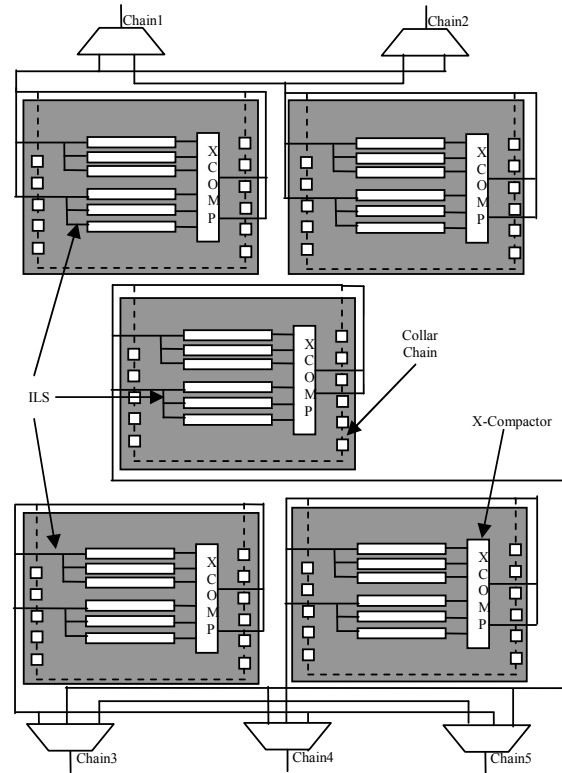

Figure 4. Hierachical Test Architecture with Test Collar Chain and Combinational Scan Compression

With ever increasing test complexity the possibility of broadcasting the test patterns to identical blocks was explored in [22]. Under such a scenario, existing broadcasting methods such as Illinois Scan Architecture (ILS) [21] are in a better position to exploit this opportunity. In this paper, we choose the combinational approach, i.e., ILS as decompressor, as it can

be implemented using a commercial Automatic Test Pattern Generation (ATPG) tool. For the compactor side, an X-compactor approach in [12] [23] was chosen because it is independent of ATPG process and also can be verified using any logic simulator. It allows the user to design the compactor to detect the faults in the presence of x's and diagnosis it. Continuous advancements in test strategy have led the DFT engineers to contemplate the need for multi level compaction techniques [12]. Other important factor that affects the testing cost is the tester equipment itself [10]. We choose the RPCT techniques proposed in [20] to reduce the testing cost, as it eases the requirements of the tester pins.

V. PROPOSED HIERACHICAL TEST PLAN

Hierarchical system architectures have several levels of the test hierarchy where each level refers to the depth in the hierarchy tree. These types of architectures can be broadly classified into two types: interactive models and non interactive models. Classification is done based on the nature of the blocks (hard IP or soft IP) involved in the design flow [1]. Interactive models use soft IP blocks and hence there will be considerable communication between each block, while non interactive models use hard IP blocks with limited communication between the blocks. Several test strategies were proposed in the past, targeting mainly the non interactive models using a modular approach, but as mentioned before; modular techniques have limitations in terms of area overhead.
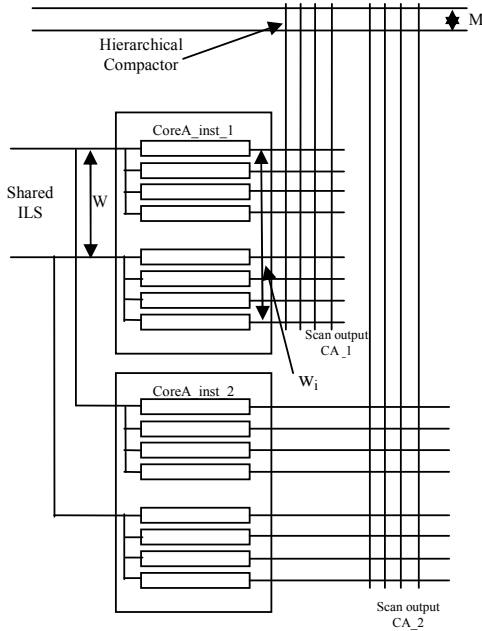

Figure 5. Hierarchical compression for idential cores in the design

In contrast the hierarchical approach is more viable for today's complex SoC designs; as it exploits the inherent properties of the system architecture compared to the modular

approach. It utilizes lesser DFT area and has a faster production time. It also consumes less power on tester, as blocks can be tested individually or in small groups. Limitation of this approach is that it requires an upfront test plan for the test architecture. The proposed test plan for hierarchical test architecture was based on the interactive model. Fig.5 shows the schematic representation of the shared ILS with hierarchical compactors. Memories in the SoC design were not considered, with assumption that it can be tested using the Memory BIST. We define the test plan problem P_{CTSR} (CTSR stands for test **C**ollar chain, **T**AM, **S**can compression, and **R**educed pin count test) by taking the design constraints into account. Some of the critical design constraints are: (a) number of partitions in the design, (b) number of flops in each partition, (c) number of top level I/O's that can be used for scan, (d) presence of glue logic or combinational circuits between the blocks. P_{CTSR} − Consider a SoC design with N blocks. If 'n' is the number of primary inputs, 'm' is the number of primary outputs of each block, 'W' is the TAM width, and 'M' is the numbers of top level scan I/O pins used for testing. Then the design of test architecture involves the following goals: (i) determine the number of test collar chains (w_c) and number of internal scan chains (w_i) for each block such that test time is minimized, (ii) determine the blocks that needs scan compression as well as their compression ratio i.e., the value of TAM (W) at the decompressor inputs and the value of w_i at the decompressor output. The value of W and w_i for each block should be selected such that overall test data volume and the corresponding test time are minimized. (iii) Decide the RPCT based on value of M and the value of W.
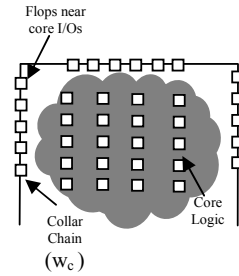

Figure 6. Partition chain around the block

The number of test collar chains needed depends on the number of flops required for the core isolation and the number of chip level pins available for scan. Fig.6 shows the partition chain creation around the block. First, flops around the I/O's that can be used for collar chain were identified, and the remaining flops are allocated to internal chains. Second, the number of internal chains is driven by the channel to chain ratio and the compression goals that are being aimed. In all scenarios, collar and internal chains need to be balanced in length [5]. Third, RPCT can be used when the length of the longest internal or collar chain is shorter than the number of I/O pins on the chip, as a result there will be increased scan chain loading. A core with RPCT and compression logic would have a test strategy that enables the isolation of the core level I/O as well as significantly reducing the scan I/O at the core level and thus reducing pin overhead. Though RPCT does not

directly affect test time and test data volume, it can be selected in conjunction with scan compression so that test time and test data volume can be minimized [20]. Fig.7 shows the steps involved in the test plan of hierarchical test architecture.

Test Plan for Hierarchical DFT Methodology

1) Decide the number of collar chains required for each block based on number of I/O's of that block.

2) Decide on the internal scan chain depth common for all the blocks.

3) Decide on the scan compression ratio for each block.

4) Insert scan for all sub blocks with number of scan chain decided in step3 and with flops in each chain as per step2.

5) Design an ILS decompressor at the scan-in side and hook to the sub block scan ins. If identical blocks are present, then share ILS decompressior.

6) Design X-Compactor and hook from each sub block scan- outs. If identical blocks are present then use hierarchical compactor.

7) If glue logic is present in top-level either treat it as another sub block and repeat steps 1 to 6 or use the partition collar chains to test it.

8) Hook up decompressor and compactor of all the blocks to the top level ports.

Figure 7. Proposed Test Plan for Hierachical Test Architecture

VI. EXPERIMENTAL SETUP

We constructed two prototype SoC designs based on ISCAS 89 benchmark circuits as shown in fig.8. Benchmark circuits were synthesized at TSMC 180nm technology. We follow the test procedure given in [5] for collar chain insertion.

Figure 8. Prototype SoC Design 1   Prototype SoC Design 2

The collar chain acts as isolation ring around the core with controllability and observability of faults in the core without any interference from logic outside of the core. When running the ATPG for the internal scan chains at the core level, functional inputs are ignored and functional outputs are masked. This emulates an embedded core in a chip. Collar chains can also be used to test the interconnect wires and the glue logics present between the cores. For the prototype SoC design 1 shown in fig.8, the glue logic was tested using the output collar chain of the core s38417 and the input collar chain of the core s38584. The scan cell of output collar chain

(core s38417) was used to launch data while the scan cell of the input collar chain (core s38584) was used to capture data. In order utilize the ILS technique as proposed in [21]; the scan inserted netlists were modified to incorporate the ILS. We utilize the technique proposed in [22], where in shared ILS can be used to apply identical test stimuli to all identical cores at the same time. By using this technique, both test application time and test generation efforts can be minimized to large extent. A hierarchical X-compactor proposed in [12] was used to compact the scan outputs of the shared ILS. For the remaining cores, single level X-Compact was used [23]. The compactor was modeled as a black box during the ATPG process, as the commercial DFT tool used could not recognize the compactor used. Compactor circuit was later verified using the logic simulator. RPCT was used at the top level for the two designs. Scan insertion, ATPG, RPCT were performed using the commercial DFT tools.

VII. RESULT AND DISCUSSION

In this section, we present the experimental results and analyze the cost trade off offered by the proposed test plan. The test coverage was above 90% for all the cores in the two designs. In this analysis we mainly focus on other two important factors: area and test cycles. We compare the expression for area and test cycle results of collar chain with IEEE P1500 wrapper.
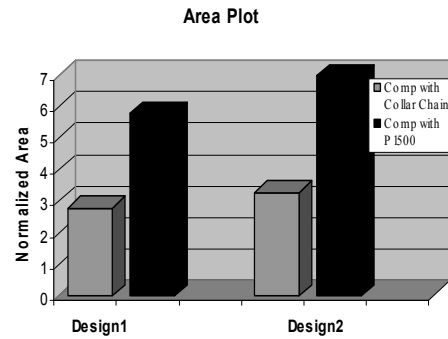

Figure 9. Area utilised by DFT logic in the SoC designs

Fig.9 shows the area utilized DFT logic in both of the two designs. There was approximately 50% area reduction when test collar chain is used, since it does not add much DFT logic as it uses the flops present in the design. Another advantage of collar chain it reduces the number of internal scan flops required for scan compression. Fig.10 shows the test cycles required for two designs. Test cycle for design with collar chain increases significantly due to increase in pattern count. Test pattern count gets increased mainly due to the separate test runs required for collar chains to mop up the coverage loss in the internal scan chains. However this can be reduced if the TAMs are brought under the scan compression as proposed in [19].
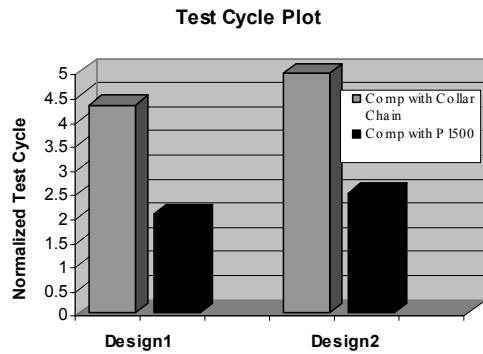
Test Cycle Plot

Figure 10. Test cycle required for SoC designs

This case study also highlights how the flexibility and cost effectiveness of the proposed combination (collar chain with combinational compression) can play crucial role in testing large industrial designs with identical blocks especially in the scenario presented in [7]. It should also be noted that the compression achieved is heavily influenced by no-isolation versus isolation due to change is X-densities. But there are situations for example, where three processor cores will be surrounded by a single test collar and tested at the same time. However if it is a modular design, it generally makes sense to use the same partitioning for test as that used by design for developing it. There would be no point in developing the three core test block with single test collar around it, when design treats it as three separate components from the perspective of design re-usability to bin parts based on lower functionality requiring independent test content for each. The modularity is usually decided by designers and is generally not a variable that can be manipulated by DFT engineers.

VIII. CONCLUSION AND FUTURE WORK

In this paper, we analyzed the limitations of modular test architectures. Based on the analysis, we proposed a test plan for hierarchical test architectures. We demonstrated the feasibility of the test plan using commercial ATPG tool and also presented experimental results that showed 50% reduction in DFT area using the block isolation method. Future work involves developing a test plan for test architecture using sub-optimal test collar with area and testing time as primary constraints.

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