Cross-Memory Polynomial Modeling for RF Circuits

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Abstract — **A new behavioral model is proposed which can provide similar accuracy to the memory polynomial model (MPM) but is shown to have a more efficient architecture for digital hardware implementation. These features have been achieved by the proposed formulation, in which the nonlinear weights of the memory terms are a function of only the present input sample. The new approach is evaluated and compared with the conventional MPM using a Wideband Code Division Multiple Access (WCDMA) signal applied to two different amplifier circuits.**

Index Terms — *behavioral modeling; memory polynomial; digital predistortion; linearization; memory effects.*

I. INTRODUCTION

Modern wireless communication industries are developing at a rapid pace. The increasing demand for high data rates is resulting in increasing bandwidths of modulation schemes used in telecommunication standards. Very often widened signal bandwidths and efficient PA architectures lead to inevitable memory effects which considerably degrade the quality of the modulation on the transmitted signal. Moreover, these modern standards have highly varying envelope signals with high peak-to-average power ratios (PAPR), even more than 10 dB. This large variation makes it challenging to have both a linear and energy efficient system.

One main approach to overcome the aforementioned problems is using digital predistortion to compensate for the memory effects and to linearize the system. The predistorter can be made by inverse modeling. The model should include memory and nonlinearity effects [1], [2]. For this purpose, numerous methods have been proposed in the literature [1]-[3]. Among them, Volterra-based models have been extensively used, thanks to their simplicity and good performance [4]. One of the most well-established classes of Volterra-based models is the memory polynomial model (MPM) [5] and those originating from it [4]. MPM has been extensively used as the reference model for comparison with new methods, because of its relatively good accuracy and mathematically compact form. The model can be further improved by including cross terms at the cost of increased complexity [4].

In this paper, a novel model is proposed by a modification to the MPM. With the suggested formulation, the new cross-memory polynomial model (CMPM) partly benefits from the effect of cross terms in the generalized memory polynomial model (GMPM), although it has the same number of coefficients as MPM. The model will be evaluated and compared with MPM. The results confirm its suitable performance for a wide bandwidth and over a wide range of power levels. Optimum architectures for both MPM and CMPM are also proposed to reduce the floating-operation per second (FLOPS) [6]. Based on this architecture the CMPM is more efficient in FPGA implementation than the MPM.

The paper is organized as follows. In section II, the approach is introduced. Section III discusses the evaluation results, and the conclusion is made in section IV.

II. MODELING APPROACH

A conventional MPM is formulated as [5]

$$y(n) = \sum_{m=0}^{M-1} g_m\left(\left|x(n-m)\right|\right) x(n-m) \qquad (1)$$

where $g_k\left(\left|x(n-m)\right|\right)$ is the nonlinearity term, and m is the memory depth. This equation shows that the output is the weighted sum of the input samples at recent time instants. The weight of each sample is a nonlinear function of the same sample, defined by

$$g_m\left(\left|x(n-m)\right|\right) = \sum_{k=1}^{K} a_{km} \left|x(n-m)\right|^{k-1} \qquad (2)$$

where K is the nonlinearity order, and a_{km}'s are the coefficients which should be identified. In this paper, g_m is called the nonlinear weight. The nonlinear function indicates the nonlinearity of the memory effect.

MPM yields very good results in modeling nonlinear circuits with memory. Its performance can even be improved if the cross terms are included in the formulation [4], [6]. The modified model is the generalized memory polynomial, denoted as follows

$$y(n) = \sum_{m=0}^{M-1} \Big[g_m\big(\big|x(n)\big|, \big|x(n-1)\big|, \ldots, \big|x(n-(M-1))\big|\big)$$
$$.x(n-m)\Big] \tag{3}$$

$$g_m\big(\big|x(n)\big|, \big|x(n-1)\big|, \ldots, \big|x(n-(M-1))\big|\big) =$$
$$\sum_{k=1}^{K} a_{km}^{(0)} \big|x(n)\big|^{k-1} + \sum_{k=1}^{K} a_{km}^{(1)} \big|x(n-1)\big|^{k-1} + \cdots \tag{4}$$
$$+ \sum_{k=1}^{K} a_{km}^{(M-1)} \big|x(n-(M-1))\big|^{k-1}$$

As can be clearly seen, the number of coefficients in the generalized formulation has been increased. This rise leads to a higher computational load.

This paper proposes a new model, which has the simplicity of the memory polynomial formulation, but partly benefits from the cross terms, like in GMPM. The idea is to use the magnitude of the present input sample to compute the nonlinear weights of the memory terms. This modification is originated from the fact that the system has memory, and its recent samples are linked together. Evaluating the validity of this assumption is the subject of this paper. The suggested new model is written as

$$y(n) = \sum_{m=0}^{M-1} g_m\big(\big|x(n)\big|\big) x(n-m) \tag{5}$$

$$g_m\big(\big|x(n)\big|\big) = \sum_{k=1}^{K} a_{km} \big|x(n)\big|^{k-1} \tag{6}$$

The number of coefficients is the same as in MPM. It should be mentioned that, although only the first order of the delayed input is used in the formulation, the method still models nonlinear memory effects. That is because the weight of each term is still nonlinear, even though it is now a nonlinear function of only the current sample.

Since the memory term is at a different time from the variable of the nonlinear weight for m≠0, eq. (5) has cross terms which endow the model with an improved characterization performance compared to those found in eq. (3), and which can compensate for the simplification of the nonlinear function in eq. (6). This feature is discussed in the next section. Moreover, the absolute input value only at the present time is considered for the nonlinear gain computation. Hence the complexity, especially for FPGA implementation, can be reduced and the model is more computationally and energy efficient although the number of the coefficients is the same as the memory polynomial. This gain of efficiency can be illustrated by referring to table I [6] and Fig. 1. In all diagrams of Fig. 1, the complex-complex multipliers are illustrated in dark gray, while the light gray circles are complex-real multipliers and the white circles indicate real-real multipliers. If a standard architecture for the FPGA implementation is used as in Fig. 1a, more FLOPS will be utilized than if the proposed

architecture in Fig. 1b is used. This is mainly due to the higher number of complex-complex multiplications in Fig. 1a. It is worth mentioning that the propagation delay difference due to the branch in Fig. 1b connecting the input to the last multiplier is not a critical issue and can be compensated, if required, by inserting a delay block in that branch.
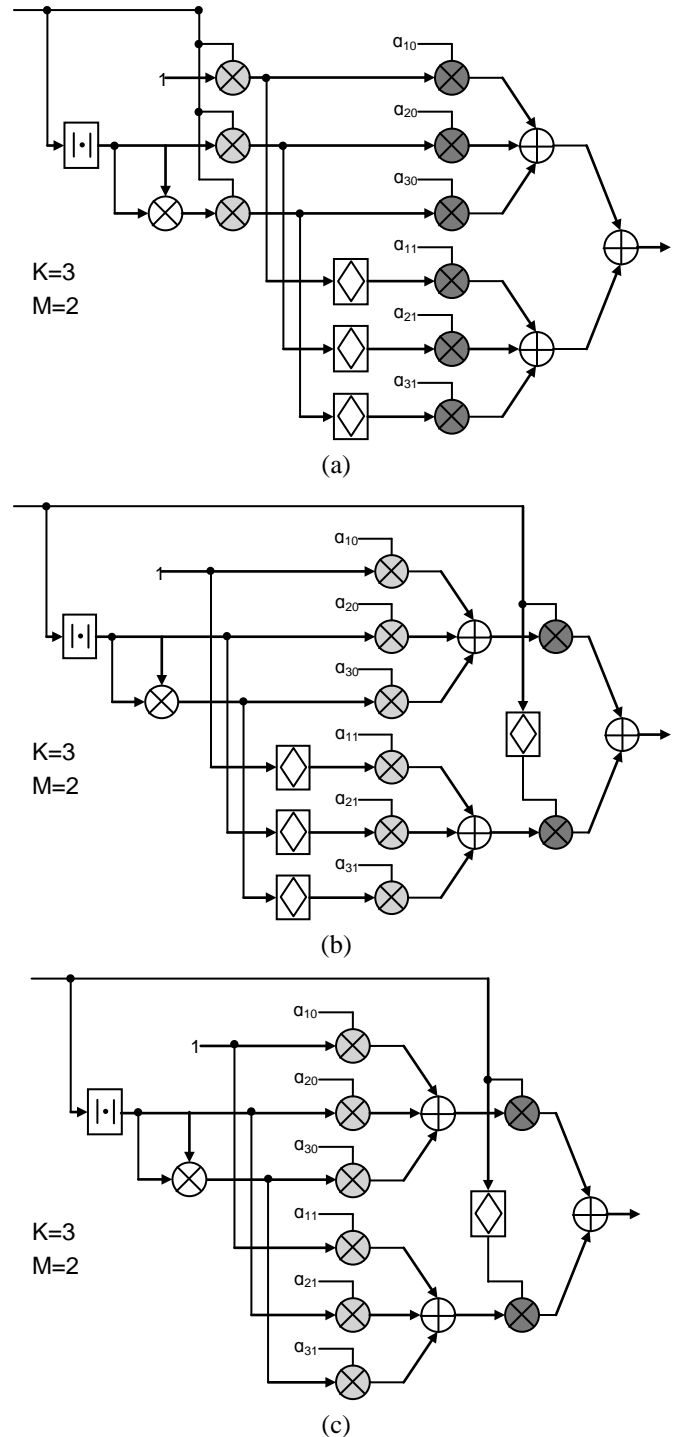

(a)

(b)

(c)

Figure 1.   Standard architecture of MPM, b) proposed architecture for MPM and c) proposed architecture for CMPM.

If the same optimized architecture is applied in CMPM, it can be easily seen that a lower number of delay blocks than in MPM is required, while the rest of the circuit remains the same as for MPM, as shown in Fig. 1c. Therefore the overall FPGA architecture complexity has been reduced by using the CMPM.

Like the MPM, the equations for determining the coefficients are linear, and common methods like Recursive Least Square can be used to find them.

Operation	Number of FLOPs
Conjugate	0
Delay	0
Real addition	1
Real multiplication	1
Complex addition	2
Complex-real multiplication	2
$|.|^2$	3
Complex – complex multiplication	6
Square-root	6~8

III. EVALUATION RESULTS AND DISCUSSION

The new model is evaluated by comparing its performance with MPM, as well as with a memoryless model which is defined by $M=1$ in eq. (5). The model has been identified by applying a WCDMA single-carrier signal to the amplifier. Only 3000 time samples were used for the parameters estimation. The performance is then evaluated using a much longer sequence comprising about 50000 samples. The carrier frequency in both cases is 2.14 GHz. The recursive least square method is used for solving the set of linear equations to find the coefficients of eq. (6). The performances of the models are examined by testing two amplifier evaluation boards.

The first device under test, referred to as Amp #1, is a Sirenza amplifier evaluation board, and the second one, hereafter indicated by Amp #2, is a Freescale amplifier. Both devices are tested such that their instantaneous power exceeds the 1 dB compression point. The test setup is illustrated in Fig 2. It consists of an arbitrary waveform generator (AWG) and a vector signal analyzer (VSA), both connected to a PC. The baseband digital signal is generated in the PC and uploaded into the AWG. Then the AWG converts the signal into an RF time-domain waveform with a 2.14 GHz carrier frequency. The generated AWG output signal passes through the amplifier and is detected and captured by the VSA. The VSA converts the waveform back into the baseband digital domain using its internal ADCs. The digitized output is fed back to the PC for processing in MATLAB. Note that in these experimental evaluations the aim is to show the suitable accuracy of the model. So a PC has been used for the
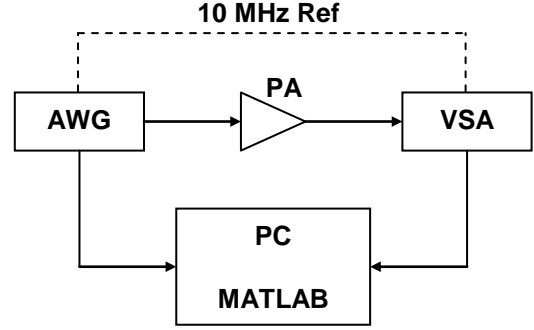

Figure 2.   Measurement set-up for modeling.

computations and the FPGA architectures have not been implemented yet.

The measurement and its corresponding modeling results for a single carrier WCDMA signal applied to Amp #1 are shown in Fig. 3. In this evaluation, CMPM and MPM have the same memory depth and polynomial order of 4 and 7, respectively. The figure illustrates the highly suitable performance of the proposed models although the instantaneous power level of the amplifier is reaching the 2 dB compression point.

To show the consistency of the CMPM, the Amp #2 output has been measured and modeled. The results are shown in Fig 4. In this case both the MPM and CMPM have the same memory depth and polynomial order of 3 and 9, respectively. The convincing performance of the CMPM is also proved in this evaluation which uses a WCDMA signal reaching the 2 dB compression point.

The assessment of the performance can be made easier with table II. The criteria in table II for assessment is the normalized mean square error (NMSE), defined by

$$NMSE(dB) = 10\log_{10}\left[\frac{\frac{1}{N}\sum_{n=1}^{N}|\hat{y}(n)-y(n)|^2}{\frac{1}{N}\sum_{n=1}^{N}|y(n)|^2}\right] \quad (7)$$
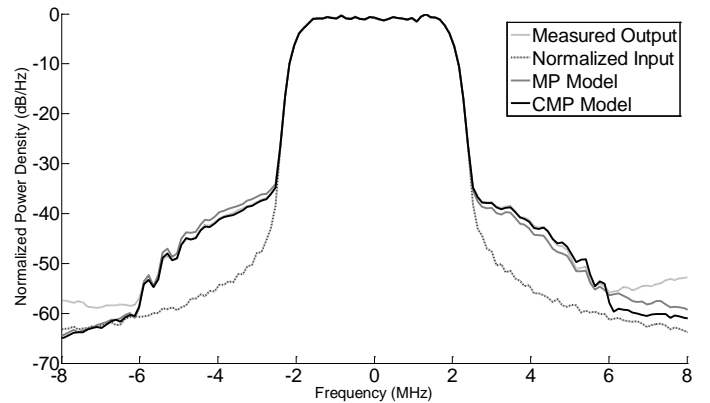

Figure 3.   Modeling performances of MPM and CMPM for Amp #1 with a measured 1xWCDMA signal reaching the 2 dB compression point of the DUT.
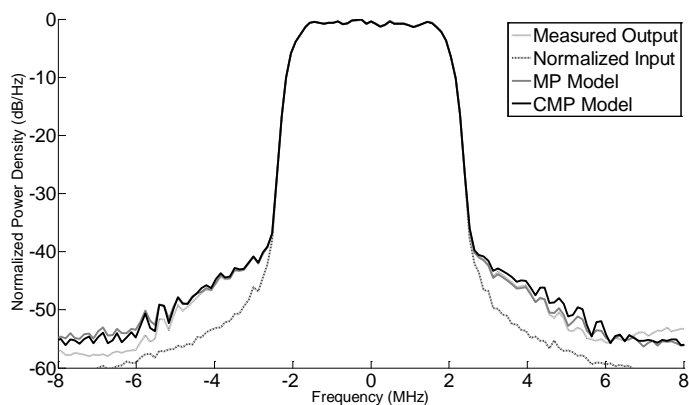
Figure 4. Modeling performances of MPM and CMPM for Freescale Amp #2 with a measured 1xWCDMA reaching the 2 dB compression point of the DUT.
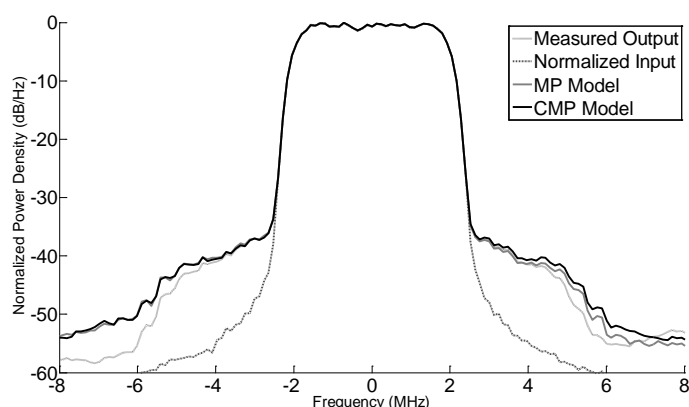

Figure 5. Modeling performances of MPM and CMPM for Freescale Amp #2 with a measured 1xWCDMA reaching the 2.5 dB compression point of the DUT.

TABLE II.   PERFORMANCE OF CMPM AND MPM FOR MEASURED WCDMA SIGNAL RECHING THE 2 DB COMPRESSION POINT

		NMSE (dB)
Amp #1	ML	-27.4
	MPM	-38.5
	CMPM	-39.1
Amp #2	ML	-27.8
	MPM	-39.1
	CMPM	-39.6

in which $\hat{y}(n)$ and $y(n)$ are the estimated and the measured output, respectively.

A quantitative comparison is shown in table II where ML stands for the memoryless model. According to the table, the CMPM has a slightly better performance than MPM. Note that the big differences between NMSE values of both MPM and CMPM, and the NMSE value of the memoryless model indicate the existence of memory.

The modeling capability of both MPM and CMPM have upper limit for high output power. This fact can be seen when the output power of Amp # 2 for instance is increased to reach the 2.5 dB operating point. Although both models in this case have still NMSE values higher than -39 dB, their prediction of adjacent channel power levels start to degrade as shown in Fig. 5. Therefore, like any other models care has to be taken when working with the CMPM and MPM at power levels close to saturation.

All these results confirm the reliable performance of CMPM, although the nonlinear weight is simplified into a function of only the present input sample. The model has the capability to model the behavior of a microwave power amplifier with power levels close to saturation.

IV. CONCLUSION

A novel formulation for modeling RF circuits is proposed. It is a modification to the memory polynomial with memory weights as a nonlinear function of the present input sample, implying a simpler and more energy-efficient implementation in FPGA. The performance of the proposed model is assessed using WCDMA signals on two different devices. The experimental results show that the method can suitably model nonlinear circuits with memory effects in wideband applications and up to high power levels close to saturation.

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