350 mV, 0.5 mW, 5 GHz, 130 nm CMOS Class-C VCO Design Using Open Loop Analysis

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Abstract — **This paper presents a design method of LC cross-coupled oscillators using a large signal S-parameter open loop approach instead of typical negative resistance methodology presented in the literature. The open loop technique allows extraction of loaded quality factor of the complete oscillator circuit and observe how oscillation conditions change with increasing oscillator signal amplitude. As a result, highly non-linear modes of oscillator operation (class-C in this case), can be analysed without necessity of conducting time consuming transient simulations. The presented method is not technology specific and allows fast calculations under changing bias conditions. The simulated class-C 130 nm CMOS oscillator operates at 5 GHz from a reduced power supply of 350 mV, achieving average SSB phase noise better than -115 dBc/Hz at 1 MHz offset from the carrier, using a relatively low loaded quality factor ($Q_L \approx 10$) LC resonator. The presented VCO has tuning range of 280 MHz to compensate for process and temperature variations. In steady state, MOSFET devices in the oscillator operate in class-C i.e. for $V_{GS} < V_{th}$, resulting in low power consumption of less than 0.5 mW RMS.**

Keywords — **CMOS, voltage controlled oscillators, open loop analysis, large signal S-parameters.**

I Introduction

Design of LC oscillators at RF frequencies using deep CMOS technology becomes a challenge to meet the stringent performance of modern communication standards. A trend for battery operated, hand held devices, promotes low power solutions and leads to improved energy consumption of whole RF systems. This forces the RF designers to find the ways to implement circuits under reduced voltage headroom and lower current amplitudes - clearly a quite demanding task if the expected performance has to remain high. In case of oscillators, the performance metrics include: low phase noise to avoid the destructive effects of reciprocal mixing, large signal swing to provide enough drive for mixers or frequency dividers and small footprint for cheap integration. These requirements become even more stringent when the deep submicron technologies are taken into account due to an unique set of additional phenomena related to high degree of scaling.

The practical observation of LC oscillator behavior leads to conclusion that the power consumption of the circuit is not constant. In general, less power is consumed to sustain the oscillations than to start them. Thus, once signal is generated and its amplitude is stable, the bias conditions of the circuit can change such the amount of current drawn from the power supply is decreased resulting in smaller RMS power. This can be obtained for example by setting the gate voltage of MOS transistors below a threshold voltage so the only force periodically switching the transistors "on" and "off", comes from the sinusoidal signal generated by the oscillator itself. Thus, while biased in class-C, active devices in the oscillator core stay "on" for shorter time during each period than during start-up [1–6].

The described case is not trivial to analyse in practical circuits, as the conditions to sustain oscillations differ from the ones during start-up period. To start the oscillator we use two DC biased cross-coupled transistors producing negative resistance which net amount is larger than combined losses of a resonator. The negative resistance is a small signal parameter found as a derivative of the corresponding bias state and can't be calculated in class-C where DC current is 0. Moreover, because the oscillator is a closed-loop system, it is impossible to observe how various circuit parameters change with increasing amplitude, especially the loaded quality factor of the resonator (controlling res-

onator selectivity and phase noise of the oscillator)

When negative resistance approach becomes no longer practical, a feedback analysis can be used instead, even if the original circuit of interest is not normally considered to be a feedback oscillator. This paper proves this can be achieved by combining two techniques known as Alechno's virtual ground circuit transformation [7] and Randall-Hock's open loop gain correction [8] leading to a simple, intuitive design methodology of LC cross-coupled oscillators operating under class-C bias.

II Open loop analysis of a cross-coupled oscillator

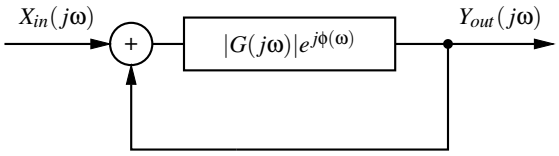

Fig. 1: Generic positive feedback oscillatory circuit.

The feedback approach to oscillator relies on two important parameters: open loop gain and phase response of the loop. As depicted in Figure 1, a feedback oscillator consists of generic transconductance block, which output is sampled back to the input. Under certain conditions, this circuit has the potential to become unstable if for zero input excitation $X(j\omega)$ the output response $Y(j\omega)$ is non-zero. These conditions are widely known as Barkhausen's criteria:

$$|G(j\omega)| = 1 \rightarrow \text{Amplitude condition} \tag{1}$$

that is the system has unity open loop gain $G(j\omega)$, and

$$\phi(\omega) = 2k\pi \quad \text{for} \quad k = 0, 1, \ldots \rightarrow \text{Phase condition} \tag{2}$$

the total phase shift of open loop equals zero (or multiple of 2π). Phase $\phi(\omega)$ of open loop leads to a loaded quality factor Q_L described by:

$$Q_L = -\frac{\omega_0}{2}\frac{\partial\phi(\omega)}{\partial\omega}\bigg|_{\omega=\omega_0} \tag{3}$$

a) Circuit transformation

To successfully analyse a cross-couple oscillator using open loop technique, the feedback loop around the circuit has to be recognised first. In many oscillators that are considered negative resistance systems, this loop can be obscured and additional circuit transformations may be necessary to identify it. One of the simplest methods of such transformations found in literature is Alechno's technique [7]. Although in cross-coupled oscillators the feedback loop is rather obvious to identify, Alechno's technique proves useful still, as it allows to rearrange circuit such the main parasitics can be included in open loop analysis. The described method makes it possible to introduce a virtual ground in one of the nodes, not grounded under normal operation (the oscillator output for example). It has to be noted that as in any transformation of this kind, resulting circuits are different to the closed loop counterparts and thus represent approximations with finite accuracy. However (1)-(3) are now available directly (either through calculations or simulations), making open loop analysis possible.

Figure 2 depicts classical low voltage cross-coupled VCO architecture, with single differential planar inductor, tank capacitance being a combination of MIM capacitor and MOS varactors, and NMOS pair used for compensation of energy losses in the resonator. Applying Alechno's transformation to this circuit, yields an open loop equivalent presented on 3. Roman numerals on both figures correspond to the same nodes in both circuits. Quick glance at the transformed circuit reveals that, in fact, two loops can be recognised. The main loop under consideration is formed between drain of M_2 and gate of M_1, and the second one, made of LC components around M_1. In general, the LC-M_1 loop can be unstable itself, however only in a presence of M_2 (and the main loop) the proper Barkhausen's criteria for whole VCO can be defined. This is due to the fact that in practical situations, amplitude condition (1) for both loops is much different.

The loop has been opened at node II, with respective ports P_1 and P_2 characterised with generic impedance Z_s. The transformation has been conducted in steps. First, all of the points at RF ground have been connected together (V_{dd}, V_{SS}, V_b and V_{tune}). Then, the outputs at node IV has been connected to the virtual ground, leading to a single feedback loop between M_1

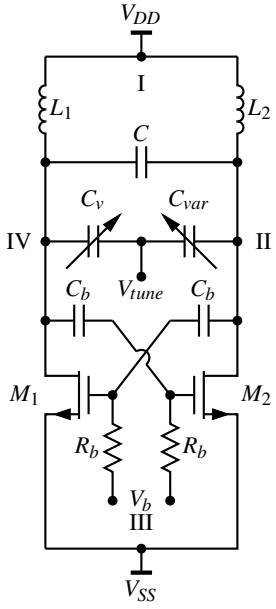

Fig. 2: Low voltage CMOS VCO topology.

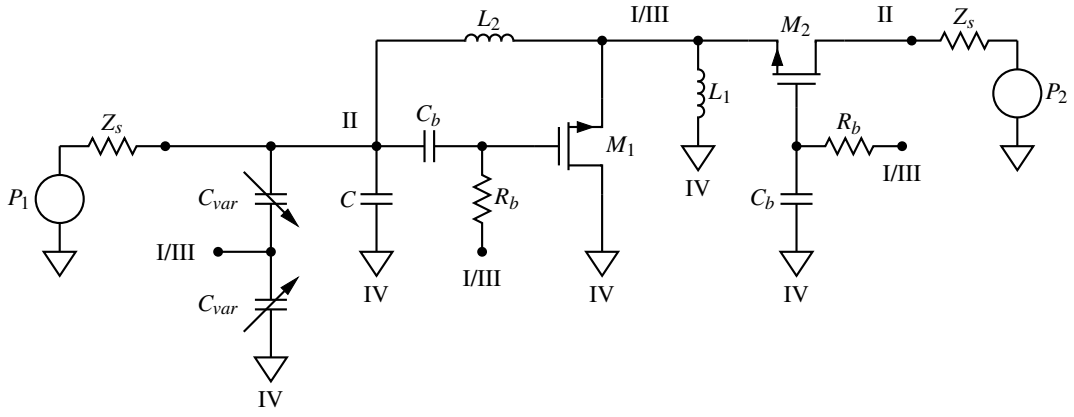

Fig. 3: Open loop equivalent of cross-coupled oscillator.

and M_2 with a single reference to the virtual ground. After transformation, all transistors and varactors have to be DC biased through set of blocking capacitors and RF chokes, omitted from Figure 3 for clarity.

Equations (1)-(3) can be calculated using relatively fast two port network S-parameter analysis in any RF circuit simulator and post processed in MATLAB. We have recognised that since an oscillator operates under large signal regime, large signal S-parameters are the most suitable for the characterisation. Small signal behaviour can be still extracted, providing that relatively low magnitudes of test signals from P_1 and P_2 are applied.

b) Gain correction

The last important step of the analysis is a correction of calculated results due to unmatched impedances of open loop ports and test generators P_1 and P_2. In theory, during circuit simulation, corresponding reflection coefficients on each port could be extracted for every frequency of interest and subsequently used to calibrate Z_s for each source. This process however is tediously slow and becomes impractical especially during oscillator start-up and bias changes. It is then more practical to use Randall-Hock's correction of open loop transfer function accounting for unmatched port impedances [8].

$$G_{cr}(j\omega) = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}} \tag{4}$$

The corrected gain (4) allows to estimate (1)-(3) at the same time capturing small and large signal behavior of an open loop cascade from Figure 3.

III VCO DESIGN

Using the circuit presented on Figure 2 together with UMC 130 nm RF process libraries, 5 GHz, low power CMOS oscillator has been designed. The important circuit parameters are presented in Table 1. The loaded quality factor of the resonator averages on 10 at resonant frequency of 5 GHz. Gates of both transistors are biased through DC block capacitor C_b and high resistance RF resistor, forming RF block to ground. Cross-coupled pair is formed using minimum length devices. As circuit is intended to operate well under 1 V and with limited headroom, no current source was used, allowing for relatively large output signal swing, in the range of V_{dd}. Oscillator produces two out-of-phase sinusoidal signals at nodes II and IV respectively, that

Table 1: Circuit paramters of the proposed VCO.

Part	Dimensions	Value@5 GHz	Comments
$L_1 + L_2$	OD=220 µm, W=9.7 µm, S=1.6 µm, NT=2	1.4 nH Q=19	single differential inductor
C	W=0.2 µm, L=20 µm, NF=10, M=4, nm=5	440 fF Q=50	MOM RF
C_{var}	W=2.54 µm, L=0.25 µm, NF=6, M=5	221.3 fF Q=40–80	MIS RF
M_1, M_2	W=1.2 µm, L=0.12 µm, NF=5, M=6	–	RF
C_b	W=50 µm, L=40 µm, M=1	2 pF Q=50	MIM RF
R_b	W=1 µm, L=7 µm, M=1	7 kΩ	High-res. RF
C_{prst}	ideal	0.15 pF	load and layout parasitics

in the practical circuit have to be extracted through the buffer amplifiers, not included in this paper. To account for parasitic capacitances of layout and buffer amplifiers, two 0.15 pF capacitors were included in the circuit, connected in parallel between nodes II-III and IV-III, respectively.

IV Simulated results

a) Open loop transfer function analysis

The circuit from Figure 3 has been co-simulated in Eldo RF and MATLAB. Large signal steady state (SST) simulation allows to extract scattering parameters matrix of interest as function of frequency and port amplitude. When the correction algorithm (4) is employed, a real source impedance of 50 Ω can be used directly. To achieve good accuracy, SST has been set to 11 harmonics. During start-up, the circuit is biased with $V_b = 500$ mV, initially consuming RMS power of 0.82 mW from 350 mV supply voltage. When oscillator reaches steady state, the power consumption increases to 0.94 mW RMS. The increased power consumption can be attributed to two factors. Firstly, large signal swings influence voltage controlled parasitics of the transistors, such more current is drawn by them during operation of the oscillators. Secondly, because drain currents of cross-coupled pair in any LC oscillator have a from of short pulses, they introduce harmonics on top of DC signal required for bias. Thus, in steady state some additional power from the source is transferred into the harmonics.

Figures 4 and 5 present the results of gain and phase calculations of corrected open loop transfer function, $G_{cr}(j\omega)$. Tuning voltage V_{tune} is set to 0 as the varactors are used to tune the oscillator in steady state. Also, for this tuning voltage the varactors have also the lowest Q factor and potentially have the most influence on transient behavior of the tank.

When the signal amplitude of the test sources is small, in the range of 30 µV, the circuit provides gain margin of approximately 8.44 dB at frequency of 4.82 GHz where phase shift around the loop equals 0, refer to curves marked with ◯ on Figures 4 and 5. This rather excessive gain margin during start-up is due to size of the transistors used. When in class-C the same devices have to deliver narrow current pulses yet with enough amplitude to compensate the total resonator losses and finite output conductances of cross-coupled pair. When the same transistors are biased, such a DC current flows through them (i.e. during oscillator start-up), the drain currents in the range of 1.2 mA introduce the open loop gain of 8 dB. Figure 5shows that the resonant frequency of the open loop cascade is only 5% lower than of the closed loop case, approximated from transient analysis to be equal to 5.08 GHz. When signal amplitude rises, the non-linearities of both transistors cause compression of gain, until it's margin drops to 0 dB (curves marked with △). This is the moment when oscillator reaches it's steady state. To observe this behavior, the amplitude on both ports of open loop cascade has to increase from initial small signal value to 470 mV. Note, that under large signal conditions, a loaded quality factor of the oscillator, as depicted on Figure 6, drops by 50% from its initial value of 9.4

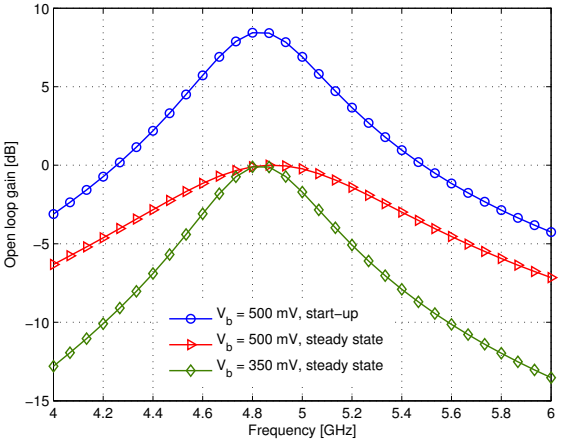

Fig. 4: Open loop gain of the proposed oscillator.

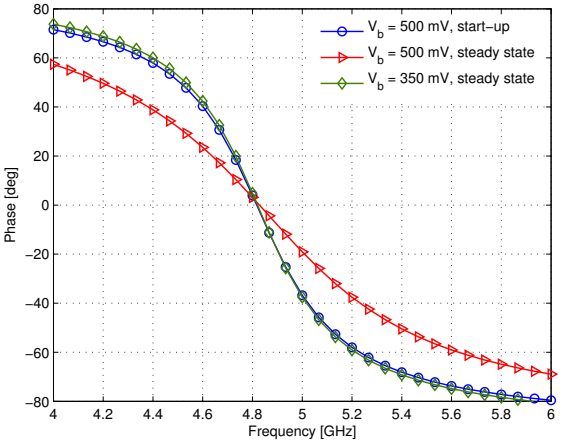

Fig. 5: Phase characteristics of the proposed oscillator.

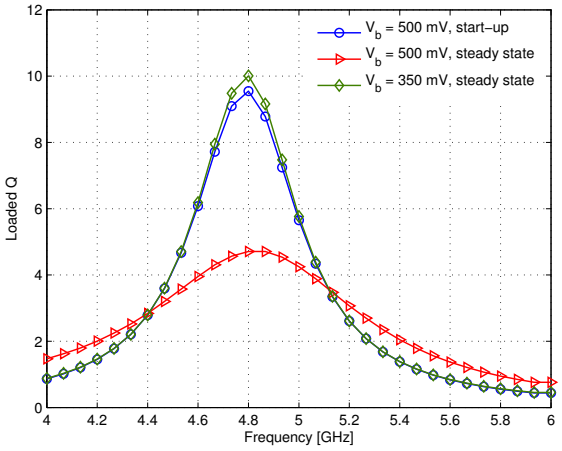

Fig. 6: Loaded Q factor of the proposed oscillator.

Table 2: Performance comparison with state of the art class-C oscillators.

Ref.	CMOS	VDD	f_0	f_m	$\mathcal{L}(f_m)$	FBW	P	FOMT
	µm	V	GHz	MHz	dBc/Hz	%	mW	dBc/Hz
[2]	0.18	1.2	4.84	1	-125	2.1	3.4	-180
[3]	0.18	0.2	4.5	1	-104	1	0.114	-166
[4]	0.18	1	3.1	1	-123	20	1.57	-197
[5]	0.13	1	5.2	3	-131	14	1.4	-197
[6]	0.09	0.6	5.1	3	-127	2.6	0.86	-181
This work	**0.13**	**0.35**	**5**	**1**	**-115**	**5.6**	**0.5**	**-187**

down to 4.71. This can be explained by instantaneous drain current increase during switching, effectively increasing drain to source conductances in both transistors and present higher load to the resonator. In the last case, curves marked with $\diamondsuit$ on Figures 4-6 represent steady state response of the same oscillator where the bias conditions has been modified. Both transistors are now biased as class-C devices and $V_b = 350$ mV for $V_{th} = 400$ mV. Less power drawn from the source reduces the amount of current in the circuit, resulting in smaller oscillation amplitude. When the oscillator operates in class-C, the voltage amplitude on both ports necessary to decrease the open loop gain to 0 dB is close to 250 mV. The transient simulation conducted to compare these results showed the signal with amplitude of 268 mV, that is 7% larger than found using the open loop technique. The main source of this error comes from the use of varactors, that are inherently non-linear, and therefore introducing additional set of amplitude dependant parasitics that are distributed differently in the closed and open loop circuits. Although in the case of class-C bias scheme a generated RF amplitude is smaller, the transistors stay "on" for shorter period than during start-up, effectively reducing a loading presented to the resonator. This manifests itself in a improvement of loaded quality factor, that as depicted in Figure 6, now much closer to the value of original, unloaded tank. One can think that the Q_L increase should immediately translate into smaller phase noise, however in the case of class-C oscillator this mechanism is not straightforward. Firstly, relatively short current pulses consists of larger number of spectral components that are responsible for noise folding in the oscillators [9]. Secondly, class-C VCO operates under smaller RMS power and generates smaller amplitudes that may not necessarily translate into an improved phase noise performance.

b) Phase noise and figure of merit comparison

To compare the performance of various oscillators, a normalized parameter known as figure of merit with tuning range (FOMT) can be used. This function allows fair benchmark of phase noise of oscillators working at different frequencies, tuning ranges, fractional bandwidths and power consumption. One generally accepted $FOMT$ has the following form:

$$FOMT = \mathcal{L}(f_m) - 20log\left(\frac{f_0}{f_m}\frac{FBW}{10}\right) + 10log\,(P) \tag{5}$$

where $\mathcal{L}(f_m)$ is phase noise at frequency offset of f_m, f_0 is resonant frequency, FBW is fractional bandwidth in % of the carrier and P is a maximum DC power consumption of the core expressed in mW. Since in the presented paper class-C oscillator does not consume power in a static sense, (5) is modified such a RMS power is taken into account instead.

As in the case of open loop analysis from the previous section, oscillator biased with $V_b = 500$ mV has been simulated. The average SSB phase noise at 1 MHz offset from the carrier is equal to -116.37 dBc/Hz, for 0.94 mW RMS power consumed from 350 mV power supply. For the tuning range of 280 MHz and 5 GHz carrier, (5) yields $FOMT_1 = -185.4$ dBc/Hz.

The average phase noise for the proposed class-C VCO biased at $V_b = 350$ mV is equal to -115.66 dBc/Hz at 1 MHz from the carrier. This proves that improved Q_L does not translate into lower phase noise in this case, as the amplitude of RF signal is now smaller due to a smaller power consumption. Transient simulations reveal that RMS power in steady state for this bias condition is equal to 0.48 mW, 49% less than during start-up. These values translate to $FOMT_2 = -187.6$ dBc/Hz, thus although phase noise is only 0.7 dB worse for the proposed bias scheme, the figure of merit improves by more than 2 dB. Table 2 presents a performance comparison of realised state of the art class-C VCOs presented in the literature. Even though the results presented in this paper are simulated, there is still 5 to 7 dB safety margin of theoretical FOMT in comparison to the VCOs with tuning ranges below 10%. Authors of [4] and [5] employed switched capacitor or varactor arrays, effectively increasing FOMT over a single varactor solution presented in this paper by the cost of the chip area, not included in the comparison.

V Conclusion

In this paper we have presented a new analysis and design methodology of class-C cross-coupled CMOS oscillators. The use of open loop approach and large signal S-parameter simulations allow to estimate oscillation amplitude and load quality factor of the circuit, and subsequently optimise it if necessary for low phase noise and low power operation. The obtained results match these of transient simulations, confirming that the proposed open loop technique provides simple and intuitive yet effective tool improving the design of high performance, low voltage CMOS oscillators.

Acknowledgments

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