A 90nm, Low Power VCO with Reduced KVCO and Sub-band Spacing Variation

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***Abstract*— In this paper we present the design of a low power VCO with reduced variations in VCO gain (K_{VCO}) and sub-band spacing resolution (f_{res}). The proposed VCO is designed using a 90nm CMOS process to cover a tuning range of 23%. Variations in K_{VCO} and f_{res} are reduced by factors of 6 and 17 respectively over a conventional sub-banded VCO, designed using the same process, to meet the same tuning range. This makes the proposed VCO more suited to stable PLL operation with its reduced K_{VCO} requirements resulting in an improvement in phase noise performance over the conventional VCO by 2 dB. Due to the reduced loading on the VCO tank achieved by the presented design, power consumption is kept extremely low at 850 μW from a 1 V supply.**

I. Introduction

Phase-locked loops (PLLs) are important building blocks in modern communication systems. At the heart of the PLL is a voltage-controlled oscillator (VCO), responsible for generating the output frequency of the PLL. In order to account for process, voltage and temperature (PVT) variation, and to support multi-standard operation, the VCO is required to operate over a sufficiently large frequency range. This requirement, together with the reduced supply voltages that accompany modern low power nanoscale technologies, imply the design of a VCO with a large tuning constant (K_{VCO} — frequency change per volt). A large K_{VCO} is however highly undesirable in terms of optimum phase noise performance as it translates any noise on the VCO control line to frequency modulation of the output signal. This leads to increased jitter of the output signal, which can be particularly problematic for PLLs operating as frequency synthesizers [1].

This issue is typically addressed by dividing the tuning range into discrete smaller bands (sub-bands), such that a wide tuning range can be realised with a small K_{VCO} for each sub-band [2]. Illustrated in Fig. 1 is a VCO tuning curve which has been divided into n discrete sub-bands to achieve the same original tuning range, but with a smaller K_{VCO}.

The illustration of Fig. 1 is not realistic however, as in practice sub-band spacing resolution (f_{res}) and K_{VCO} are not constant. Instead they reduce over sub-bands, resulting in a reduction in the frequency range covered by the VCO. This leads to excessive K_{VCO} values required to meet the specified tuning range which will degrade the phase noise performance of the VCO. In addition, ΔK_{VCO} is very severe on PLL operation as PLL loop bandwidth is proportional

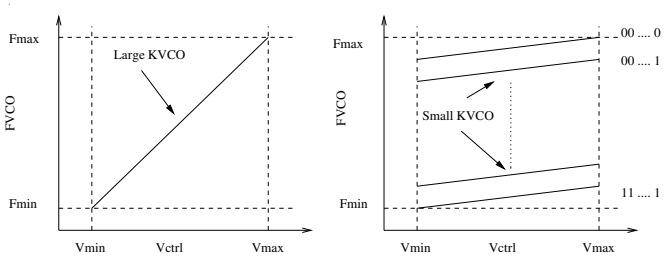

Fig. 1. Sub-banding of single VCO tuning curve

to K_{VCO}. Therefore, in the absence of additional calibration, loop bandwidth will vary with ΔK_{VCO} hence affecting the noise performance and loop stability of the PLL itself. Although a reduction in ΔK_{VCO} alone will improve PLL noise performance and loop stability, it should be accompanied by a corresponding reduction in f_{res} variation (Δf_{res}) to optimise the potential tuning range and achieve a more PVT robust solution. Therefore to address this issue, we present the novel design of a low power, sub-banded VCO with reduced ΔK_{VCO} and Δf_{res}.

The paper is organised as follows. Section II details the problem of ΔK_{VCO} and Δf_{res}. Related work is reviewed in Section III. The proposed technique and circuit implementation are presented in sections IV and V. Experimental results are then presented in section VI with a conclusion given in section VII.

II. Sub-banded VCOs

Dividing the tuning range into n sub-bands is conventionally achieved using a switched capacitor array which consists of $n-1$ equi-valued (or binary weighted) switchable capacitors, selectable via a digital word. The switching in(out) of one capacitor adds(subtracts) from the total tank capacitance, forcing VCO operation to move down(up) one sub-band respectively.

The reduction in K_{VCO} occurs because the percentage change in capacitance, caused by the varactor, reduces as more capacitance is added to the tank. The reduction in f_{res} then occurs because the percentage change in capacitance, caused by switching in a capacitor, reduces as more capacitance is added to the tank. As a result both K_{VCO} and f_{res} reduce as more capacitors are switched in.

In [3] it was shown that band to band variation

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reduces K_{VCO} by the following factor:

$$\Delta K_{VCO} = C\sqrt{C} \tag{1}$$

where C represents a change in capacitance (*for example*: from switching in the entire switched capacitor array).

This changes f_{res} by the same factor which, as shown in (2), preserves a constant percentage overlap between bands:

$$\Delta OV \propto \frac{\Delta f_{res}}{\Delta K_{VCO}} \tag{2}$$

where ΔOV represents the variation in percentage overlap between bands.

As a result, the overall frequency range covered by the VCO also reduces by the same factor leading to a reduction in the tuning range as follows:

$$TR_{reduced} = \frac{(\frac{2\Delta F}{C\sqrt{C}})}{2F_{max} - (\frac{\Delta F}{C\sqrt{C}})} \cdot 100 \tag{3}$$

where the reduced tuning range (%), frequency range and maximum frequency of the VCO are represented by $TR_{reduced}$, ΔF and F_{max} respectively.

As seen from (3), the original tuning range can simply be restored by increasing ΔF by $C\sqrt{C}$ which is achieved in practice by increasing the average K_{VCO} by the same factor. This however is highly undesirable because, as explained in section I, any increase in K_{VCO} leads to an increase in noise translation from VCO control line to the output signal.

III. Related Work

Some methods have been proposed to reduce ΔK_{VCO} and Δf_{res}. In [4] the use of an additional serial LC-tank with variable inductor configuration is proposed to reduce ΔK_{VCO}. Due to the additional LC-tank this solution consumes large power and die area. In [5] the use of additional varactors to reduce the ΔK_{VCO} of groups of sub-bands is proposed. This solution however requires an additional complex biasing scheme to reduce ΔK_{VCO} down to a specified level. In addition, both solutions do not address Δf_{res}. If ΔK_{VCO} is reduced then, as shown in (2), Δf_{res} should also be reduced by the same amount to preserve a constant overlap between bands. This achieves a more PVT robust VCO which optimise's its dynamic tuning range while avoiding frequency dead-zones at extreme corners. In [6], [7], the use of an additional varactor array in conjunction with the conventional switched capacitor array is proposed to achieve simultaneous reductions in both ΔK_{VCO} and Δf_{res}. In [6] unused varactors in the array are simply switched out whilst those in [7] are connected to a fixed potential. Due to the additional array, the quality factor of the tank (Q_{tank}) is degraded over conventional approaches, leading to degraded phase noise performance and increased power consumption.

IV. Proposed Technique

The proposed technique simultaneously reduces both ΔK_{VCO} and Δf_{res}. Unlike [6], [7], this is achieved using one single array resulting in reduced loading of Q_{tank}. The array consists of $n-1$ switchable varactor branches to split the specified tuning range into n sub-bands, as shown in Fig. 2. Each varactor branch is selectable via digital control signals which select(de-select) the branches by switching them in(out) respectively. De-selecting varactor branches by completely switching them out offers a more attractive solution over fixing them to a fixed potential [7], as it further reduces loading of Q_{tank} for the higher frequency bands, where the majority of the branches will be switched out.

A. Design Procedure

Each varactor branch is sized according to its required C_{max} and C_{min} values necessary to achieve the specified K_{VCO} and f_{res}. The procedure for calculating these values is as follows:

1) Calculate C_{min} for the sub-band of interest (C_{min_n}):

$$C_{min_n} = \frac{1}{L(2\pi f_{max_n})^2} \tag{4}$$

where f_{max_n} is the maximum frequency of the sub-band, taking into account the specified f_{res}. This is calculated as follows:

$$\begin{aligned} f_{max_n} &= f_{max_n-1} - f_{res} \\ &= f_{max_n-1} - (\Delta f_{n-1}(1 - OV)) \end{aligned} \tag{5}$$

where the maximum frequency and frequency range covered by the previous sub-band are f_{max_n-1} and Δf_{n-1} respectively.

2) Calculate the change in C_{min} between the sub-band of interest and the previous one ($\Delta C_{min_n \to_n -1}$):

$$\Delta C_{min_n \to_n -1} = C_{min_n} - C_{min_n-1} \tag{6}$$

where C_{min_n-1} is the minimum capacitance of the previous sub-band.

3) Calculate C_{max} for the sub-band of interest (C_{max_n}):

$$C_{max_n} = \frac{1}{L(2\pi f_{min_n})^2} \tag{7}$$

where f_{min_n} is the minimum frequency of the sub-band, taking into account the specified K_{VCO}. This is calculated as follows:

$$f_{min_n} = f_{max_n} - (K_{VCO} V_{tune}) \tag{8}$$

where V_{tune} is the tuning voltage range.

4) Calculate the change in C_{max} between the sub-band of interest and the previous one ($\Delta C_{max_n \to_n -1}$):

$$\Delta C_{max_n \to_n -1} = C_{max_n} - C_{max_n-1} \tag{9}$$

where C_{max_n-1} is the maximum capacitance of the previous sub-band.

Equations (6) and (9) give the required C_{min} and C_{max} values respectively for the sub-band of interest. Once obtained, the relevant varactor branch is sized to achieve both values and inserted into the array. Repeating this procedure $n-1$ times thus completes the array.

V. Circuit Description

To verify the proposed technique a low power, sub-banded VCO with center operating frequency of 4.8 GHz was designed for a 1P9M 90nm CMOS process. The tuning range of the circuit is divided into 16 sub-bands with reduced ΔK_{VCO} and Δf_{res}. The schematic of the VCO is shown in Fig. 2.

The LC-tank consists of a differential spiral inductor (L) and p-n junction diode varactors (D_1, D_2). A differential spiral inductor is used due to its higher quality factor (Q) and lower area requirements over its single ended counterpart [8], which measured an inductance of 4 nH and Q of 16 at 4.8 GHz. P-type diode varactors are used due to their higher Q-values and linearity over the alternative N-type MOSFET varactors available for the process used. Anodes of both varactors are clamped to Vss through resistors (R) to ensure no forward biasing, requiring them to be de-coupled from the tank using metal-insulator-metal capacitors (C_s). This offers the additional advantage of further improving varactor linearity [9], thereby reducing AM-FM up-conversion of flicker noise from the bias source [10].

Flicker noise from the bias source can be completely eliminated by removing the bias source [11]. However this causes the amplitude of the oscillator signal to become more susceptible to PVT variations. Therefore to achieve a potentially more PVT robust circuit, a bias source is used which employs p-type MOSFETs ($P1$, $P2$) due to their lower flicker noise. Negative resistance necessary for oscillation is then generated by the cross-coupled NMOS transistor pair ($N1$, $N2$).

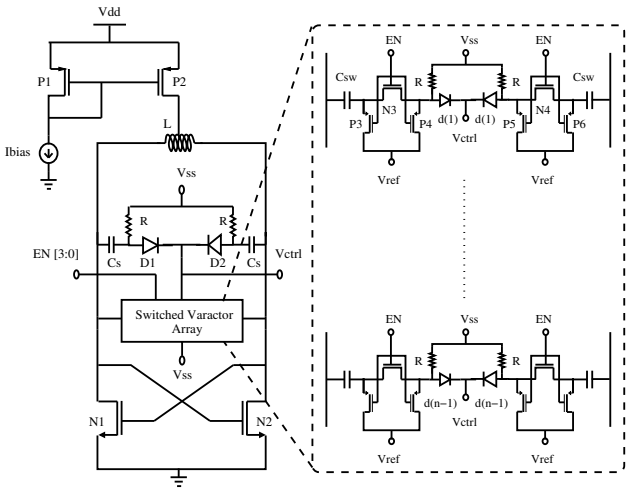

Fig. 2. Circuit diagram of the proposed VCO

The switched varactor array consists of 15 branches, also illustrated in Fig. 2. An identical varactor configuration that was used in the LC-tank is employed, where NMOS transistors ($N3, N4$) are used to switch the varactors in(out) of the bank. These switches are made wide to reduce their series resistance which loads Q_{tank} when EN = 1. Loading of Q_{tank} is further reduced by PMOS transistors ($P3 - P6$), which maintain the switches completely off when EN = 0 [12].

VI. Experimental Results

The proposed VCO was designed for a 1P9M 90nm CMOS process. To demonstrate the achieved reductions in ΔK_{VCO} and Δf_{res}, the proposed VCO was compared with a conventional VCO designed using the same process, to meet the same tuning range. The resulting tuning characteristics of both VCOs are shown in Fig. 3, with a performance comparison of both circuits presented in Table I.

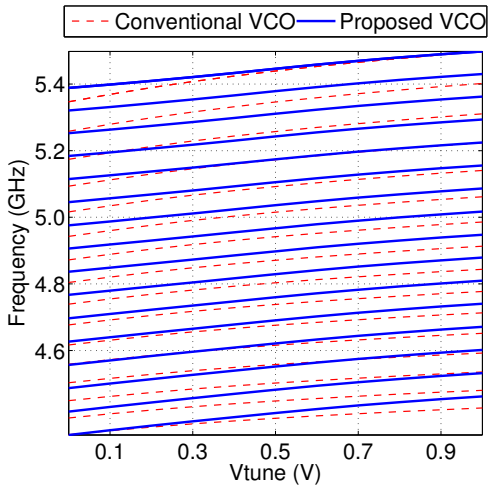

Fig. 3. Simulated tuning characteristics of the VCOs

TABLE I
Performance Summary Comparison

	Conventional VCO	Proposed VCO
Technology	90nm CMOS	
Power Supply	1V	
ΔF	1150 MHz (4.35GHz – 5.5GHz)	
TR	23%	
ΔK_{VCO}	± 30%	± 4.6%
Δf_{res}	± 30%	± 1.7%
OV	40%	≈ 40%
Power Consumption	900 μW	850 μW

Table I clearly shows the reductions achieved in ΔK_{VCO} and Δf_{res} by factors of 6 and 17 respectively over the conventional VCO. This is shown in further detail in Figs. 4 and 5 which plot K_{VCO} and f_{res} respectively over all sub-bands for both VCOs.

As explained in section II and shown in Fig. 3, designing with reduced ΔK_{VCO} and Δf_{res} enables the specified tuning range to be covered with lower K_{VCO} values for the upper frequency bands, hence improving the phase noise performance of these bands. This improvement is shown in Fig. 6 which plots the simulated phase noise of the top frequency band for both VCOs (i.e. worst case scenarios). Measurements taken at 1 MHz offset from the carrier frequency (f_{osc} = 5.45 GHz) show the proposed VCO to achieve a phase noise improvement of 2 dB. This improvement is slightly larger than predicted due

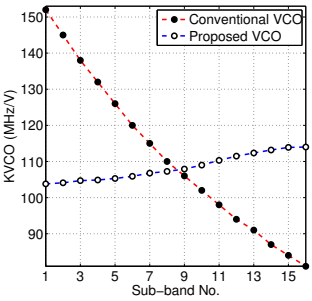

Fig. 4. K_{VCO} over sub-bands

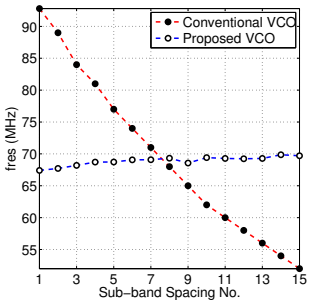

Fig. 5. f_{res} over sub-band spacings

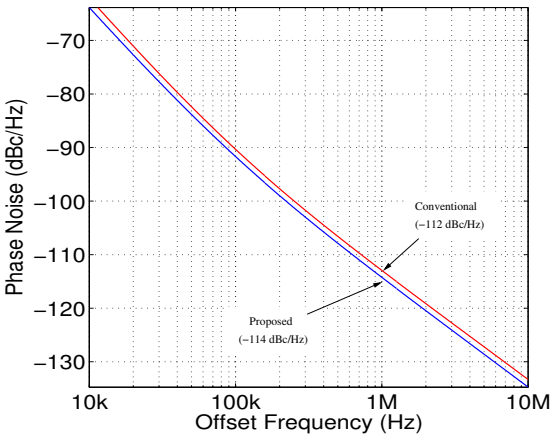

Fig. 6. Simulated Phase Noise of VCOs

to K_{VCO} reduction alone, as the lower K_{VCO} requirements for the proposed VCO will increase the L/C ratio of its tank. This leads to an improved Q_{tank} [8] hence offering a further improvement in phase noise.

Table I also shows the low power requirements of the proposed technique. This is due to the reduced loading of Q_{tank} as a result of using one single array consisting of varactor branches which can be completely switched out when not in use. Power consumption is slightly less than for the conventional VCO (due to the higher L/C tank ratio [8]) and is significantly less than for previously reported techniques concerned with reducing ΔK_{VCO} and Δf_{res}. This is shown in Table II which displays the overall performance of the proposed technique against such previously reported publications.

VII. Conclusion

This paper presented a novel design of low power, sub-banded VCO exhibiting reduced ΔK_{VCO} and Δf_{res}. The design was verified for a 90nm CMOS process and achieves ΔK_{VCO} and Δf_{res} values of $\pm 4.6\%$ and $\pm 1.7\%$ respectively, to maintain the percentage overlap between bands at $\approx 40\%$. Reductions in ΔK_{VCO} and Δf_{res} are by factors of 6 and 17 respectively over a conventional sub-banded VCO designed using the same process, to meet the same tuning range. This makes the proposed VCO more suited to stable PLL operation. In addition it reduces K_{VCO} requirements resulting in a phase noise improvement over the conventional VCO by 2 dB. Reduced loading of Q_{tank} then keeps the overall power consumption extremely low at 850 μW from a 1 V supply.

TABLE II
Performance Comparison Against Recent Publications

Ref.	[4]	[5]	[6]	[7]	This Work
ΔK_{VCO} ($\pm\%$)	12	4.4	20.4	12.5	4.6
Δf_{res} ($\pm\%$)	N/A [a]	N/A [a]	N/A [a]	9	2.2
ΔF (MHz)	1320	1050	720	825	1150
Technology	0.25μm BiCMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	90nm CMOS
Power Supply (V)	2.8	2.8	1.8	1.8	1
Power (mW)	11.2	– [b]	9	– [b]	0.85

[a] Δf_{res} not addressed, hence reducing PVT robustness.
[b] Not specified for VCO used.

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