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Reconfigurable Class S Power Amplifiers at RF and Microwave Frequencies

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***Abstract*- When a delta-sigma modulator (DSM) is placed before a class D switching stage the combination can be used to amplify time varying envelope signals. However a bandpass DSM is commonly employed and is required to have a sampling frequency approximately four times the carrier frequency. At RF or microwave frequencies proprietary hardware was previously needed to implement the DSM. However, it is shown here in simulation and from experimental measurement that a suitable DSM for class S power amplifiers can be implemented at RF and microwave frequencies using mid-range FPGA technology.**

***Index Terms*- Class S, efficiency, power amplifiers, sigma-delta modulation**

I. INTRODUCTION

It has been forecast that co-design of DSP algorithms and power amplifier characteristics will lead to improved efficiency, linearity and wider operating bandwidths [1]. One example of this type of co-design is the class S PA. It can achieve high efficiency through DSP generation of the input signal to an efficient switched mode PA. In recent years there has also been increased interest in system on chip (SoC) design which involves incorporating a large number of electronic components on a single integrated circuit (IC). The aims of improved efficiency and linearity for a high frequency transceiver SoC design requires the integration of digital, analog, mixed signal and radio frequency functions in a single design. Publication of work on class S power amplification has increased with interest in finding suitable means of integrating the baseband DSP and RF front end functions of wireless devices. Class S PA theory is detailed in many sources including [2] and [3], results of simulations for devices operated in current mode and voltage mode at high frequency are shown in [4] and [5] respectively. Experimental measurements for a complete design at RF frequencies are not as widely available. This is because implementing a complete class S PA at high frequencies is a difficult task which supposes achieving high sampling frequencies for the delta-sigma modulation (DSM) stage.

Although previous implementations of the DSM for high frequency have been achieved these are expensive as they require fabrication and are often designed for signals at specific frequencies [6]. In this paper we present a reconfigurable platform to drive high frequency class S amplifiers using mid-range FPGA boards with embedded multi-gigabit serial links.

II. THEORY

A typical Class S power amplifier is shown in Figure 1.

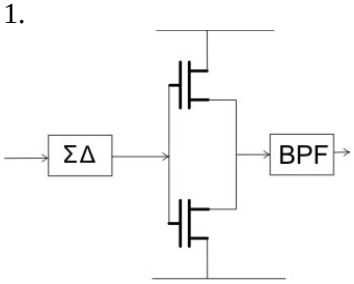


Fig. 1. Conventional Class-S power amplifier

The class S PA contains a DSM connected in series with a class D switch-mode amplifier stage and bandpass filter. A conventional design uses a bandpass DSM with a sampling frequency four times the carrier frequency of the transmit signal.

In this paper a new approach is proposed to circumvent this limitation and allow design of the class S PA with a DSM sample frequency equal to a fraction of the output signal carrier frequency. The proposed amplifier is described as a combination of a lowpass or bandpass sigma-delta modulator in series with a mixing stage, a class D switch-mode power amplifier and finally a bandpass filter. This is a novel

implementation using a frequency shifting stage and successfully integrates both the DSM and frequency shifting functions on the FPGA board.

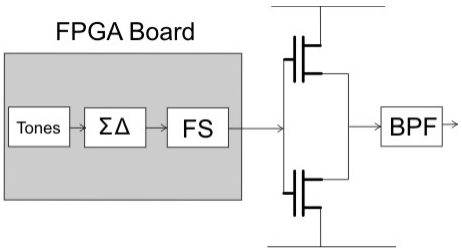
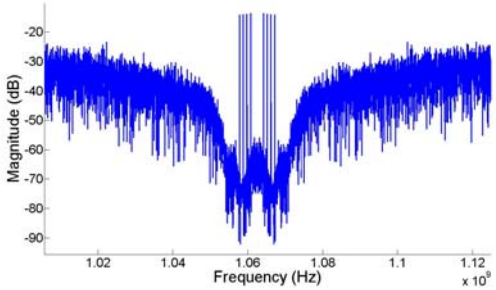


Fig.2. Proposed Class S power amplifier

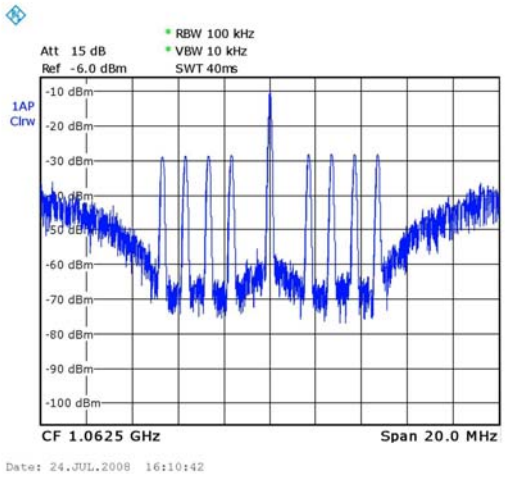
Operation of the new design is as follows: An analog input signal is converted to a two or three level digital signal by a lowpass DSM. Next a frequency shifting stage on the FPGA receives the DSM output and copies it to the multi gigabit transceiver (MGT) on the FPGA board. The signal data rate is adapted here to fs/2 and digital mixing is performed by processing the signal samples at this point with predetermined integer values. The differential Common-Mode-Logic (CML) signal at the output of the MGT is the high frequency signal needed to drive the switch mode amplifier stage. The final stages are described as a voltage mode class D amplifier with tuned output matching network.

III. SIMULATION AND MEASUREMENT

The proposed architecture is first simulated in Matlab to determine the limitations at the required frequency of operation. In this example the sampling frequency of the DSM stage is 106.25MHz, the bandwidth of the transmit signal is 3MHz and the final output sampling frequency chosen was 1.06GHz. The resulting output signal spectrum for this setup from simulations in Matlab is shown in Figure 3(a). In Figure 3(b) the output signal from the multi-gigabit transceiver port of a Spartan 3 FPGA evaluation board measured on a Rhode and Schwarz FSL spectrum analyzer is plotted.



(a)



(b)

Fig.3. (a) From simulation in Matlab, (b) From experimental measurement of FPGA board

IV. CONCLUSION

In this paper a new approach is proposed to allow design of the class S PA with a DSM sampling frequency equal to a fraction of the carrier frequency. This enables easy integration of the switch mode power amplifier for SoC designs and in the short term an effective, low cost and reconfigurable testbench for further research in this area. It is planned to extend this work to test the performance of various switch mode power amplifier stages.

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