# Hardware Design for Quadrature Phase Detection Algorithm in ECVT

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***Abstract*—Core processing for calculating phase and amplitude of the detected signal was built on FPGA (Field-Programmable Gate-Array) platform. Phase shift demodulation algorithm employs IP core provided by Xilinx FPGA. Direct digital synthesizer (DDS), multiplier, accumulator, and CORDIC (coordinate rotation digital computer) modules were used as excitation-reference signal generator, signal multiplication, accumulation, and conversion to polar coordinate in order to conduct trigonometric operation respectively. Hardware design was emulated on MATLAB-Xilinx System Generator to observe its performance. Phase detection range 0-114.58$^o$ and mean absolute error 0.58$^o$ have been achieved. Data processing rate solely at digital signal stage was approximately 100data/s suitable for 32-channel ECVT (electrical capacitance volume tomography) system.**

***Keywords—quadrature demodulation; phase detection; system generator; FPGA; ECVT***

## I. INTRODUCTION

Phase detection is one of the most important feature in data acquisition system for electrical capacitance volume tomography (ECVT). ECVT is a volumetric (real-time 3D) tomography technique based on capacitance measurement which has replaced classical system in two-dimensional slicing for tomography imaging [1]. Data acquisition system collects data obtained from sensor to be formed and sent to computer which manipulates the data pattern into image using specific algorithm.

In the well-known circuitry for capacitance to voltage (C-V) conversion, measurement accuracy is affected by phase conformity between output C-V signal and reference signal. This circumstance makes phase tracking necessary for system's reliability to reduce phase error [2][3]. Fig. 1 shows a phase sensitive demodulation (PSD) mechanism in front of C-V circuit to extract information from measured capacitance.

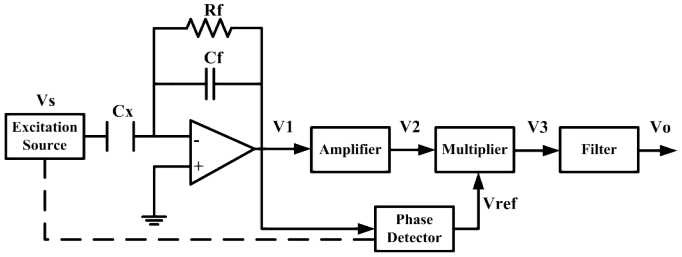


Fig. 1. Capacitance to voltage circuitry with phase sensitive demodulation

According to Fig. 1, if both $V_{ref}$ and $V_2$ signals have identical phase, $V_o$ will only related to amplitude of input signals. However, practically two signals added into demodulator will generate additional phase difference which decreases output amplitude and causes measurement error. The additional phase difference is relevant toward stray capacitance, and different stray capacitance brings different phase angle. Therefore, phase shift will impose certain error. By using coherent demodulation to detect the signal with phase tracer circuit, this kind of problem can be well addressed. Consequently, multiplier output will reach maximum, circuit is stray-immune, in the same time sensitivity and stability of the system can be improved [2].

Performance improvement will be achieved by implementing most functionality into digital hardware rather than analog. FPGA is employed as control processing core, excitation signal generation, and signal demodulation. The modular design of FPGA produces minimal hardware overhead, flexible, fast, and stable in order to facilitate further development of measurement system.

## II. QUADRATURE DEMODULATION

In phase detection, sine signal needs to be demodulated with measured parameter. Digital demodulation makes use of reference signal generated from DDS to digitally modulate measured signal to obtain its amplitude and phase.

$$u(n) = A\sin\left(\frac{2\pi}{N}n+\theta\right);\ i(n) = \sin\left(\frac{2\pi}{N}n\right);\ q(n) = \cos\left(\frac{2\pi}{N}n\right)$$
$$R = \sum_{n=0}^{N-1} i(n)\cdot u(n) = \sum_{n=0}^{N-1} \sin\left(\frac{2\pi}{N}n\right)\cdot A\sin\left(\frac{2\pi}{N}n+\theta\right) = NA\frac{1}{2}\cos\theta$$
$$I = \sum_{n=0}^{N-1} q(n)\cdot u(n) = \sum_{n=0}^{N-1} \cos\left(\frac{2\pi}{N}n\right)\cdot A\sin\left(\frac{2\pi}{N}n+\theta\right) = NA\frac{1}{2}\sin\theta$$
$$Z = \sqrt{R^2+I^2}\ ;\ \theta = \tan^{-1}\frac{I}{R} \qquad (1)$$

This syncronous modulation and demodulation (PSD also known as phase shift demodulation) has high precision and adaptation level based on matched filter theory which is linier time-invariant by maximizing signal-to-noise ratio (SNR). Considerations in PSD are: input signal frequency and phase must be similar, reference signal should be justified accurately, anticipate phase shift because of stray capacitance and resistance channel, and degradation of SNR due to

frequency difference between driving signal and reference signal.

Demodulation is accomplished through several steps. First, phase difference between digitized reference signal and measured signal is identified. Second, delay the reference signal with specific number from sampling period according to phase difference value obtained from preceding step to match reference signal's phase with measured signal's phase. Last, multiply the measured signal with adjusted reference signal in one sine wave period and then accumulate the results accordingly [4].

Integration of DDS and PSD module into single FPGA hardware improves systematic SNR dan simplifies peripheral circuits. For real-time processing, large amount of data on front-end with high-speed and relatively simple pre-processing architecture are suitable for FPGA implementation [5].

## III. HARDWARE DESIGN METHOD

Phase detection algorithm i.e. phase shift demodulation is built using Xilinx FPGA IP core. DDS, multiplier, accumulator, and CORDIC are functioned as excitation-reference signal generation, signal multiplication, accumulation, and conversion to polar coordinate in order to conduct trigonometric operation respectively.

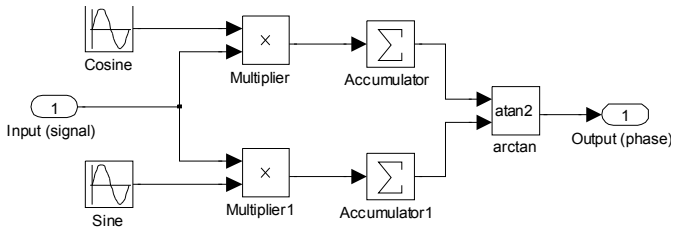


Fig. 2. Quadrature phase detection scheme

Block diagram in Fig. 2 represents signal flow (contains phase shift) with quadrature demodulation mechanism, where accumulation results will be brought to inverse tangent calculation to obtain phase output value. Equation identity of multiplication between sine with sine and sine with cosine also division sine-cosine is elaborated in (2).

$$A\sin(\omega_1 t+\theta)\times\sin(\omega_2 t) = \frac{A}{2}\cos\big((\omega_1-\omega_2)t+\theta\big)-\frac{A}{2}\cos\big((\omega_1+\omega_2)t+\theta\big)$$
$$A\sin(\omega_1 t+\theta)\times\cos(\omega_2 t) = \frac{A}{2}\sin\big((\omega_1-\omega_2)t+\theta\big)+\frac{A}{2}\sin\big((\omega_1+\omega_2)t+\theta\big)$$
$$\tan\theta=\frac{\sin\theta}{\cos\theta} \qquad (2)$$

Therefore, phase can be extracted if the detected signal is multiplied with reference sine and cosine signal, both of which have identical frequency. Sum frequency component is then eliminated by accumulating multiplication result. As been known, accumulation of symmetrical signal with zero offset will produce zero mean value so that the sum frequency component signal will vanish from equation. In the end, with division operation tangent phase angle will be obtained and then the inverse is phase value. Those division and inverse mechanism are conducted after conversion into polar domain using CORDIC operation.

Implementation of the mechanism on Xilinx System Generator is described in Fig. 3

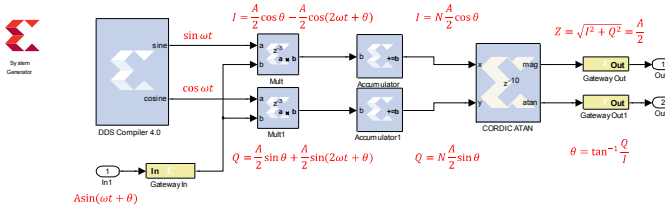


Fig. 3. Xilinx System Generator core block

Whereas, signal flow is depicted in Fig. 4 below.

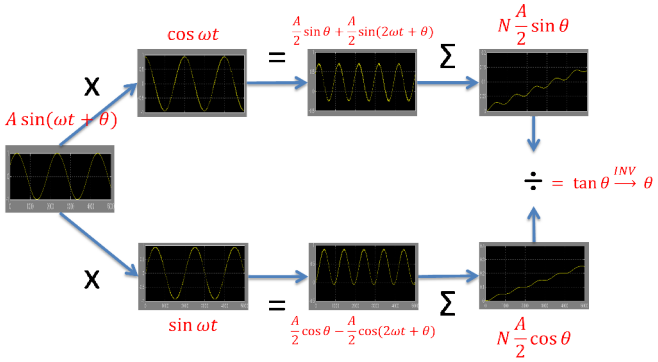


Fig. 4. Quadrature phase detection signal flow

Synchronous sine and cosine signal produced by DDS IP core implemented in FPGA are directly used in digital domain for demodulation. Compared with conventional analog demodulation, the method can eliminate the possibility of frequency mismatch and phase variation between signals. Computation process is conducted in dedicated modules (multiplier-accumulator) and avoiding data buffer so that digital demodulation can be performed online in order to maximize acquisition rate. Consquently, it will introduce a relatively simple system with better reliability [6].

## IV. SIMULATION RESULT

Hardware-software co-simulation using MATLAB-Xilinx System Generator allows to design and observe the characteristics of hardware; on the other hand manipulate the input signal and process the output signal by software. Fixed-point number will be used to maintain consistency with practical running process in digital device [7].

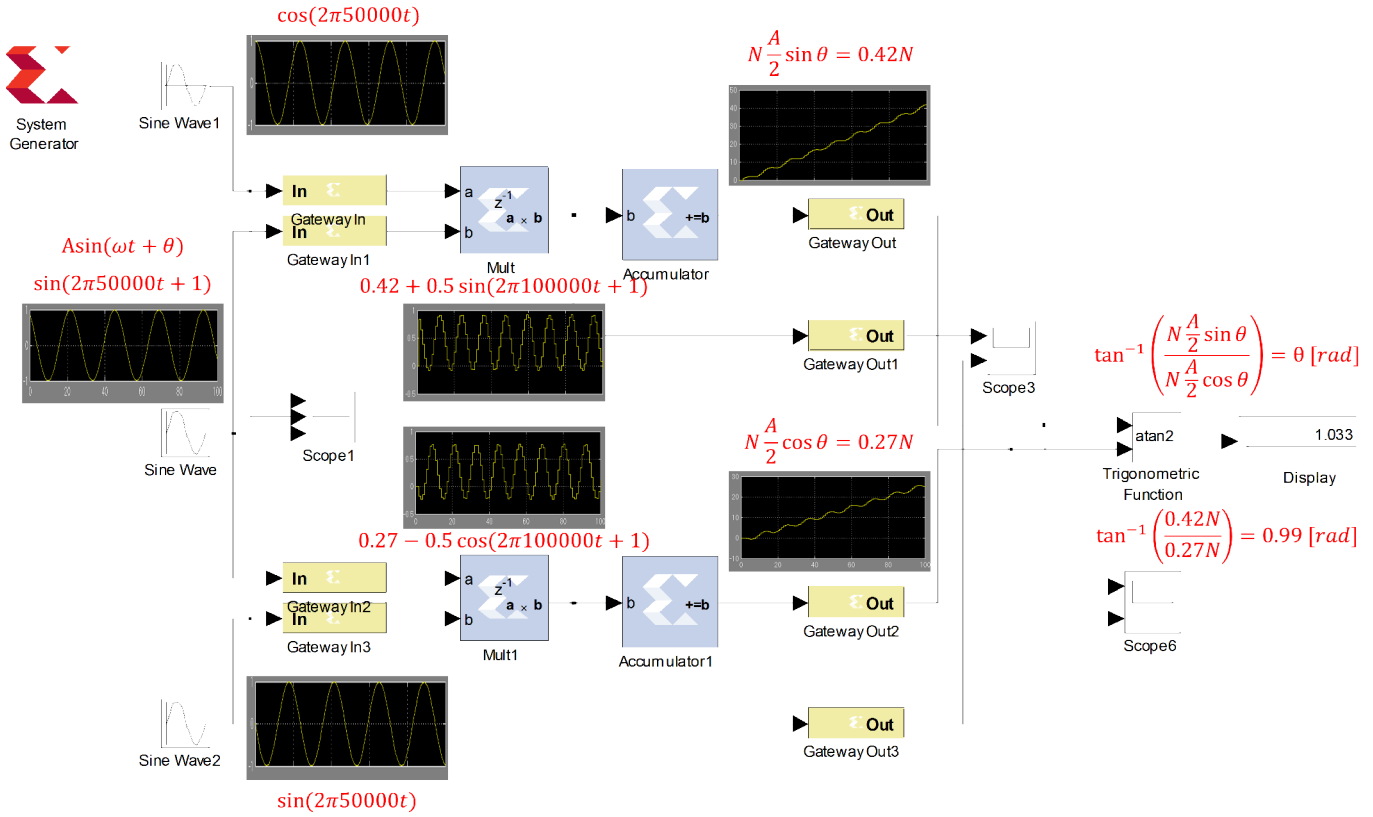


Fig. 5. Implementation of Xilinx IP core for quadrature demodulation

### A. *MATLAB-Xilinx System Generator*

The development issues in hardware design using MATLAB Xilinx System Generator comprises: 1) determining design specification, 2) designing a system in Simulink utilizing System Generator blocks, 3) simulating the design, 4) generating hardware description language (HDL) code, 5) implementing HDL code into target hardware [8]. Step 1 through 3 were applied to foresee system's performance and capability for further ECVT development.

Implementation result of Xilinx IP Core multiplier and accumulator for quadrature demodulation calculation is shown in Fig. 5. In the system, input sine signal 50kHz (chosen operation frequency) is applied with phase shift 1 radian. Hardware multiplier then multiply the signal with each of reference sine and cosine signal where the frequency is set similar to the input signal. Each multiplication result is brought into hardware accumulator to be accumulated thus high frequency component will be eliminated and accumulation of phase function will remain. Trigronometric operation *atan2* (two-input inverse tangent) is applied using MATLAB function. On the display, phase value (in radian) is shown.

### B. *System Overview*

Overview of the system for phase shift demodulation implemented on Xilinx System Generator is shown as following Fig. 6.

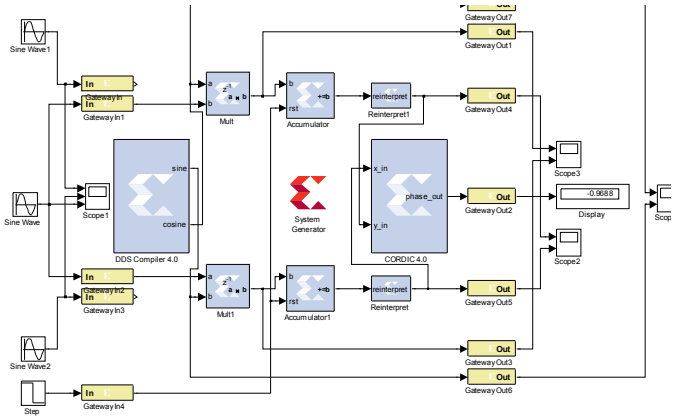

Fig. 6. Quadrature phase detection system overview

From the design, system specification that can be provided is formulated in TABLE I.

TABLE I. SYSTEM SPECIFICATION

| | | | | |
|---|---|---|---|---|
| **Operational Frequency** | | 50kHz | | |
| **Phase Detection Range** | | 0-114.58° / -57.29°-57.29° | | |
| Res=8-bit ; Clk=100MHz ; MAE=0.8529° | Res=16-bit ; Clk=100MHz ; MAE=0.5794° | Res=8-bit ; Clk=200MHz ; MAE=3.6494° | Res=16-bit ; Clk=200MHz ; MAE=3.9960° | |
| **Data Proc. Rate** | 1785 data/s (8Ch) | 416 data/s (16Ch) | 100 data/s (32Ch) | |

Equation (3) and (4) were used to derive data rate and mean absoulte error (MAE) respectively,

$$Throughput = \frac{f_{clk}}{\frac{f_{ADC}}{f_{op}} N_{period} \frac{n(n-1)}{2}} \quad (3)$$

$$MAE = \frac{1}{N}\sum_{i=1}^{N} |f_i - c_i| \quad (4)$$

where $f_{clk}$=hardware clock; $f_{ADC}$=ADC sampling rate; $f_{op}$=operational frequency; $N_{period}$=number of signal period; n=measurement channel; N=number of data; $f_i$=theoretical value; $c_i$=measured value.

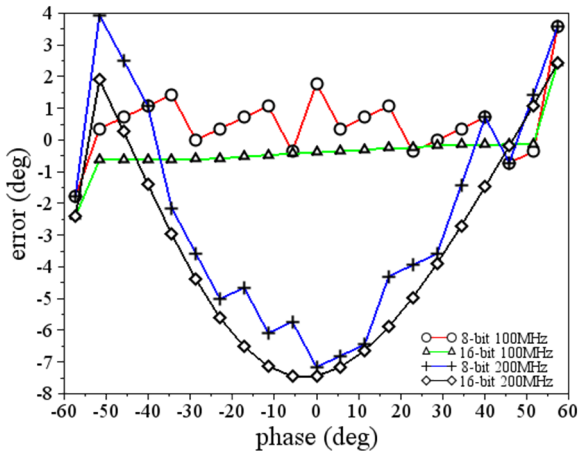


Fig. 7. Measurement error plot

Measurement error is plotted in Fig. 7 showing the most linear result at 16-bit data and 100MHz clock frequency.

## V. CONCLUSION

Core processing for calculating phase and amplitude of the detected signal was designed on FPGA platform. Hardware-software co-simulation using MATLAB-Xilinx System Generator allows to design and observe the characteristics of hardware; on the other hand manipulate the input signal and process the output signal by software. To perform hardware test with real input and output, the design needs to be downloaded onto FPGA and connected with external blocks.

The optimum system design, adjusted to 16-bit data resolution and clock speed 100MHz, gives phase detection range 0-114.58° (or ±57.29°) and mean absolute error 0.58°. Data processing rate solely at digital signal stage is approximately 1785data/s (for 8-channel), 416data/s (for 16-channel), and 100data/s (for 32-channel).

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## REFERENCES

[1] Warsito, W.; Marashdeh, Q.; Fan, Liang-Shih, "Electrical Capacitance Volume Tomography," *Sensors Journal, IEEE* , vol.7, no.4, pp.525,535, April 2007

[2] H. Zhang, D. Ren, L. M. Du, "A new improved data acquisition system for electrical capacitance tomography," Advanced Materials Research, vol. 756-759, pp. 1527-1531, September 2013.

[3] Xuehui Zhang; Huaxiang Wang, "Digital phase-sensitive demodulation in electrical capacitance tomography system," *Intelligent Control and Automation, 2008. WCICA 2008. 7th World Congress on* , vol., no., pp.6730,6733, 25-27 June 2008

[4] Haili Zhou; Lijun Xu; Zhang Cao; Chenfeng Xu, "An alternative digital multiplication demodulation method for electrical capacitance tomography," *Instrumentation and Measurement Technology Conference (I2MTC), 2012 IEEE International* , vol., no., pp.1204,1209, 13-16 May 2012

[5] Xuehui Zhang; Huaxiang Wang; Ziqiang Cui; Lei Tang, "A Novel ECT System Based on FPGA and DSP," *Innovative Computing, Information and Control, 2007. ICICIC '07. Second International Conference on* , vol., no., pp.510,510, 5-7 Sept. 2007

[6] Huaxiang Wang; Ziqiang Cui; Yanbin Xu; Lifeng Zhang; Yongbo He, "Digital signal processing in electrical capacitance tomography," *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on* , vol., no., pp.465,468, Nov. 30 2008-Dec. 3 2008

[7] Lijun Xu; Haili Zhou; Zhang Cao; Wuqiang Yang, "A Digital Switching Demodulator for Electrical Capacitance Tomography," *Instrumentation and Measurement, IEEE Transactions on* , vol.62, no.5, pp.1025,1033, May 2013

[8] Ownby, M.; Mahmoud, W.H., "A design methodology for implementing DSP with Xilinx® System Generator for Matlab®," *System Theory, 2003. Proceedings of the 35th Southeastern Symposium on* , vol., no., pp.404,408, 16-18 March 2003