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# Fundamental Approach in Digital Circuit Design for 1-MHz Frequency PWM Gate Drive Application

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***Abstract*— This paper discusses the design of a digital programmable logic circuit to produce a 5 V - output square wave pulses for four high power MOSFET switches using a fixed PWM circuit. It will be applied to drive the synchronous rectifier buck converter (SRBC) circuit. The PWM signals with multiple fixed time delay of 15 ns, 232 ns, 284 ns and 955 ns are generated. The steps taken to analyze each propagation time delay of each logic gate used and its combination are carefully studied. A multiplexer is added at the output of the logic circuit to select and produce the desired output pulses of 20 % duty ratio. The logic outputs are compared with the analog pulses and results match each other within 1 % in difference.**

***Keywords*— Duty Ratio, Fixed Time Delay, MOSFET, PWM.**

## I. INTRODUCTION

Various researches have been conducted and they are still on-going in power electronics field, especially in high switching frequency of PWM gate drive applications. One example of the PWM gate drive applications is the implementation of a fixed PWM mode circuit. A digital PWM signal usually comes with a fixed delay time. Nowadays, many companies manufacture delay lines in a form of delay chips and processors. Some implement tapped delay line (as shown in Fig.1) in an integrated chip by extracting a signal output within the delay line, optionally scaling it, and usually adding with other taps to form an output signal [1, 2]. Other manufacturers produce delay lines using a fixed combination of logic gates in a single chip [3].

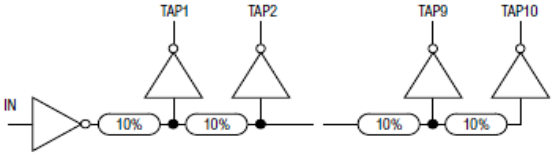


Fig. 1 Tapped Delay Line Diagram

Despite of the purchasing cost, the major drawback is the fixed specification of delay time designed in the chips. This limitation makes it difficult to produce the desired delays in a particular design without referring back to the manufacturers. Furthermore, majority of the design only caters for the value of the delay time, not the duty ratio of the pulses.

However, there has been an increasing research in generating the delay signals using logic gates to overcome the fixed delay problem produced by delay lines chips. In order to produce the required fixed delay time, basic concepts used in producing the delays need to be addressed. The implementation of series of inverters, flip-flops and multiplexers in a delay circuit are commonly used [4-12].

As the system demands for higher performance, application of a high speed clock becomes more important. As the clock signal propagates to a certain path, its duty cycle may distort and require adjustment. In order to maintain the duty cycle, a controlled duty cycle circuit would need an adjustable delay circuit to generate certain delay [13].

This work will concentrate on the fundamental to generate specific delays using a combinational logic gates and how to produce and maintain the duty ratio of 20 %. The delayed signals from the proposed logic gates circuit will be used to feed four driving MOSFETs and drive high and low side switches in SRBC circuit.

## II. METHODOLOGY

This work is based on simulation using Cadence PSpice simulator. Four different circuits are proposed to generate each delay. The proposed basic design of the logic gate delay circuit in this work is a 2-bit multiplexer.

### *A. 15-ns Logic Delay*

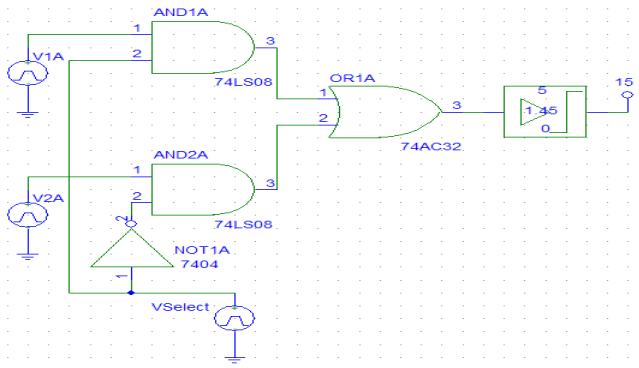


Fig. 2 Schematic for 15 ns Delay

The 2-bit multiplexer as shown in Fig. 2 consists of:

- two 2-input positive 74LS08 AND gates
- two data input signals, *V1A* and *V2A* generated from *Vpulse*, fed to one of the inputs of two 2-input positive 74LS08 AND gates
- a select input, *VSelect* generated from *Vpulse* as the second input for both 2-input positive 74LS08 AND gates
- a 7404 NOT gate connected at one of the inputs of second AND gate
- a 74AC32 OR gate used to combine the logic outputs from the two AND gates and subsequently produce final logic output
- a gain block with limiter (or level shifter), GLIMIT

The *V1A* and *V2A* are the input data signals for the multiplexer as tabulated in Table I. *V1A* signal has to be delayed in order to generate a 5 V - pulse with 200 ns width while *V2A* is the second input with 800 ns width. Here, the settings for *V1A* and *V2A* will be constant for all four proposed circuits. *VSelect* is used to control which data signal to appear at the output of multiplexer (the data input signal from *V1A*). A level shifter with a gain of 1.45 is connected at the output of OR gate to increase final output pulses to be 5 V.

TABLE I INPUT DATA SIGNALS FOR *V1A* AND *V2A*

| ***Vpulse* / Parameters** | ***V1A*** | ***V2A*** | ***VSelect*** |
|---|---|---|---|
| ***V1* (V)** | 0 | 0 | 0 |
| ***V2* (V)** | 5 | 5 | 5 |
| **Delay Time, $T_D$ (s)** | 0 n | 0 n | 0 n |
| **Rise Time, $T_R$ (s)** | 5 n | 5 n | 5 n |
| **Fall Time, $T_F$ (s)** | 5 n | 5 n | 5 n |
| **Pulse Width, $P_W$ (s)** | 200 n | 800 n | 900 n |
| **Period, $P_{ER}$ (s)** | 1 u | 1 u | 1 u |

The implementation of AND gate from 74LS08 with 74AC32 OR gate are chosen to be the suitable combinational logic gate in producing 15 ns delay. These gates are selected due to their small propagation delay time from low to high output level $t_{PLH}$ and small propagation delay time from high to low output level $t_{PHL}$ compared to other types of gate. Table II below shows the comparison of propagation delay based on datasheet of several gates within the same switching characteristic of $C_L$=15 pF, $T_A$=25 °C and $V_{CC}$ of 5 V.

Since 15 ns is a small delay interval, the lowest amount of propagation delay of AND gate and OR gate available in PSpice simulator have to be selected. Looking at the maximum value for AND gate, 74LS08 and 74ALS08 show the lowest propagation delay time. However, 74LS08 has much lower $t_{PLH}$ than 74ALS08. A lower propagation delay time from low to high output level is more important since it determines the start of a pulse which contributes to the delay time. For OR gate, 74AC32 shows the lowest propagation delay at maximum value with 7.5 ns for $t_{PLH}$ and 7.0 ns for $t_{PHL}$. A possible calculation to produce 15 ns delay is (1).

$$9\text{ns(ANDgate)} + 6\text{ns(ORgate)} = 15\text{ns} \quad (1)$$

TABLE II COMPARISON OF PROPAGATION DELAY

| Logic Gate | Part | $t_{PLH}$(ns) | | | $t_{PHL}$(ns) | | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max |
| NOT | **7404** | | **12** | **22** | | **8** | **15** |
| | 74LS04 | 3 | | 10 | 3 | | 10 |
| | **74ALS04B** | **3** | | **11** | **2** | | **8** |
| | 74AC04 | 1.5 | 4.0 | 7.0 | 1.5 | 3.5 | 6.5 |
| AND | 7408 | | 8 | 15 | | 10 | 20 |
| | **74LS08** | **4** | | **13** | **3** | | **11** |
| | 74ALS08 | 4 | | 14 | 3 | | 10 |
| | 74AC08 | 1.5 | 5.5 | 7.5 | 1.5 | 5.5 | 7.0 |
| OR | 7432 | | 10 | 15 | | 14 | 22 |
| | 74LS32 | 3 | | 11 | 3 | | 11 |
| | 74ALS32 | 3 | | 14 | 3 | | 12 |
| | **74AC32** | **1.5** | **5.5** | **7.5** | **1.5** | **5.0** | **7.0** |

### *B. 232-ns Logic Delay*

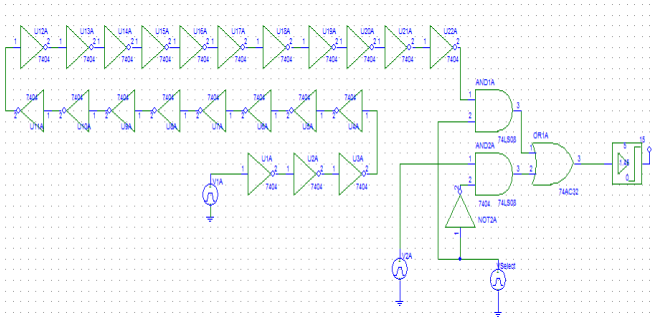

Fig. 3 Schematic for 232 ns Delay

In order to generate a 232 ns delay signal, the same 2-bit multiplexer circuit with same *V1A*, *V2A* and *VSelect* are used as shown in Fig. 3. The additional logic gates used will be a chain of 22 7404 inverters. Again, *VSelect* is used to enable *AND1A* gate and generate the delayed input signal.

Since 232 ns is a bigger delay than 15 ns, a maximum propagation delay time is required in order to obtain the desired value with fewer gates. This is an important factor in order to make a compact and simple design. Referring to Table II, 7404 NOT gate can provide a delay between 8 ns - 22 ns compared to other type of NOT gates. So, this gate can be selected using its 10 ns – delay. A possible calculation to produce 232 ns delay is shown below (2) with 15 ns delay generated from the previous 2-bit multiplexer.

$$[22_{7404\text{NOT}} \times 10\text{ns}] + 15\text{ns} = 232\text{ns} \quad (2)$$

### C. 284-ns Logic Delay

In order to produce the nearest value of 284 ns delay signal, the last 2 inverters are chosen from 74ALS04B while the rest of 26 inverters are maintained from 7404 chips (Fig. 4).

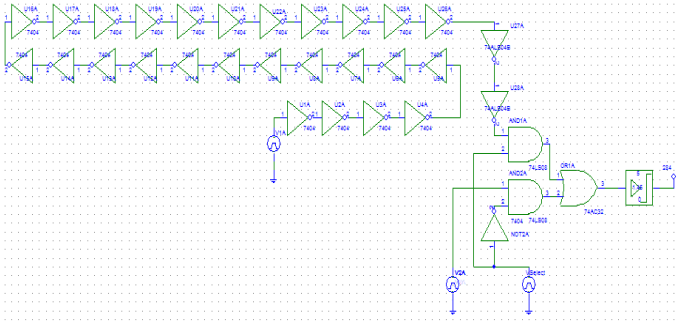

Fig. 4 Schematic for 284 ns Delay

Referring to Table II, 74ALS04B NOT gate is selected and not from either 74AC04 or 74LS04 since it can offer a suitable low propagation delay (2 ns to 11 ns). Too low or too high propagation delay of the NOT gate will make the output signal to be delayed less or more than 284 ns. Using the 5 ns – delay of 74ALS04B NOT gate, a possible calculation to produce 284 ns delay is (3).

$$[26_{7404\text{NOT}} \times 10\text{ns}] + 15\text{ns} + [2_{74\text{ALS04BNOT}} \times 5\text{ns}] = 285\text{ns} \quad (3)$$

### D. 955-ns Logic Delay

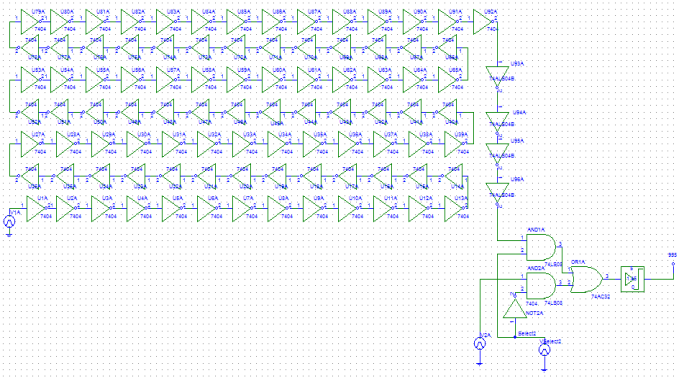

Fig. 5 Schematic for 955 ns Delay

A total of 96 7404 inverters, 92 7404 inverters and 4 74ALS04B are used to generate a 955 ns delay signal as shown in Fig. 5. However, since a total of 955 ns delay time plus 200 ns duty ratio is more than 1 us (1.155 us), the control input *VSelect2* has to be adjusted as shown in Table III. In order to have pulses from *AND1A* gate selected, the period for *VSelect2* is changed to 1.2 us and the pulse width to 1.19 us. A possible calculation to produce 955 ns delay is (4).

$$[92_{7404\text{NOT}} \times 10\text{ns}] + 15\text{ns} + [4_{74\text{ALS04BNOT}} \times 5\text{ns}] = 955\text{ns} \quad (4)$$

TABLE III ADJUSTMENT OF $V_{SELECT2}$

| ***Vpulse* / Parameters** | ***VSelect2*** |
|---|---|
| ***V1* (V)** | 0 |
| ***V2* (V)** | 5 |
| **Delay Time, $T_D$ (s)** | 0 n |
| **Rise Time, $T_R$ (s)** | 5 n |
| **Fall Time, $T_F$ (s)** | 5 n |
| **Pulse Width, $P_W$ (s)** | 1.19 u |
| **Period, $P_{ER}$ (s)** | 1.2 u |

## III. SIMULATION RESULTS

### A. 15-ns Logic Delay

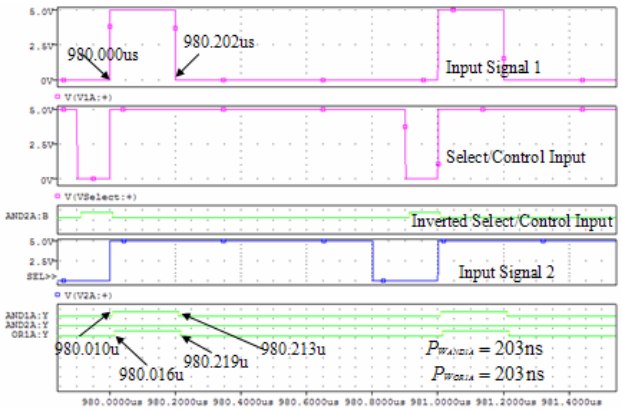


Fig. 6 Digital Simulation for 15-ns Logic Delay

From the waveform shown in Fig. 6, it is observed that *V1A* input signal produces 202 ns duty ratio. This is due to the setting of 5 ns for rise time, $T_R$ and fall time, $T_F$ parameters in *Vpulse* symbol resulting in 5 ns - time delay in the *V1A* pulses for low to high signal and 5 ns time delay for high to low signal.

In order to have *V1A* pulses chosen, the output signal from *AND2A* gate is used to produce zero output. Then the *OR1A* gate will add the outputs from *AND1A* and *AND2A* gates and subsequently produce the desired final output.

*B. 232-ns Logic Delay*

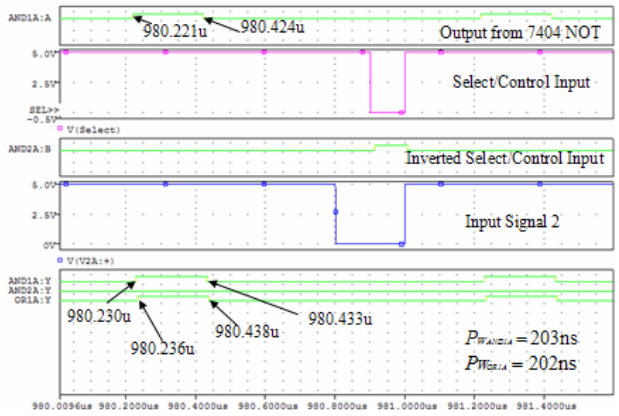


Fig. 7 Digital Simulation for 232-ns Logic Delay

From Fig. 7, the input signal from *V1A* is delayed 221 ns with 203 ns pulse width. This means that each 7404 inverter can provide practically 10 ns delay. Then the delayed signal is fed to *AND1A* gate which provides approximately 9 ns delay which yields 980.230 ns (980.230 us – 980.221 ns) while for 74AC32 *OR1A* gate, this creates an approximately 6 ns delay (980.236 us – 980.230 ns).

*C. 284-ns Logic Delay*

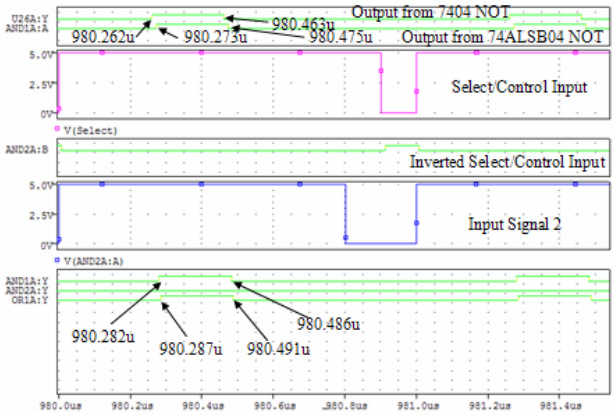


Fig. 8 a Digital Simulation for 284-ns Logic Delay

In Fig. 8, *V1A* is first delayed by 262 ns and then by 273 ns. A 7404 inverter provides approximately 10 ns delay and two 74ALS04B inverters produce 11 ns delay (980.273 us – 980.262 us) are used. The delayed signal is subsequently fed to *AND1A* gate which gives an approximately 9 ns to delay the signal to be 282 ns while 74AC32 *OR1A* gate, approximately 5 ns delay (980.287 us – 980.828 us).

*D. 955-ns Logic Delay*

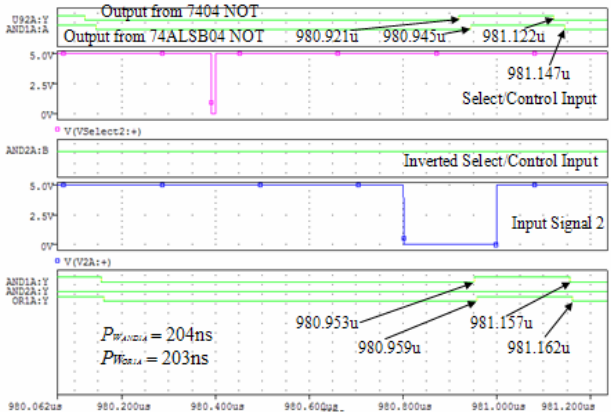


Fig. 9 Digital Simulation of 955-ns Logic Delay

From Fig. 9, the input signal from V1A is first delayed by 921 ns and then by 945 ns. This shows that each 7404 inverter can provide practically 10 ns delay and four 74ALS04B inverters produce 24 ns delay (each 74ALS04B produces 6 ns). Then the delayed signal is fed to AND1A gate which generates approximately 8 ns delay signal to 980.953 ns (980.530 us – 980.945 ns) while 74AC32 OR1A gate, approximately 6 ns delay (980.959 us – 980.953 ns).

## IV. Analysis

In generating delays using logic gates, the selection of suitable logic gates is important. In particular, the propagation delay time of logic devices are influenced by production variations and vary in accordance with temperature. Table IV shows the summary of the resulting delays produced by logic gates implemented in four logic gates as proposed.

TABLE IV SUMMARY OF DELAY

| | **Time Delay** | | | |
|---|---|---|---|---|
| | **15 ns** | **232 ns** | **284 ns** | **955 ns** |
| **74LS08 AND gate** | 10 ns | 9 ns | 9 ns | 8 ns |
| **74AC32 OR gate** | 6 ns | 6 ns | 5 ns | 6 ns |
| **7404 NOT gate** | - | 10 ns | 10 ns | 10 ns |
| **74ALS04B NOT gate** | - | - | 5.5 ns | 6 ns |

Since this is not an ideal case, the value in the simulation may be different due to repeating simulation process. This is due to the software design tolerance of ±5% . Thus, it is difficult to determine the actual delay value produced by each of the logic gates used.

Apart from selecting the appropriate logic gates and varying the numbers of inverters to produce the desired delay value, the value of select/control input, *VSelect* also plays an important role. For 955 ns time delay, the switching period is not in the range of 1 us. In order to get the required output, both pulse width and period of *VSelect* signal are adjusted to be larger than 1 us. This is where the important of multiplexer comes in this design in order to select correct

delayed signal to the output.

In this work, the required additional logic gates are simply placed at the input of multiplexer. This is due to further increase in the pulse width of the output pulses when more logic gates are added at the output of multiplexer. As a result, the logic is modified and the required additional delay gates are placed only at the input of the multiplexer to preserve the required 20 % duty cycle. Table V shows the comparison of results between the generated pulses from *Vpulse* and the proposed logic gate designs after the implementation of level shifter.

TABLE V DELAY TIME & PWM COMPARISON

| Parameter | Delay time | | | Pulse width | | |
|---|---|---|---|---|---|---|
| | ***Vpulse*** | **Logic Gate Design** | **% of error (%)** | ***Vpulse*** | **Logic Gate Design** | **% of error (%)** |
| *V1* | 15 ns | 14 ns | 6.67 | 202 ns | 204 ns | 0.99 |
| *V2* | 232 ns | 234 ns | 0.86 | 202 ns | 204 ns | |
| *V3* | 284 ns | 286 ns | 0.70 | 202 ns | 204 ns | |
| *V4* | 955 ns | 958 ns | 0.31 | 202 ns | 204 ns | |

It is observed that the percentage of errors in the delay values and the pulse widths generated by logic gate design are within 1 %. Therefore, this digital circuit design approach may be considered for the implementation in ASIC programming or IC design.

## V. CONCLUSION

The combination and addition of propagation time delay of all logic gates can be used to generate time delays. It is important to know which logic gates to be selected as each logic gate has its own specification. Other than the time delay, the duty ratio of the pulses can also be maintained to be approximately 200 ns. The digital approach has shown good results where they match with the analog simulation having comparative results of within 1% difference in delays and 0.99 % in pulse width.

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## REFERENCES

[1] J.O. Smith, Physical Audio Signal Processing, Dec 2008 Ed. Online: "http://ccrma.standford.edu/~jos/pasp/"accessed 3 May 2009.

[2] DS1110 10-Tap Silicon Delay Line Datasheet by Dallas Semiconductor

[3] SN74LS31 Delay Elements Datasheet by Texas Instruments

[4] K. Murakoshi, T. Morie, M. Nagata and A. Iwata, "An Arbitrary Chos Generator Core Circuit Using PWM/PPM Signals", Proc. of Asia and South Pacific Design Auto. Conf., pp. 23-24, 2000.

[5] K. Hayashi, T. Akiyama. A.J. Drake, "Pulse Signal Delay Circuit", United States Patent, 20 May 2003.

[6] G.D. Carpenter, A.J. Drake, F.H. Gebara, C.T. McDowell and H.C. Ngo, "Digital Duty Cycle Corrector", United States Patern, 18 May 2006.

[7] T. Otsuka and A. Wada, "Delay Circuit", United States Patern, 2 Nov. 2006.

[8] T.S. Lin, "50% Duty Cycle Clock Generator", United States Patern, 14 Oct. 2004

[9] B. J. Patella, A. Prodic, A. Zinger and D. Maksimovic, "High-Frequency Digital PWM Controller IC for DC-DC Converters", *IEEE Transaction on Power Electronics*, Vol. 18, No. 1, pp 438-445, January 2003.

[10] A. K. Reddy "Digital Delay Architecture", *United States Patent Application Publication*, 18 September 2008.

[11] V. Bocci, G. Chiodi, F. Iacoangeli, R. Nobrega, D. Pinci, W. Rinaldi "Time-multiplexing of signal using highly integrated digital delay: an FPGA implementation", *IEEE Nuclear Science Symposium Conference Record*, pp. 398-402, 2005.

[12] S. Balaji, V. B. Chandratre, M. Tewani "0.35u, 1 GHz, CMOS Timing Generator Using Array of Digital Delay Lock Loops", *21st International Conference on VLSI Design*, pp. 613-617, 2008.

[13] R. L. White "Method and Delay Circuit with Accurately Controlled Duty Cycle", *United States Patent*, 9 October 2004.