A Simple Transistors Width Adjustment Method on CMOS Transmission Gate Switch to Reduce Hold Error of S/H Circuit

Agung Setiabudi[#], Hiroki Tamura[*], Koichi Tanno[†]

[#] Department of Materials and Informatics, University of Miyazaki, 1-1 Gakuenkibanadai-nishi, Miyazaki, 889-2192, Japan
E-mail: z3t1502@student.miyazaki-u.ac.jp

[*] Department of Environmental Robotics, University of Miyazaki, 1-1 Gakuenkibanadai-nishi, Miyazaki, 889-2192, Japan
E-mail: htamura@cc.miyazaki-u.ac.jp

[†] Department of Electrical and System Engineering, University of Miyazaki, 1-1 Gakuenkibanadai-nishi, Miyazaki, 889-2192, Japan
E-mail: tanno@cc.miyazaki-u.ac.jp (Corresponding Author)

Abstract— **Sample and Hold (S/H) circuit is one of the most important circuits in analog and mixed signal integrated circuit. This circuit is the main block of many applications, such as switched capacitor circuit, analog to digital converter (ADC), etc. The majority of S/H circuits are implemented using MOS technology because the high input impedance of MOS devices performs excellent holding functions. Ideal characteristics of the S/H circuit are low hold error, low On-resistance and constant On-resistance in all voltage levels. There are some techniques to reduce the hold error and achieve low On-resistance. However, these techniques need additional compensation circuit. For this reason, a simple transistors width adjustment method on CMOS transmission gate (TG) switch to reduce hold error of S/H circuit without additional circuit that can be implemented in the actual design process is proposed in this paper. The basic idea of the proposed method is balancing hold error caused by N-type and P-type MOS transistor in CMOS switch that is used in S/H circuit. The performance of the proposed method is evaluated using HSPICE with 0.6 µm CMOS standard process. As a result, using 1.5 V constant input in the PMOS transistor width W_P range of 3 to 35 µm the average W_N/W_P ratio given by this proposed method is 0.928 with the average absolute hold error is 0.427 mV and maximum absolute hold error is 0.8 mV.**

Keywords— **sample and hold circuit; hold error; hold error reduction; CMOS switch; clock feedthrough; channel charge injection.**

I. INTRODUCTION

An analog switch is a basic building block in analog and mixed-signal integrated circuits (ICs). It is the main block of many applications such as switched capacitor circuit [1], delta-sigma modulation, analog to digital converter (ADC) [2], etc. The on/off behavior of an analog switch is controlled by the gate voltages that produce an inversion layer that acts as channel underneath the gates. The simplest circuit that uses an analog switch is sample and hold (S/H) circuit. This circuit use only one analog switch and capacitor. The majority of S/H circuits are implemented using MOS technologies because of the high input impedance of MOS devices performs excellent holding functions. The analog switch in the S/H circuit can be implemented using only one MOS transistor. However, the problem of non-uniform on-resistance, narrow analog signal swings and the existence of hold error limit its performance. To pass a wide analog signal swing and overcome the non-uniform on resistance problem, single MOSFET switch is replaced by a complementary MOS (CMOS) transmission gate (TG) Switch.

One of the most important parameter of S/H circuit performance is accuracy. However, the error voltage induces by the turning off of an MOS switch limit the accuracy of S/H circuit. This error is called hold error in S/H circuit. In general, a MOS switch is not ideal switch. A finite amount of mobile charge is stored in the channel when MOS transistor is on. When transistor turns off, the channel charge disappears through either the source/drain electrodes or substrate electrodes. Charge which disappears through source/drain is deposited on hold capacitor creating an error component to the sample voltage. This phenomenon is called channel charge injection. In a MOS transistor it is also known that it has parasitic capacitance that is formed by overlapping between gate and diffusion (source and drain). When transistor turns off, this overlap capacitance also flow the charge to hold capacitor creating another error component to sample voltage. This phenomenon is called clock feed through. These two mechanisms are the main sources that create an error in sample voltage [3].

Some research has been done and published regarding these two mechanisms. Models of strong inversion channel injection and gate-to-drain overlap capacitive coupling in

NMOS switches have been analyzed [3], [4]. The use of the continuous equation to model clock feedthrough for a single MOSFET switch has been revealed [5]. The extended analysis and measurement of channel charge injection has been studied [6]. More recently, channel charge injection model that includes weak inversion region is investigated [7]. A new Simplified model for channel charge injection, modeling in Z-domain and modeling in SIMULINK are examined [8], [9] [10]. All of these papers, however, only consider a single NMOS switch. The analysis and model of clock feedthrough in TG switch has also been studied [11]. From all of these papers, it can be obtained the analysis and model of channel charge injection and clock feedthrough in detail. However, these papers focus on analysis and model, not the techniques to reduce the hold error. Moreover, there are some techniques to reduce the hold error caused by channel charge injection and clock feedthrough. However, they need additional large compensation circuit. This paper proposed a new design method based on the analysis to reduce the hold error that can be implemented in the actual design.

II. MATERIAL AND METHOD

Sample and hold (S/H) circuit consist of two main parts, first is an analog switch and second is hold capacitor. The analog switch is used to control the connection between signal-source (input) node and data-holding (output) node, whereas the hold capacitor is used to hold the data in output node. A simple S/H circuit using a single NMOS transistor as an analog switch and a hold capacitor is shown in Fig. 1.
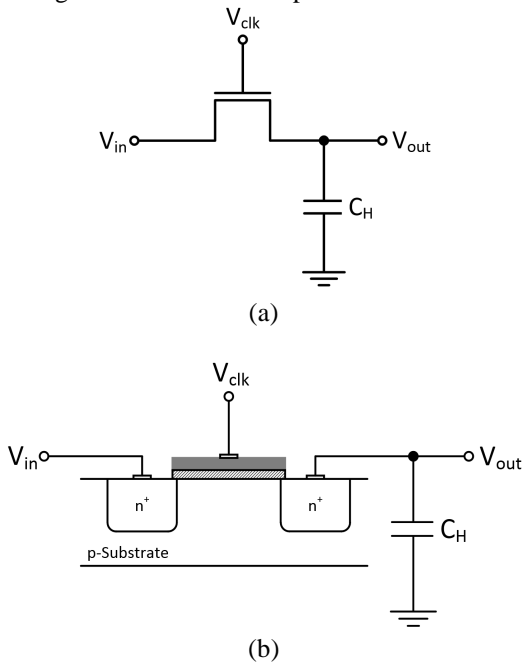

(a)

(b)

Fig. 1 S/H circuit: (a) Circuit schematic, (b) Device cross section

The operation of S/H circuit takes place in two phases: sampling and hold. When the clock voltage (V_{clk}) which is applied to the gate of the transistor is high, the transistor is on. Channel appears underneath the gate and connecting drain and source of the transistor. In this phase, the input node and output node are connected, and sampling function is performed. After the switch is turned off, the data

appearing in the holding (output) node will be held until the next operation step occurs. This phase is called hold phase. In the transition phase between sampling and hold, some physical phenomenon exists inside the transistor cause hold error in the hold phase. These phenomena are called Channel Charge Injection (CCI) and Clock Feedthrough (CFT).
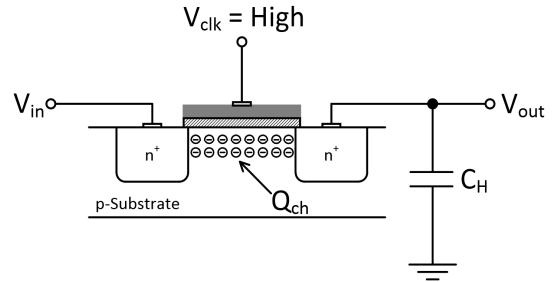
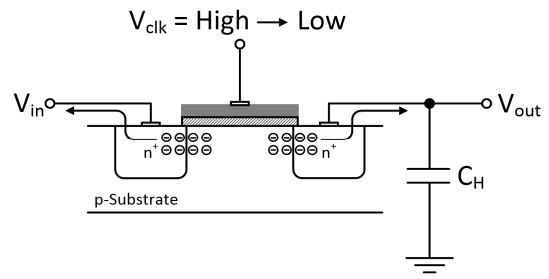

Fig. 2 Sampling phase of S/H circuit

Fig. 3 On-Off transition phase of S/H circuit

A. Channel Charge Injection

Consider the S/H circuit of Fig. 1 and suppose that the S/H circuit is in the sampling phase. In this condition, the transistor is ON and a channel exists at the oxide-silicon interface. This phase can be depicted in Fig. 2. The total charge in the inversion layer (channel) can be obtained as

$$Q_{ch} = -WLC_{ox}\left(V_{hclk} - V_{in} - V_T\right) \qquad (1)$$

Where W is channel width, L is channel length, C_{ox} is oxide capacitance per unit area, V_{hclk} is the high level of clock voltage, and V_T is the threshold voltage of the transistor. In many applications, the high level of clock voltage is equal to the supply voltage ($V_{hclk} = V_{DD}$). Thus, the equation (1) can be rewritten as (2).

$$Q_{ch} = -WLC_{ox}\left(V_{DD} - V_{in} - V_T\right) \qquad (2)$$

When the switch turns off (S/H circuit enter hold phase), Q_{ch} exits through the source and drain terminals like shown in Fig. 3, this phenomenon is called "channel charge injection". The charge injected to the left side of Fig. 3 is absorbed by the input source, creating no error. Whereas, the charge injected to the right side is deposited on C_H, creating an error in the output node. Assuming that the amount of charge which flow to the left side equal to the one which flows to the right side, it is obtained that the amount of charge causes an error in the output node is $Q_{ch}/2$. Therefore, the error voltage caused by channel charge injection then can be written as follow

$$\Delta V_{CCI} = \frac{Q_{ch}}{2C_H} \qquad (3)$$

$$\Delta V_{CCI} = \frac{-WLC_{ox}\left(V_{DD} - V_{in} - V_T\right)}{2C_H} \qquad (4)$$

B. Clock Feedthrough

MOS transistor is a device which has parasitic capacitance formed by overlapping between gate and diffusion. On the turning off process, the MOS switch couples the clock transition to the hold capacitor (C_H) through this overlap capacitance (gate-drain or gate-source overlap capacitance), as shown in Fig. 4. The coupling current that flows from gate to drain/source through overlap capacitance causes an error in the output node. The error voltage caused by clock feedthrough can be written as follow

$$\Delta V_{CFT} = -\frac{L_{ov}WC_{ox}}{L_{ov}WC_{ox} + C_H}V_{hclk} \qquad (5)$$

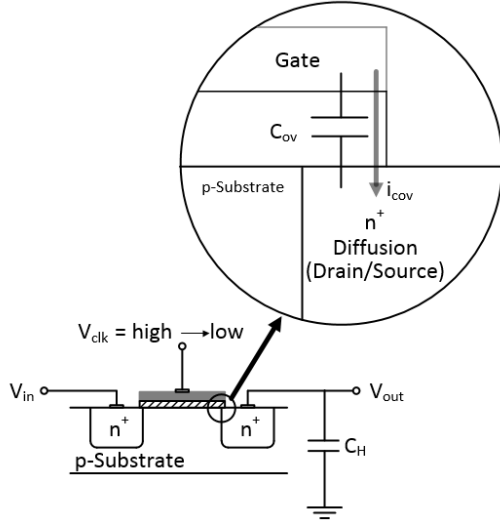Where L_{ov} is gate-drain or gate-source overlap length.

Fig. 4 Clock feedthrough

C. Basic Model of Hold Error in S/H Circuit Using CMOS Switch

Figure 5 shows schematic of basic S/H circuit using CMOS switch. The switch part of this circuit consists of two MOS transistors, N-type MOS transistor and P-type MOS transistor (complementary). By using CMOS switch in this circuit, the problem of narrow input voltage swing and non-uniform on-resistance can be solved. The input range of this switch is nearly 0V-V_{DD}, on-resistance of this switch also relatively uniform.

The total hold error of this circuit is the total error caused by channel charge injection and clock feedthrough in N-type MOS transistor and P-type MOS transistor. There are four error components in this circuit, ΔV_{CCIN} (error voltage caused by channel charge injection on N-type MOS transistor), ΔV_{CFTN} (error voltage caused by clock feedthrough on N-type MOS transistor), ΔV_{CCIP} (error voltage caused by channel charge injection on P-type MOS transistor), and ΔV_{CFTP} (error voltage caused by clock feedthrough on P-type MOS transistor). The total hold error then can be written as

$$\Delta V = \Delta V_{CCIN} + \Delta V_{CFTN} + \Delta V_{CCIP} + \Delta V_{CFTP} \qquad (6)$$

$$\Delta V_{CCIN} = -\frac{W_N L_N C_{ox}(V_{DD} - V_{in} - V_{TN})}{2C_H} \qquad (7)$$

$$\Delta V_{CFTN} = -\frac{L_{ovN}W_N C_{ox}}{L_{ovN}W_N C_{ox} + L_{ovP}W_P C_{ox} + C_H}V_{hclk} \qquad (8)$$

$$\Delta V_{CCIP} = \frac{W_P L_P C_{ox}(V_{in} - |V_{TP}|)}{2C_H} \qquad (9)$$

$$\Delta V_{CFTP} = -\frac{L_{ovP}W_P C_{ox}}{L_{ovN}W_N C_{ox} + L_{ovP}W_P C_{ox} + C_H}V_{hclk} \qquad (10)$$
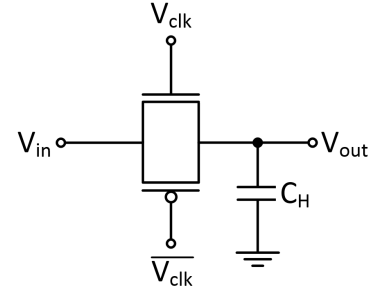

Fig. 5 S/H circuit using CMOS switch

D. Proposed Method

Some techniques have been developed by many researchers to decrease hold error voltage in S/H circuit [12-21]. Most of them use an additional circuit to decrease the hold error. Adding additional circuit means that it will increase the chip area and power consumption as well. To avoid that drawback, another approach to decrease hold error is proposed in this paper.

S/H circuit which uses CMOS as its switch has four error components as written in equations (7) - (10). These equations can be rewritten as

$$\Delta V = \frac{1}{2C_H}C_{ox}\left\{ \begin{matrix} W_P L_P (V_{in} - |V_{TP}|) \\ -W_N L_N (V_{PP} - V_{in} - V_{TN}) \end{matrix} \right\}$$
$$+ \frac{L_{ovP}W_P - L_{ovN}W_N}{L_{ovP}W_P C_{ox} - L_{ovN}W_N C_{ox} + C_H}C_{ox}V_{hclk} \qquad (11)$$

This equation consists of two types of parameter and variable. First one is device parameter and the second one is design variable. Device parameter is a value or constant which is given by technology of fabrication process regarding the intrinsic condition of the device. These parameters include C_{ox}, V_{TN}, V_{TP}, L_{ovN}, and L_{ovP}. Whereas design variable is a variable which its value can be chosen or given by designer freely or based on some constraints. These variables include V_{DD}, V_{in}, V_{hclk}, C_H, W_N, W_P, L_N, and L_P. The approach used in this research is minimizing hold error by adjusting design variable.

Theoretically, hold error produced by N-type MOS transistor and hold error produced by P-type MOS transistor in CMOS switch are in opposite sign. Therefore, the basic idea to decrease hold error in S/H circuit using CMOS switch is by adjusting design variable, so that the absolute value of hold error produced by N-type MOS transistor equal to the absolute value of hold error produced by P-type MOS transistor. If this condition can be achieved, hold error in S/H circuit will be zero.

In design variable, V_{DD}, V_{in}, V_{hclk} are determined by its application. Based on equation (11), small hold error can be achieved by setting a large value of C_H. However, a large value of C_H will cause large chip area as well. By this

condition, the possible variables which can be adjusted to decrease hold error are width and length of N-type and P-type MOS transistor. However, hold error is not the only problem in S/H circuit, the other problem is on-resistance. In design, length of the MOS transistor is usually set to the minimum value of standard process used to achieve low on-resistance. Thus, only width of N-type and P-type MOS transistor that will be adjusted to decrease hold error.

Assuming that the total overlap capacitor of N-type and P-type MOS transistor is small enough compared to hold capacitor ($W_P L_{ovP} C_{ox} + W_N L_{ovN} C_{ox} << C_H$). The error voltage caused by clock feedthrough in CMOS switch can then be written as

$$\Delta V_{CFT} = \frac{L_{ovP} W_P - L_{ovN} W_N}{L_{ovP} W_P C_{ox} - L_{ovN} W_N C_{ox} + C_H} C_{ox} V_{hclk}$$
$$\approx \frac{L_{ovP} W_P - L_{ovN} W_N}{C_H} C_{ox} V_{hclk} \quad (12)$$

Using this approximation, equation (11) can then be written in two free design variables W_N and W_P as

$$\Delta V = a W_P - b W_N \quad (13)$$

$$a = \frac{1}{2C_H} L_P C_{ox} (V_{in} - |V_{TP}|) + \frac{L_{ovP} C_{ox} V_{hclk}}{C_H} \quad (14)$$

$$b = \frac{1}{2C_H} L_N C_{ox} (V_{DD} - V_{in} - V_{TN}) + \frac{L_{ovN} C_{ox} V_{hclk}}{C_H} \quad (15)$$

From equation (13) it can be known that total hold error consists of two simple parts with a different sign, the width of P-type MOS transistor W_P with a coefficient a and width of N-type MOS transistor W_N with a coefficient $-b$. The coefficient a and b is shown in equations (14) and (15), respectively. These equations can now be used to adjust W_P and W_N properly to achieve zero hold error. By setting ΔV to zero in equation (13), it can be obtained the ratio between W_P and W_N as shown in equation (16).

$$W_N = \frac{a}{b} W_P \quad (16)$$

This ratio can be used to determine W_P and W_N in the design process to decrease hold error in S/H circuit. However, in some cases, it is difficult to get the value of a and b in equation (16) exactly because the length of overlap capacitance of N and P type MOS transistor L_{ovN} and L_{ovP} are sometimes not given directly in the model parameter of MOS transistor. L_{ovN} and L_{ovP} are the variations of the fabrication process. Therefore, it is difficult to determine the value theoretically. Without the value of L_{ovN} and L_{ovP}, it is not possible to get the ratio between W_P and W_N theoretically. To solve this problem, another approach is used to obtain the length of overlap capacitance by making a simultaneous equation use numerical values gotten from preliminary simulations. To make this approach, equation (13) is rewritten as

$$x_i L_{ovP} - y_i L_{ovN} = z_i \quad (17)$$

$$x_i = \frac{W_{Pi} C_{ox} V_{hclk}}{C_H} \quad (18)$$

$$y_i = \frac{W_{Ni} C_{ox} V_{hclk}}{C_H} \quad (19)$$

$$z_i = \Delta V_i + \frac{1}{2C_H} Cox \left\{ \begin{array}{l} W_{Ni} L_N (V_{DD} - V_{in} - V_{TN}) \\ - W_{Pi} L_P (V_{in} - |V_{TP}|) \end{array} \right\} \quad (20)$$

Equation (17) is an equation with two unknowns free variable L_{ovN} and L_{ovP}. The solution of this equation can be obtained by forming simultaneous equation from this basic equation. A simultaneous equation can be formed by doing two preliminary simulations with a different value of W_P and W_N, so that it is obtained equation (21). This equation then can be solved to get the value of L_{ovN} and L_{ovP}.

$$\begin{cases} x_1 L_{ovP} - y_1 L_{ovN} = z_1 \\ x_2 L_{ovP} - y_2 L_{ovN} = z_2 \end{cases} \quad (21)$$

Algorithm 1 Proposed method
1: **Begin**
2: Determine V_{DD}, V_{in}, V_{hclk}, and C_H;
3: C_{ox}, V_{TN}, V_{TP} ← device parameter model;
4: L_N, L_P ← minimum length of standard process;
5: ε ← Desired value;
6: W_P ← Desired value;
7: **If** L_{ovN} & L_{ovP} can be obtained from device parameter model **then**
8:      $a \leftarrow \{1/(2C_H)\} L_P C_{ox} (V_{in} - |V_{TP}|) + (L_{ovP} C_{ox} V_{hclk})/C_H$;
9:      $b \leftarrow \{1/(2C_H)\} L_N C_{ox} (V_{DD} - V_{in} - V_{TN}) + (L_{ovN} C_{ox} V_{hclk})/C_H$;
10:      $W_N \leftarrow (a/b) W_P$;
11: **else**
12:      **for** i = 1 to 2 **do**
13:          $W_{Pi} \leftarrow W_P$;
14:          $W_{Ni} \leftarrow W_{Pi} - ((i - 1)\mu m)$;
15:          Do simulation;
16:          $\Delta V_i \leftarrow$ Simulation result;
17:          **if** $(|\Delta V_i| \leq |\varepsilon|)$ **then**
18:              $W_N \leftarrow W_{Ni}$;
19:              **End**
20:          **else**
21:              $x_i \leftarrow (W_{Pi} C_{ox} V_{hclk})/C_H$;
22:              $y_i \leftarrow (W_{Ni} C_{ox} V_{hclk})/C_H$;
23:              $z_i \leftarrow \Delta V_i + \{1/(2C_H)\} C_{ox} \{W_{Ni} L_N (V_{DD} - V_{in} - V_{TN}) - W_{Pi} L_P (V_{in} - |V_{TP}|)\}$;
24:          **end**
25:      **end**
26:      $L_{ovN} \leftarrow (y_1 z_2 - y_2 z_1)/(x_2 y_1 - x_1 y_2)$;
27:      $L_{ovP} \leftarrow (x_1 z_2 - x_2 z_1)/(x_2 y_1 - x_1 y_2)$;
28:      $a \leftarrow \{1/(2C_H)\} L_P C_{ox} (V_{in} - |V_{TP}|) + (L_{ovP} C_{ox} V_{hclk})/C_H$;
29:      $b \leftarrow \{1/(2C_H)\} L_N C_{ox} (V_{DD} - V_{in} - V_{TN}) + (L_{ovN} C_{ox} V_{hclk})/C_H$;
30:      $W_N \leftarrow (a/b) W_P$;
31:      **if** $(\Delta V_2 < 0)$ **and** $(W_{N2} < W_N)$ **then**
32:          $W_N \leftarrow W_{N2}$;
33:      **end**
34: **end**
35: **End**

This complete proposed method is shown in Algorithm 1. This algorithm is made to make the proposed method more procedural and more comfortable to be implemented in the actual design process. The first step in this method is determining all design variables based on the application and getting device parameter from device parameter model. After that, to get low on-resistance of the switch, lengths of the transistors are set to minimum value. In this method, variable epsilon (ε) is introduced as a small error which is tolerated in preliminary simulations. After determining ε, W_P is set to the desired value that designer wants to use. The consideration that is usually used to choose the width of the transistor is on-resistance, the wider transistor the lower on-resistance. If the lengths of overlap capacitances can be obtained directly from the model parameter of CMOS transistor, then W_N can be calculated directly by using equation (16). But if the lengths of overlap capacitances cannot be obtained directly then the next step is doing two preliminary simulations to form equation (21) and get L_{ovN} and L_{ovP}. However, if the hold error produced in these preliminary simulations is less than or equal to ε, then the final W_N is W_N that is used in the preliminary simulation and process is finished. If hold error in preliminary simulations is larger than ε then W_N is calculated using equation (16). To ensure that the final hold error produced by equation (16) is less than hold error produced by preliminary simulations, selection condition at line 29 in algorithm 1 is applied.

III. RESULTS AND DISCUSSION

In this section, the steps in algorithm 1 are done to obtain the width of N-type and P-type MOS transistor (W_N and W_P). The value of design variables and device parameters used in this algorithm are shown in Table 1. Device parameter shown in Table 1 are taken from 0.6 µm standard CMOS process model parameter and preliminary simulations are done using HSPICE with this model parameter.

TABLE I
THE VALUE OF VARIABLES AND PARAMETERS OF N AND P TYPE MOS TRANSISTOR

Variable/Parameter	Value
V_{DD}	3 V
V_{in}	1.5 V
V_{hclk}	3 V
f_{clk}	1 MHz
C_H	1 pF
C_{ox}	2.60373×10^{-3} F/m^2
V_{TN}	0.734587 V
V_{TP}	-0.876414 V
L_N, L_P	0.6 µm
W_P	5 µm

The value of L_{ovN}, L_{ovP}, and W_N obtained from this algorithm are 0.09895 µm, 0.10300 µm, and 4.70248 µm, respectively. The performance of this proposed method is then re-evaluated using HSPICE. The simulation will show the hold error produced by S/H circuit which uses W_N and W_P produced by previous steps. The result of this simulation indicates that the hold error produced by S/H circuit which

its W_N/W_P ratio is 4.70/5 is 0.3 mV (0.02% from input voltage).

Figure 6 shows the simulation result of 0.2 V peak-to-peak amplitude sinusoidal input with the frequency of 100 kHz. In this simulation, the same W_N and W_P are used (4.70/5). From the figure, it can be known that the hold error is minimal, 0.6 mV in 1.6 V input voltage and -1.1 mV in 1.4 V input voltage. Furthermore, this proposed method is evaluated in the various width of the transistor. Using constant input of 1.5 V, this proposed method is simulated from 3 to 35 µm. Hold error produced by this simulation is shown in Fig 6. From Fig. 7 it can be known that the absolute value of hold errors produced by this proposed method in the range of 3 to 35 µm are less than 0.8 mV, with the minimum error is 0 V and maximum error is 0.8 mV. In the range of 3 to 35 µm, the average W_N/W_P ratio given by this proposed method is 0.928 with the average hold error is 0.427 mV.
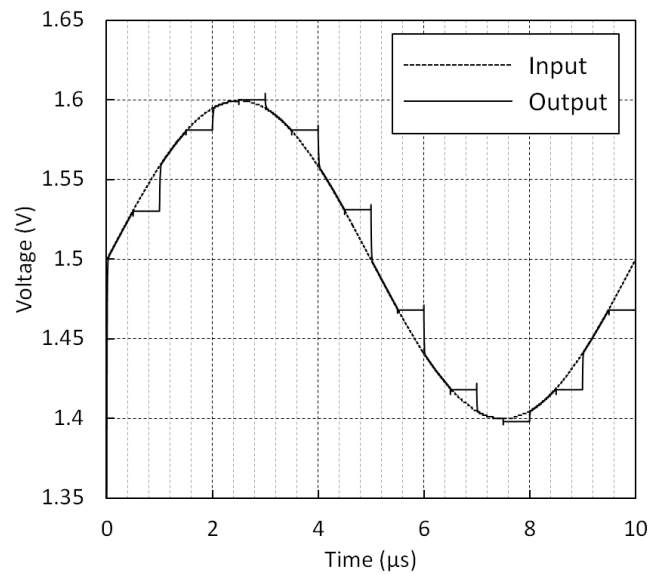

Fig. 6 Simulation result of 0.2 V peak-to-peak amplitude sinusoidal input with the frequency of 100 kHz
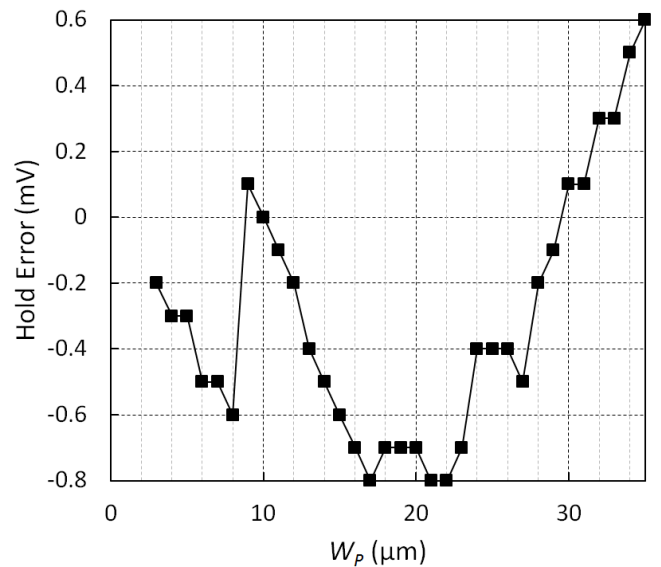

Fig. 7 Hold error produced by a proposed method in the various transistor widths

IV. Conclusion

In this paper, a new method to decrease the hold error in S/H circuit is proposed. Basic notion of the proposed method is to adjust design variable, in this case the width of N-type and P-type MOS transistor in CMOS switch (W_N and W_P) so that the absolute value of hold error caused by N-type MOS transistor equal to the absolute value of hold error caused by P-type MOS transistor. To construct this proposed method, some analyses an underlying mathematical model of hold error of S/H circuit is done. From the result of the analysis, an algorithm of this proposed method is made to make it more procedural and more comfortable to be implemented in the actual design condition.

The proposed method performance is evaluated using HSPICE with 0.6 µm CMOS standard process. As a result, using 1.5 V constant input in the W_P range of 3 to 35 µm the average W_N/W_P ratio given by this proposed method is 0.928 with the average absolute hold error is 0.427 mV and maximum absolute hold error is 0.8 mV. The proposed method is the simulated using 0.2 V peak-to-peak amplitude sinusoidal input with the frequency of 100 kHz and 4.70/5 W_N/W_P ratio. As a result, the hold error is 0.6 mV in 1.6 V input voltage and -1.1 mV in 1.4 V input voltage.

Future work of this research is to develop this proposed method using more detail mathematical model of channel charge injection and clock feedthrough and evaluate that new proposed method through HSPICE simulation and measurement of fabricated transistors.

References

[1] Y. Fan, Y. Huijing and L. Gang, *"A 4th-order Switch-capacitor Low-pass Filter for Quartz Gyroscope Interface Circuit,"* TELKOMNIKA, Vol. 11, No. 10, pp. 5718-5724, 2013.

[2] Y. Fan, Y. Huijing and L. Gang, *"A High-Performance Sigma-Delta ADC for Audio Decoder Chip,"* TELKOMNIKA, Vol. 11, No. 11, pp. 6570-6576, 2013.

[3] B.J. Sheu, J.H. Shieh, and M. Patil, *"Modeling charge injection in MOS analog switches,"* IEEE Transactions on Circuits and Systems, vol. CAS-34, no. 2, pp. 214-216, 1987.

[4] B.J. Sheu and C. Hu, *"Switch-induced error voltage on a switched capacitor,"* IEEE Journal of Solid-State circuits, vol. SC-19, no. 4, pp. 519-525, 1984.

[5] G. Wegmann and E. Vittoz, and F. Rahali, *"Charge injection in analog MOS switches,"* IEEE Journal of Solid-State Circuits, vol. SC-22, no. 6, pp. 1091-1097, 1987.

[6] J.H. Shieh, M. Patil, and B J. Sheu, *"Measurement and analysis of charge injection in MOS analog switches,"* IEEE J. Solid-State Circuits, vol. SC-22, no. 2, pp. 277-281, Apr. 1987.

[7] Y.B. Gu and M.J. Chen, *"A new quantitative model for weak inversion charge injection in MOSFET analog switches,"* IEEE Transactions on Electron Devices, vol. 43, no. 2, pp. 295-301, 1996.

[8] A. Danchiv, M. Bodea, *"A New Simplified Model for Charge Injection Induced Sample and Hold Error,"* 15th IEEE Mediterranean Electrotechnical Conference MELECON 2010, pp.743-748. 2010.

[9] P. Torkzadeh and M. Atarodi, *"Channel Charge Injection analysis and its modeling in z-domain for switched-capacitor integrators,"* 2009 52nd IEEE International Midwest Symposium on Circuits and Systems, Cancun, pp. 126-129, 2009.

[10] P. Torkzadeh, M. Atoradi, *"Behavioral Modeling of Clock Feed-Through and Channel Charge Injection NonIdeal Effects in SIMULINK for Switched-Capacitor Integrator,"* Elsevier Simulation Modelling Practice and Theory 18, pp.483-499, 2009.

[11] W. Xu, G. Friedman, "Clock Feedthrough in CMOS Analog Transmission Gate Switches," Springer Analog Integrated Circuits and Signal Processing, 44, 271-281, 2005.

[12] B. Razavi, *"Design of analog CMOS integrated circuits,"* McGraw-Hill, 2001.

[13] R. C. Yen, P. R. Gray, *"A MOS switched-capacitor instrumentation amplifier,"* IEEE Journal of Solid-State Circuits, 17 (6), pp. 1008–1013, 1982.

[14] A. Abolhasani, M. Tohidi, K. Hadidi, A. Khoei, *"A new high-speed, high-resolution open-loop CMOS sample and hold,"* Analog Integrated Circuits and Signal Processing, 78 (2), pp. 409–419, 2014.

[15] T. Moradi Khanshan, M. Nematzade, K. Hadidi, A. Khoei, Z. D. Koozehkanani, J. Sobhi, *"Very linear open-loop CMOS sample-and-hold structure for high precision and high-speed ADCs,"* Analog Integrated Circuits and Signal Processing, 88 (1), pp. 23–30, 2016.

[16] M. Mousazadeh, *"A highly linear open-loop high-speed CMOS sample and hold,"* Analog Integrated Circuits and Signal Processing, 90 (3), pp. 703–710, 2017.

[17] T. Nonthaputha, M. Kumngern, S. Lerkvaranyu, *"CMOS sample-and-hold circuit using current conveyor analog switch,"* in 2016 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp. 1–4, 2016.

[18] L. Mountrichas, S. Siskos, *"A high-speed offset canceling distributed sample-and-hold architecture for flash A/D converters,"* Microelectronics Journal, 44 (12), pp. 1123-1131, 2013.

[19] K. Ding, K. Cai, Y. Han, "Design of a high-speed sample-and-hold circuit using a substrate-biasing-effect attenuated T switch," Microelectronics Journal, 41 (12), pp. 809–814, 2010

[20] P. Pouya, A. Ghasemi, H. Aminzadeh, *"A low-voltage high-speed high linearity MOSFET-only analog bootstrapped switch for sample-and-hold circuits,"* in 2015 2nd International Conference on Knowledge-Based Engineering and Innovation (KBEI), pp. 418–421, 2015.

[21] T. B. Nazzal, S. A. Mahmoud, "Low-power bootstrapped sample and hold circuit for analog-to-digital converters, in: 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1–4, 2016.