Better luminescent properties were observed on the films with the standard powder $ZnGa_2O_4$ x-ray diffraction pattern. Also, the substarte temperature above 500°C leads to the films with the standard powder $ZnGa_2O_4$ x-ray diffraction pattern. The effect of the strength of the ligand field on the resulting energy levels, labeled by their spectroscopic terms $^4A_2$, $^4T_1$, $^4T_2$, and ^2E. The main transition between the excited state ($^4T_2$) and luminescent center ($^4A_2$) is 2.64 eV of blue light emission (470 nm).

Uniform $ZnGa_2O_4$ phosphor films deposited by magnetron sputtering at proper pressure and power are obtained. Good luminescent characteristics of low voltage cathodoluminescence phosphor films are observed in this research.

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Numerical Calculations of the Electrical Effects Induced by Structural Imperfections on MOS Capacitors

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ABSTRACT

As the thickness of gate quality SiO_2 is reduced, minor structural interface imperfections begin to play an important role in device performance and yield. To isolate the effects of a variety of such interface imperfections on electric field distribution within the SiO_2 layer of biased metal oxide semiconductor capacitors, numerical calculations were carried out. The results indicate that strong electric field distortions may be expected for almost any interfacial defect configuration, being highest for metal precipitates. Technological consequences of the findings are also discussed.

The study of the high-field breakdown of thin SiO_2 layers has become an important issue because, due to the downscaling of the geometry of microelectronics devices, without the appropriate scaling of the supply voltages, the devices are submitted to higher electric fields which enhance the probability of charge injection into the gate oxide thus leading to the possibility of accelerated degradation of the SiO_2 layer and of the Si-SiO_2 interface.

On actual metal/oxide/semiconductor (MOS) devices the gate oxide thickness may vary, say, between 5 and 20 nm. For such kinds of devices, the degree of uniformity and homogeneity of the SiO_2 bulk properties as well as those of the interfaces MOS is important for the adequate performance of the device. SiO_2 bulk defects play a fundamental role on the final performance and yield of modern devices. They have been extensively investigated,[1-7] and it was demonstrated that they can be effectively suppressed if appropriate precautions are taken. In that case the interface or surface properties (roughness and surface defects) become of an increasing importance as far as high-field breakdown is concerned,[8,9] demanding, therefore, increased attention.

With regard to this latter point, it is of interest to note the difficulty in assessing the electrical effect of the presence of a single defect on device characteristics. For example, microscopic defects such as microasperities are quite easily detected by atomic force microscopy (AFM), and there exists even a correlation between the presence of a collectivity of such asperities (numerically quantified as roughness) and device characteristics.[10] But there is still a lack of a well-established correlation between a single, nanometer-sized, defective spot and the effect(s) it causes on device performance. Numerical calculations, however, constitute an exciting tool for approaching that problem because they allow one to isolate and to investigate the effect of a single defect on the performance of simple devices. Because numerical calculations usually allow one to carry out a two-dimensional analysis, the geometrical effect of the single defect can be investigated.

Using that latter approach, in a recent publication it was found that a single structural defect, 2×2 nm^2 sized, located at the Si/SiO_2 interface of an MOS capacitor biased into accumulation, is sufficient to strongly affect the spatial distribution of the electric field within the oxide, yielding extremely high local electric field values,[11] even higher than the claimed "intrinsic" (but macroscopic) breakdown field (13.2 MV/cm) obtained experimentally with the aid of MOS capacitor breakdown tests of 20 nm thick gate quality SiO_2.[12] The apparent contradiction may be solved if one remembers that the experimentally obtained "intrinsic" breakdown field is a macroscopic-collective quantity whereas numerical calculations allow one to obtain a microscopic-local quantity.

In order to continue with this former study, numerical calculations of defective MOS capacitors, biased into accumulation at high electric fields, were again carried out in this work. However, in contrast to that former work, the defective spot, positioned at the interfaces as shown in Fig. 1, is now assumed to be made of different materials. This was done in order to establish the most detrimental defect configuration (position and material the defect is made of), this is to say, the configuration which produces the largest local electric field enhancement in the capacitor.

The Simulated MOS Geometry

The operation of a bidimensional Al-gated MOS capacitor, prepared on an either p- or n-type silicon substrate was simulated using the PISCES program.[13] The doping level of the 100 mm thick substrate was fixed at 10^{15} cm^{-3}, the gate size at 1 mm, and the SiO_2 thickness at 20 nm. At either the Al/SiO_2 or the Si/SiO_2 interface a 1×1 nm^2 asperity (defect) was introduced. The dielectric constant (ϵ) and bandgap (E_g) of the material making the asperity were fixed at such values as to represent Al_2O_3, SiO_x (including SiO_2) or a metallic precipitate. According to its geometry, this asperity was classified positive or negative (here, respectively, defined as positive or negative roughness), corresponding to a local thinning or increase of the oxide thickness (d_{ox}). In addition, the simulated structure was assumed to be back-side contacted with Al.

The final structure is schematically shown in Fig. 1. For numerical calculation purposes, 1700 nodes were preferentially distributed over the regions of highest potential gradients *i.e.*, at the interfaces and over the asperity/defect.

For simulation purposes, this structure was biased at 24 V and always into accumulation in order to have the electric field essentially falling within the oxide. The value of 24 V was chosen because it results in an electric field of about 12 MV/cm across the oxide, a value which is lower than that reported to cause "intrinsic" breakdown (13.2 MV/cm) but close enough to it so that one can conveniently compare the inhomogeneities of the electric field,

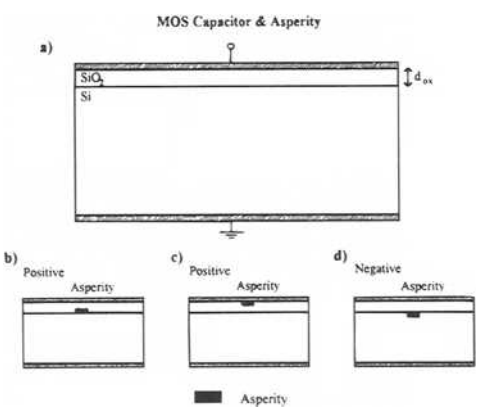

Fig. 1. Schematic drawing of the simulated MOS capacitor showing the negative and positive asperities considered throughout this work.

Table I. List of the various values of which the parameters characterizing the asperity material are made.

Material/parameters	Dielectric constant ($\times \epsilon_o$)	Energy gap (eV)
Al_2O_3	9	9
SiO_x	3.5 to 4.5	8.5 to 9.5
Metal	900	0.05
Si or SiO_2	11.7 or 3.9	1.1 or 9

caused by the asperity, to that of the "intrinsic" breakdown value.

The various possible configurations of the asperity used during this work are shown in Fig. 1 whereas the various possible values of the dielectric constant (ϵ) and bandgap (E_g) of that asperity, representing therefore the different kinds of material defects, are summarized in Table I.

The analysis of the calculated electric field distribution was carried out in two ways: (*i*) a line plot along the four lines defined in Fig. 2 (cuts a, b, c, and d), and (*ii*) a plot of the spatial distribution of the electric field vectors, close to the region of the asperity (an example is given in Fig. 3b).

Concerning the validity of this approach used throughout this work, we recall Ref. 14 and 15 which discuss the application of the Maxwell equations on microscopic media, this is to say, on the polarizability of molecules (or equivalently, the stressing of chemical bonds) of an amorphous material. The stressing of the bond above a critical value will result in breakdown of the dielectric: in that case the local electric field acting on the bond is so high that it removes the electron making up the bond.

The electric field which will polarize the molecule is the result of the externally applied field plus the electric field which the medium will build up by means of polarization of all the molecules except that one under consideration. With these considerations we always have a continuous distribution of the local electric field. This justifies the use of the present continuum approach to evaluate electric field variations on a nanometer scale.

For a complete and rigorous analysis, considerations of quantum-mechanical nature should be taken into account, too. However, for simple cases such as ours, which considers an isotropic and homogeneous material (silicon dioxide), the classical approach is satisfactory.[15]

Results

Al_2O_3 asperity (Fig. 1c).—The simulation of the MOS structure containing the Al_2O_3 asperity was performed having in mind the formation of this oxide[16] during the sintering process usually carried out to improve back-side contacting and Si/SiO_2 interface states density annealing.

Figure 3a shows that the electric field inside the Al_2O_3 asperity (4 MV/cm) is much lower than that found within the bulk SiO_2 (11.5 MV/cm). It also shows that the electric field within the SiO_2 but very close to the asperity reaches very high values (16.5 MV/cm), much higher than the reported intrinsic breakdown field of SiO_2 (13.2 MV/cm).

Figure 3b shows that the electric field becomes visibly distorted at a distance of approximately 7 nm from Al_2O_3

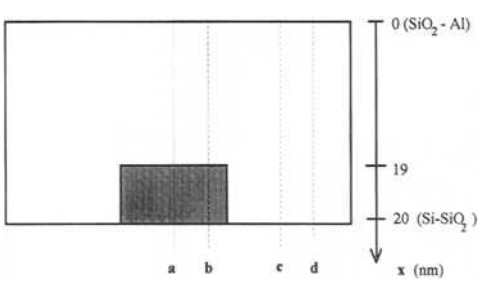

Fig. 2. Four lines, a, b, c, and d, along which the electric field intensity was analyzed: a, center of the asperity; b, still within the asperity, but close to its border; c, outside the asperity; d, far away from the asperity; *x* is the distance counted from the Al/SiO_2 interface.

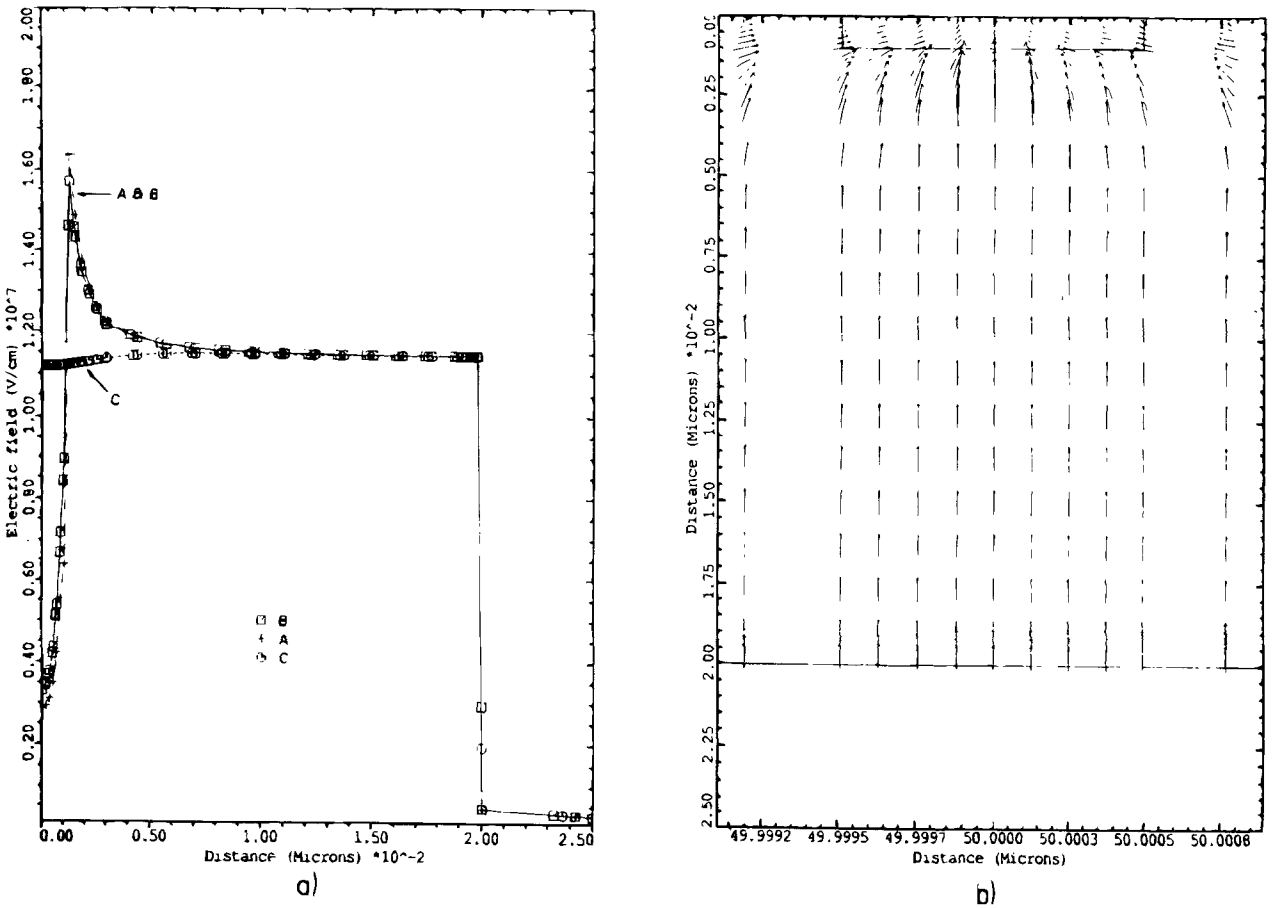

Fig. 3. (a and b) show the distribution of the electric field intensity along the lines a, b, and c, defined in Fig. 2 as well as the spatial distribution of the electric field vectors in the vicinity of the Al_2O_3 asperity.

the asperity. Note that the lengths of the vectors in this kind of figure are proportional to the absolute values of the electric fields.

Metal precipitate.—During the normal processing steps needed for device fabrication, contamination, notably by metals, may occur. Their presence may be a result of inadequate wafer handling (with metal tweezers, for example) as well as the result of the use of nonultrapure chemicals, just to mention a few examples. As a result, mobile ions may be found in gate oxides and metal precipitates at surfaces and interfaces.

In order to make the asperity exhibit a metallic character, this is to say, play the role of a metal precipitate, the bandgap (E_g) and dielectric constant of that asperity were given the values of 0.05 eV and 900 ϵ_o, respectively (see Table I).

Positive asperity (Fig. 1b).—Figure 4 shows that for this kind of asperity the maximum electric field reaches 21 MV/cm, at approximately x = 19 nm, along cut a) (defined in Fig. 2). For larger values of x but still smaller than 20 nm (*i.e.*, inside the precipitate), the electric field assumes insignificant values. Outside the precipitate (cut c, 5 nm distant from the precipitate) the field is slightly reduced to values lower than those found in the bulk SiO_2 (11.8 MV/cm).

The spatial distribution of the electric field vector (Fig. 4b) shows that on the laterals of the precipitate the field is that much distorted as to make an angle of 90° with respect to that of the unperturbed field within the bulk SiO_2. Inside the precipitate, the electric field vanishes as expected for a conducting material. The substrate was assumed to be p-type.

Negative asperity (Fig. 1d).—For this type of asperity the field reaches a maximum of 12.6 MV/cm at approximately 20 nm whereas the value of the unperturbed field was 12.4 MV/cm. Inside the precipitate, the field vanishes again, as expected. Within the silicon, close to the precipitate, the electric field reaches 2.5 MV/cm thus leading to the possibility of electric breakdown of the silicon substrate (0.3 MV/cm). Outside the precipitate, but within the SiO_2, the field is practically undisturbed.

The spatial distribution of the electric field vector, shown in Fig. 5b, exhibits a strong perturbation which is maximum close to the borders of the precipitate. The existence of significantly strong fields inside the silicon substrate can again be observed. The substrate was n-type for this simulation.

SiO_x precipitate (Fig. 1b and d).—In this case, the electric field within the positive asperity as well as in its vicinity remained unchanged with respect to its value within the bulk SiO_2. For the case of a negative asperity, the field distortion was equivalent to that found for a (negative) SiO_2 asperity, to be commented on in the next section.

This latter result is an evidence that SiO_x precipitates, typically found in CZ-grown silicon, probably do not directly induce any electric field enhancement in its vicinities. They may, however, act as gettering centers for metals, acting in that case probably more like the metallic precipitate already discussed above.

Single Si/SiO_2 interface asperity.—This kind of asperity is a purely geometric one (no material other than Si or SiO_2 is involved). It may be induced by the oxidation process itself, which roughens the Si/SiO_2 interface[17,18] or may be the result of well-developed SiO_2 precipitates existing in the bulk Si and which become attached[19-21] to the evolving Si/SiO_2 interface during an oxidation process.

Positive asperity: Si protrusion into SiO_2 (Fig. 1b).—Figure 6a shows that a maximum field intensity of 16.5 MV/cm is reached at x = 19 nm, along cut a. Outside of the asperity, for values of x lower than 20 nm, the electric field was lower than the nondisturbed field within the bulk SiO_2,

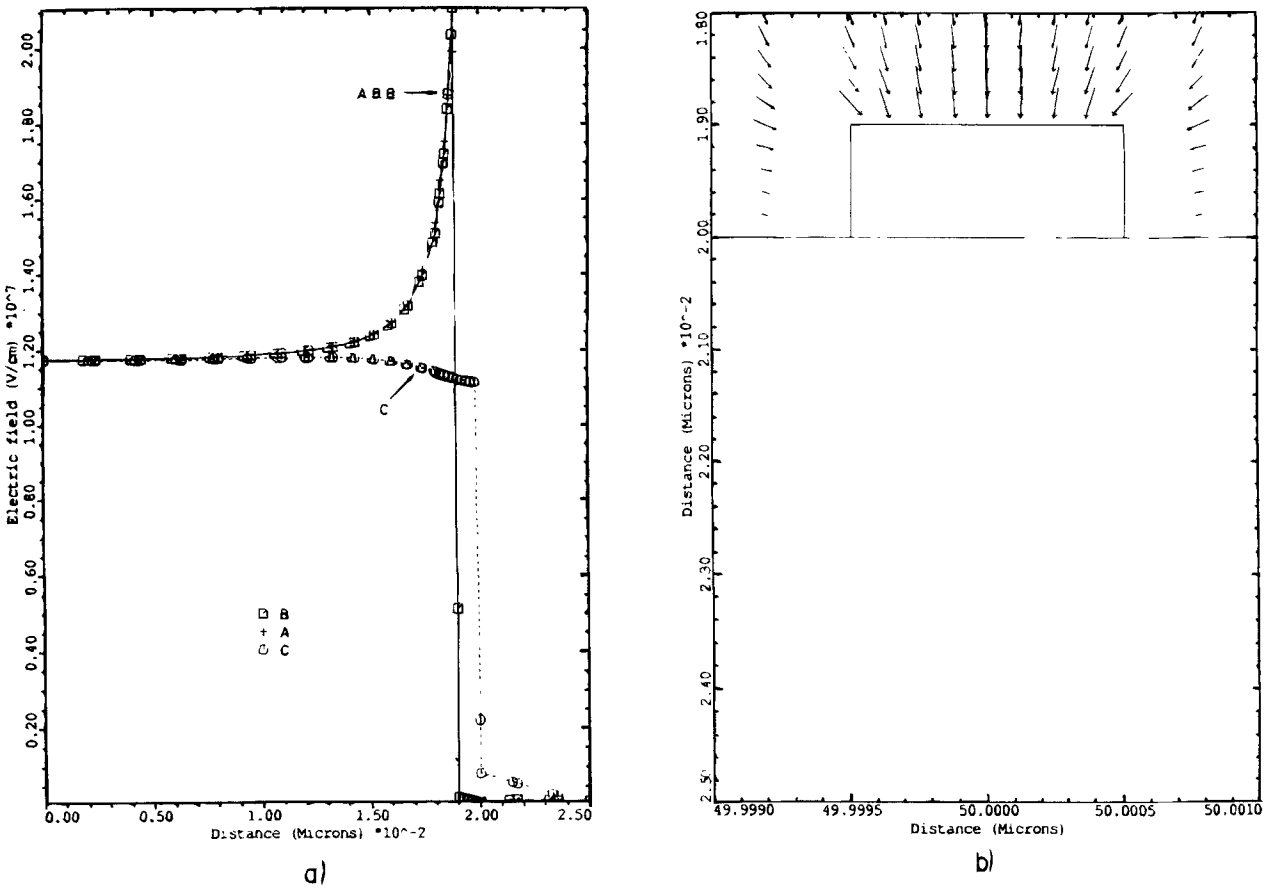

Fig. 4. (a and b) show the distribution of the electric field intensity along the lines a, b, and c defined in Fig. 2 as well as the spatial distribution of the electric field vectors in the vicinity of the positive asperity with metallic character.

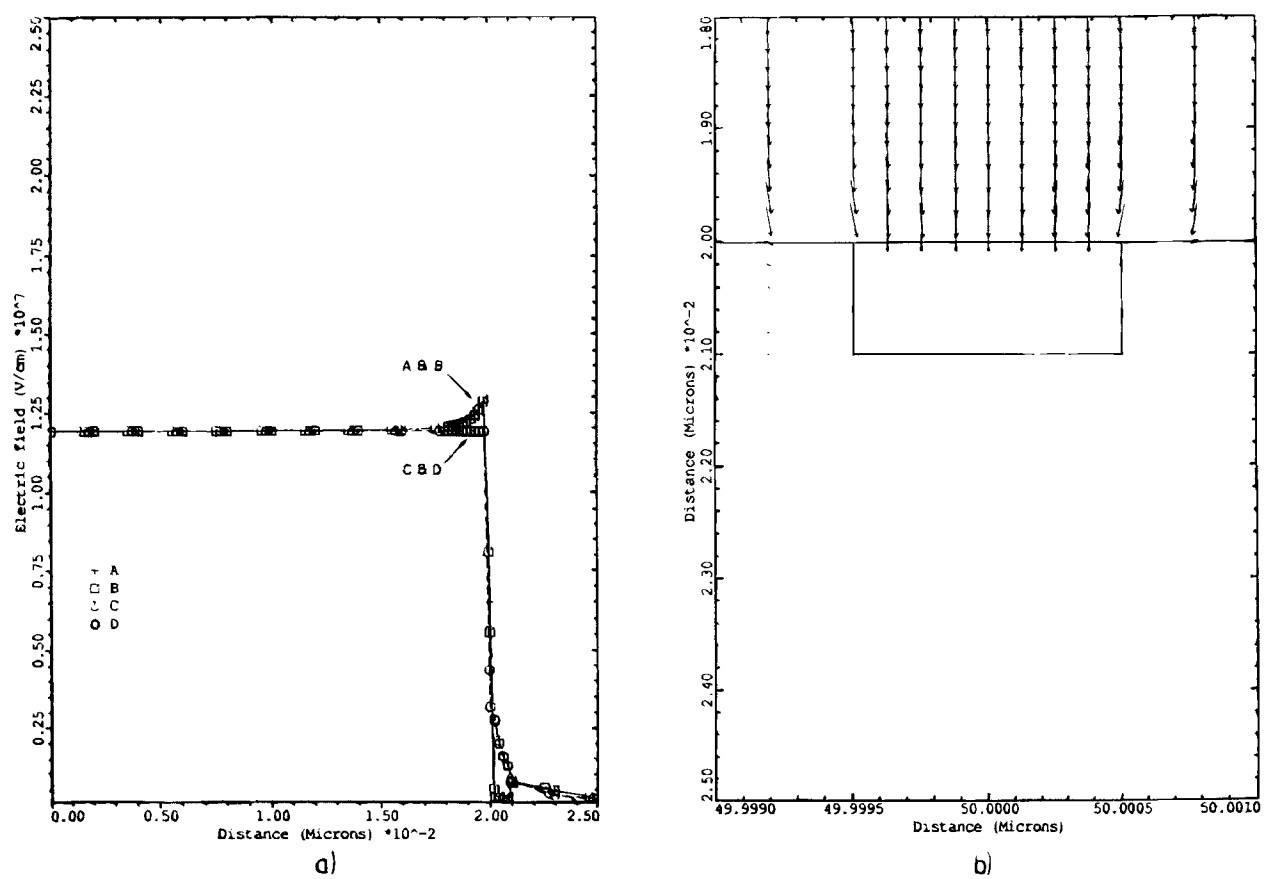

Fig. 5. (a and b) show the distribution of the electric field intensity along the lines a, b, and c defined in Fig. 2 as well as the spatial distribution of the electric field vectors in the vicinity of the negative asperity with metallic character.

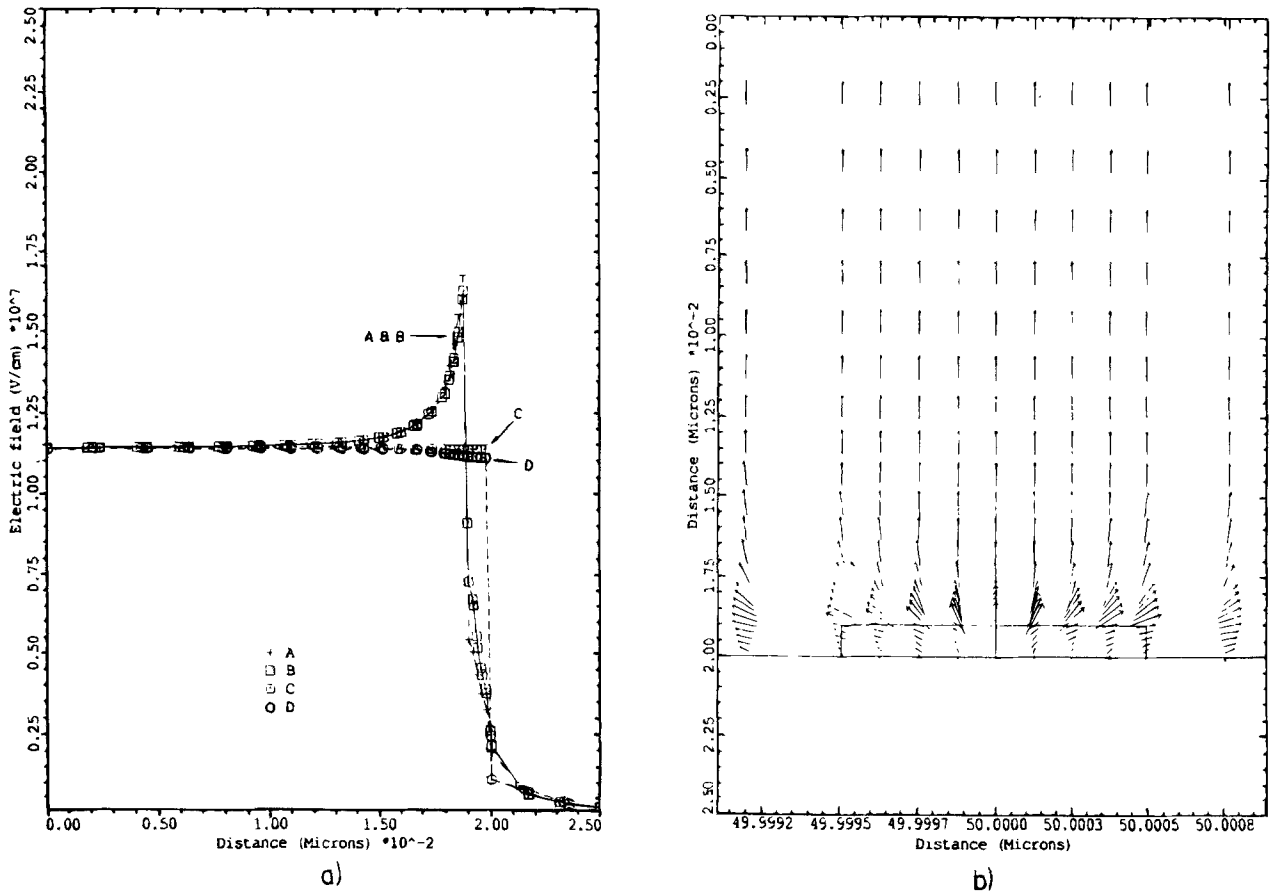

Fig. 6. (a and b) show the distribution of the electric field intensity along the lines a, b, and c defined in Fig. 2 as well as the spatial distribution of the electric field vectors in the vicinity of the positive Si asperity.

which was 11.3 MV/cm. The substrate was assumed to be p-type. The electric field distribution, shown in Fig. 6b, exhibits strong distortions close to the border of the asperity. It can easily be seen that within the silicon asperity the electric field is not neglectable, being lower but still of the same order of magnitude as that found in the bulk SiO_2.

Negative asperity: SiO_2 protrusion into the Si substrate (Fig. 1d).—This is the case where the oxide thickness is locally larger than the average value d_{ox} so that a local reduction of the electric field may be expected. In Fig. 7a the electric field within the protrusion as well as in its vicinities behave as expected: along cuts a and b, which pass both across the protrusion, the electric field starts becoming lower at x = 19 nm. On the other hand, the field along cut c, which passes outside the protrusion, reaches a value of 2.5 MV/cm within the Si.

The spatial distribution of the electric field (Fig. 7b) shows the field distortion to be highest close to the laterals of the protrusion. The electric field within the silicon is quite high, being comparable to that of the SiO_2. The substrate was assumed to be n-type.

Positive Si asperity and a positive charge of 10^{15} cm^{-2} (Fig. 1b).—The value of the effective oxide charge Q^+ usually found in Si/SiO_2 systems is of the order of 10^{10} cm^{-2}. This value represents a macroscopic measure. However, on a nanometric scale the spatial distribution of such positive charges may not be homogeneous. Having this in mind, MOS capacitors containing positive Si asperities with positive Si/SiO_2 charges Q^+ of various values were simulated. Figure 8a shows the result for an extreme case: Q^+ = 10^{15} cm^{-2}. It is seen that an electric field of up to 90 MV/cm may concentrate at the Si/SiO_2 interface, a value which by far exceeds the intrinsic breakdown field value of SiO_2. It is also observed that the distortion of the electric field is extremely localized, covering an area (around the asperity) of approximately 15 nm in diameter.

The spatial distribution of the electric field vector, in the vicinities of the asperity, is strongly distorted yielding extremely high field gradients (Fig. 8b).

Summary of the results.—The results concerning the electric field intensity dependence on the particular defect configuration simulated, are summarized in Table II. It is again important to state that for all the calculations carried out the size, *i.e.*, the geometry of the asperity, was kept constant (1 × 1 nm^2). Only the parameters ϵ, E_g, and Q^+ and the relative position of the asperity with regard to the Si/SiO_2 or Al/SiO_2 interfaces were changed.

From this table it is seen that for the particular asperity size used throughout this work it is the metallic precipitate that most strongly perturbs the electric field close to the asperity.

The foregoing findings may be summarized as follows:

1. The perturbation of the electric field due to the presence of a 1 × 1 nm^2 asperity is limited to its vicinity (~10 nm radius).
2. Although not explicitly shown, for the particular geometry of the asperity used throughout this work, positive charges Q^+ at the Si/SiO_2 interface do not affect the local field unless its value surpasses ~10^{13} cm^{-2}.
3. The larger the ϵ_p/ϵ_{ox} ratio, the larger the electric field within the SiO_2, but close to the asperity. This effect will occur independently of the presence of the asperity. But it will be enhanced in case the asperity is present because of its geometrical effect.
4. The maximum of the electric field resides within the SiO_2, in the region immediately above the asperity. It may reach values up to one order of magnitude higher than those obtained by simply dividing the externally applied voltage by the nominal oxide thickness.

Discussion

From a technological viewpoint these results just presented let one draw some interesting considerations.

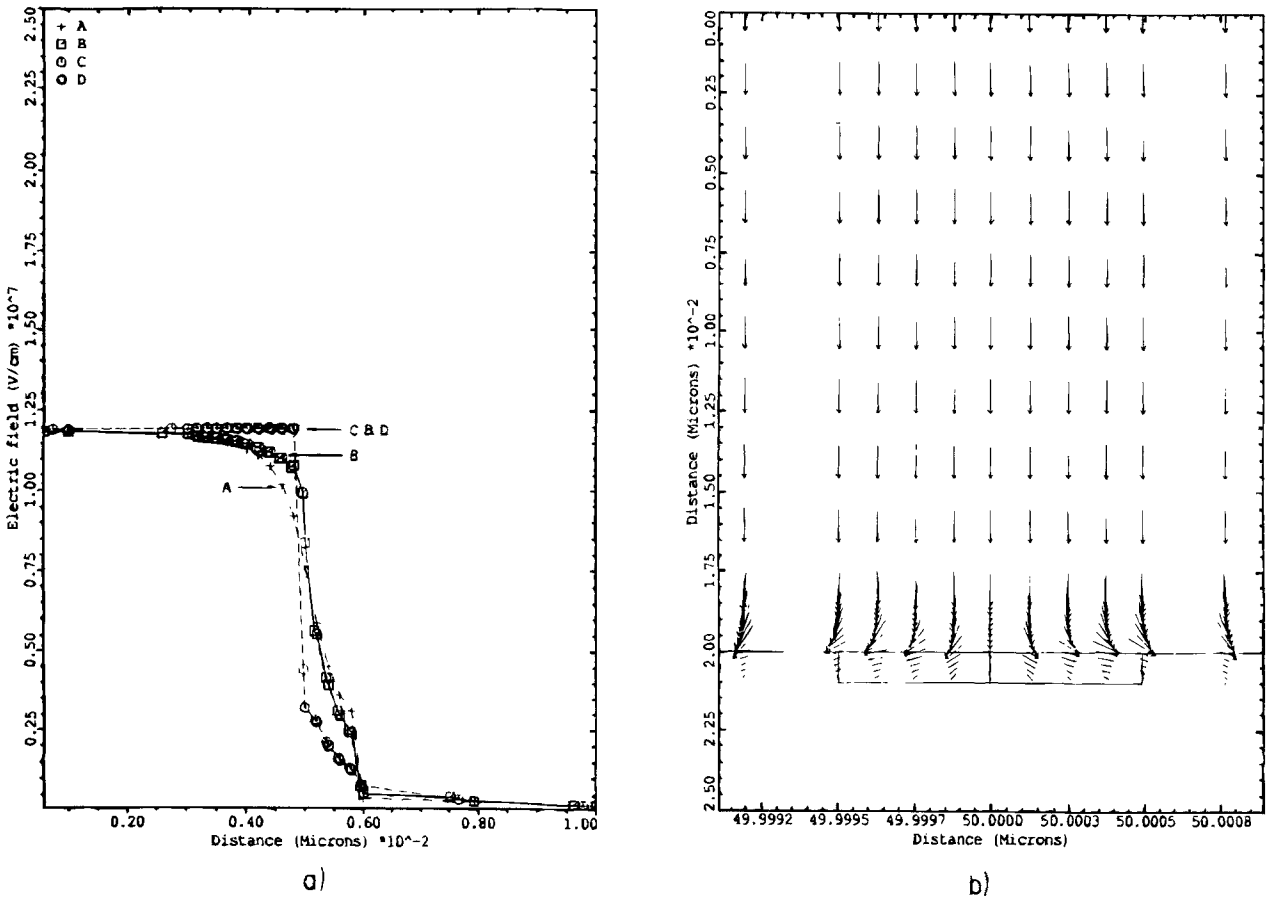

Fig. 7. (a and b) show the distribution of the electric field intensity along the lines a, b, and c defined in Fig. 2 as well as the spatial distribution of the electric field vectors in the vicinity of the negative Si asperity.

It was clearly shown that interface roughness, characterized in this work by a 1×1 nm^2 asperity, can strongly affect the electric field close to it, especially if it is a positive asperity (as earlier defined). The perturbation induced by this asperity is limited to a radius of about 10 nm. This implies that in the presence of such an asperity the dielectric strength of a 10 nm thick SiO_2 layer may be tremendously degraded.

Another important point which needs some consideration refers to the electric field distribution inside the SiO_2 layer. Our results clearly show that in the case where a single asperity is present at either the Al/SiO_2 or at the Si/SiO_2 interface, the electric field distribution is far from being homogeneous. This allows one to extrapolate that in case more than one asperity is present, especially in the case when an asperity is present at both the Al/SiO_2 interface and at the Si/SiO_2 interface, a severe field distortion within the SiO_2 layer should build up. It is then expected that the interface/surface effects (in our case displaying short range effects ~10 nm) will dominate the MOS capacitor operation and therefore breakdown phenomena.

Note the particular case of an Al_2O_3 asperity at the Al/SiO_2 interface. According to our results, the electric field was enhanced from 11.5 (in the bulk of the SiO_2) to 16.5 MV/cm immediately above the asperity. It is expected that depending on the sintering process, the average thickness of the Al_2O_3 layer (height of asperities) may vary. Accordingly, different field enhancements at the asperity may be expected, depending on the sintering parameters.

Since the formation of Al_2O_3 asperities is dependent on the reaction of Al with the underlying SiO_2, it is clear that if a stable gate material (GM) is used, *i.e.*, which would not react with SiO_2, and if its as-deposited SiO_2/GM interface were extremely flat, a lower SiO_2 surface roughness should be expected. As a consequence, the deterioration characteristics of a device with such interface characteristics should be improved.

One also observed the highly detrimental effect of the metallic precipitate which persists even for the negative asperity. This may have severe consequences if one thinks about the adhesion of bulk SiO_x precipitates to the growing SiO_2 layer upon thermal oxidation. If the SiO_x precipitates are not decorated by metals, our simulations showed that upon device operation no field enhancement should be expected. From this point of view, oxides grown on CZ or on FZ material should not exhibit any differences in their breakdown characteristics (no substrate effect). This, however, is in contrast with findings which showed the oxides grown on CZ material to exhibit worse breakdown characteristics than those grown on FZ material.[17,18] However, as also shown by our simulations, if this SiO_x precipitate is decorated by metals (it is assumed here that defect configuration 7 represents that condition in a first approximation), a field enhancement may be expected, even if the asperity (or roughness) is negative. In this way, metal decorated SiO_x precipitates may explain why the average breakdown field of oxides grown on CZ material is loser than those grown on FZ material. It is, of course, assumed in this discussion that a local field enhancement is a sufficient condition to accelerate the deterioration of the oxide.

Finally, an interesting case tested by means of the simulations was that of a local (microscopic) positive charge concentration. Although in this work only the case for an extreme and unrealistic charge concentration of 10^{15} cm^{-2} was explicitly shown, our study showed that only a localized positive charge concentration of 10^{13} cm^{-2} or higher may cause a local field enhancement. A nominal or effective (macroscopic) positive charge of 10^{11} cm^{-2} or higher can, of course, be thought of as being the result of a highly irregular charge distribution reaching values locally of up to 10^{13} cm^{-2}, or perhaps even somewhat higher. In that case,

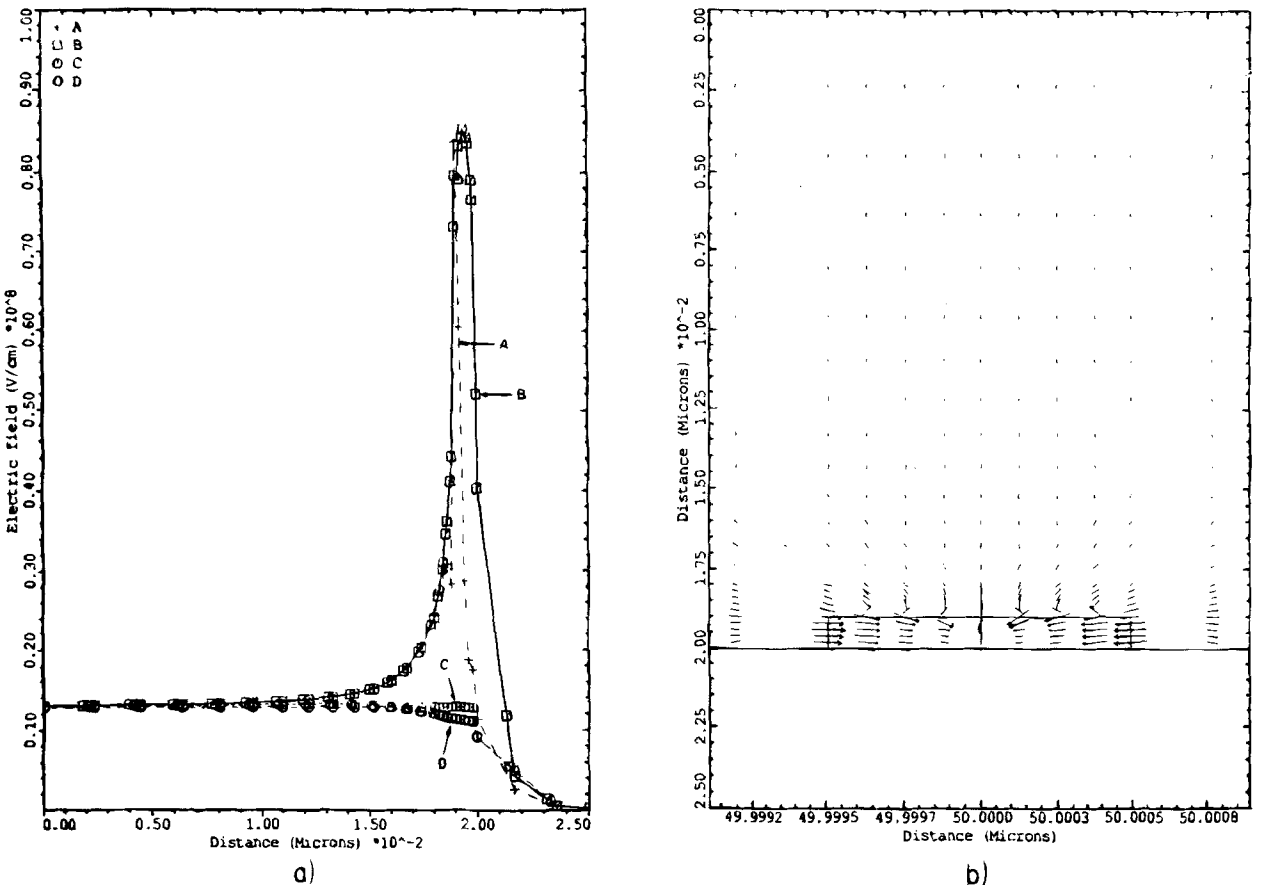

Fig. 8. (a and b) show the distribution of the electric field intensity along the lines a, b, and c defined in Fig. 2 as well as the spatial distribution of the electric field vectors in the vicinity of the positive Si asperity and a positive charge of 10^{15} cm^{-2}.

local field enhancement would again occur, resulting in accelerated deterioration of the oxide.

Conclusions

Square 1 × 1 nm^2 structural defect at the Al/SiO_2 or Si/SiO_2 interfaces of MOS capacitors biased into accumulation displayed the following effects upon numerical calculations.

1. A positive asperity is always detrimental (in the sense of its definition in the introduction of this work) whereas a negative asperity is of no harm unless it presents metallic characteristics. This implies that SiO_x precipitates are expected to be harmless with regard to breakdown characteristics of gate oxides unless they are decorated by metals.
2. Positive localized charges Q^+ are of no concern as long as their value remains below 10^{13} cm^{-2}. Higher values have an increasingly detrimental effect: a charge of 10^{15} cm^{-2} locally enhanced the electric field by up to one order of magnitude.

According to the results of our simulations, the most detrimental defects are expected to be those which associate positive asperities, metallic characteristics, and a localized positive charge (higher than 10^{13} cm^{-2}).

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Table II. Ratio of the maximum field value E_{max} in the vicinity of the asperity and the nonperturbed electric field E_b in the bulk SiO_2 (at least 10 nm far away from the asperity). The results correspond to the case of $Q^+ = 10^{10}$ cm^{-2}.

Asperity/material	Al_2O_3	SiO_x	Metal	Si or SiO_2
Positive	1.43	≈1	1.77	1.46
Negative	—	≈1	1.02	≈1

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Positive Charge Induced by Inorganic Spin-On-Glass

Influence of Silicon Oxide with High Yield of Water Absorption

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ABSTRACT

We investigated the influence of composite oxides on the electrical property of the Si/SiO_2 interface using a high frequency capacitance-voltage (*C-V*) technique. The composite oxides are composed of inorganic spin-on-glass (SOG) and nondoped silicate glass (NSG) film deposited by atmospheric pressure chemical vapor deposition with a high yield of water absorption. The density of SOG-related positive charge is enhanced about 1.8 times higher by laying the NSG film under the SOG film, while no enhancement is observed by laying it on the SOG film. The enhancement is because the underlying NSG film absorbs water generated by the dehydration of $Si(OH)_4$ during the SOG curing process. The water-absorbed NSG film seems to increase the amount of atomic hydrogen which generates the positive charge.

Spin-on-glass (SOG) is widely used with silicon oxides deposited by chemical vapor deposition (CVD) in the fabrication of metal oxide semiconductor integrated circuit (MOS IC) devices as an intermetal oxide (IMO) layer for its good planarity. The SOG film is formed by a spin-coating of SOG material dissolved in an organic solvent and is cured at a relatively low temperature when the film is used as the IMO in an aluminum interconnection system. However, the impurities contained in an insufficiently cured SOG film often cause some degradations of device characteristics such as mobile charge induced by bias-temperature (BT) stress,[1,2] hot carrier degradation,[3-6] and parasitic channel formation.[7-11] As for the parasitic channel formation, a positive charge induced by SOG (SOG-related positive charge) inverts the surface of p-type silicon substrate under the field oxide. It has been reported that the positive charge is located in the IMO layers[7-10] or at the Si/SiO_2 interfacial region.[11] The generation of the SOG-related positive charge can be suppressed by laying the plasma-enhanced chemical vapor deposition (PECVD) silicon oxide (p-SiO) with high dangling bond density under the SOG film.

On the other hand, CVD silicon oxide is commonly deposited by low pressure CVD (LPCVD), atmospheric pressure CVD (APCVD), or PECVD. It is well known that the CVD silicon oxide exhibits high yield of water absorption according to the deposition condition.[12-26] In addition, the silicon oxide containing water causes some problems such as corrosion of aluminum (Al) metallization,[27] poor adherence of photoresist,[28,29] hillock formation,[23] degradation of transistor characteristics due to BT stress,[16] hot carrier degradation,[25,30] and flatband voltage (V_{FB}) shift due to electron injection.[31]

In this study, we investigated the influence of composite oxides composed of the inorganic SOG film and APCVD silicon oxide with a high yield of water absorption on the electrical property of the Si/SiO_2 interface. The positive charge density was evaluated by a high frequency *C-V* technique. The yield of water absorption was evaluated by a Fourier transform infrared (FTIR) analysis combined with a pressure cooker treatment (PCT).

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Experimental

MOS capacitors.—To evaluate the charge in composite oxides, MOS capacitors were fabricated and subjected to high frequency (1 MHz) *C-V* measurements. Figure 1 shows the sample structure. p-Type (100) silicon substrates with resistivity of 50 Ω · cm were used. A 0.2 μm thick SiO_2 layer was grown by a wet oxidation (pyrogenic) for all wafers. After the oxidation, various types of composite oxides were formed on the SiO_2 film. The silicon oxides used in this study were SOG film, p-SiO film, nondoped silicate glass (NSG) film deposited by APCVD and a-NSG film which was a NSG film annealed in an N_2 ambient at 1000°C for 15 min. The SOG was a phosphorus-doped inorganic-type material which contained 8 weight percent (w/o) of silanol [$Si(OH)_4$] and 0.16 w/o of P_2O_5. The material was spin-coated on the wafer. The coated wafers were cured in an N_2 ambient at 400°C for 15 min in a furnace tube. p-SiO film was deposited at 400°C using an $SiH_4/N_2O/N_2$ (280/2500/3000 sccm) mixture as reactant gases in a dual frequency (250 kHz to 13.56 MHz) PECVD system. The total gas pressure was kept constant at 2.0 Torr and RF-power was 800 W. NSG film was deposited at 410°C using a 5% SiH_4/O_2 (1180/90 sccm) mixture as reactant gases. After the formation of silicon oxides, all wafers were annealed in an N_2 ambient at 450°C for 15 min, and *C-V* curves were measured at five points on each wafer using a mercury (Hg) probe as an electrode.

Analysis.—To measure the density of the dangling bond in the silicon oxides, electron spin resonance (ESR) measurements were carried out at room temperature using a JEOL JES FE3XG spectrometer operating at X band (9.36 GHz) with a 100 kHz magnetic field modulation. MgO served as a calibration standard. For the ESR measurements, 1 μm of silicon oxides were formed on the p-type silicon wafers with high resistivity (250 Ω · cm). The refractive index was measured using an ellipsometry at a wavelength of 632.8 nm.