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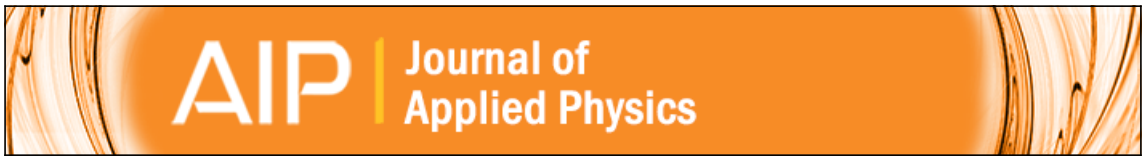

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Growth and characterization of GaAs on Si by vacuum chemical epitaxy

M. A. Cotta and M. M. G. de Carvalho
Inst. Fisica Gleb Wataghin, UNICAMP, CP 6165, 13081, Campinas, SP, Brazil

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Undoped GaAs epitaxial layers have been grown on Si substrates by vacuum chemical epitaxy. Triethylgallium and arsine were used as gallium and arsenic sources, respectively. The layers have shown KOH etch pit densities in the range 7×10^{6}–2×10^{7} cm^{-2} and residual hole concentration of 10^{15} cm^{-3}. The layer crystallinity was found to be strongly influenced by the substrate preparation and also by the water partial vapor pressure in the growth chamber.

I. INTRODUCTION

Vacuum chemical epitaxy (VCE) is a technique first developed by Fraas,[1-4] which tries to combine the advantages of metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). The basic idea is to utilize a hot wall graphite pyrolysis chamber where the substrate, upside down, gets in contact with group-III alkyl and group-V hydrides molecules in a high vacuum system. The graphite reaction chamber is contained within a stainless-steel vacuum chamber, which makes VCE systems much safer than conventional MOCVD systems. The vacuum chamber is pumped down to $1–2\times10^{-7}$ Torr before growth by a turbomolecular pump, and its atmosphere can be monitored by means of a residual gas analyzer (RGA). During the growth process, the total pressure is approximately 10^{-3} Torr. No carrier gas is needed to introduce the reagent molecules into the chamber and the utilization efficiency of these molecules is very high. These features and the relatively low cost of the system contribute to make it interesting for III-V compounds epitaxy.

Until now, a few studies have been made of VCE growth features,[5-7] but none of them presented any results of III-V compounds heteroepitaxy on Si substrates. We show here the first study on GaAs/Si growth by VCE. We have chosen this kind of heteroepitaxy for two main reasons. First, for the advantages of combining Si integrated circuits and GaAs circuits in the same monolithic structure, in spite of the great number of difficulties involved in this work. Second, because GaAs/Si growth by several epitaxial techniques has been intensively studied in the last years, so allowing us to compare the results obtained with VCE with those obtained with other techniques.

II. EXPERIMENT

The epitaxial growth has been carried out in our VCE reactor,[7] with initial pressure of about $1–2\times10^{-7}$ Torr. The substrates were *p*-type (B-doped) Si with net-carrier concentrations in the range 10^{15}–10^{16} cm^{-3}, cut 4° off (100) toward [011]. The substrates were degreased and chemically oxidized in a H_2SO_4:H_2O (2:1) solution. The oxide was then removed by dipping the substrates into dilute hydrofluoric acid (HF:H_2O,1:1). A thin protective silicon oxide was formed by exposing the Si substrates to 18 MΩ deionized water. The substrate was then immediately mounted on In-free Mo sample holders and loaded into VCE reactor. Thermal treatment to remove the oxide layer before growth was made by heating the substrate to 900 °C for 40 min in an AsH_3 atmosphere. The growth was carried out in two steps:[8] the first GaAs layer with about 500 Å thickness was grown at a temperature of 450 °C, at a low growth rate ($\simeq$25 Å/min) and annealed at 700 °C for 10 min. The second layer was grown on the first one with growth rates and temperatures in the range of 0.6–2.0 μm/h and 680–700 °C, respectively.

Molten KOH etching was carried out to estimate the dislocation density. The KOH etching was performed at 300–350 °C[9] and the observed small etch pits were also counted as etch pit density (EPD). Cu$K\beta$ x-ray diffraction (XRD) measurements were performed in order to evaluate the crystalline quality of the layers. Photoluminescence (PL) at 2 K and electrochemical capacitance-voltage (*C-V*) profiling were also performed to give information about the layers quality.

III. RESULTS AND DISCUSSION

Figure 1 shows the 2-K PL spectrum for a nonannealed 500-Å thick GaAs buffer layer, where we can observe the electron-to-heavy hole (*e*-HH) exciton-related transition. No PL signal was observed for the annealed sample. We believe the formation of misfit dislocations at the interface between the regrown buffer layer and Si[10] can be related to the decrease in PL intensity for the annealed sample. In such a thin layer the interface region contribution to the PL intensity must be more important than in the case of thicker samples.

Recently, some authors[11,12] have reported great improvement in the smoothness and defect density of GaAs/Si by lowering the arsenic overpressure during MBE growth of the initial GaAs layer. The low cracking efficiency[7] of the VCE hot wall pyrolysis may be contributing to improve on the quality of the GaAs buffer layers grown at low temperatures ($\simeq$450 °C), even when relatively high V/III ratios are employed. Indeed, the morphology of these thin layers grown by VCE shows few observable structures by optical microscopy [Fig. 2(a)] and a smoother surface than in the case of thicker layers [Fig. 2(b)], grown at higher temperatures and growth rates. The EPD of these thicker samples is in the range 7×10^{6}–2×10^{7} cm^{-2}, depending on the layer

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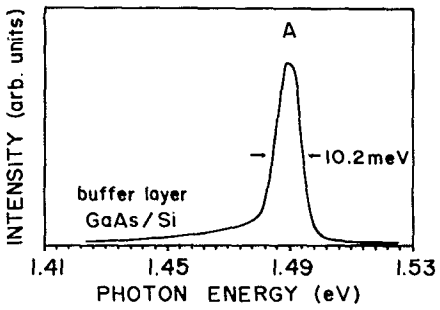

FIG. 1. 2-K PL spectrum of 500-Å-thick nonannealed GaAs buffer layer. Only the electron-to-heavy hole exciton-related transition can be observed.

thickness: thicker layers show smaller EPD values. Also, as it can be observed from Fig. 2(c), the etch pits align along the same direction. This feature indicates that the epitaxial layer is almost single domain, without large antiphase domain structures.[8] An anisotropic chemical etching ($3NH_4OH:1H_2O_2:5OH_2O$) has been employed to open stripes in the GaAs surface. Scanning electron micrographs of these etch patterns (Fig. 3) showed no antiphase domain structures, consistent with the results of Fischer *et al.*[13]

2-K PL spectrum of the undoped GaAs/Si (Fig. 4) shows four peaks already mentioned in literature.[14,15] Peak A corresponds to the electron-to-heavy hole exciton-related transition. The high energy shoulder of the dominant recombination process, associated to electron-to-light hole exciton-related transition, is not observed, due to the low radiative recombination efficiency of the sample as well as to the excitation densities in the range of mW/cm^2.[15] A linewidth of 5.3 meV is observed for peak A in Fig. 4, where the 2-K PL spectrum of a high purity homoepitaxial GaAs layer grown at the same run is shown for comparison. The biaxial tensile stress X, caused by the different thermal expansion coefficients of GaAs and Si, is evaluated from the shift of the $m_j = \pm\frac{1}{2}$ subband-to-band transition energy compared to bulk GaAs 2 K luminescence by using the expression:

$$E^{hh} = E^0 + [2a(S_{11} + S_{12}) + b(S_{11} - S_{12})]X \quad (1)$$

where a, and b are the GaAs hydrostatic and shear deformation potentials, respectively, and S_{11} and S_{12} are the elastic compliance tensor components. Using published values[15] ($a = -8.4$ eV, $b = -1.76$ eV, $S_{11} = 1.16\times10^{-3}$ $kbar^{-1}$, $S_{12} = -0.37\times10^{-3}$ $kbar^{-1}$), we obtain $X = 3.0$ kbar for the sample shown in Fig. 4. This value agrees very well with those found for the samples grown by MBE and MOCVD.[16,17] The luminescence line B at 1.470 eV is probably the band-to-carbon acceptor ($e - C_{As}$) recombination,[15] while line D at 1.429 eV should be a defect-related transition, since its intensity increases for thicker or annealed samples. The origin of peak C at 1.445 eV in PL spectrum is not known, but it is possibly the same transition observed by Stolz *et al.*[15] at 1.449 eV.

With regard to the electrical quality, all samples of GaAs on Si grown by VCE are p-type. Homoepitaxial GaAs layers grown in the same run show concentrations $\simeq 1.10^{15}$ cm^{-3} and Hall mobilities as high as 475 cm^2/V s at 300 K.

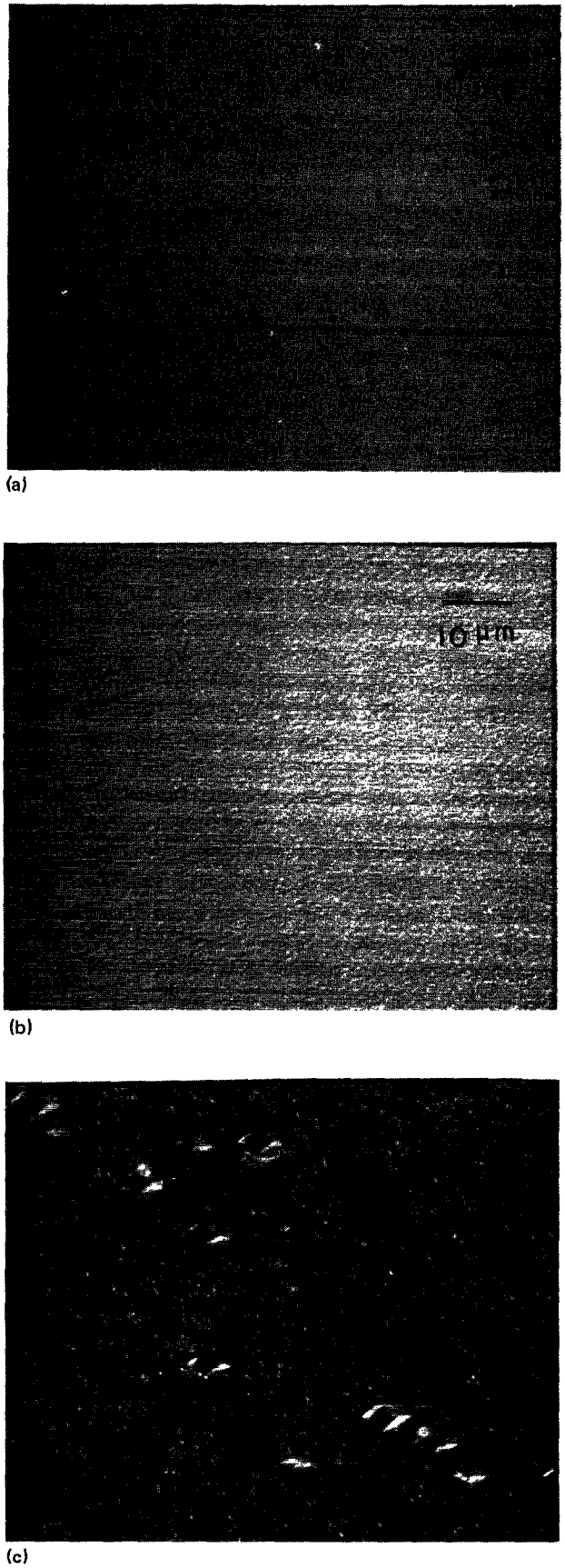

FIG. 2. Optical micrograph of the surface of the (a) 500-Å-thick GaAs buffer layer, (b) 1.2-μm thick GaAs layer grown on a thin buffer layer like that shown in (a); (c) molten KOH etch pattern for the same sample in (b).

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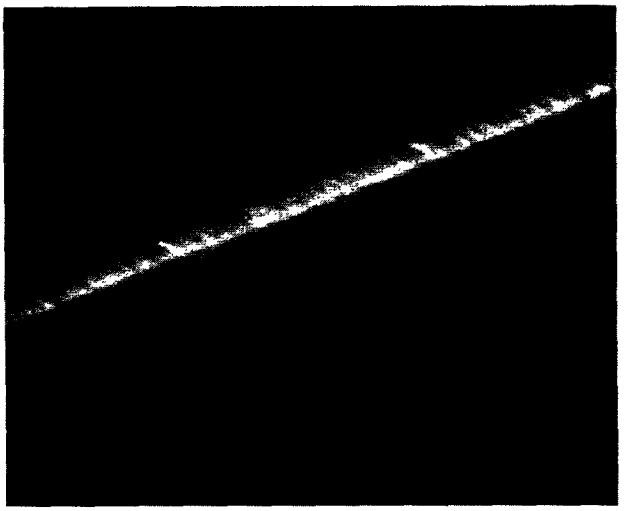

FIG. 3. Scanning electron micrograph of the anisotropically etched stripe pattern on the GaAs/Si surface.

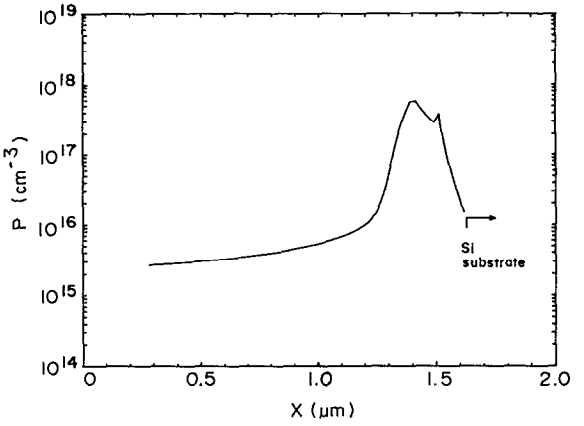

FIG. 5. Electrochemical *C-V* profile of the charge distribution of a 1.5-μm-thick GaAs layer on Si.

Electrochemical *C-V* profiling of GaAs on Si showed an inhomogeneous charge distribution along the layer: although the hole concentration p remains in the range 2×10^{15}–1×10^{16} cm^{-3}, there is a heavy residual p-doping in a $\simeq$0.3-μm thick region near the interface GaAs-Si (Fig. 5), which indicates that Si diffusion is not strong. Due to this rise in hole concentration, Hall measurements for GaAs on Si are not reliable.[14,18] The effect of antiphase domains in the electrical quality of the layers should be negligible, according to the etching results described above.

The crystalline quality of GaAs on Si grown by VCE can be estimated by the full width at half maximum (FWHM) of the (400) GaAs diffraction peaks, given in Table I. These values decreased by increasing the layer thickness (samples No. 71 to 73), annealing at temperatures of $\simeq$800 °C (samples No. 57 and 61) and also by lowering the GaAs growth rate (samples No. 57 and 72). These results agree with those found in literature[19,20] for other epitaxial techniques. Even so, the FWHM values are still very high. Through them, we can estimate[21] a dislocation defect density of $\simeq10^8$ cm^{-2}. The difference between this result and the observed EPD can be due to the difficulty of obtaining a good quantitative defect analysis by molten KOH etching of GaAs on Si.[22]

In our analysis, two main factors may be contributing to these large FWHM values and to the low PL efficiency of these samples. First of all, we have noticed a strong influence of the substrate preparation before growth on final results. In our case, the most important step has shown to be HF etching. HF quality and the time it is being used needed to be considered. Electronic grade HF containers which are open for more than a determined period ($\simeq$ one month) do not provide good morphologies anymore, as it can be seen from Fig. 6. For these reasons, much care must be taken during substrate preparation in order to avoid loosing growth runs, since our VCE reactor does not permit an *in situ* surface analysis before growth, neither a visual observation of the surface during growth. Besides that, there is a residual H_2O atmosphere in our reactor which can be estimated (through the RGA data) to be in the range of 0.5 ppm during growth, assuming that there is no H_2O contamination coming from the sources. Freundlich *et al.*[19] have shown that this value is

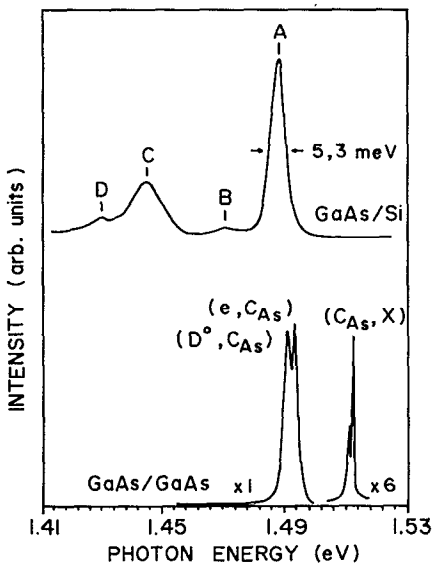

FIG. 4. 2-K PL spectra of GaAs layer grown in the same run on Si and SI GaAs substrates.

TABLE I. Growth conditions (growth temperature T_g, V/III ratio, growth rate dx/dt and total thickness h) and FWHM values of GaAs on Si grown by VCE.

Sample No.	T_g (°C)	V/III ratio	dx/dt (μm/h)	h (μm)	FWHM (arc sec)
57	680	14	1.2	1.2	1485
61[a]	680	14	1.2	1.2	1215
66	680	14	1.2	2.8	990
71	700	20	0.6	0.6	1440
72	700	20	0.6	1.2	1282
73	700	20	0.6	1.8	877

[a] Annealed at 800 °C for 5 min after growth.

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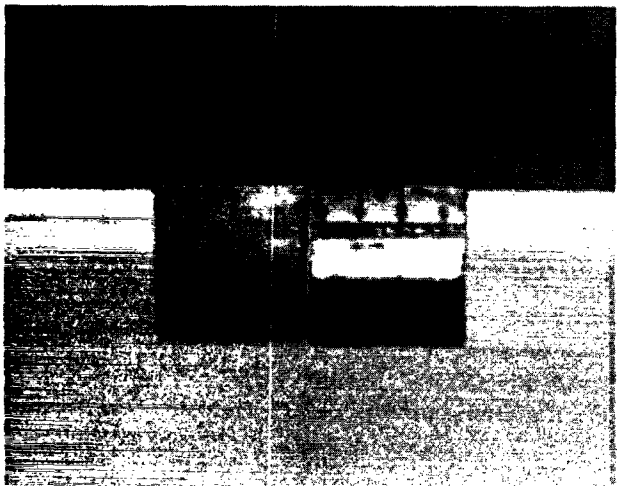

FIG. 6. Photograph of two GaAs/Si samples grown in the same run when: (left-hand side) the substrate was etched with electronic grade HF from a container which was opened $\simeq$ one month before, and (right-hand side) the substrate was etched with common HF from a just-opened container.

the maximum allowed limit of water vapor content in a MOCVD reactor atmosphere, in order to obtain good surface morphologies and crystalline qualities, so, in our case, small fluctuations of H_2O contents in VCE reactor, which actually occur, could lead to variations in the GaAs on Si quality. Indeed, an increase of FWHM has been observed with an increase of H_2O peak intensity in RGA spectrum. To check this point, a scanning Auger analysis has been performed on a sample consisting on a 500-Å-thick GaAs buffer layer on Si substrate, and showed oxygen contamination at the GaAs/Si interface. To study the influence of Si oxide in FWHM values of the GaAs layer, we have performed a growth in the same conditions as those of sample No. 57 in Table I, but on a Si substrate which was not thermally treated at 900 °C before growth. The FWHM value for this sample was $\simeq$26% greater than that for sample No. 57, so oxygen contamination on the Si surface can indeed be responsible for the large FWHM values of the GaAs/Si grown by VCE. Whenever this contamination comes from an incomplete oxide desorption or from the growth chamber atmosphere remains to be determined.

IV. CONCLUSIONS

We have shown here that the VCE technique can be used for GaAs epitaxy on Si. The results we have obtained so far agree with those obtained by using MOCVD and MBE techniques.

Through this work we could also observe that the VCE reactor atmosphere contamination, which happens everytime a substrate is replaced, is a serious problem, specially for Si heteroepitaxy. Although the first VCE system designed by Fraas[1] did not contain a load-lock chamber, it was included in the system later.[3] Actually, the lack of a load-lock chamber in our system imposes severe limitations. In our point-of-view, the H_2O vapor contents of the VCE reactor would only be lowered if we adopt its use. Also, in a recent work, Jönsson *et al.*[23] have shown *in situ* reflectance difference measurements which could be successfully used in VCE growth chambers. This kind of analysis would solve the problem of loosing growth runs when, for example, the substrate has not been perfectly prepared. We believe these modifications to our basic VCE system should be carried out in order to improve on Si heteroepitaxy by VCE.

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