A NEW, WATER-COOLED, 250KW, MODULAR MATRIX CONVERTER WITH HYBRID MODULATION AND INTELLIGENT GATE DRIVERS

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DOCTOR OF PHILOSOPHY

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Abstract

Matrix converter are direct AC/AC converters that directly connect each input phase to each output phase through an array of controlled semiconductors, inherently capable of bidirectional power flow. The main advantage of Matrix Converters is the absence of bulky reactive elements, that are subject to aging, and reduce the system reliability. In addition, Matrix Converter can work with high efficiency levels, that can be further enhanced by adopting a new PMW-based modulation technique, that reduces switching losses. These characteristics, combined with the complete custom design of the hardware components, permit to obtain a converter characterized by an excellent power density value.

Preface

Matrix converters are a kind of direct AC to AC power converters, consisting in an array of controlled semiconductor switches that directly connect each input phase to each output phase, and so they provide bidirectional power flow. The main advantage of Matrix Converters is that they are devoid of an intermediate DC link and, consequently, of bulky intermediate reactive elements, that are subject to aging and typically are the most unreliable element in any converter. In addition to this, Matrix Converters provide nearly sinusoidal input and output waveforms and controllable input power factor. In the light of the above, it's not surprising that Matrix Converters have received considerable attention as a good alternative to the typical Active Front End back to back with a Voltage Source Inverter configuration, which provides similar performances, albeit with some differences, the most notable one being the voltage levels. The early work dedicated to unrestricted frequency changers used thyristors with external forced commutation circuits to implement the bidirectional controlled, which were bulky and inefficient, but the advent of the power transistor gave momentum to the research in this field, resulting in the works of A. Alesina and M.

Venturini in the early 1980's [Venturini and Alesina(1980)], where they presented the Matrix topology as we know it today and invented its first modulation technique. Afterwards the research in this fields continued mainly in two lines. One line focuses on the development of bidirectional switches: in fact it must be noted that currently there are no discrete semiconductor devices that allow four quadrant switching operation, and so it is necessary to obtain it by combining discrete devices. The other line focused instead on alternative modulation techniques allowing higher voltage transfer ratio and better current quality. The first modulation technique presented by Alesina and Venturini, in fact, were limited to a voltage transfer ratio of 0.5. This ratio was then raised to 0.866 by means of third harmonic injection , a value which represents an intrinsic limitation of three-phase Matrix Converters with balanced supply voltages [Alesina and Venturini(1988)]. Other modulation techniques were then presented, like the "indirect method" [Huber and Borojevic(1989)] ,which describes the system as a traditional Active Front End connected by means of a "virtual DC-link" with a Voltage Source Inverter, and applies the well-known SVM technique.

However, Matrix Converters present several difficulties in their actual realization. First, the absence of free-wheeling diodes means that during the commutations it is necessary to actively provide the current with an alternative flowing path. Second, dangerous events like short-circuits and over-voltages must be managed with additional circuitry (like clamp units). Last, many switching techniques require additional information regarding voltages and currents flowing in the converter.

Chapter 1 gives an overview of the basic principles of matrix converters.

Chapter 2 proposes a novel modulation technique, namely the “Calvini Modulation” that allows obtaining a better performance in terms of efficiency.

Chapter 3 presents the complete design and the specifications of the converter, with the aim to obtain a product able to dominate the single-axis application market.

Chapter 4 presents the hardware development and the new solutions applied to obtain the wanted performances

Chapter 5 presents the various hardware tests of the isolated single components and their result.

Chapter 6 presents the whole assembled machine and the measurements made on it.

Chapter 7 is dedicated to the closing comments

Bibliography

[Alesina and Venturini(1988)] A. Alesina and M. Venturini. Intrinsic amplitude limits and optimum design of 9-switches direct pwm ac-ac converters. In *PESC '88 Record., 19th Annual IEEE Power Electronics Specialists Conference*, pages 1284–1291 vol.2, April 1988. doi: 10.1109/PESC.1988.18273.

[Huber and Borojevic(1989)] L. Huber and D. Borojevic. Space vector modulator for forced commutated cycloconverters. In *Conference Record of the IEEE Industry Applications Society Annual Meeting,*, pages 871–876 vol.1, Oct 1989. doi: 10.1109/IAS.1989.96746.

[Venturini and Alesina(1980)] M. Venturini and A. Alesina. The generalised transformer: A new bidirectional, sinusoidal waveform frequency converter with continuously adjustable input power factor. In *1980 IEEE Power Electronics Specialists Conference*, pages 242–252, June 1980. doi: 10.1109/PESC.1980.7089455.

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Chapter 1

Introduction

1.1 Overview

Matrix Converters, due to their ability to convert waveforms in a single stage, can be considered the most efficient AC/AC converter topology, capable of reducing various operation losses associated with conventional AC/DC/AC converters. At their core, matrix converters can be seen as “phase selector” devices, that directly transfer one input phase to an output phase. Fig.1.1 shows the core structure for a three-phase to three-phase Matrix Converter, when the converter is fed from a three phase voltage source at the input and provides power to an inductive load, but the available topologies are not limited this one, among them the three-phase to single-phase topology

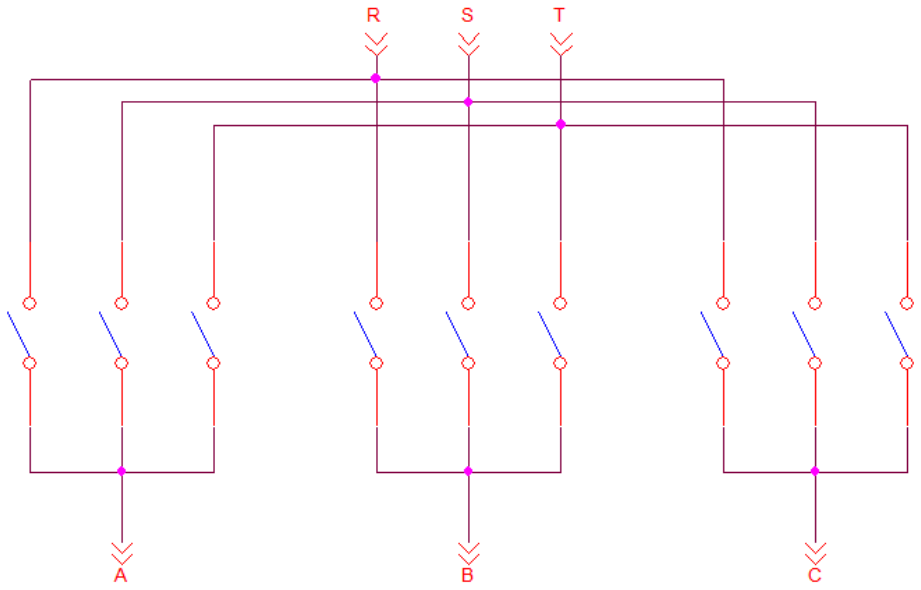

Figure 1.1: Matrix Converter core structure

Obviously, due to some physical and technological limitations that are not taken in consideration in this idealization, an actual Matrix Converter is a more complex device, consisting at least in a power conversion section, an input filter and a clamp unit, as it will be discussed in the following chapters.

1.2 The bidirectional switch problem

The ideal bidirectional switches that appear in Fig.1.1 are not readily available as discrete semiconductors and must be obtained starting from traditional unidirectional devices.
Three main different configurations have been proposed in literature [[Neft and Schauder(1988), S. Bernet and Lipo(1996), Ziogas and Khan(1986)]] and are shown in Fig. 1.2, Fig. 1.3 and Fig. 1.4.

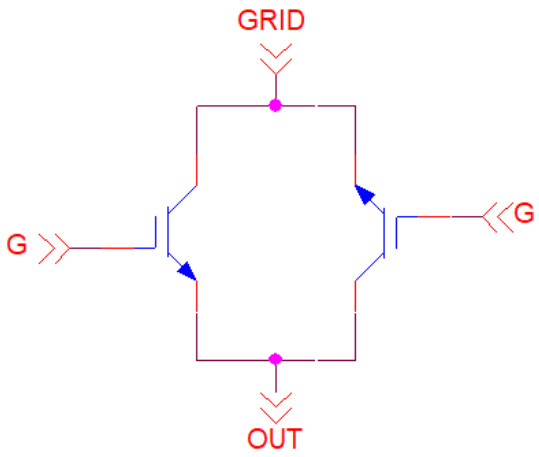

Figure 1.2: Bidirectional switch realized with reverse blocking IGBTs

The first configuration is the simplest from the topological point of view and uses two anti-paralleled reverse blocking IGBTs. In this switch arrangement there are two separated internal current conduction paths in both directions, and these paths can be independently controlled in order to safely commutate the load current between different bidirectional switches. In this way it would be theoretically possible to eliminate local snubbers on the switches. However, reverse blocking IGBTs did not receive the favors of the market, and consequently have not improved much in comparison with traditional IGBTs or SiC FETs, and they topically present very high switching losses, while they do not behave much better in terms of conduction losses when compared with the IGBTs in series with a blocking diode.

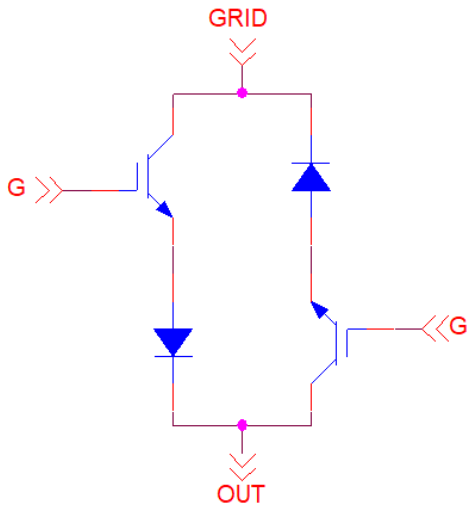

Figure 1.3: Bidirectional switch realized with two diodes and two traditional IGBTs

In the light of the above, the second bidirectional switch configuration retains the same advantages of the first while enabling higher switching frequencies, at the cost of doubling the number of components (but not their cost or the die area). Higher switching frequencies mean smaller reactive components, which are always the bulkiest elements of a converter. Since the aim of this thesis was to design and develop a ready-to-market product, this was the chosen configuration for the switches, albeit with some tiny differences that will be discussed in the following chapters.

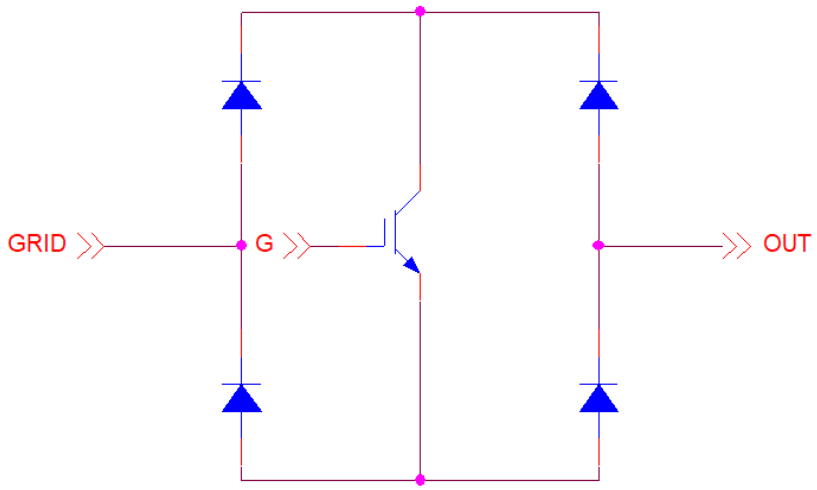

Figure 1.4: Bidirectional switch realized with single traditional IGBTs and diode bridge

The third switch configuration is listed for the sake of completeness; it uses a diode bridge that permits current flow in both directions when the central IGBT is closed. While this solution it is certainly the one that costs less, since diodes are way cheaper than IGBTs, it presents two big drawbacks. The first and most evident is that current needs to flow in three different devices, resulting in higher conduction losses when compared to the two aforementioned configurations. The second is that this configuration needs additional local snubbers, due to the fact that there are no separate conduction paths for the two possible current directions, and so, in order to perform a commutation, it is necessary to choose between closing the in-going switch before opening the outgoing one (resulting in an over-current), or, vice versa, opening the outgoing switch before closing the in going one (resulting in an over-voltage).

1.3 Commutation strategies

One of the main issues related to the control of Matrix Converters is the current commutation: the (bidirectional) switches are not protected by the DC-link capacitors and there are no natural freewheeling paths. It can be said that the current commutation between

switches in the Matrix topology is more difficult to achieve than in other, more traditional, solutions.

When considering commutation strategies for matrix converters two general basic rules must be adhered:

- commutation should not cause a short circuit between the two input phases, because the consequent high circulating current might destroy the switches
- commutation should not cause an interruption of the output current because the consequent overvoltage might likely destroy the switches.

Consider the simplified commutation circuit shown in Fig.1.5

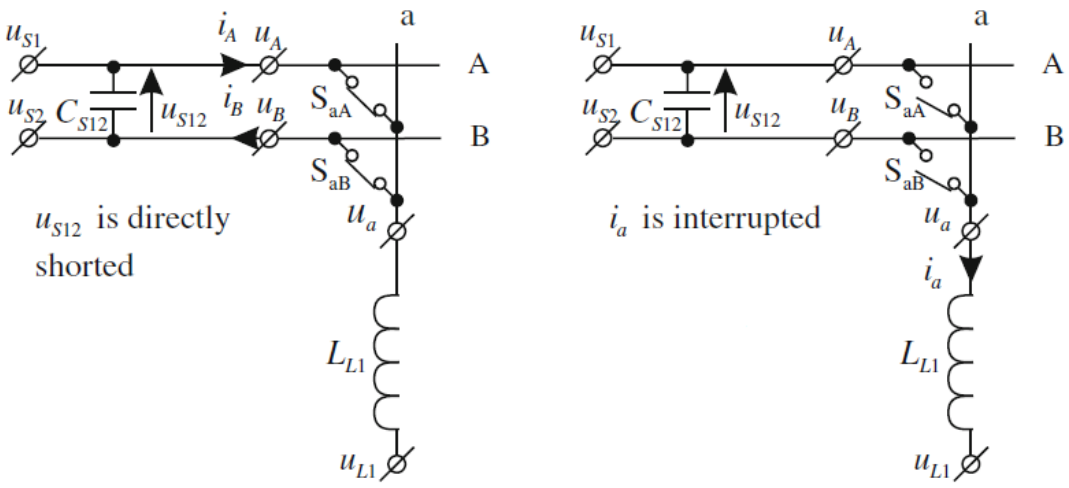

Figure 1.5: Simplified commutation circuit

When the switches are turned on simultaneously, the voltage sources will be shorted directly and the switches will be damaged due to overcurrents. On the other hand, if all the switches are turned off simultaneously, in the first instant after the switching-off an over-voltage will be generated which could destroy the semiconductors. The spikes of over-voltage depend on load current and duration of current interruption. However, the semiconductor devices cannot be switched instantaneously between states because of propagation delays and finite switching times, and various methods have been proposed to avoid these difficulties and to ensure a safe and successful commutation. The most common one (and

the one which was utilized in the converter developed during this thesis) is the four-step commutation strategy, also known as “semi-soft current commutation”. In order to explain the strategy it is helpful to refer to the elementary commutation cell shown in Fig.1.6.

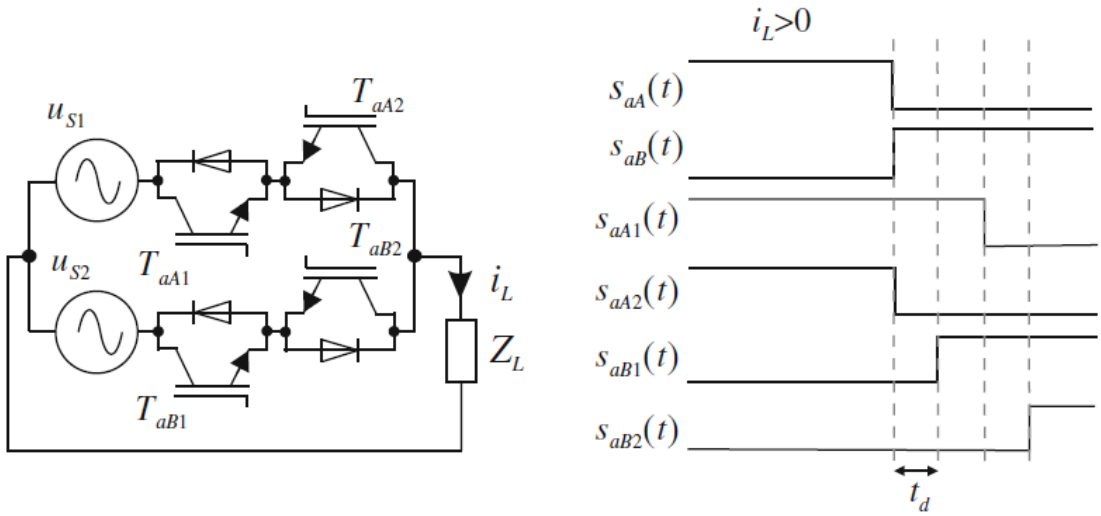

Figure 1.6: Elementary commutation cell with positive load current

The strategy assumes that when the output phase is connected to an input phase, both the IGBTs of the bi-directional switch S1 have to be turned on simultaneously. The following example assumes that the load current is in the direction as shown in Fig.1.6 and the upper bi-directional switch (S1) is closed. In this method, it is needed to know the current direction, which is used to determine which device in the active switch cell is not current conducting. The commutation process is shown as a timing diagram in Fig.1.6. In the beginning, both IGBTs of switch S1 are turned on in the same instant. In the first step, the IGBT T_{aA2}, which is not conducting the load current, is turned off. In the second step, after delay interval time t_d , the transistor T_{aB1} that will conduct the current is turned on. This allows both cells to be turned on without short circuiting the input phases and provides a path for the load current. Depending on the instantaneous input voltages, there are two kinds of commutation process after the second step. If $u_{S2} > u_{S1}$ and $i_L > 0$, then the conducting diode of switch cell S1 could be reverse biased and a natural commutation could take place. In the third step the IGBT T_{aA1} is turned off. If there is no natural commutation during the second step, then a hard commutation happens when, in the third step, IGBT

T_{aB1} is turned off. It must be noted that this uncertainty is reflected in the actual output voltage in terms of $V \cdot s$, but can usually be considered neglectable. In the fourth step, transistor T_{aB2} is turned on to also allow the conduction of negative currents. The time delay has to be set to a value higher than the maximum propagation time of the IGBT signals. In this strategy half of the commutation process is soft switching and half is hard switching, hence the name "semi-soft current commutation". However, when the currents are around the zero value, the current direction is not certain, and incorrect decisions can be made as to which switches conducts the load current. This can be a problem if no protection device (a clamping unit) is employed, however it is also true that the resulting overvoltages around the zero current value are usually limited. Fig.1.7 shows the commutation circuit and timing diagram for the condition $i_L < 0$.

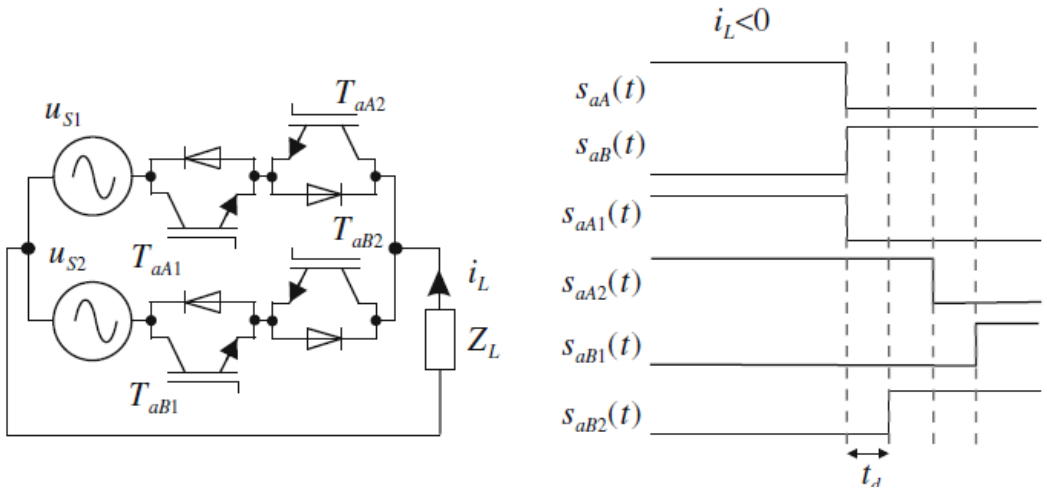

Figure 1.7: Elementary commutation cell with negative load current

1.4 Comparison with traditional solutions

Following the considerations of 1.2, the circuit of Matrix Converter topology is presented in Fig.1.8, where the switches are implemented with the double anti-paralleled IGBTs configuration.

In this section the Matrix topology will be compared with the traditional AC/AC solutions that are listed below, along with their principal characteristics.

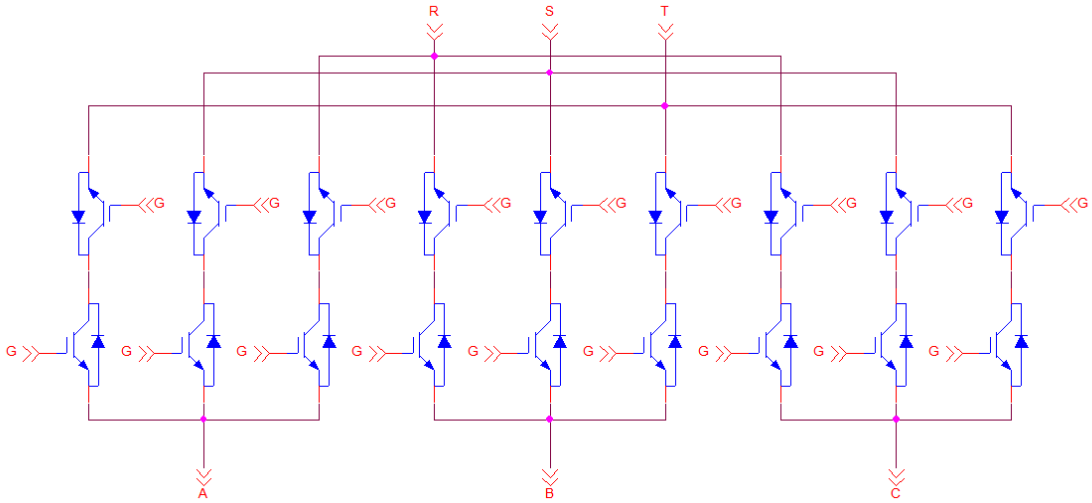

Figure 1.8: Matrix converter schematic

1.4.1 Diode Bridge Rectifier + Full Bridge Inverter

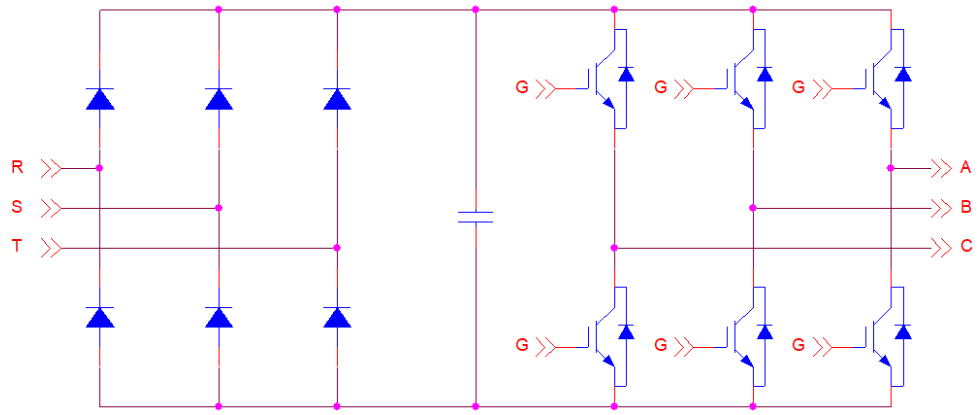

Figure 1.9: Diode bridge rectifier with full bridge inverter schematic

In this indirect AC/DC/AC topology, shown in Fig.1.9, the input diode bridge rectifies an AC source into a DC, which is then smoothed out by some bulky and prone to aging DC-link capacitors and made available to a full bridge inverter, which then feeds the load. It is possible to feed multiple Full Bridge Inverters on the same Diode Bridge Rectifier.

This solution is still the most diffused, being consolidated and available at low cost, albeit presenting some serious limitations. First, the input diode bridge prevents bidirectional power flow. This not only prevents this topology for being used in power generation applications, but also from carrying out any regenerative braking operation in any motor application. In fact, the most diffused braking solution makes use of a chopper unit dissipating the motor energy that is made available on the DC-link by inverting the power flow in the full bridge.

Second, the pulsating current absorption of the diode bridge rectifier on the capacitors causes a large amount of harmonics that produces distortion of the input line voltages. This gives rise to a series of problems regarding the performance of sensitive loads and equipment connected to the same supply, causes additional losses on the utility system, lowers power factor due to waveform form factor and may excite electrical resonances. After all, this topology is the one that raised the problem of the power quality.

1.4.2 Active Front End + Full Bridge Inverter

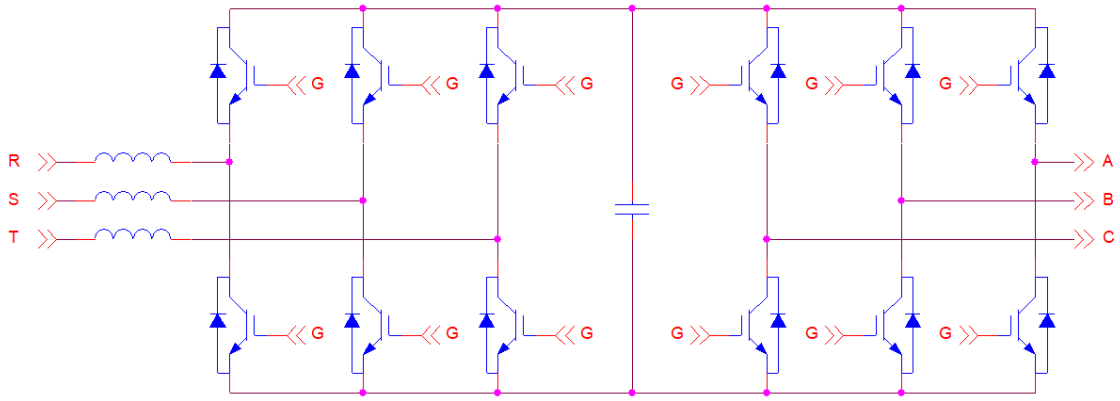

Figure 1.10: Active Front End with full bridge inverter schematic

In this indirect AC/DC/AC topology (also known as back-to-back converter), shown in Fig.1.10, the input Active Front End rectifies an AC source into a DC, which is then smoothed out by DC-link capacitors and made available to a full bridge inverter, which

then feeds the load. It is possible to feed multiple Full Bridge Inverters on the same Active Front End.

The Active Front End is capable of shaping the input current, and enables the operation with near-unity power factors with almost perfectly sinusoidal current and, consequently, low harmonic distortion. In addition, the converter is capable of bidirectional power flow and, of course, of regenerative braking. This solution is virtually capable of supplying any possible output voltage, since the the Active Front End can step up the voltage while the Full Bridge Inverter can step it down. With that said, it must be noted that while addressing many of the problems of the Diode Bridge Solution, this topology is still affected by the necessity of adopting a large DC-link capacitor.

1.4.3 Cycloconverter

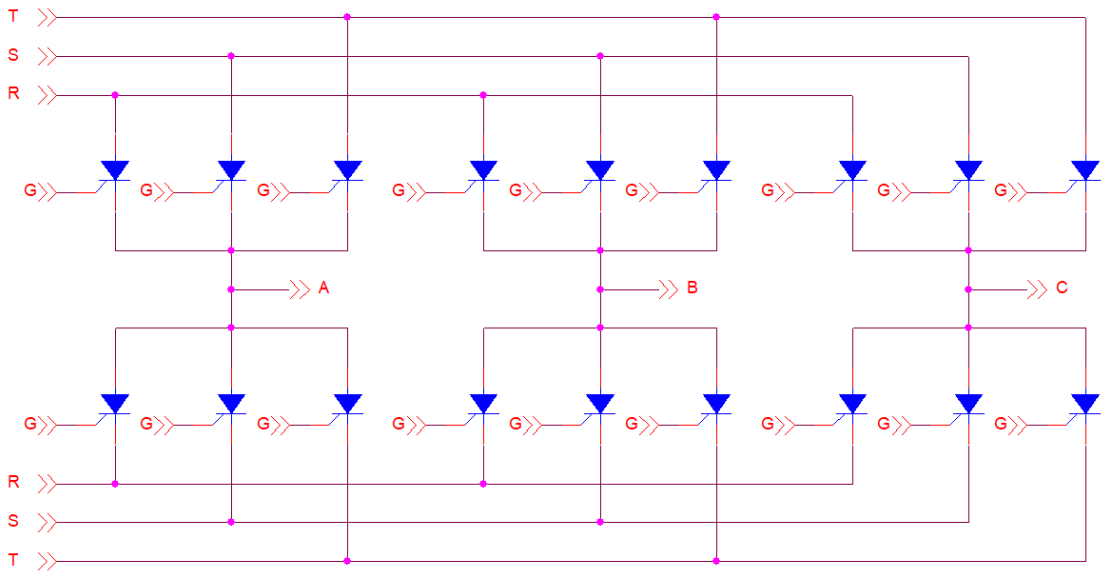

Figure 1.11: Cycloconverter schematic

A cycloconverter, shown in Fig.1.11, is basically a self-commutated Matrix Converter based on thyristors, and it is effectively a direct AC/AC converter. Since a cycloconverter is capable of turning its (bidirectional) switches off only when the AC supply current crosses the zero, it is capable of supplying its load only with a fundamental frequency that it is a

fraction (typically less than one-third) of the AC input frequency. Moreover, in a cycloconverter the input current always lag behind the input voltage, effectively making impossible unity-power factor operation. Last, both output and input current are heavily distorted, and this distortion increases proportionally with output frequency. This relevant drawbacks limits the usage of cycloconverters typically to low number of poles, slow rotating, high power motors, operating off of the mains grid. In fact, cycloconverters are usually seen only in naval traction applications, where they are fed from the relatively high frequency (typically 400Hz) on-board generators and provide power to large motors directly connected to the propeller.

1.4.4 Comparison

After this analysis it's possible to say that in comparison with the other converters, the Matrix Converter shines in high-performance, highly reliable single-axis applications, where space and efficiency are at premium. In fact, the Matrix Converter presented in this thesis was mainly developed for supplying HVAC systems and high performance medium size (500 kW) direct-drive motors.

1.5 Aim of the thesis

As already mentioned, the aim of this thesis was to develop a state-of-the-art converter using the Matrix Topology and take advantage of the DC-link absence in order to create a converter as small as possible in pursue of motor-drive integration. To do that a new modulation technique, called "Calvini modulation", able to reduce switching losses (and so heat sink dimensions) when compared to the traditional ones, was developed for this specific drive and every design choice, that will be discussed in the next chapters, was made with system miniaturization in mind. All the possible aspects, from the electronic boards to the mechanical assembly were pointed towards compactness.

Bibliography

[Neft and Schauder(1988)] C.L. Neft and C.D. Schauder. Theory and design of a 30-hp matrix converter. *Conference Records of IEEE/IAS Annual Meeting*, pages 934–939, 1988.

[S. Bernet and Lipo(1996)] T. Matsuo S. Bernet and T.A. Lipo. A matrix converter using reverse blocking nptigbts and optimised pulse patterns. *Proceedings of IEEE/PESC96*, pages 107–113, 1996.

[Ziogas and Khan(1986)] P. D. Ziogas and S. I. Khan. Analysis and design of forced commutated cycloconverter structures with improved transfer characteristics. *IEEE Transactions on Industrial Electronics*, IE-33(3):271–280, Aug 1986. ISSN 1557-9948. doi: 10.1109/TIE.1986.350233.

Chapter 2

The Calvini Modulation

2.1 Overview

The first rigorous mathematical analysis of a Matrix Converter modulation technique has been developed by Venturini and Alesina, and enabled a maximum voltage transfer ratio (VTR) of 50%. Venturini and Alesina then discovered that it was possible to increase the value of the maximum VTR, by introducing a common-mode voltage (CMV) by means of injecting a third harmonic, effectively raising its value to $\frac{\sqrt{3}}{2}$. This third harmonic is not a fixed value, but instead it must be calculated as a combination of third harmonic grid frequency and third harmonic output frequency. This value not only can only be obtained in presence of balanced supply voltages and balanced load, but also represents an intrinsic limitation [[Alesina and Venturini(1988)]] of the three-phase to three-phase matrix converter. In fact, the subsequent space-vector modulation (SVM) approach, proposed in [[Huber and Borojevic(1989)]] achieves the same voltage transfer ratio of $\frac{\sqrt{3}}{2}$.

The converter presented in this thesis was developed in conjunction with a new modulation approach presented in [[Pipolo and Formentini(2019)]] the Calvini Modulation, in which a new common-mode-voltage addition technique is exposed, which calculates the common-mode voltage components by taking into account the knowledge of output power demand , maintaining the same maximum VTR of 86.6%. However, this technique, when compared to the Venturini's method, enables the reduction of the commutation losses. At the very core, in fact, the Calvini modulation tries to always switch only between the two

closest input phases. This also has the intuitive side effect of reducing the output ripple and current harmonic distortion.

2.2 The Calvini Modulation

The detailed Calvini Modulation analysis is reported in the following section, as it was covered in [[Pipolo and Formentini(2019)]]. The electrical quantities under investigation are shown in Fig.2.1.

It is clear that, in every time instant, in a three phase system the three sinusoidal input waveforms will be at three different levels, except in an infinitesimal time lapse where two phases could be equal. This means that there will exist a phase with the highest voltage , a middle one, and the lower one.

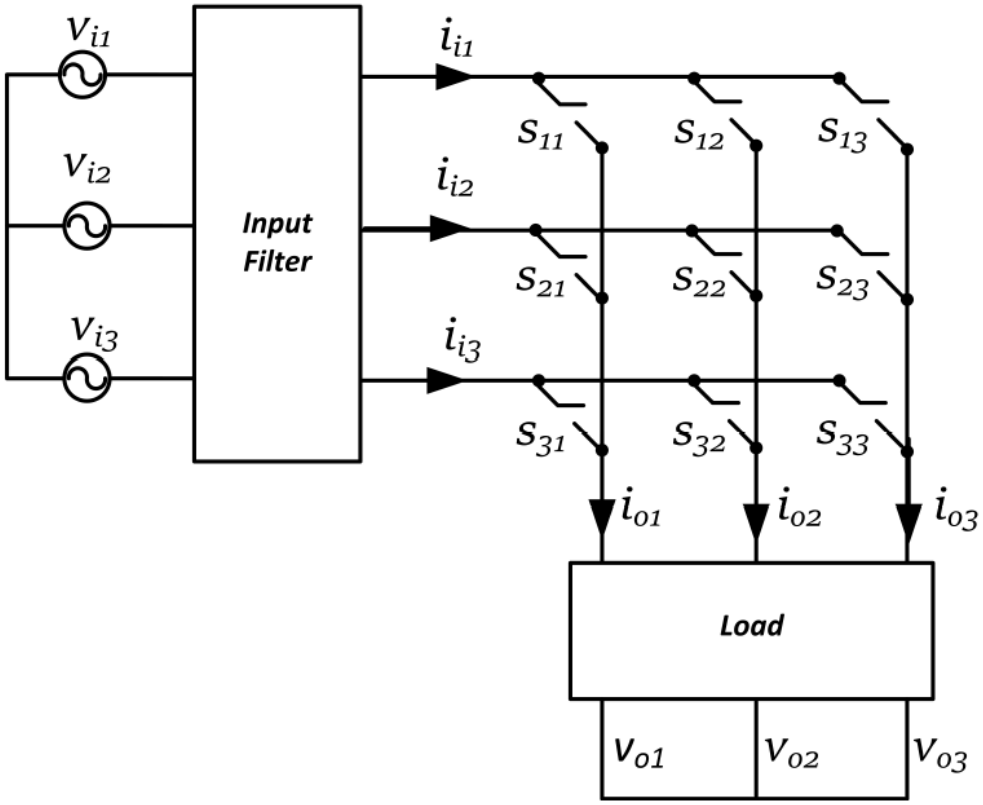

Figure 2.1: Quantities under investigation in the Matrix Converter

We will assume that in a specific time instant :

$$\begin{aligned} v_{i1} > v_{i2} > v_{i3} \\ v_{o1} > v_{o2} > v_{o3} \end{aligned} \tag{2.1}$$

As we said, it is our desire to obtain the output voltages starting from the closest input phase, and so, if we also assume that, in a certain moment

$$v_{o2}^{*} + v_o < v_{i2} \tag{2.2}$$

Where the asterisk denotes a reference quantity and v_o the common mode voltage to be injected.

Then, in order to obtain v_{o1} we will switch between v_{i1} and v_{i2}, while in order to obtain vo2 and vo3 we will switch between vi2 and vi3.

In the light of the above, it will hold true that

$$v_{o1} + v_o = d_{11}v_{i1} + d_{21}v_{i2} \tag{2.3}$$

Where d_{11} is the duty cycle associated with switch s_{11}, d_{21} is the duty cycle associated with switch s_{21}, etcetera. Since it must always be that

$$d_{11} + d_{21} = 1 \tag{2.4}$$

we will then solve the system formed by 2.3 and 2.4 for the duty cycles obtaining

$$\begin{aligned} d_{11} &= (v^*_{o1} + v_o - v_{i2})(v_{i1} - v_{i2}) \\ d_{21} &= (v_{i1} - v^*_{o1} - v_o)(v_{i1} - v_{i2}) \end{aligned} \tag{2.5}$$

In the same manner we can solve the two other systems formed by,

$$\begin{aligned} v_{o2} + v_o &= d_{22}v_{i2} + d_{32}v_{i3} \\ d_{22} + d_{32} &= 1 \end{aligned} \tag{2.6}$$

and

$$\begin{aligned} v_{o3} + v_o &= d_{23}v_{i2} + d_{33}v_{i3} \\ d_{23} + d_{33} &= 1 \end{aligned} \tag{2.7}$$

that result in

$$
\begin{aligned}
d_{22} &= \frac{(v^*_{o2} + v_o - v_{i2})}{(v_{i2} - v_{i3})} \\
d_{32} &= \frac{(v_{i1} - v^*_{o2} - v_o)}{(v_{i2} - v_{i3})} \\
d_{23} &= \frac{(v^*_{o3} + v_o - v_{i3})}{(v_{i2} - v_{i3})} \\
d_{33} &= \frac{(v_{i2} - v^*_{o3} - v_o)}{(v_{i2} - v_{i3})}
\end{aligned} \tag{2.8}
$$

Also input currents can be expressed as function of duty cycles and output currents resulting in

$$i_{i1} = i_{o1} d_{11} \tag{2.9}$$

$$i_{i2} = i_{o1} d_{21} + i_{o2} d_{22} + i_{o3} d_{23} \tag{2.10}$$

$$i_{i3} = i_{o2} d_{32} + i_{o3} d_{33} \tag{2.11}$$

If we then substitute the aforementioned duty cycles in 2.9 we obtain

$$i_{i1} = \frac{i_{o1}(v_o + v_{i2} + v^*_{o1})}{(v_{i1} + v_{i2})} \tag{2.12}$$

In order to ensure sinusoidal input currents, an input current reference can be defined. Equation 2.12 can then be solved for v_o resulting in

$$v^I_o = (\frac{i^*_{i1}}{i_{o1}})(v_{i1} - v_{i2}) + v_{i2} - v_{o1} \tag{2.13}$$

We can then calculate the input current reference i^*_{i1}

by assuming unitary power factor and imposing a power balance between input and output

$$i^*_{i1} = P_o v_{i1} / V_i^2 = (i_{o1} v^*_{o1} + i_{o2} v^*_{o2} + i_{o3} v^*_{o3}) \frac{v_{i1}}{(v^2_{i1} + v^2_{i2} + v^2_{i3})} \tag{2.14}$$

If 2.2 does not hold true and we have instead

$$v^*_{o2} + \nu_o > v_{i2} \tag{2.15}$$

then, in order to obtain v_{o1} and v_{o2} we will switch between v_{i1} and v_{i2}, while in order to obtain v_{o3} we will switch between v_{i2} and v_{i3}.

Following that, we reapply the same steps and we find that in this case we have

$$\begin{aligned}
d_{11} &= \frac{(v^*_{o1} + \nu_o - v_{i2})}{(v_{i1} - v_{i2})} \\
d_{21} &= \frac{(v_{i1} - v^*_{o1} - \nu_o)}{(v_{i1} - v_{i2})} \\
d_{12} &= \frac{(v^*_{o2} + \nu_o - v_{i2})}{(v_{i1} - v_{i2})} \\
d_{22} &= \frac{(v_{i1} - v^*_{o2} - \nu_o)}{(v_{i1} - v_{i2})} \\
d_{23} &= \frac{(v^*_{o3} + \nu_o - v_{i3})}{(v_{i2} - v_{i3})} \\
d_{33} &= \frac{(v_{i2} - v^*_{o3} - \nu_o)}{(v_{i2} - v_{i3})}
\end{aligned} \tag{2.16}$$

$$\begin{aligned}
i_{i1} &= i_{o1} d_{11} + i_{o2} d_{12} \\
i_{i2} &= i_{o1} d_{21} + i_{o2} d_{22} + i_{o3} d_{23} \\
i_{i3} &= i_{o3} d_{33}
\end{aligned} \tag{2.17}$$

$$\nu^{II}_o = (\frac{i^*_{i3}}{i_{o3}})(v_{i3} - v_{i2}) + v_{i2} - v_{o3} \tag{2.18}$$

$$i^*_{i3} = P_o v_{i3} / V_i^2 = (i_{o1} v^*_{o1} + i_{o2} v^*_{o2} + i_{o3} v^*_{o3}) \frac{v_{i3}}{(v^2_{i1} + v^2_{i2} + v^2_{i3})} \tag{2.19}$$

So, the common mode voltage from 2.13 must be added whenever 2.2 does hold true, and 2.18 must be added when 2.15 holds true.

2.3 Calvini Modulation VTR and operative range

With the assumption of studying a balanced three phase system (Fig.2.2), we can restrict the system analysis to a voltage input and output angle between $[-\frac{\pi}{3}, \frac{\pi}{3}]$, since the waveforms present a periodicity of $\frac{2\pi}{3}$.

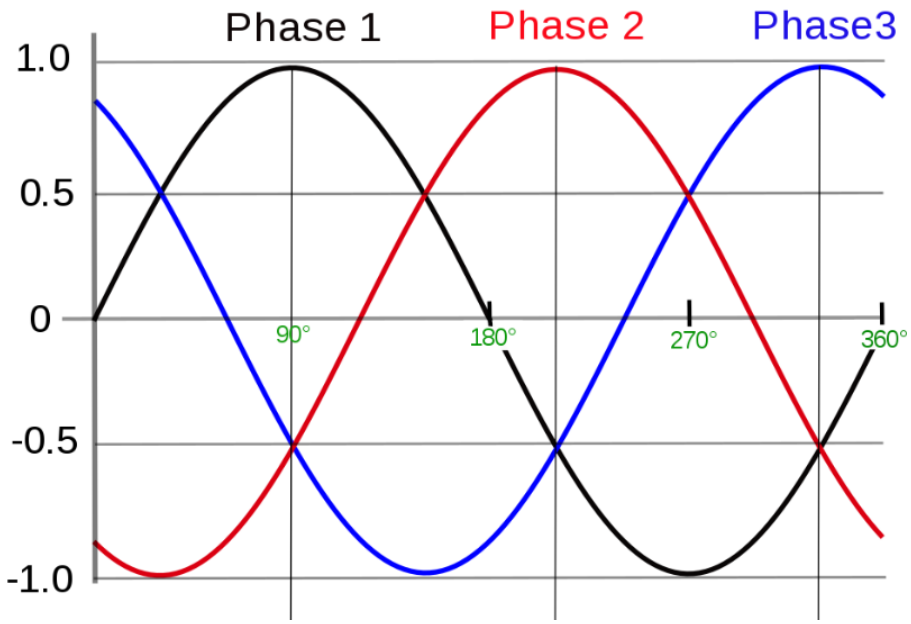

Figure 2.2: Normalized three phase system

If we want 2.1 to hold true in a three phase system we can express it as

$$
\begin{aligned}
v_{i1} &= V_i cos(\theta_i) \\
v_{i2} &= V_i cos(\theta_i - \frac{2\pi}{3}) \\
v_{i3} &= V_i cos(\theta_i + \frac{2\pi}{3}) \\
&[0, \frac{\pi}{3}]
\end{aligned}
\tag{2.20}
$$

and

$$\begin{gathered} v_{i1} = V_i cos(\theta_i) \\ v_{i2} = V_i cos(\theta_i - \frac{2\pi}{3}) \\ v_{i3} = V_i cos(\theta_i + \frac{2\pi}{3}) \\ [-\frac{\pi}{3}, 0] \end{gathered} \tag{2.21}$$

the same can be said for output reference voltages and output currents, which can be written in the following form

$$\begin{gathered} v^*_{o1} = V_o cos(\theta_o) \\ v^*_{o2} = V_o cos(\theta_o \pm \frac{2\pi}{3}) \\ v^*_{o3} = V_o cos(\theta_o \mp \frac{2\pi}{3}) \\ i_{o1} = I_o cos(\theta_o + \phi_o) \\ i_{o2} = I_o cos(\theta_o + \phi_o \pm \frac{2\pi}{3}) \\ i_{o3} = I_o cos(\theta_o + \phi_o \mp \frac{2\pi}{3}) \end{gathered} \tag{2.22}$$

The reference current can be expressed as

$$\begin{gathered} i^*_{i1} = I^*_i cos(\theta i) \\ i^*_{i2} = I^*_i cos(\theta_i \mp \frac{2\pi}{3}) \\ i^*_{i3} = I^*_i cos(\theta_i \pm \frac{2\pi}{3}) \end{gathered} \tag{2.23}$$

Where I^*_i is obtained imposing power balance between input and output

$$I_i^* = \frac{I_o V_o cos(\phi_o)}{V_i} \tag{2.24}$$

Now that we have an expression for all the voltages and currents, we can now replace them in 2.13 and 2.18, thus obtaining the expressions for the common mode voltages to be added

$$v_o^I = \left(\frac{cos(\phi_o)cos(\theta_i)(cos(\theta_i) - cos(\theta_i \mp \frac{2\pi}{3}))}{cos(\theta_o + \phi_o)} - cos(\theta_o) \right) V_o + cos(\theta_i \mp \frac{2\pi}{3}) V_i \tag{2.25}$$

$$v_o^{II} = \left(\frac{cos(\phi_o)cos(\theta_i \pm \frac{2\pi}{3})(cos(\theta_i \pm \frac{2\pi}{3}) - cos(\theta_i \mp \frac{2\pi}{3}))}{cos(\theta_o \pm \frac{2\pi}{3} + \phi_o)} - cos(\theta_o \pm \frac{2\pi}{3}) \right) V_o + cos(\theta_i \mp \frac{2\pi}{3}) V_i \tag{2.26}$$

which are valid only if $[-\frac{\pi}{6} < \phi < \frac{\pi}{6}]$.

Now, we can evaluate the maximum voltage transfer ratio. The analysis is restricted to

$$\theta_o \in [0, \frac{\pi}{3}], \theta i \in [0, \frac{\pi}{3}]$$
$$v_{o2}^* + v_o^I < v_{i2}$$

but it's applicable to all the other cases.

In this interval it follows that

$$v_{o1}^* + v_o^I < v_{i1} \tag{2.27}$$

$$v_{o3}^* + v_o^I > v_{i3} \tag{2.28}$$

Since we already know the expressions for all the voltages in 2.27 from 2.20, 2.22 and 2.25, we can rewrite the expression as

$$\sqrt{3} \left(cos(\theta_i + \frac{\pi}{3}) \right) \frac{(V_i cos(\phi_o + \theta_o) + V_o cos(\phi_o) cos(\theta_i))}{cos(\phi_o + \theta_o)} < 0 \tag{2.29}$$

being $cos(\theta_i + \frac{\pi}{3})$ and $cos(\phi_o + \theta_o)$ always positive in the aforementioned interval, we can rewrite it as

$$\frac{V_o}{V^i} < \frac{cos(\phi_o + \theta_o)}{cos(\phi_o)cos(\theta_i)} \tag{2.30}$$

which is the expression of the VTR.

The maximum value of the VTR that respects 2.27 is then found numerically. By applying the same steps it can also be found the maximum VTR respecting 2.28.

Thus said, for each angle ϕ_o, the lowest VTR will be the one that can be obtained in order to obtain a balanced three phase output. In this way it is possible to obtain the Calvini Modulation operative range, which is reported in Fig. 2.3.

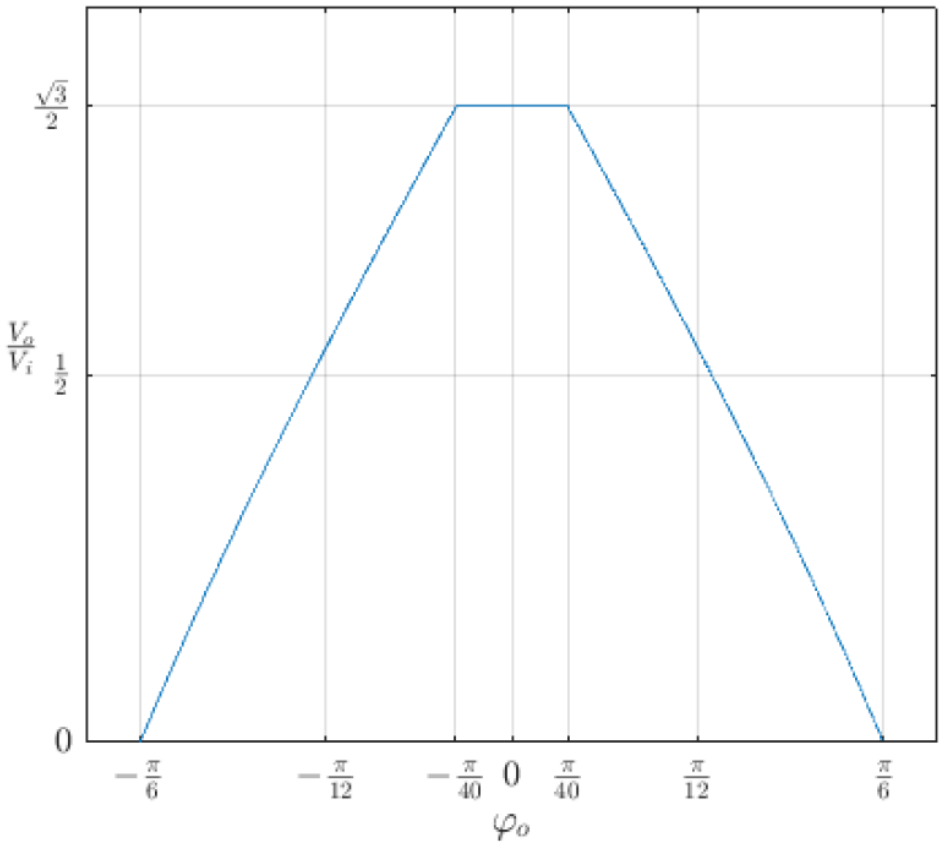

Figure 2.3: Voltage Transfer Ratio with Calvini modulation

.

It is evident that this new modulation technique is capable of obtaining the same VTR permitted by the Venturini's method, but the choice of always switching between the closest input phases narrows the output current displacement angle limits at which it is obtainable.

2.4 Hybrid Venturini-Calvini modulation

From the practical point of view, the Calvini Modulation is capable, when pushed to VTR limit, only of feeding an almost purely resistive load, and, in any cases, its VTR decreases very rapidly with the decrease of the output current power factor. In order to (partially) retain the advantages of the reduced switched voltage while extending its operative range, it was chosen to "assist" the Calvini's modulation with the Venturini's.

Basically the idea is to get the advantages of both modulations by adding the Calvini's common mode voltage were applicable, and then switching to the Venturini's one when outside of the Calvini's range. In particular, whenever the modulation is running and applied to the converter, it is necessary to switch to Venturini's modulation if the sum of the common mode voltage and the voltage reference, computed with the aforementioned method, exceeds the maximum (or the minimum) input voltage.

This means, however, that the switching losses obtained with this method depend somewhat from the load characteristics.

In the following chapter this intermediate modulation technique will be evaluated for usage in the converter in object.

Bibliography

[Alesina and Venturini(1988)] A. Alesina and M. Venturini. Intrinsic amplitude limits and optimum design of 9-switches direct pwm ac-ac converters. In *PESC '88 Record., 19th Annual IEEE Power Electronics Specialists Conference*, pages 1284–1291 vol.2, April 1988. doi: 10.1109/PESC.1988.18273.

[Huber and Borojevic(1989)] L. Huber and D. Borojevic. Space vector modulator for forced commutated cycloconverters. In *Conference Record of the IEEE Industry Applications Society Annual Meeting,*, pages 871–876 vol.1, Oct 1989. doi: 10.1109/IAS.1989.96746.

[Pipolo and Formentini(2019)] S. Pipolo and A. Formentini. A new modulation approach for matrix converter. In *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, pages 1021–1027, May 2019.

Chapter 3

Top-Level converter design

3.1 Matrix converter diffusion

At the current time, Matrix Converters did not receive the favors of the industry and are rarely seen outside the research laboratories. This can be due to the fact that they present a relatively complex topology when compared with the alternative solutions, and also due to the fact that, until now, they were not cost-competitive.

In fact, with regard to the mostly impacting components, in terms of economic costs, a matrix converter requires 18 power transistors and 18 power diodes, whether a back-to-back converter requires only 12 power transistors and 12 power diodes. However, as mentioned in the previous chapters, a matrix converter requires a small second-order input filter just to reduce the input current harmonic distortion, whether a back-to-back converter requires large input inductors and even larger DC-link capacitors.

Nowadays, the price of power semiconductors are steadily dropping year by year, while the costs of reactive elements is remaining stable. The author and his colleagues found that, at the start of the development of their matrix converter, the price for a back-to-back converter of the same power rating would have been comparable.

3.2 Commercial availability

The world's first commercial Matrix Converter, for the low voltage variable-frequency drives (VFDs) market, was manufactured by Yaskawa Electric in 2005 and presented with the name of "Varispeed AC", implemented with $1200V$ reverse-blocking Fuji IGBTs. The product was mainly advertised from Yaskawa for its bidirectional power flow capability and its performances in terms of total harmonic distortion.

One year later, in 2006, also Fuji Electric announced a Matrix Converter, presented under the name of "Frenic-MX", using, of course, their own semiconductors devices. Fuji, however, did not heavily advertise the product and retired it from its products portfolio shortly after. Currently Fuji does not sell Matrix Converters to the public.

Yaskawa Electric, on the contrary, extended their Matrix Converter product line in the medium voltage market ($3.3kV$ to $6.6kV$, $2.5MW$ to $5MW$, obtained by means of interconnecting multiple three-phase Matrix Converters) and continued with the development and the improvement of its low-voltage drives, which peaked with the introduction of its latest U1000 Industrial Matrix Drive, which covers the $4-650kW$ power range.

Currently Yaskawa Electric its the only company which is present on the market with a Matrix Converter.

Figure 3.1: Yaskawa's U1000 family

3.3 Existing solution

A good starting point for the development of the new device is the analysis of the mechanical dimensions of Yaskawa's U1000 0930AUB, a $560kW$ Matrix Converter. This converter's "all-out" dimensions , as reported from the datasheet in Fig.3.2 , are roughly $1835mm[H]X1070mm[W]X445mm[D]$, for a total volume of $0.873m^3$and a total mass of $630kg$, resulting in a power density of $641\frac{kW}{m^3}$ and a volumetric power density $0.888\frac{kW}{kg}$.

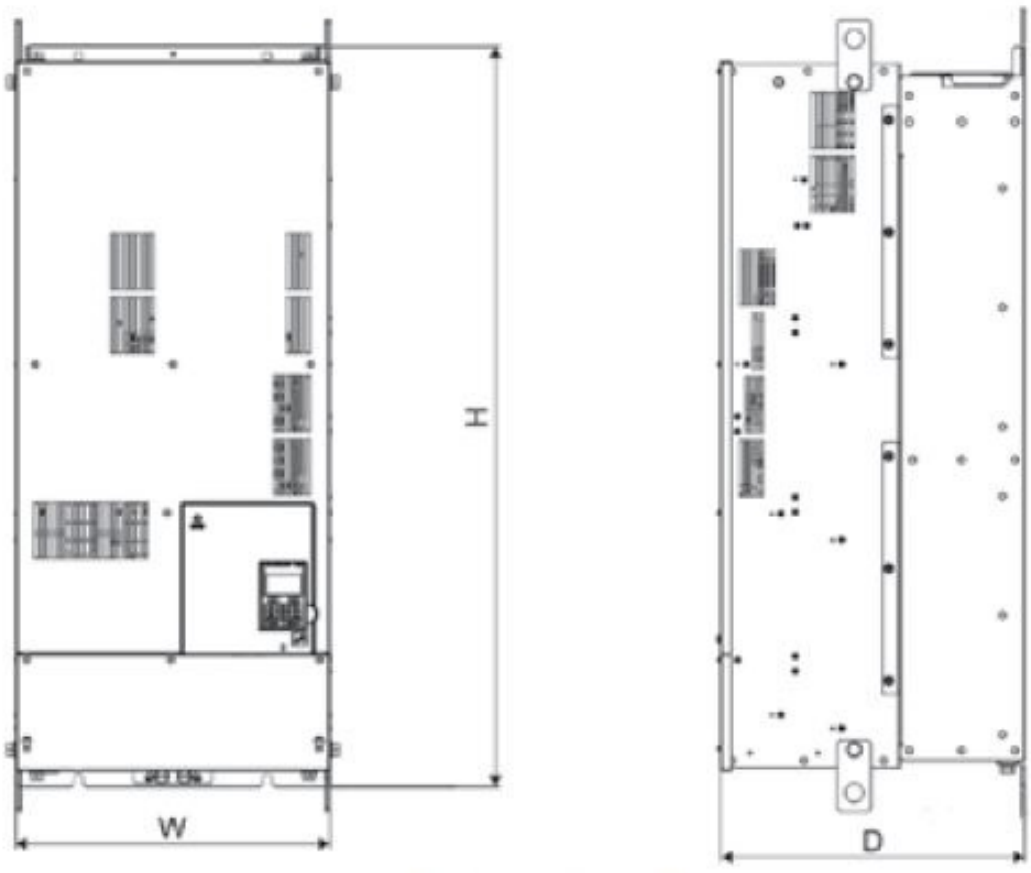

Figure 3.2: Yaskawa's Matrix Converter outer dimensions

The Yaskawa's converter uses forced air cooling and switches up to at a frequency of 4kHz, for a maximum fundamental output frequency of 400Hz. It already includes the clamp unit for over-voltage protection inside the frame and accepts an input voltage as high as $480V$ with a nominal output current of $900A$. However, U1000 0930AUB it does not include the PWM input filter EUJ711820M, which must be installed separately and which all out dimensions are roughly $1350mm[H]X700mm[W]X440mm[D]$, while its mass is $345kg$. This means that the most significant converter data when assembled can be represented by those of Tab 3.1.

Quantity	Value	U.M.
Rated power	560	kW
Total volume	1.289	m^3
Total weight	975	kg
Mass power density	434	$\frac{kW}{m^3}$
Volumetric power density	0.667	$\frac{kW}{kg}$

Table 3.1: Yaskawa's 560kW Matrix converter assembly data

No further construction details regarding this converter are known, neither the bandwidth of the current control loop.

3.4 Proposed solution

3.4.1 Overview

One of the goal of this thesis was to create a converter as small as possible, which could compete with the Yaskawa's solution in the $500kW$ power range. Furthermore, it was deemed necessary to give special care to the communication loop bandwidth, in order to decrease its delays that tend to decrease the bandwidth having in mind to develop a product ready for high-end single axis applications.

Considering these design constraints, as a first attempt it was decided that the converter would have been characterized by the following features :

- Input voltage from $380V_{rms}$ to $480V_{rms}$ ($400V_{rms}$ nominal)
- Nominal current $800A_{rms}$
- Water cooling, in order to maximize its power density
- Custom IGBT modules to enable a low leakage inductance layout
- Intelligent ad programmable gate driver with on-board fast acting protection systems and on-board measurements
- High-bandwidth fiber optic communication between gate drivers and control board

3.4.2 Power quality and loss estimation

In chapter 2 we presented the Hybrid modulation technique, but before deciding if implementing it or not in our converter, a comparison with the traditional Improved Venturini's modulation is due.

To compare the power quality and the losses between the Venturini's modulation and the Hybrid modulation, it is necessary to choose a load that, for convenience, can be considered representative of a typical single-axis high power application, like a permanent magnet synchronous motor with stator inductance $I_{rms} = 800A$ $L_s = 100\mu H$, stator resistance $R_s = 0.24\Omega$ and top speed (in field weakening region) $\omega_{max} = 3500rpm = 550rad/s$.

This would result, at top speed, in having a $cos\phi$ equal to

$$\phi = tan^{-1}\left(\frac{\omega_{max}L_s}{R_s}\right) = 0.16rad$$

which is a value valid for the Hybrid modulation since

$$0.52rad \approxeq \frac{\pi}{6} > \phi > \frac{\pi}{40} \approxeq 0.0785rad$$

After that, it is necessary to choose a non ideal IGBT, the same that will be then used for the converter's design in the following chapter, the IGC193T120T8RM from Infineon. A first-attempt switching frequency of $12kHz$ (for reactive elements evaluation) is then chosen on the basis of the criteria of having equal conduction and switching losses, if those would happen in a back to back converter. In addition, to drive these IGBTs, a commutation pattern must be chosen along with a feasible dead time, i.e. 4 step current commutation [[Deng(2014)]] and $1\mu s$.

To evaluate the actual behavior of the converter, also an input filter must be considered. According to [[Trentin and Zanchetta(2012)]] it was chose to use a capacitance of $300\mu F$ and a $5\mu H$ line inductance with parallel damping resistor of $500m\Omega$ assisted by the already available grid impedance, estimated to be around at least $15\mu H$ in series with $40m\Omega$. This results in a filter configuration like the one that can be seen in Fig.3.3.

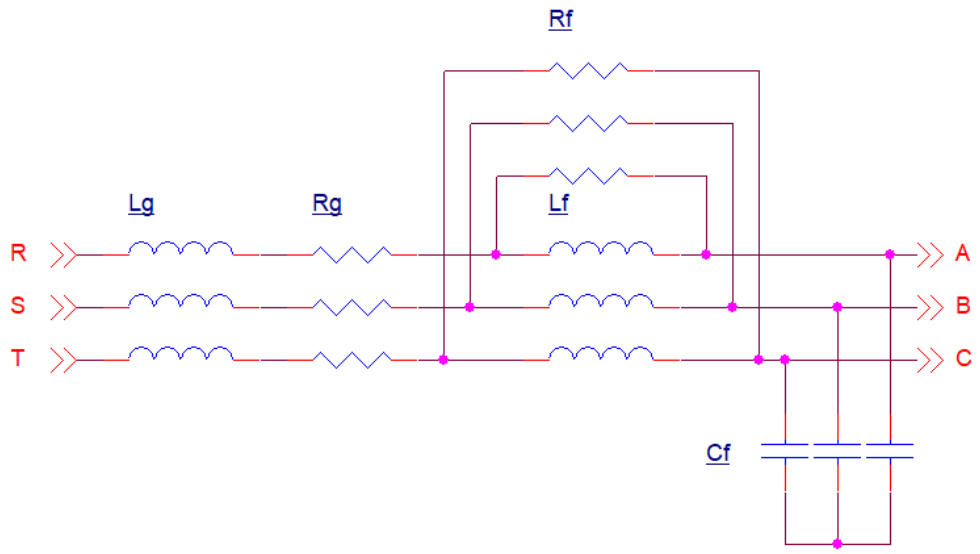

Figure 3.3: Proposed Matrix Converter line filter configuration

The VTR is then set to the maximum achievable value of $\frac{\sqrt{3}}{2}$in order to evaluate the worst-case conditions.

Usually the reason for increasing switching frequency is to reduce ripple and, consequently, harmonic distortion, in order to satisfy the requirements of the regulations on power quality. In the light of the above, a simulation in the MATLAB environment is then run comparing both the modulations for the same input current THD, which occurs at different switching frequencies. It must be noted that, whenever switching between the two modulations is not required, i.e. when it is possible to always compute the duty cycles with the Calvini's modulation technique, both Venturini's and Calvini's modulation obtain the same results in terms of distortion. However, this is not the case that was analyzed, and, due to the introduction of the "modulation switching" non linearity in the hybrid technique, the harmonic content is worsened. This means that with the hybrid technique it will be necessary to increase the switching frequency in order to obtain the same THD of the Venturini's modulation.

In Fig.3.4 it is shown the FFT of grid input current obtained with the Hybrid modulation, with a switching frequency of $10kHz$ for a THD% of 8.48%. It can be noted that the

most relevant contribution to the THD% is located at the cutoff frequency of the input filter, while the highest harmonic introduced by the Hybrid technique is located at 5th harmonic of the fundamental frequency.

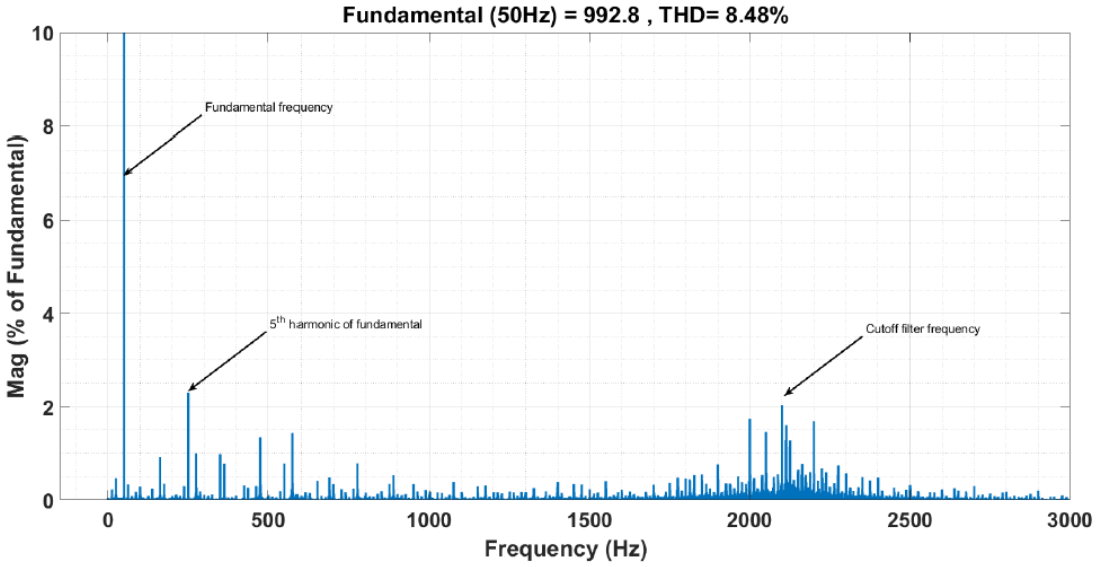

Figure 3.4: Simulation results of grid input current FFT with Hybrid modulation

In Fig.3.5 it is shown instead the FFT of grid input current obtained with the traditional Venturini's modulation, which obtains the same THD of 8.48% with a switching frequency of $7.1kHz$. Also for Venturini's modulation, the most relevant contribution to the THD% is located at the cutoff frequency of the input filter, with the highest harmonic due to the modulation itself located at 5th harmonic of the fundamental frequency.

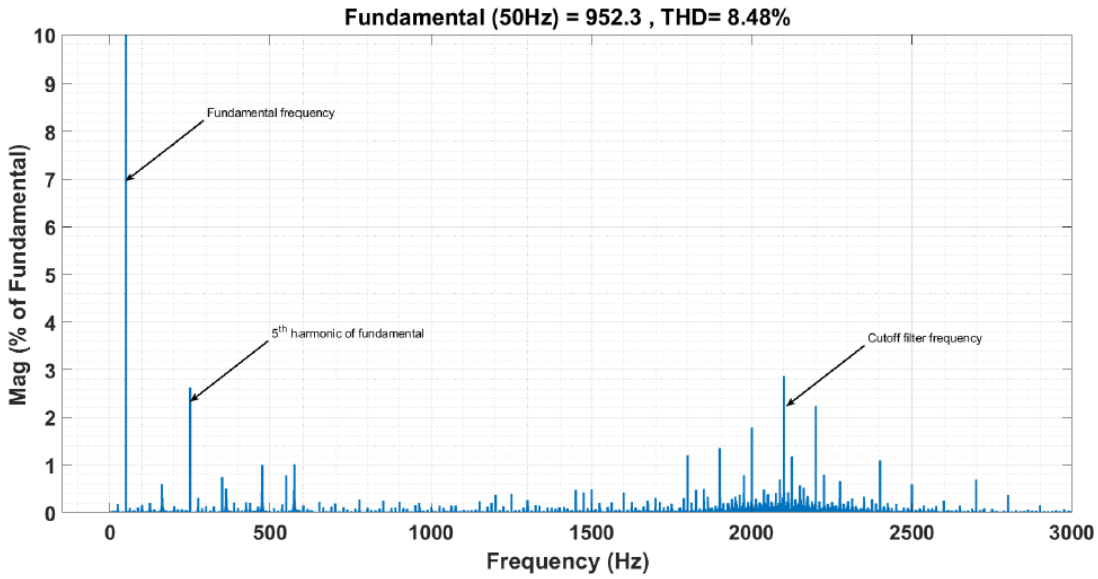

Figure 3.5: Simulation results of grid input current FFT with Venturini's modulation

The output currents are then evaluated in the same operating points, and shown in Fig.3.6 and Fig.3.7. The two results are very close to each other, but it can be stated that the Hybrid modulation performs better in this terms. The main reason behind this lies into the higher switching frequency, which reduces the current ripple in the load.

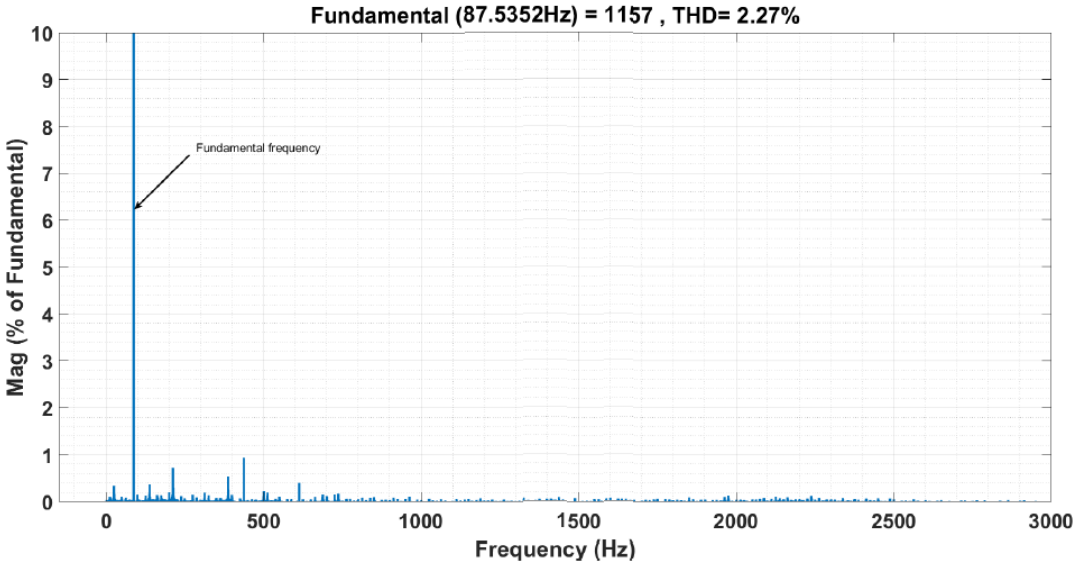

Figure 3.6: Simulation results of output current FFT with Hybrid modulation

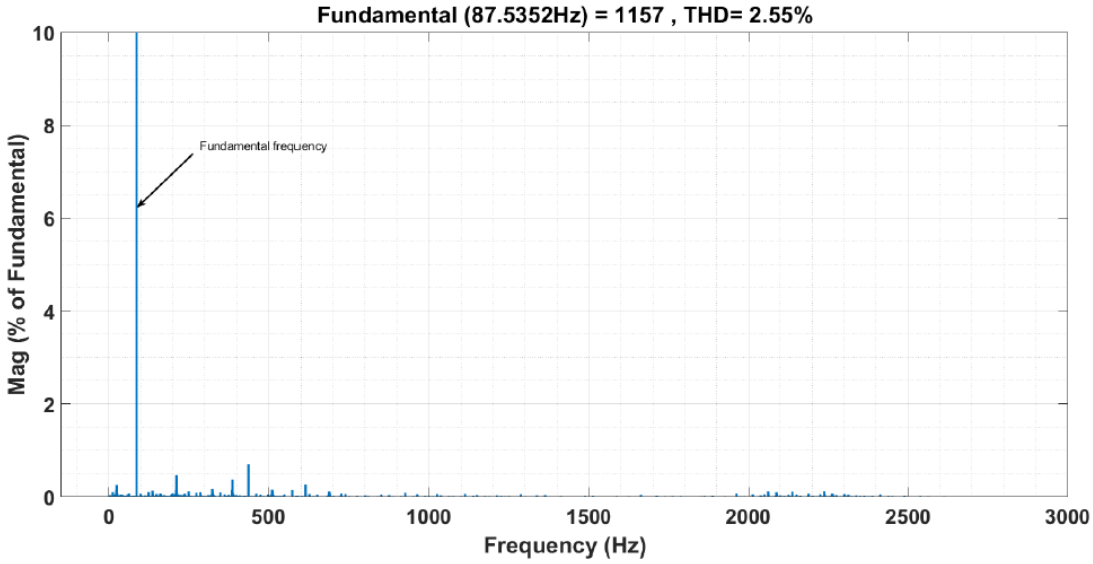

Figure 3.7: Simulation results of output current FFT with Venturini's modulation

Last, it is essential to evaluate the losses in the semiconductors with the two aforementioned modulation techniques, since they are needed to design the thermal management part of the converter.

In Fig.3.8 is reported a comparison between both conduction and switching losses with the two different techniques. Since the current which feeds load is the same for both techniques, it does not surprise that the conduction losses are quite similar for both approaches. In fact, the type and number of devices simultaneously in conduction does not change between the two modulation strategies, with current flowing in two switches, i.e. two IGBTs and two diodes. On the contrary, since the proposed approach acts on the closest input voltages rather than of using all three phases voltages, the switching losses are significantly reduced. In the end, the new approach attains a 3.5 kW of switching losses versus 5.8 kW of traditional modulation, and so it was decided to use it in our converter.

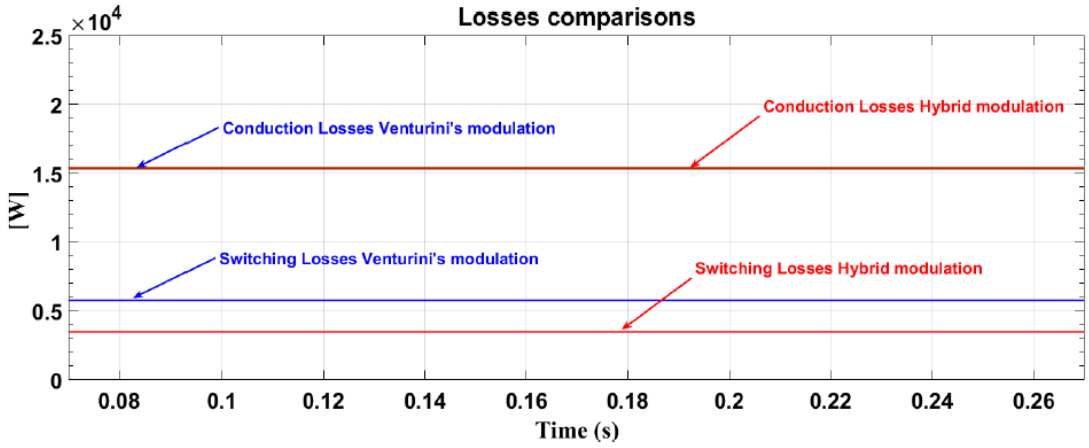

Figure 3.8: Simulation results of the losses in the semiconductor devices

3.4.3 Ratings and main components parameters

All this considered, it was evaluated convenient to split the machine in multiple $250kW$ modules, in order to cover different power sizes with the same product. Please note that from now on, if not made explicit, all the considerations regarding the converter will be related to the single $400A_{rms}$ module.

Following the same process of section 3.4.2, the main electrical values were evaluated for the 250kW size and are presented in Tab 3.2 and Tab 3.3.

Quantity	Value	U.M.
Nominal voltage	400	V_{rms}
Maximum working voltage	480	V_{rms}
Nominal output current	400	A_{rms}
Nominal maximum output voltage	415	V_{rms}
Nominal Switching frequency	16	kHz
Maximum Switching frequency	32	kHz
Maximum output frequency	2	kHz

Table 3.2: Matrix Converter 250kW module ratings

Name	Description	Value
Lg	Grid inductance (estimated)	15μH
Rg	Grid resistance	40$m\Omega$
Lf	Filter inductance	10μH
Rf	Filter damping resistor	1Ω
Cf	Filter phase-to neutral capacitance	180μF

Table 3.3: Matrix Converter 250kW module filter parameters

Bibliography

[Deng(2014)] Y. Guo W. Deng. An improved 4-step commutation method application for matrix converter. In *2014 17th International Conference on Electrical Machines and Systems (ICEMS)*, pages 3590–3593, Oct 2014. doi: 10.1109/ICEMS.2014.7014112.

[Trentin and Zanchetta(2012)] A. Trentin and P. Zanchetta. Automated optimal design of input filters for direct ac/ac matrix converters. *IEEE Transactions on Industrial Electronics*, 59(7):2811–2823, July 2012. ISSN 1557-9948. doi: 10.1109/TIE.2011.2163283.

Chapter 4

Converter design

4.1 Overview

In the following paragraphs the principal design decisions will be presented. The converter can be divided mainly in two macro components, that is the power stage and the control system.

Anyways, our objective will be to optimize the converter as a whole entity, and not the single components, so many dimensioning criteria will be linked together.

4.2 Power Stage

4.2.1 Power stage architecture

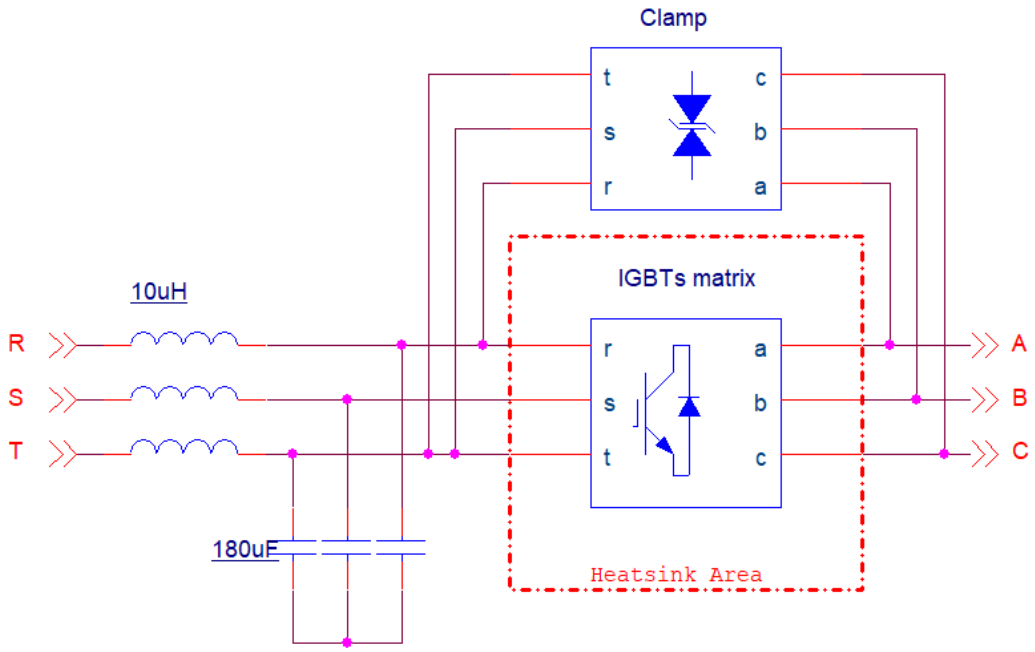

Figure 4.1: Power Stage high level schematic

Fig.4.1 is an high level schematic of the main power stage components that had to be designed for our converter. Please note that the Rf damping resistor is absent since it was chosen to incorporate it inside the inductor, as it will be explained later.

The power comes from the three-phase grid and passes through the L-C input filter, which is responsible for reducing the THD% induced in the grid.

After the filter we encounter the input side of the actual Matrix Converter, consisting in 9 bidirectional switches.

On the load side of the Matrix Converter we directly find the load with no further inductance added in series, since the load itself is typically inductive in its nature.

Last, a clamp unit is put in parallel with the load, and it also presents a connection with the input side of the Matrix Converter for system startup (details will be discussed further).

4.2.2 Matrix Converter layout

The first and most basic decision revolves around the actual semiconductor devices to be used in the Matrix Converter.

Due to the current. frequency and voltage levels of our converter, it was deemed necessary to create the bidirectional switches with the switch topology involving two IGBTs and two diodes.

Two custom modules were then produced by Semikron for this specific application, composed by three star-connected IGBTs, each in series with a diode, one module in common emitter configuration and one module in common collector configuration.

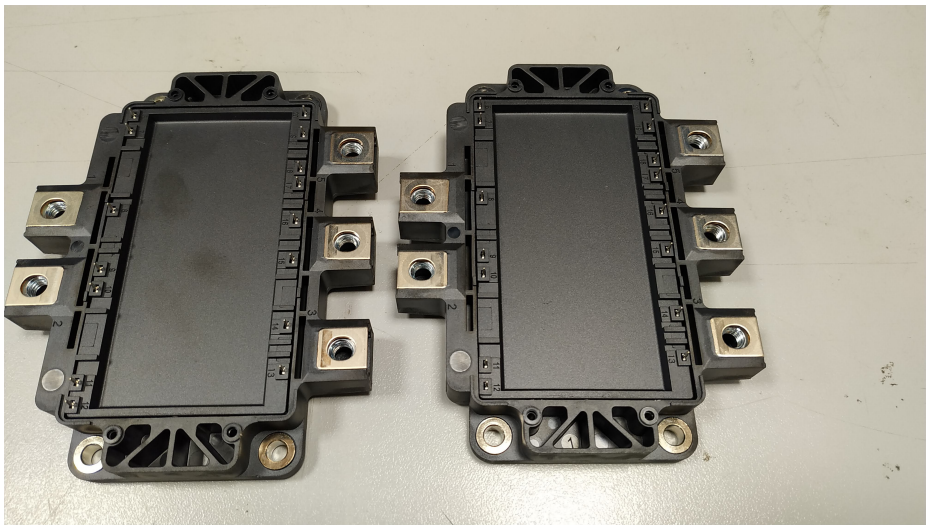

Figure 4.2: Semikron custom Matrix AXT and AXB modules

This unusual configurations, as we will discuss later, of course increases the number of isolated power supplies needed for the operation of the gate drivers, but also permits to fully exploit the internal space available inside of a standard Semix5 package.

In actual fact, inside the module, each IGBT is composed by two paralleled Infineon IGC193T120T8RM IGBTs and each diode is composed by eight paralleled Infineon SKCD31C120I4F diodes. Fig.4.3 and Fig.4.4 show the dies of the aforementioned components, along with their most relevant mechanical dimensions.

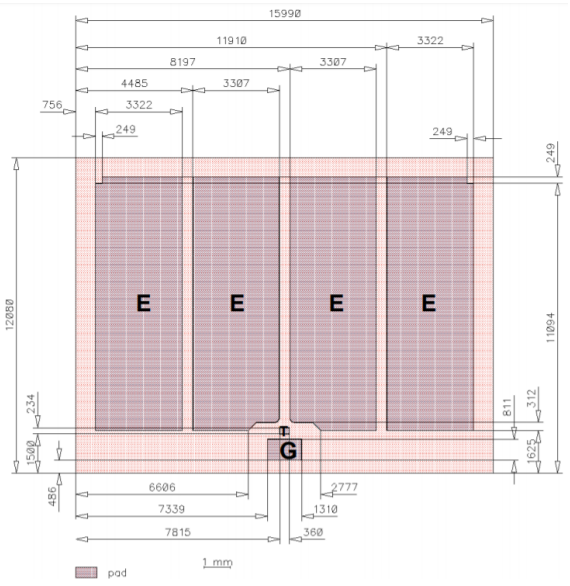

Figure 4.3: IGC193T120T8RM die

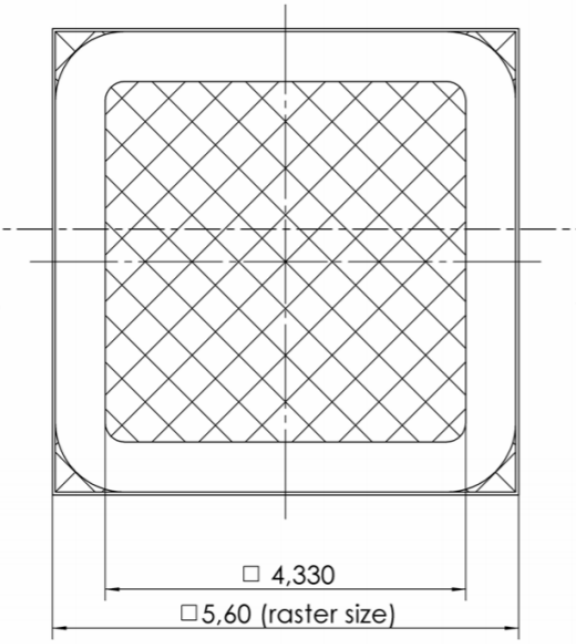

Figure 4.4: SKCD31C120I4F die

In the light of the above, to obtain the desired matrix topology, it is necessary to use a common emitter module and a common collector module per output phase, for a total of six modules (Fig.4.5).

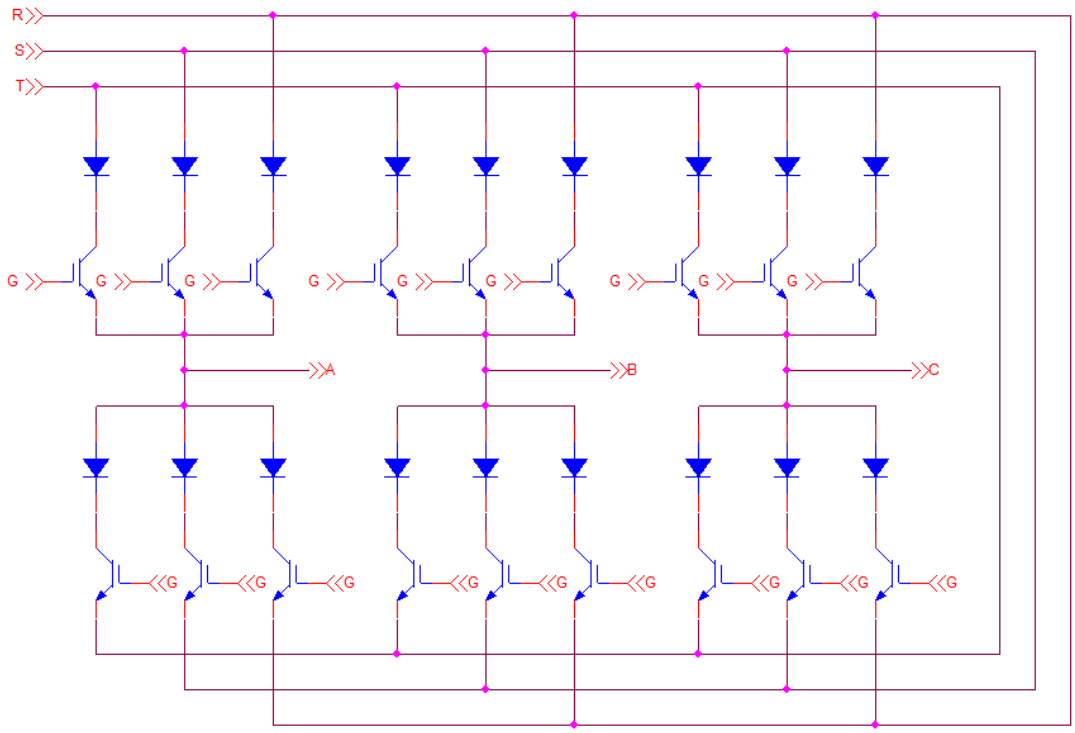

Figure 4.5: Actual matrix topology obtained with Semikron's custom power modules

4.2.3 Cold plate heat sink

Heat sinks, along with reactive elements, are usually among those components that are critical for the dimensions of a converter so, as mentioned in chapter 3, to obtain a high power density, it was chosen to use a water cooled plate, with mixture of water and ethylene glycol as coolant.

Due to the layout of the Semix5 modules, it was evaluated to be convenient to arrange them in a in-line, two layers fashion, with one layer formed by the common collector modules and the other formed by the common emitter ones. This way it was possible to cool the IGBTs with a single heat sink put in between the modules, and also to have the same output phases of the converter facing each other, thus simplifying the connections.

For this same last reason, it was also decided to put the water inlet and outlets on the same heat sink surface.

The core of a water-cooled cold plate lies in the design of the coolant circuit, which, for a given flow rate, has the aim to decrease as much as possible the convective thermal resistance $R_{th_{convective}}$ between the fluid and the surfaces of the ducts, all while obtaining a pressure drop Δp that should be as low as possible, since the flow losses, and so the work that has to be done by the plant's pumps, are proportional to it.

These two objectives, however, are in contrast to each other, since under the imposed constant flow rate condition :

$$R_{th_{convective}} \propto \frac{1}{u} \tag{4.1}$$

while

$$\Delta p \propto u^2 \tag{4.2}$$

where u is the velocity of the fluid. In general, for constant laminar flow rate

$$u \propto \frac{1}{A_w} \tag{4.3}$$

where $A_w$is the cross section of the duct.

However, another consideration that must be made is that, to reduce $R_{th_{convective}}$ and to have an homogeneous temperature distribution, it is beneficial to cover all the possible surface available under the modules. If, in order to increase fluid velocity, we want to cover the same cold plate surface with a narrow channel with low A_w, the channel length has to increase, and so the pressure drop accordingly. So, what we see is that, in this specific design, (2) becomes

$$\Delta p \propto u^3 \tag{4.4}$$

To worsen this situation further, is must be also taken into account that, for the same reasons, a longer channel means an higher number of U turns, and so higher concentrated

pressure drops. The system is strongly non-linear, but it is already clear from this surface-level analysis that it leans towards large and short water channels.

Last, a consideration from the manufacturing point of view: large and short channels can be realized with a limited number of passes of large milling tools.

In the light of the above, the cooling circuit was iteratively designed and optimized with the aid of PTC Creo CAD software and Menthor Graphic FloEFD CFD tool. Table 4.1 contains the constraints and requirements used for the design process, while Fig.4.6 presents the resulting channel layout, where it can be noted a cross-section enlargement in the turns, to reduce the pressure drops.

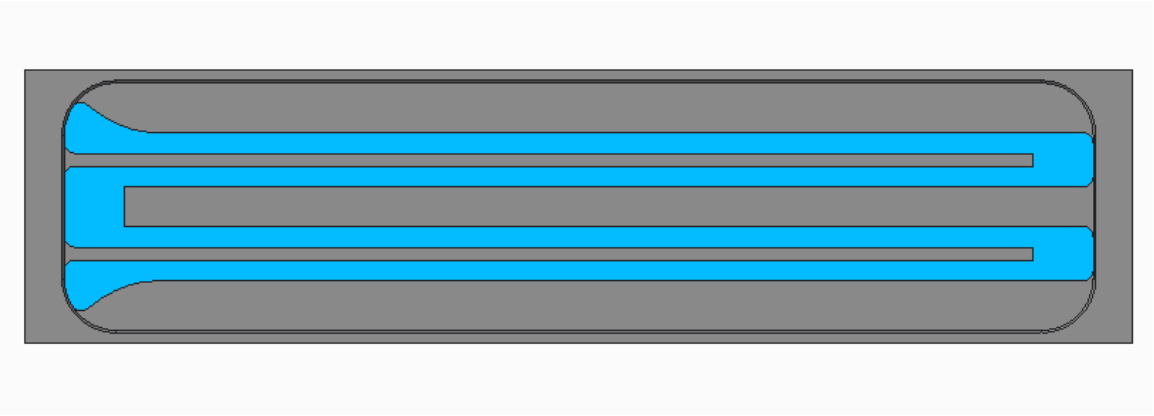

Figure 4.6: Proposed coolant circuit layout

Quantity	Value	U.M.	Source
Heat generated per module	1000	W	Loss analysis
Target maximum surface temperature	75	$°C$	Semix5 thermal data
Nominal coolant flow rate	2.78	$\frac{m^3}{s}$	Industry standard
Target maximum pressure drop	30	kPa	Industry standard
Target maximum channel-to-ambient pressure	500	kPa	Industry standard
Inlet fluid temperature	40	$°C$	Industry standard
Water/ethylene glycol ratio	1 : 1	$unitless$	Industry standard

Table 4.1: Heat sink design data

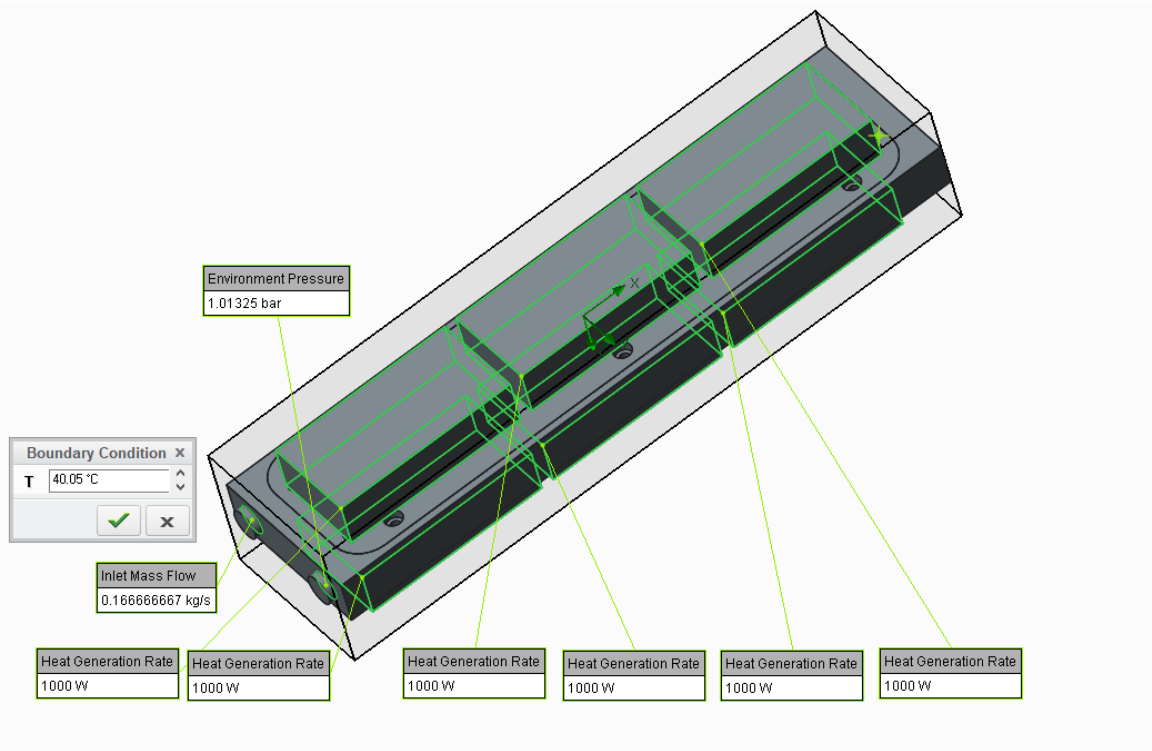

Figure 4.7: Cold plate CFD model with highlighted boundary conditions

Fig.4.7 represents the model used in the simulation, along with its boundary conditions. To speed up the simulation, the Semix5 are not represented and are replaced with their thermal pad footprint, and neither gravity nor heat radiation were considered, since the former is not influential, while neglecting the latter is both conservative and only marginally influential. In Fig.4.8 it can be seen the fluid temperature distribution , while the static pressure distribution is presented in Fig.4.9. Fig.4.10 and Fig.4.11 show the temperature distributions of both the cold plate surfaces.

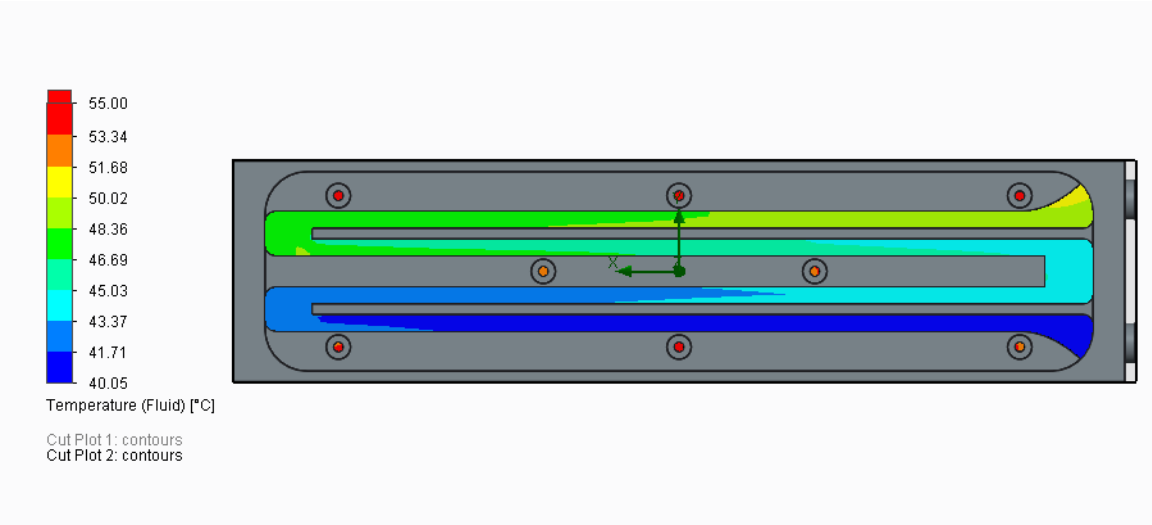

Figure 4.8: Coolant temperature distribution

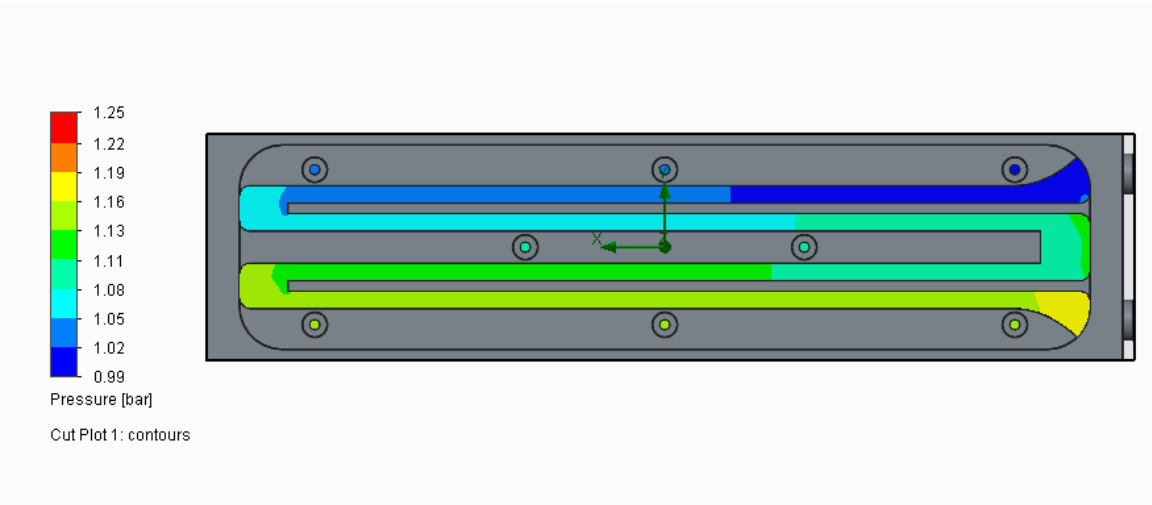

Figure 4.9: Coolant static pressure distribution

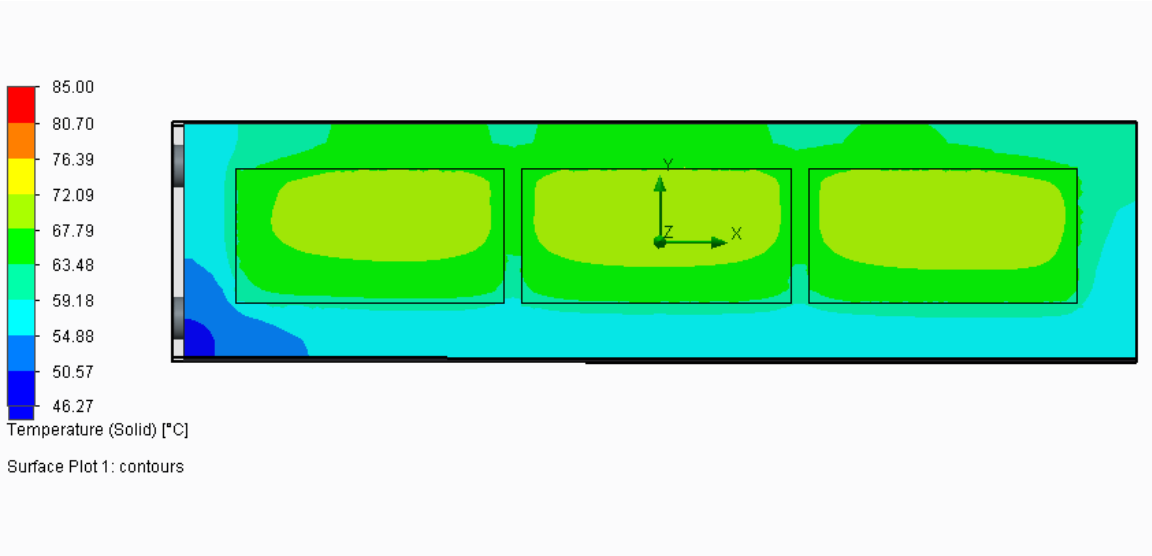

Figure 4.10: Temperature distribution on the surface of the receptacle

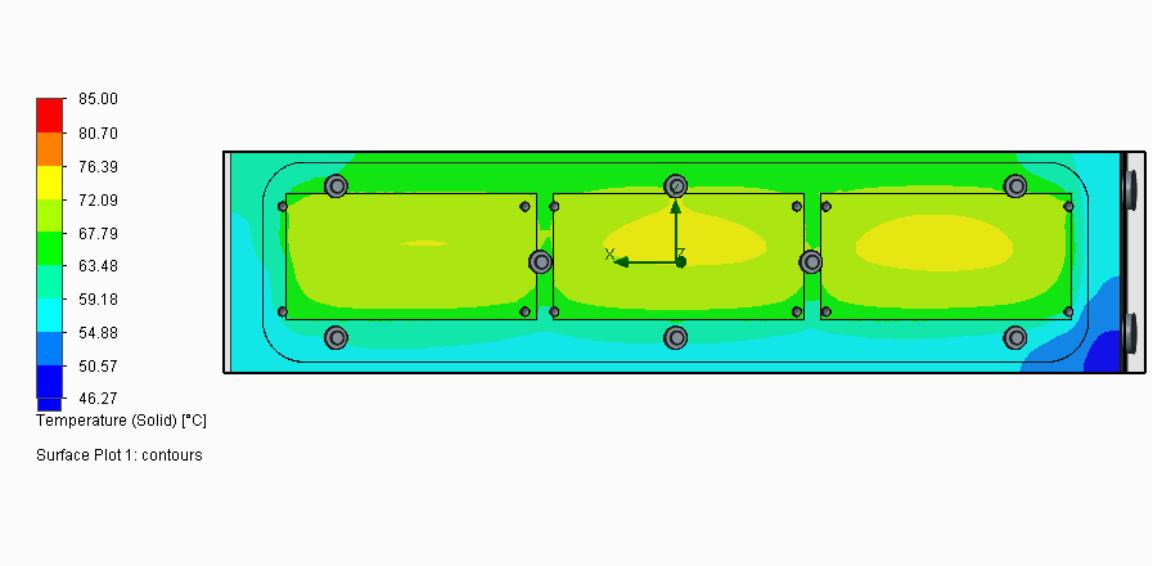

Figure 4.11: Temperature distribution on the surface of the cover

Fig.4.12 and Fig.4.13 show the two parts that form the heat sink, and also highlight the o-rings positions, used for guaranteeing the water tightness up to the required maximum channel-to-ambient pressure.

Fig.4.14 shows the resulting upper plate deformation under maximum channel-to-ambient pressure condition, which can be considered neglectable since its way smaller than the o-rings housing width.

Finally, the complete assembly, formed by both modules and heat sink, can be seen in Fig.4.15. Table 4.2 sums up the results.

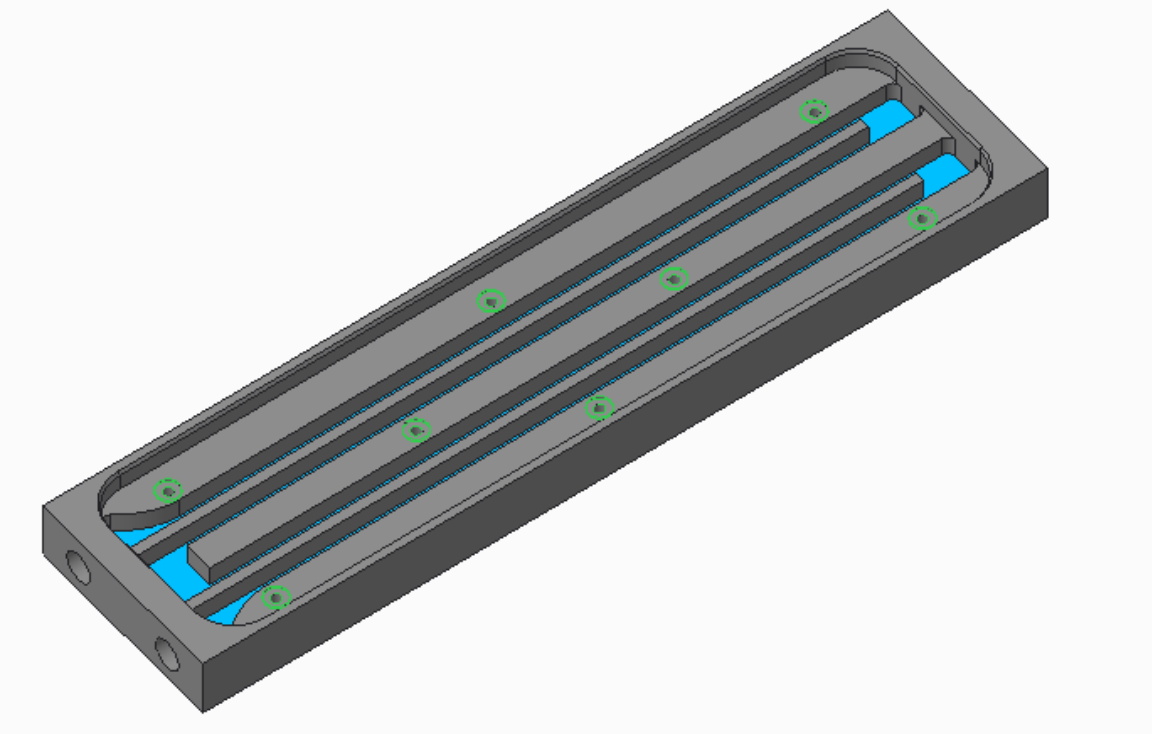

Figure 4.12: Cold plate receptacle wet area

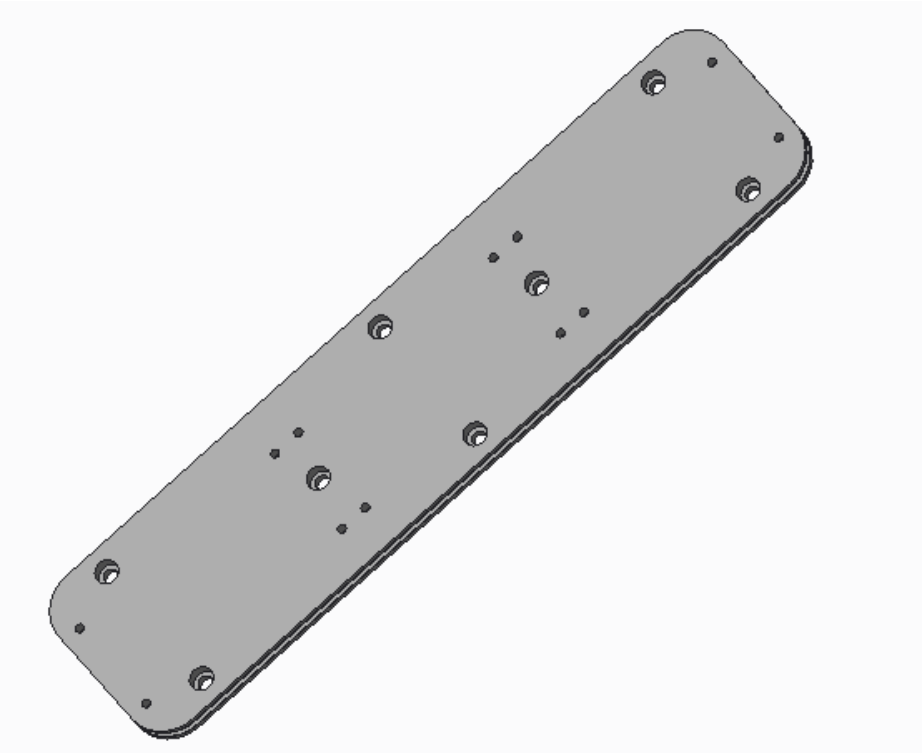

Figure 4.13: Cold plate cover

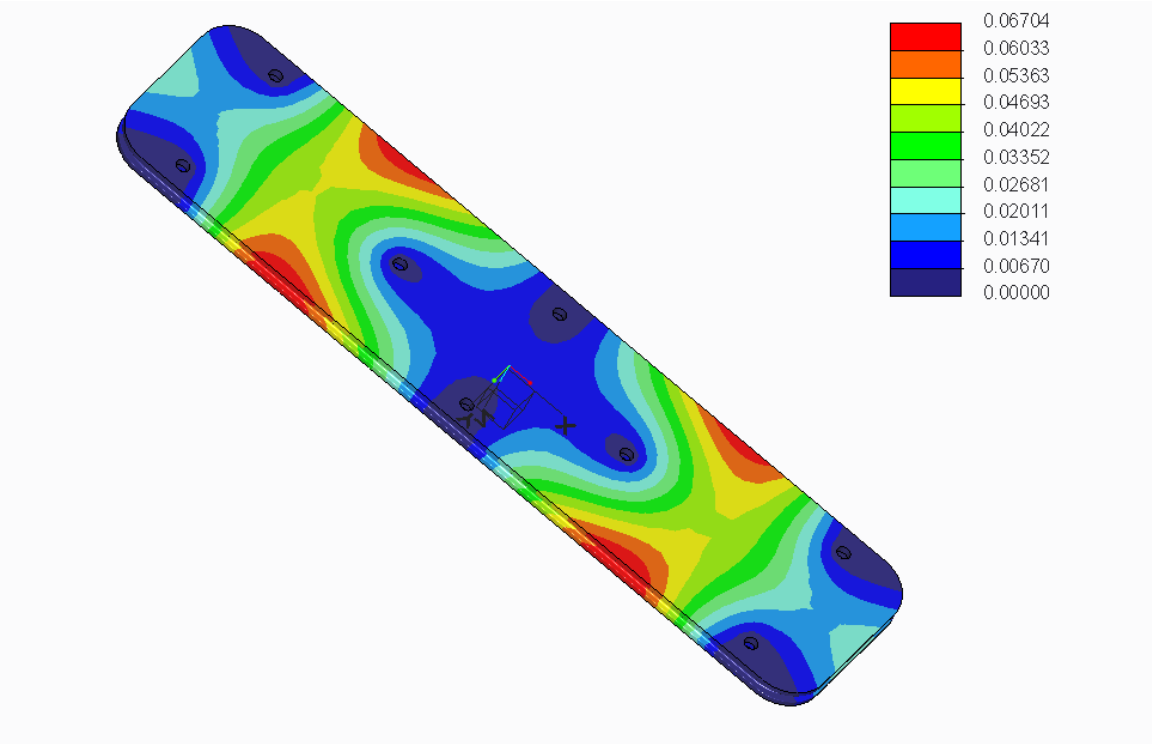

Figure 4.14: Displacement caused by water pressurized at 500*kPa*

Actual maximum surface temperature	71°*C*
Actual Maximum pressure drop	22*kPa*
Water tightness up to 500*kPa*	*Yes*

Table 4.2: Heat sink performances

Figure 4.15: Cold plate assembly

4.2.4 Input filter : capacitors busbar

The main challenge of the input filter design lies in minimizing the stray inductance between the IGBTs and the capacitors, while maintaining a space-efficient design. The target input capacitance value, as from table 3.2, was set at $180\mu F$ phase-to neutral.

It must also be considered that, in a matrix converter, AC-specific capacitors are needed to guarantee long-term reliability, which typically present a lower energy density with respect to DC ones.

That said, it was chosen to utilize ultra low-inductance, 480Vac, MKP1847H57048 and MKP1847H54048 capacitors from Vishay, arranged in a delta connection, thus reducing the necessary capacitance value to $60\mu F$.

To further minimize the stray inductance, it was chosen to directly solder the capacitors pins onto the copper busbars. In Fig.4.16 it is presented the solution implemented to enable soldering without thermal risks for the capacitors, since normally the busbar would require to be heated due to its good heat-sinking capabilities.

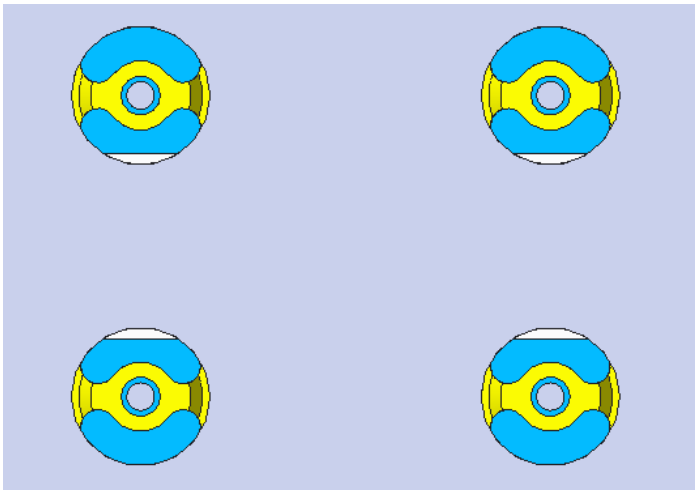

Figure 4.16: Capacitors direct soldering on busbar with thermal relief pad

The choice to mix the capacitance values was made for purely mechanical design reasons. This way, in fact, it was possible to put the smaller capacitors above the IGBTs, better exploiting the space available, as seen in Fig.4.17, and to fit the remaining capacitors behind the heat sink in two rows shorter than the heat sink itself.

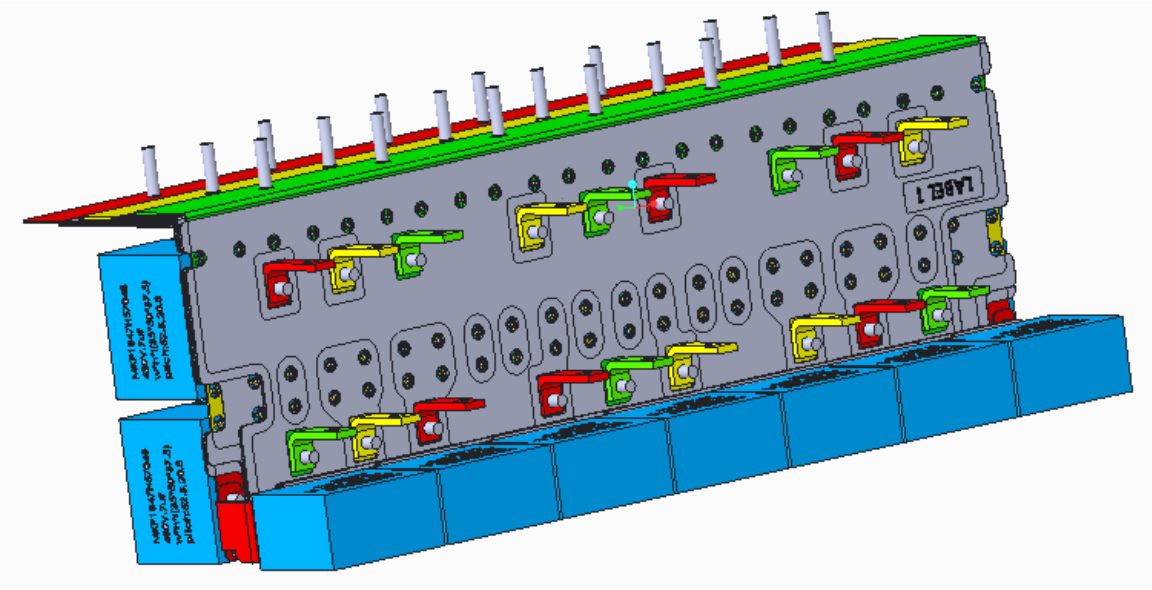

Figure 4.17: Busbar capacitors arrangement

It can be noted that the current paths that involve the smaller capacitors present a not negligible inductance value, due to their position being relatively far from the IGBTs. However, it was hypothesized that, for the suppression of the fastest transients, it could be sufficient the capacitance from the nearest capacitors only, which are separated from the IGBTs only by a copper bracket, as already shown in Fig. 4.17.

4.2.5 Input filter : Inductor

Magnetic components are usually the bulkiest one, since the known magnetic and conductive materials, when compared to the know dielectric materials, permit a lower energy density (this is one of the reasons for which the voltage impressed topologies are way more popular than the current impressed topologies), and so it was decided not to use commercial components. Instead, a custom inductor was designed for this application, and its dimensions were adapted to the mechanical layout of the previous components. The target line inductance was set to be $10\mu H$.

The author wanted to try to design a three-phase single turn feed-through inductor to achieve extreme easiness of assembly, and this desire leaded the necessity to create an

unusual magnetic core. For example, if we look among the standard three-phase cores, the most economical and compact one, which is the E core, is not suitable for designing a single-turn component. In fact, in a multi-turn inductor, copper is wound around the core's columns, which act as a mechanical support for the winding, like in Fig.4.18.

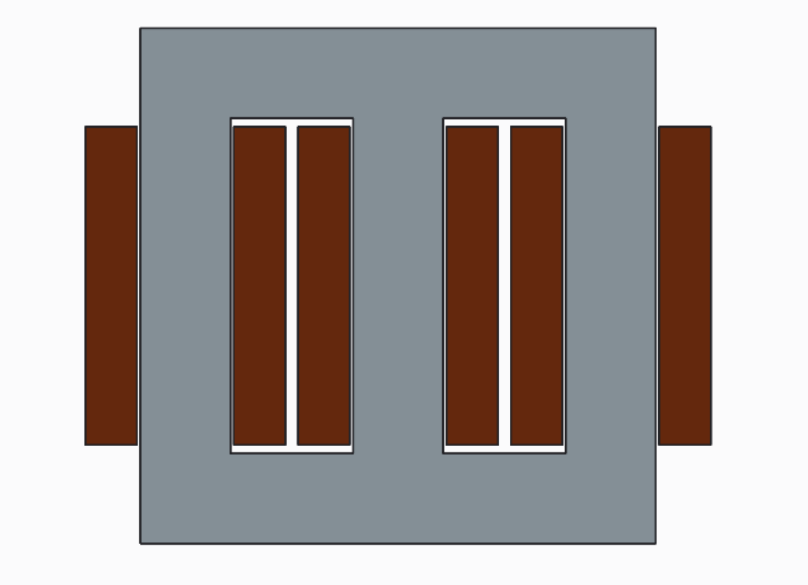

Figure 4.18: Traditional laminated E-core

This is not true for an inductor with a single bar that passes inside the core. A five-column shell core could have been used for this purpose, due to the presence of 4 winding windows, but it would have not been an optimal choice due to the fact that the fourth window would not have been utilized by the three phase system, and also to the fact that one of the bar would have had half cross section when compared to the others, due to the smaller external winding windows, as shown in Fig4.19. In addition, also the core iron would have been badly utilized due to the thinner outer limbs.

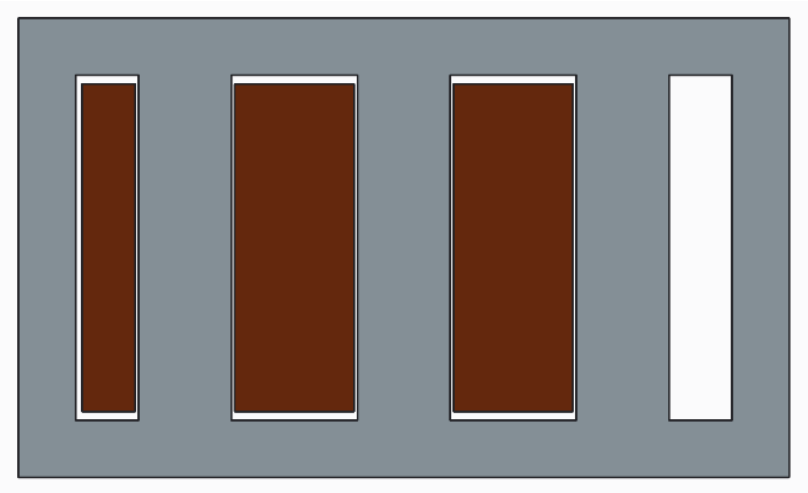

Figure 4.19: Traditional five-column shell core with three through bars

So it was conceived a 4 asymmetrical columns design to be obtained by custom laser cut of the lamination, which can be seen in Fig4.20.

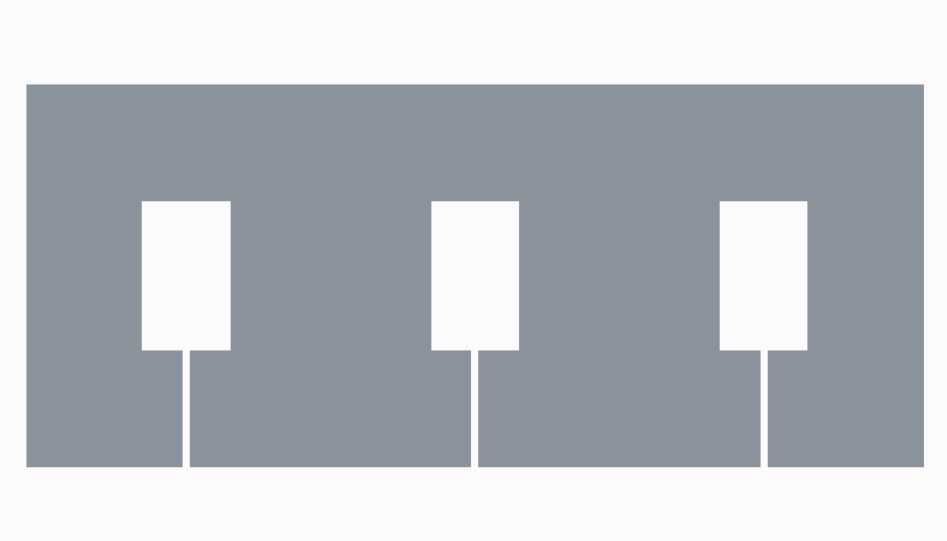

Figure 4.20: Custom 4 columns, through bars design

In this configuration we have the air-gaps in one of the yokes (and so the core does not need to be held together in place by an external frame) and $\phi_S$shares its path with $\phi_R$on one side and ϕ_T on the other.

Thus, the total flux in the two central columns is

$$\phi_1 = \phi_R + \phi_S \tag{4.5}$$

$$\phi_2 = \phi_S + \phi_T \tag{4.6}$$

and, since we are working with a symmetrical three phase system , assuming that the three line currents are balanced,

$$\phi_1 = \phi_M sin(wt) + \phi_M sin(wt + \frac{2\pi}{3}) \tag{4.7}$$

$$\phi_2 = \phi_M sin(wt) + \phi_M sin(wt + \frac{4\pi}{3}) \tag{4.8}$$

which leads to the solution

$$max|\phi_1| = max|\phi_2| = \sqrt{3}\phi_M \tag{4.9}$$

This leads to the necessity of having the two central columns $\sqrt{3}$ times larger than both the outer columns and the yokes.

However, this 4 columns solution is more advantageous when compared to using three single phase inductors, since it uses a fraction of the iron for the columns, which is

$$\frac{2+2\sqrt{3}}{6} = 0.91 \tag{4.10}$$

Let us proceed now with the actual dimensioning of the 4 column inductor.

Normally, in air-cooled power inductor design, the design input data (actual values reported in brackets) are

- Inductance value $(10\mu H)$
- RMS current value $(400A)$
- Peak-to-peak ripple or actual harmonic content (taken from simulations of chapter 3)

- Peak current value before saturation $(570A)$

While the constraints are limited to

- Maximum hot spot temperature $(100°C)$
- B<Bsat

And the degrees of freedom are :

- Core columns width
- Core depth
- Number of turns
- Winding window height
- Winding window width
- Core material

However, in addition to restrict the number of turn to 1, the author did not want to exceed the “all-out” height and width already determined by the assembly formed by the IGBTs on their cold plate and the busbar.

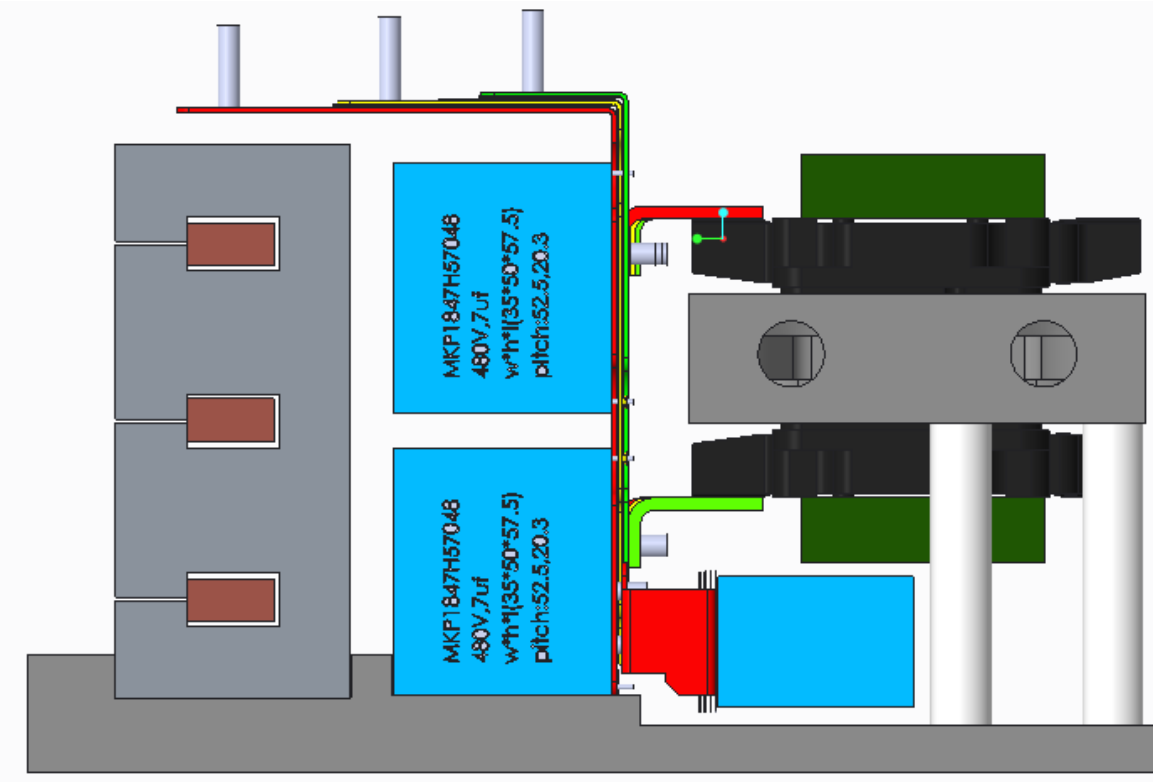

Figure 4.21: Custom inductor positioning

Since it was deemed convenient to place the inductor as in Fig.4.21, the constraint list was modified, with the actual values for the calculations reported in brackets :

- Hot spot temperature $<100°C$
- $B < Bsat$
- $(3WindingWindowWidth) + \left(2+2\sqrt{3}\right)CoreColumnsWidth = AssemblyHeight$ $(455mm)$
- $CoreDepth < AssemblyWidth$ $(200mm)$
- $NumberOfTurns$ (1)

And the degrees of freedom were reduced to :

- Core depth

- Winding window height
- Winding window width
- Core material

The outcome of the process lead us to the core lamination that can be seen in Fig.4.22. The drawing also reports the stack length and the chosen material. Due to the supposed low harmonic content of the input current, and thanks to the use of Fe-Si, which is a lossy material when compared to powdered iron or ferrite, it was possible to maintain an high value of B, reduce overall dimensions and remove the parallel damping resistor.

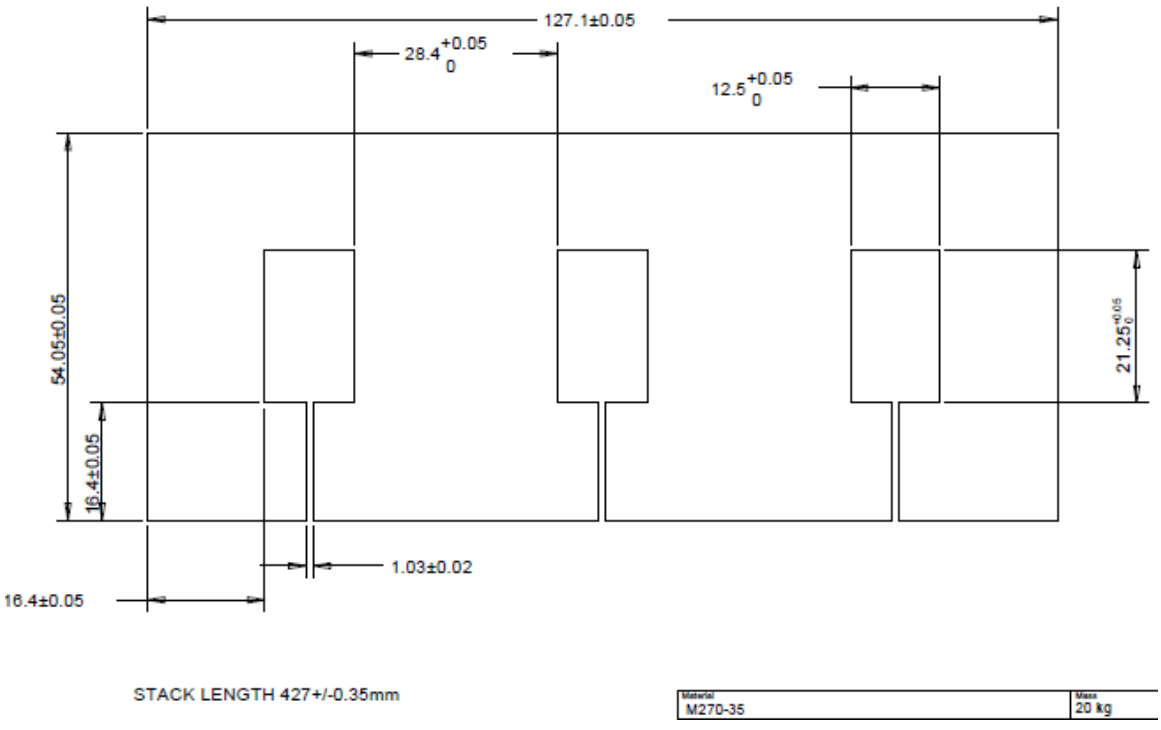

Figure 4.22: Custom inductor lamination with actual dimensions

This inductor was then analyzed with the Finite Element Method in Ansys Maxwell in order to verify core losses and copper losses due to skin effect and air gap flux fringing. Due to the geometry of the system, it was deemed necessary only to carry on a 2D FEM analysis. Fig.4.23 presents the results.

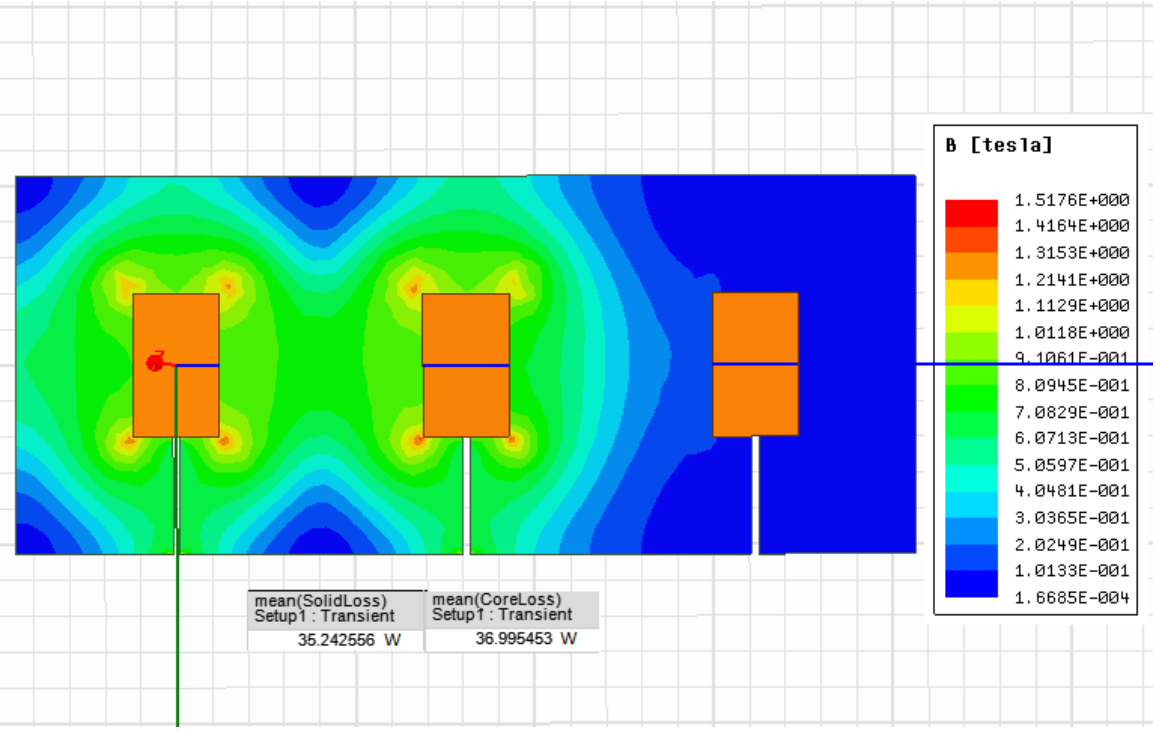

Figure 4.23: 2D FEM analysis of the custom inductor

In addition, a 3D model of the inductor was built in PTC Creo and put in the Matrix converter assembly, and a CFD analysis was performed with the aid of the FloEFD tool, with the aforementioned losses results taken from the electromagnetic simulation.

This was in order to verify the hot spot temperature in the inductor in the nominal conditions, that is :

- 40W lost in the iron
- 40W lost in the copper
- Ambient temperature 50°C
- Natural air cooling at sea level pressure
- No irradiation (conservative assumption that speeds up the simulations and gives only a small contribute at the supposed temperatures)

The results are shown in Fig.4.24, where it can be seen that the inductor temperature is lower than the predicted one, probably due to conservative assumptions regarding the convective heat transfer coefficient made in the design process.

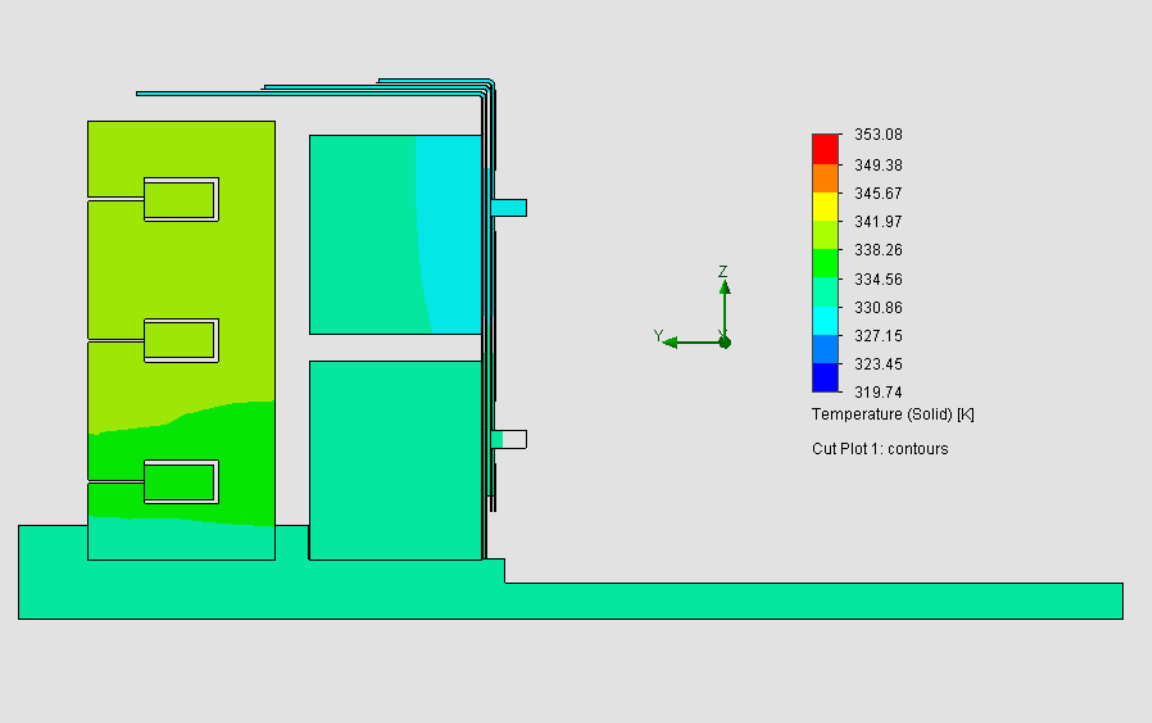

Figure 4.24: CFD analysis of the thermal behavior of the custom inductor

4.2.6 Clamp unit

As already mentioned, the clamp unit is an additional safety element that behaves passively during normal operation and becomes active during fault states.

In fact, in case of loss of control or sudden system shutdown, all the switches may open, leaving the current in the inductive load with no path to circulate in. This situation, if left uncontrolled, leads to severe over-voltages that can destroy the switches. The clamp unit can avoid this problem by providing local energy storage capabilities. Fig. 4.25 shows the principle schematic of the device.

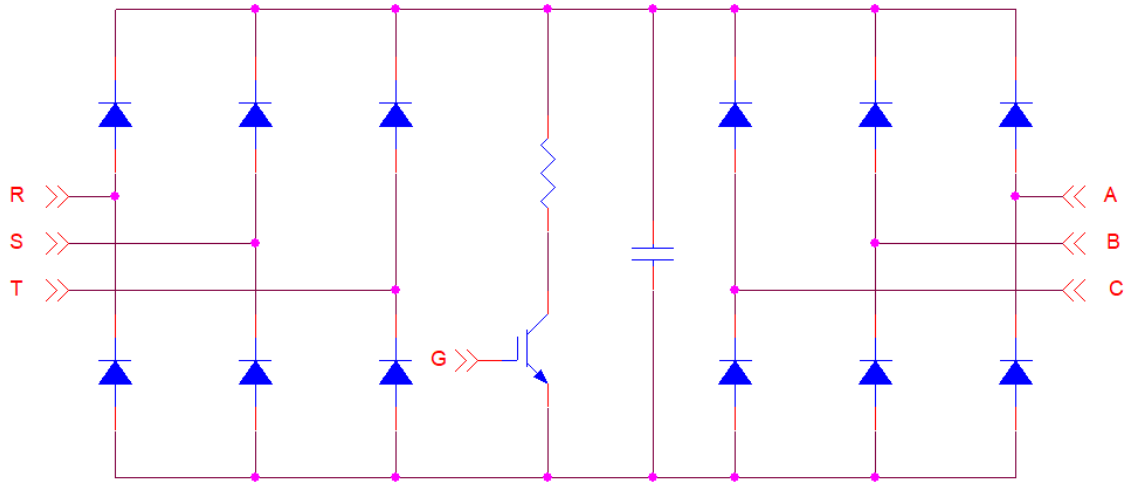

Figure 4.25: Matrix clamp unit schematic

The motor side three-phase diode bridge (D1-D6) is composed by Infineon IDM10G120C5 SiC diodes, in order to ensure a fast turn-on response during the over-voltage event. During this event, the clamp sensing stage detects if the voltage goes higher than the $900V$ threshold, and eventually turns on the clamp IGBTs in order to short the current onto the braking resistor. These kind of resistors, however, present a not-negligible inductance, ad so the transient over-voltage protection has to be done by the capacitors on the DC link, which must be able to safely soak up the energy of the motor's leakage inductance (we considered $50\mu H$ to be a reasonable value) at the converter's rated current ($400A_{rms}$) . Given this, at any given time, considering the motor a balanced three-phase load and the converter a balanced supply, since the power is constant, the magnetic energy stored in the motor amounts to :

$$E_{leak} = \frac{3}{2}\left[\frac{1}{2}L_{leak}\left(\sqrt{2}I_{rms}\right)^2\right] \tag{4.11}$$

this energy must be compared with that which can be stored in the aforementioned capacitors between the over-voltage detection threshold and the switches breakdown voltage, which is

$$E_{clamp} = \frac{1}{2}\left[C\left(V_{breakdown}^2 - V_n^2\right)\right] \tag{4.12}$$

$$E_{leak} \leq E_{clamp} \tag{4.13}$$

which leads to the value

$$C \geq 38.09\mu F \tag{4.14}$$

In the end, two $1200V$, $20\mu F$ capacitors were put in the clamp unit.

Regarding to the second diode bridge that is presented in the schematic, its purpose is safely precharging the DC link capacitors through a PTC resistor when the converter is connected to the grid.

In addition, the DC-link voltage is sensed by an isolated op-amp and made available to the control board, which is also able to trigger the clamp at will through an isolated input.

Last, it must be noted that, while the clamp unit has to be powered by a 12V external supply to be fully operational, the detection and clamping functions can be carried out also in case of loss of supply, with the board getting the required power from the sensing stage itself.

4.3 Control system

4.3.1 Control system layout

The proposed layout is shown in Fig.4.26 .

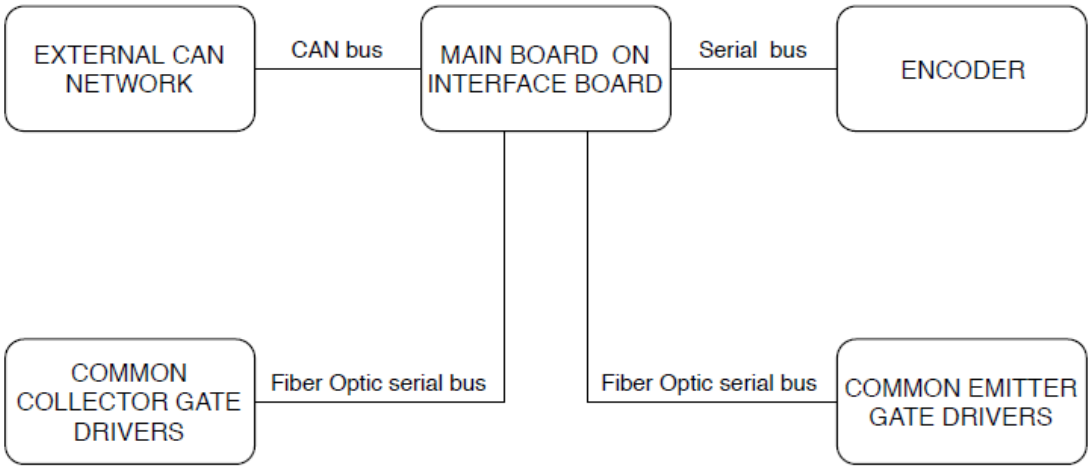

Figure 4.26: Communication ring layout

Here we have a main control board that takes the set-points from an external device via CAN Bus or Serial Port. Speed and position feedbacks are instead given to the board by a second port, a serial synchronous interface (using BiSS open protocol), that must be connected to an encoder.

Last, we have two daisy chain ring between control board and gate drivers.

The first loop carries the information between the master board and the gate drivers equipped on the common emitter modules, while the second one takes care of the information between the slave units on the common collector modules and the master.

The target speed of the communication of these ring was set to be 1us, to permit a current control loop of 1 MHz, needed to ensure good control performances with servomotors.

It can be noted that in this scheme the electrical quantities measurements devices are completely absent.

Here we have another innovation that stands off more traditional architectures: in fact, all the other information that are necessary for controlling the converter, travel through these communication rings between control board and gate drivers, which are :

- analogical measurements of current and voltage

- analogical measurements of module temperature
- faults
- IGBTs turn-on and turn-off time
- current direction (for the 4-step commutation)

Fig. 4.27 presents the communication frame structure, along with its contents.

Data Units

Switching Data Unit

Fields	**Arb <-> node loop 1**	**Arb <-> node loop 2**	**Arb <-> node loop 3**	**CRC**
Size (bits)	20	20	20	8

Data fields

Switching PDU is "bidirectional": in the case of receiving a switching data unit, each node loop device reads the data specifically addressed to it from the frame and inserts data into the frame while that frame passes through the node.

Arbiter to node loop data unit (one for each node loop)

Symbol	**S**	**T1**	**T2**	**IG**	**MT**
Size (bits)	3	7	7	2	1

S
IGBT state for the next commutation

T1
first duty cycle

T2
second duty cycle

IG
IGBT excluded from commutation (assuming only one commutation in 1us)

MT
current/voltage or temperature selection

Node loop to Arbiter data unit (one for each node loop)

Symbol	**M**	**CD**	**CE**	**GE**
Size (bits)	12	3	1	1

M
Current, voltage or temperature value, depending from then node loop and the value of **MT**

CD
IGBTs comparator value for current direction

CE
CRC error on previous received communication

GE
Global error

CRC

The CRC specified for this data unit is CRC8 with polynomial $\mathbf{x^8 + x^2 + x^1 + 1}$

Figure 4.27: Master board - gate drivers communication frame

This extremely simple layout was made possible by designing an intelligent gate driver board [[Zorzi and Calvini(2018)]], which will be discussed later.

4.3.2 Control Board

The control board can be split into two sub-units.

The first one is formed by the Z-turn lite board, a commercial board manufactured by Myir Tech, powered by an XC7Z010 SoC, which consists in an ARM-Cortex A9 processor integrated with a Xilinx Zynq 7007 FPGA. The outer communication rings (CAN, serial), the outer control loops (position, speed) and the third harmonic injection are all executed by the processor, while the current control loop and the modulator run on the FPGA, which is also responsible for the internal communication ring. Fig.4.28 shows the aforementioned board.

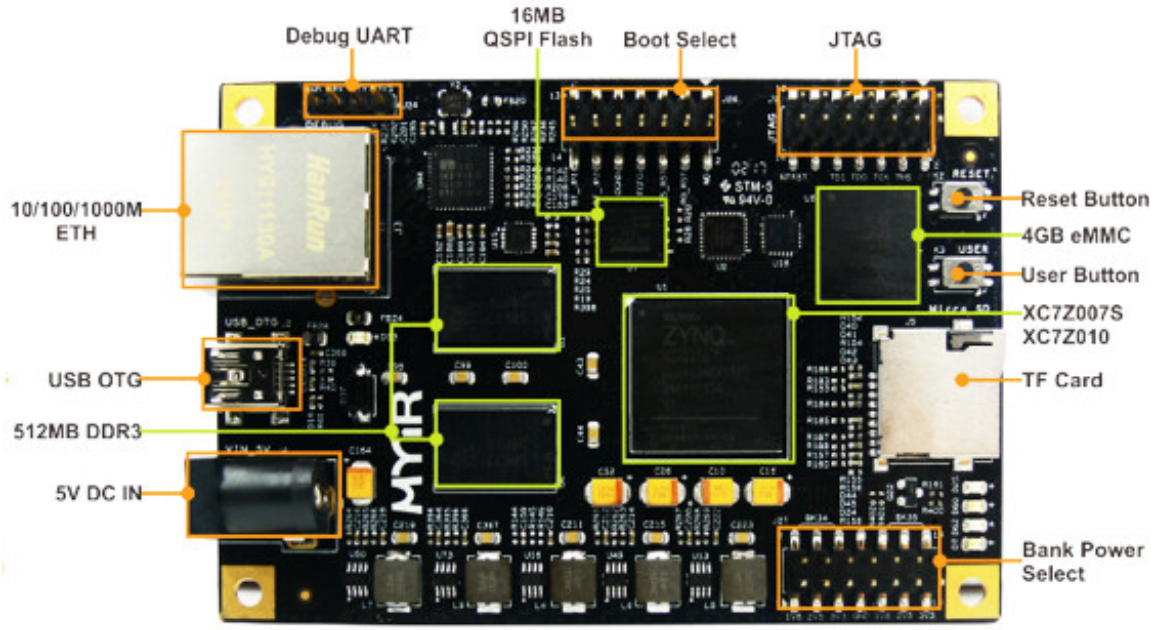

Figure 4.28: Z-turn Lite board

The second sub-unit is represented by an interface between the Z-turn lite board and the rest of the elements of the converter. While CAN and Serial Encoder ports are quite standard, the communication between control board and gate drivers is realized by means

of fiber optic communication. This permits to achieve very high speed (250 Mbps) while maintaining galvanic isolation and, more importantly, makes the system almost immune to noise. Six fiber optic transceivers are housed on every control board, and permit controlling up to three matrix converters (the reasons for this last statement will be discussed further in this chapter).

It is also worth mentioning that the interface board takes an external DC supply, ranging from 30 to 60V , converts it and distributes it to all the other boards of the Matrix Converter.

4.3.3 Gate drivers

The gate driver units were one of the most ambitious challenges in the design of the converter. Their development spanned through 2 years and a half, and required several revisions of the boards. This is due to the fact that most of the issues that were dealt with involved, in a direct or indirect way, stray capacitances or leakage inductances, related to the components and, more importantly, to the board layout. In addition, as we will see, the board accommodates high speed signaling traces. Due to this layout dependency, many modifications to the board required a new PCB. Fig.4.29 and Fig.4.30 present the latest board versions.

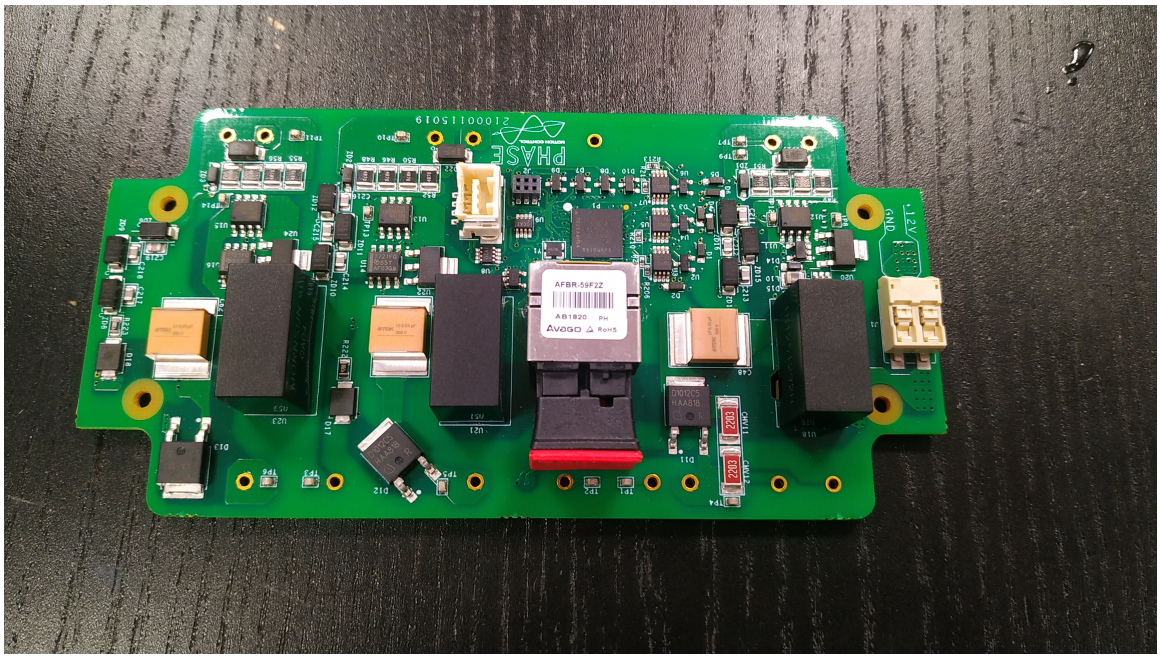

Figure 4.29: Common emitter gate driver board

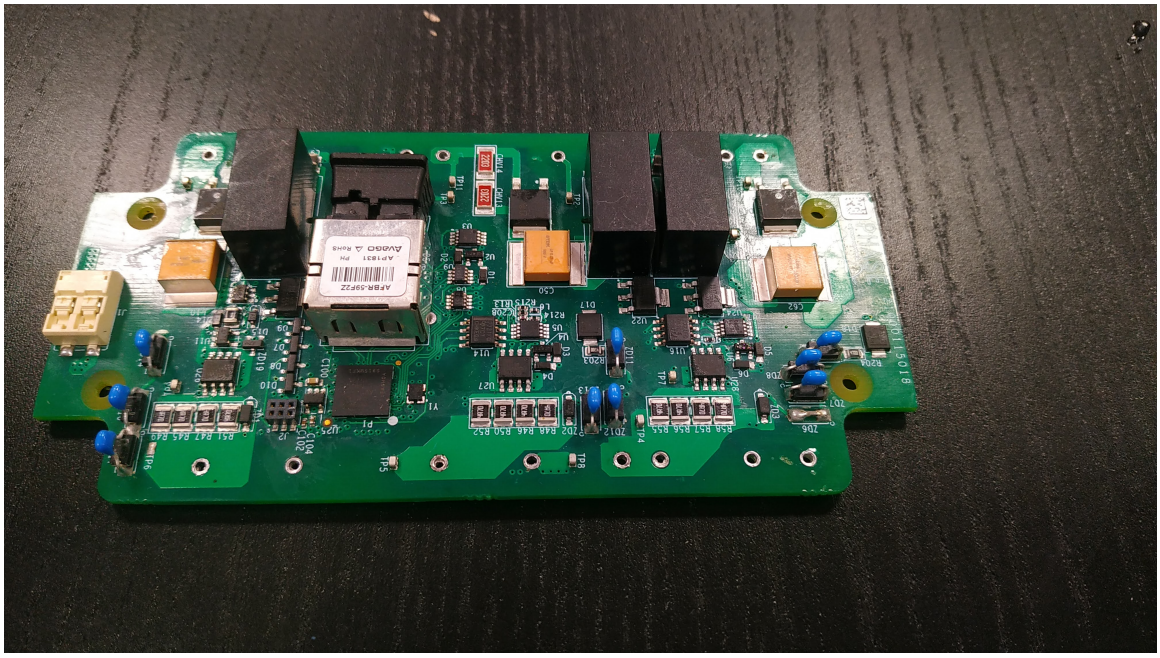

Figure 4.30: Common collector gate driver board

Overview

The gate driver units were one of the most ambitious challenges in the design of the converter.

At its core, a gate driver is a mean to isolate and amplify a logic signal and carry it to the power element. However, in the proposed configuration, in order to make the physical layout of the converter as compact and user-friendly as possible, as well as to reduce the amount of noise picked up from signal cables, it was decided to centralize all the measurements and the safety functions on the gate drivers themselves. This choice, however, implies the need of an external power supply, in order to guarantee safe operation of the device even during loss of grid events. Moreover, the coordination of all these functions need some form of processing capabilities, entrusted to an Intel MAX10 FPGA, one per single gate driver board. This unit was considered particularly suitable for the objective, thanks to its low cost and its integrated flash memory, which permits to simplify the board layout and improve the system reliability.

Power supplies

Depending on which module is dealt with, different considerations on the design of the power supply stage must be made. The switching signal must be driven between the IGBT's gate and emitter, and the three different gate driver circuits present on each of the three boards equipped onto the common collector modules must adopt three different isolated power supplies: each of the IGBTs emitters is, in fact, connected to one of the input phases, and so a common ground is not possible. This restriction is of course absent from the common emitter modules, which intrinsically share a common point, and thus do not need isolated supplies. However, as mentioned before, an external low voltage DC source is needed for safety reason, which of course needs to be isolated from the high voltages present on the board. Taking into account each of these three considerations, the proposed solution makes use of three DC-DC flyback converters, that guarantee galvanic isolation both from the external source for both type of gate drivers and between the three circuits in common collector modules.

Gate driving

Even to ensure fast and reliable switching operation, the MOS gate of the IGBTs does not require more than few watts of power at the target switching frequency. An off-the-shelf IC would be sufficient to build this board stage, if presenting high current sourcing and sinking capabilities. This is important to save space, cost and design efforts. Capacitive couplers can be used on the common collector boards, in order to transport the signal from the FPGA to the two isolated gate driving ICs.

Active Clamp

In case of an anomaly or malfunction, it is possible for the IGBTs collector-emitter voltages (V_{ce}) to rise above their maximum rated value during the turn-off. In order to avoid these events, each of the gate driver circuit of each board was equipped with an active clamp circuit, consisting in the scheme of Fig.4.31.

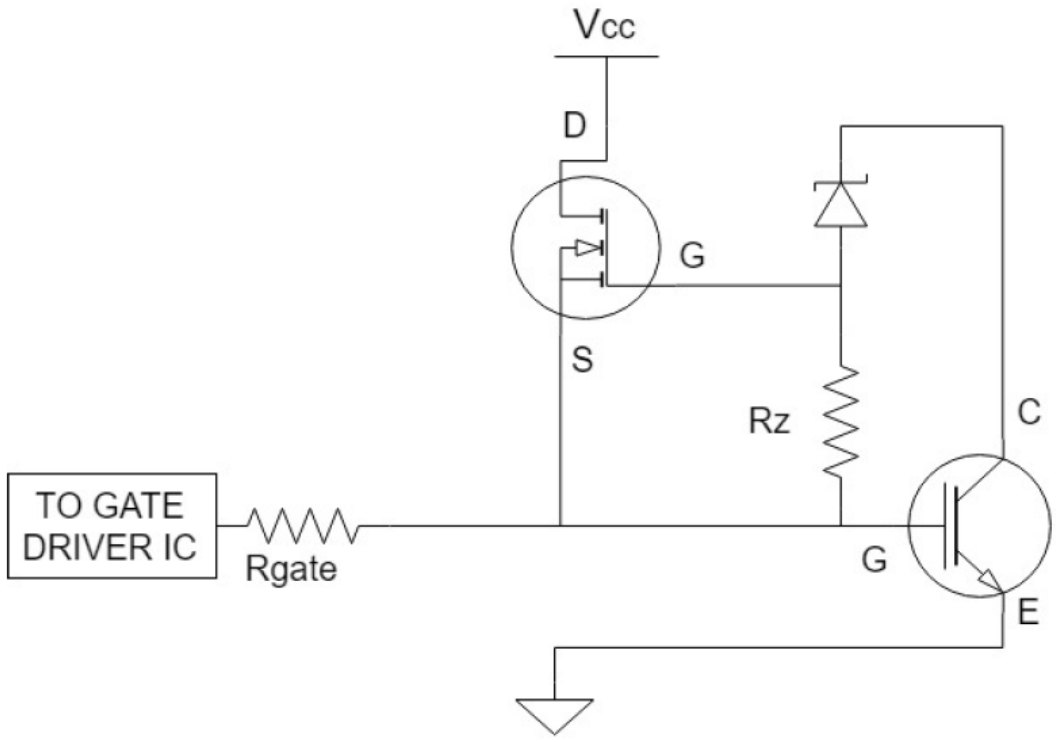

Figure 4.31: Active clamp principle schematic

The Zener diode must be chosen with a breakdown voltage (V_{br}) well above the working voltages of the converter, but before the maximum allowed V_{ce}. This causes a voltage of the value

$$V_{gs} = V_{ce} - V_{br} \tag{4.15}$$

between the resistor R_z terminal, and so between gate and source of the MOSFET, which must be chosen to enter saturation at /

$$V_{gs} < V_{ce_{MAX}} - V_{br} \tag{4.16}$$

Whenever a dangerous over-voltage occurs, the clamp circuit provides the IGBT with the necessary turn-on voltage, allowing current to flow through it and thus effectively reducing V_{ce}.

Sensing

In order to correctly control the presented converter, it is necessary to measure many different quantities. To reduce the costs of the gate driver boards, as well as to save on-board space, the quantities being monitored on the two types of boards differ slightly from each other. A basic scheme can be seen in fig.4.32.

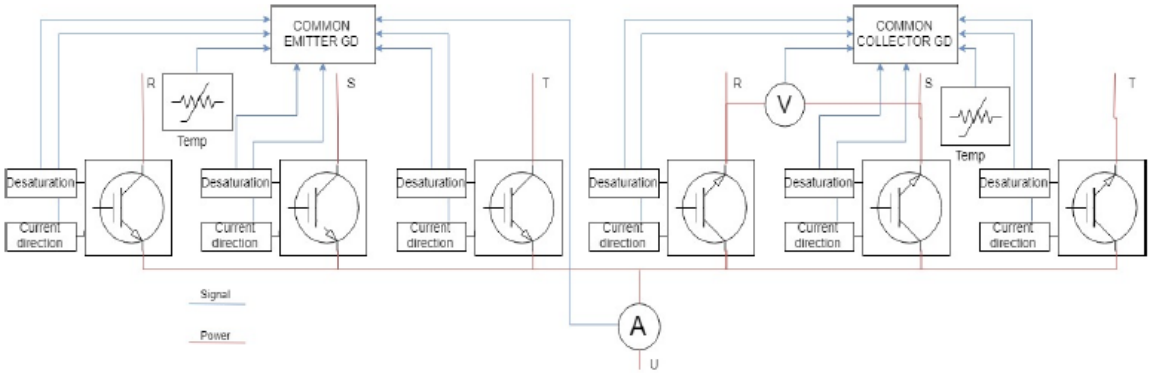

Figure 4.32: Gate Driver to Control Board daisy chain communication ring

The three common collector boards read the phase voltages (one per board) with a simple and robust off-the- shelf operational amplifier IC. On the other hand, current flowing

through each of the three lines of the converter is monitored on the common emitter gate drivers, by the means of Hall effect current transducers. It worthy of mention that this critical measurement is not directly fed to the FPGA ADC, due to the consistent delay that would inevitably be introduced by the ADC input capacity and the output impedance of the sensor. Instead, an additional operational amplifier provides low capacitance and high impedance input to the sensor, and, on the other hand, low output impedance to the ADC. The remaining quantities are measured by both the board types, starting with temperature monitoring, which is accomplished by a PTC integrated in the modules' package. Another fundamental quantity that must be evaluated in order to guarantee safe operation of the device is the aforementioned V_{ce}. In fact, in case of short circuit, the current in the affected IGBT rises rapidly, increasing the V_{ce} drop and desaturating the device. Such events must be flagged for each of the 18 IGBTs, and transmitted to the master unit. In addition, immediate countermeasures can be taken by the gate driver units themselves, thanks to the onboard FPGA, which is set to turn off an IGBT in case the desaturation flag appears for more than 5us after the turn on, effectively protecting it from destruction. Since the exact Vce value is superfluous, while its detection speed is of primary concern, simple and cheap comparator ICs can carry out this operation. Finally, the proposed Matrix converter, makes use of the 4-step commutation technique, and so it is needed to know the direction of the current for the correct determination of the switching pattern. The aforementioned Hall effect sensors are not fit for this due to inevitably large measurement offset around the zero. However, the current direction can be reliably determined by monitoring the voltage drop across the diode in series to each of the 18 IGBTs, and, since the same considerations that are valid for the desaturation detection can be also made in this case, a solution that makes use of comparators still applies.

Optical fiber communication

As stated before, it is of primary concern to both provide galvanic isolation between the master unit and the slaves (due to the floating nature of their ground potential), as well as to guarantee signal integrity in devices inherently working in noisy environments (due to the high $\frac{di}{dt}$ and $\frac{dV}{dt}$ associated with the operation of the converter). In order to deal with those two necessities not only it was chosen to carry out all the data exchange by the means of

optical fiber communication, but also to adopt Low Voltage Differential Signaling (LVDS) between the transceiver and the FPGA, thus preventing the effects of common mode noise. In addition, particular attention was given to the PCB layout of the LVDS routes, in terms of balancing and total length, as shown in Fig.4.33.

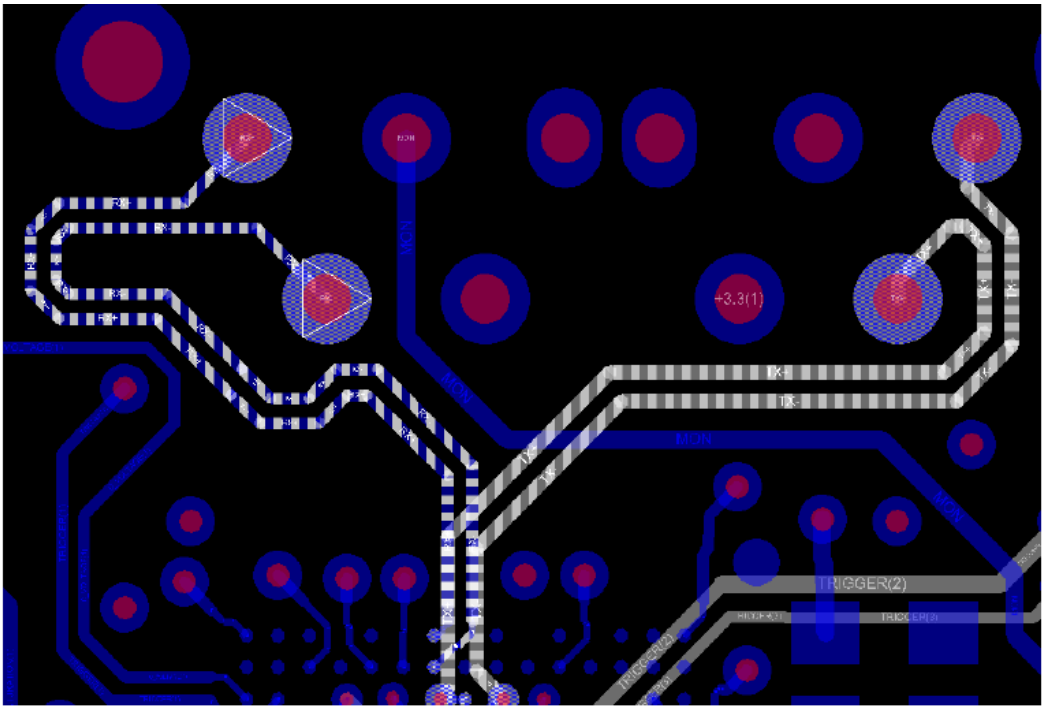

Figure 4.33: Optical Fiber module LVDS routes

Since the communication frame was estimated to be 68 bits long, as already presented in Fig.4.27 , and transmitted over the time of 1us, it was deemed necessary to use a transceiver capable of handling at least 68 Mbps, like AVAGO's AFBR-59F2Z.

Bibliography

[Zorzi and Calvini(2018)] A. Zorzi and M. Calvini. Intelligent gate driver for a modular three-phase matrix converter. In *2018 IEEE 4th International Forum on Research and Technology for Society and Industry (RTSI)*, pages 1–5, Sep. 2018. doi: 10.1109/RTSI.2018.8548379.

Chapter 5

Testing

5.1 Overview

The development of a power converter is not an easy task, and it can be profitable to try to decouple the possible problems, that could arise during its operation, as much as possible. A way to do so is testing the single components of the assembly or, if not possible, testing them with the lowest possible number of elements under test. This approach also goes well with the industrial reality, where the various components require different efforts in terms of workforce and time to be realized, an so become often available in an order that is not the one required for testing purposes.

In the following sections we will discuss the various tests that were carried out on the designed devices that were presented in the former chapter, with the exception of the capacitor busbar. This element, in fact, required a special attention just from the mechanical point of view, but was made of commercial off-the-shelf components that during their operation are not subject to relevant stresses, if their datasheet ratings are considered.

5.2 Heat sink tests

5.2.1 Aim of the tests

The main aim of test was to verify the effective cold plate performances, estimated by CFD and FEM analysis, whose results were reported in Table 4.2. This required two different test benches.

5.2.2 Test 1 - water tightness

This test was carried on in order to verify the capability of the heat sink to withstand a channel-to-ambient pressure of $500kPa$.

To perform this test, the heat sink was connected to a manifold at the inlet, further connected to an absolute pressure analog gauge and to a hand pump. The entire test bench was then left inside a temperature-controlled chamber for $24h$, in order to eliminate temperature-dependent pressure variations, and water was pumped inside the heat sink, thus forcing air to exit through the outlet. Then, the outlet was blocked with a cork, and the system was brought to a pressure of about $600kPa$. After waiting a few minutes, the pressure transient due to the remaining air bubbles trapped inside was considered to be finished, and the pressure gauge reading was recorded. The system was left under pressure inside the chamber for about 24 hours. After this time, the pressure gauge reading was recorded again and was compared with the initial post-transient reading. The pressure difference was found to be negligible, so the test was considered a success. Fig.5.1 presents the test bench with the DUT, while Table 5.1 presents the boundary conditions, the readings and the results.

Figure 5.1: Water tightness test bench

Quantity	Value	U.M.
Water/Ethylene glycol ratio	1 : 1	$unitless$
Ambient temperature	20	$°C$
Post-transient test pressure	634	kPa
Final test pressure	628	kPa

Table 5.1: Water tightness test readings data

5.2.3 Test 2 - surface temperature and pressure drop

This test was, unsurprisingly, carried out after water tightness verification, since eventual leakages would have had an impact on the results.

To provide the necessary heating power to the system, with the correct footprint, it was chosen to directly use the Semix5 modules. Due to the fact that the power and control stages were, of course, not fully available at the time of this test, it was decided to put the modules in series and fully bias each of IGBTs gates, supplying the system with a DC controlled source in order to provide the nominal power losses (plus 10%, to keep an over-sizing margin). An independent measurement system, represented by a watt meter (Yokogawa 760101-S15) was also connected to the DUT.

Fig.5.2 presents the electrical connection schematic. It must be noted that in this test isolated supplies are still necessary, so the gate bias voltage was provided by means of two 6LR61 batteries in series

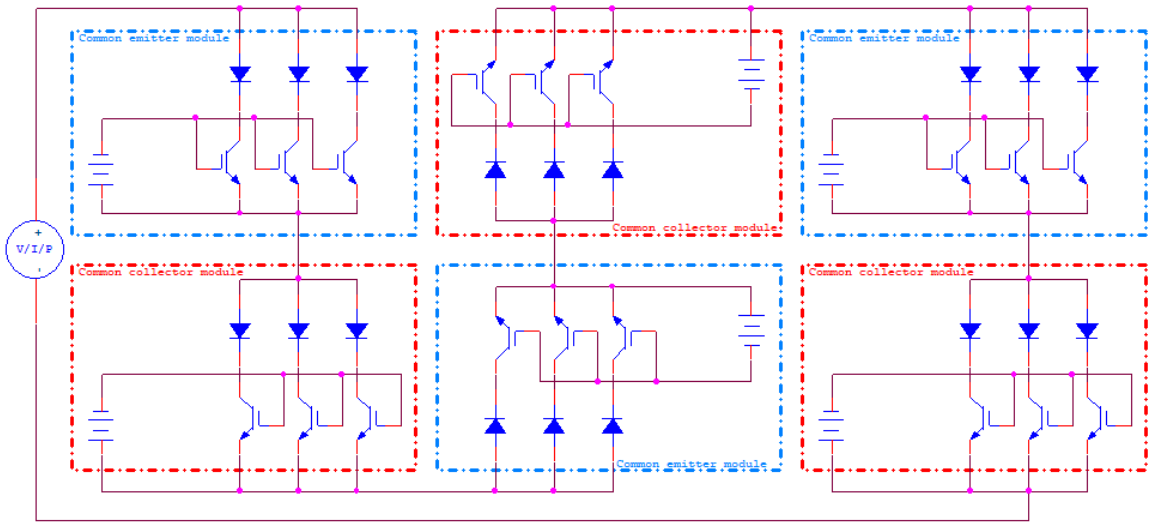

Figure 5.2: IGBTs connection schematic

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The heat sink, with the modules fastened onto it, was then connected to two manifolds, further connected to a differential digital pressure gauge (PCE-910) and to the plant water discharge and return. A control valve was present on the discharge, while a flow meter was connected to the return. Water temperature was kept constant by a chiller unit. The piping schematic is reported in Fig.5.3.

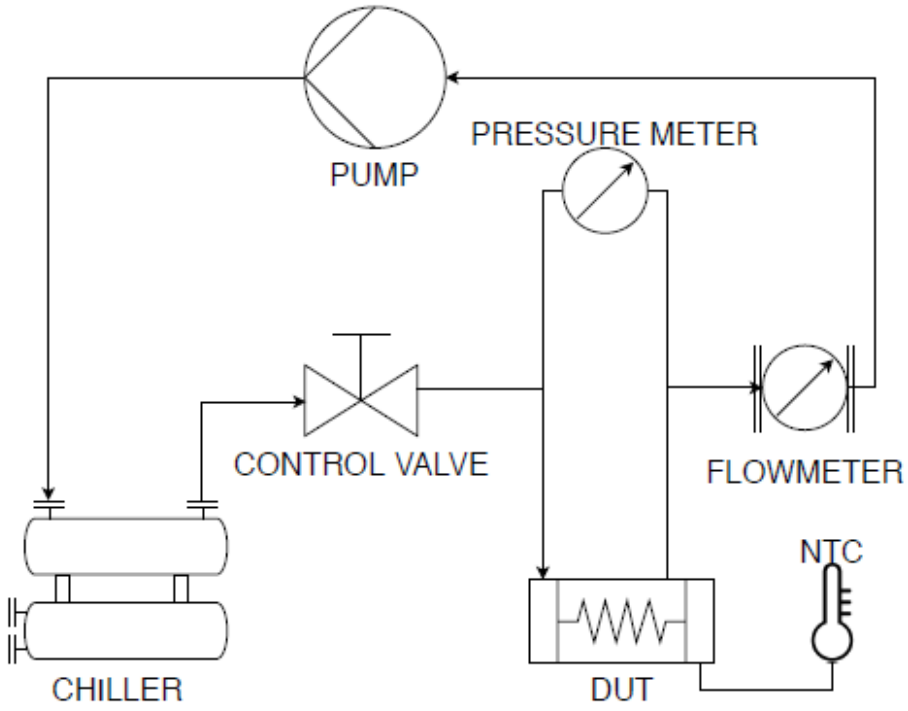

Figure 5.3: Test piping schematic

For measuring the surface temperature, it was chosen to use the NTCs of the Semix5 modules, which are housed onto the internal side of the thermal pad, and to read their value by means of a digital multimeter. This introduces an error in the measurements due to the temperature drop in both the thermal pad and the thermal grease interface due to their associated thermal resistances. However, not only this is a conservative assumption , but also these two thermal resistances can be considered negligible when compared to both thermal pad-to-junction thermal resistance and plate surface-to-water thermal resistance. In addition, another approximation had to be made: in fact, it was not possible to carry on the test at the nominal fluid temperature flow, due to the fact that the test was done by using the cooling circuit of a factory, whose temperature could not be changed.

This said, after having controlled the supply to the target power value, the control valve was adjusted up to the nominal coolant flow, and the NTCs resistance values were monitored. The thermal transient was considered finished after the NTCs readings began fluctuating about the same resistance values, only due to the variations in the inlet fluid temperature. At this stage, inlet temperature and the NTCs readings were recorded, along with the differential pressure between inlet and outlet.

Fig.5.4 presents the test bench with the DUT, while Table 5.2 presents the boundary conditions, the readings and the results.

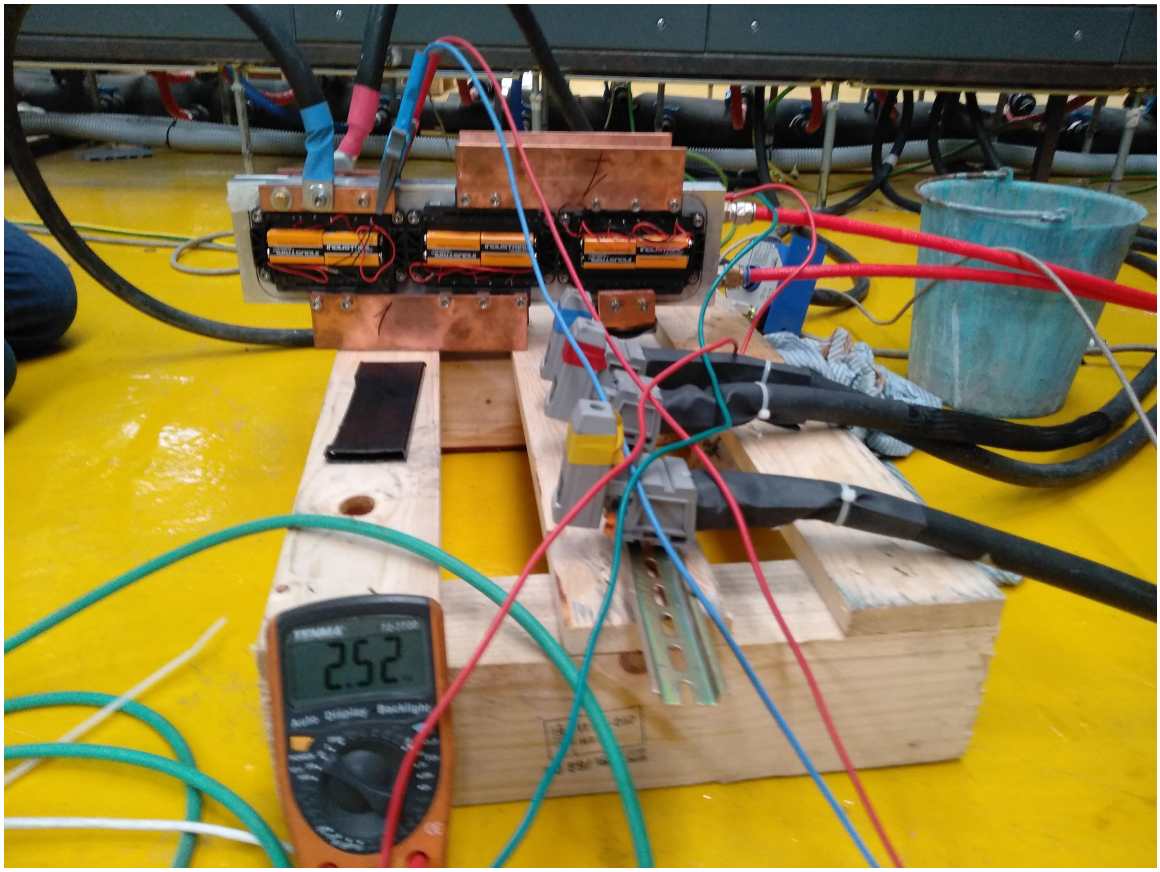

Figure 5.4: Pressure drop and surface temperature test bench

Quantity	Value	U.M.
Water/Ethylene glycol ratio	1 : 1	$unitless$
Ambient temperature	20	$°C$
Coolant flow rate	2.78	$\frac{m^3}{s}$
Pressure drop	33	kPa
Heat generation rate	6.66	kW
Inlet fluid temperature	15	$°C$
Maximum thermal pad temperature	71	$°C$

Table 5.2: Pressure drop and surface temperature test data

5.3 Inductor test

5.3.1 Aim of the test

The main aim of test was to verify the thermal behavior of the inductor, estimated by CFD and FEM analysis (whose results were reported in Fig 4.10 and Fig 4.11) along with its inductance and resistance values. A single test bench was sufficient to complete these tasks.

5.3.2 Test setup and results

Due to the obvious lack of the actual finished matrix converter, it was not possible to stress the component with the actual waveform. Instead, the inductor was connected to a power controlled DC power supply, with the test power set so to have in the copper only the same global power losses predicted by the FEM analysis (coming from both copper and iron). While this means that iron losses verification was not possible, the test put more stress on the component, since the copper temperature resulted higher than what it would have been with the correct losses distribution. One PT1000 temperature sense resistor was put on the inductor external iron surface, while another one was put directly inside the central slot. The system was then powered on, waiting for both the PT1000s to reach stable readings, thus signaling steady state condition. At this point, the supply was quickly disconnected and a variable frequency RLC meter was connected to all the three inductor phases, in order

to measure their resistance and inductance values, at several different frequencies. Fig.5.5 shows the DUT onto the test bench, where it can be noted that the inductor was placed with its biggest surface onto an isolating mat, to stress it further in case of possible future design modifications. Table 5.3 presents the boundary conditions, the readings and the results. Even if it was not possible to perform the test under the nominal temperature rating of the component, due to lack of a such high temperature heated room, the test was considered successful, since the maximum ΔT was not reached. This is an acceptable statement due to the power controlled power supply, that permitted us to ignore the variations in copper resistance and iron loss coefficient (the latter very small, thanks to the adoption of Fe-Si) associated with temperature.

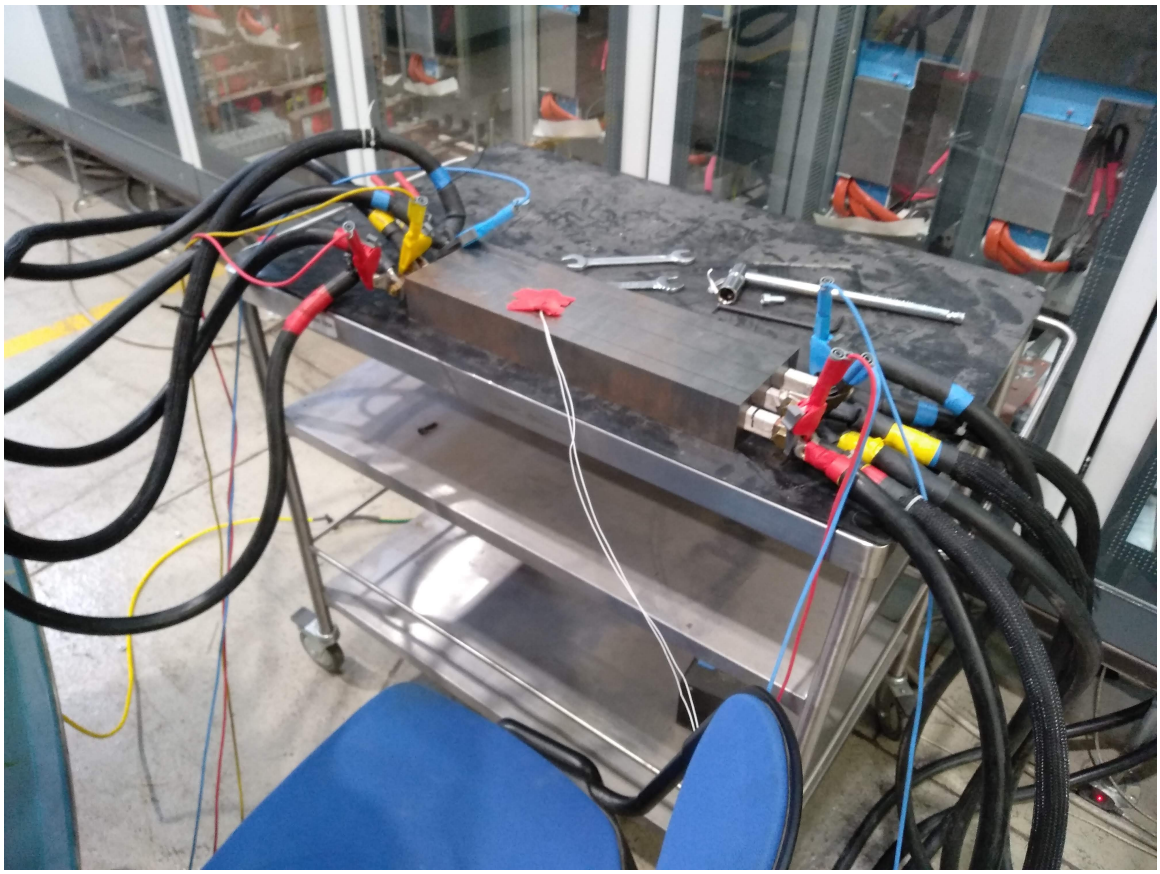

Figure 5.5: Inductor under test

Quantity	Value	U.M.
Ambient temperature	20	$°C$
Maximum outer iron temperature	73	$°C$
Maximum central slot temperature	88	$°C$
Heat generation rate	80	W
Phase R inductance @ $100Hz$	9.72	μH
Phase S inductance @ $100Hz$	9.63	μH
Phase T inductance @ $100Hz$	9.44	μH
Phase R inductance @ $120Hz$	9.61	μH
Phase S inductance @ $120Hz$	9.55	μH
Phase T inductance @ $120Hz$	9.31	μH
Phase R inductance @ $1kHz$	8.76	μH
Phase S inductance @ $1kHz$	8.61	μH
Phase T inductance @ $1kHz$	8.34	μH
Phase R inductance @ $10kHz$	8.425	μH
Phase S inductance @ $10kHz$	8.22	μH
Phase T inductance @ $10kHz$	7.99	μH

Table 5.3: Inductor test data

5.4 Capacitor busbar test

5.4.1 Aim of the test

The aim of this test was simply to verify the capacitance values of the unit. The frequency dependence of this parameter was not of interest and was not explored.

5.4.2 Test setup

An RLC meter was first connected between each of the phases to measure the capacitance, reporting the readings that can be found in Table 5.4. Polypropylene capacitors temperature dependence is really low, and so the test was not performed in a temperature controlled room. Fig.5.6 shows the unit.

Figure 5.6: Capacitor Busbar

Quantity	Value	U.M.
Phase R-S capacitance	62	μF
Phase S-T capacitance	61	μF
Phase T-R capacitance	61	μF

Table 5.4: Busbar measured capacitance values

5.5 Clamp unit tests

5.5.1 Aim of the test

The aim of test was to verify the intervention of the clamp unit even with supply voltage disconnected, with the unit supplying itself through the voltage sensing stage. It would

have been also interesting to verify the clamping effectiveness by opening a short circuit onto an inductance of an appropriate value, but the lack of the appropriate components postponed this test.

5.5.2 Test setup

To execute the test, both the grid-side precharge bridge and the output-side clamp bridge were connected through two phases only to a Cockcroft-Walton generator controlled by a Variac. This way, it was possible to safely test the clamp intervention level. In fact, while the Cockcroft-Walton generator is capable of very high voltage levels, its output impedance prevented him to supply the load in a destructive way, since the clamp unit its not intended for continuous operation, but rather for low duration, low energy events. A voltage probe was then connected between the DC LINK terminals of the clamp unit, triggering the oscilloscope onto the negative voltage slope of the clamping event.

Fig.5.7 shows the connection schematic, while Fig.5.8 confirms the correct intervention level of the DUT.

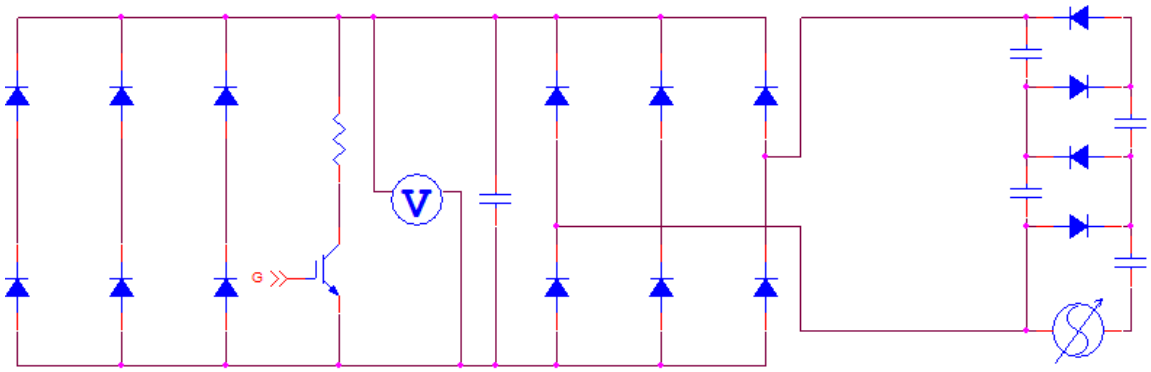

Figure 5.7: Clamp unit test connection schematic

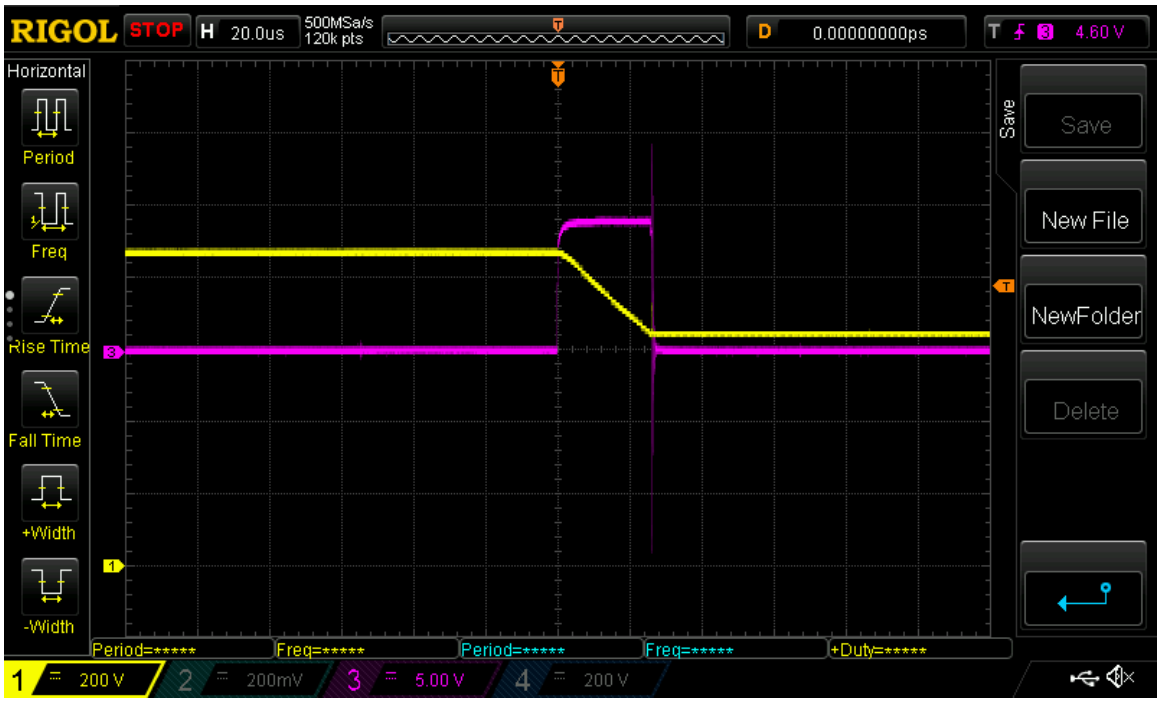

Figure 5.8: Clamp unit intervention acquisition
IGBT Gate-Emitter Voltage(violet, $5V/div$)
IGBT Collector-Emitter Voltage (yellow, $200V/div$)
Time scale : $20\mu s/div$

5.6 Gate Driver tests

5.6.1 Aim of the test

The gate driver unit is one of the key elements of the system and carries on many different functions, that had to be tested thoroughly and will separately be dealt with in the following sections.

5.6.2 Test setup

All the tests that had to be carried on the gate driver unit share the same test bench setup, since all of them had to be carried under the worst-case scenario from the electromagnetic radiation point of view, i.e. the short circuit event, followed by forced turn-off of the IGBT.

During and immediately after the short circuit, in fact, the board experiences the maximum $\frac{dI}{dt}$s and $\frac{dV}{dt}$s, and so the maximum stress on the components.

A test bench was set up, connecting the devices under test (DUTs) in a way closely resembling the final converter connection scheme, as shown in Fig.5.9. In this configuration, the module is directly connected in parallel with a variable DC voltage supply, capable of sourcing high pulsed currents for the necessary time thanks to the capacitor C1, whose connection inductance to the module is minimized by keeping the cables as short as possible. By keeping another IGBT always closed and connected to the other one by means of the other capacitor C2 , it is possible to create a freewheeling path for the short circuit current. This can always be performed during the converter operation, by keeping closed the IGBT that is reversely biased. C2 will then discharge on R_d, which represents the finite resistance of the short circuit path. Fig.5.10 depicts the DUT.

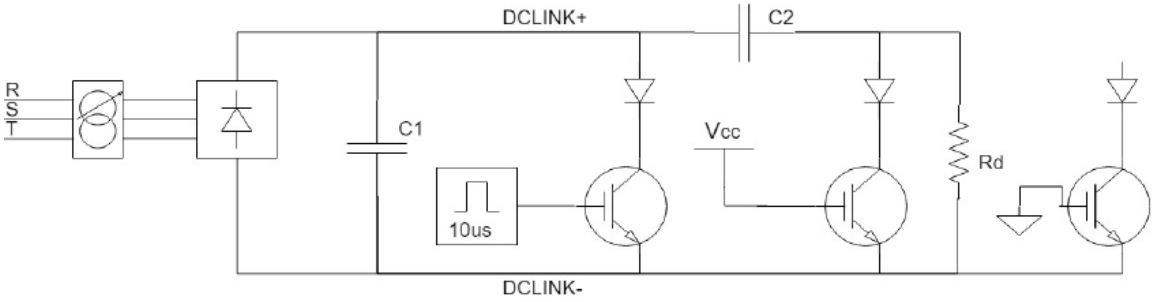

Figure 5.9: Test bench scheme

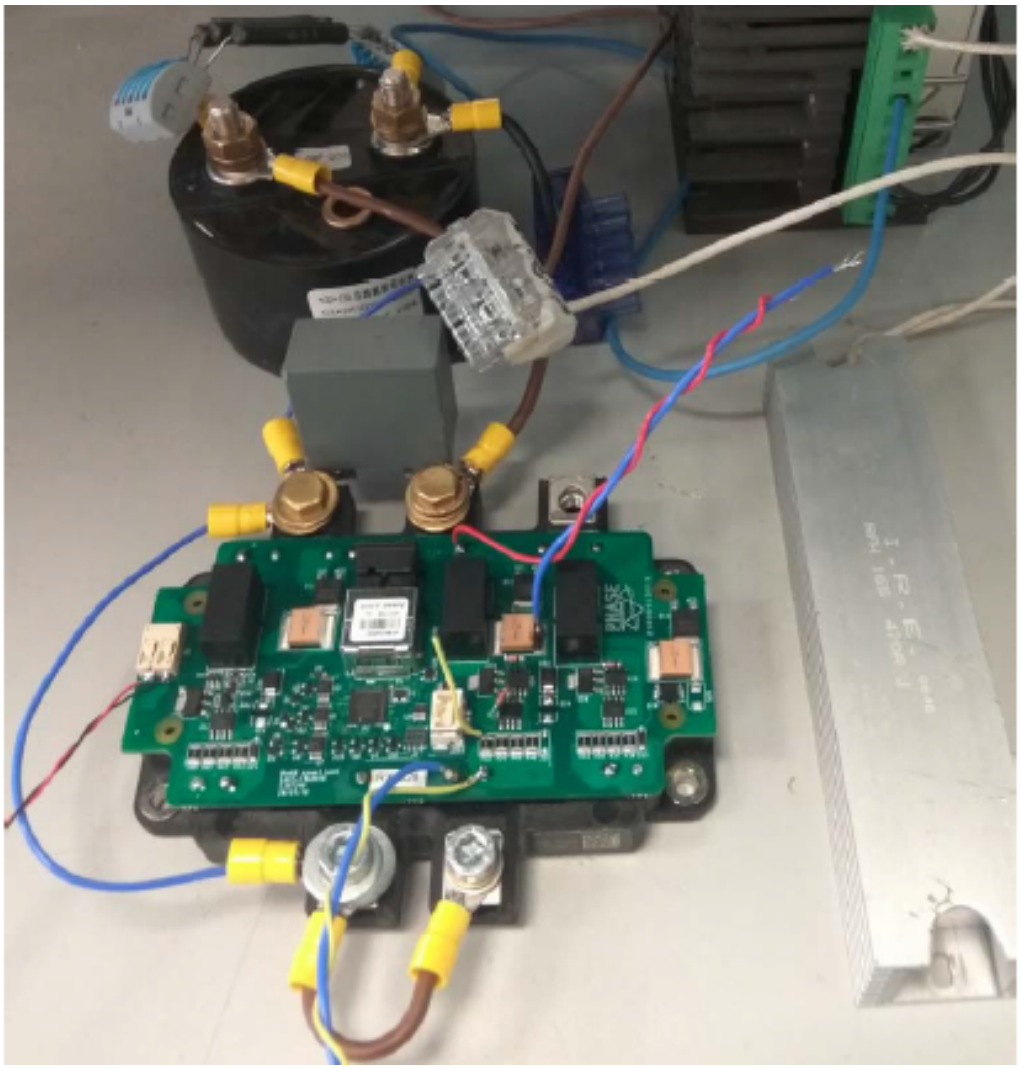

Figure 5.10: Actual test bench

5.6.3 Active Clamp

This test serves the purpose of checking the capability of the on-board active clamp in reducing the voltage overshoots after the short circuit event and the consequent IGBT turn-off, and was performed under two different assumptions.

In the first case, we assume that the converter is properly functioning, and an external short circuit causes the desaturation to intervene. This event is simulated by setting the

FPGA to turn-on one IGBT for $5\mu s$, and then immediately to turn it off. The leakage inductance of the module causes the voltage to rise at the turn-off and adds up with the source voltage, while the current in the external connection inductances freewheels in the path of Fig.5.9 and the resulting voltage does not stress further the active IGBT A voltage probe was then connected across collector and emitter of the former IGBT, while another one was connected between gate and emitter. A current probe was connected in series with the IGBT. Fig.5.11 shows the results of the test.

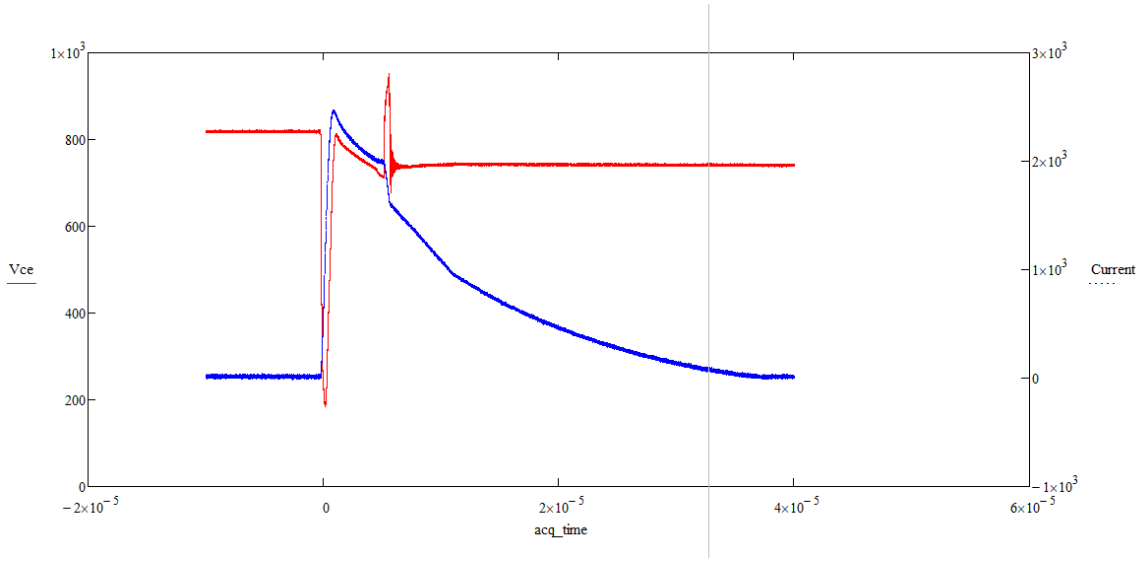

Figure 5.11: Active clamp intervention during short circuit with free-wheeling path
IGBT Collector current (blue, $1kA/div$)
IGBT Collector-Emitter Voltage (red, $200V/div$)
Time scale : $20\mu s/div$

In the second case, we assume that the converter is not properly functioning, and a short circuit causes the desaturation to intervene. Due to the malfunction, we also assume that the free-wheeling path is not present. This event is simulated by setting the FPGA to turn-on one IGBT for $5\mu s$, and then immediately to turn it off, but this time the free-wheeling IGBT is left turned off. This time, the leakage inductance of the module adds up with the external connection stray inductances and causes the voltage to rise at the turn-off way more steeply than before. Again, a voltage probe was connected across collector and

emitter of the former IGBT, while another one was connected between gate and emitter and current probe was connected in series with the IGBT. Fig.5.12 shows the results of the test.

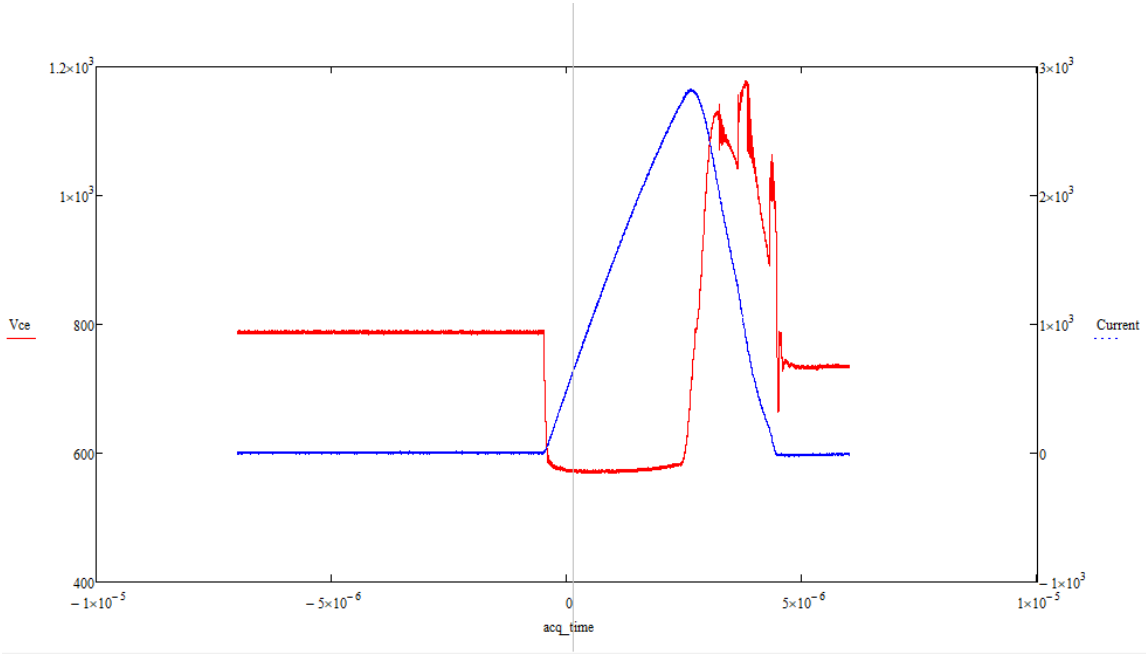

Figure 5.12: Active clamp intervention during short circuit without free-wheeling path
IGBT Collector current (blue, $1kA/div$)
IGBT Collector-Emitter Voltage (red, $200V/div$)
Time scale : $5\mu s/div$

5.6.4 Gate driving voltage

In order to achieve high efficiency and prolong the IGBTs' life, it is necessary to obtain steep turn-on and turn-off ramps, thus minimizing the amount of time in which the component is not saturated. This test was aimed at verifying the gate driving signal quality, and so the active clamp circuit was disconnected during the trials. This of course meant that it was necessary to decrease the source voltage, to prevent the device destruction. A voltage probe was connected between gate and emitter, while a current probe was connected in series with the IGBT. The result of the waveform acquisition can be seen in Fig.5.13, where a little ramp tail due to miller effect can be seen during the turn-off.

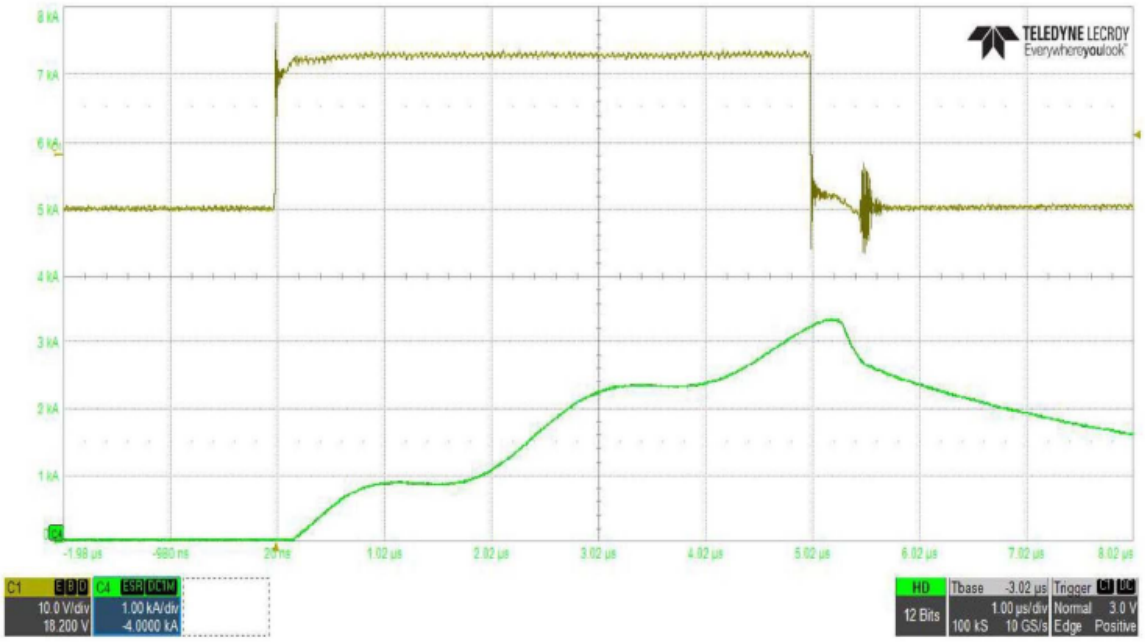

Figure 5.13: Simultaneous acquisition of gate driving signal (yellow) and short circuit current(green)
IGBT Collector current (Green, $1kA/div$)
IGBT Gate-Emitter Voltage (Ocher, $10V/div$)
Time scale : $1\mu s/div$

5.6.5 Communication signal integrity test

This test was done in order to verify the integrity of the data transmitted through the optical fiber during the aforementioned short circuit event. A direct comparison with an oscilloscope between a known transmitted signal and the output waveform at the receiver end is not possible, because the differential error that would be introduced by the insertion of the probe would be comparable to the LVDS signal amplitude. In the light of the above, a square wave signal at the frequency of $100MHz$ (well above the target communication frequency) was synthesized by FPGA N°1 and transmitted to FPGA N°2, which was equipped on the board under test. FPGA N°2 was set to turn on one of the IGBTs for the duration of

$5\mu s$ (which is considered a safe short circuit time for the IGBTs) every $5s$, all while reading the incoming signal on the optical fiber and transmitting it back. FPGA N°1 receives the returning signal and compares it to the original one. If it finds any differences, it sets high an error flag that can be read directly with a JTAG connection. The operation must be repeated for all the three possible short circuits configurations. No error flags were risen during the test, which can be considered successful.

5.6.6 Measurement signals test

As already mentioned in the former chapters, each gate driver unit is equipped with comparators, whose outputs are fed to the digital inputs of the FPGA, along with sensors that are used in the acquisition of several analog quantities, which are then fed to the ADC of the FPGA. To verify the correct readings of each of these devices, they were fed with a known input quantity, which was then compared to the result of the reading, while the FPGA, again, was programmed to trigger a short circuit event for $5\mu s$ every $5s$. All these acquisitions were made on board and read through JTAG connection, in order to obtain the most accurate results. This test found no anomalies.

5.7 Interface board tests

As per the gate driver unit, the interface board carries out many different functions, that had to be tested thoroughly and will separately be dealt with in the following sections.

5.7.1 System power supply test

As mentioned in the previous chapter, the interface board was designed to be able to supply the entire system logic from a variable 16 to 60 V DC supply. It was estimated that no more than $120W$ were necessary with all the devices connected. While it is true that this power is distributed to all the system with different voltage levels, the on-board buck converter is the most stressed one, since all the power flows through it. To test it, a 1Ω power resistor was connected across one of the $12V$ outputs, and the system was left in a temperature

controlled room for about $1h$ in order to let it reach steady state thermal conditions. Fig.5.14 shows the DUT.

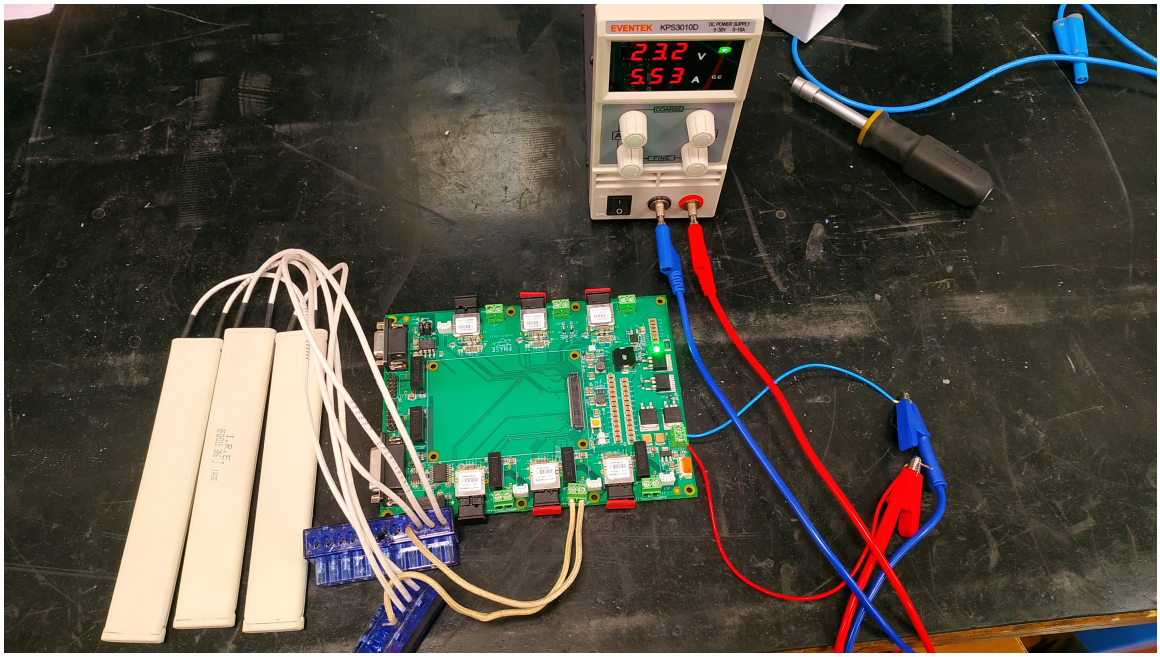

Figure 5.14: Interface Board with power resistors connected

A thermal image of the device Fig.5.15 was then taken, showing no criticality.

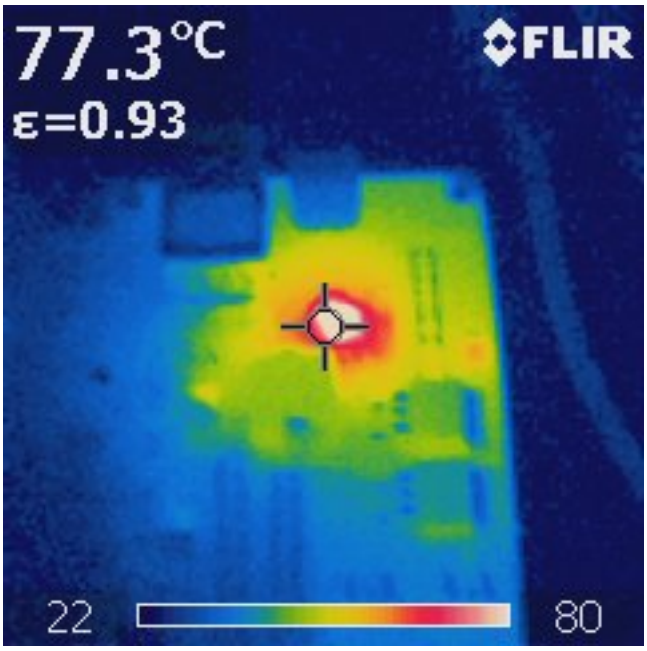

Figure 5.15: Thermal image of the buck converter area

5.7.2 Communication interfaces test

To test CAN, serial and optical fiber communication it was chosen to use two different interface boards, each connected with its Z-turn Lite board. As in 5.6.5, the on board SoCs were programmed to send the same data packets on each of the aforementioned buses contemporaneously, and to rise a flag in case of loss of data that could be read with the SoC programmer itself. No errors arose during the operation.

Chapter 6

Results

6.1 Preamble

In this chapter we will present the outcome of the thesis, that is the complete converter along with the preliminary test results, carried out at reduced power output.

On the basis of having all the single hardware components behaving correctly, the first prototype of Matrix converter was assembled onto his custom mechanical housing, wired and programmed. Fig 6.1 shows the assembled converter in its definitive setup.

The tests that are going to be discussed were carried out at the laboratories of the University of Nottingham, and, unfortunately, were not carried out at full power in the nominal point, due to the lack of enough power available from the facility.

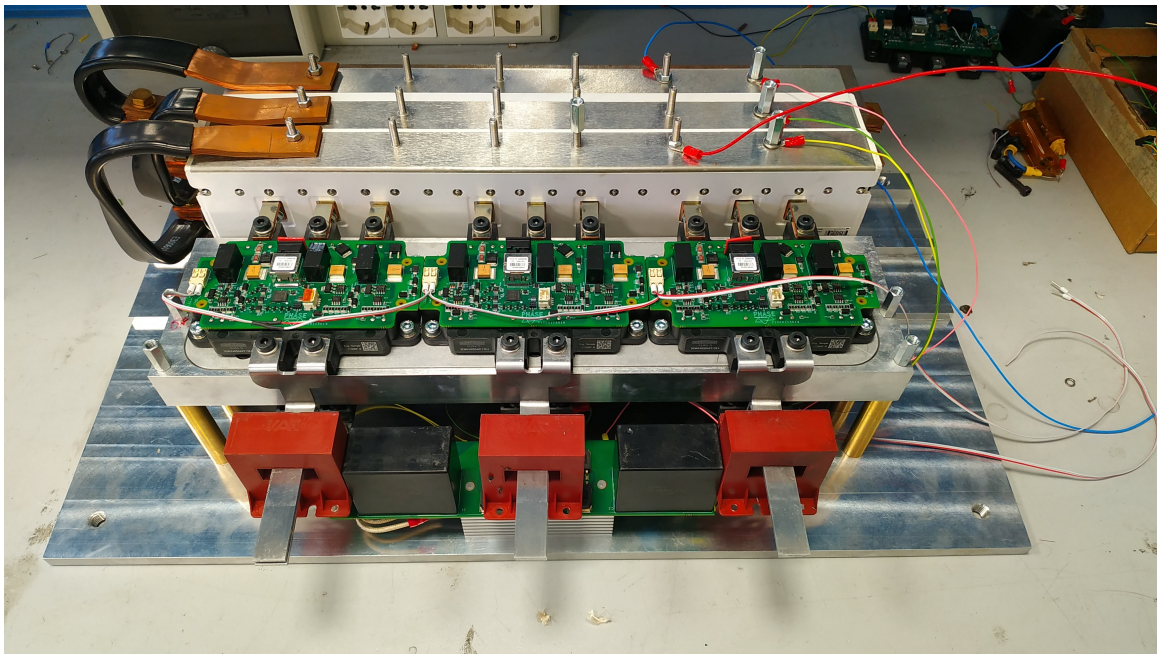

Figure 6.1: Assembled Matrix converter

The final all-out dimensions and parameters regarding the assembled converter are shown in Tab 6.1 .

Quantity	Value	U.M
All out length	600	mm
All out width	320	mm
All out depth	190	mm
Mass	40	kg
Volume	0.0365	m^3
Mass power density	6.25	$\frac{kW}{kg}$
Volumetric power density	6850	$\frac{kW}{m^3}$

Table 6.1: Final assembled converter parameters

6.2 Test bench setup

To test the system functionality, and to highlight the behavior of the new modulation strategy and demonstrate his performances in the most significant operating points, it was chosen to carry on the trials at the maximum permitted value of $\frac{\sqrt{3}}{2}$ in combination with the load values reported in Tab 6.2. By changing the output frequency on the load, and so the load reactance, the power factor, and so the resulting phase shift, could be set accordingly to Fig 6.2, which shows the two different values of φ_0 where the experimental tests were performed.

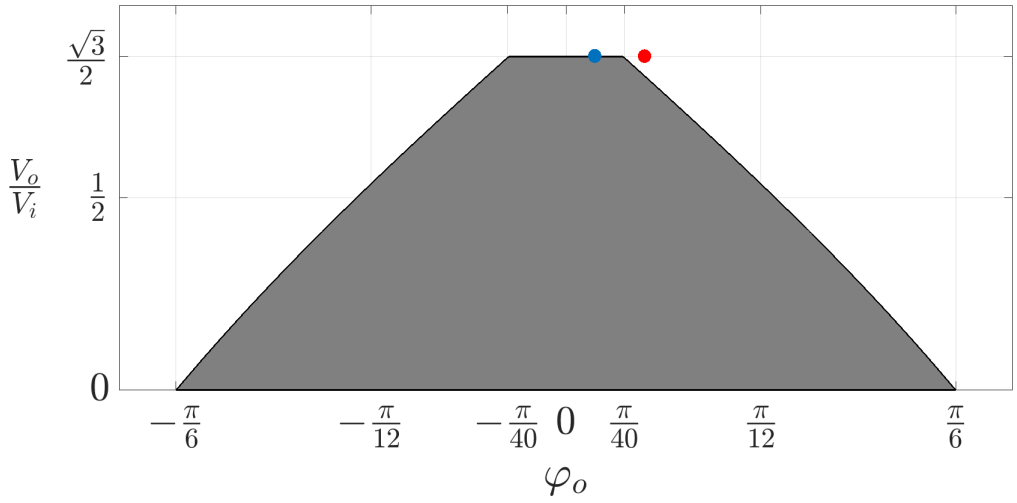

Figure 6.2: Maximum VTR operative region and reference working points

The first test point (depicted as a blue dot) , was chosen in the gray area representing all the operative conditions where the experimental hybrid modulation can rightly feed the load, without the need to switch between Calvini's technique and Venturini's technique. On the other hand, the second test point (depicted as a red dot) was set to be in the region where the Calvini's modulation cannot obtain the required voltage, and has to be assisted with the Venturini's one. The following analysis are valid also for the relative regions where the operative points are located. A PI control loop was implemented by setting a control bandwidth equal to $4Hz$ for all experimental tests. All the comparisons are performed paralleling the new modulation strategy with Venturini's method at the same switching

frequency. The latter has been chosen such that the THD on input current is equal for both modulations in the first operative point. This condition will, of course, change in the second operative point. To achieve this, the switching frequency is established to be $13kHz$, which corresponds to a THD on input current of 8.6 for both modulations.

6.2.1 First operative point

To obtain an operative point inside this region, taking into account the output parameters listed in Tab 6.2, and fixing the voltage transfer ratio to the maximum value, the output frequency is chosen equal to $100Hz$ so the PF value is 0.9992, which corresponds to $\varphi_0 \cong \frac{\pi}{80}$.

Quantity	Value	U.M
Load inductance	1.1	μH
Load resistance	17.5	Ω

Table 6.2: Output load parameters

In Fig. 6.3 and Fig.6.4, the unfiltered line-to-line output voltage obtained with the new modulation and the Venturini's modulation are shown respectively. It is possible to appreciate the cornerstone of the hybrid modulation technique, that is employing the closest input voltages in synthesizing the output ones. In fact, it is possible to note that in different moments, the unfiltered amplitude voltage swing is reduced accordingly, and this is especially evident in those areas around the output peaks.

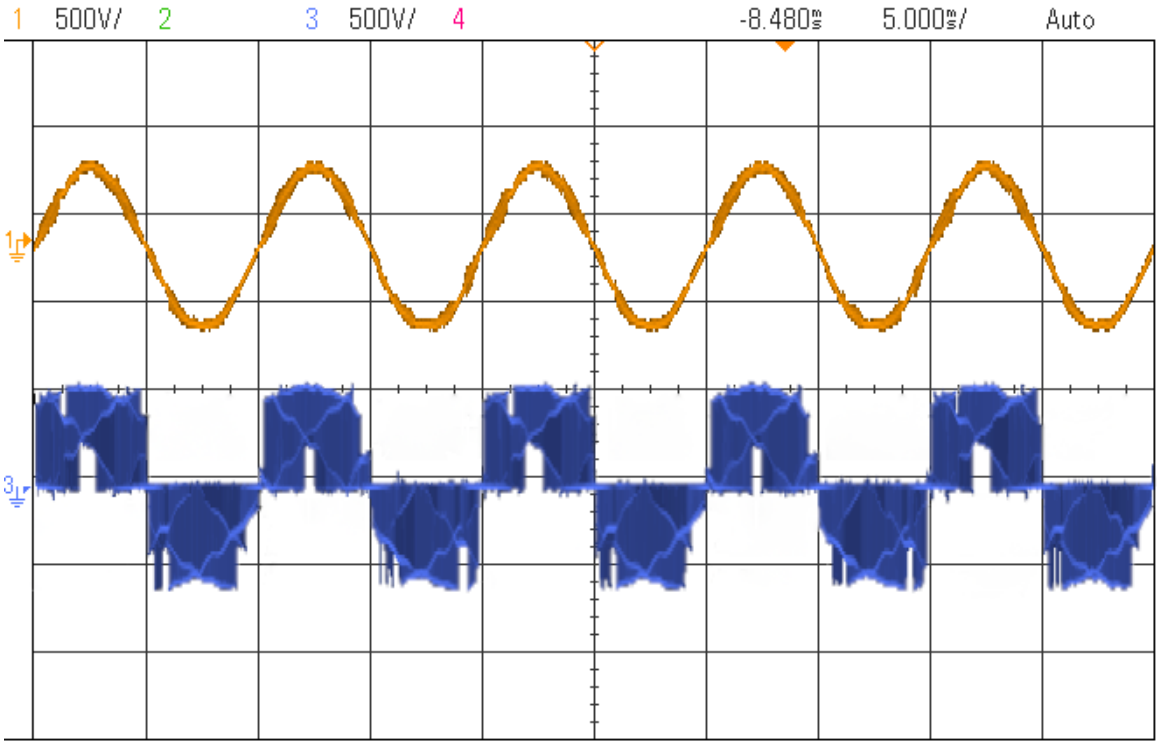

Figure 6.3: Hybrid modulation output waveform acquisitions
Line-to-line filtered Input Voltage (ocher,$500V/div$)
Line-to-line unfiltered Output Voltage (blue, $500V/div$)
Time scale : $5ms/div$

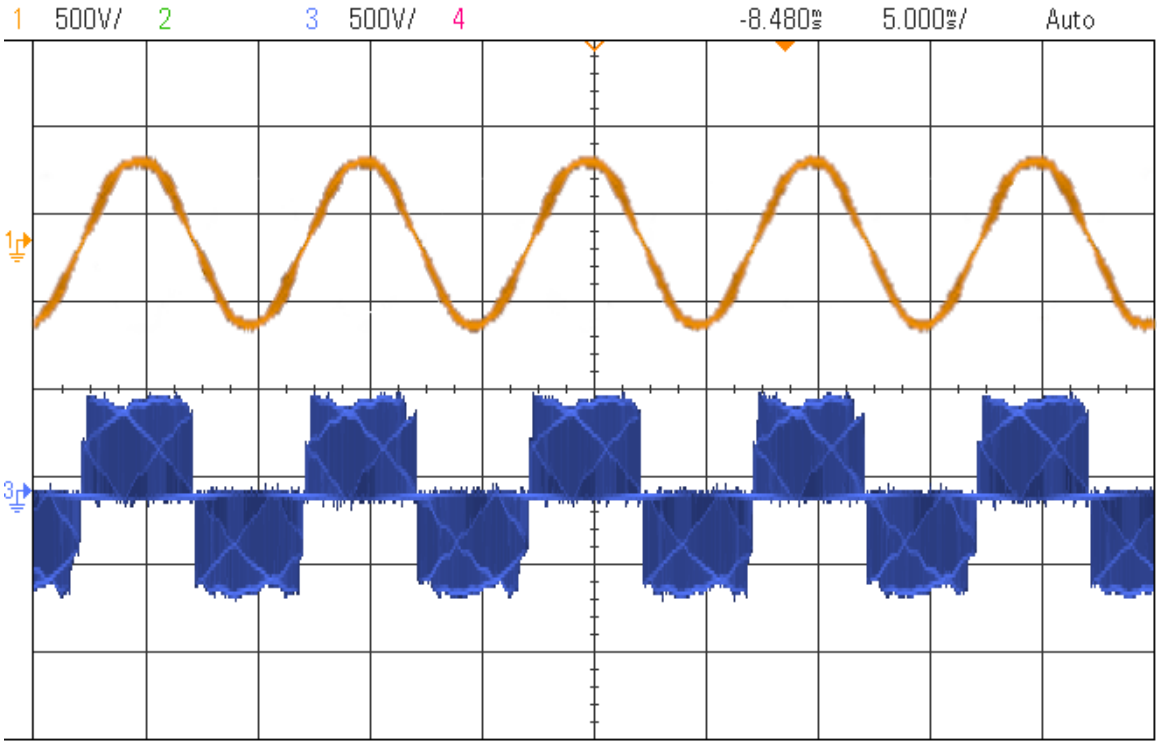

Figure 6.4: Venturini's modulation output waveform acquisitions
Line-to-line filtered Output Voltage (ocher, $500V/div$)
Line-to-line unfiltered Output Voltage (blue, $500V/div$)
Time scale : $5ms/div$

In Fig. 6.5 and in Fig. 6.6, input-output voltages and currents achieved with the new modulation and Venturini's modulation are shown respectively. In particular, in both figures, the orange waveform represents the phase input voltage related to phase A; the green waveform indicates the input current related to the same input phase; the blue line identifies the line-to-line output voltage measured across phases c and b, and finally, magenta waveform depicts the output current of phase b.

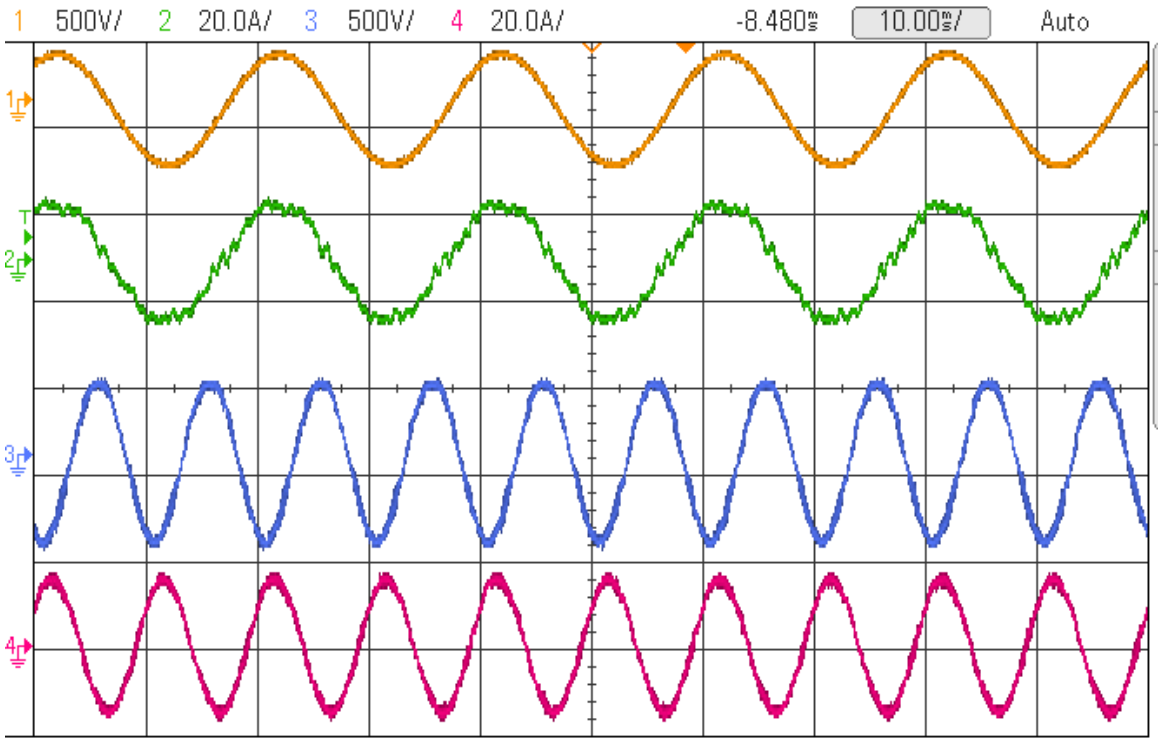

Figure 6.5: Hybrid modulation acquisitions in operative point 1
Line-to-line Input Voltage (ocher, $500V/div$)
Line input current (green, $20A/div$)
Line-to-line filtered Output Voltage (blue, $500V/div$)
Line output current (violet, $20A/div$)
Time scale : $10ms/div$

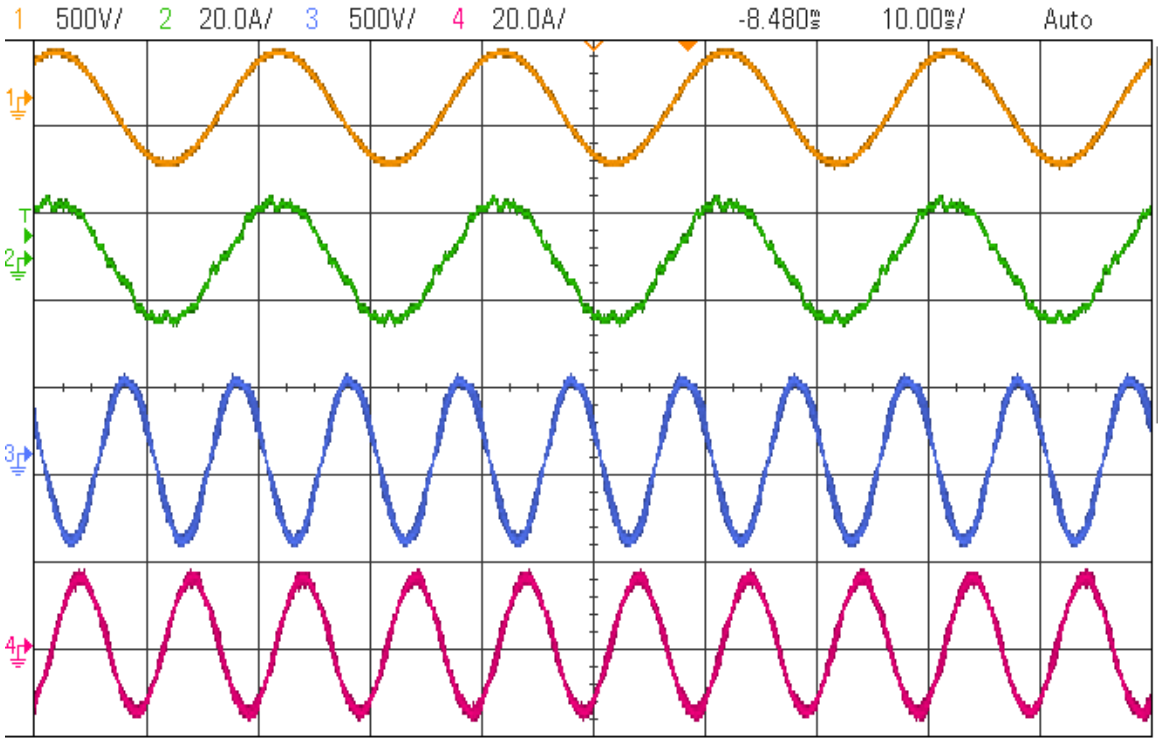

Figure 6.6: Venturini modulation acquisitions in operative point 1
Line-to-line Input Voltage (ocher, $500V/div$)
Line input current (green, $20A/div$)
Line-to-line filtered Output Voltage (blue, $500V/div$)
Line output current (violet, $20A/div$)
Time scale: $10ms/div$

Fig. 6.7 shows the harmonic spectra of the input current obtained with the hybrid modulation technique, while Fig. 6.8 shows the harmonic spectra of the input current obtained with the Venturini's modulation technique. It can be noted that the harmonic spectra are quite similar : this is due to the fact that this particular working point is chosen to be at same THD for both the techniques.

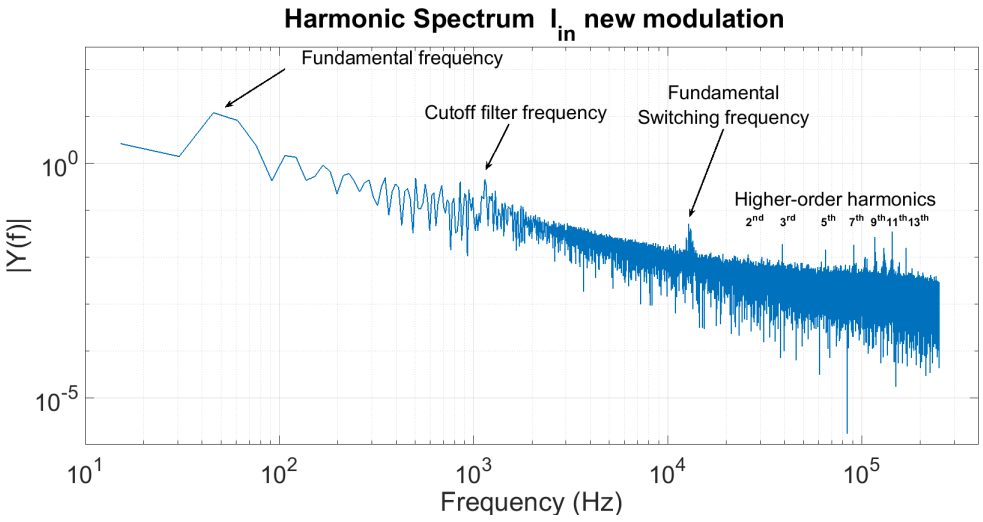

Figure 6.7: Harmonics Spectrum of input current achieved with Hybrid modulation with output frequency 100Hz

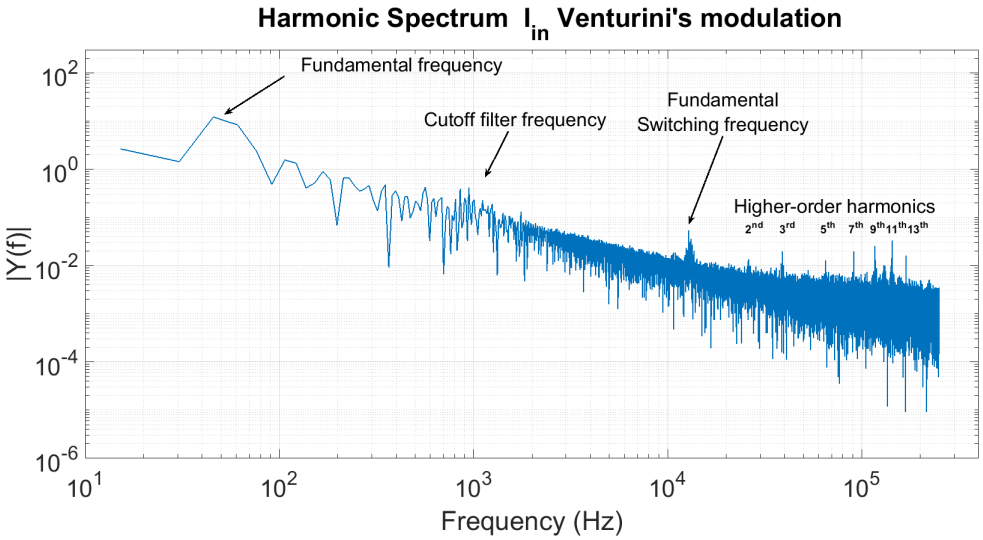

Figure 6.8: Harmonics Spectrum of input current achieved with Venturini's modulation with output frequency 100Hz

Harmonic spectra of output current (Fig. 6.9 Fig. 6.10) demonstrate that a lower harmonic content can be achieved by applying a new modulation strategy. In fact, the harmonic

components at the switching frequency and the higher-order switching harmonics are reduced for proposed modulation. That is reflected on THD, analytically computed on all harmonics, which stands at 6.70 for the hybrid modulation versus 7.70 obtained with the Venturini's one.

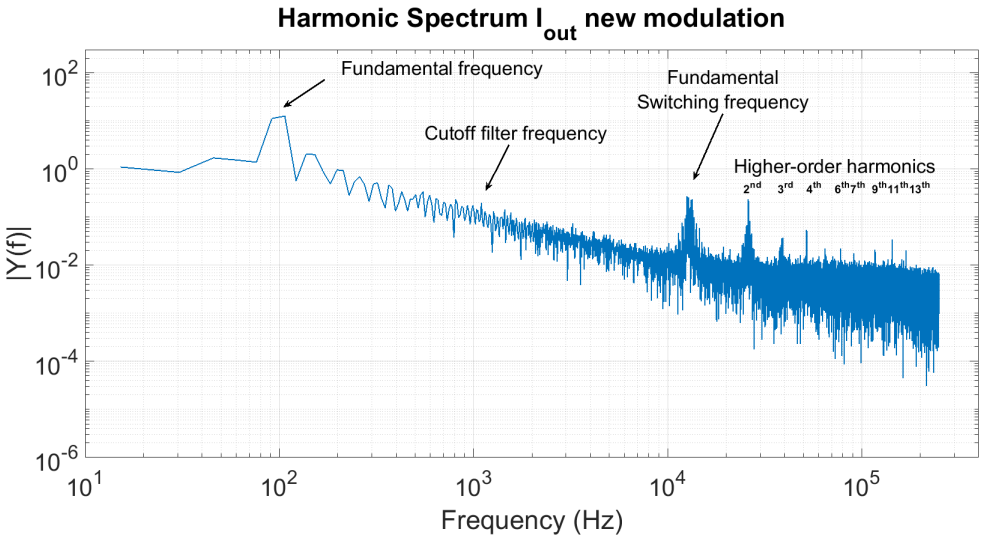

Figure 6.9: Harmonics Spectrum of output current achieved with hybrid modulation with output frequency set to 100Hz.

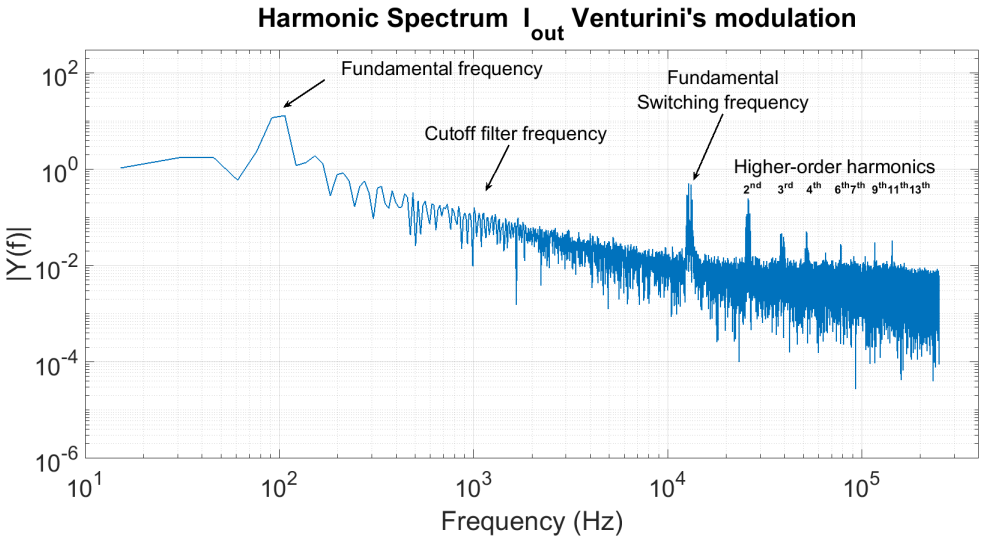

Figure 6.10: Harmonics Spectrum of output current achieved with Venturini's modulation with output frequency set to 100Hz.

6.2.2 Second operative point

To achieve an operative point which falls in the hybrid region and to maintain the same hardware configuration of table 6.1, the output frequency of this operative point is set to be $250Hz$. This permits to lower the power factor to the value of 0.9952 which corresponds to $\varphi_0 \cong \frac{\pi}{32}$. As expected, in this condition, the Venturini's modulation distorts less the input current (9%) when compared to the hybrid one (10.5%) . However, the hybrid modulation's THD on output current is still lower (6.7%) than that obtained with Venturini's modulation (7.6%).

6.2.3 Efficiency

In this section, efficiency comparisons are conducted in order to highlight how the proposed technique can affect it. The comparisons have been performed for five minutes during a continuative test in the same operative points listed in 6.2.1 and 6.2.2. The test consisted of acquiring the efficiency data through a PPA5530-N4L Power analyzer and to measure the temperature of the modules by using the integrated NTCs. In particular, input and output data are acquired measuring the total losses in the power electronic devices and input filter

at the same time. Since the comparisons are performed for equal THD in one of the two considered operative points and the harmonic spectra for both modulations are very similar in that case as shown in Fig.6.7 and Fig.6.8, it is reasonable to assume that the computed efficiency does not involve the harmonic response of the input filter. The acquired data depicted in Fig. 6.11 and Fig. 6.12 show the efficiency of proposed modulation compared to the Venturini's. These figures show the raw efficiency data and the related linear regression, where can be appreciate a better efficiency for proposed modulation either in case it works with the support of the Venturini's modulation (output frequency set to $250Hz$, Fig. 6.12) and when it works alone (output frequency equal to $100Hz$, Fig. 6.11).

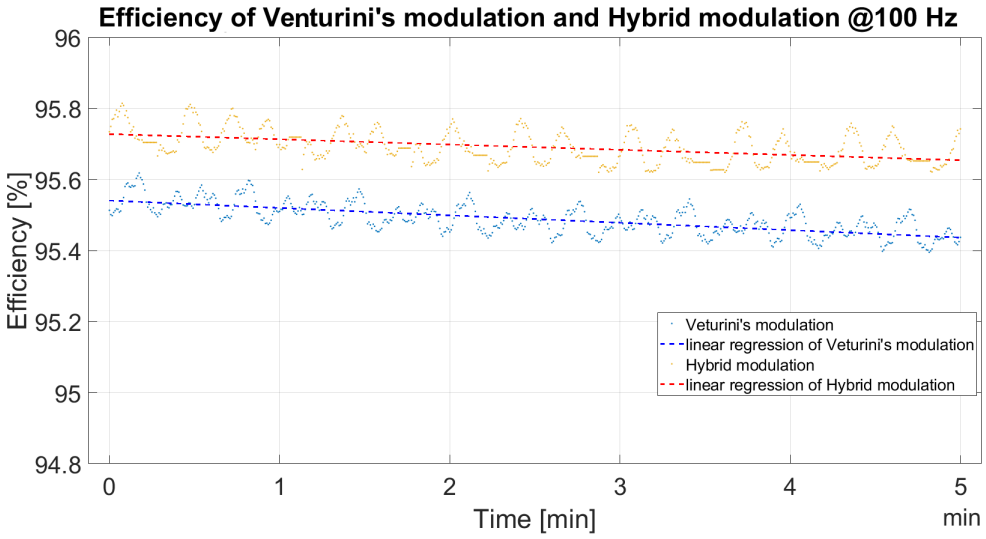

Figure 6.11: Efficiency graph of Hybrid modulation vs. Venturini's modulation with output frequency 100Hz

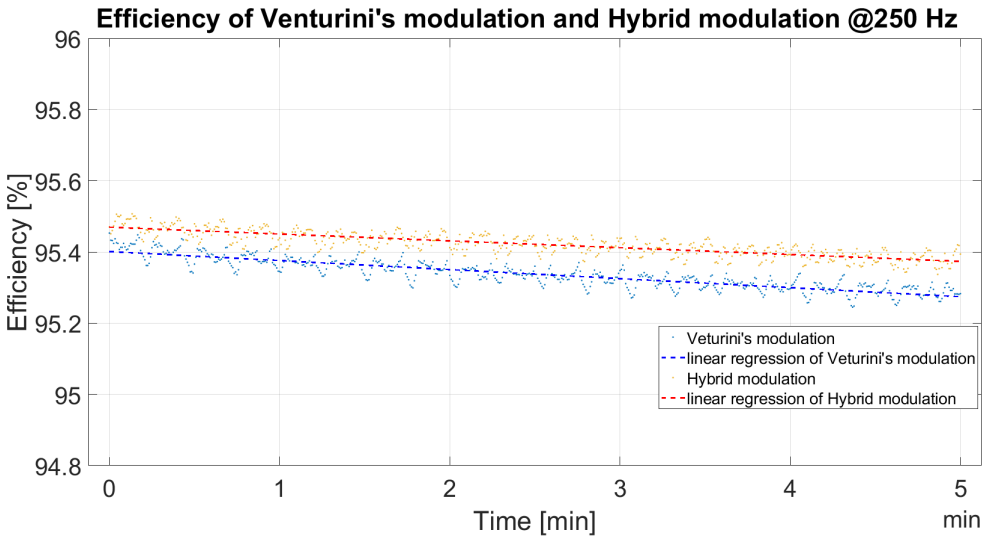

Figure 6.12: Efficiency graph of Hybrid modulation vs. Venturini's modulation with output frequency 250Hz

Since using the hybrid modulation implies to swap to the Venturini's technique when necessary, the output voltage is composed in these cases by using all three-phase input voltages. Accordingly, the losses for the hybrid modulation in the second operative point are higher then those achieved when the Calvini's technique is assisted by the Venturini's but anyway lower than those achieved through the Venturini's modulation alone. Consequently, the highest efficiency is achieved when the new modulation is used alone (0.2 increase compared with Venturini's) which corresponds in terms of power to $135W$ referred to the rated power of $6.8kW$. These behavior are confirmed by thermal data which have been acquired by comparing the temperatures obtained in all modulations (Fig. 6.13 and Fig.6.14). After five minutes, the temperature gaps between the new and hybrid modulation compared to Venturini's modulation achieve three degrees when the new technique works alone and two degrees when the hybrid modulation is used.

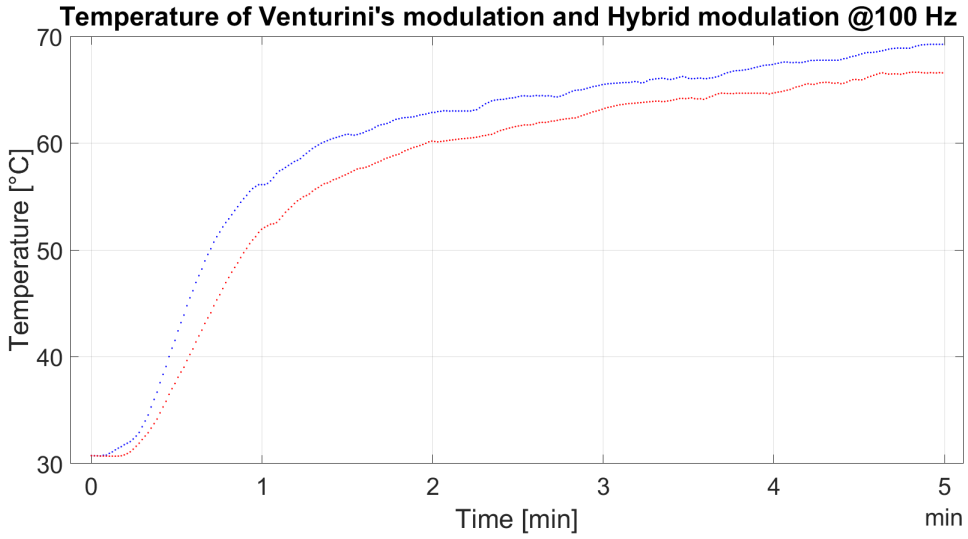

Figure 6.13: Thermal results with output frequency 100Hz
Temperature with Hybrid modulation (red dotted line, $10°C/div$)
Temperature with Venturini modulation (blue dotted line, $10°C/div$)
Time scale: $1min/div$

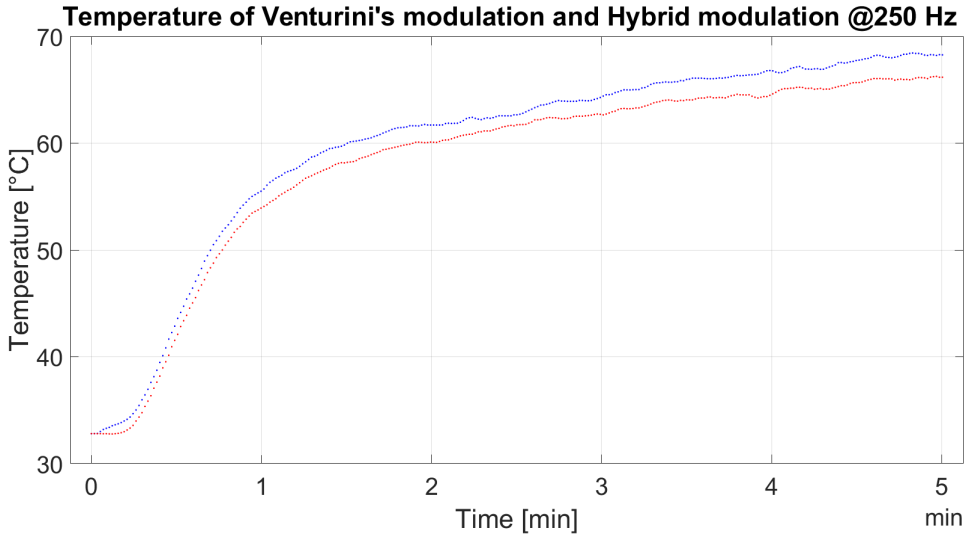

Figure 6.14: Thermal results with output frequency 250Hz
Temperature with Hybrid modulation (red dotted line, $10°C/div$)
Temperature with Venturini modulation (blue dotted line, $10°C/div$)
Time scale: $1min/div$

Chapter 7

Conclusions

7.1 Closing Comments

A new extremely compact 250kW matrix converter has been developed, offering unrivaled mass and volumetric power densities. All the hardware has been designed and built from scratch, thus permitting to optimize the system as a whole entity.

All the hardware pieces have been thoroughly tested, and, in the end, found compliant with the expectations.

This process was not without errors, and required a lot of efforts. Modern computing resources where used where possible, in order to verify all the analytical approaches that were used in the design processes. In particular, CFD and FEM analysis helped in optimizing their related components, saving time and granting an higher degree of confidence in terms of those second order (and higher) behaviors that usually are not taken into account in the dimensioning. However, this approach was not applicable to all the system components, in particular to all the electronic boards. These, in fact, required a lot of iterations and a lot of tuning before becoming fully functional, especially the gate driver boards, which also required FPGA programming before all the tests were carried out.

Moreover, a new modulation strategy for Matrix converters has been introduced and validated onto the prototype, that is the Calvini's modulation. The key concept behind it is to synthesize the output voltage only by switching between the two closest input voltages instead of all the three phases voltages, calculating the duty cycle accordingly. This way, it

is intuitive to perceive that the switching losses can be significantly reduced, enhancing the system efficiency, as well as to understand that the output current ripple becomes smaller. This, however comes with the cost of dramatically reducing the operative area where maximum VTR can be achieved. Nevertheless, whenever the load demands a smaller power factor, this drawback can be offset while maintaining the benefits of the Calvini modulation strategy, by implementing the Calvini's modulation along with the traditional Venturini's one, in what is called hybrid modulation technique. To validate both the new modulation and the hybrid technique, significant experimental tests have been carried out on our 250 kW Matrix converter. The experimental results have highlighted that, compared with traditional Venturini's modulation, the hybrid method achieves higher efficiency and a lower harmonic content in the output currents, despite having a higher THD on the input currents. However, a lower THD on output currents is also achieved when new modulation works alone, with the additional benefits to match the same THD on the input current and the highest efficiency.

Unfortunately, up to now, it was not possible to test the converter at full power due to the lack of a suitable electrical source and a of chiller unit, and so to obtain the results of the previous chapter in the nominal point. The author, however, after having verified the proper functioning of the system, is persuaded that these results will not be far from those presented in the simulations. Anyways, this shortcoming will be addressed in the immediate future, as the unit will be soon transferred to the high-power area of the university of Nottingham, where it will be tested along with another identical converter and two motors in motor-brake configuration.

7.2 Future work

Matrix converters are becoming an attractive alternative to traditional back-to-back converters, especially where reverse power flow is needed along with high power density, in a world where power electronic conversion equipment is becoming more and more endemic in everyday life, and it is expected to gain even more momentum with the imminent electrification of the private transportation system. In this respect, while on-vehicle converters only require a DC/AC conversion stage in order to feed the motor, the same does not

true for what concerns the off-line battery chargers. These systems, in fact, being at their core AC/DC converters, require multiple stages due to the necessity of guaranteeing galvanic isolation between charger and vehicle, and so are typically realized with an isolation transformer in combination of cascade AC/DC/AC/DC stages. The author is persuaded that these converters would greatly benefit from a reduced AC/AC/DC power stage, that could be realized with a Matrix topology always working under the Calvini's modulation requirements, since the VTR limit would be a lesser problem thanks to the isolation transformer. The inherent bidirectionality of the Matrix converter would also enable the much sought-after stabilization of the grid by means of harvesting energy from the batteries of the vehicles connected to the grid, which is a feature that is going to be necessary for the efficient exploitation of the proliferating renewable energy sources.

7.3 Acknowledgments

The author would like to thank all the following people that, in a way or another, took part in reaching the goals of this thesis.

- First and foremost, my family and my loved one, for helping me to stay on track even in my darkest hour. Sanity is a luxury when your mind is twisted as mine.
- My friends, for all the laughs that we made together and all the discussions that stirred my curiosity. You are the spice of life, and I do like spices, as much is I like a good beer.
- Marco Calvini, my mentor and teacher, and of course the inventor of the Calvini's modulation. *Words cannot express my immense gratitude towards you.* You are one of the most brilliant person I've ever met in my entire life and I'm honored of having the opportunity of working beside you and learning from you. I'm always amazed by how you are capable of obtaining the greatest results from simplest intuitions.
- Marco Venturini, CEO of Phase Motion Control and one of the Matrix converter pioneers, for always fueling all the research activities in the company, and for all the good advice that he gave me.

- Davide Tenti, technical director of Phase Motion Control, for letting me work beside Marco Calvini, and for having taught me what truly is the sense of proportion.
- Andrea Formentini's research group at the university of Nottingham and Pasquale Picece at Phase Motion Control, who worked on the project.
- All my colleagues at Phase Motion Control R&D laboratory. All of you helped me in some way and I owe you one.
- Gabriele Bino, my old time friend and colleague, for all the serious and not-so-serious discussion that we made in the hallways. Don't let the 1000-faces demon catch you, or you'll be closed forever in a room with Hi-ho and Winnie the Pooh arguing about possible dangers, like having a newborn splitting a $35mm^2$cable in two with his own hands.