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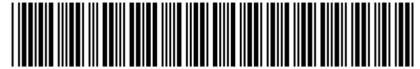

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(54) **DOUBLE-CHANNEL HEMT DEVICE AND MANUFACTURING METHOD THEREOF**

(57) An HEMT device (1), comprising: a semiconductor body (15) including a heterojunction structure (13); a dielectric layer (7) on the semiconductor body; a gate electrode (8); a drain electrode (12), facing a first side (8') of the gate electrode (8); and a source electrode (10), facing a second side (8") opposite to the first side (8') of the gate electrode; an auxiliary channel layer (20), which extends over the heterojunction structure (13) between the gate electrode (8) and the drain electrode (12), in electrical contact with the drain electrode (12) and at a distance from the gate electrode, and forming an additional conductive path for charge carriers that flow between the source electrode and the drain electrode.

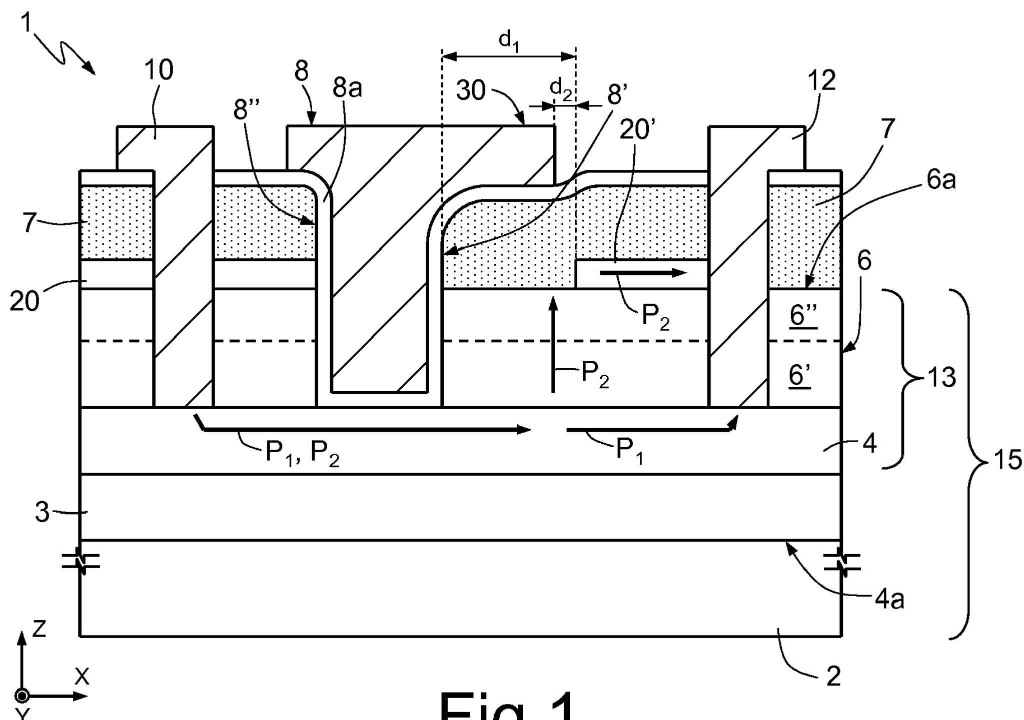

Fig.1

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Description

[0001] The present invention relates to an HEMT device and to a method for manufacturing the same.

[0002] Known to the art are HEMTs with heterostructure made, in particular, of gallium nitride (GaN) and gallium and aluminium nitride (AlGaN). For example, HEMT devices are appreciated for use as power switches thanks to their high breakdown threshold. In addition, the high current density in the conductive channel of the HEMT enables a low ON-state resistance (R_{ON}) of the conductive channel.

[0003] In order to favour use of HEMTs in high-power applications, recessed-gate HEMTs have been introduced.

[0004] A problem with devices of this type regards the drastic reduction of current, due to an increase of the ON-state resistance (R_{ON}), during switching operations. The temporary increase in the R_{ON} value after high-voltage biasing (400-600 V) in the OFF state is deemed to be caused by an excessive trapping of the charge carriers in the channel, in the buffer layer, or at the surface.

[0005] In order to reduce this problem, various solutions have been adopted.

[0006] The document by D. Jin et al., "Total current collapse in High-Voltage GaN MIS-HEMTs induced by Zener trapping", Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, U.S.A., represents a method of control of defects during the stage of epitaxial growth of the channel and an appropriate design of the "field plate" structures. This method, however, does not solve the problem and requires a control of the growth stage, which has an impact on the costs of industrial production of HEMTs.

[0007] The document by P. Moens et al., "On the Impact of Carbon-Doping on the Dynamic Ron and Off-state Leakage Current of 650V GaN Power Devices", ON Semiconductor, suggests that the optimization of the doping profile with carbon atoms of the semiconductor body of the HEMT at the level of the buffer layer may provide a solution to the aforementioned problem. However, the presence itself of impurities such as carbon atoms may itself be the cause of further trapping of carriers and R_{ON} degradation.

[0008] The document by J. Würfl et al., "Techniques towards GaN power transistors with improved high voltage dynamic switching properties", 2013, discusses the limitation of dynamic switching in a GaN power device and proposes techniques for improving fast switching at high voltage by modifying the structure of the buffer layer of an HEMT. The aforementioned problems, however, are not solved.

[0009] There is thus felt the need to provide an HEMT device and a manufacturing method thereof that are alternative to the ones proposed according to the prior art, and that will overcome the drawbacks set forth above.

[0010] According to the present invention, an HEMT device and a manufacturing method thereof are thus provided, as defined in the annexed claims.

[0011] For a better understanding of the present invention, preferred embodiments thereof are now described, purely by way of nonlimiting example and with reference to the attached drawings, wherein:

- Figure 1 shows, in lateral sectional view, an HEMT device according to one embodiment of the present disclosure;
- Figure 2 shows, in lateral sectional view, an HEMT device according to a further embodiment of the present disclosure;
- Figure 3 shows, in lateral sectional view, an HEMT device according to a further embodiment of the present disclosure;
- Figure 4 shows, in lateral sectional view, an HEMT device according to a further embodiment of the present disclosure;
- Figure 5 shows, in lateral sectional view, an HEMT device according to a further embodiment of the present disclosure;
- Figures 6A-6E show, in lateral sectional views, successive manufacturing steps of the HEMT device of Figure 1; and
- Figure 7 shows the plot of the drain current of the HEMT device of Figure 1 in different conditions of drain voltage, compared with an HEMT device according to the known art.

[0012] Figure 1 shows, in a triaxial system of axes X, Y, Z orthogonal to one another, an HEMT device 1 of a normally-off type, based upon gallium nitride, including a substrate 2, made, for example, of silicon, or silicon carbide (SiC) or sapphire (Al_2O_3); a buffer layer 3, of gallium and aluminium nitride (AlGaN) or of gallium and indium nitride (InGaN) or, in general, of AlGaN or InGaN alloys, which extends over the substrate 2 and is designed to enable a better depletion of the two-dimensional electron gas (2DEG) in the overlying conductive channel; a channel layer 4, of gallium nitride (GaN) or intrinsic InGaN, which extends over the buffer layer 3 and has a thickness comprised between approximately 10 nm and 2 μm, approximately 1 μm; a barrier layer 6, of intrinsic aluminium and gallium nitride (AlGaN) or, more in general, of compounds based upon ternary or quaternary alloys of gallium nitride, such as AlxGa1-xN, AlInGaN, InxGa1-xN, AlxIn1-xAl, which extends over the channel layer 4 and has a thickness comprised between approximately 5 nm and 400 nm, e.g. approximately 15 nm; an insulation layer 7, of dielectric material such as silicon nitride (Si_3N_4) or silicon oxide (SiO_2), which extends over a front side 6a of the barrier layer 6; and a gate region 8, which extends in the semiconductor body 3 between a source region 10 and a drain region 12.

[0013] The substrate 2, the buffer layer 3, the channel layer 4, the barrier layer 6, and the insulation layer 7 lie in respective planes parallel to the plane XY and are stacked on one another in the direction Z.

[0014] The channel layer 4 and the barrier layer 6 form a heterostructure 13. The substrate 2, the buffer layer 3, and the heterostructure 13 are defined, as a whole, by the term "semiconductor body 15".

[0015] The gate region 8 is separated and insulated laterally (i.e., along X) by the source region 10 and drain region 12 by respective portions of the insulation layer 7. The gate region 8 is of a recessed type; i.e., it extends in depth through the insulation layer 7 and completely through the barrier layer 6, as far as the channel layer 4.

[0016] In other words, the gate region 8 is formed in a trench 9 dug through the insulation layer 7 and the barrier layer 6.

[0017] A gate dielectric layer 8a extends in the trench 9 facing the bottom and the side walls of the trench 9. The gate dielectric 8a may further extend, optionally, outside of the trench 9, i.e., on the insulation layer 7. A gate metallization 8b completes filling of the trench 9 and extends over the gate dielectric layer 8a. The gate dielectric layer 8a and the gate metallization 8b form the gate region 8 of the HEMT device 1.

[0018] The gate region 8 has a first side 8' facing the drain region 12 and a second side 8" facing the source region 10. The first and second sides 8', 8" of the gate region 8 extend, at least in part, parallel to one another and to the plane XY.

[0019] According to one aspect of the present disclosure, an auxiliary channel 20 extends over a front side 6a of the barrier layer 6 between, and electrically coupled to, the source region 10 and the drain region 12. In particular, the auxiliary channel 20 extends between the first side 8' of the gate region 8 and the drain region 12, and between the second side 8" of the gate region 8 and the source region 10. However, the portion of auxiliary channel that extends between the gate region 8 and the source region 10 may be absent.

[0020] In even greater detail, the auxiliary channel 20 extends between, and in contact with, a portion of the source region 10 and a respective portion of the gate oxide 8a that defines the second side 8" of the gate region 8, and further in direct contact with the drain region 12. However, the auxiliary channel 20 is not in direct contact with the first side 8' of the gate region 8, but at a distance therefrom. Thus, the auxiliary channel 20 extends in the proximity of the first side 8' without ever being in direct contact therewith. The auxiliary channel 20 extends at a distance d_1 (measured in the direction X) from the first side 8' of the gate region 8 chosen so that the electrical field is not excessively high on the first side 8'. An electrical field is considered too high if it causes, or may cause, breakdown of the gate dielectric.

[0021] The present applicant has found that values of the distance d_1 equal to, or greater than, 0.5 μm are sufficient to satisfy the aforementioned conditions for the choice of d_1.

[0022] According to one embodiment of the present disclosure, in the presence of a gate field plate 30, the auxiliary channel 20 extends laterally staggered with respect to the metal layer that provides the field plate 30 by a maximum distance (measured along X) not greater than a value d_2. The value of distance d_2 is chosen so that there do not arise the problems, discussed with reference to the known art, of depletion of the two-dimensional gas (2DEG) and increase of the ON-state resistance as a result of the trapping phenomena. The exact choice of d_2 may be made experimentally, by experimental tests on a test device.

[0023] The present applicant has found that values of the distance d_2 equal to, or smaller than, 0.5 μm are such as to overcome the drawbacks of the known art.

[0024] The auxiliary channel 20, according to one embodiment, is made of gallium nitride (GaN) with an N-type doping, in particular with a density of dopant species comprised between $1\cdot10^{18}$ cm^{-3} and $1\cdot10^{19}$ cm^{-3}, in particular $1\cdot10^{18}$ cm^{-3}. In this case, the thickness of the auxiliary channel 20 is comprised between 5 nm and 100 nm, in particular 50 nm.

[0025] According to an alternative embodiment, shown in detail in Figure 2, the auxiliary channel 20 is a heterostructure including a layer of gallium and aluminium nitride (AlGaN) 22 overlying a layer of gallium nitride (GaN) 24. The AlGaN layer 22 has a thickness comprised between 5 nm and 50 nm, with aluminium concentration comprised between 15% and 50% (for example, 25%); the GaN layer 24 has a thickness comprised between 2 nm and 50 nm, for example 8 nm.

[0026] With reference to the barrier layer 6, in both of the embodiments of Figures 1 and 2, it is preferably formed by two intermediate AlGaN layers 6', 6" having concentrations of aluminium different from one another. According to an aspect of the present disclosure, the concentration of aluminium in the second intermediate layer 6" is lower than the concentration of aluminium in the first intermediate layer 6'. In particular, the first intermediate layer 6', which extends in direct contact with the channel layer, is made of AlGaN with a concentration of aluminium comprised between 10% and 40%, for example 25%, whereas the second intermediate layer 6", which extends directly over the first intermediate layer 6', is made of AlGaN with a concentration of aluminium lower than the previous one, namely, comprised between 5% and 30%, for example 15%, or else with a profile of concentration of aluminium decreasing in the direction Z moving away from the first intermediate layer 6' (e.g., 30% of aluminium at the interface with the first intermediate layer 6' and 5% of aluminium at the front side 6a). The second intermediate layer 6" further includes silicon doped with N-type dopant species.

[0027] This conformation of the barrier layer 6 enables reduction of the barrier between the auxiliary channel 20 and the barrier layer 6.

[0028] During operation of the HEMT 1, the charge carriers flow from the source region 10 to the drain region 12, following the conductive paths designated by P_1 and P_2 in Figure 1. As may be noted, in the portion of active area comprised between the gate region 8 and the source

region 10, the conductive paths P_1 and P_2 coincide; instead, in the portion of active area comprised between the gate region 8 and the drain region 12, the conductive paths P_1 and P_2 do not coincide. Here, part of the charge carriers flows towards the drain region 12 passing through the two-dimensional electron gas (2DEG) in the channel 4 (path P_1), whereas part of the charge carriers flows towards the drain region 12 passing through the two-dimensional gas (2DEG) in the channel 4, the barrier layer 6, and the auxiliary channel 20.

[0029] The choice, by the charge carriers, of the conductive path P_1 or P_2 is a function of the electrical resistance encountered in said path by the charge carriers.

[0030] In the case of undesired increase of the resistance R_{ON} in the channel layer 4 (as a result of the known trapping phenomena) the conductive path P_2 is privileged over the conductive path P_1. In this way, during switching operating conditions of the HEMT 1 where, as a result of the traps in the channel layer 4, the resistance R_{ON} increases, there always exists an alternative path for the current, i.e., the one offered by the auxiliary channel 20.

[0031] Operation of the HEMT device 1 is thus not inhibited by the traps in the channel layer 4.

[0032] The distance d_1 between the first side 8' of the gate region 8 and the auxiliary channel 20 guarantees that, at the operating voltages considered (e.g., 400 and 600 V), the electrical field at the gate region 8 is not of an excessively high value such as to break the gate oxide 8a.

[0033] According to a further aspect of the present disclosure, illustrated in Figure 3, the HEMT 1 (according to any of the embodiments of Figure 1 or Figure 2) further has a field-plate metal layer 30, which extends as prolongation of the gate metallization 8b towards the drain region 12 until it overlies (in top plan view or, equivalently, in the direction Z) the auxiliary channel 20. The auxiliary channel 20 and the field-plate metal layer 30 are separated from one another by the insulation layer 7 and, if present, the gate dielectric 8a.

[0034] As an alternative to the field-plate metal layer 30 of a gate-connected type, there may be present one or more field plates of the source-connected type, i.e., electrically coupled to the metallization of the source region 10, as illustrated in Figure 5 (a source-connected field plate is identified by the reference number 34).

[0035] With reference to Figure 4, the field-plate metal layer 34 extends between the gate region 8 and the drain region 12 in parallel to the auxiliary channel 20, until it overlaps the latter (in top plan view or, equivalently, in the direction Z). The auxiliary channel 20 and the field-plate metal layer 34 are separated from one another by the insulation layer 7, by a passivation layer 32 and, if present, by the gate dielectric 8a. The passivation layer 32 has the function of insulating electrically the field-plate metal layer 34 from the gate region 8.

[0036] According to a further embodiment shown in Figure 5, the auxiliary channel 20 extends laterally staggered (in the direction X) with respect to the field-plate metal layer 34, i.e., not overlapping it (in the direction Z).

[0037] In this case, the maximum distance, measured in the direction X, between the edge that delimits the end of the field-plate metal layer 34 and the edge that defines the start of the auxiliary channel 20 is d_3 and has a value chosen so that there is not created a 2DEG region excessively depleted from the traps present in the buffer.

[0038] The value of d_3 is, in particular, equal to, or less than, 0.5 μm.

[0039] When both the gate field plate 30 and the source field plate 34 are present, the auxiliary channel 20 extends so that it is in at least one of the two conditions mentioned above with reference to Figures 3-4, i.e., that (i) the auxiliary channel 20 at least partially overlaps one between the gate field plate 30 and the source field plate 34; and/or (ii) the auxiliary channel 20 extends staggered with respect to both the gate field plate and the source field plate 30, 34 and at a distance, measured in the direction X, not greater than d_2 or d_3 from at least one between the gate field plate 30 and the source field plate 34.

[0040] Described in what follows, with reference to Figures 6A-6E, are steps for manufacturing the HEMT device 1 of Figure 1.

[0041] Figure 6A shows, in cross-sectional view, a portion of a wafer 50 during a step for manufacturing the HEMT device, according to one embodiment of the present invention. Elements of the wafer 50 that are common to the ones already described with reference to Figure 1 and shown in Figure 1, are designated by the same reference numbers and are not described in detail any further.

[0042] In particular, the wafer 50 is provided, comprising: the substrate 2, made, for example, of silicon (Si) or silicon carbide (SiC) or aluminium oxide (Al_2O_3), having a front side 2a and a rear side 2b opposite to one another in a direction Z; the buffer layer 3 on the front side 2a of the substrate 2, of aluminium and gallium nitride (AlGaN) or of gallium and indium nitride (InGaN); the channel layer 4, of gallium nitride (GaN), having its own underside 4a that extends adjacent to, and overlying, the buffer layer 3; and the barrier layer 6, which extends over the channel layer 4. The barrier layer 6 and the channel layer 4 form the heterostructure 13.

[0043] According to the present disclosure, formation of the barrier layer 6 envisages: formation of a first intermediate layer 6' on the channel layer by depositing AlGaN (e.g., via MOCVD or MBE) until a thickness is reached comprised between 5 nm and 20 nm, for example, 8 nm; and formation of a second intermediate layer 6" by depositing AlGaN and doped silicon with a doping level of $1 \cdot 10^{18}$ cm^{-3} on the first intermediate layer 6', until a thickness comprised between 5 nm and 20 nm, for example 8 nm, is reached.

[0044] During deposition of the first intermediate layer 6', the concentration of aluminium is adjusted so that it is comprised between 10% and 40%; during deposition of the second intermediate layer 6", the concentration of

aluminium is adjusted so that it is comprised between 50% and 30%.

[0045] Alternatively, the second intermediate layer 6" is formed so that it has a profile of concentration of aluminium decreasing in the direction Z moving away from the first intermediate layer 6' (e.g., 30% of aluminium at the interface with the first intermediate layer 6' and 5% of aluminium at the front side 6a).

[0046] Next, on the front side 6a of the barrier layer 6 an auxiliary channel layer 56 is formed, for example by depositing gallium nitride, GaN, with N-type doping (e.g., by MOCVD or MBE), according to the embodiment already described with reference to Figure 1.

[0047] Alternatively, according to the embodiment of Figure 2, the auxiliary channel layer 56 is formed by depositing a first layer of gallium nitride (GaN), of an intrinsic type and, then, over it, an AlGaN layer. Deposition of both the GaN layer and the AlGaN layer that form the auxiliary channel layer 56 is carried out by deposition (e.g., via MOCVD or MBE), modulating selectively the desired amount of aluminium in both layers.

[0048] Then (Figure 6B), a step of masked etching of the auxiliary channel layer 56 is carried out to remove first selective portions thereof at a region 57' where, in subsequent machining steps, the gate trench 9 will be formed, and to remove further second selective portions of the auxiliary channel layer 56 that extend alongside the region 57' for a length, in the direction X, equal to d_1 (region 57" identified in Figure 6B). In particular, the removed second selective portions of the auxiliary channel layer 56 extend as lateral prolongation of the first selective regions, towards the portion of wafer 50 that will house the drain region of the HEMT device 1. This process step defines the distance d_1 between the drain region 8 and the auxiliary channel 20, as described previously.

[0049] Then, once again with reference to Figure 6B, formed on the wafer 50 (and thus on the auxiliary channel layer 56 thus structured and at the regions 57', 57") is a passivation layer 52, of dielectric or insulating material, for example silicon nitride (SiN) or silicon oxide (SiO_2). The passivation layer 52 has a thickness comprised between 5 nm and 300 nm, for example 100 nm, and is formed by CVD or atomic-layer deposition (ALD), and, at the end of the manufacturing steps, will form the insulation layer 7.

[0050] Next (Figure 6C), the passivation layer 52 is selectively removed, for example by lithographic and etching steps, for removing selective portions thereof in the region 57' of the wafer 50 where the gate region 8 of the HEMT device 1 is to be formed.

[0051] The etching step may stop at the underlying barrier layer 6 (to provide an HEMT of a normally-on type), or else it may proceed partially into the barrier layer 6 (the latter embodiment is shown in Figure 6B). In this second case, a surface portion 4' of the underlying channel layer 4 is exposed. Etching of the barrier layer 6 is carried out, for example, by dry etching.

[0052] The trench 9 is thus formed, which extends throughout the thickness of the passivation layer 52 and for an underlying portion of the barrier layer 6.

[0053] There is then formed, for example by deposition, the gate-dielectric layer 8a, made, for example, of a material chosen from among aluminium nitride (AlN), silicon nitride (SiN), aluminium oxide (Al_2O_3), and silicon oxide (SiO_2). The gate-dielectric layer 8a has a thickness chosen between 1 and 50 nm, for example 20 nm.

[0054] Next (Figure 6D), a step of deposition of conductive material on the wafer 30 is carried out to form a conductive layer 58 on the gate dielectric layer 8a, in particular in order to fill the trench 9. For example, the conductive layer 58 is made of metal material, such as tantalum (Ta), tantalum nitride (TaN), titanium nitride (TiN), palladium (Pa), tungsten (W), tungsten silicide (WSi_2), titanium/aluminium (Ti/Al), or nickel/gold (Ni/Au).

[0055] The conductive layer 58 is then selectively removed by lithographic and etching steps in themselves known for eliminating it from the wafer 50 except for the portion thereof that extends in the trench 9, thus forming the gate metallization 8b. During the same step, using an appropriate mask for etching of the conductive layer 58, it is further possible to define, in a per se known manner, the gate field plate 30, described with reference to Figure 3.

[0056] The gate metallization 8b and the gate dielectric 8a form, as a whole, the recessed-gate region 8 of the HEMT device of Figure 1.

[0057] Then (Figure 6E), one or more further steps of masked etching of the gate dielectric 8a, of the passivation layer 52, of the auxiliary channel layer 56, and of the barrier layer 6 are carried out to remove selective portions thereof that extend in regions of the wafer 50 where the source and gate regions 10, 12 of the HEMT device 1 are to be formed.

[0058] Removal of the selective portions of the passivation layer 52 leads to formation of the insulation layer 7 illustrated in Figure 1. Likewise, removal of selective portions of the auxiliary channel layer 56 leads to formation of the auxiliary channel 20 illustrated in Figure 1.

[0059] In particular, openings are formed on opposite sides (sides 8' and 8") of the gate region 8, and at a distance from the gate region 8, until the channel layer 4 is reached.

[0060] Next, a step of formation of ohmic contacts is carried out to provide the source and drain regions 10, 12, by depositing conductive material, in particular metal such as titanium (Ti) or aluminium (Al), or alloys or compounds thereof, by sputtering or evaporation, on the wafer 50. A next step of etching of the metal layer thus deposited is then carried out to remove said metal layer from the wafer 50 except for the metal portions that extend within source and drain openings to form therein the source region 10 and the drain region 12, respectively.

[0061] Next, a step of rapid thermal annealing (RTA), for example at a temperature comprised between approximately 500 and 900°C for a time of from 20 s to 5 min, enables formation of electrode ohmic contacts of

the source region 10 and drain region 12 with the underlying channel layer (having the two-dimensional gas 2DEG).

[0062] The HEMT device 1 shown in Figure 1 is thus formed.

[0063] Figure 7 represents the plot (obtained by simulation) of the drain current (which is indicative of the ON-state resistance R_{ON}) as a function of the drain stresses, for two biasing values provided by way of example (400 V and 600 V), and in both the case where the auxiliary channel is present according to the present disclosure and in the case where the auxiliary channel is absent according to the prior art. In particular, with reference to Figure 7:

- the curve C_1 shows the plot of the drain voltage as a function of the drain current in pre-stress conditions in an HEMT device provided with the auxiliary channel 20, according to the present disclosure;
- the curve C_2 shows the plot of the drain voltage as a function of the drain current in pre-stress conditions in an HEMT device according to the known art, without of the auxiliary channel 20;
- the curve C_3 represents the plot of the drain voltage as a function of the drain current in post-stress conditions (400 V) in an HEMT device provided with the auxiliary channel 20, according to the present disclosure;
- the curve C_4 represents the plot of the drain voltage as a function of the drain current in post-stress conditions (400 V) in an HEMT device according to the known art, without the auxiliary channel 20;
- the curve C_5 represents the plot of the drain voltage as a function of the drain current in post-stress conditions (600 V) in an HEMT device provided with the auxiliary channel 20, according to the present disclosure; and
- the curve C_6 represents the plot of the drain voltage as a function of the drain current in post-stress conditions (600 V) in an HEMT device according to the known art, without the auxiliary channel 20.

[0064] As may be noted, the presence of the auxiliary channel 20 (curves C_1, C_3, C_5) determines a marked increase in the drain current as compared to an embodiment that does not envisage it (curves C_2, C_4, C_6), in operating conditions comparable to one another.

[0065] Consequently, according to the present disclosure, the operating and functional characteristics of the HEMT device 1 are improved as compared to what is available according to the prior art.

[0066] An HEMT device provided according to the present invention shows high values of current irrespective of the operating conditions, and irrespective of the traps present in the channel layer (which does not require any specific optimization for reduction of the traps). The performance of the device is markedly improved.

[0067] Finally, it is clear that modifications and variations may be made to what is described and illustrated herein, without thereby departing from the scope of the present invention, as defined in the annexed claims.

[0068] For example, according to further embodiments (not shown), the semiconductor body 5 may comprise, if need be, just one or else more than one layers of GaN, or GaN alloys, appropriately doped or of an intrinsic type.

[0069] Further, according to one embodiment, the source region 10 and the drain region 12 extend in depth in the semiconductor body 5, completely through the barrier layer 6 and partially through the channel layer 4, and terminate within the channel layer 4.
Alternatively, the metallizations of the source and drain contacts may further be provided only partially recessed within the barrier layer 6, or else facing the front side 6a of the barrier layer 6.

[0070] The metallizations of the source, drain, and gate contacts may be made using any material designed for the purpose, such as, for example, formation of contacts of AlSiCu/Ti, Al/Ti, or W-plug, etc.

[0071] Further, according to one embodiment, the gate region 8 does not extend completely through the barrier layer 6, but terminates at the front side 6a of the barrier layer; in this case, the HEMT device is of a normally-on type.

Claims

1. An HEMT device (1), comprising:

a semiconductor body (15) including a heterojunction structure (13) that forms a main conductive channel (4) of the HEMT device (1);
a dielectric layer (7) on the semiconductor body;
a gate electrode (8), a drain electrode (12), and a source electrode (10) aligned to one another in a direction (X), wherein the drain electrode (12) extends facing a first side (8') of the gate electrode (8), and the source electrode extends facing a second side (8"), opposite to the first side in said direction (X), of the gate electrode,

characterized by further comprising an auxiliary channel layer (20), which extends over the heterojunction structure (13) between the gate electrode (8) and the drain electrode (12), in electrical contact with the drain electrode (12) and at a distance from the gate electrode (8), and forms a conductive path additional to the main conductive channel (4) for charge carriers that flow between the source electrode and the drain electrode.

2. The HEMT device according to claim 1, wherein the auxiliary channel layer (20) extends at a distance from first side (8') of the gate electrode (8) that is equal to, or greater than, 0.5 μm along said direction (X).

3. The HEMT device according to claim 1 or claim 2, wherein the auxiliary channel layer (2) is of gallium nitride with N-type doping.

4. The HEMT device according to claim 1 or claim 2, wherein the auxiliary channel layer (20) includes a layer of gallium and aluminium nitride, having a concentration of aluminium comprised between 10% and 40%, which extends over a layer of gallium nitride having a concentration of aluminium comprised between 5% and 30%.

5. The HEMT device according to any one of the preceding claims, wherein the heterojunction structure (13) comprises: a channel layer (4), of a first material, and a barrier layer (6), of a second material, extending over the channel layer (4), the first and second materials having different band gap,
and wherein the barrier layer (6) includes: a first intermediate layer (6') including gallium and aluminium nitride having a concentration of aluminium comprised between 10% and 40%, and a second intermediate layer (6"), which extends over the first intermediate layer (6'), including gallium and aluminium nitride having a concentration of aluminium comprised between 5% and 30%.

6. The HEMT device according to any one of the preceding claims, further comprising a field plate (30) which extends over the dielectric layer (7) and overlaps, at least in part, the auxiliary channel layer (20).

7. The HEMT device according to any one of claims 1-5, further comprising a field plate (30), which extends over the dielectric layer (7), wherein the field plate extends further at a distance, along said direction (X), from the auxiliary channel layer (20).

8. The HEMT device according to claim 7, wherein said distance is equal to, or less than, 0.5 μm.

9. The HEMT device according to any one of claims 6-8, wherein said field plate is either a gate field plate, electrically coupled to the gate electrode (8), or a source field plate, electrically coupled to the source electrode (10).

10. A method of manufacturing of an HEMT device (1), comprising the steps of:

forming a heterojunction structure (13) in a semiconductor body (15) thus defining a main conductive channel (4) of the HEMT device (1);
forming a dielectric layer (7) on the semiconductor body;
forming a gate electrode (8), including forming a conductive gate region (8b) and a gate dielectric (8a) that insulates electrically the conductive gate region (8b) from the semiconductor body;
forming a drain electrode (12) and a source electrode (10) aligned to one another and to the gate electrode in a direction (X), wherein the drain electrode is formed facing a first side (8') of the gate electrode, and the source electrode is formed facing a second side (8"), opposite to first side in said direction (X), of the gate electrode,

characterized in that it further comprises the step of forming an auxiliary channel layer (20) on the heterojunction structure (13) between the gate electrode (8) and the drain electrode (12), in electrical contact with the drain electrode (12) and at a distance from the gate electrode (8), thus forming a conductive path, additional to the main conductive channel (4), for charge carriers that flow between the source electrode and the drain electrode.

11. The method according to claim 10, wherein the step of forming the auxiliary channel layer (20) comprises forming the auxiliary channel layer (20) at a distance the from first side (8') of the gate electrode (8) equal to, or greater than, 0.5 μm along said direction (X).

12. The method according to claim 10 or claim 11, wherein forming the auxiliary channel layer (20) comprises depositing a layer of gallium nitride with N-type doping.

13. The method according to claim 10 or claim 11, wherein forming the auxiliary channel layer (20) comprises depositing a layer of gallium nitride having a concentration of aluminium comprised between 20% and 30% and, then, depositing a layer of gallium and aluminium nitride, having a concentration of aluminium comprised between 10% and 20%.

14. The method according to any one of claims 10-13, wherein forming the heterojunction structure (13) comprises:

depositing a channel layer (4), of a first material, and depositing a barrier layer (6), of a second material, on the channel layer (4), the first and second materials having different band gaps,
and wherein forming the barrier layer (6) includes: depositing a first intermediate layer (6') of gallium and aluminium nitride having a concentration of aluminium comprised between 20% and 30%, and depositing a second intermediate layer (6"), on the first intermediate layer (6'), of gallium and aluminium nitride having a concentration of aluminium comprised between 10% and 20%.

15. The method according to any one of the preceding

claims, further comprising forming a field plate (30) on the dielectric layer (7) and overlapping, at least in part, to the auxiliary channel layer (20).

16. The method according to any one of claims 10-14, further comprising forming a field plate (30) on the dielectric layer (7), at a distance, along said direction (X), from the auxiliary channel layer (20).

17. The method according to claim 16, wherein said distance is equal to, or less than, 0.5 μm.

18. The method according to any one of claims 15-17, wherein forming said field plate includes either of the following steps: forming a gate field plate electrically coupled to the gate electrode (8); or forming a source field plate electrically coupled to the source electrode (10).

5 10 15 20 25 30 35 40 45 50 55

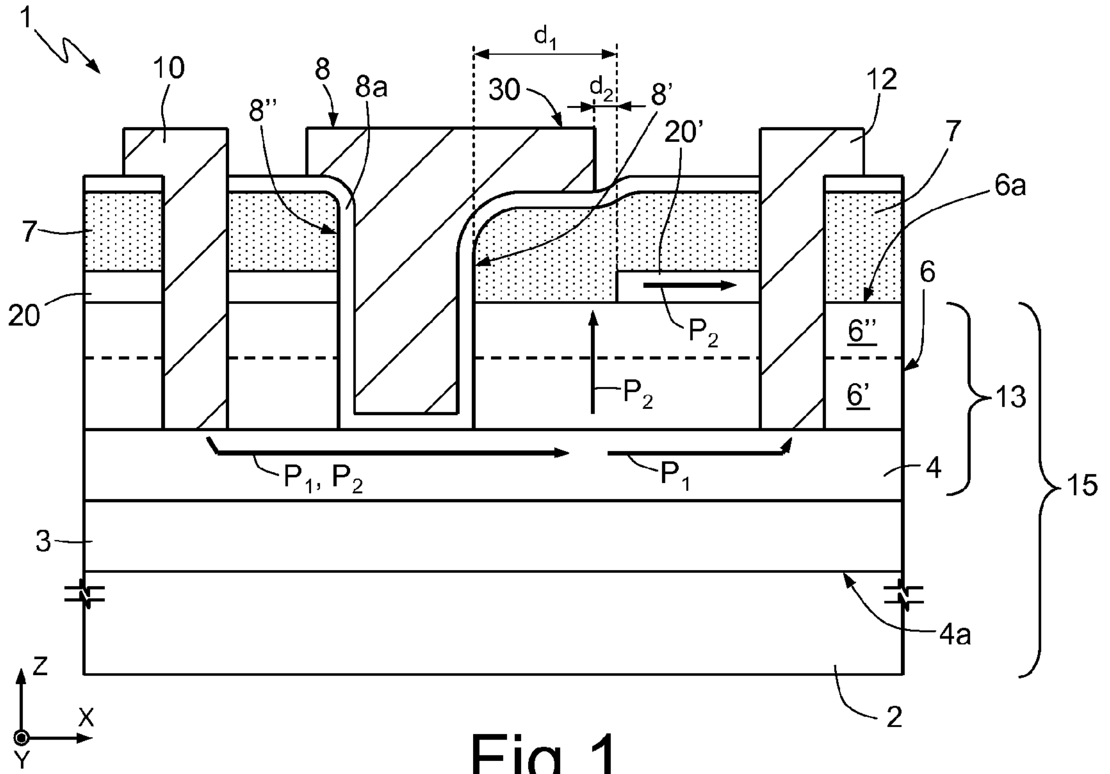

Fig.1

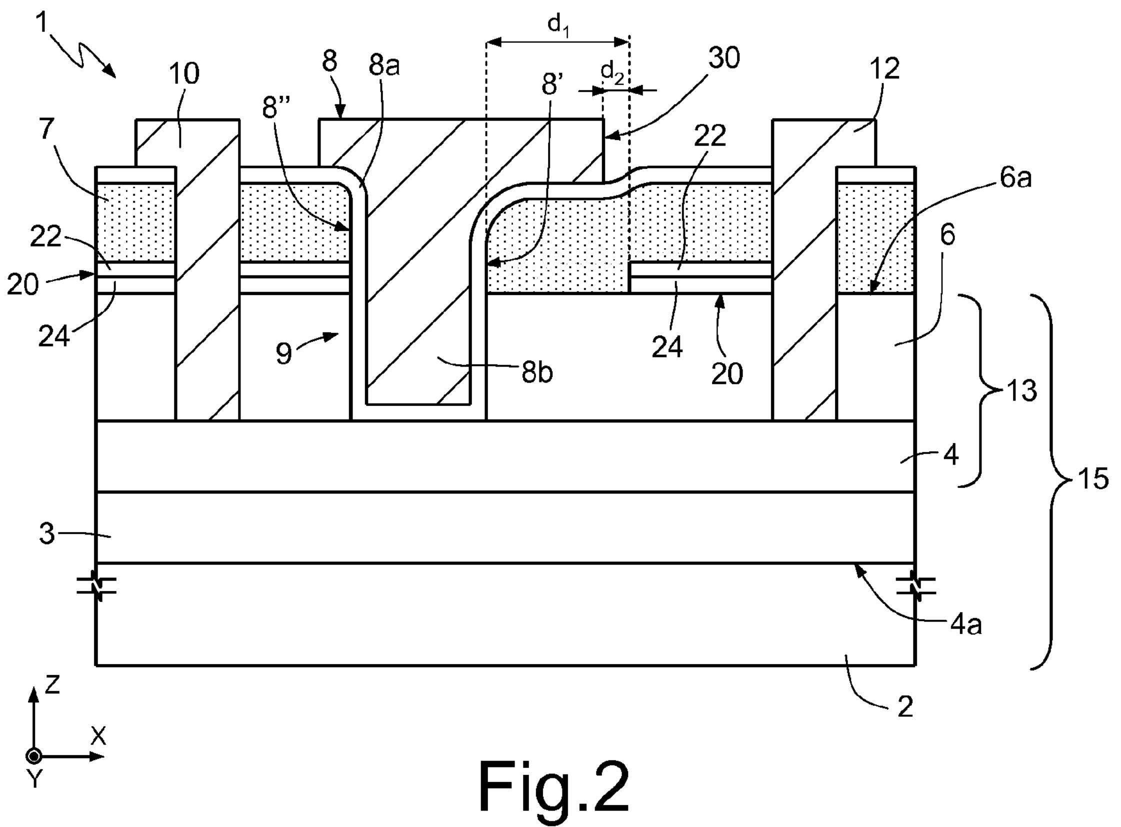

Fig.2

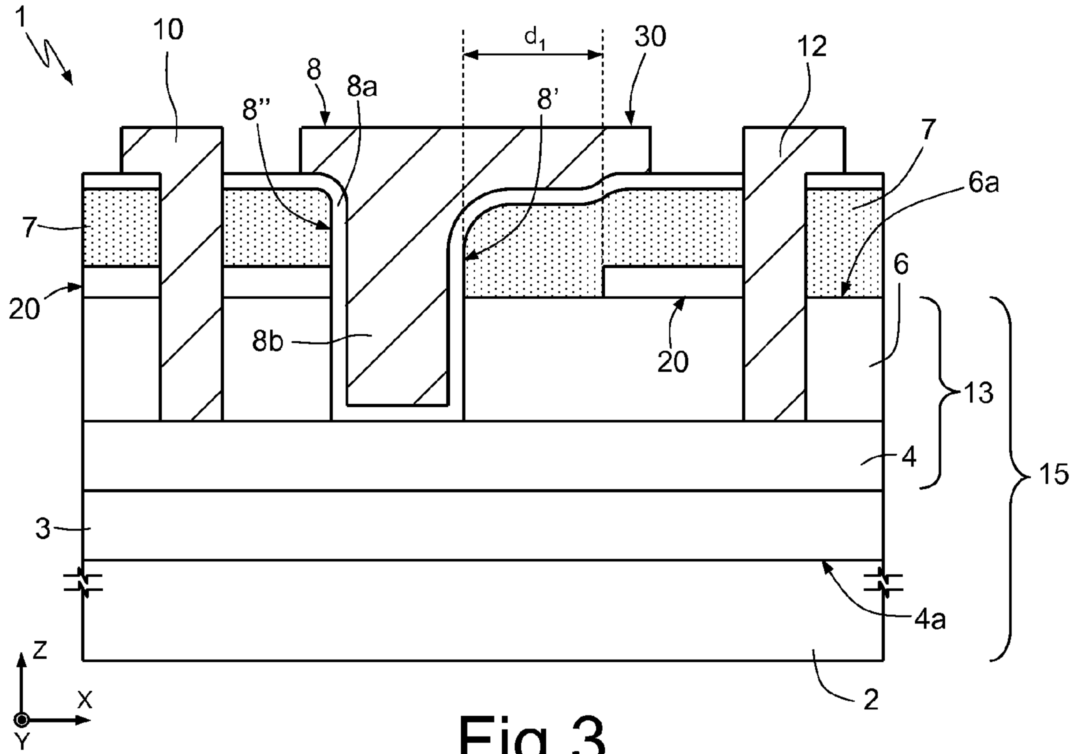

Fig.3

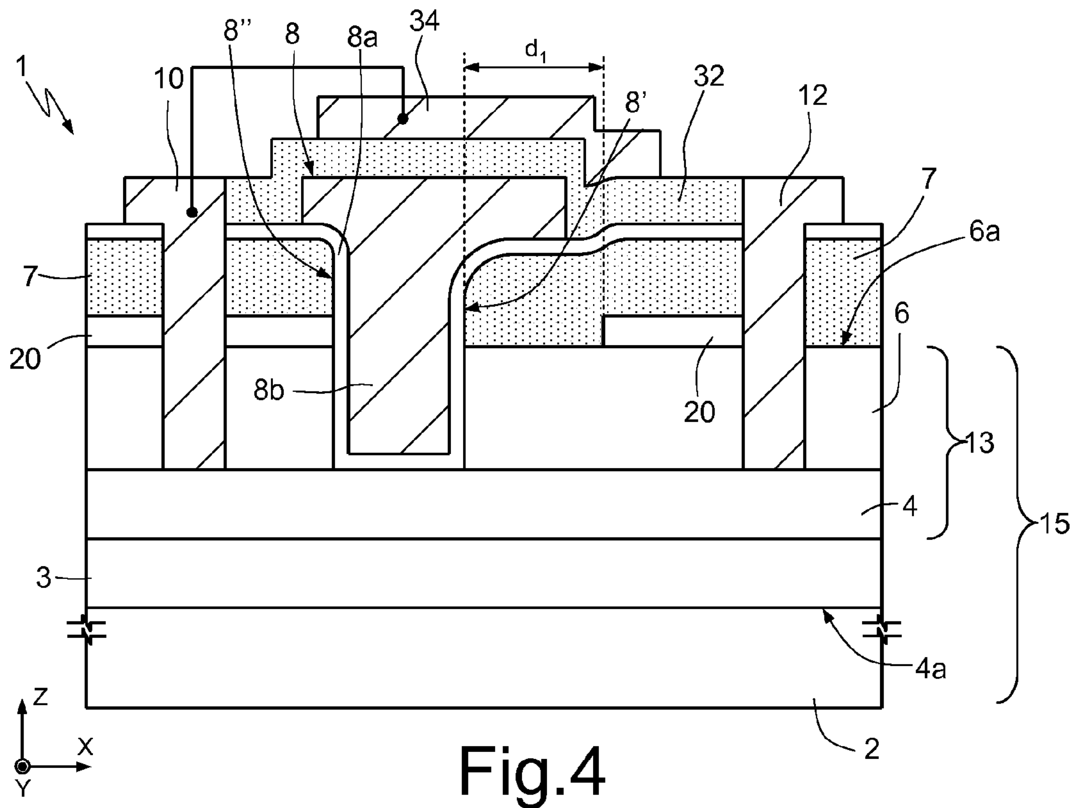

Fig.4

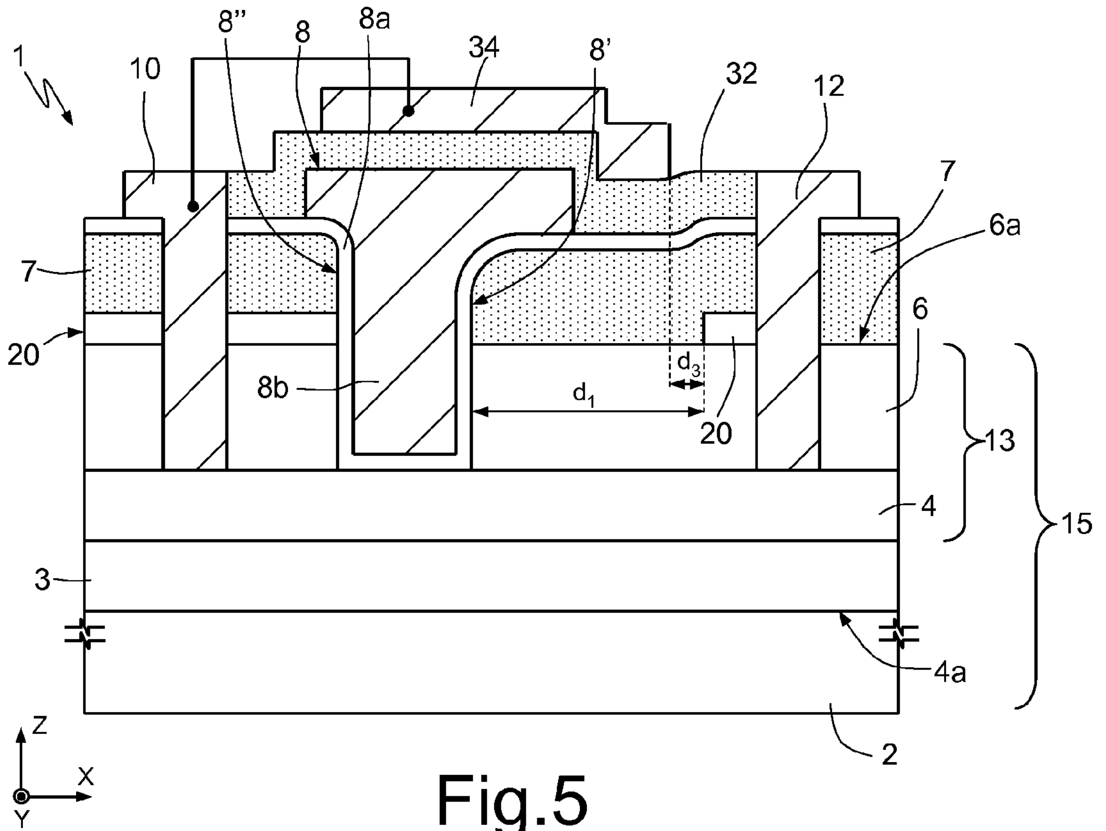

Fig.5

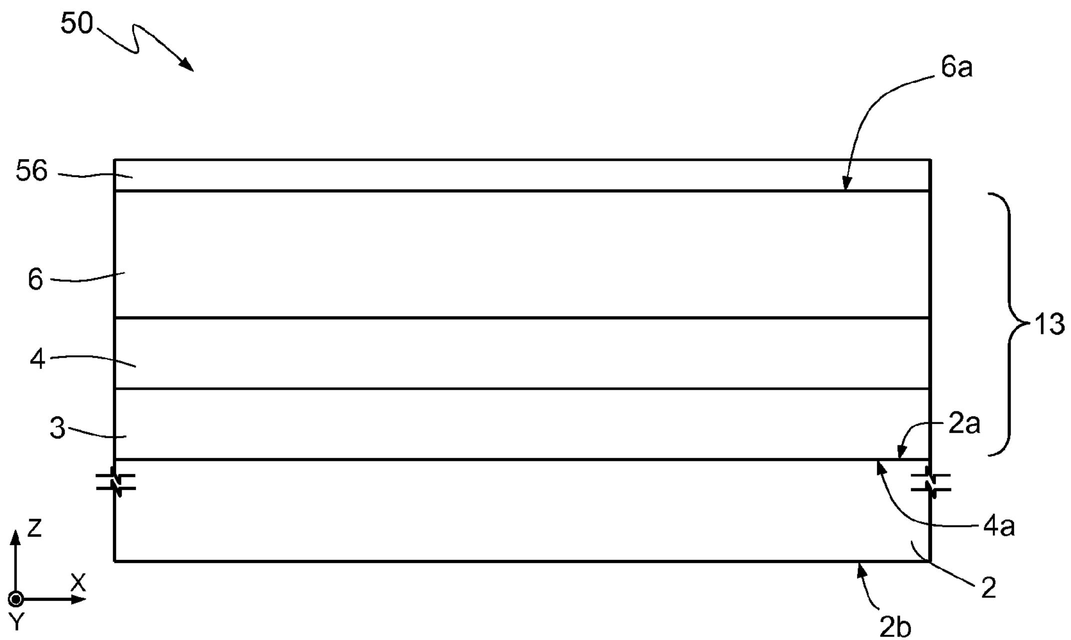

Fig.6A

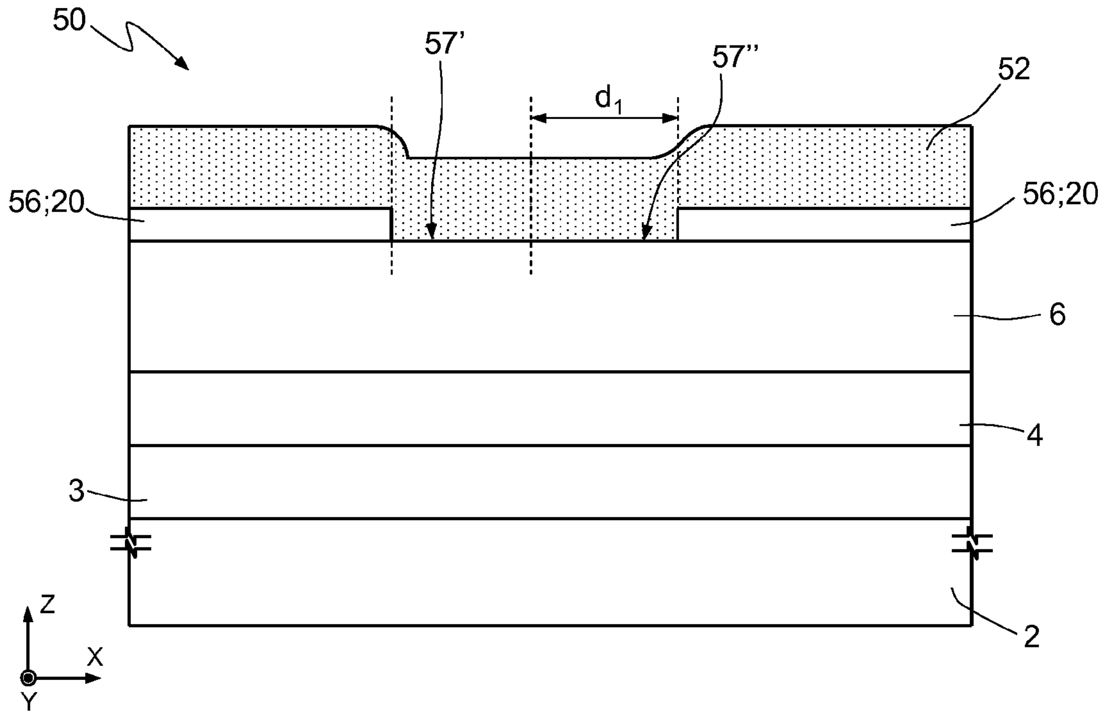

Fig.6B

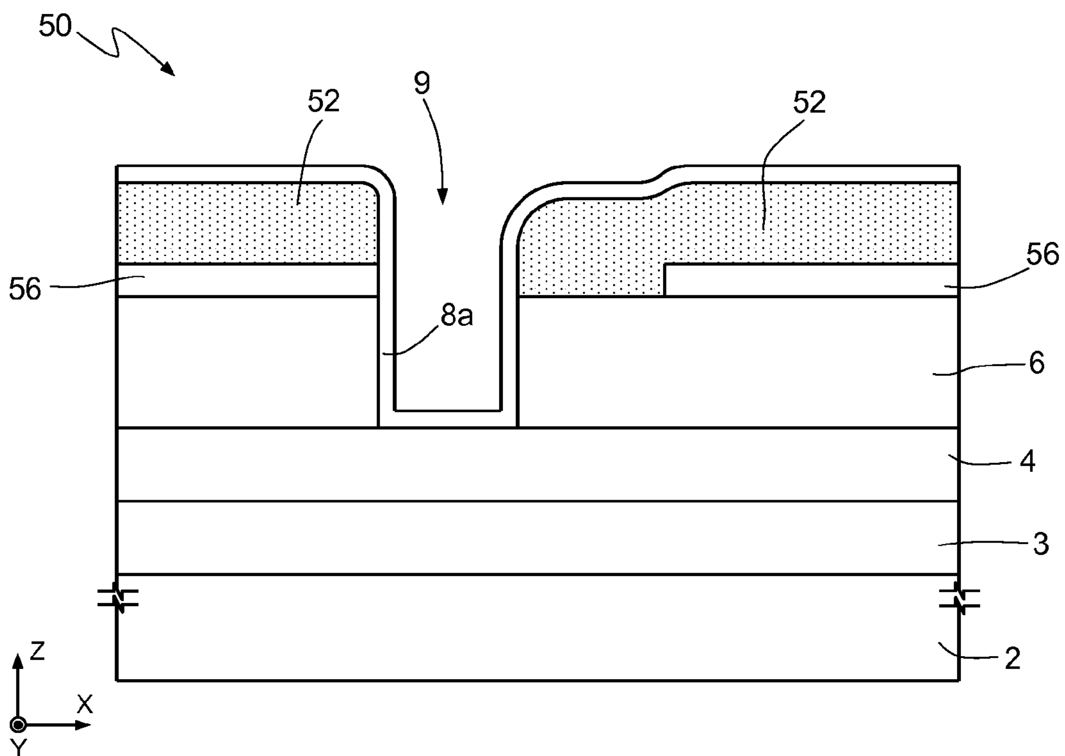

Fig.6C

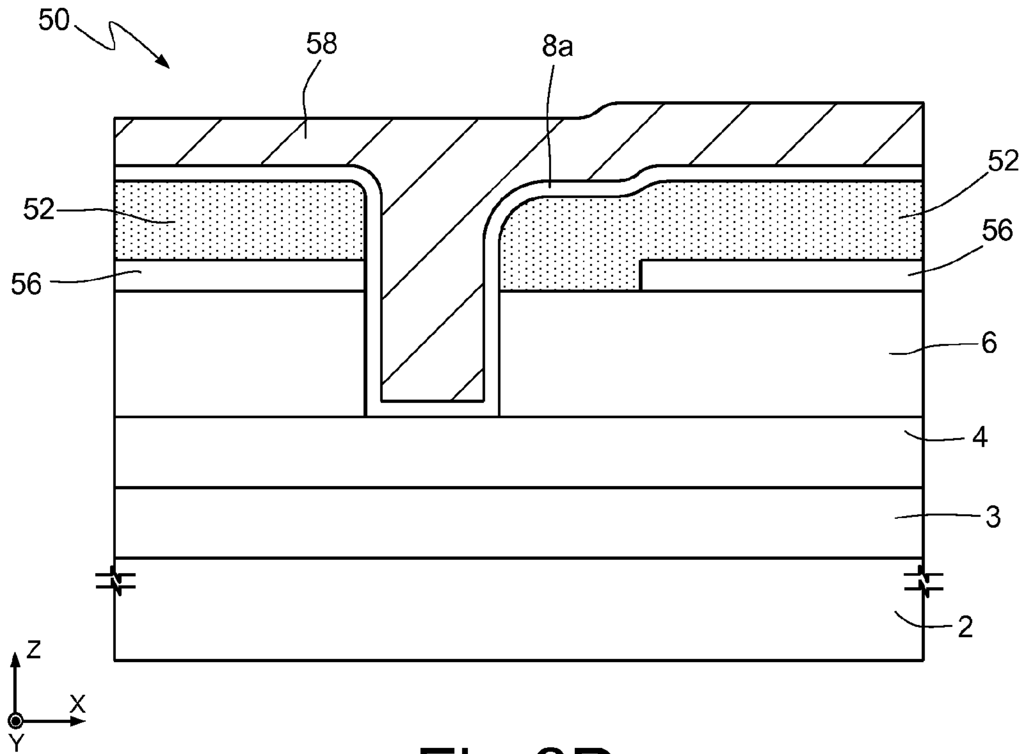

Fig.6D

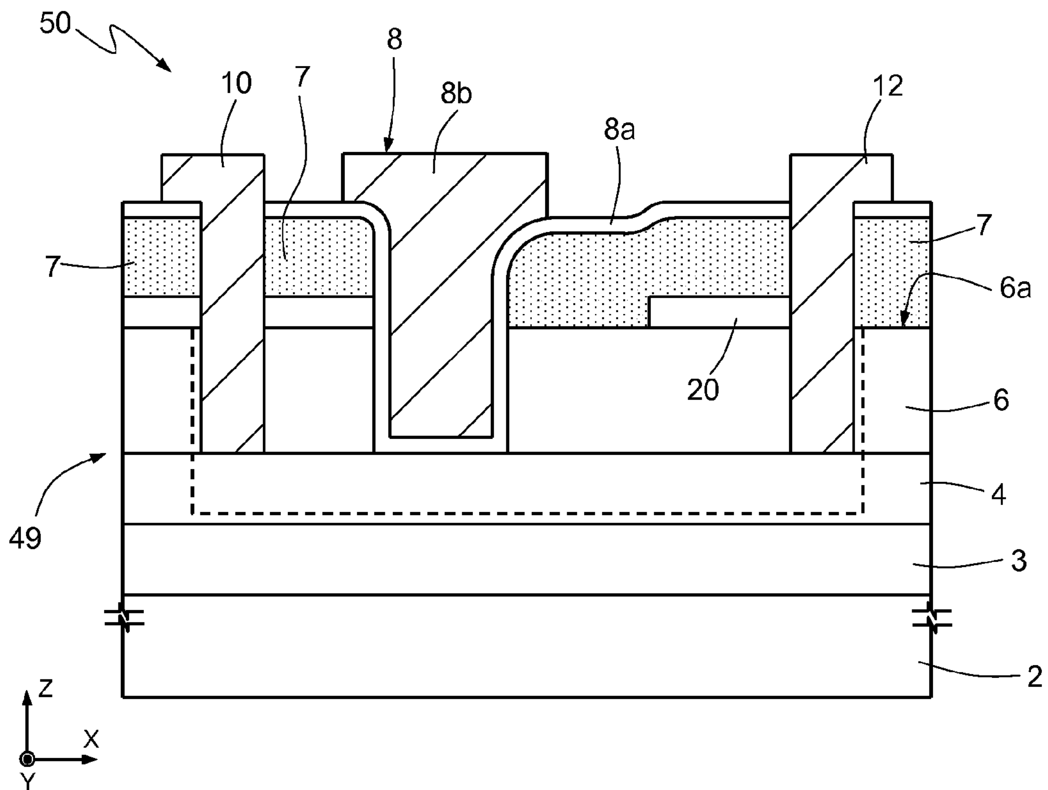

Fig.6E

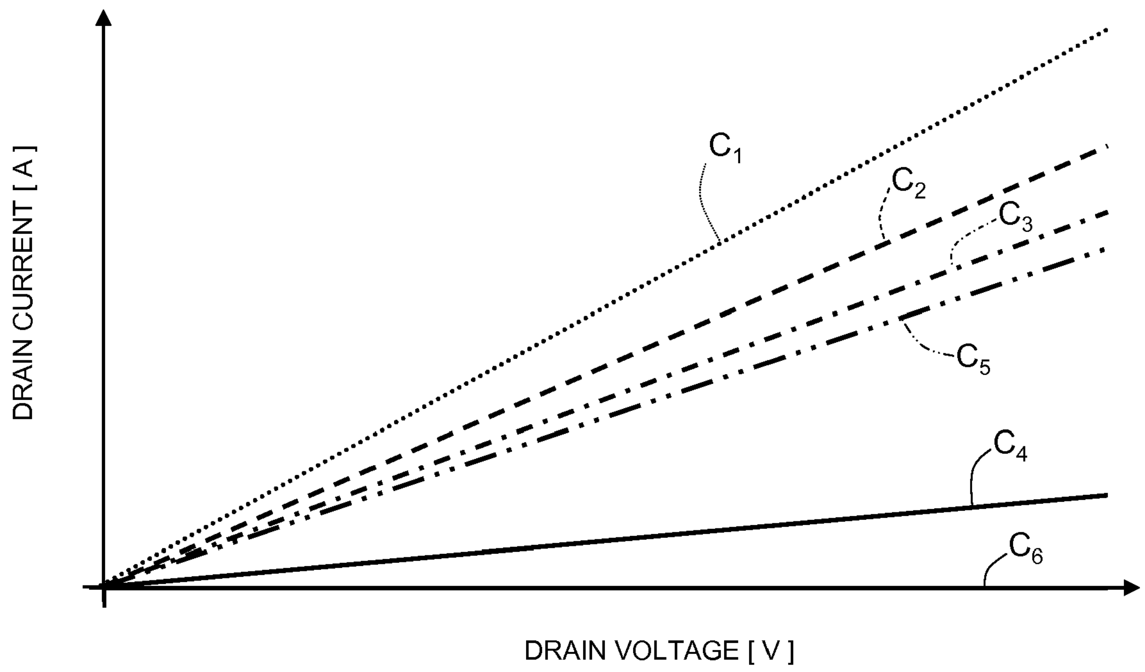

Fig.7

EUROPEAN SEARCH REPORT

Application Number
EP 16 42 5047

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H01L

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The present search report has been drawn up for all claims

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Place of search	Date of completion of the search	Examiner
Munich	7 December 2016	Norga, Gerd

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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