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(54) HIGH ELECTRON MOBILITY TRANSISTOR AND MANUFACTURING METHOD THEREOF

(57) HEMT (1; 21; 31; 51) including a buffer layer (4), a hole-supply layer (6) on the buffer layer (4), a heterostructure (7) on the hole-supply layer (6), and a source electrode (16). The hole-supply layer (6) is made of P-type doped semiconductor material, the buffer layer (4) is doped with carbon, and the source electrode (16) is in direct electrical contact with the hole-supply layer (6), such that the hole-supply layer (6) can be biased to facilitate the transport of holes from the hole-supply layer (6) to the buffer layer (4).

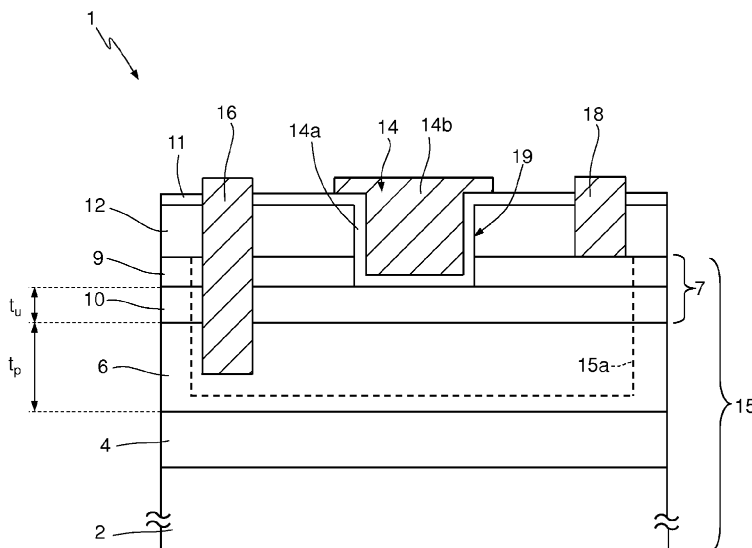

Fig.1

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Description

PRIORITY CLAIM

[0001] This application claims priority from Italian Patent Application No. 102017000064155 filed on 09/06/2017.

[0002] The present invention relates to a high-electron-mobility field-effect transistor (HEMT) and a method for manufacturing the HEMT transistor. In particular, the present invention relates to an HEMT transistor with high stress resilience during OFF-state.

[0003] High electron-mobility field-effect transistors (HEMT) based on the formation of layers of high-mobility two-dimensional electron gas (2DEG) at a heterojunction, i.e. the interface between semiconductor materials with different band gaps, are known. For example, HEMT transistors based on a heterojunction between a layer of aluminium nitride and gallium (AlGaN) and a layer of gallium nitride (GaN) are known.

[0004] HEMT transistors based on AlGaN/GaN heterojunctions offer various advantages that make same particularly suitable and widely used in a range of different applications. For example, the high breakdown threshold of the HEMT transistors is used by high-performance power switches; the high mobility of the electrons in the conductive channel makes it possible to build high-frequency amplifiers. Furthermore, the high concentration of electrons in the 2DEG makes it possible to achieve low ON-state resistance (R_{ON}).

[0005] Due to the high cost of gallium nitride substrates, HEMT transistors based on AlGaN/GaN heterojunctions are usually made by growing GaN and AlGaN layers on silicon substrates. Consequently, HEMT transistors built in this manner are planar, i.e. having source, gate and drain electrodes that are aligned on a plane parallel to the substrate.

[0006] When used in power applications, the potential drop V_{DS_OFF} between the source electrode and the drain electrode in OFF-state conditions of the HEMT transistors may reach several hundreds of volts, depending on the power supply voltage. Consequently, a malfunction mechanism in the HEMT transistors is caused by the formation of high electrical fields, and consequent breakdown, in the region between the gate electrode and the drain electrode in OFF-state conditions. As a result, the breakdown threshold of the HEMT transistor is an important figure of merit of the HEMT transistor.

[0007] Another important figure of merit of the HEMT transistor is the ON-state resistance R_{ON}, which should be minimized to save power.

[0008] Furthermore, a known problem in known HEMT transistors relates to an increase in the ON-state resistance R_{ON} as a result of the stress caused by the high voltage V_{DS_OFF} in OFF-state. Said reversible increase in R_{ON} can be attributed to a range of factors, including emission/capture phenomena inside trap states in a buffer layer of the HEMT transistor. In known HEMT transistors, the buffer layer emits holes as a function of the quantity of trap states, going on to form a layer of negative charges inside same. This layer of negative charges causes a partial emptying of the 2DEG, which thus increases the ON-state resistance R_{ON}.

[0009] A range of different solutions for individually optimizing the aforementioned figures of merit of HEMT transistors are known. However, optimizing one figure of merit normally has a negative impact on one or more other figures of merit.

[0010] For example, the breakdown threshold of the HEMT transistor can be increased by increasing the distance between the gate electrode and the drain electrode of the HEMT transistor, thereby reducing the electrical field for the same power supply voltage. However, this solution also causes an unwanted increase in the ON-state resistance R_{ON}.

[0011] Another known solution is disclosed in Tanaka, K. et al., "Suppression of current collapse by hole injection from drain in a normally-off GaN-based hybrid-drain-embedded gate injection transistor", Appl. Phys. Lett., 107, 163502 (2015). Said document relates to an HEMT transistor in which a layer of P-type doped gallium nitride (p-GaN) is formed by growth on a barrier layer of aluminium nitride and gallium, and connected to a drain electrode. This transistor has increased R_{ON} as a result of the substantially negligible stress in OFF-state (V_{DS_OFF} = 800 V) . Nonetheless, an increase in R_{ON} is observed in static conditions, regardless of stress.

[0012] It is therefore particularly important to provide a method to prevent R_{ON} from increasing as a result of the stress in OFF-state in HEMT transistors that does not have a negative effect on the breakdown threshold.

[0013] The purpose of the present invention is to provide an HEMT transistor and a related manufacturing method that address the drawbacks in the prior art.

[0014] The present invention provides for an HEMT transistor and a method for manufacturing the HEMT transistor, as defined in the attached claims.

[0015] The present invention is further described below with reference to preferred embodiments of same, which are provided purely as non-limiting examples, and to the attached drawings, in which:

- Figure 1 is a lateral cross section of an HEMT transistor according to one embodiment of the present invention,
- Figure 2 is a lateral cross section of an HEMT transistor according to another embodiment of the present invention,
- Figure 3 is a lateral cross section of an HEMT transistor according to another embodiment of the present invention,
- Figures 4A to 4H show manufacturing steps of the HEMT transistor in Figure 1, and

- Figure 5 is a lateral cross section of an HEMT transistor according to another embodiment of the present invention.

[0016] Figure 1 shows, in a system of three axes X, Y, Z that are orthogonal to one another, a side view in the plane XZ of an HEMT device 1 based on an AlGaN/GaN heterojunction.

[0017] The HEMT device 1 includes a substrate 2, a buffer layer 4 arranged on the substrate 2, a hole-supply layer 6 arranged on the buffer layer 4, and a heterojunction or heterostructure 7 arranged on the hole-supply layer 6. Optionally, one or more additional buffer layers (or interface layers) (not shown) made from compounds of the group III-V of the periodic table, including gallium, are arranged between the substrate 2 and the buffer layer 4. The one or more interface layers are designed to maintain the drain voltage when the device is powered off and to reduce the density of threading dislocations, and therefore of trap states.

[0018] The substrate 2 is for example made of silicon or silicon carbide (SiC) or sapphire (Al_2O_3), or GaN. The buffer layer 4 is made of intrinsic or N-type doped gallium nitride, and has a high concentration of carbon impurities, for example a concentration of between 10^{16} and 10^{19} cm^{-3}, in order to attenuate the vertical leakage towards the substrate 2.

[0019] The hole-supply layer 6 is made of P-type doped gallium nitride, for example using magnesium (Mg) with a concentration of between 10^{17} and 3.10^{19} cm^{-3}.

[0020] The heterostructure 7 in particular includes a channel layer 10 arranged on top of the buried layer 6, and a barrier layer 9 arranged on top of the channel layer 10. The channel layer 10 is made of intrinsic gallium nitride (GaN). The barrier layer 9 is made of aluminium nitride and gallium (AlGaN) with a thickness of between 10 nm and 30 nm. The channel layer 10 and the barrier layer 9 are generally made of materials that, when coupled together as shown in Figure 1, form a heterojunction that enables the formation of a two-dimensional gas layer (2DEG).

[0021] The HEMT device 1 also includes an insulating layer 12 arranged on the heterostructure 7. The insulating layer 12 is made of dielectric material, for example silicon nitride (Si3N4) or silicon dioxide (SiO2) and has a thickness of between 5 nm and 100 nm.

[0022] Hereinafter, the substrate 2, the buffer layer 4, the hole-supply layer 6 and the heterostructure 7 are referred to as a whole using the term semiconductor body 15. The semiconductor body 15 contains an active region 15a that is the active portion of the HEMT device 1.

[0023] The HEMT device 1 also includes a gate region 14 arranged between source region 16 and drain region 18. The active region 15a is arranged laterally (i.e. along the axis X) between the source region 16 and the drain region 18. The active region 15a extends depthwise (i.e. along the axis Z) into the layers of the semiconductor body 15 in which the gate region 14, the source region 16 and the drain region 18 are arranged.

[0024] The gate region 14 is separated laterally from the source region 16 and the drain region 18 by respective portions of the insulating layer 12. The gate region 14 extends depthwise through the insulating layer 12 and into the heterostructure 7, ending at the interface between the barrier layer 9 and the channel layer 10.

[0025] The gate region 14 is formed in a trench 19 hollowed out of part of the semiconductor body 15, the depth of which is the same as the depth of the gate region 14. A dielectric layer 11 made of insulating material, such as silicon dioxide, is arranged on the insulating layer 12 and inside the trench 19, partially filling the trench 19 and forming a gate dielectric layer 14a inside the trench 19. In particular, the gate dielectric layer 14a is arranged on the bottom and on the inner side walls of the trench 19. A gate metallization 14b is arranged in the trench 19 on the gate dielectric layer 14a, completely filling the trench 19. The gate dielectric layer 14a and the gate metallization 14b form the gate region 14 of the HEMT device 1.

[0026] The source region 16, which is made of conductive material such as titanium (Ti) or aluminium (Al), extends across the insulating layer 12 and the heterostructure 7, ending inside the hole-supply layer 6.

[0027] The drain region 18, which is made of conductive material such as titanium (Ti) or aluminium (Al), extends across the insulating layer 12, ending at the interface between the insulating layer 12 and the barrier layer 9. According to another embodiment not shown in the figures, the drain region 18 may be recessed, i.e. penetrate a portion of the semiconductor body 15 beneath the interface between the insulating layer 12 and the barrier layer 9.

[0028] The HEMT device 1 is a normally-off device, hence the need to bias the gate region 14 with a voltage V_G greater than a threshold voltage V_{th} to generate a conductive channel between the source region 16 and the drain region 18. When in use, the value of the current I_{DS} between the source region 16 and the drain region 18 depends on the concentration of electrons in the 2DEG at the interface between the barrier layer 9 and the channel layer 10. The buffer layer 4 has trap states, for example due to the high concentration of impurities therein. The buffer layer 4 emits holes as a function of the quantity of trap states, going on to form a layer of negative charges inside same. This layer of negative charges causes a reduction in the concentration of electrons in the 2DEG. Furthermore, when the HEMT transistor is in OFF-state, there is a high voltage V_{DS_OFF} between the source region 16 and the drain region 18. The stress caused by the voltage V_{DS_OFF} in OFF-state generates further trap states inside the buffer layer 4. The hole-supply layer 6 has a high concentration of P-type impurities, and is therefore a source of holes to replace the holes emitted by the buffer layer 4 and to neutralize the layer of negative charges inside same. According to one aspect of the present invention, the source region 16 extends up to the hole-supply layer 6, biasing same such as to facilitate the transport of holes from

the hole-supply layer 6 to the buffer layer 4. Consequently, following the stress caused by the voltage V_{DS_OFF} in OFF-state, the HEMT transistor 1 is not subject to an increase in ON-state resistance R_{ON}.

[0029] The neutralization mechanism for the layer of negative charges inside the buffer layer 4 can be optimized by appropriately selecting a thickness t_p of the hole-supply layer 6, a thickness t_u of the channel layer 10 and a surface concentration N_A of dopant species of the hole-supply layer 6. The applicant has verified that, for a given thickness t_u of the channel layer 10 and a given surface concentration N_A of dopant species of the hole-supply layer 6, the thickness t_p of the hole-supply layer 6 is preferably determined using the following equation:

$$t_{\mathrm{p}} > -t_{\mathrm{u}} + \sqrt{t_{\mathrm{u}}^2 + 2\frac{\varepsilon B}{qN_{\mathrm{A}}}} + \sqrt{\frac{2\varepsilon E_{\mathrm{A}}}{qN_{\mathrm{A}}}} \quad (1)$$

where q is the elementary charge (approximately $1.6 \cdot 10^{-19}$ C); B is the band gap of the material of the buffer layer 4; E_A is the distance in the band diagram between the trap states, for example generated by the presence of carbon atoms, and the valence band of the buffer layer (4); and ε is the dielectric constant of the material of the hole-supply layer 6. In this embodiment, the buffer layer 4 is a carbon-doped layer of gallium nitride, for which B = 3.4 eV, E_A = 0.9 eV, $\varepsilon = 9\varepsilon_0$, where so is the dielectric constant of the void. The value of E_A can be determined using known methods provided in the literature, for example in A. Chini et al., "Experimental and Numerical Analysis of Hole Emission Process From Carbon-Related Traps in GaN Buffer Layers", Trans. Elec. Dev., 63(9), pages 3473-3478, 2016.

[0030] For example, for a concentration $N_A = 10^{17}$ cm^{-2} of active dopant species in the hole-supply layer 6 and a thickness t_u = 100 nm of the channel layer 10, it is preferable to select a thickness t_p of the hole-supply layer 6 that is greater than 204 nm. More generally, the hole-supply layer 6 may have a thickness of between 10 nm and 1 μm and a concentration of active dopant species of between 10^{17} cm^{-2} and 10^{19} cm^{-2}, while the channel layer 10 may have a thickness of between 10 nm and 1 μm.

[0031] Figure 2 shows a normally-on HEMT transistor 21 according to another embodiment of the present invention. Elements of the HEMT transistor 21 in Figure 2 that are common with the HEMT transistor 1 in Figure 1 are identified using the same reference signs and are not further described. With reference to Figure 2, the gate region 14 extends depthwise into the insulating layer 12, ending at the interface between the insulating layer 12 and the barrier layer 9. Consequently, unlike the HEMT transistor 1 in Figure 1, the gate region 14 does not extend into the barrier layer 9.

[0032] The presence of the source region 16, arranged in direct electrical contact with the hole-supply layer 6, makes it possible to obtain the same advantages as described above in relation to the HEMT transistor 1.

[0033] Figure 3 shows a normally-off HEMT transistor 31 according to another embodiment of the present invention. Elements of the HEMT transistor 31 in Figure 3 that are common with the HEMT transistor 1 in Figure 1 are identified using the same reference signs and are not further described. With reference to Figure 3, the gate region 14 extends across the insulating layer 12, the heterostructure 7, the hole-supply layer 6 and part of the buffer layer 4, ending inside the buffer layer 4.

[0034] In this embodiment, the buffer layer 4 of p-GaN is partially interrupted by the trench of the gate region 14. This technical solution allows to obtain a turn-on threshold more positive (important for normally-off devices), guarantying in any case the possibility to have a source of holes required to fill-in the traps negatively charged during turning-off of the device.

[0035] The presence of the source region 16, arranged in direct electrical contact with the hole-supply layer 6, makes it possible to obtain the same advantages as described above in relation to the HEMT transistor 1.

[0036] During use, when the gate region 14 is biased with a voltage V_G greater than a threshold voltage V_{th}, a conductive channel 32 (shown schematically using arrows) is created between the source region 16 and the drain region 18 that extends along the axis Z through the hole-supply layer 6 and along the axis X through the buffer layer 4, beneath the gate region 14. This ensures that the path of the current through the p-GaN hole-supply layer 6 is minimized and the ON-state resistance R_{ON} is further optimized.

[0037] Manufacturing steps of the HEMT device 1 in Figure 1 are described below with reference to Figures 4A to 4H.

[0038] Figure 4A is a cross section of a portion of a wafer 40 during a manufacturing step of the HEMT device 1, according to one embodiment of the present invention. Elements of the wafer 40 that are common with the subject matter described with reference to Figure 1 and shown in Figure 1 are indicated using the same reference signs.

[0039] In particular and as shown in Figure 4A, there is arranged the wafer 40 including the substrate 2, which is for example made of silicon (Si) or silicon carbide (SiC) or aluminium oxide (Al_2O_3), with a front side 2a and a rear side 2b arranged opposite one another in a direction Z, and the buffer layer 4, which is made of intrinsic or N-type doped gallium nitride (GaN), the lower side 4a of which is arranged on the front side 2a of the substrate 2 (additional interface layers not shown in the figure may also be included).

[0040] As shown in Figure 4B, the hole-supply layer 6 made of P-type doped gallium nitride (GaN) is then formed, for

example using epitaxial growth. By way of example, the thickness t_p of the hole-supply layer 6 is between 10 nm and 1 μm, determined on the basis of the equation (1) given above.

[0041] As shown in Figure 4C, the heterostructure 7 is then formed. In a first step, the channel layer 10 made of intrinsic gallium nitride (GaN) is formed, for example using epitaxial growth. The thickness t_u of the channel layer 10 is between 10 nm and 1 μm, determined on the basis of the equation (1) given above. The barrier layer 9 made of aluminium nitride and gallium (AlGaN) is then formed, for example using epitaxial growth. The thickness of the barrier layer 9 is between 10 nm and 30 nm. The exposed upper side of the barrier layer 9 forms a front side 7a of the heterostructure 7.

[0042] As shown in Figure 4D, the insulating layer 12, which is made of an insulating or dielectric material such as silicon nitride (SiN), silicon oxide (SiO_2), nickel oxide (NiO) or another material, is then formed on the front side 7a of the heterostructure 7. The insulating layer 12 has a thickness of between 5 nm and 300 nm, for example 100 nm, and is formed by chemical vapour deposition (CVD) or atomic layer deposition (ALD).

[0043] As shown in Figure 4E, the insulating layer 12 is then selectively removed, for example using lithography and etching steps, such as to remove selected portions of same in the region of the wafer 40 where the gate region 14 is to be formed in successive steps (or in a portion of the active area 15a).

[0044] An etching step is then carried out on the barrier layer 9, using the same lithography mask as the etching step for the insulating layer 12. Etching is terminated once the interface with the channel layer 10 has been reached. This forms a trench 19. Alternatively, in a manner not shown in the figures, the etching step for the barrier layer 9 is not carried out, in order to manufacture the HEMT transistor 21 in Figure 2. Alternatively, in a manner not shown in the figures, the etching step of the barrier layer 9 is followed by an etching step of the channel layer 10, an etching step of the hole-supply layer 6 and an etching step of the buffer layer 4, using the same lithography mask as for the etching step of the insulating layer 12, in order to manufacture the HEMT transistor 31 in Figure 3. In this case, the channel layer 10 and the hole-supply layer 6 are completely removed in the selected portions defined by the lithography mask of the etching step of the insulating layer 12, the etching of the buffer layer 4 terminating inside same, before reaching the interface with the substrate 2.

[0045] As shown in Figure 4F, a deposition or growth step of the gate dielectric layer 14a, for example made of a material selected from aluminium nitride (AlN), silicon nitride (SiN), aluminium oxide (Al_2O_3) and silicon oxide (SiO_2), is then carried out. The thickness of the gate dielectric layer 14a is selected to be between 5 nm and 50 nm.

[0046] As shown in Figure 4G, one or more further mask etching steps are then carried out on the dielectric layer 14a, the insulating layer 12 and the semiconductor body 15 to remove selected portions thereof arranged in regions of the wafer 40 where the source region 16 and the drain region 18 of the HEMT device 1 are to be formed. In particular, a first aperture 60a and a second aperture 60b are formed on opposite sides, along X, of the gate region 14, and away from the gate region 14. The first aperture 60a extends depthwise through the insulating layer 12 and the heterostructure 7, ending inside the hole-supply layer 6. The second aperture 60b extends depthwise through the insulating layer 12, ending at the interface between the insulating layer 12 and the barrier layer 9. Alternatively, in a manner not shown in the figures, the second aperture 60b may penetrate a portion of the semiconductor body 15 beneath the interface between the insulating layer 12 and the barrier layer 9.

[0047] As shown in Figure 4H, an ohmic-contact formation step is then carried out to form the source region 16 and the drain region 18, depositing conductive material, in particular metal such as titanium (Ti) or aluminium (Al), or alloys or compounds thereof, using sputter or evaporator and a photolithographic mask for lift-off, inside the apertures 60a, 60b. The conductive material completely fills the apertures 60a, 60b, forming the source region 16 and the drain region 18 respectively. After deposition, a rapid thermal annealing (RTA) step is carried out, for example at a temperature of between approximately 500°C and 800°C for a time of between 30 seconds and 2 minutes.

[0048] A deposition step of conductive material on the wafer 40 is then carried out to form the gate metallization 14b on the gate dielectric layer 14a, in particular completely filling the trench 19. For example, the gate metallization 14b is made of a metal material such as tantalum (Ta), tantalum nitride (TaN), titanium nitride (TiN), palladium (Pa), tungsten (W), tungsten silicide (WSi_2), titanium aluminium (Ti/Al), nickel gold (Ni/Au). The gate metallization 14b is deposited selectively in the trench 19 and at a distance between the source region 16 and the drain region 18 using lithography steps which are known per se. The gate metallization 14b and the gate dielectric layer 14a together form the recessed gate region 14 of the HEMT device 1 in Figure 1.

[0049] The HEMT device 1 shown in Figure 1 is thus formed.

[0050] Figure 5 shows a normally-off HEMT transistor 51 according to another embodiment of the present invention. Elements of the HEMT transistor 51 in Figure 5 that are common with the HEMT transistor 1 in Figure 1 are identified using the same reference signs and are not further described.

[0051] With reference to Figure 5, the HEMT transistor 51 includes a gate region 54 arranged on the insulating layer 12 between the source region 16 and a drain region 58, and is separated from said regions. The drain region 58, which is made of conductive material such as titanium (Ti) or aluminium (Al), extends across the insulating layer 12 and the barrier layer 9, ending at the interface between the barrier layer 9 and the channel layer 10.

[0052] The HEMT transistor 51 also includes a buried region 56 of P-type doped gallium nitride extending in the gate

region 54, depthwise through the insulating layer 12, ending at the interface between the insulating layer 12 and the barrier layer 9. The structure formed by the gate region 54 and by the buried region 56 is known in the prior art as a "p-GaN gate" and an HEMT transistor containing such a structure is known as a "p-GaN gate transistor".

[0053] The presence of the source region 16, arranged in direct electrical contact with the hole-supply layer 6, makes it possible to obtain the same advantages as described above in relation to the HEMT transistor 1.

[0054] The advantages of the invention according to the present disclosure are clear from the foregoing. In particular, the present invention makes it possible to nullify the effect of stress on R_{ON} without reducing the breakdown threshold value and without increasing the value of R_{ON} before the stress.

[0055] Finally, it is evident that modifications and variations may be made to the subject matter described and illustrated without thereby moving outside the scope of protection of the present invention, as defined in the attached claims.

[0056] For example, the metallization of the contacts (source, drain, gate) on the front of the wafer can be carried out using any variants known in the literature, such as the formation of contacts using AlSiCu/Ti, Al/Ti, or W-plug, and the like.

[0057] Furthermore, the buffer layer 4, the hole-supply layer 6 and the heterostructure 7 can be made of other materials selected from compound materials in the group III-V.

Claims

1. High-electron-mobility field-effect transistor, HEMT, (1; 21; 31; 51) including:

   - a semiconductor body (15) including a buffer layer (4), a hole-supply layer (6) arranged on the buffer layer (4), and a heterostructure (7) arranged on the hole-supply layer (6), and
   - a source electrode (16),

   characterized in that the hole-supply layer (6) is made of P-type doped semiconductor material, and **in that** the source electrode (16) i
   s in direct electrical contact with the hole-supply layer (6), so that the hole-supply layer (6) can be biased to favour the transport of holes from the hole-supply layer (6) to the buffer layer (4).

2. HEMT according to claim 1, wherein the heterostructure (7) includes a channel layer (10) arranged on the hole-supply layer (6), and a barrier layer (9) arranged on the channel layer (10), and in which the channel layer (10) and the barrier layer (9) are made of respective compound materials including elements in the group III-V.

3. HEMT according to claim 2, wherein a thickness t_u of the channel layer (10), a surface concentration N_A of dopant species of the hole-supply layer (6) and a thickness t_p of the hole-supply layer (6) are determined using the following equation:

$$t_{\mathrm{p}} > -t_{\mathrm{u}} + \sqrt{t_{\mathrm{u}}^2 + 2\frac{\varepsilon B}{q N_{\mathrm{A}}}} + \sqrt{\frac{2\varepsilon E_{\mathrm{A}}}{q N_{\mathrm{A}}}}$$

   where q is the elementary charge; B is the band gap of the semiconductor material of the buffer layer (4); E_A is the distance of trap states from the valence band of the buffer layer (4); and ε is the dielectric constant of the semiconductor material of the hole-supply layer (6).

4. HEMT according to claim 2 or claim 3, wherein the thickness t_u of the channel layer (10) is between 100 nm and 500 nm, the surface concentration N_A of dopant species of the hole-supply layer (6) is greater than $6 \cdot 10^{16}$ cm^{-2}, and the thickness t_p of the hole-supply layer (6) is greater than 300 nm.

5. HEMT according to any one of claims 2 to 4, further comprising a gate region (14; 54) extending beyond the interface between the hole-supply layer (6) and the buffer layer (4), and ending within the buffer layer (4).

6. HEMT according to any one of claims 2 to 4, further comprising a gate region (14; 54) extending up to, o beyond, the interface between the barrier layer (9) and the channel layer (10), ending outside the hole-supply layer (6).

7. HEMT according to any one of claims 2 to 4, further comprising:

an insulating layer (12) arranged on the barrier layer (9) ; and
a gate region (14; 54) extending up to, or beyond, the interface between the insulating layer (12) and the barrier layer (9), ending outside the barrier layer (9).

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8. HEMT according to any one of claims 5 to 7, wherein the gate region (14; 54) includes a dielectric gate region (14a) and a conductive gate region (14b), the conductive gate region (14b) being electrically isolated from the semiconductor body (15) by the dielectric gate region (14a).

9. HEMT according to any one of claims 5 to 8, further comprising a drain electrode (18; 58) arranged at a distance from the source electrode (16) and in direct electrical contact with the semiconductor body (15),
and wherein the gate region (14; 54) is arranged at a distance from the source electrode (16) and from the drain electrode (18; 58).

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10. HEMT according to any one of the preceding claims, in which the buffer layer (4) includes impurities configured to generate trap states that facilitate the emission of holes from the buffer layer (4), thus forming a layer of negative charges inside therein.

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11. HEMT according to any one of claims 2 to 5, also including:

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- a drain electrode (58) extending up to the interface between the barrier layer (9) and the channel layer (10), and
- a gate electrode (54, 56) that includes a metal region (54) and a P-type doped gallium nitride region (56) between the metal region (54) and the heterostructure (7).

12. Method of manufacturing a high-electron-mobility field-effect transistor, HEMT, (1; 21; 31; 51), including the steps of:

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- forming a buffer layer (4) on a substrate (2),
- forming a hole-supply layer (6) on the buffer layer (4),
- forming a heterostructure (7) on the hole-supply layer (6), and
- forming a source electrode (16),

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characterized in that:

the step of forming the hole-supply layer (6) includes forming a layer of P-type doped semiconductor material, and the step of forming the source electrode (16) includes forming the source electrode (16) in direct electrical contact with the hole-supply layer (6), such that the hole-supply layer (6) can be biased to facilitate the transport of holes from the hole-supply layer (6) to the buffer layer (4) .

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13. Method according to claim 12, wherein the step of forming the heterostructure (7) includes:

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- forming a channel layer (10) on the hole-supply layer (6), and
- forming a barrier layer (9) on the channel layer (10), and in which the steps of forming the channel layer (10) and the barrier layer (9) include forming layers of respective compound materials including elements in the group III-V.

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14. Method according to claim 13, wherein the step of forming the channel layer (10) includes forming the channel layer (10) with a thickness t_u, and the step of forming the hole-supply layer (6) includes forming the hole-supply layer (6) with a surface concentration N_A of dopant species and a thickness t_p, the thicknesses t_u, t_p and the surface concentration N_A being determined using the following equation:

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$$t_{\mathrm{p}} > -t_{\mathrm{u}} + \sqrt{t_{\mathrm{u}}^2 + 2\frac{\varepsilon B}{qN_{\mathrm{A}}}} + \sqrt{\frac{2\varepsilon E_{\mathrm{A}}}{qN_{\mathrm{A}}}}$$

55

where q is the elementary charge, B is the band gap of the semiconductor material of the buffer layer (4), E_A is the distance of the trap states from the valence band of the buffer layer (4), and ε is the dielectric constant of the semiconductor material of the hole-supply layer (6).

15. Method according to claim 13 or 14, wherein:

- the step of forming the channel layer (10) includes forming a channel layer (10) with a thickness (t_u) of between 100 nm and 500 nm,
- the step of forming the hole-supply layer (6) includes forming a hole-supply layer (6) with a surface concentration (N_A) of dopant species greater than $6 \cdot 10^{16}$ cm^{-2}, and a thickness (t_p) greater than 300 nm.

16. Method according to any one of claims 12 to 15, wherein the step of forming the buffer layer (4) includes introducing impurities into the buffer layer (4), said impurities being designed to generate trap states that facilitate the emission of holes from the buffer layer (4), thus forming a layer of negative charges inside same.

17. Method according to any one of claims 13 to 16, further comprising the step of forming a gate electrode (14; 54), including: etching a trench through the barrier layer (9), the channel layer (10), the hole-supply layer (6) and, in part, the buffer layer (4) ; and filling-in said trench by a dielectric gate region (14a) and a conductive gate region (14b) in such a way that the conductive gate region (14b) is electrically isolated from the barrier layer (9), the channel layer (10), the hole-supply layer (6) and the buffer layer (4) through the dielectric gate region (14a).

18. Method according to any one of claims 13 to 16, further comprising the step of forming a gate electrode (14; 54), including: etching a trench through the barrier layer (9) up to the interface between the barrier layer (9) and the channel layer (10), ending outside the hole-supply layer (6); and filling-in said trench by a dielectric gate region (14a) and a conductive gate region (14b).

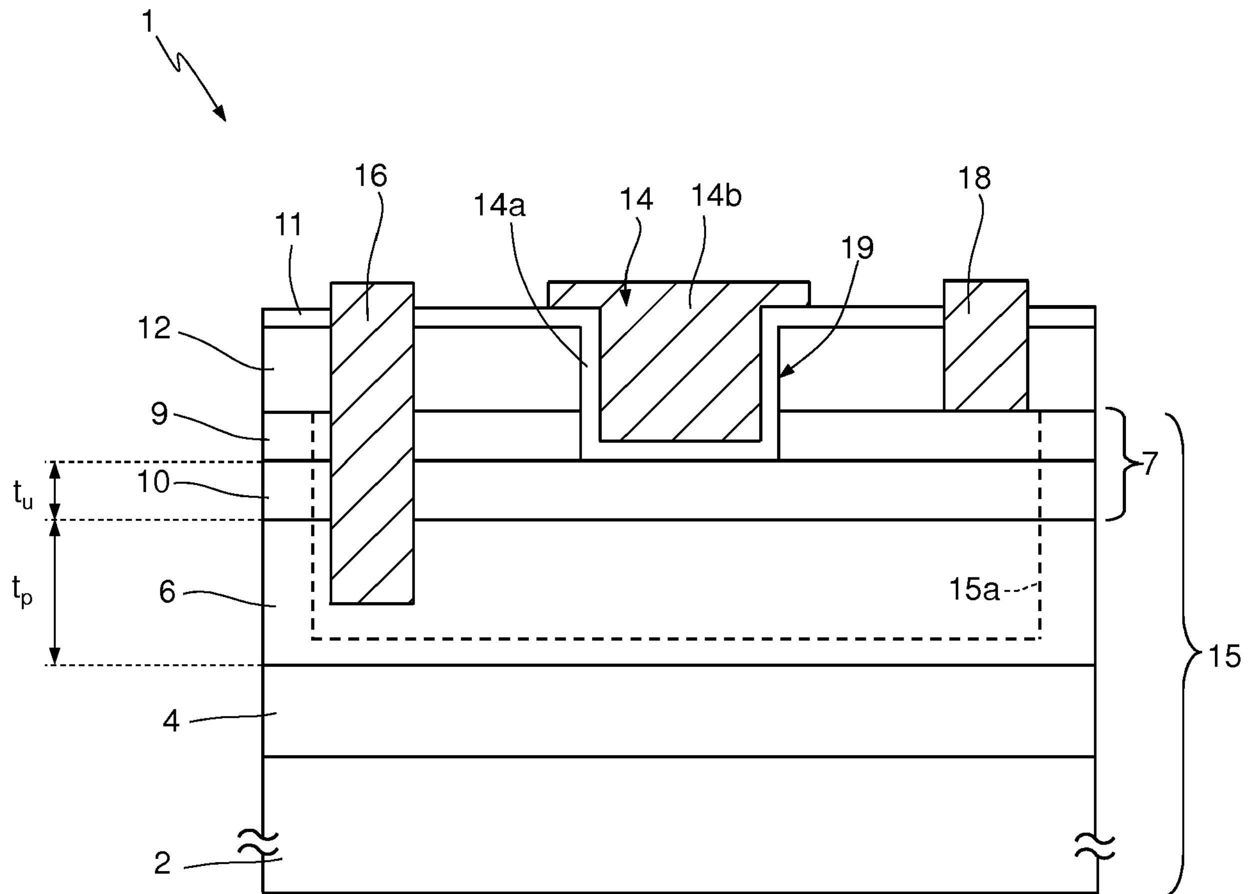
19. Method according to any one of claims 13 to 16, further comprising the step of forming an insulating layer (12) on the barrier layer (9),
The step of forming the gate electrode (14; 54) including: etching a trench through the barrier layer (9) up to the interface between the insulating layer (12) and the barrier layer (9), ending outside the barrier layer (9); and filling-in said trench by a dielectric gate region (14a) and a conductive gate region (14b).

20. Method according to any one of claims 13 to 16, further including the steps of:

- forming a drain electrode (58) up to the interface between the barrier layer (9) and the channel layer (10), and
- forming a gate electrode (54, 56),

in which the step of forming the gate electrode (54, 56) includes:

- forming a metal region (54), and
- forming a P-type doped gallium nitride region (56) between the metal region (54) and the heterostructure (7).



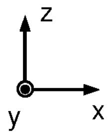


Fig.1

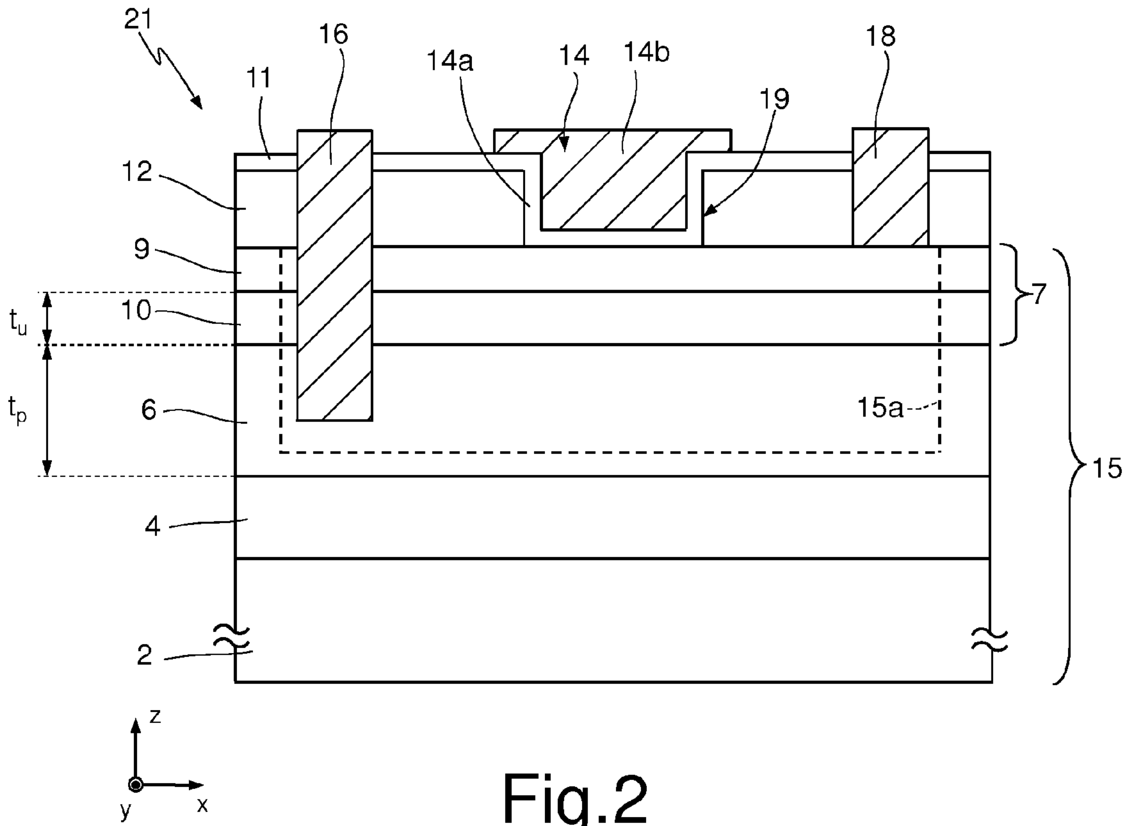


Fig.2

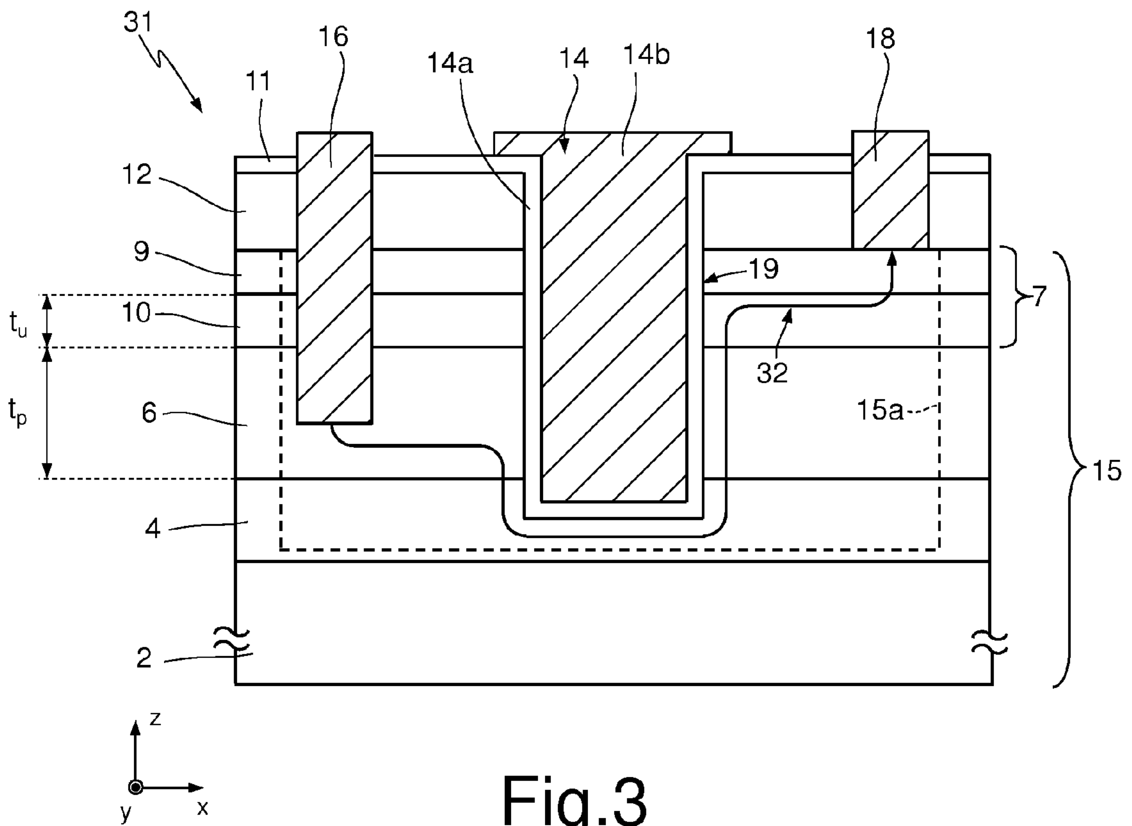


Fig.3

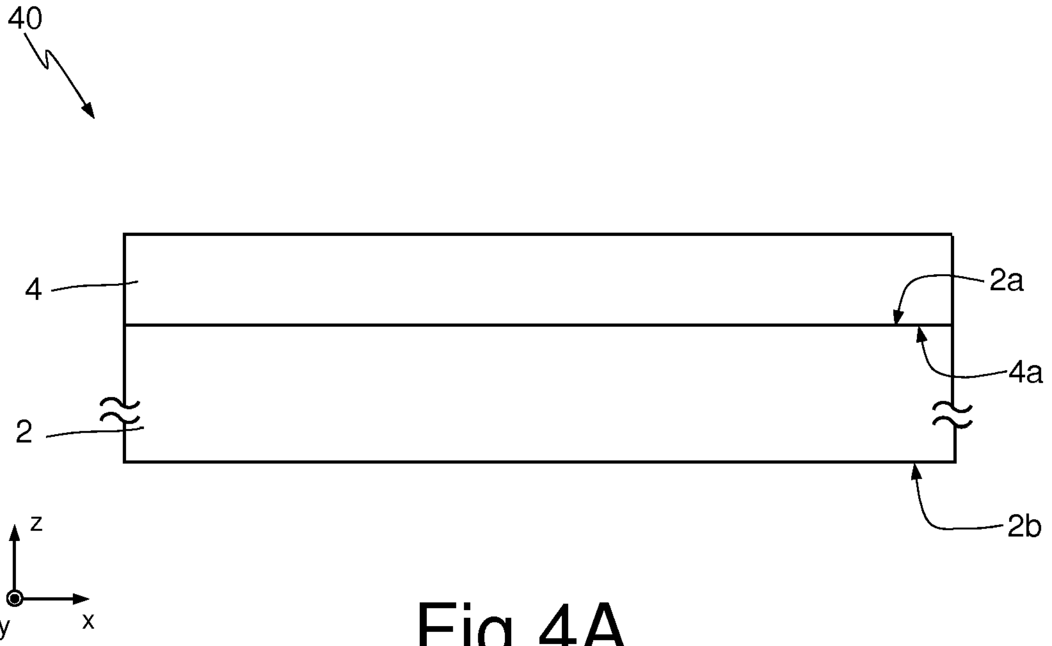


Fig.4A

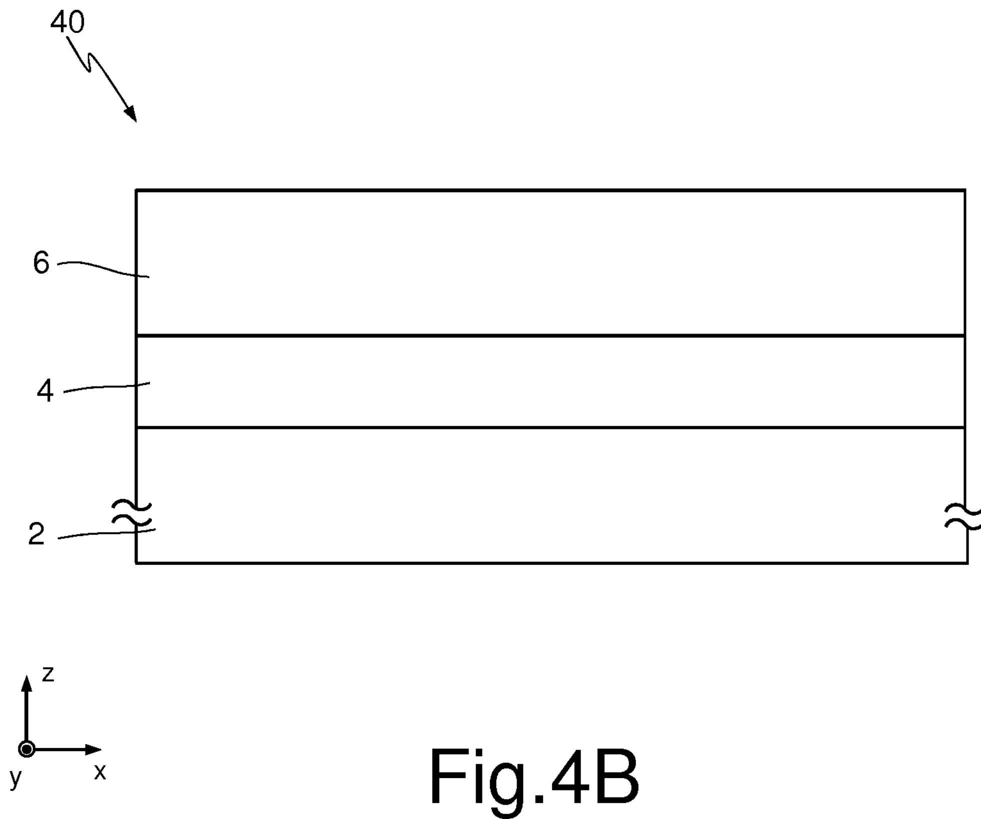


Fig.4B

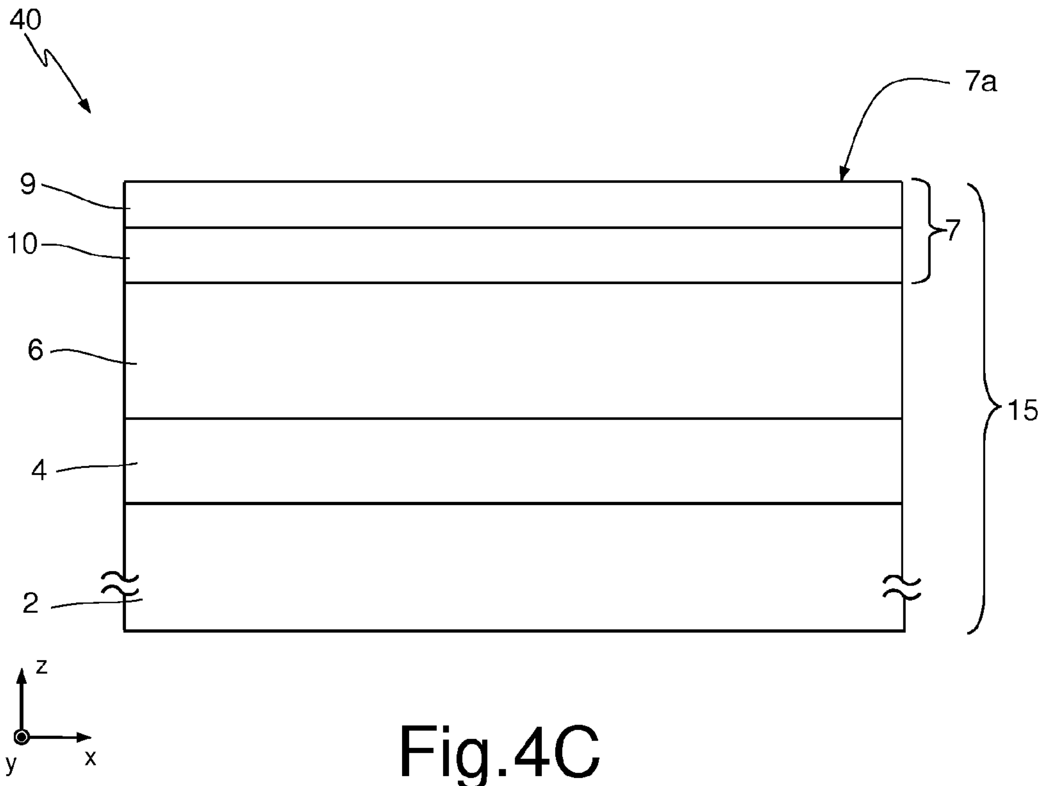


Fig.4C

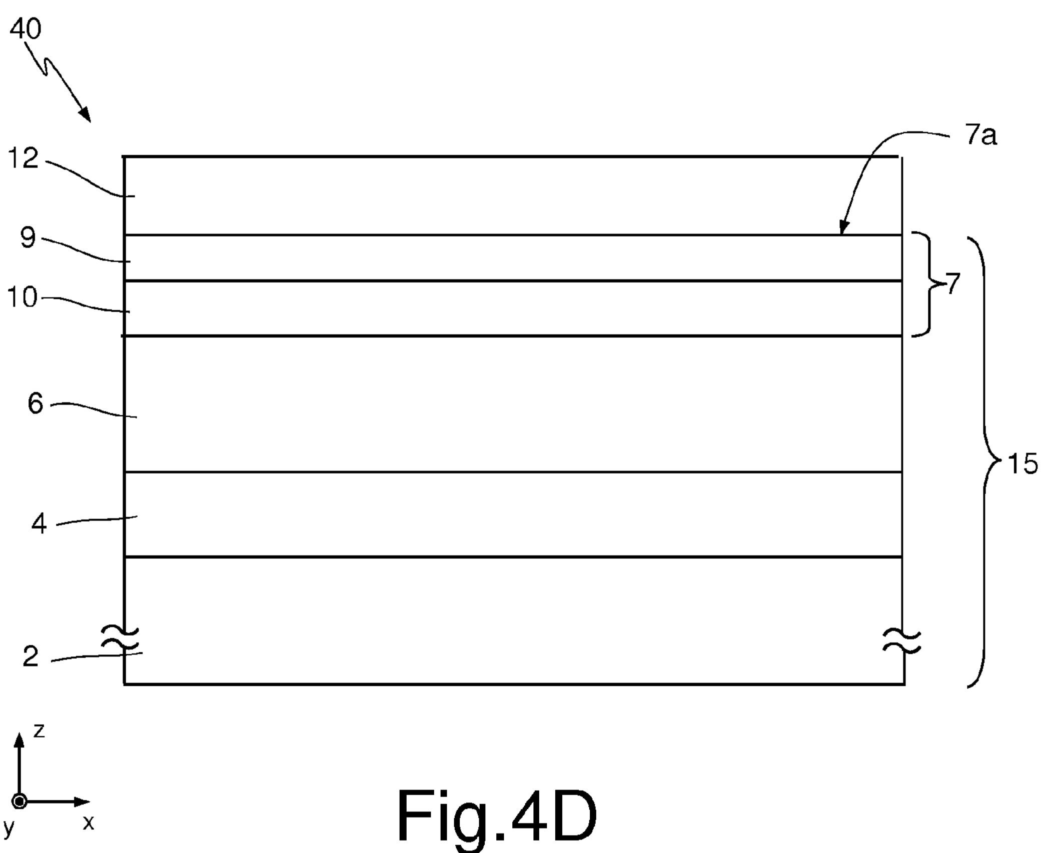


Fig.4D

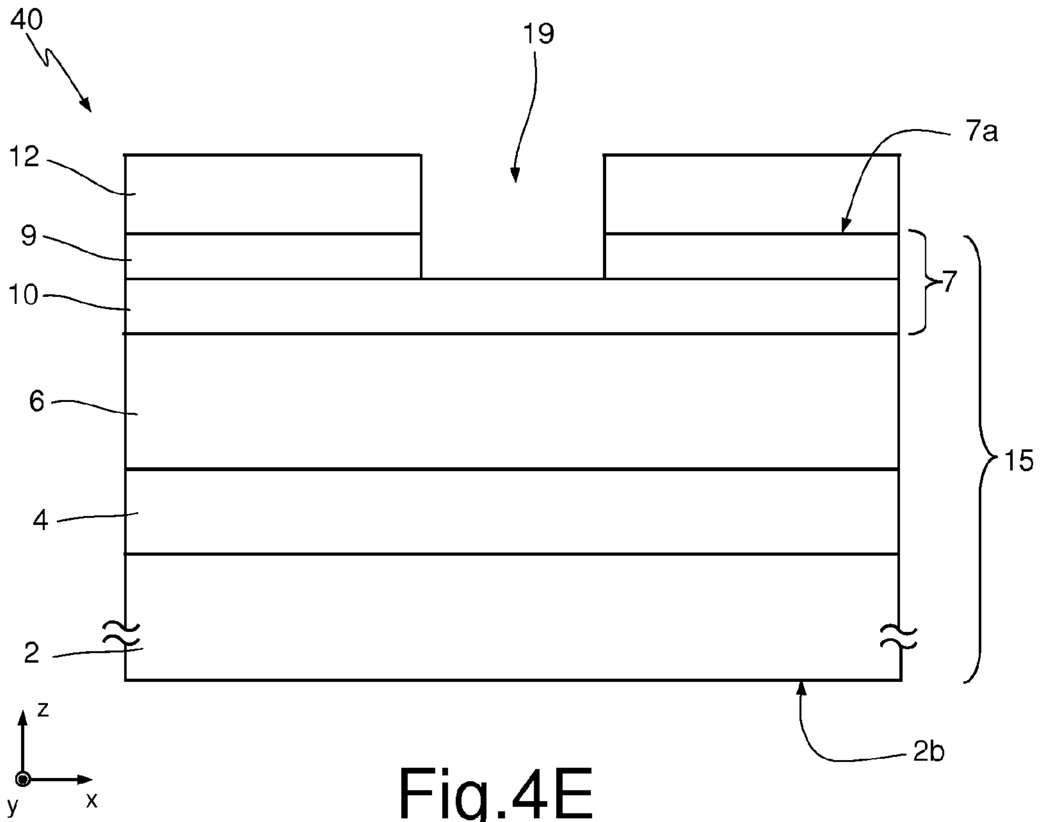


Fig.4E

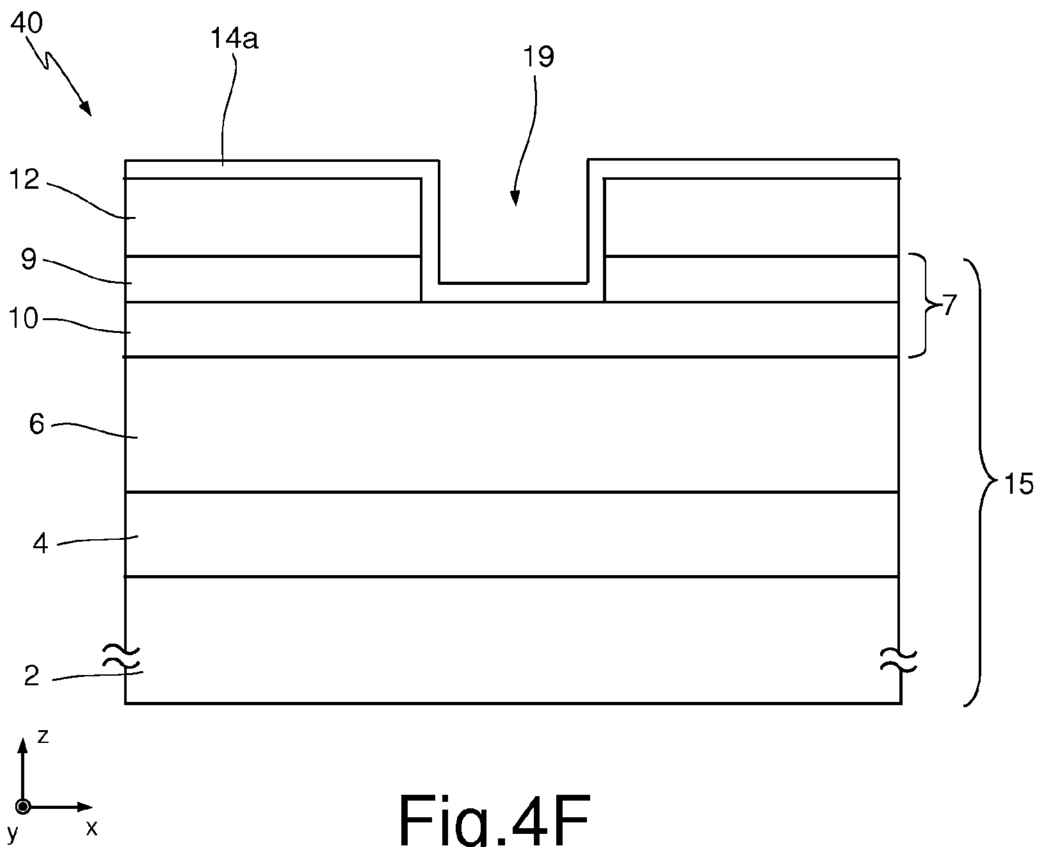


Fig.4F

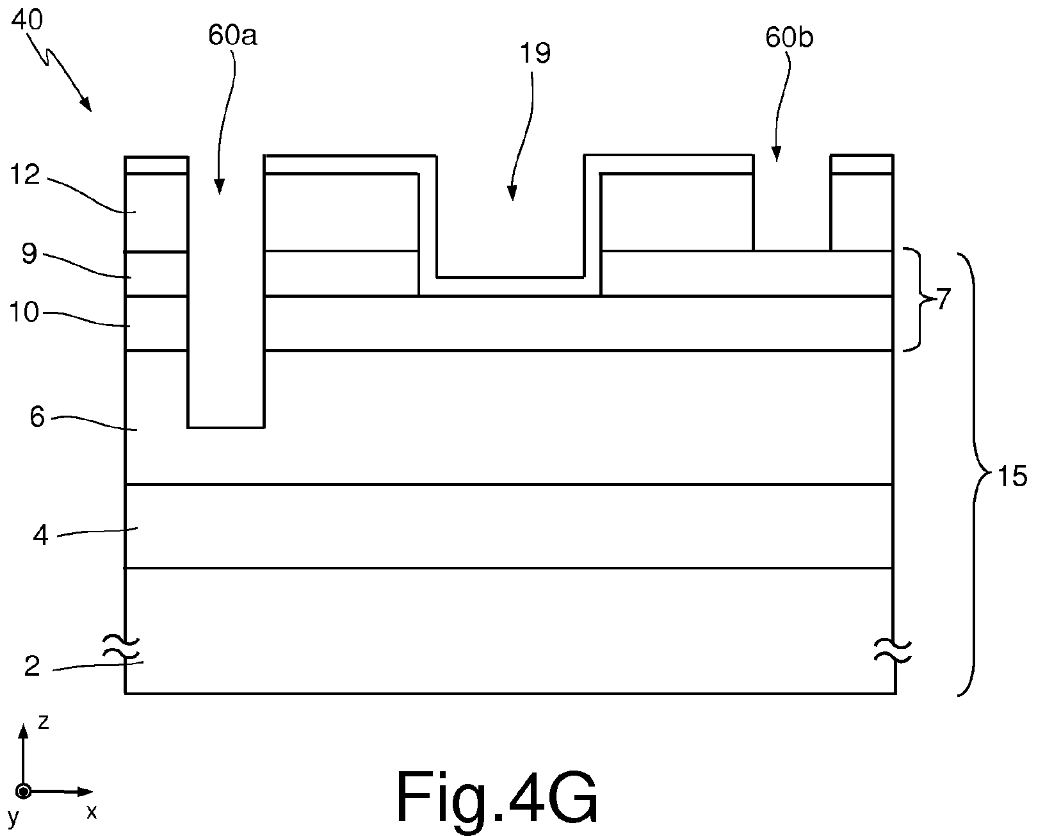


Fig.4G

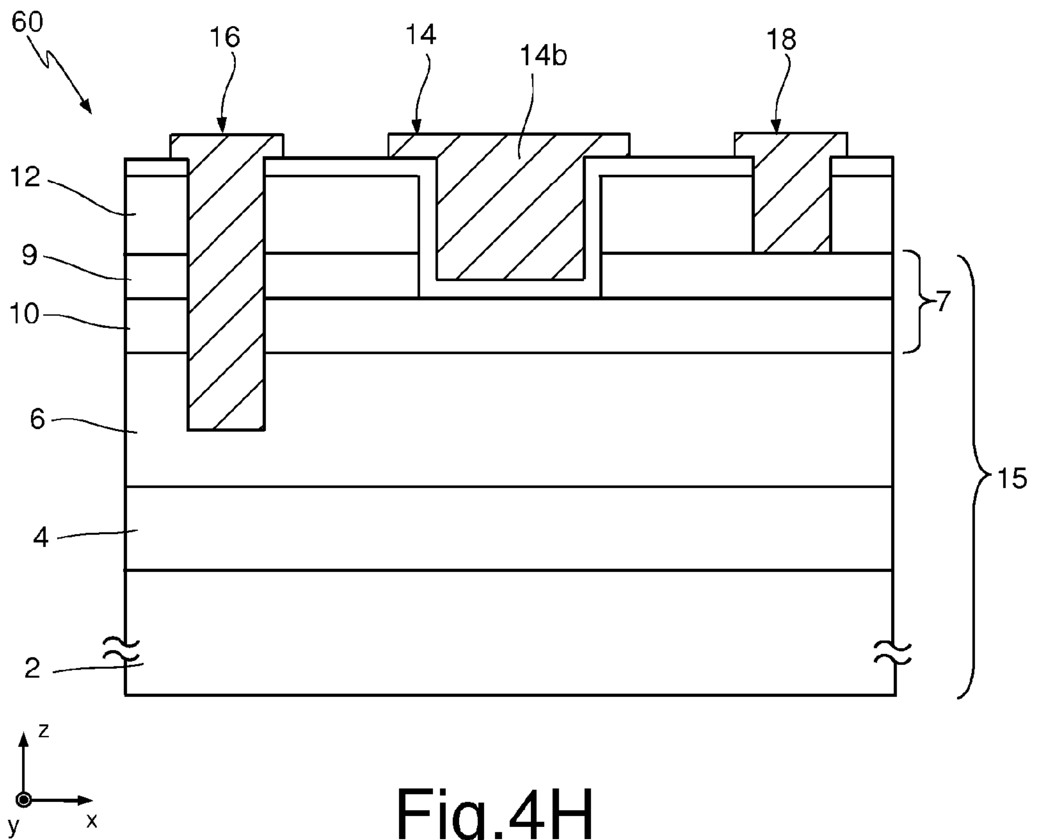
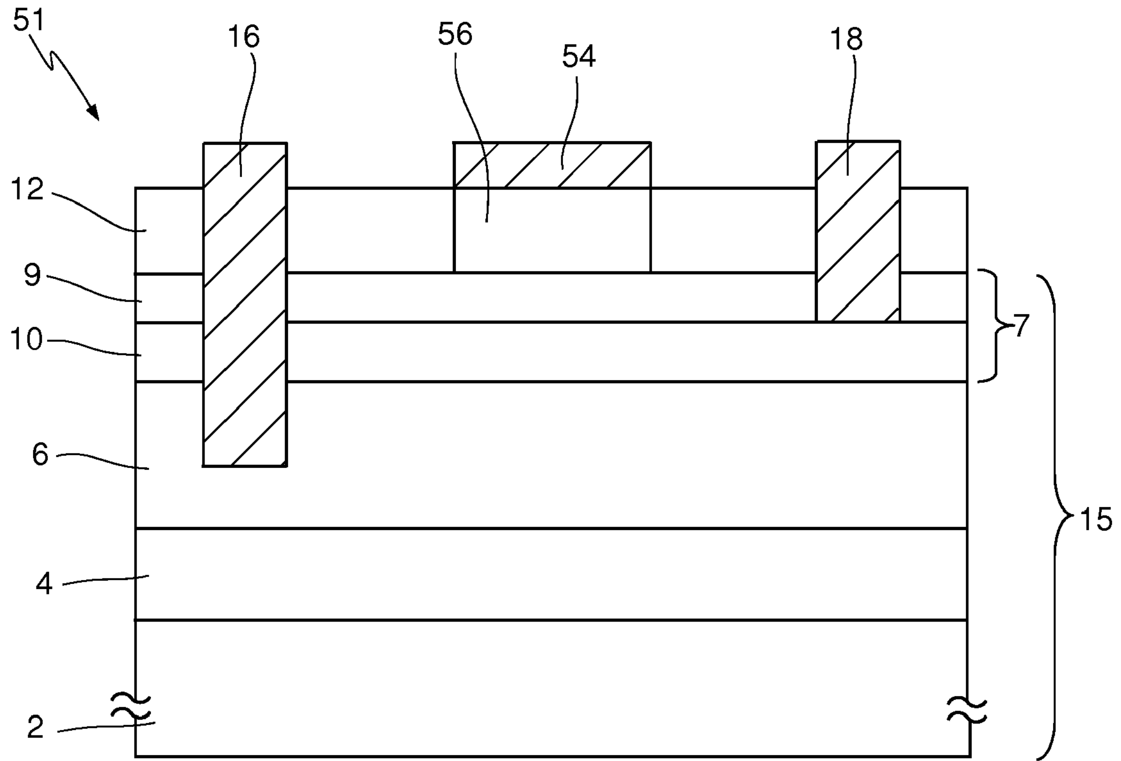


Fig.4H



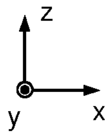


Fig.5

EUROPEAN SEARCH REPORT

Application Number
EP 18 17 6875

5 10 15 20 25 30 35 40 45 50 55

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	EP 2 884 539 A1 (RENESAS ELECTRONICS CORP [JP]) 17 June 2015 (2015-06-17) * e.g. figures 28, 42 and associated text *	1-4, 6-16, 18-20	INV. H01L29/778 H01L21/336 H01L29/10 H01L29/417
X	EP 2 028 694 A2 (SHARP KK [JP]) 25 February 2009 (2009-02-25) * e.g. figures 1, 4 and associated text *	1-20	ADD. H01L29/423 H01L29/207 H01L29/20
X	US 2011/272708 A1 (YOSHIOKA AKIRA [JP] ET AL) 10 November 2011 (2011-11-10) * e.g. figure 3 and associated text *	1-10, 12-17	

TECHNICAL FIELDS SEARCHED (IPC)
H01L

The present search report has been drawn up for all claims

1

Place of search	Date of completion of the search	Examiner
Munich	26 October 2018	Moehl, Sebastian

CATEGORY OF CITED DOCUMENTS

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5

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