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(54) **Fabrication of single or multiple gate field plates**

Herstellung von einfachen oder mehrfachen Gatefeldplatten

Fabrication de plaques de champ de grille unique ou multiple

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention.

[0001] This invention relates to semiconductor devices, and more particularly, to the fabrication of single or multiple gate field plates.

2. Description of the Related Art.

[0002] (Note: This application references to various publications as indicated in the specification by reference numbers enclosed in brackets, e.g., [x]. A list of these publications ordered according to these reference numbers can be found below in the section entitled "References.")

[0003] In a semiconductor-based field effect transistor (FET), a large electric field arises during normal operation in the gate-drain access region. Field plating is a well-known technique for improving device performance under high electric field operation as well as alleviating surface traps phenomena [1], [2]. For example, field plating has been an effective and well-known technique in order to alleviate all the detrimental effects (breakdown voltages, trapping effects, reliability) that take places in devices operating at high electric field. An example of a GaAs-based HEMT with a gate comprising a field-plate extension towards the drain on a SiN passivation layer is known from reference [17].

[0004] The basic concept of field plating relies on the vertical depletion of the device active region, thus enabling larger extensions of the horizontal depletion region. This results in a lower electric field in the device active region for a given bias voltage, alleviating all the detrimental effects (low breakdown, trapping phenomena, poor reliability) that take place whenever a device is operated at a high electric field. Moreover, a field plate positioned in the gate drain access region has also the capability of modulating the device active region, resulting in a decrease of surface traps effects that prevent proper device operation under large radio frequency (RF) signals

[0005] What is needed, however, are improved methods of fabricating single or multiple gate field plates as well as improved structures incorporating single or multiple gate field plates.

SUMMARY OF THE INVENTION

[0006] The present invention provides a method of fabricating a III-Nitride High Electron Mobility Transistor (HEMT) according to claim 1, and a HEMT according to claim 3.

[0007] Also discussed herein are improved methods of fabricating single and multiple gate field plates. A fabrication process discussed herein uses consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation on the surface of field effect transistors. The advantages of the fabrication process include tight control of the dielectric material thickness, and the absence of any exposure of the surface of the device active region to any dry or wet etch process that may induce damage in the semiconductor material forming the field effect transistor. Moreover, the dielectric material deposited on the device surface does not need to be removed from the device intrinsic regions, which enables the realization of field-plated devices without damage caused by the dry or wet etch processes. Using multiple gate field plates reduces gate resistance through the use of multiple connections, thus improving performances of large periphery and/or sub-micron gate devices. Finally, by properly adjusting the thickness of the dielectric material, parallel gate contacts can be deposited on top of the dielectric material, in order to significantly reduce gate resistance by electrically connecting the parallel gate contacts on device extrinsic regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1A is a cross-sectional and FIG. 1B is a top view of a field effect transistor (FET);
FIG. 2A is a device cross-section and FIG. 2B is a device top view illustrating dielectric material deposition/growth;
FIG. 3A is a device cross-section and FIG. 3B is a device top view illustrating dielectric material being removed from device extrinsic regions;
FIG. 4A is a device cross-section and FIG. 4B is a device top view illustrating evaporation of gate field plate;
FIG. 5A is a device cross-section and FIG. 5B is a device top view illustrating an example of multiple field plate structure;
FIG. 6 is a graph of simulation of f_{max} dependence vs. gate finger width;
FIG. 7A is a device cross-section, FIG. 7B is a device top view and FIG. 7C is a device cross-section illustrating a multiple field plate device for reduced gate resistance;
FIG. 8 is a schematic cross-section of a unit cell of a nitride-based HEMT (High Electron Mobility Transistor) device;
FIG. 9 is a schematic cross-section of a unit cell of a nitride-based HEMT device having a different configuration from the device illustrated in FIG. 8; and
FIG. 10 is a graph that illustrates the effect of field plate distance on device performance.

[0009] Only the device shown in Fig. 8 is a device according to the present invention. Devices shown in other figures are alternative devices not according to the present invention but which nevertheless provide background information useful for understanding the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0010] In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Overview

[0011] Below is described a simple fabrication process for the realization of single or multiple gate field plate structures for field effect transistors (FETs). This process uses simple and typically well-controlled consecutive processing steps of dielectric material deposition or growth, dielectric material etch and metal evaporation.

Fabrication Process

[0012] FIGS. 1A, 1B, 2A, 2B, 3A, 3C, 4A, and 4B illustrate the steps of one possible realization of the fabrication process, wherein the fabrication process comprises a method of fabricating gate field plates.

[0013] FIG. 1A is a cross-sectional and FIG. 1B is a top view of a field effect transistor (FET) 10 that includes source and drain ohmic contacts 12 and 14, a gate contact 16 and an active region 18. The steps of the fabrication process are applied on the field effect transistor 10 or other device. The method generally comprises performing consecutive steps of dielectric material deposition or growth, dielectric material etch and metal evaporation to create one or more field plates on a surface of the device, wherein the steps permit a tight control on field plate operation and wherein the dielectric material deposited on the surface does not need to be removed from the active region 18, thereby enabling realization of a field-plated device without using a low-damage dielectric material dry or wet etch process. The performing step further comprises the steps of: (1) depositing or growing the dielectric material on the intrinsic and extrinsic regions of the device, wherein the dielectric material thickness is controlled in order to achieve proper operation of the device; (2) patterning the dielectric material by the dry or wet etch process or by a lift-off process, so that the dielectric material remains principally on an active region of the device; and (3) evaporating a field plate on the patterned dielectric material, wherein gate and field plate contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween. These steps are described in more detail below in conjunction with FIGS. 2A, 2B, 3A, 3B, 4A and 4B.

[0014] FIG. 2A is a device cross-section and FIG. 2B is a device top view illustrating the first step of the fabrication process, which comprises depositing or growing the dielectric material 20 on intrinsic and extrinsic regions of the device 10. The dielectric material 20 thickness is the critical parameter to be controlled in order to achieve proper operation of the finished device 10. However, this is usually a well controlled process in most deposition/growth techniques, e.g., PECVD (Plasma Enhanced Chemical Vapor Deposition). Typical materials are silicon nitrides and oxides, but others can be used, as long as they can be patterned by dry or wet etching or by lift-off.

[0015] FIG. 3A is a device cross-section and FIG. 3B is a device top view illustrating the second step of the fabrication process, which comprises patterning the dielectric material 20, by etch or removal from device extrinsic regions 22, so that the dielectric material 20 remains principally on an active region 18 of the device 10. In the case where the pattern is formed by etching, it should be stressed that the device 10 surface will be protected during this step, preventing any exposure of the surface of the active region 18 to any dry or wet etch process that may induce damage in the semiconductor material forming the device. After this step, ohmic contacts 12, 14 are electrically accessible, as well as the gate portion 16 that resides in the device extrinsic region 22.

[0016] FIG. 4A is a device cross-section and FIG. 4B is a device top view illustrating the third step of the fabrication process, which comprises creating a field plate 24 on the patterned dielectric material 20, wherein gate 16 and field plate 24 contacts are electrically shorted at least at one side of the extrinsic region, providing a low resistance connection therebetween. Preferably, metal evaporation is used to form the field plate 24, wherein the field plate 24 comprised of a metal stripe or contact. The field plate 24 is positioned in a gate 16 drain access region, thereby providing a capability of modulating the active region 18, resulting in a decrease of surface traps effect that prevent proper device operation under large RF signals. The field plate 24 is connected to both sides of the device intrinsic region, and the gate 16 and field plate 24 are electrically shorted at least at one side of the extrinsic region 22, providing a low resistance connection between the two metal lines thereof. The offset and length of the field plate 24 are optimized with respect to the targeted device performance, i.e., breakdown voltage, RF performance, etc.

[0017] If a multiple field plate structure is required, the three steps of dielectric material deposition/growth, dielectric material etch and metal evaporation described in FIGS. 2A, 2B, 3A, 3B, 4A and 4B can be repeated.

[0018] FIG. 5A is a device cross-section and FIG. 5B is a device top view illustrating an example of creating multiple connections using multiple gate field plates in order to reduce gate resistance, thereby improving the performance of a large periphery device and/or sub-micron gate device. This example is a two field plate structure, which includes another layer of dielectric material 26 and another field plate 28 comprised of a metal stripe or contact. Dielectric material 26 thickness, field plate 28 length and offset with respect to the gate 16 and other field plates 24, and the number of field plates 24, 28 introduced, comprise fabrication process parameters. Using multiple field plates 24, 28 allows more freedom in device 10 design, and has a significant impact in the realization of high voltage devices 10.

[0019] Another advantage of the processes discussed herein is the possibility of alleviating the decrease in RF performance induced by gate resistance in a large periphery device. Typically, the frequency of maximum oscillation (f_{max}) decreases at the increasing of the gate finger width due to the increase in gate resistance.

[0020] FIG. 6 is a graph of simulation of fmax dependence vs. gate finger width. As indicated in the graph, the introduction of a field plate structure shorted on both ends of the active region can improve f_{max} performances of devices with large finger width. Using a field plate with a resistance Rf equivalent to the gate resistance Rg and connected to both sides of the active region significantly improves f_{max} performance. Further improvement can be achieved by lowering field plate resistance. It should be stressed that this decrease will be observed only if the parasitic capacitances added by the field plate structure are negligible compared to those of the intrinsic device. This can be achieved by proper choice of dielectric material and its thickness, and has to be considered as an optimization process.

[0021] Multiple connections between the gate and field plate also results in a significant decrease in the gate resistance. In order to achieve this multiple connection without severely degrading RF operation, a small portion of the active region is etched prior to gate deposition to create the multiple connections between the gate and the field plates without degrading the device's RF operation.

[0022] In this region, the gate and field plates can be connected without introducing any additional parasitic capacitance to the device. Again, device performance improves only if the introduced parasitic capacitance is small as compared to those of the intrinsic device. Furthermore, the spacing between individual active regions is used to engineer the thermal impedance of the device more effectively than a device with a conventional topology.

[0023] Critical parameters are the choice of dielectric material, the thickness of the dielectric material, and the length of the field plates. These critical parameters have to be considered as optimization steps of the proposed fabrication process.

[0024] Using this method allows the fabrication of large periphery devices with a reduced number of air bridges. Moreover, the fabrication of sub-micron devices can take advantage of the present invention. Typically, sub-micron gates are fabricated using a T-shape process, since the T-shape reduces gate resistance as compared to a standard gate shape. Low gate resistance can be achieved even with sub-micron gates by creating the multiple connections without a T-shape process.

[0025] In addition, a parallel gate contact can be deposited on top of the dielectric material by properly adjusting the material dielectric thickness, in order to significantly reduce gate resistance by creating multiple connections using the parallel field plates on the device extrinsic regions. The low resistance path is provided by the parallel field plates, through a proper choice of the width at which the connection between the gate and field plates occurs.

[0026] FIG. 7A is a device cross-section, FIG. 7B is a device top view and FIG. 7C is a device cross-section illustrating examples of multiple field plate structures for reduced gate resistance. Moreover, having a field plate covering the gate source access region, such as shown in FIGS. 7A, 7B and 7C, is also used for of modulating source access resistance for improving device linearity performance.

Gallium Nitride-Based High Electron Mobility Transistor with Field Plates

[0027] GaN based transistors including AlGaN/GaN High Electron Mobility Transistors (HEMTs) are capable of very high voltage and high power operation at RF, microwave and millimeter-wave frequencies. However, electron trapping and the ensuing difference between DC and RF characteristics has limited the performance of these devices. SiN passivation has been successfully employed to alleviate this trapping problem, resulting in high performance devices with power densities over 10 W/mm at 10 GHz. For example, [3] discloses methods and structures for reducing the trapping effect in GaN transistors. However, due to the high electric fields existing in these structures, charge trapping is still an issue.

[0028] The present invention has been successfully utilized for improving the performance of AlGaN/GaN HEMT power devices. At 4 GHz operation, power densities of 12W/mm and 18.8W/mm have been achieved for devices on sapphire and silicon carbide substrate, respectively. Due to the simplicity of the processing step involved in the field plate fabrication, the present invention can be used in the development of Al GaN/GaN HEMTs technology and other semiconductor devices. Using properly designed multiple field plates greatly improves both breakdown and large RF signal performance in such devices.

[0029] A GaN-based HEMT includes a channel layer and a barrier layer on the channel layer. Metal source and drain ohmic contacts are formed in contact with the barrier layer. A gate contact is formed on the barrier layer between the source and drain contacts and a spacer layer is formed above the barrier layer. The spacer layer may be formed before or after formation of the gate contact. The spacer layer may comprise a dielectric layer, a layer of undoped or depleted $Al_xGa_{1-x}N$ (0<=x<=1) material, or a combination thereof. A conductive field plate is formed above the spacer layer and extends a distance Lf (field plate distance) from the edge of the gate contact towards the drain contact. The field plate may be electrically connected to the gate contact. In some embodiments, the field plate is formed during the same deposition step as an extension of the gate contact. In other embodiments, the field plate and gate contact are formed during separate deposition steps. This arrangement may reduce the peak electric field in the device resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field may also yield other benefits such as reduced leakage currents and enhanced reliability.

[0030] An embodiment of the invention is illustrated in FIG. 8, which is a schematic cross-section of a unit cell 30 of a nitride-based HEMT device. Specifically, the device 30 includes a substrate 32, which may comprise silicon carbide, sapphire, spinel, ZnO, silicon or any other material capable of supporting growth of Group III-nitride materials. An $Al_zGa_{1-z}N$ (0<=z<=1) nucleation layer 34 is grown on the substrate 32 via an epitaxial crystal growth method, such as MOCVD (Metalorganic Chemical Vapor Deposition), HVPE (Hydride Vapor Phase Epitaxy) or MBE (Molecular Beam Epitaxy). The formation of nucleation layer 34 may depend on the material of substrate 32. For example, methods of forming nucleation layer 34 on various substrates are taught in [4] and [5]. Methods of forming nucleation layers on silicon carbide substrates are disclosed in [6], [7] and [8].

[0031] A high resistivity Group III-nitride channel layer 36 is formed on the nucleation layer 34. Channel layer 36 may comprise $Al_xGa_yIn_{(1-x-y)}N$ (0<=x<=1, 0<=y<=1, x+y<=1). Next, an $Al_xGa_{1-x}N$ (0<=x<=1) barrier layer 38 is formed on the channel layer 36. Each of the channel layer 36 and barrier layer 38 may comprise sub-layers that may comprise doped or undoped layers of Group III-nitride materials. Exemplary structures are illustrated in [3], [9], [10], [11] and [12]. Other nitride-based HEMT structures are illustrated in [13] and [14].

[0032] In the embodiment illustrated in FIG. 8, a Group III-nitride semiconductor spacer layer 40 is grown on the $Al_xGa_{1-x}N$ barrier layer 28. Spacer layer 40 may have a uniform or graded composition. Spacer layer 40 may be undoped and/or may be designed to be fully depleted as grown.

[0033] Source 42 and drain 44 electrodes are formed making ohmic contacts through the barrier layer 38 such that an electric current flows between the source and drain electrodes 42, 44 via a two-dimensional electron gas (2DEG) induced at the heterointerface between the channel layer 36 and barrier layer 38 when a gate electrode 46 is biased at an appropriate level. The formation of source and drain electrodes 42, 44 is described in detail in the patents and publications referenced above.

[0034] The spacer layer 40 may be etched and the gate electrode 46 deposited such that the bottom of the gate electrode 46 is on the surface of barrier layer 38. The metal forming the gate electrode 46 is patterned to extend across spacer layer 40 so that the top of the gate 46 forms a field plate structure 48 extending a distance Lf away from the edge of gate 46 towards drain 44. Stated differently, the part of the gate 46 metal resting on the spacer layer 40 forms an epitaxial field plate 48. Finally, the structure is covered with a dielectric passivation layer 50 such as silicon nitride. Methods of forming the dielectric passivation 50 are described in detail in the patents and publications referenced above.

[0035] An alternative device not according to the invention is illustrated in FIG. 9, which is a schematic cross-section of a unit cell 30 of a nitride-based HEMT device having a different configuration from the device illustrated in FIG. 8. The substrate 32, nucleation layer 34, channel layer 36 and barrier layer 38 in the device 30 illustrated in FIG. 9 are similar to the corresponding layers illustrated in FIG. 8. In some arrangements, the substrate 32 comprises semi-insulating 4H-SiC commercially available from Cree, Inc. of Durham, N.C., the nucleation layer 34 is formed of AlN, and the channel layer 36 comprises a 2 μm thick layer of GaN:Fe, while barrier layer 38 comprises 0.8 nm of AlN and 22.5 nm of $Al_xGa_{1-x}N$, wherein x = 0.195, as measured by PL (photoluminescence).

[0036] The gate electrode 46 is formed after formation of barrier layer 38 and passivation layer 50 is deposited on the device. A field plate 48 is then formed on the passivation layer 50 overlapping the gate 46 and extending a distance Lf in the gate-drain region. In the device illustrated in FIG. 9, passivation layer 50 serves as a spacer layer for the field plate 48. The overlap of the field plate 48 above the gate 46 and the amount of extension in the gate-drain region may be varied for optimum results. Field plate 48 and gate 46 may be electrically connected with a via or other connection (not shown).

[0037] In some arrangements, the field plate 48 may extend a distance Lf of 0.2 to 1 μm. In some arrangements, the field plate 48 may extend a distance Lf of 0.5 to 0.9 μm. In preferred arrangements, the field plate 48 may extend a distance Lf of 0.7 μm.

[0038] A GaN-based HEMT structure in accordance with the device of FIG. 9 was constructed and tested. The device achieved a power density of 32 W/mm with 55% Power Added Efficiency (PAE) operating at 120 V and 4GHz.

[0039] The effect of field plate distance (Lf) on device performance was tested. Devices were fabricated generally in accordance with the device of FIG. 9 except that the field plate length Lf was varied from a distance of 0 to 0.9 μm. The PAE of the resulting devices was then measured. As illustrated in FIG. 10, the PAE showed improvement once the field plate length was extended to 0.5 μm, with an optimum length of about 0.7 μm. However, the optimum length may depend on the specific device design as well as operating voltage and frequency.

References

[0040]

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[2] Y. Ando et al. "10-W/mm AlGaN-GaN HFET With a Field Modulating Plate," IEEE Electron Device Letters, Vol. 24, No. 5, May 2003, pp. 289-291.

[3] U.S. Patent No. 6,586,781, issued July 1, 2003, to Wu, et al., entitled "Group III nitride based FETs and HEMTs with reduced trapping and method for producing the same."

[4] U.S. Patent No. 5,290,393, issued March 1, 1994, to Nakamura, entitled "Crystal growth method for gallium nitride-based compound semiconductor."

[5] U.S. Patent No. 5,686,738, issued November 11, 1997, to Moustakas, entitled "Highly insulating monocrystalline gallium nitride thin films."

[6] U.S. Patent No. 5,393,993, issued February 28, 1995, to Edmond, et al., entitled "Buffer structure between silicon carbide and gallium nitride and resulting semiconductor devices."

[7] U.S. Patent No. 5,523,589, issued June 4, 1996, to Edmond, et al., entitled "Vertical geometry light emitting diode with group III nitride active layer and extended lifetime."

[8] U.S. Patent No. 5,739,554, issued April 14, 1998, to Edmond, et al., entitled "Double heterojunction light emitting diode with gallium nitride active layer."

[9] U.S. Patent No. 6,316,793, issued November 13, 2001, to Sheppard, et al., entitled "Nitride based transistors on semi-insulating silicon carbide substrates."

[10] U.S. Patent No. 6,548,333, issued April 15, 2003, to Smith, entitled "Aluminum gallium nitride/gallium nitride high electron mobility transistors having a gate contact on a gallium nitride based cap segment."

[11] U.S. Patent Application Publication No. 2002/0167023, published November 14, 2002, by Chavarkar, Prashant; et al., entitled "Group-III nitride based high electron mobility transistor (HEMT) with barrier/spacer layer."

[12] U.S. Patent Application Publication No. 2003/0020092, published January 30, 2003, by Parikh, Primit, et al., entitled "Insulating gate AlGaN/GaN HEMT."

[13] U.S. Patent No. 5,192,987, issued March 9, 1993, to Khan, et al., entitled "High electron mobility transistor with GaN/$Al_xGa_{1-x}N$ heterojunctions."

[14] U.S. Patent No. 5,296,395, issued March 22, 1994, to Khan, et al., entitled "Method of making a high electron mobility transistor."

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[16] S. Karmalkar, U.K. Mishra, Very high voltage AlGaN-GaN HEMT using a field plate deposited on a stepped insulator, Solid State Electronics, 45 (2001) 1645-1652.

[17] U.S. Patent No. 6,586,813, issued July 1, 2003, to Masaki, et al, entitled "High-Speed compound semiconductor device operable at large output power with minimal leakage current"

Conclusion

[0041] This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching.

Claims

1. A method of fabricating a III-Nitride based High Electron Mobility Transistor (30), comprising:

providing a substrate (32) capable of supporting growth of III-nitride materials;
providing a III-nitride barrier layer (38) on a III-nitride channel layer (36) on or above the substrate (32);
providing a group III-nitride semiconductor spacer layer (40) directly on the barrier layer (38);
providing an opening in the group III-nitride semiconductor spacer layer for a gate contact (46);
depositing the gate contact (46) in the opening such that the bottom of the gate contact is directly on the barrier layer (38);
providing a source contact (42) in direct contact with the channel layer (36) and a drain contact (44) in direct contact with the channel layer (36), wherein the source (42) and drain (44) contacts make ohmic contact through the barrier layer (38) such that an electric current flows between the source and drain electrodes via a two-dimensional electron gas (2DEG) induced at the heterointerface between the channel layer (36) and barrier layer (38) when the gate contact (46) is biased at an appropriate level;
creating at least one field plate (48) on and in direct contact with the group III-nitride semiconductor spacer layer (40), wherein the field plate is a top of the gate contact (46) and is formed from the gate material extending across the group III-nitride semiconductor spacer layer (40)

such that it extends a distance Lf from an edge of the gate contact (46) towards the drain contact (44); and

covering the field plate (48) and group III-nitride semiconductor spacer layer (40) with a dielectric passivation layer (50) so that the passivation layer is in direct contact with the field plate (48) and group III-nitride semiconductor spacer layer (40); and

wherein the group III-nitride semiconductor spacer layer (40) is in direct contact with the barrier layer (38) across the entire length between the source contact (42) and the gate (46) and across the entire length between the drain contact (44) and the gate (46).

2. The method according to claim 1, wherein the channel layer (36) comprises $Al_xGayIn_{(1-x-y)}N$ (0<=x<=1, 0<=y<=1, x+y<=1) and the barrier layer (38) comprises $Al_xGa_{1-x}N$ (0<=x<=1).

3. A III-nitride based High Electron Mobility Transistor device (30), comprising:

a substrate (32) capable of supporting growth of III-nitride materials;

a III-nitride barrier layer (38) on a III-nitride channel layer (36) on or above the substrate (32);

a group III-nitride semiconductor spacer layer (40) directly on the barrier layer (38);

an opening in the group III-nitride semiconductor spacer layer (40) for a gate contact (46);

the gate contact (46) in the opening, wherein the bottom of the gate contact is directly on the barrier layer (38);

a source contact (42) in direct contact with the channel layer (36) and a drain contact in direct contact with the channel layer (36);

a field plate (48) on and in direct contact with the group III-nitride semiconductor spacer layer (40), wherein the field plate (48) is a top of the gate contact (46) and is formed from the gate material extending across the group III-nitride semiconductor spacer layer (40) such that it extends a distance Lf from an edge of the gate contact (46) towards the drain contact (44);

a dielectric passivation layer (50) covering and in direct contact with the field plate (48) and group III-nitride semiconductor spacer layer (40); and

wherein the group III-nitride semiconductor spacer layer (40) is in direct contact with the barrier layer (38) across the entire length between the source contact (40) and the gate (46) and across the entire length between the drain contact (44) and the gate (46), and

the source (42) and drain (44) contacts make ohmic contact through the barrier layer (38) such that an electric current flows between the source and drain electrodes via a two-dimensional electron gas (2DEG) induced at the heterointerface between the channel layer (36) and barrier layer (38) when the gate contact (46) is biased at an appropriate level.

4. The HEMT according to claim 3, wherein the channel layer (36) comprises $Al_xGayIn_{(1-x-y)}N$ (0<=x<=1, 0<=y<=1, x+y<=1) and the barrier layer (38) comprises $Al_xGa_{1-x}N$ (0<=x<=1).

Patentansprüche

1. Verfahren zur Herstellung eines III-Nitrid-basierten Transistors mit hoher Elektronenbeweglichkeit (30), umfassend:

Bereitstellen eines Substrats (32), das geeignet ist, das Wachstum von III-Nitrid-Materialien zu fördern;

Bereitstellen einer III-Nitrid-Barriereschicht (38) auf einer III-Nitrid-Kanalschicht (36) auf dem oder oberhalb des Substrats (32);

Bereitstellen einer Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) unmittelbar auf der Barriereschicht (38);

Bereitstellen einer Öffnung in der Gruppe-III-Nitrid-Halbleiterabstandshalterschicht für einen Gate-Kontakt (46);

Abscheiden des Gate-Kontakts (46) in der Öffnung derart, dass die Unterseite des Gate-Kontakts unmittelbar auf der Barriereschicht (38) angeordnet ist;

Bereitstellen eines Source-Kontakts (42) in unmittelbarem Kontakt mit der Kanalschicht (36), und eines Drain-Kontakts (44) in unmittelbarem Kontakt mit der Kanalschicht (36), wobei die Source- (42) und die Drain- (44) Kontakte durch die Barriereschicht (38) einen Ohmschen Kontakt derart herstellen, dass zwischen der Source- und der Drain-Elektrode über ein zweidimensionales Elektronengas (2DEG) ein elektrischer Strom fließt, das an der Hetero-Grenzfläche zwischen der Kanalschicht (36) und der Barriereschicht (38) dann erzeugt wird, wenn der Gate-Kontakt (46) in angemessener Höhe vorgespannt ist;

Erzeugen mindestens einer Feldplatte (48) auf und in unmittelbarem Kontakt mit der Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40), wobei die Feldplatte eine Oberseite des Gate-Kontakts (46) ist und aus dem Gate-Material gebildet ist, das sich über die Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) derart erstreckt, dass es sich entlang eines Abstands Lf von einer Kante des Gate-Kontakts (46) zum

Drain-Kontakt (44) hin erstreckt; und
Abdecken der Feldplatte (48) und der Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) mit einer dielektrischen Passivierungsschicht (50) derart, dass die Passivierungsschicht in unmittelbarem Kontakt mit der Feldplatte (48) und der Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) ist; und
wobei die Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) über die gesamte Länge zwischen dem Source-Kontakt (42) und dem Gate (46), und über die gesamte Länge zwischen dem Drain-Kontakt (44) und dem Gate (46) in unmittelbarem Kontakt mit der Barriereschicht (38) ist.

2. Verfahren gemäß Anspruch 1, wobei die Kanalschicht (36) $Al_xGa_yIn_{(1-x-y)}N(0<=x<=1, 0<=y<=1, x+y<=1)$ umfasst, und die Barriereschicht (38) $Al_xGa_{1-x}N(0<=x<=1)$ umfasst.

3. III-Nitrid-basierter Transistor mit hoher Elektronenbeweglichkeit (30), umfassend:

ein Substrat (32), das geeignet ist, das Wachstum von III-Nitrid-Materialien zu fördern;
eine III-Nitrid-Barriereschicht (38) auf einer III-Nitrid-Kanalschicht (36) auf dem oder oberhalb des Substrats (32);
eine Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) unmittelbar auf der Barriereschicht (38);
eine Öffnung in der Gruppe-III-Nitrid-Halbleiterabstandshalterschicht für einen Gate-Kontakt (46);
den Gate-Kontakt (46) in der Öffnung, wobei die Unterseite des Gate-Kontakts unmittelbar auf der Barriereschicht (38) angeordnet ist;
einen Source-Kontakt (42) in unmittelbarem Kontakt mit der Kanalschicht (36) und einen Drain-Kontakt in unmittelbarem Kontakt mit der Kanalschicht (36);
eine Feldplatte (48) auf und in unmittelbarem Kontakt mit der Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40), wobei die Feldplatte (48) eine Oberseite des Gate-Kontakts (46) ist und aus dem Gate-Material gebildet ist, das sich über die Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) derart erstreckt, dass es sich in einem Abstand Lf von einer Kante des Gate-Kontakts (46) zum Drain-Kontakt (44) hin erstreckt;
eine dielektrische Passivierungsschicht (50), welche die Feldplatte (48) und die Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) abdeckt und in unmittelbarem Kontakt mit dieser ist; und
wobei die Gruppe-III-Nitrid-Halbleiterabstandshalterschicht (40) über die gesamte Länge zwischen dem Source-Kontakt (40) und dem Gate (46), und über die gesamte Länge zwischen dem Drain-Kontakt (44) und dem Gate (46) in unmittelbarem Kontakt mit der Barriereschicht (38) ist, und
wobei der Source- (42) und der Drain- (44) Kontakt durch die Barriereschicht (38) Ohmschen Kontakt derart herstellen, dass zwischen der Source- und der Drain-Elektrode über ein zweidimensionales Elektronengas (2DEG) ein elektrischer Strom fließt, das an der Hetero-Grenzfläche zwischen der Kanalschicht (36) und der Barriereschicht (38) erzeugt wird, wenn der Gate-Kontakt (46) in angemessener Höhe vorgespannt ist.

4. HEMT gemäß Anspruch 3, wobei die Kanalschicht (36) $Al_xGa_yIn_{(1-x-y)}N(0<=x<=1, 0<=y<=1, x+y<=1)$ umfasst, und die Barriereschicht (38) $Al_xGa_{1-x}N(0<=x<=1)$ umfasst.

Revendications

1. Procédé de fabrication d'un transistor à haute mobilité d'électrons à base de nitrure III (30), comprenant :

la fourniture d'un substrat (32) apte à soutenir la croissance de matériaux à base de nitrure III ;
la fourniture d'une couche barrière de nitrure III (38) sur une couche canal de nitrure III (36) sur le substrat (32) ou au-dessus de celui-ci ;
la fourniture d'une couche d'espacement semi-conductrice de nitrure du groupe III (40) directement sur la couche barrière (38) ;
la fourniture d'une ouverture dans la couche d'espacement semi-conductrice de nitrure du groupe III pour un contact de grille (46) ;
le dépôt du contact de grille (46) dans l'ouverture de sorte que la partie inférieure du contact de grille se trouve directement sur la couche barrière (38) ;
la fourniture d'un contact de source (42) en contact direct avec la couche canal (36) et d'un contact de drain (44) en contact direct avec la couche canal (36), les contacts de source (42) et de drain (44) étant en contact ohmique au travers de la couche barrière (38) de sorte qu'un courant électrique circule entre les électrodes de source et de drain via un gaz d'électrons bidimensionnel (2DEG) induit au niveau de l'hétéro-interface entre la couche canal (36) et la couche barrière (38) lorsque le contact de grille (46) est polarisé à un niveau approprié ;
la création d'au moins une plaque de champ (48) sur la couche d'espacement semi-conductrice

de nitrure du groupe III (40) et en contact direct avec celle-ci, la plaque de champ étant une partie supérieure du contact de grille (46) et étant formée à partir du matériau de grille s'étendant à travers la couche d'espacement semi-conductrice de nitrure du groupe III (40) de manière à s'étendre à une distance Lf d'un bord du contact de grille (46) vers le contact de drain (44) ; et
la couverture de la plaque de champ (48) et de la couche d'espacement semi-conductrice de nitrure du groupe III (40) avec une couche de passivation diélectrique (50) de sorte que la couche de passivation soit en contact direct avec la plaque de champ (48) et la couche d'espacement semi-conductrice de nitrure du groupe III (40) ; et
dans lequel la couche d'espacement semi-conductrice de nitrure du groupe III (40) est en contact direct avec la couche barrière (38) sur toute la longueur entre le contact de source (42) et la grille (46) et sur toute la longueur entre le contact de drain (44) et la grille (46).

2. Procédé selon la revendication 1, dans lequel la couche canal (36) comprend $Al_xGa_yIn_{(1-x-y)}N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$) et la couche barrière (38) comprend $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$).

3. Transistor à haute mobilité d'électrons à base de nitrure III (30), comprenant :

un substrat (32) apte à soutenir la croissance de matériaux à base de nitrure III ;
une couche barrière de nitrure III (38) sur une couche canal de nitrure III (36) sur le substrat (32) ou au-dessus de celui-ci ;
une couche d'espacement semi-conductrice de nitrure du groupe III (40) directement sur la couche barrière (38) ;
une ouverture dans la couche d'espacement semi-conductrice de nitrure du groupe III (40) pour un contact de grille (46);
le contact de grille (46) dans l'ouverture, la partie inférieure du contact de grille se trouvant directement sur la couche barrière (38) ;
un contact de source (42) en contact direct avec la couche canal (36) et un contact de drain en contact direct avec la couche canal (36) ;
une plaque de champ (48) sur la couche d'espacement semi-conductrice de nitrure du groupe III (40) et en contact direct avec celle-ci, la plaque de champ étant une partie supérieure du contact de grille (46) et étant formée à partir du matériau de grille s'étendant à travers la couche d'espacement semi-conductrice de nitrure du groupe III (40) de manière à s'étendre à une distance Lf d'un bord du contact de grille (46) vers le contact de drain (44) ;
une couche de passivation diélectrique (50) couvrant la plaque de champ (48) et la couche d'espacement semi-conductrice de nitrure du groupe III (40) et en contact direct avec celles-ci ; et
dans lequel la couche d'espacement semi-conductrice de nitrure du groupe III (40) est en contact direct avec la couche barrière (38) sur toute la longueur entre le contact de source (42) et la grille (46) et sur toute la longueur entre le contact de drain (44) et la grille (46), et
les contacts de source (42) et de drain (44) sont en contact ohmique au travers de la couche barrière (38) de sorte qu'un courant électrique circule entre les électrodes de source et de drain via un gaz d'électrons bidimensionnel (2DEG) induit au niveau de l'hétéro-interface entre la couche canal (36) et la couche barrière (38) lorsque le contact de grille (46) est polarisé à un niveau approprié.

4. Transistor HEMT selon la revendication 3, dans lequel la couche canal (36) comprend $Al_xGa_yIn_{(1-x-y)}N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$) et la couche barrière (38) comprend $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$).

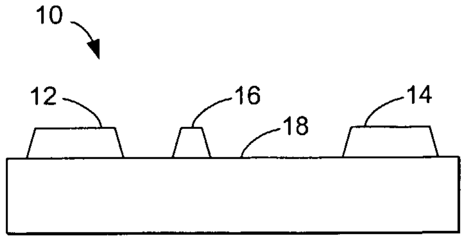

FIG. 1A

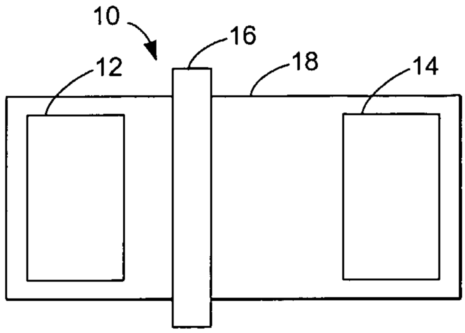

FIG. 1B

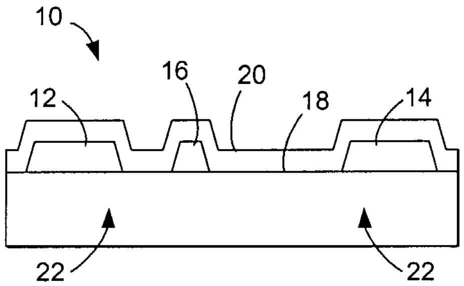

FIG. 2A

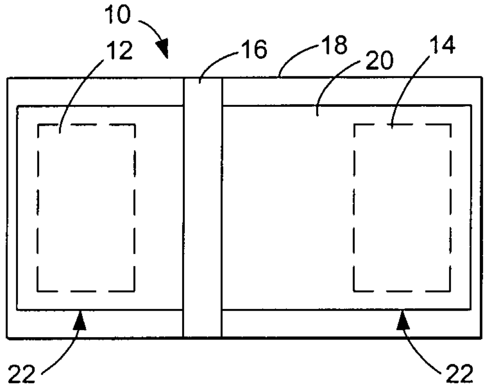

FIG. 2B

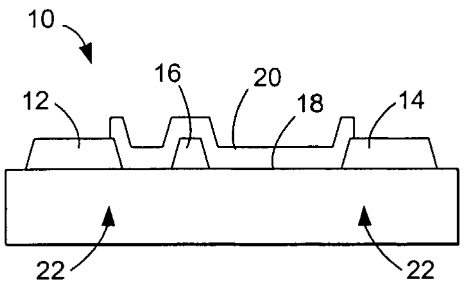

FIG. 3A

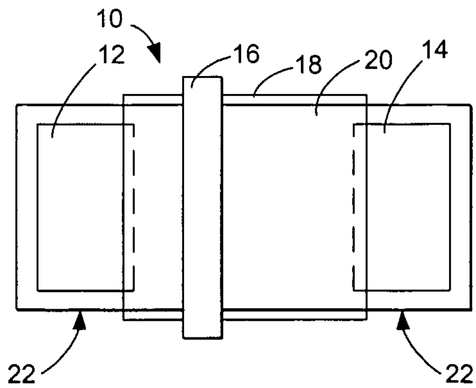

FIG. 3B

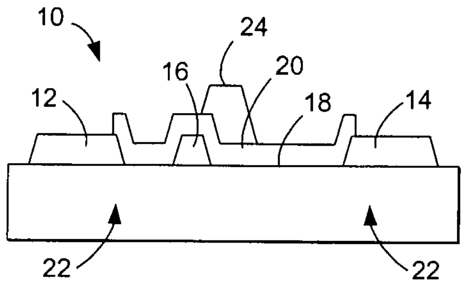

FIG. 4A

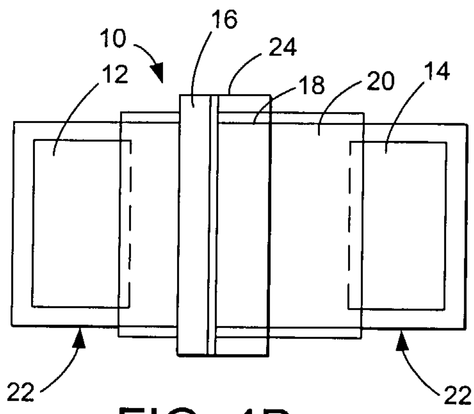

FIG. 4B

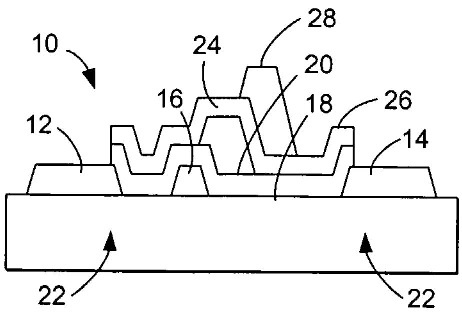

FIG. 5A

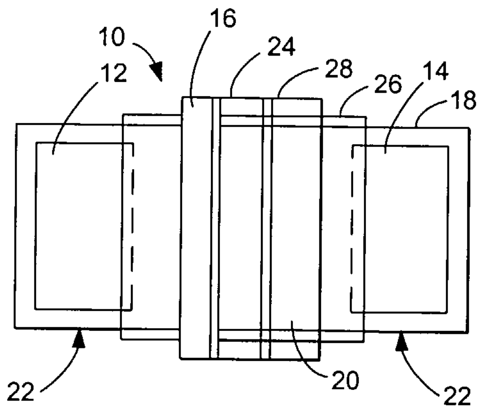

FIG. 5B

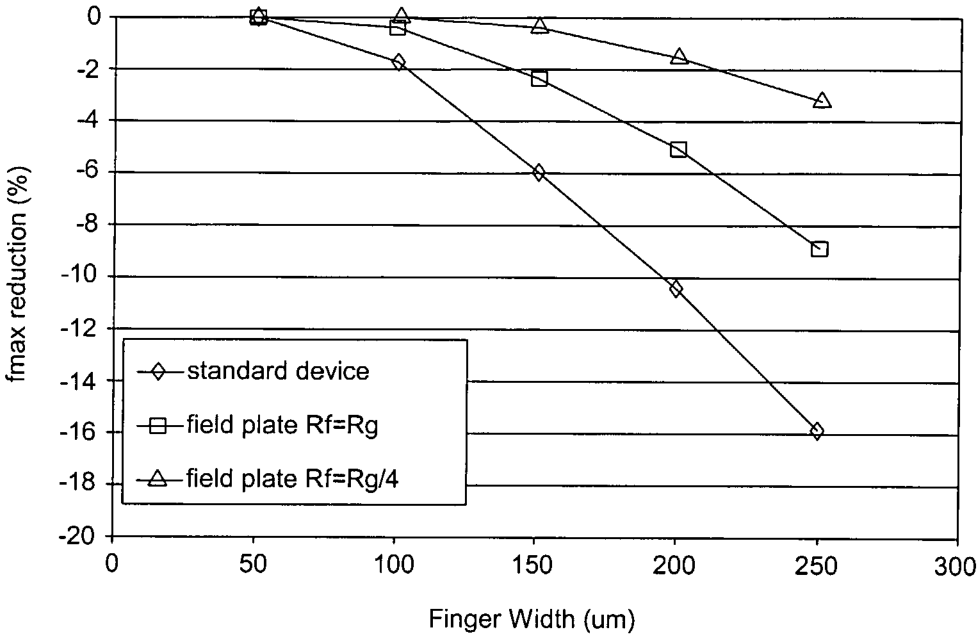

FIG. 6

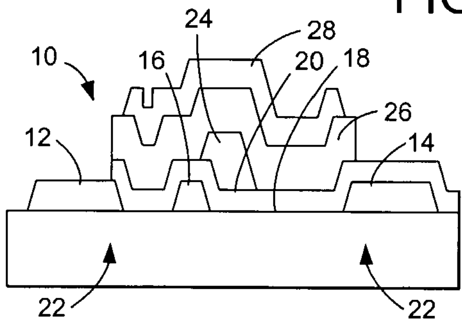

FIG. 7A

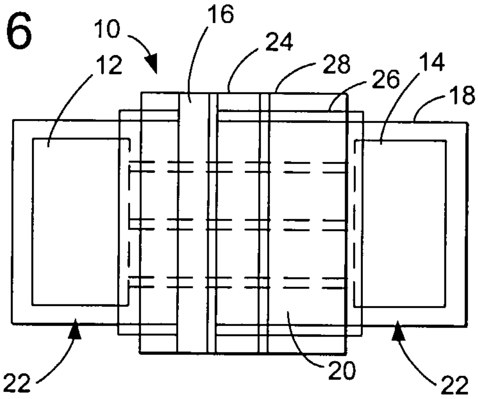

FIG. 7B

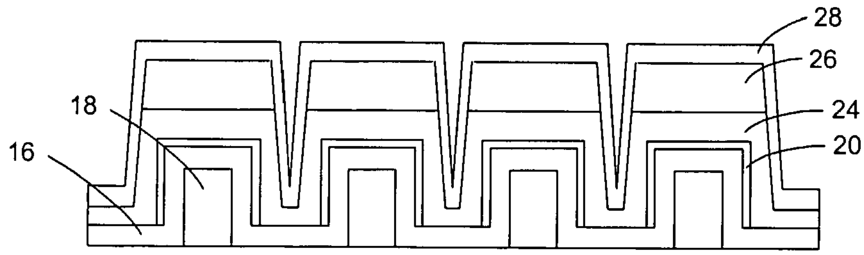

FIG. 7C

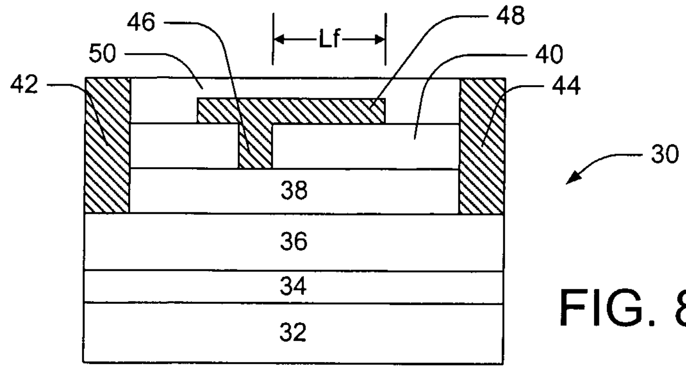

FIG. 8

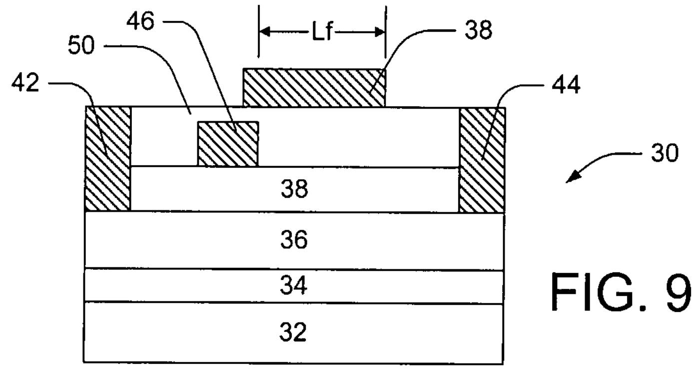

FIG. 9

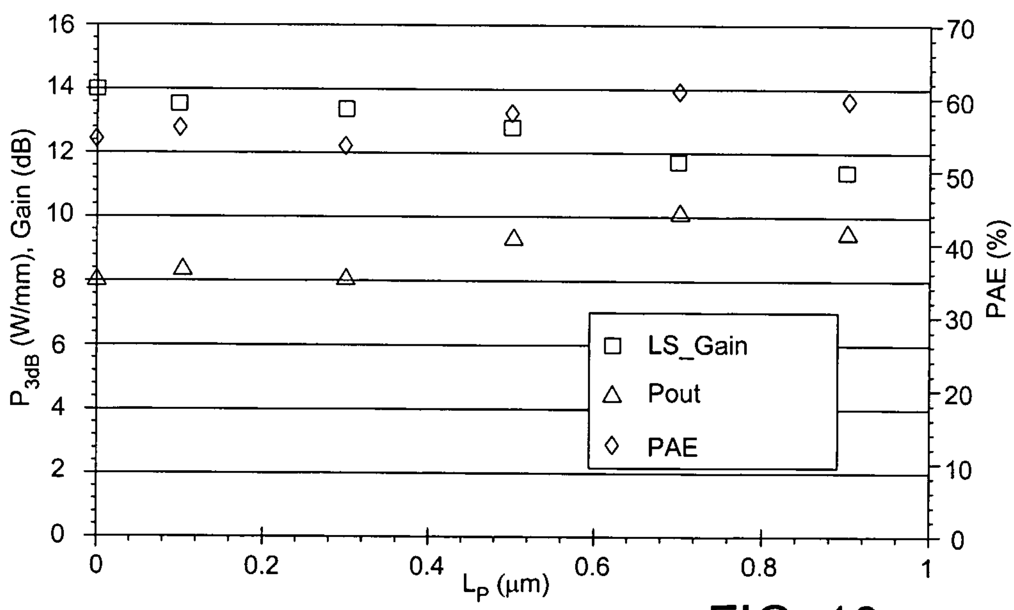

FIG. 10

REFERENCES CITED IN THE DESCRIPTION

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